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Implications of Ageing through Power Cycling on the Short Circuit Robustness of 1.2-kV SiC MOSFETs

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***Abstract*—In this paper, the reliability performance of 1.2-kV SiC power MOSFET modules is investigated through the combination of both accelerated power cycling tests and short circuit tests. The short-circuit robustness of SiC MOSFETs is investigated after stressing the dies under power cycling tests. In this way, the implications of different levels of degradation on the short circuit capability can be better understood. During the power cycling tests, some electrical parameters, either related to the package or the die, may experience variations as a consequence of the device ageing (e.g., increase in bond wire resistance and increase in gate leakage current). The effect of these parameter variations on the short-circuit withstanding capability of SiC MOSFETs is investigated for the first time in this work. The proposed method helps to understand which degradation effects under normal operation have a major implication on the short-circuit robustness, which gives a more realistic information about the root cause of the failures observed in the field.**

***Index Terms*—SiC MOSFET, short circuit, accelerated power cycling tests, aging indicators, thermal cycling, Kelvin terminal, gate-oxide, reliability, power semiconductor device.**

I. INTRODUCTION

The reliability prediction of power converters has been a major research topic in the last decades with the aim of considering this factor in the Design for Reliability (DfR) phase of power electronic systems [1]. Several methods have been proposed to estimate the lifetime of power semiconductor devices, however, the available methods are now outdated, especially for modern power applications, where SiC MOSFETs are starting to be implemented. The Military standard -217F [2] based on constant failure rate models was widely used to predict the lifetime of the components, which is now obsoleted since 1995, but an updated version (Military-Handbook-217H) is still used [3]. The FIDES methodology is based on physics-of-failure models and supported by the analysis of different stresses such as temperature and humidity from the field returns, however, the models are generic and limited to a few number of components [4]. Furthermore, the device manufactures have proposed reliability models based on accelerated aging tests, such as power cycling [5] and temperature cycling under constant load profiles [6], neglecting the real mission profile. As a consequence, many reliability engineers are in need to run power cycling tests at different operating conditions (t_{on}, I_{load}, T_j, and ΔT_j) [7]–[11]. With

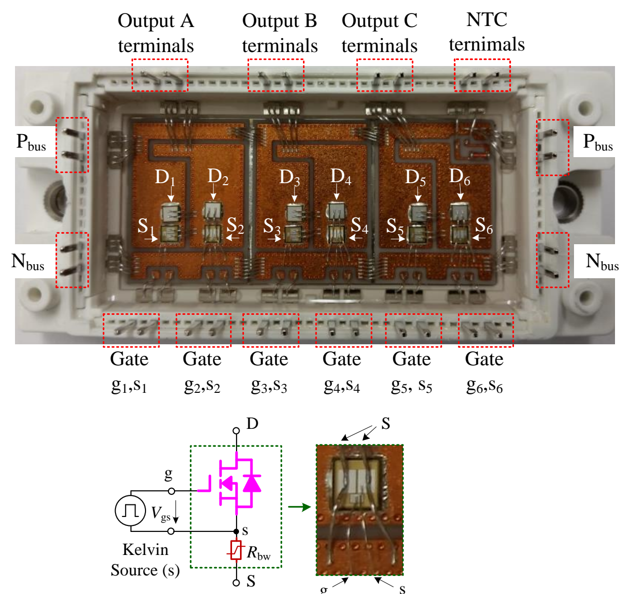

Fig. 1. A view of the 1.2-kV/ 20-A SiC power MOSFET module showing the Kelvin-source terminal and its equivalent circuit.

the results from these tests, it is possible to estimate the lifetime of the component based on the application requirements and the type of power semiconductor package (i.e. gel-filled [6], molded modules [8], single or multi-chip modules [11]). A more accurate reliability estimation method for power semiconductors are those approaches taking into account the mission profiles (i.e., wind speed, ambient temperature, solar irradiance, etc) [12]–[14], in order to estimate the real thermo-mechanical stress at the solder layer or bond wire interface [15]. Another approach that is nowadays gaining popularity is to use online condition monitoring parameters, such as the die forward voltage or bond wire voltage, as an indicator for the Remaining Useful Life (RUL) [16]–[18]. However, the increasing trend of the forward voltage with the number of cycles is not yet well understood and it varies from one device to another. Among the discussed reliability methods, though, there is one aspect that has been neglected in all of them; i.e. the effect of abnormal events, in particular short circuits, on the lifetime estimation of the power semiconductor.

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Over the years, the reliability of power semiconductors has been assessed either by running power cycling tests or by performing repetitive short circuit testing to induce failure mechanisms and detect failure indicators that could anticipate the catastrophic failure of the device. Most of the experimental activities related to both power cycling and repetitive short circuit have been done for silicon IGBTs [6]–[8], [12], [14], [17], describing various failure types (i.e., bond wire lift off [6], solder degradation [19], metallization reconstruction [20]) and their indicators (i.e., on-state voltage increase, gate-emitter threshold voltage shifts, junction temperature increase and gate-leakage current incraese) [21]. On the other hand, a few data can be found for SiC MOSFETs stressed under power cycling tests [11], [22], [23], thermal cycling tests [24] or repetitive short circuit tests [25]–[28]. These studies have been focused on performing short-circuit tests and/or repetitive short-circuit tests on fresh devices, without taking into account that the short-circuit robustness of a semiconductor device could be quite different as the device degrades. The novelty of this paper is the study of the short-circuit robustness of a commercial silicon carbide MOSFET power module when the semiconductor device shows different levels of degradations after power cycling tests. The final goal is to compare the implications of a short circuit on a non-degraded SiC MOSFET and a degraded one, which gives a more realistic information about the effect of a short circuit when the device is operating in the field. This information can be useful to estimate the lifetime of power semiconductor devices.

This paper is organized as follows: Section II presents the results from the accelerated power cycling tests on the SiC MOSFETs showing different degradation levels. Section III demonstrates the implication of a short circuit event on the selected SiC MOSFETs having different degradation levels after the accelerated power cycling tests. Section IV discusses the types of degradations observed in SiC MOSFETs after power cycling tests and the effect of this degradation on the SiC MOSFET short-circuit capability. Finally, concluding remarks are given.

II. Accelerated Cycling Tests

A. Device Under Test

A commercial 1.2-kV/ 20-A SiC power MOSFET module has been selected as the device under test. This module is a six-pack (three-phase) SiC power MOSFET module which is typically used in solar inverters, motor drives and UPS systems. As it can be observed in Fig. 1, there are four power terminals for the positive bus connection (P_{bus}), four power terminals for the negative bus connection (N_{bus}) and six terminals corresponding to the three output phases (Output A, Output B and Output C). Additionally, there are six gate terminals denoted as g-s (gate-source) (bottom of Fig.1). The module has three Direct Bond Copper (DBC) substrates; each section contains two SiC MOSFETs and two freewheeling diodes which are configured as a phase leg. The upper-side SiC MOSFETs are named as S_1, S_3 and S_5 and the lower-side devices are named as S_2, S_4 and S_6. The monitoring of die voltage and bond wire voltage is possible since the DUT has a Kelvin-source terminal. The Kelvin-source terminal can be clearly observed in Fig. 1 with the additional bond wire from the die's emitter to the gate return path (s).

B. DC-based power cycling setup

The principle of the DC-based cycling setup is to stress the device under repeated thermal cycling, where the desired junction temperature swing (ΔT_j) is controlled by adjusting the t_{on}/t_{off} durations and the load current. The schematic diagram of the experimental test bench is shown in Fig. 2 and the picture of the test bench is presented in Fig. 3 . The tester includes a DC current generator (DELTA SM 45-140) providing the load current flowing through each device, three Intelligent Power Modules (IPMs) switches operated in interleaved mode with 1 ms overlap to control the load current, a cooling/heating system (Julabo A40) to ensure that the heatsink temperature is kept constant during the test, an optical fiber condition unit (Opsens), six isolated optical fibers (OTG-F-10) to monitor the junction temperature, and a measurement board to monitor both the die's on-state voltage drop and the bond wire voltage drop, which has been previously described in [29]. A Field-Programmable Gate Array (FPGA) provides the driving signals for the DUTs and the IPM switches. Since the SiC dies have different static characteristics, six independent commercial SiC MOSFET gate drivers (CREE CRD-001) with adjustable output voltages are used to ensure that the devices are always in on-state. Each device operates under the same stress, because the small variations in threshold voltage can be counteracted by applying different gate-source voltages with independent gate drivers. During the tests, the drain current, gate voltage, on-state voltage, bond wire voltage and junction temperature are acquired and stored by means of a Personal Computer (PC).

The selected test conditions for the power cycling tests are the following: a constant current of 12 A is injected sequentially through each MOSFET for a period of 2 seconds and then a cooling period of 4 seconds is selected. The heatsink temperature has been set to 55°C and the maximum junction temperature at the initial conditions was 125°C, with a junction temperature variation of 60°C. A relatively low positive gate voltage of 8 V has been selected to increase the power losses and achieve a reasonable junction temperature variation of 60°C. The selection of a low gate voltage has also the benefit of minimizing the trapping effects at the Si/SiO_2 oxide interface, which results in an undesired shift of the thermal stress ΔT_j, as discussed in [22]. The power cycling parameters are summarized in Table I.

C. Power Cycling Experimental Results

The performance of the 1.2-kV/ 20-A SiC power MOSFET module has been evaluated in a DC-based power cycling tester. Figure 4 shows the evolution of the on-state die resistance (R_{die}) and bond wire resistance (R_{bw}) with the number of cycles for the six SiC MOSFETs inside the power module. The bond wire resistance increases gradually for the six devices, with the difference that some of the SiC MOSFETs show a positive step in the resistance value; for example device S_5

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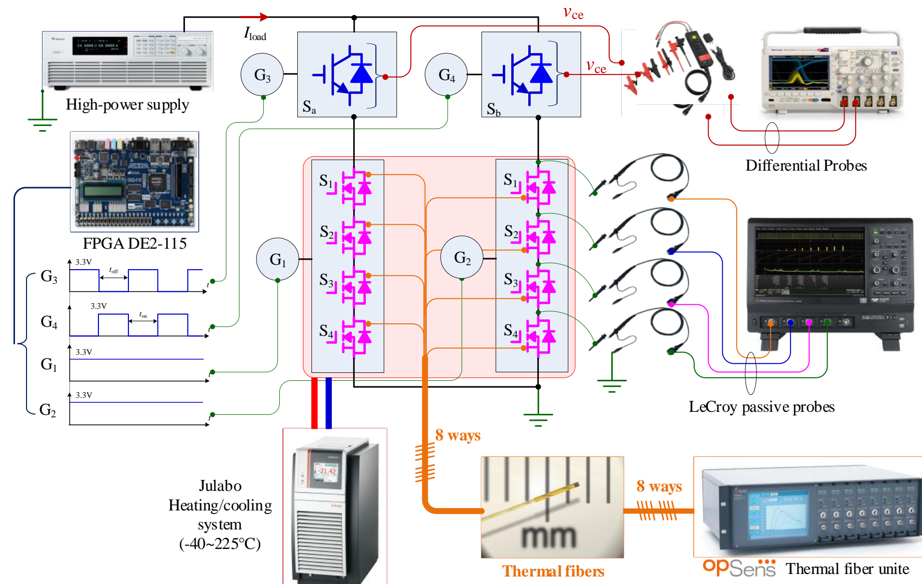

Fig. 2. Schematic diagram of the DC-based power cycling test platform.

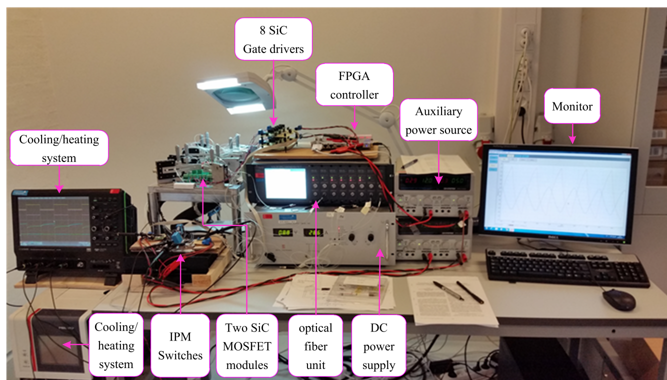

Fig. 3. Picture of the DC-based power cycling test platform.

TABLE I
POWER CYCLING TESTS PARAMETERS

Parameters	Value
Load current	12 A
Heatsink temperature	55 °C
Maximum T_j	125 °C
ΔT_j	60 °C
Pulse duration (t_{on})	2 s
Pulse duration (t_{off})	4 s
Gate voltage	8 V

shows a step in resistance increase at 20,000 cycles, device S_1 at 50,000 cycles and device S_4 at 60,000 cycles. It is worth to mention that after the test, the bond wires were still connected to the SiC MOSFETs. This demonstrates that the sharp increase in bond wire resistance does not necessarily imply that the bond wires lift off from the dies, alternatively, this trend indicates that the interface between the bond wire and the chip is degrading (i.e., crack formation). A deeper understanding of the bond-wire degradation mechanism can be made from the experimental results, where the high-side devices degrade faster than the lower side devices. The observed difference in respect to the bond wire degradation is related to the asymmetrical internal layout of the SiC power MOSFET module, as observed in Fig. 1. The high-side devices (i.e., S_1, S_3 and S_5) are mounted on DBC substrates having a smaller area than the low-side devices (i.e., S_2, S_4 and S_6). This leads to thermal impedance differences, as previously investigated in [30], where the devices mounted on a smaller DBC have a smaller heat spreading and therefore a larger thermal impedance. For the SiC power MOSFET module under investigation, the high-side SiC MOSFETs are expected to have larger thermal impedances than the low-side devices, which means that the high-side chips are exposed to higher thermal loadings and therefore reduced lifetimes, as observed through the experiments.

The die resistance behaviour shows a gradual decrease with the number of cycles at the end of this test, however, if the SiC MOSFETs are power cycled until the bond-wire lift-off is observed, the die resistance will finally increase as previously observed in [23]. The goal of this experiment was not to fail the SiC MOSFET but to stop the test at about 50% of its end-of-life, with the aim of studying the implication of different degradation levels on the short-circuit capability of SiC MOSFETs.

Power cycling tests have been done in order to study the effect of a short-circuit event on a degraded SiC MOSFET, rather than applying a short circuit on a new device, as it is typically done. Because the device has been aged through power cycling tests, it is not supposed to operate as a fresh device, and therefore, the short-circuit robustness may be lower than expected. In order to evaluate the impact of a short

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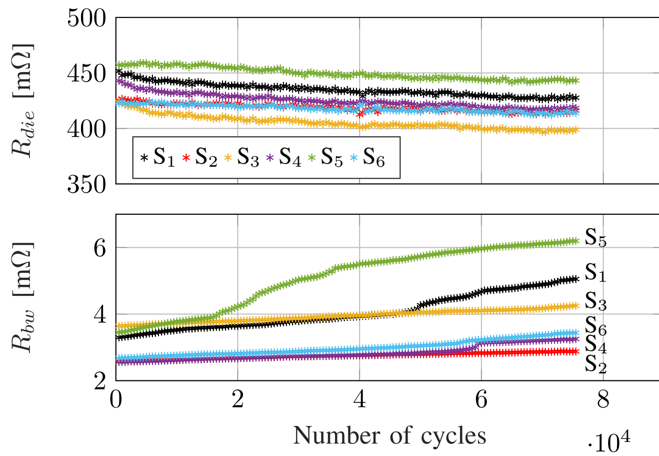

Fig. 4. Evolution of the die resistance R_{die} and bond wire resistance R_{bw} of the six SiC MOSFETs inside the 1.2kV/ 20-A power module throughout the power cycling test.

circuit on a degraded device and thereafter compare it to the short circuit robustness of a non-degraded device, the lower-side SiC MOSFETs, devices S_2, S_4 and S_6, have been further tested. The high-side devices show a larger degradation level, which could be considered as damaged devices, and therefore the argument to only test the low-side SiC MOSFETs. Among the low-side devices, different degradation levels are also observed. The evolution of the bond wire resistance in Fig. 4 shows an increasing trend with number of cycles, the percentage increase is 28% of its initial value for device S_6, 26% for device S_4 and 13% for device S_2. It can be concluded that S_6 device shows a more significant bond wire degradation than S_4 and S_2 devices. The impact of different degradation levels on the short-circuit robustness will be evaluated in the following.

The static characteristics have been measured before and after the tests by means of an Agilent B1506A power device analyzer at room temperature. The B1506A power device analyzer/curve tracer operates over a wide range up to 3-kV/ 1.5-kA, enabling the device characterization of medium-to high power modules in an automated way. This characterization is needed to find out which electrical parameters have shifted from their initial values due to the ageing of the device. Fig. 5 reveals the static transfer characteristic curve before and after the power cycling tests for the lower-side SiC MOSFETs . The following trends have been found:

- The threshold voltage (V_{th}) does not change.
- The drain current (I_D) decreases with increasing gate-source voltage.

It is important to point out that these trends differ from the aging phenomena typically observed in the literature after stressing the SiC MOSFETs through power cycling tests [27]. A threshold voltage shift has been found in most of the SiC MOSFETs [31] because the power cycling test were performed at the nominal on-state gate voltage, leading to trapping effects at the Si/SiO_2 and threshold voltage instabilities. In order to explain the two effects, the differences in the I_D-V_{GS} curve between the aging trends observed in the literature (i.e., V_{th}

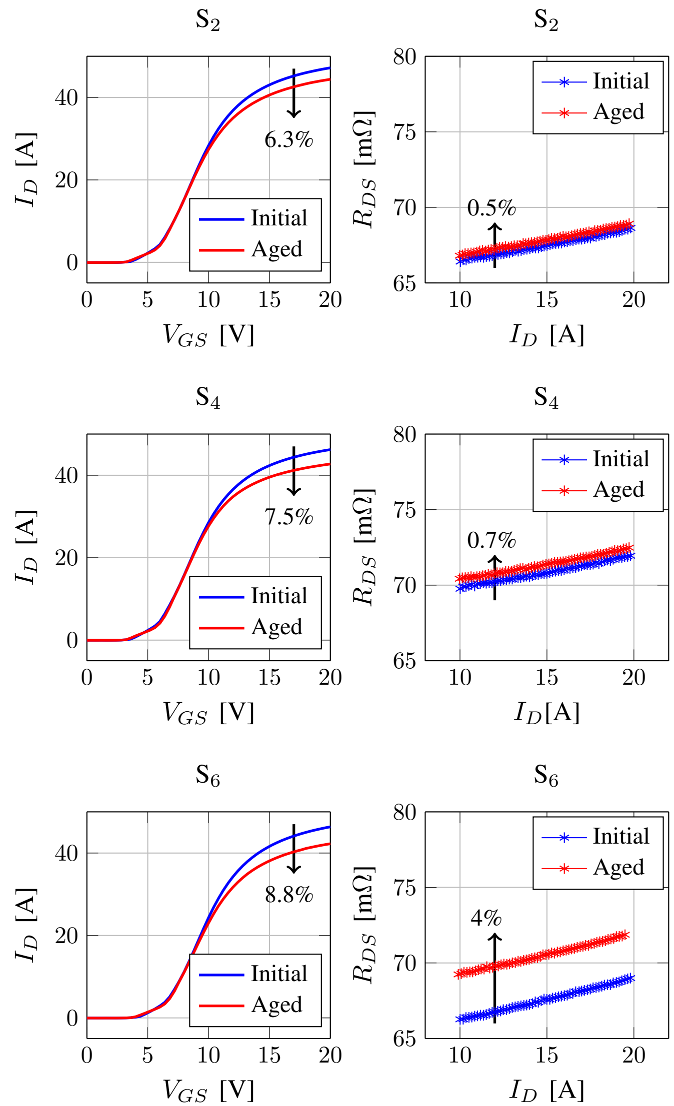

Fig. 5. Static transfer characteristics before and after power cycling tests.

Fig. 6. On-state resistance before and after power cycling tests.

shift and similar I_D) and the ones presented in this paper (i.e., same V_{th} and I_D reduction) are highlighted in Figs. 7a and 7b, respectively. Among other factors, the drain current can only decrease at a fixed drain-source voltage when the gate-source voltage is reduced or the threshold voltage positively increases. Since the threshold voltage does not change for the results presented in this work, the reduction of the drain current can only be due to the reduction of the gate bias voltage. This phenomenon has been previously pointed out in [27], [28], after stressing the SiC MOSFET through repetitive short circuit events. The short-circuit test eventually lead to gate-oxide instabilities resulting in a gate-leakage current increase and therefore gate bias voltage and drain current reduction. The typical I-V characteristics for device S_6, which is the one showing the largest degradation level, are plotted in Fig. 8, demonstrating that there is no obvious change in threshold voltage. The I-V characteristics at different V_{GS} for devices S_2 and S_4 show the same behavior and they are not included

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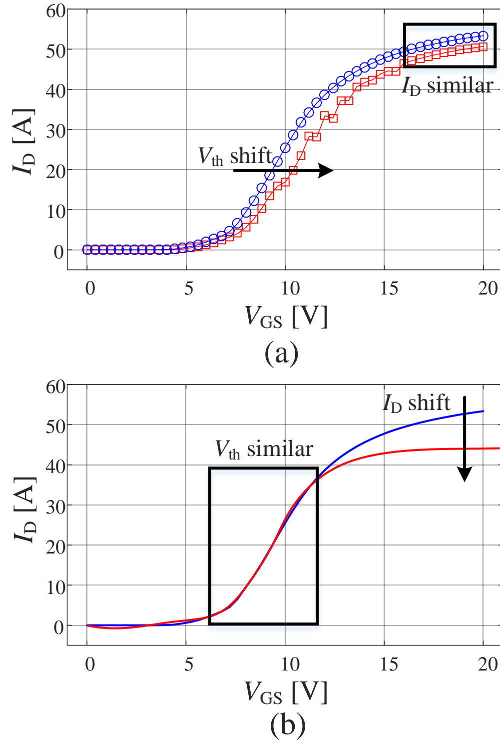

Fig. 7. The static output characteristic I_D-V_{GS} before and after power cycling tests: (a) trends observed when the positive gate voltage is 20 V [31] and, (b) trends observed when the positive gate voltage is 8 V (this work).

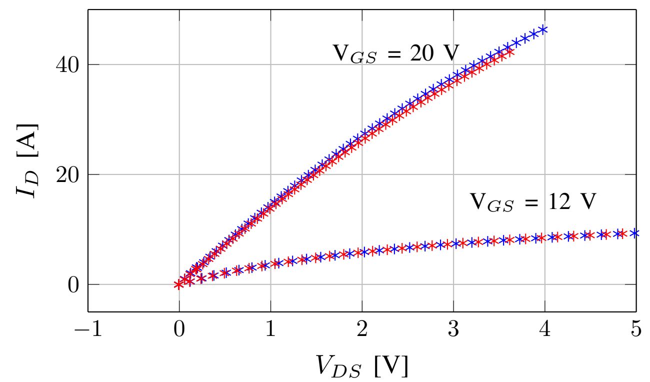

Fig. 8. Static I-V characteristics of device S_6 before and after power cycling tests.

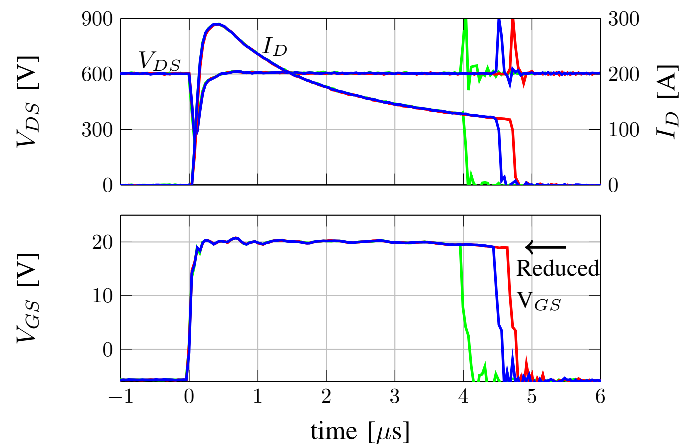

Fig. 9. Short-circuit performance of the non-degraded 1.2-kV/ 20-A SiC power MOSFET (S_4) with increasing short-circuit time. Testing conditions: V_{DC} = 600 V, V_{GS} = +20 V/ -5 V and T_j = 25°C.

in the paper.

Furthermore, the low-side SiC MOSFETs show slightly different degradation levels. For example in Fig. 5, the drain current reduction is about 6.3% from its initial value for device S_2, 7.5% for device S_4 and 8.8% for device S_6. Therefore, the SiC MOSFET S_6 shows a larger gate-oxide degradation than devices S_2 and S_4.

The on-state resistance has also been evaluated before and after the power cycling test in Fig. 6. The on-state resistance sums up to the die resistance, bond wire resistance, aluminium surface resistance and DBC resistance. The trends in Fig. 6 show that the on-state resistance increases with ageing, and once again, the device S_6 shows the largest parameter shift.

III. Short-Circuit Experimental Results

A. Short Circuit Test of a Non-Degraded SiC MOSFET

To understand which degradation effects under accelerated power cycling tests have a major implication on the short-circuit robustness of the 1.2-kV/ 20-A SiC power MOSFET module, short-circuit characterization was firstly carried out on a non-degraded SiC MOSFET. The short circuit tests have been performed with a 2.4-kV/ 10-kA Non-Destructive Tester (NDT) described in [32]. After setting up the experiment parameters (i.e., V_{DC} = 600 V and V_{GS} = +20 V/ -5 V), the low side SiC MOSFET S_4 was tested by increasing the short circuit pulse duration in steps of 0.1 μs until a clear degradation and/or failure occurred. Only one fresh SiC MOSFET has been tested to use it as a reference for later comparison. The waveforms sampled by the oscilloscope have been acquired at the end of every test, i.e., the drain-source voltage, V_{DS}, the drain current, I_D, and the gate-source voltage, V_{GS}. The acquired waveforms have been stored with the aim of monitoring the drain current and gate voltage tendencies with the increasing short-circuit time.

Fig. 9 shows that the non-degraded SiC MOSFET is capable of withstanding short-circuits under 600 V drain voltage and 25°C up to 4.9 μs. When the short-circuit test at t_{sc} = 4.9 μs has been performed, a reduction of the on-state gate voltage waveform with increasing short-circuit pulse duration is observed, which is an indicator that the gate leakage current increases [32], [33]. The next short-circuit test at t = 5 μs lead to gate-oxide breakdown failure, which is not shown in Fig. 9 for the sake of clarity. The gate voltage reduction typically leads to a permanent damage of the gate-oxide, whose indicator is the reduction of the bias gate voltage of about 1 V or 2 V. The V_{GS} reduction is selected as a failure criterion to determine the maximum short-circuit pulse duration of each device.

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B. Short Circuit Experimental Results After Power Cycling Degradation

During the accelerated power cycling tests, some electrical parameters, either package-related (i.e., bond wire resistance) or die-related (i.e., drain current decrease), have shifted from their initial value due to the ageing of the device. The purpose of this work is to experimentally demonstrate which degradation effects under accelerated power cycling tests have a major impact on the short-circuit robustness of SiC MOSFETs. To investigate the impact of different parameter variations, the low-side SiC dies, showing the lower degradation levels and therefore still functional, have been tested under the same short circuit test conditions. From the power cycling results, it has been observed in Fig. 4 that S_2 device shows the lowest degradation level followed by device S_4 and S_6.

The short-circuit behaviour of the single-chip SiC power MOSFET module has been experimentally investigated under the following conditions: V_{DC} = 600 V, V_{GS} = +20 V/ -5 V and initial junction temperature of 25°C. The maximum short-circuit withstanding capability has been determined by increasing the short-circuit pulse until a severe degradation is observed, for example the reduction of the on-state gate voltage waveform. Fig. 10 shows the short-circuit experimental results corresponding to device S_4 and after degrading the device through the accelerated power cycling tests. The gate voltage waveform shows a reduction of its on-state value for a short-circuit pulse duration of 4 μs, which serves as a failure indicator to determine the maximum short-circuit capability. This is a good method because the gate-oxide becomes permanently damaged and it is not fully isolated any more. It is important to note that the short-circuit withstanding capability of device S_4 is reduced when compared to the non-degraded SiC MOSFET, being the maximum short circuit time 4 μs for the aged device and 4.9 μs for the non-degraded device.

After each short circuit test, the power module was characterized by means of the Agilent B1506A power device analyzer at room temperature. Fig. 11 reveals the trend of the static electrical characteristics for two different short-circuit pulse lengths. The impact of the short-circuit pulse length is clearly visible on the I_D-V_{GS} curve, where a positive shift in the threshold voltage is observed. This phenomenon typically occurs in SiC MOSFETs due to weak gate-oxide reliability [25], [34]. The I_D-V_{DS} curve shows that the on-state resistance increases because of the threshold voltage shift. This parameter shift results in lower short-circuit energy generation but leads to increased power losses during normal operation.

Similarly as before, short circuit tests combined with static characterizations were carried out on the 1.2-kV/ 20-A SiC MOSFET for devices S_2 and S_6. The short circuit experimental results for device S_6 can be observed in Fig. 12 and the experiments for device S_2 are presented in Fig. 13. The I-V static characteristics for device S_6 can be observed in Fig. 14. The three devices behave very similar since the same electrical parameters have shifted with increasing short circuit time (i.e., threshold voltage and drain current reduction). The

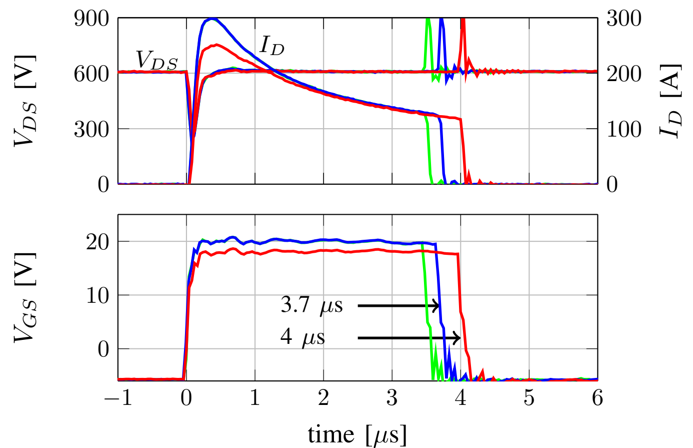

Fig. 10. Short-circuit tests of the 1.2-kV/ 20-A SiC power MOSFET (S_4) with increasing short-circuit time, after stressing the device through the accelerated power cycling tests. Testing conditions: V_{DC} = 600 V, V_{GS} = +20 V/ -5 V and T_j = 25°C.

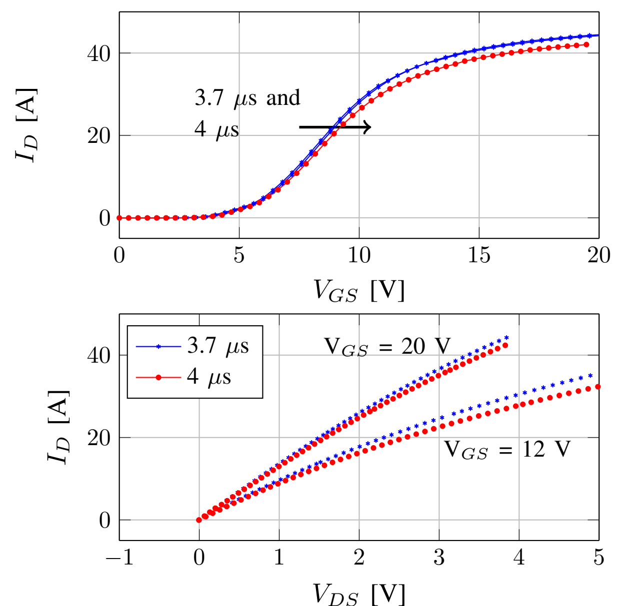

Fig. 11. I-V characteristics of the degraded 1.2-kV/ 20-A SiC power MOSFET S_4 along the short circuit tests.

aging indicator during short circuit was the reduction of the gate-source voltage, either from the beginning of the short circuit event (i.e., Fig. 10) or V_{GS} reduction with increasing short-circuit time (i.e., Figs. 12 and 13). This phenomenon eventually leads to a gate-oxide breakdown due to increased gate leakage current [35]. In the following, the maximum short-circuit time ($t_{sc,max}$) under a bias voltage of 600 V and initial junction temperature of 25°C is listed in Table II, showing that there is a correlation between the level of degradation and the short-circuit robustness.

IV. Impact of SiC MOSFET Degradation through Power Cycling on the Short-Circuit Robustness

The results from the accelerated power cycling tests indicate that there are two ageing indicators that change as a result

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TABLE II
MAXIMUM SHORT CIRCUIT TIME AFTER POWER CYCLING AGEING

SiC MOSFET	$t_{sc,max}$
Non-degraded S_4	4.9 μs
Power cycled S_2	4.2 μs
Power cycled S_4	4 μs
Power cycled S_6	3.9 μs

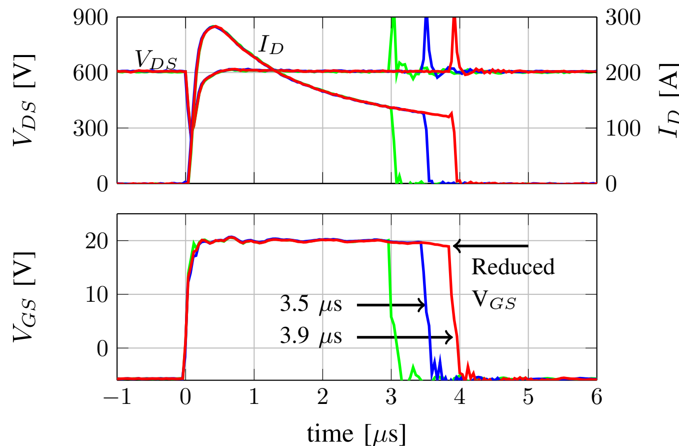

Fig. 12. Short-circuit tests of the 1.2-kV/ 20-A SiC power MOSFET (S_6) with increasing short-circuit time, after stressing the device through the accelerated power cycling tests. Testing conditions: V_{DC} = 600 V, V_{GS} = +20 V/ -5 V and T_j = 25°C.

of the SiC MOSFET degradation: (1) increase of bond wire resistance due to the repetitive thermo-mechanical stresses at the bond wire interconnection and (2) reduction in drain current at high V_{GS} (i.e., increase in gate leakage current), indicating gate-oxide weakness.

The effect of the increased bond wire resistance on the short-circuit robustness of the SiC MOSFET is illustrated in Fig. 15. In order to understand the implications of the bond wire ageing, the less degraded SiC MOSFET (i.e., device S_2

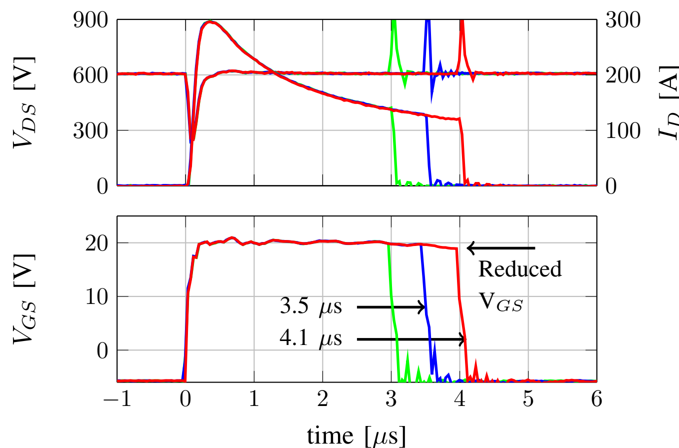

Fig. 13. Short-circuit tests of the 1.2-kV/ 20-A SiC power MOSFET (S_2) with increasing short-circuit time, after stressing the device through the accelerated power cycling tests. Testing conditions: V_{DC} = 600 V, V_{GS} = +20 V/ -5 V and T_j = 25°C.

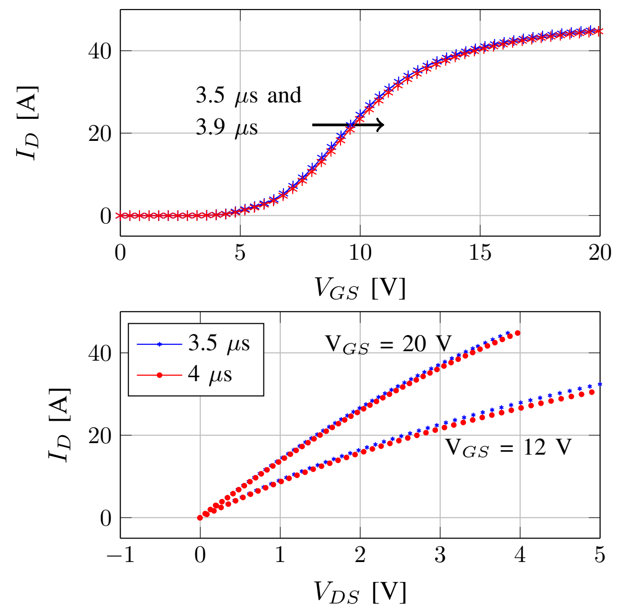

Fig. 14. IV characteristics of the degraded 1.2-kV/ 20-A SiC power MOSFET S_6 along the short circuit tests.

in Fig. 4) and the most degraded SiC MOSFET (i.e. device S_6 in Fig. 4) are considered as study cases. When a short circuit event occurs, the drain voltage is fixed by the DC bus voltage, which in this case is 600 V, and the drain current is limited by the MOSFET saturation region, whose values are 296 A for device S_2 and 283 A for device S_6. At the end of the power cycling tests, the bond wire resistance was 2.8 mΩ and 4.2 mΩ for devices S_2 and S_6, respectively. The difference in the resistance value leads to a voltage drop across the bond wire of 0.82 V and 1.18 V under a short circuit condition, for devices S_2 and S_6 respectively. With this simple calculation, it can be understood that the increased bond wire resistance has a negligible effect on the die's short circuit energy, and therefore, the junction temperature variation is expected to be similar for both devices. This means that the reduced short circuit capability of device S_6 with respect to device S_2 cannot be due to the degradation of the bond wires after the power cycling experiments.

The effect of the gate-oxide degradation through power cycling tests on the short-circuit robustness has a more important implication. Previous studies have shown that after performing accelerated power cycling tests, the threshold voltage V_{th} experiences a positive shift, as discussed in [11] and [22]. More in particular, the work presented in [23] presents accelerated power cycling tests until bond wire lift off is detected for the same part number as the SiC MOSFET studied in this paper. The evolution of the die resistance shows a negative trend in the first number of cycles but this trend becomes positive with increasing number of cycles, resulting in a threshold voltage positive shift [23]. The threshold voltage stability is affected by oxide-trap charging and oxide-trap activation, which becomes more critical with larger applied positive gate bias. In this work, the selected positive gate voltage was particularly low (i.e., V_{GS} = 8 V) with the aim of minimizing oxide-trap

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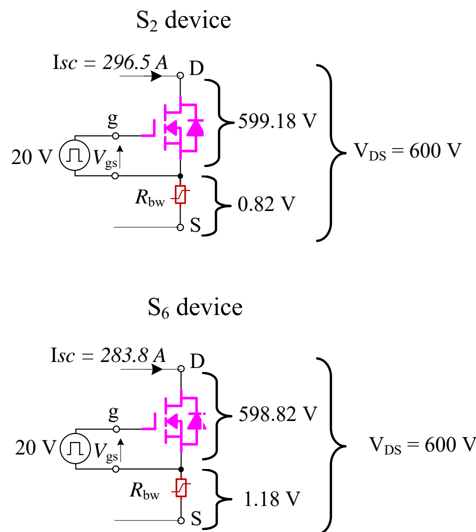

Fig. 15. Implications of the increased bond wire resistance through power cycling on the short-circuit behaviour.

mechanisms and reduce the impact of the temperature shift during the power cycling tests, as explained in [22]. After the power cycling experiments, which have been stopped at the 50% of its end-of-life, the threshold voltage does not show any change, however, the transfer characteristics in Fig. 5 indicate that the drain current decreases when the gate voltage is relatively high (i.e., from 10 V up to 20 V). To better understand this phenomenon, the expression of the drain current as a function of V_{GS} is reported below:

$$I_D = \mu_{n,channel} \frac{W}{L} \frac{C_{ox}}{2} \left[2(V_{GS} - V_{th})V_{DS} - V_{DS}^2 \right] \quad (1)$$

The drain current depends on the threshold voltage (V_{th}), channel mobility ($\mu_{n,channel}$), oxide capacitance (C_{ox}) and length (L), width (W) of the channel. However, none of these parameters drift from their initial values after the accelerated power cycling tests. One hypothesis to explain the reduction of drain current could be related to the increase in gate leakage current, which reduces the positive gate voltage and therefore the drain current. The existence of a current flowing through the gate indicates that the gate-oxide presents some resistive paths leading to the damage of the device. It is worth to note that the short circuit capability of the studied SiC MOSFET becomes weaker (i.e., the maximum short-circuit time is reduced) as higher drain current reduction is observed in the transfer characteristics in Fig. 5. The implication of decreased drain current through power cycling on the short-circuit behaviour is that the Si/SiO_2 interface is degraded and therefore the short-circuit robustness capability is lower.

V. Conclusions

This paper investigates the implications of the ageing through accelerated power cycling tests on the short circuit capability of SiC MOSFETs. The experimental results from the power cycling tests show that some of the electrical parameters have shifted from their initial value as a consequence of the device degradation. These parameters are package-related such as the increase in bond wire resistance and die-related such as the decrease in drain current at high gate bias voltages. The effect of the increased bond wire resistance on the short-circuit robustness of the SiC MOSFET has a minor implication since its variation barely affects the short-circuit energy. Furthermore, the SiC MOSFET has a Kelvin-source terminal for the connection to the gate terminal, which means that the bond wire voltage drop variation does not affect the gate voltage value.

On the other hand, the effect of the gate-oxide degradation through power cycling tests on the short-circuit robustness has a more important implication. The effect of the decreased drain current at high VGS on the short-circuit robustness of the SiC MOSFET is a more important implication because its variation implies trapping effects at the Si/SiO_2 interface leading to smaller short-circuit withstanding times. In this work, it has been discovered that the maximum short-circuit time is reduced due to the power cycling tests, resulting in gate-oxide breakdown, as higher drain current reduction is observed from the transfer characteristics. Therefore, one can conclude that the effect of ageing through power cycling on the short-circuit robustness in SiC MOSFETs is a lower gate-oxide reliability, resulting in reduced short-circuit capability.

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