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An Isolated Bidirectional Single-Stage Inverter Without Electrolytic Capacitor for Energy Storage Systems

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Abstract— **This paper presents a new Isolated Bidirectional Single-Stage Inverter (IBSSI) suitable for grid-connected Energy Storage Systems (ESSs). The IBSSI contains no electrolytic capacitor. Therefore, its reliability and lifetime are improved in comparison with well-known two-stage Voltage Source Inverters (VSIs) without increasing the converter cost. In the IBSSI, a High-Frequency Transformer (HFT) is used to isolate the Energy Storage Device (ESD) from the grid. In addition, an active snubber is used to suppress the voltage spikes caused by the leakage inductance of the HFT and improve the converter efficiency. Boosting capability with a high-voltage ratio is also provided by the IBSSI. In this paper, a novel switching algorithm based on Space Vector Modulation (SVM) is developed to maintain the volt-second balance on the HFT and generate three-phase balanced currents. The switching algorithm also provides soft switching conditions for the main switches, which are explained in the paper. Moreover, a single-loop control system is employed to regulate the input and output currents. The test results of 3 kW prototype with SiC power devices show that the IBSSI can inject/draw three-phase currents to/from the grid with a unity power factor and without using any ac current sensors in discharging/charging mode.**

Index Terms— **battery, bidirectional converter, energy storage system, grid-connected inverter, high-frequency isolation, reliability.**

I. INTRODUCTION

Grid-tied Energy Storage Systems (ESSs) are used along with renewable-energy sources to solve the intermittency problem and improve the peak load management [1]–[3]. Well-known two-stage Voltage Source Inverters (VSIs) are typically used for grid integration of Energy Storage Device (ESDs) [3]–[5]. However, the two-stage VSIs need bulky electrolytic capacitors, which restrict their lifetime and they are known as a cause of reliability reduction and inverter failure [6]–[9]. Several current-fed topologies with single-stage boosting capability have been presented in the papers which do not need electrolytic capacitors and they are preferred from the reliability viewpoint. In [10]–[19], single-stage three-phase current-fed topologies for photovoltaic and fuel cell applications have been explained. Moreover, different aspects of the single-stage current-fed structure such as switching pattern [10], control scheme [11], [12], increasing voltage boost ratio [13], reducing common mode currents [14], [16] and dynamic modeling and stability analysis [15], [18], [19] along with its advantages have been studied. Despite the benefits of this structure, it is not suitable for battery-based ESSs due to a unidirectional power flow characteristic. In [20]–[23] bidirectional current-fed topologies have been introduced, but none of them provide isolation between the dc input and the grid. Galvanic isolation is necessary for some applications, like grid-connected ESSs, for safety requirements and grounding the input dc source [4], [24]–[26]. In [27] a bidirectional three-phase converter with high-frequency isolation has been presented for ESSs. In this topology, shoot-through is possible in the low voltage side of the HFT. Also, due to the high ripple input current, a large input capacitor is required. Furthermore, the series connection of the HFT leakage inductance and the dc-link inductor in specific switching states and the resultant voltage spikes should be considered. Voltage spikes are known as a problem of isolated current-fed topologies such as current-fed push-pull structure. In order to suppress the voltage spikes and improve the efficiency of this type of converters, modified switching strategies have been presented in [28]–[30]. Also, active snubber circuits have been suggested to prevent the voltage spikes. In [31]–[34] the active clamp circuits have been introduced for current-fed dc/dc push-pull converters.

In this paper, a new Isolated Bidirectional Single-Stage Inverter (IBSSI) is presented. Having a bidirectional power flow path, high-frequency isolation, boosting capability with a high-voltage ratio, high reliability due to eliminating the electrolytic capacitors and single-stage energy transfer are the features of the IBSSI. In addition, an active snubber is used in the IBSSI to suppress the voltage spikes and improve the efficiency. A novel switching method to prevent the HFT saturation is also designed.

The rest of the paper is organized as follows: section II describes the configuration of the proposed topology. Section III introduces the switching algorithm, an active snubber design and soft switching conditions. In addition, different switching states in charging and discharging modes as well as the HFT waveforms are analyzed in this section. Section IV demonstrates the control strategy of the converter. Operation

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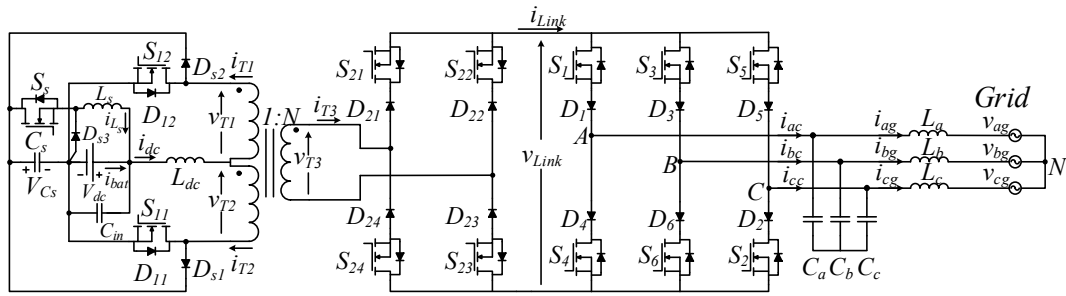
Fig. 1. The topology of the Isolated Bidirectional Single-Stage Inverter (IBSSI) with an energy storage device (V_{dc}).

of the IBSSI with the proposed control and switching methods is verified in section V.

II. PROPOSED TOPOLOGY

The IBSSI is shown in Fig. 1. As can be seen, the IBSSI contains no electrolytic capacitor. Also, an HFT facilitates achieving a high boost ratio and provides galvanic isolation between the ESD (V_{dc}) and the grid. Therefore, the IBSSI is suitable for grid integration of low voltage ESDs. In the IBSSI, the input dc inductor (L_{dc}) smoothen the current drawn from (injected to) the ESD. As demonstrated in Fig. 1, the active snubber circuit is a buck converter with two additional diodes D_{s1} and D_{s2}. In contrast to conventional buck converters, the role of the buck converter in the IBSSI is to regulate its input voltage (V_{C_s}) instead of the output voltage. The clamp capacitor (C_s) absorbs the stored energy in the leakage inductance of the HFT and suppresses the voltage spikes on the switches S_{11} and S_{12}. Therefore, the voltage across these switches is limited to the snubber capacitor voltage (V_{C_s}). Recycling the stored energy in the HFT leakage inductances by means of the active snubber improves the converter efficiency. The active snubber also provides open circuit protection for the converter. With respect to Fig. 1 and the protection provided by the active snubber, it can be seen that neither a shoot-through nor an open-circuit fault is possible in the IBSSI.

In comparison with a two-stage VSI containing an LCL output filter, the dc link capacitors and inverter-side filter inductors are eliminated in the IBSSI. The dc link capacitors and the output filter inductors are large components in the two-stage VSI. Therefore, eliminating them in the IBSSI leads to the reduction of the converter weight and required space. The additional weight and space due to the extra diodes in the IBSSI are not significant in comparison with the large inductors and bulky electrolytic capacitors in the VSI.

In the IBSSI, the high-frequency ripple currents of the output filter capacitors are high, while the required capacitance of them is low. Thus, it is possible to use MKP capacitors, which are able to withstand high ripple current and also have a long lifetime and a low failure rate.

III. MODULATION METHOD AND OPERATING MODES

A. Switching algorithm

The switching strategy is based on the SVM method [35]. With respect to this method, the active vectors and the reference current vector are demonstrated in Fig. 2. Also, the switching states of the IBSSI corresponding to each active vector are given in Table I. As can be seen, each active vector can be implemented by two switching states. The redundant switching states are used to balance the HFT volt-second product. Based on the phase angle of the reference current (θ_0), the appropriate sector and adjacent space vectors are identified. In Fig. 2, it is arbitrarily assumed that $\vec{I}_{ref}$ is located in the third sector. The reference current is then synthesized using a combination of selected space vectors (two active vectors followed by a zero vector) with specific dwell times. Calculation of the dwell times is based on the ampere-second balance principle, which can be formulated as:

$$T_s \vec{I}_{ref} = T_1 \vec{I}_3 + T_2 \vec{I}_4 + T_0 \vec{I}_0 \qquad (1)$$

$$T_s = T_1 + T_2 + T_0 \qquad (2)$$

Where T_s is the switching period and T_1, T_2 and T_0 are the dwell times for the nearby space vectors $\vec{I}_3$, $\vec{I}_4$ and $\vec{I}_0$, respectively. Substituting for current vectors in (1) and solving the resultant equations leads to:

$$T_1 = m T_s \sin(\frac{\pi}{3} - \delta), \quad 0 < \delta \le \frac{\pi}{3} \qquad (3)$$

$$T_2 = m T_s \sin(\delta), \quad 0 < \delta \le \frac{\pi}{3} \qquad (4)$$

$$T_0 = T_s \left(1 - m \sin(\delta + \frac{\pi}{3})\right), \quad 0 < \delta \le \frac{\pi}{3} \qquad (5)$$

The modulation index is defined as:

$$m = \frac{N |\vec{I}_{ref}|}{I_{dc}} \qquad (6)$$

Where N is the HFT turns ratio. In addition, due to the presence of L_{dc}, the overall boost ratio of the IBSSI is equal to $\frac{N}{1-D}$, where D can be defined as:

$$D = \frac{T_0}{T_s} = 1 - m \sin(\delta + \frac{\pi}{3}), \quad 0 \le \delta < \frac{\pi}{3} \qquad (7)$$

In order to maintain the continuity of the dc input current (i_{dc}), the gate pulses of all switches should be synchronized. Moreover, the HFT flux balance should be satisfied. To meet these conditions and with respect to that the IBSSI operates as a single-stage converter without any intermediate decoupling capacitor, a specific switching pattern is required. The designed switching pattern in discharging mode is shown in Fig. 3. As can be seen, the switching frequency of S_{11} and S_{12} is chosen as half of S_1-S_6 switching frequency and the gate
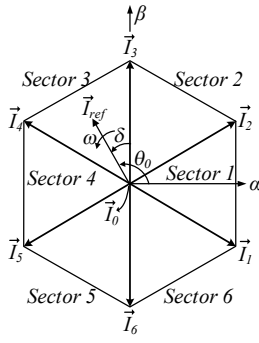
Fig. 2. Space vectors diagram of the IBSSI.

TABLE I
SWITCHING STATES OF THE IBSSI

Space vector	Switching states in discharging mode	Switching states in charging mode
$\vec{I}_1$	$\{S_6, S_1, S_{12}\} or \{S_6, S_1, S_{11}\}$	$\{S_6, S_1, S_{21}, S_{23}\} or \{S_6, S_1, S_{22}, S_{24}\}$
$\vec{I}_2$	$\{S_1, S_2, S_{12}\} or \{S_1, S_2, S_{11}\}$	$\{S_1, S_2, S_{21}, S_{23}\} or \{S_1, S_2, S_{22}, S_{24}\}$
$\vec{I}_3$	$\{S_2, S_3, S_{12}\} or \{S_2, S_3, S_{11}\}$	$\{S_2, S_3, S_{21}, S_{23}\} or \{S_2, S_3, S_{22}, S_{24}\}$
$\vec{I}_4$	$\{S_3, S_4, S_{12}\} or \{S_3, S_4, S_{11}\}$	$\{S_3, S_4, S_{21}, S_{23}\} or \{S_3, S_4, S_{22}, S_{24}\}$
$\vec{I}_5$	$\{S_4, S_5, S_{12}\} or \{S_4, S_5, S_{11}\}$	$\{S_4, S_5, S_{21}, S_{23}\} or \{S_4, S_5, S_{22}, S_{24}\}$
$\vec{I}_6$	$\{S_5, S_6, S_{12}\} or \{S_5, S_6, S_{11}\}$	$\{S_5, S_6, S_{21}, S_{23}\} or \{S_5, S_6, S_{22}, S_{24}\}$
$\vec{I}_0$	$\{S_{11}, S_{12}\}$	$\{D_{11}, D_{12}\}$

pulses of S_{11} and S_{12} are 180 degrees shifted from each other. Therefore, one of S_{11} or S_{12} is held on during one switching cycle and the other is turned off for T_1+T_2 seconds. Also, it can be observed that there are only two switching transitions in each switching period and always one of S_{11} or S_{12} is conducting for the whole of the switching period. In addition, sufficient overlap is provided to make sure that no interruption occurs in the dc current path. This method ensures that the magnetizing current is balanced without any dc offset; also, it is well adapted to the aforementioned SVM scheme and does not need any extra calculations. It is important to note that there is no switching for S_{21}, S_{22}, S_{23}, and S_{24} in discharging mode and they are always on in this mode.

In charging mode, the same switching pattern is used with the difference that the gate pulse of S_{11} is applied to S_{22} and S_{24}. Also, the gate command of S_{12} is applied to S_{21} and S_{23}. The switching commands of S_{21} to S_{24} are shown in Fig. 4. As can be seen, always two switches in the full-bridge stage are conducting, which ensures a continuous current path for the tertiary winding leakage inductance of the HFT and prevents voltage spikes over the full-bridge switches in the charging mode. In charging mode, the polarity of the link voltage and the dc input current (Fig. 4) are reversed compared to discharging mode. Synchronous rectification for D_{11} and D_{12} is realized by turning on S_{11} and S_{12} respectively; in this way, the efficiency of the converter in charging mode is improved. It is important to note that in this mode, a synchronous rectification scheme is used with the assumption that the dc-inductor current is continuous. In discontinuous mode, synchronous rectification is not utilized.

B. Analysis of the HFT volt-second balance

In the conventional switching algorithms used for current-fed push-pull dc/dc converters (where the dc link voltage is fixed), the push-pull switches are alternately switched on and off with an equal duty cycle in order to ensure a balanced flux operation [29]–[31]. But, due to the variable link voltage (v_{Link}) in the IBSSI as shown in Fig. 3, the conventional switching method results in an unbalanced volt-second product and pushes the HFT toward saturation. The proposed switching algorithm prevents saturation of the HFT. The

voltage waveform across the HFT tertiary winding is analyzed to verify the balanced flux operation. Assuming a unity power factor at the output side of the IBSSI and the α-β plane as shown in Fig. 2, line-to-line voltages are given by:

$$v_{ab}(t) = \sqrt{3}V_m \cos(\omega t + \frac{\pi}{6}) \tag{8}$$

$$v_{bc}(t) = \sqrt{3}V_m \cos(\omega t + \frac{\pi}{6} - \frac{2\pi}{3}) \tag{9}$$

Where V_m is the maximum phase voltage. The corresponding switching commands, the link voltage and the winding voltage of the HFT are shown in Fig. 3. In the third sector, switches S_2 and S_3 are turned on for T_1 seconds and the link voltage is equal to V_{bc} from t_0 to t_3; where V_{bc} is the instantaneous value of v_{bc} at t_0. The current path in this time interval is shown in Fig. 5(a). Afterward, for T_2 seconds the switches S_4 and S_3 are turned on and the link voltage follows a step change from V_{bc} to V_{ba} at t_3 and it is equal to V_{ba} from t_3 to t_4; where V_{ba} is the instantaneous value of v_{ba} at t_0. In the remaining time of the switching period (T_0) the link is shorted by concurrent conduction of switches S_6 and S_3 from t_4 to t_6. Therefore, the link voltage from t_0 to t_6 can be expressed as:

$$v_{Link}(t) = V_{bc} = \sqrt{3}V_m \sin(\omega t_0), \quad t_0 \le t < t_3 \tag{10}$$

$$v_{Link}(t) = V_{ba} = -\sqrt{3}V_m \cos(\omega t_0 + \frac{\pi}{6}), \quad t_3 \le t < t_4 \tag{11}$$

$$v_{Link}(t) = 0, \quad t_4 \le t < t_6 \tag{12}$$

From Fig. 5(a), it can be concluded that when S_{12} is turned on and S_{11} is turned off, diodes D_{22} and D_{24} carry the current on the high-voltage side of the HFT. Thus, the link voltage is put on the HFT winding with reverse polarity for T_1+T_2 seconds within one switching period ($v_{T3}=-v_{Link}$). In this state, the volt-second product applied to the high-voltage winding in one switching period can be calculated as:

$$\lambda_1 = \int_{T_S} v_{T3}(t)dt = \int_{T_S} -v_{Link}(t)dt = -T_1 V_{bc} + T_2 V_{ab} \tag{13}$$

Replacing the line-to-line voltages in (13) gives:

$$\lambda_1 = -mT_s \sin(\frac{\pi}{3} - \delta).\sqrt{3}V_m \sin(\theta_0) + mT_s \sin(\delta).\sqrt{3}V_m \cos(\theta_0 + \frac{\pi}{6}) \tag{14}$$

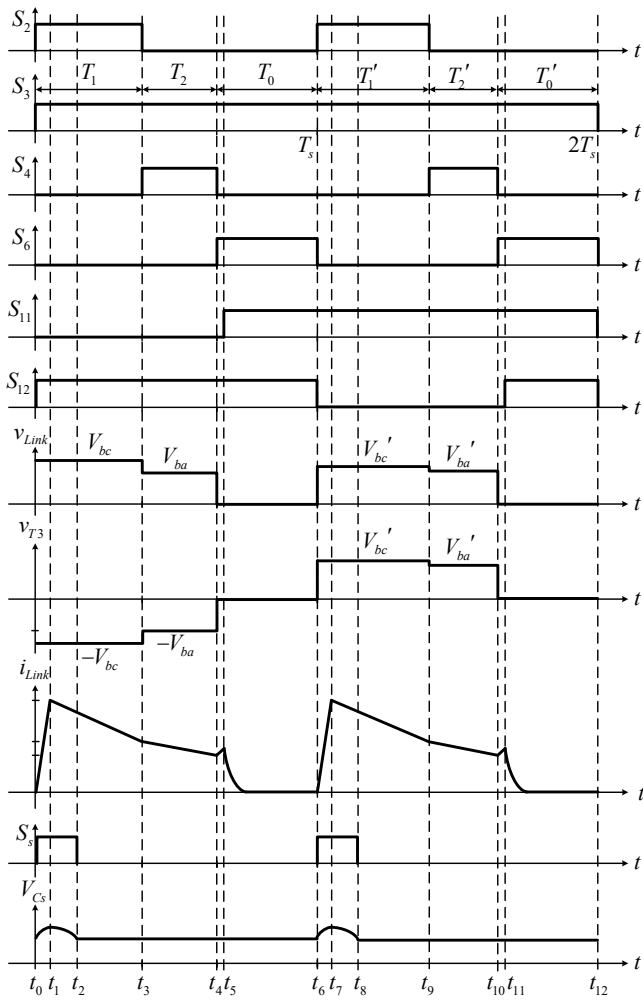From (14), by doing some mathematical operations, the volt-second product is simplified as:

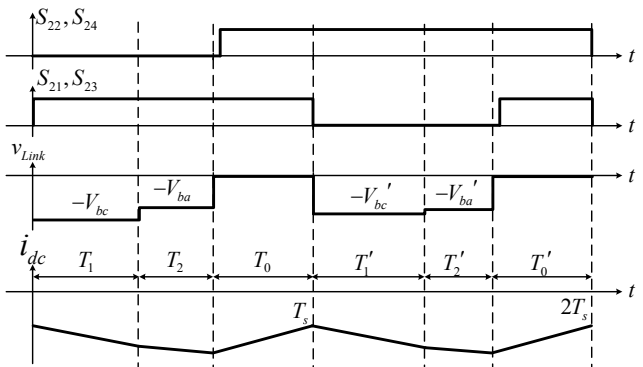Fig. 3. Key waveforms of the IBSSI in discharging mode.

Fig. 4. Key waveforms of the IBSSI in charging mode.

$$\lambda_1 = -\frac{3}{2} m V_m T_s \tag{15}$$

It can be seen that the volt-second product is constant and independent of the reference current vector angle. In the next switching period (from t_6 to t_{12} in Fig. 3), S_{11} is on and S_{12} is off; diodes D_{21} and D_{23} conduct and the winding voltage is equal to the link voltage ($v_{T3}=v_{Link}$). Thus, the corresponding volt-second product is:
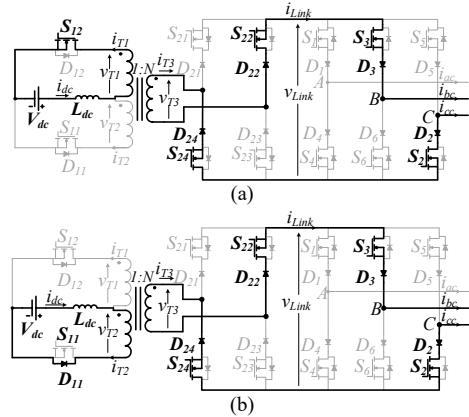

Fig. 5. The switching states of the IBSSI from t_0 to t_3 (a) in discharging mode, (b) in charging mode.

$$\lambda_2 = \int_{T_S} v_{Link}(t)dt = T_1' V_{bc}' - T_2' V_{ab}' \tag{16}$$

Where V_{bc}' and V_{ab}' are the instantaneous value of line-to-line voltages v_{bc} and v_{ab} at t_6, respectively. T_1' and T_2' are the dwell times calculated by the switching algorithm at t_6. Replacing the dwell times and line-to-line voltages in (16) gives:

$$\lambda_2 = \frac{3}{2} m V_m T_s \tag{17}$$

From (15) and (17) it is deduced that the sum of the volt-second areas is zero and the HFT resets in two switching periods. The switching state of the IBSSI and the current path from t_0 to t_3 in charging mode is shown in Fig. 5(b). Since the switching commands of the converter are the same in charging and discharging modes, the balanced flux operation is also guaranteed in charging mode.

C. Active snubber operation

The different operating modes of the active snubber are depicted in Fig. 6 (a) to (d). As demonstrated in Fig. 6 (b), by turning off S_{12} at the end of the overlapping period of S_{11} and S_{12} (Fig. 6 (a)), the leakage inductance of the HFT forces the current into snubber diode D_{s2} and charges the snubber capacitor. The voltage across the snubber capacitor and the gate pulse of the snubber switch are shown in Fig. 3. The capacitor voltage rises from t_6 to t_7. On the other hand, the snubber switch is turned on at t_6 to regulate the capacitor voltage. The switching frequency of the snubber is the same as the main converter and its duty cycle is determined by the controller. At t_7, the leakage inductance current reaches zero and D_{s2} turns off (Fig. 6 (c)); the capacitor voltage falls as the capacitor discharges. At t_8, the snubber switch turns off while the snubber inductor current (i_{L_S}) flows through the buck converter diode (Fig. 6 (d)). The same sequence occurs when S_{11} turns off after an overlapping interval. In the time interval from t_6 to t_7 the voltage across the HFT windings is given by:

$$v_{T1} = v_{T2} = \frac{V_{Cs}}{2} \tag{18}$$

The voltage across the leakage inductance of the HFT as shown in Fig. 6 is:
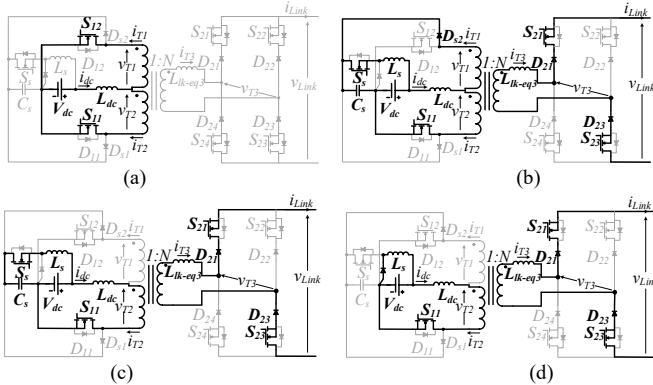
$$v_{L_{lk-eq3}} = N v_{T1} - v_{link} \tag{19}$$

Fig. 6. Switching modes of the active snubber (a) at t_6, (b) from t_6 to t_7, (c) from t_7 to t_8, (d) at t_8.

Fig. 7. Gate drive signal generation for the IBSSI.

The elapsed time between t_6 to t_7 is:

$$\tau = t_7 - t_6 = L_{lk-eq3} \frac{I_{dc}}{N V_{L_{lk-eq3}}} = L_{lk-eq3} \frac{1}{N} \frac{I_{dc}}{0.5 N V_{Cs} - v_{link}} \quad (20)$$

Where I_{dc} is the average value of the input inductor current and L_{lk-eq3} is the sum of the primary and tertiary winding leakage inductances referred to the tertiary winding. From (20) the maximum charging time of the snubber capacitor can be calculated. Furthermore, the energy transferred to the snubber capacitor can be expressed as:

$$E_{C_s} = \frac{1}{4} V_{Cs} I_{dc} \tau \quad (21)$$

Considering that $\tau < T_1$, the link voltage can be replaced from (10) in (20). In this way (21) can be expressed as:

$$E_{C_s}(\theta_i) = \frac{1}{4} V_{C_s} I_{dc} \times L_{lk-eq3} \frac{1}{N} \frac{I_{dc}}{0.5 N V_{C_s} - \sqrt{3} V_m \mathrm{Sin}(\theta_i)},$$
$$\theta_i = \frac{\pi}{2} + i \times \frac{\pi}{180}, \qquad 0 \le i < 59 \quad (22)$$

Then, the average power recycled by the active snubber during one period of the grid voltage can be calculated as:

$$P_s = 6 f_g \eta_s \sum_{i=0}^{59} E_{C_s}(i) \quad (23)$$

Where η_s is the efficiency of the active snubber and f_g is the grid frequency. The required capacity of the snubber capacitor can be calculated based on its maximum and minimum allowed voltage as:

$$C_s = \frac{2 E_{C_s}}{\left(V_{C_s}^{\max}\right)^2 - \left(V_{C_s}^{\min}\right)^2} \quad (24)$$

Where the minimum voltage of the snubber capacitor should satisfy:

$$V_{C_s}^{\min} > \frac{2}{N} v_{link}^{\max} \quad (25)$$

The design procedure of the active snubber is given in the appendix. The presented snubber circuit also provides a path for the dc current when both S_{11} and S_{12} are turned off due to a wrong command or gate drive failure and protects the switches; which improves the reliability of the converter. In this case, the dc inductor current flows through the snubber diodes and snubber capacitor. Therefore, the snubber capacitor voltage increases. Since this voltage is sensed by the microcontroller, a fault condition is detected and the gate pulse generation is stopped immediately. Hence, the snubber
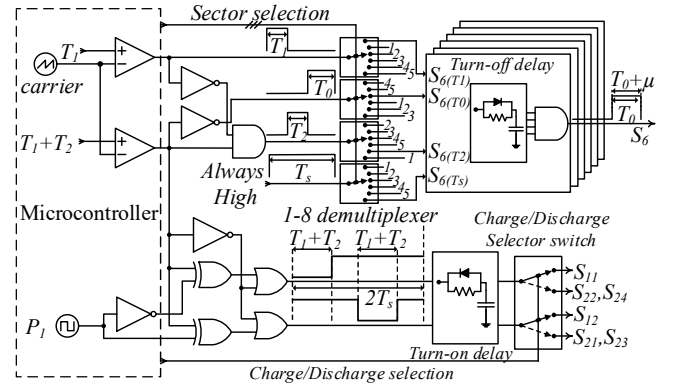
capacitor or diodes should handle the nominal dc link current for just one switching cycle.

D. ZVS/ZCS

As shown in Fig. 3, a turn-on delay is applied to the gate pulses of S_{11} and S_{12}. This turn-on delay should be selected longer than the turn-on switching time of the SiC MOSFETs. The turn-on switching time of the selected SiC MOSFETs is given as 69 ns. Since the operating conditions of the SiC MOSFETs in the IBSSI are different from those given in the datasheet and be more conservative, the turn-on delay is assumed equal to 500 ns. Therefore, the link is shorted by turning on S_6 and S_3 at t_4 and S_{11} is turned on after 500 ns at t_5 while the link voltage and the HFT winding voltage are zero. Hence, S_{11} and S_{12} are switched on under ZVS condition.

The link current (i_{link}) is illustrated in Fig. 3. In the time interval from t_1 to t_5, i_{link} is equal to $\frac{i_{dc}}{N}$. At t_5 both of S_{11} and S_{12} are turned on and the series connection of the leakage inductance of the HFT with the conducting switches on-resistance and the winding resistance forms an RL circuit. Therefore, i_{link} which is equal to $-i_{T3}$ decays to zero (due to the presence of the leakage inductance i_{T3} does not drop to zero immediately). If the link current reaches zero before t_6, the conducting switches of S_1-S_6 and the full-bridge diodes can be turned off under zero current at the end of the switching period. Regarding i_{link} waveform and the gate signal of S_6 in Fig. 3, S_6 is turned off under ZCS condition at t_6.

The leakage inductance of the HFT limits the rate of rise and fall of the transformer current i_{T3} (the rate of rise of the leakage inductance current is determined by (20)). Therefore, turn-on and turn-off losses of the D_{21}-D_{24} are small. Also, the finite current rise time leads to the reduction of the turn-on losses of S_1-S_6 at the beginning of the switching period.

E. Generation of the switching pattern

The circuit used for switching command generation is demonstrated in Fig. 7. In order to generate the switching commands, two pulses with a frequency of $\frac{1}{T_s}$ and a pulse width equal to T_1 and T_1+T_2 are generated by the microcontroller. Another pulse (P_1) with a frequency of $\frac{1}{2T_s}$ and a duty cycle of 50% is also produced. The numbers associated with the outputs of the demultiplexers correspond
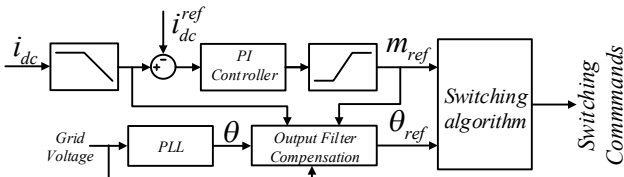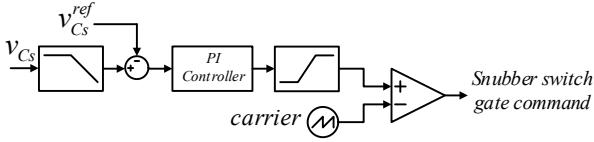
Fig. 8. Block diagram of the IBSSI control system.

Fig. 9. Block diagram of the active snubber control system.

TABLE II
SYSTEM PARAMETERS

Parameter	Comments	Value
P_{nom}	Nominal discharging output power	3 [kW]
V_{dc}	Battery input voltage	48 [V]
L_{dc}	Input filter inductor (rated current 67 A)	300 [uH]
C_{in}	Input filter capacitor	6 [uF]
L_s	Snubber inductor (rated current 7 A)	1 [mH]
C_s	Snubber capacitor	6.6 [uF]
N	Transformer turns ratio	3
C_f	Output filter capacitor (3 capacitors in parallel)	9 [uF]
L_f	Output filter inductor (rated current 7 A)	220 [uH]
f_s	Switching frequency	18 [kHz]
V_g	Grid RMS phase voltage	220 [V]
f_g	Grid frequency	50 [Hz]
S_1-S_6	SiC MOSFET	SCT2080
D_1-D_6	SiC Diode	SCS215

to inverter switches S_1 to S_6. It should be noted that the switch position of the demultiplexers from up to down corresponds to the six sectors shown in Fig. 2. The appropriate sector selection command (the switch position) is determined by three pins of the microcontroller. In order to avoid an open circuit of the dc inductor or the leakage inductance of the HFT, a turn-off delay (μ) is added by the RCD (Resistor-Capacitor-Diode) circuits. The turn-off delay should be longer than the turn-on switching time of the SiC MOSFETS (it is assumed equal to 500 ns in the prototype). A selector switch is used to apply the gate pulses to S_{11} and S_{12} in discharging mode or apply them to S_{21}-S_{24} in charging mode.

IV. CONTROL STRATEGY

The control block diagram of the IBSSI is shown in Fig. 8. As can be seen, the dc current is the only control variable and measuring the ac currents is not necessary. Thus, isolated ac current sensors can be eliminated. The dc current is sensed by a simple shunt resistor without any isolation. The reference of the dc side current is determined by the battery management system. The output of the PI controller after the limiter block in Fig. 8 is used as the modulation index reference value in equations (3) to (5). The angle of the reference current vector is determined based on the phase of the grid voltage. In order to achieve a unity power factor operation, the phase displacement due to the output CL filter is compensated. To do this, the relationship between the grid side and the converter side currents can be written as:

$$I_c = I_g(1 - \omega^2 L_f C_f) + jV_g \omega C_f \qquad (26)$$

Where I_c is the phasor of the converter side current, C_f is the value of output filter capacitors (C_a, C_b, C_c) and L_f is the value of output filter inductors (L_a, L_b, L_c). From (26) the magnitude of I_g is calculated as:

$$I_g = \frac{\sqrt{|I_c|^2 - (V_g \omega C_f)^2}}{1 - \omega^2 L_f C_f} \qquad (27)$$

By replacing $|I_c|$ in (27), the grid current can be expressed as:

$$I_g = \frac{\sqrt{(\frac{m_{ref}}{N} I_{dc})^2 - (V_g \omega C_f)^2}}{1 - \omega^2 L_f C_f} \qquad (28)$$

I_g obtained from (28) is used to calculate the reference angle of the converter current. For a unity power factor operation, the grid voltage (V_g) and the grid current (I_g) should be in
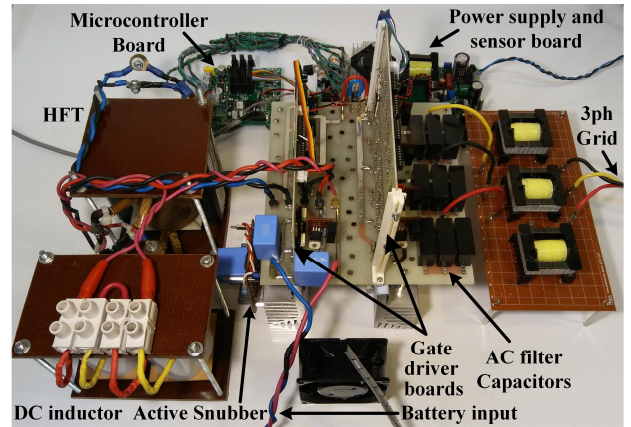

Fig. 10. Experimental Test Setup.

phase; therefore, the required phase angle of I_c relative to the grid voltage from (27) is determined by:

$$\theta_{ref} = \angle I_c = \tan^{-1}\left(\frac{V_g \omega C_f}{I_g(1 - \omega^2 L_f C_f)}\right) \qquad (29)$$

By using this compensation method, even with an error of +20% and -10% in the values of C_f and I_c, the output power factor will be more than 97% in different operating points.

The control block diagram of the active snubber is shown in Fig. 9. It is self-describing and the role of the active snubber controller is to regulate its input voltage, which is the snubber capacitor voltage.

V. PERFORMANCE EVALUATION OF THE IBSSI

A. IBSSI operation

A 3-kW prototype with the parameters summarized in Table II was built to evaluate the performance of the IBSSI. Four BP65-12 batteries with a maximum charging current of 19.5 A were connected in series and used in the prototype [36]. The test setup is shown in Fig. 10.

At the first, the reference dc current (i_{dc}^{ref}) is set to 60 A and -20 A in discharging and charging modes, respectively. The three-phase output currents and grid phase voltage in discharging and charging modes are illustrated in Fig. 11(a) and (b), respectively. It can be seen that the IBSSI generates three-phase balanced currents with a unity power factor without using any ac current sensors. With respect to Fig. 11
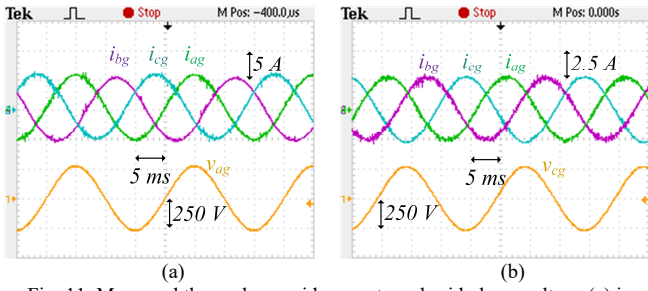
Fig. 11. Measured three-phase grid currents and grid phase voltage (a) in discharging mode when P_{out} = 2269 W, V_{dc} = 42.1 V, I_{dc} = 60 A and I_{bat} = 58.15 A, (b) in charging mode when P_{out} = -1134 W, V_{dc} = 52.18 V and I_{dc} = I_{bat} = -20 A.
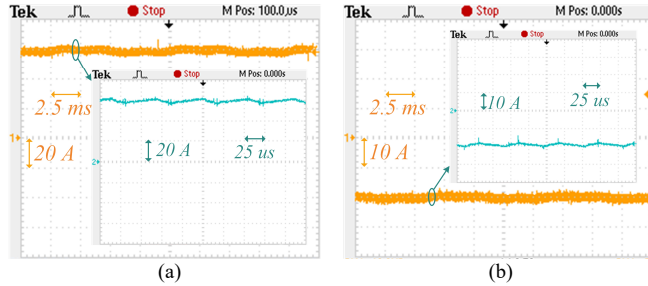

Fig. 12. Measured dc input current (i_{dc}) (a) in discharging mode when P_{out} = 2269 W, V_{dc} = 42.1 V, I_{dc} = 60 A and I_{bat} = 58.15 A, (b) in charging mode when P_{out} = -1134 W, V_{dc} = 52.18 V and I_{dc} = I_{bat} = -20 A.
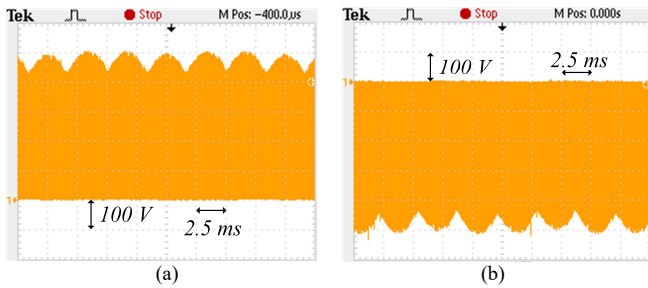

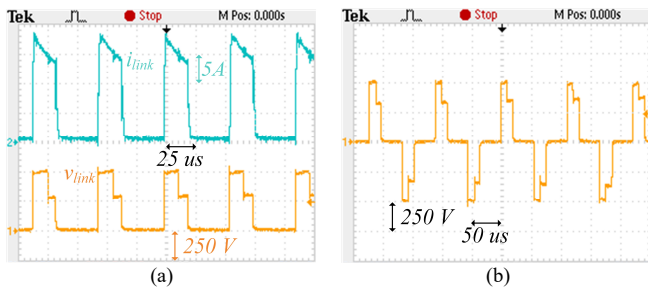Fig. 13. Measured link voltage (v_{link}) (a) in discharging mode, (b) in charging mode.

Fig. 14. Measured waveforms in discharging mode when P_{out} = 2050 W, V_{dc} = 49 V, I_{dc} = 46 A and I_{bat} = 45 A (a) the link voltage (v_{link}) and current (i_{link}) (b) the winding voltage of the HFT (v_{T3}) and current (i_{link}) (b) the winding voltage of the HFT (v_{T3}).

Fig. 15. (a) Measured link voltage (v_{link}) and current (i_{link}) in charging mode when P_{out} = -1134 W, V_{dc} = 52.18 V and I_{bat} = -20 A (b) Measured snubber capacitor voltage and switching command of the snubber switch in discharging mode.

Fig. 16. Simulated three-phase output currents and grid phase voltage in the case of a voltage dip.

the corresponding modes. The average power recycled by the active snubber in discharging mode is calculated from (23) equal to 78 W considering that L_{lk-eq3} = 7 μH, η_s = 94%, V_{Cs} = 400 V, V_m = 275 V and I_{dc} = 60 A. It should be noted that the active snubber does not operate in charging mode. Therefore, regarding Fig. 1, I_{dc} and I_{bat} are equal in this mode.

The link voltage in discharging and charging modes are shown in Fig. 13(a) and (b), respectively, for one cycle of the grid voltage. As can be seen, a continuous current path is always provided and no voltage spikes are observed. The link voltage and current in four switching cycles are shown in Fig. 14(a). The limited rise time and fall time of the link current and the step change of the link voltage are evident in this figure. As explained in section III-B, without a proper switching algorithm this step change can lead to the transformer saturation. As shown in Fig. 14(a), the link current decays to zero in each switching cycle and provides soft switching conditions for the switches and diodes. The applied voltage to the high voltage winding of the HFT (v_{T3}) is shown in Fig. 14(b). It can be observed that v_{T3} is a bipolar voltage with zero average. The waveforms of v_{link} and i_{link} in the charging mode are illustrated in Fig. 15(a). As can be seen, in the charging mode v_{link} is negative and the slope of i_{link} is positive in contrast to the discharging mode. The waveforms of the snubber capacitor voltage and the snubber switching command are shown in Fig. 15(b). According to this figure, the capacitor voltage is properly controlled at the reference value of 400 V.

The IBSSI operation during a grid voltage dip, a step change in the reference of the dc input current and under unbalanced grid voltages is also studied. Based on the IEEE Std. 929-2000 [37] a voltage dip equal to 12% is applied to the grid voltage at 0.04 s. The three-phase grid currents and the grid phase voltage are shown in Fig. 16. In this case, the PI controller tries to maintain the dc input current at the specified level. Therefore, the input power remains unchanged. With a

(a) and (b), the output power (P_{out}) in discharging and charging modes is calculated equal to 2269 W and -1134 W, respectively (these operating points were chosen arbitrarily and performing the tests in other operating points such as the rated power also leads to the same results). The dc input current (i_{dc}) in discharging and charging modes is shown in Fig. 12(a) and (b), respectively. As can be seen, it is properly controlled at the reference value, which is 60 A and -20 A in
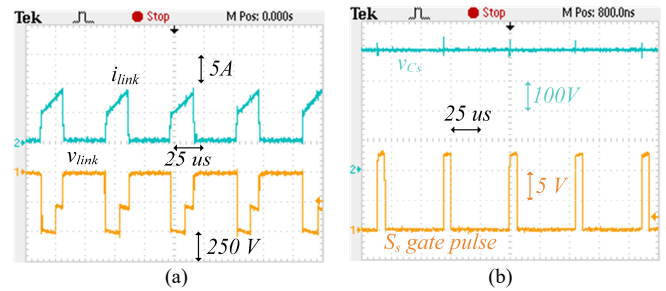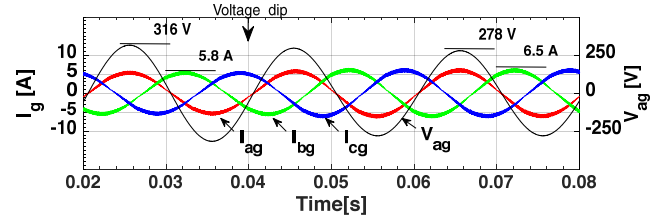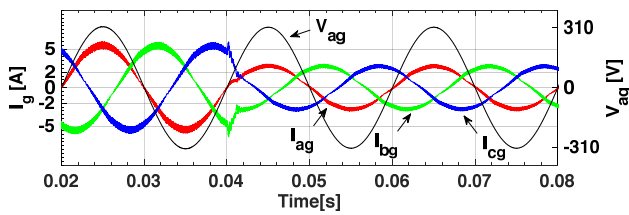
Fig. 17. Simulated three-phase output currents and grid phase voltage in the case of a step change in the reference of the dc input current.
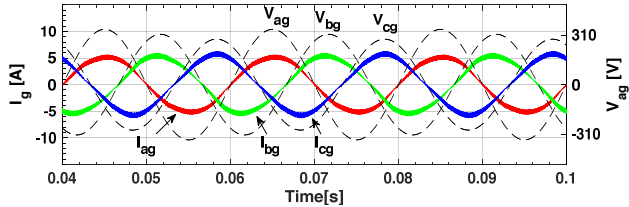

Fig. 18. Simulated three-phase output currents and unbalanced grid phase voltages.
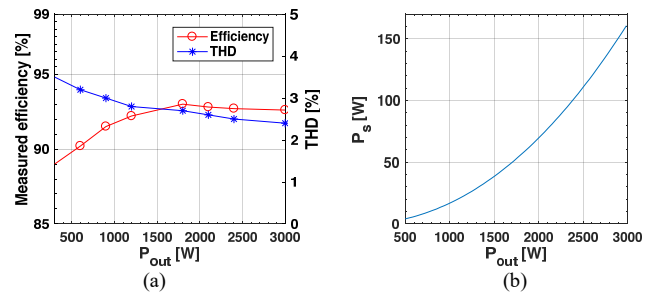

Fig. 19. (a) Measured efficiency and THD of the IBSSI, (b) Calculated recycled power by the active snubber.

TABLE III
HIGH-FREQUENCY ISOLATED DC/DC CONVERTERS EFFICIENCY

Topology	Ref.	Rated power [kW]	Input voltage [V]	Output voltage [V]	Peak Efficiency [%]
current-fed push-pull/full-bridge	[33]	5	60-110	380	97.1
	[30]	0.5	50	380	94
	[43]	0.25	20-40	400	96.6
current-fed push-pull/half-bridge	[32]	0.51	50	350	96.12
	[31]	0.2	41	350	94.52
voltage-fed push-pull/full-bridge	[28]	1	59	380	95.7

TABLE IV
OPERATION OF THE IBSSI UNDER A DISTORTED GRID VOLTAGE

Grid Voltage THD	Grid current THD at the rated power	Grid current THD at 25% of the rated power
4 %	4.42 %	6.7 %
8 %	8.65 %	15 %

constant input power, the output power should be constant, too. Regarding the constant output power and the grid voltage reduction, the output current increases. Thus, it can be stated that the IBSSI with the proposed control strategy works in a constant power mode in the case of grid voltage dips. In another transient simulation, the reference of the dc input current (i_{dc}^{ref}) is changed from 60 A to 30 A at 0.04 s. The three-phase output currents and the grid phase voltage are shown in Fig. 17. As can be seen, the three-phase balanced currents with a unity power factor are injected to grid. The IBSSI operation under unbalanced grid voltages is studied by increasing v_{ag} to $1.1v_{bg}$ and decreasing v_{cg} to $0.9v_{bg}$. The output currents and the grid phase voltages are plotted in Fig. 18. As can be seen, the output currents are unbalanced (the amplitude of i_{ag} is decreased and the amplitude of i_{cg} is increased) and the output current THD is increased to 4.2%. Moreover, it is observed that an oscillation with the frequency of $2f_g$ is created in the dc input current and the volt-second balance of the HFT is satisfied. Improving the control method to inject balanced currents to the grid in this condition is the subject of future work.

B. THD and efficiency comparison

The efficiency and the THD of the IBSSI versus the output power are shown in Fig. 19(a). Based on this figure, the maximum measured efficiency of the IBSSI is about 93% and the output current THD is less than 3.5% at different output powers.

In order to perform an efficiency comparison, the efficiencies of three-phase single-stage VSIs and isolated dc/dc converters are extracted from literatures and then the overall efficiency of a two-stage VSI is estimated by multiplying these efficiencies. The efficiencies of dc/dc converters are reported in Table III, where the average efficiency is 95.67%. It should be noted that all these topologies except the voltage-fed one are unidirectional. The efficiency of a three-phase 7 kW VSI with SiC MOSFETs has been reported equal to 98.8% in [38]. Therefore, the efficiency of a two-stage VSI with LCL filter is estimated about 94.5%, which is only 1.5% higher than the IBSSI efficiency. As can

be seen, even with high conduction losses in the IBSSI, eliminating the output converter-side filter inductors, minimizing the switching losses and utilizing an active snubber circuit result in an acceptable efficiency. In order to show the role of active snubber in efficiency improvement, the recycled power by the active snubber is calculated from (23) and plotted versus the output power in Fig. 19(b). As can be seen, the recycled power is 160 W at the rated output power (5.3% of the output power). This implies the share of the active snubber in the efficiency improvement. In order to have a more accurate efficiency comparison, the two-stage VSI (which is composed of a push-pull/full-bridge dc/dc converter and a dc/ac inverter containing an LCL filter) with the same power rating, input and output voltages and SiC MOSFETs as given in Table II is simulated and the converter losses are calculated. In this way, the efficiency of this converter is obtained equal to 94.1%, which is 1.1% higher than the efficiency of the IBSSI.

The THD values in Fig. 19 (a) are measured with the grid line to line voltage THD equal to 2%. Since no ac current sensors are used in the IBSSI, the output current THD goes up as the grid voltage THD increases. The IBSSI has been simulated in two cases in which the grid voltage THD is assumed 4% and 8%. The simulation results are provided in Table IV. The results show that under the grid voltage THD below 4.5%, the IBSSI output current THD will remain below 5% at the rated output power. However, it is possible to control the low order harmonics of the grid current when the

TABLE V
THE PRICE OF UNCOMMON COMPONENTS BETWEEN THE TWO TOPOLOGIES

Topology	Device	Part number	Price [$]	Quantity	Total price [$]
IBSSI	SiC diode	SCS215-AGC	4.72	10	47.2
	Output filter capacitor	MKP1847	3.43	9	30.87
	Output filter inductor	434-TLC/10A	10.64	3	31.92
Two-stage VSI with output LCL filter	Inverter-side filter inductor	546-159ZL	24.94	3	74.82
	Output filter capacitor	B32754	2.9	3	8.7
	DC link capacitor	LLS2V221	3.08	4	12.32
	AC current sensors	T60404-N4646-x762	13.25	3	39.75
	DC link voltage sensor	HCPL-7840 Module	11	1	11

grid voltage is highly distorted by adding ac current sensors and current control loops.

C. Reliability and cost comparison

In order to compare the reliability of the IBSSI and the two-stage VSI, the failure rates of the components are calculated based on the methods presented in [39], [40]. The dc/ac stage components' values and ratings used in the two-stage VSI are obtained from [41]. According to [39], the failure rate of each component can be calculated by multiplying the base failure rate by the acceleration factors. The data used for failure rate calculations are obtained from [42]. The failure rate of the whole converter is found by adding the failure rates of all the components. In order to calculate the failure rates, it is assumed that both converters are operating at the rated power and the same quality factor and environmental factors are used. With these assumptions, the failure rates of the two-stage VSI and the IBSSI are calculated equal to 48.69 and 38.79 $\frac{Failures}{10^6 hours}$, respectively. As can be seen, the failure rate of the IBSSI is 20% lower than the two-stage VSI, which implies that the IBSSI lifetime is increased by 25%.

In order to compare the cost of the IBSSI and the two-stage VSI, the price of uncommon components between the two topologies are extracted from Mouser Electronics and reported in Table V. From Table V, it can be concluded that the total price of the dc link capacitors, the output filter capacitors, the filter inductors, ac current sensors and dc link voltage sensor in the two-stage VSI is about 146.6 $, while the total price of the SiC diodes and the output filter capacitors and inductors in the IBSSI is about 110 $. Considering the total cost of the common components between the two topologies about 300 $, it can be concluded that the total cost of the IBSSI is about 8.2 % lower than the total cost of the two-stage VSI. Even, the cost of the IBSSI with ac current sensors is only 0.7% higher than the cost of the two-stage VSI. As can be seen, the reliability improvement is achieved without increasing the cost of the converter.

VI. CONCLUSION

A novel isolated bidirectional single-stage three-phase inverter with enhanced reliability has been presented in this paper. A single-stage energy conversion from the ESD to the grid with boosting capability is provided by the IBSSI. The boosting capability along with using the HFT provides a high voltage ratio and allows employing low voltage ESDs. Moreover, the IBSSI needs just four filter inductors, while the conventional two-stage VSI with LCL filter needs seven inductors, at least (The value and the current rating of the common inductors between the two topologies are nearly the same). In the IBSSI, the dc inductor is placed in series with the input port. Therefore, a continuous low ripple current is drawn from the input, which is essential for the ESDs. A simple control strategy with a low computational task for the microcontroller has been used in which grid-side currents and output power factor are controlled without any ac current sensors or intermediate dc link. A new switching algorithm based on SVM has been designed and applied to the converter, which prevents the HFT saturation and provides soft-switching conditions. The switching strategy has the minimum number of switchings per cycle. In addition, a novel circuit has been used to implement the switching algorithm. An active snubber circuit has been used to handle the voltage spikes caused by the leakage inductance of the HFT and improve the efficiency. It also provides additional protection for the converter. The operation of the converter in both charging and discharging modes has been analyzed. The simulation and experimental results have proved the performance of the IBSSI with the proposed switching method. The maximum efficiency of 93% with THD less than 3.5% have been achieved with the experimental setup. The reliability of the IBSSI has been improved by eliminating the electrolytic capacitor, so that its lifetime is 25% longer than the conventional two-stage VSI. The reliability improvement has been attained without increasing the cost of the converter.

APPENDIX A. ACTIVE SNUBBER DESIGN

The snubber design procedure assuming $V_{dc}^{min} = 42V, V_{dc}^{max} = 50V, \eta_s = 94\%, L_{lk-eq3} = 7\mu H, I_{dc}^{max} = 67A, V_m = 310V$ is as follows:

1- Selecting V_{C_s} with respect to (25): $V_{C_s} = 400V, V_{C_s}^{max} = 410V$.

2- Calculating the maximum value of τ from (20): $\tau_{max} = 2.467\mu s$.

3- Calculating the maximum value of the snubber inductor current from $I_{L_s}^{max} = \frac{V_{C_s} I_{dc}^{max} \tau_{max} \eta_s f_s}{4 V_{dc}^{min}} = 6.7A$.

4- Calculating the maximum duty cycle of the active snubber switch from $D_{max} = \frac{V_{dc}^{max}}{V_{C_s}} = 0.125$.

5- Calculating the snubber inductor value from $L_s = \frac{(V_{C_s} - V_{dc}^{max}) D_{max}}{f_s \Delta I_{L_s}} = 1.2mH$ where ΔI_{L_s} is the peak to peak ripple current of the snubber inductor and assumed equal to 2.1 A.

6- Calculating the snubber capacitor value from (24): $C_s = 4.3\mu F$. Since the snubber capacitor absorbs the input inductor energy during a fault condition, its rated voltage should be

selected based on this condition. The maximum voltage rise of the snubber capacitor during a fault is calculated equal to 137V. Therefore, it is appropriate to choose the rated voltage of the capacitor more than 550 V.

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VIII.   BIOGRAPHIES

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Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 30 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE

TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too.