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A DDS-Based Wait-Free Phase-Continuous Carrier Frequency Modulation Strategy for EMI Reduction in FPGA-Based Motor Drive

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***Abstract*- In AC motor drives, the fixed-frequencies harmonic components of output voltage and current from the inverter with fixed frequency pulse width modulation (FFPWM) usually lead to electromagnetic interference (EMI). The spread spectrum clock generation (SSCG) is a widely used solution of this problem. Adjusting the switching frequency to reduce EMI is one kind of practicable scheme among SSCG methods. How to design an optimal or suitable modulation profile is a research emphasis of scholars and has been discussed in depth in many literatures. However, apart from modulation profile, the mode and quality of carrier are also important and can be improved. In most frequency modulation methods, due to the limitation of the conventional carrier generation mode, the implementation of the new frequency instruction has to wait to the termination of the last switching period. In order to eliminate the waiting state and design a simpler algorithm, this paper has proposed a wait-free phase-continuous carrier frequency modulation strategy (WPCFM) by combining the direct digital frequency synthesizer (DDS) theory and proper temporal planning of control interruptions. Besides, theoretical analysis of WPCFM including quantization error, frequency jitter, phase delay and voltage distortion have been finished. Moreover, compared with conventional methods, a more convenient, feasible and simpler field-programmable gate array (FPGA) based algorithm implementation method and the control structure of WPCFM are also introduced. Analysis shows that, although WPCFM causes a slight increase of the current ripple, it can solve the partial frequency nonuniform distribution problem of conventional method and it has potential value of applications in the wide band gap (WBG) motor drive systems. The effectiveness of the WPCFM is verified by several sets of EMI reduction experiments where classical periodic carrier frequency modulations are applied.[1]**

Index Terms—Direct digital frequency synthesizer, spread spectrum frequency modulation, EMI, motor drive, FPGA.

NOMENCLATURE

N	Register bit.
M	Counting threshold.
n	Step number.
K	DDS step length.
R	Steps to complete each period.
P	Phase delay.
U_E, U_R	Expected and actual average voltage.
q, p	Phase node of frequency and level switching.
f_c	Control clock frequency.
f_e	Desired output frequency.
f_P	Frequency generated by DDS.
f_T	Frequency generated by conventional method.
f_r	Jitter frequency.
f_s	Switching frequency.
f_m	Modulation profile frequency.
m_f	Modulation index.
$\cdot^*$	Ideal parameter.
Δ	Symbol of error and variation.
$\cdot_{\inf}$	Upper bound.
$\cdot_+$, $\cdot_-$	Ceiling and floor function.

I. INTRODUCTION

NOISE is a common problem in most motor drives and other electrical systems fed by the fixed-frequency pulse width modulation (FFPWM) inverter [1]-[6]. Severe noise causes problems, impacts the user experience and finally reduces the market competitiveness of products. Hence, the suppression of noise is an important question. Conventional noise can be divided into two categories: Mechanical and Electrical Noise (EMI). Mechanical noise has lower frequency and usually comes from the vibration of mechanical structures. Suitable teeth pairing, rotor design or reduction of electromagnetic exciting force can solve this problem [7]-[9]. Besides, EMI comes from the switching action of the power devices [10]. The high values of current surge di/dt and voltage variation dv/dt come from the switching actions are mainly responsible for the different mode (DM) noise and common mode (CM) noise respectively [11]. These noises interfere with the stability of other devices that share the common direct current (DC) bus, especially for those highly

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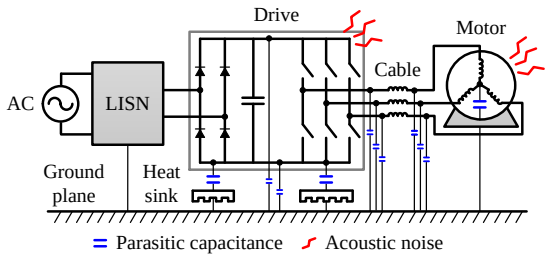

Fig. 1. The circuit schematic of a motor drive system.

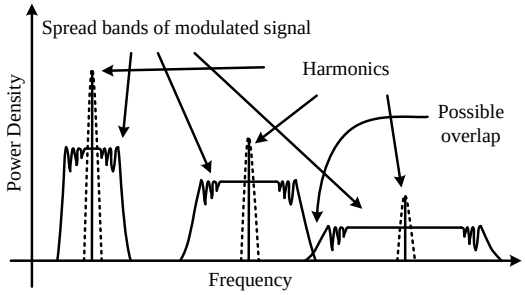

Fig. 2. Spread bands of harmonics in modulated square signals.

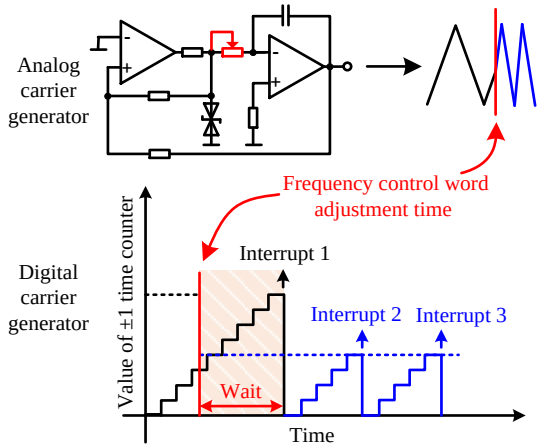

Fig. 3. The comparison of digital and analog carrier generation processes.

integrated systems like submarine system, satellite, and electric vehicle [11], [12]. In order to narrow down the pollution of EMI within an acceptable range, various electromagnetic compatibility (EMC) standards are established. Since the normal switching frequency of the motor drive inverter is comparatively slow, especially in high power rate system, the reduction of the conducted EMI is the focus in this paper. Moreover, due to the switching frequency of Si device in motor drive is usually lower than 20 kHz, thus, this noise from switching action of power device and the vibration caused by harmonic current are also acoustic. **Fig. 1** is one kind of the EMI test platform of a motor drive system [13]. The motor drive is fed by an AC power supply through a line impedance stabilization network (LISN). The parasitic capacitances between ground and different components of the motor drive system (heat sink, dc bus, device baseplate, cable, motor winding and etc.) build bridges for the flowing of CM current while DM noise propagates through the operation paths [14], [15]. Because the inductance of the motor is comparatively larger than stray capacitances, the impedance for d*i*/d*t* is larger than d*v*/d*t*. In addition, part of the DM current is absorbed by the voltage regulated capacitor that parallel to the DC bus. Thus, CM noise is more serious than DM noise in motor drive [15], [16].

About conducted EMI reduction, adding additional components such as busbar filter, LCL filter, capacitor bank, and etc., or improving the hardware design is the most direct solution [12], [15], [17]-[19]. However, the adjustment of structure and redesign of the hardware are both costly and not flexible enough. Among software solutions, the method based on Parseval theorem, which can weaken the peak-level of the spectrum (modulation gain) by spreading the dominant harmonic clusters, is called spread spectrum clock generation (SSCG) [20]-[23]. The spread spectrum based PWM techniques can be classified into four groups, including programmed PWM, periodic modulation, random modulation and chaotic modulation [24]-[26]. 1) Programmed PWM [27], [28]: achieving harmonic elimination or minimize by predetermined and optimized switching instances of generated square waveforms. However, its performance decreases when the number of harmonics becomes larger. 2) Periodic modulation [24], [26], [29]-[34]: adjusting the carrier frequency periodically, usually, triangular, sinusoidal and exponential modulation profile are preferred. 3) Random modulation [21], [35]-[42]: varying one or more gating signal parameters (switching frequency, pulse width and pulse position) randomly to spread the harmonic energy. 4) Chaotic modulation [13], [43], [44]: utilizing erratic and irregular chaotic signal generated by chaotic map or circuit to change switch signal. As an example, **Fig. 2** shows the performance of the periodic modulation based spread frequency modulation, in which the narrowed and sharp harmonic clusters are attenuated effectively.

Furthermore, spread spectrum methods can be classified according to whether switching frequency is changed or not. In those methods the switching frequency is variable, the carrier generation schemes can also be divided into two types. The first one is adding a voltage controlled oscillator into the control circuit, and changing the frequency of the carrier by tuning the hardware component parameters. Another one is based on the interrupt module of microchips like advanced RISC machines (ARM), digital signal processor (DSP), FPGA and etc. Its detailed carrier frequency adjustment process is: the controller writes next predetermined count period and interrupt trigger into control registers each time when the whole interrupt count period is finished. The second method is preferable, since no additional circuit is needed. However, in the conventional interrupt module, the response of control word of new switching frequency needs to wait for the accomplishment of last counting cycle. Thus, a delay exists and it also brings extra consideration and computational burden to the design of the frequency modulation profile. The difference between analog and digital carrier generator mention above is intuitively displayed in **Fig. 3**.

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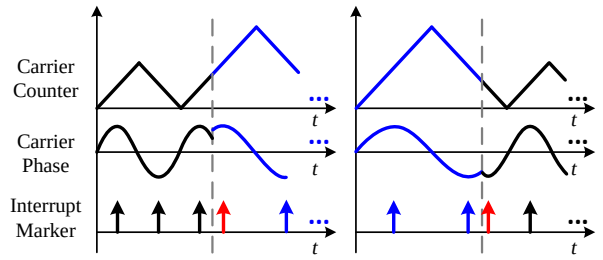
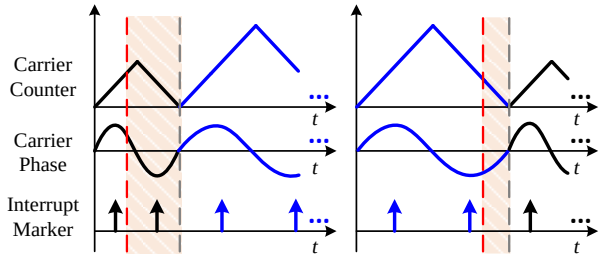


(a) The high frequency switches to the low frequency (b) The low frequency switches to the high frequency

Fig. 4. The frequency switching effect of the real time modification.



(a) The high frequency switches to the low frequency (b) The low frequency switches to the high frequency

Fig. 5. The frequency switching effect of the full period modification.

In order to avoid the delay of the frequency control and make the whole process smoother, the implementation and disadvantage of the conventional carrier generation method are discussed in detail. Then, a brief introduction to the direct digital frequency synthesizer (DDS) theory [45], [46] is done. Based on DDS, a wait-free phase-continuous carrier frequency modulation strategy (WPCFM), easy to implement, is proposed. Comprehensive analysis about WPCFM, including quantization error, frequency jitter, phase delay and voltage distortion are presented, and design method for the control parameters are derived. Analysis shows that the WPCFM has a smaller delay and simpler than the conventional methods. Furthermore, as the FPGA has many advantages at high switching frequencies [47]-[50], a Zynq-7000 system-on-a-chip (SoC) [51] based WPCFM implementation and control structure is presented in this paper. Finally, the effectiveness of WPCFM is verified by several sets of experiments where classical periodic carrier frequency modulations are applied.

II. Traditional Interruption Mechanism and DDS Strategy

In motor drives, the carrier and interrupts are related to the switching state of the power device and the sequential logic of the current control. Thus, the key point of the carrier frequency modulation is to guarantee no erroneous trigger and timing disorder of current loop control logic. In other words, the phase of the carrier need to be continuous during the modulation process and it is described in detail in the following discussion. In this section, two kinds of classical interruption mechanisms, real time modification and full period modification, are discussed. Besides, the DDS strategy is introduced in brief.

A. Real Time Modification

Most of the microchips have well-established interruption modules. In the case of timer interruption, each module has a timing counter, a counting threshold register and a phase trigger register. Each time the control clock arrives, the value of timing counter will be plus one or minus one. When the counting value reaches the phase trigger or threshold, an interruption happens and the timing counter is emptied. Hence, users can adjust the frequency and trigger easily by modifying the control words.

Assuming that the timing counter is an N-bit register, the counting threshold is M, step length is 1, and the frequency of control clock is f_c. Considering the Shannon theory and taking a sine signal as an example, the signal $\varphi_T(t)$ which is generated by a classical method can be expressed as

$$\varphi_T(t)=\sin\left(2\pi\frac{f_c}{M}t\right)\ ,\{M|1<M<2^{N-1}\} \tag{1}$$

Furthermore, using the number of steps n to replace variable t. (1) can be rewritten as

$$\varphi_T(n)=\sin\left(2\pi\frac{f_c}{M}\frac{n}{f_c}\right)=\sin\left(2\pi\frac{n}{M}\right)\ ,\{M|1<M<2^{N-1}\} \tag{2}$$

On the basis of (2), the frequency adjustment process of real time modification is to modify the counting threshold and phase trigger as long as the new frequency instruction is generated, even if the last counting period is not finished. Although real time modification is fast enough, it might cause a phase discontinuity of the signal and spurious triggering of the interruption, which can be shown in **Fig. 4**. The predetermined phase triggers in **Fig. 4** are 0.5π and 1.5π (they are arranged at the crest and trough of the sine wave). The frequency of carrier is changed directly at the dotted line. The red arrow is a spurious triggering of the interruption.

B. Full Period Modification

According to the analysis of real time modification, the reason of the phase discontinuity of the signal from real time modification is the modification of the control word that does not take the phase of current count state into consideration. Thus the full period modification in which the adjustment position is fixed at the end of the last counting period (the phase is zero) can solve this problem easily. In detail, if several instructions are happening during the waiting state, only the newest one is updated. To sum up, full period modification guarantees the continuous phase of the signal at the expense of the delay. The frequency switching progress and the waiting phenomenon of the full period modification are shown in **Fig. 5**. The instruction is written into the control register at the moment of the red dotted line. However, the new instruction can only be responded at the gray dotted line (the nearest point that its phase is zero).

C. Digital Frequency Synthesizer

The direct digital frequency synthesizer (DDS) strategy was proposed in 1971 and this method can achieve frequency synthesizing and adjust the frequency of signal on-line from the concept of phase. Nowadays, it is applied into radar, communications, electronic countermeasures, instruments and

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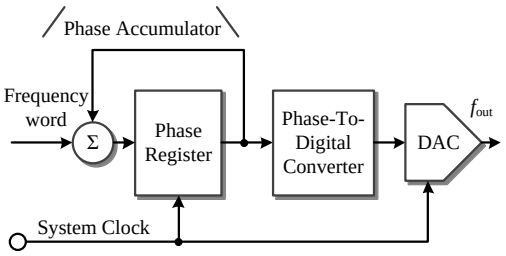
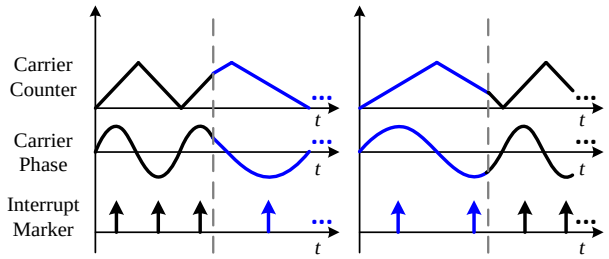


Fig. 6. The direct digital frequency synthesizer schematic diagram.



(a) The high frequency switches to the low frequency (b) The low frequency switches to the high frequency

Fig. 7. The frequency switching effect of the direct digital frequency synthesizer.

other fields. **Fig. 6** shows a schematic diagram of the classical DDS algorithm. A phase accumulator is used to count the frequency word and control the phase of the signal directly.

Assuming the timing counter is an N-bit register with a step length of K(K∈N+), and the frequency of the control clock is f_c. Considering the Shannon theory and taking the sine signal as an example, the signal $\varphi_P(t)$ which is generated by the DDS can be expressed as

$$\varphi_P(t)=\sin\left(2\pi\frac{K}{2^N}f_c t\right)\ ,\left\{K\middle|1<K<2^{N-1}\right\} \tag{3}$$

Furthermore, using the number of steps n to replace variable t, (3) can be rewritten as

$$\varphi_P(n)=\sin\left(2\pi\frac{K}{2^N}f_c\frac{n}{f_c}\right)=\sin\left(2\pi\frac{K}{2^N}n\right)\ ,\left\{K\middle|1<K<2^{N-1}\right\} \tag{4}$$

According to (4), dislike real time modification and full period modification, the modification of K, instead of the threshold, is used to achieve the carrier and make the interruption. In addition, the trigger condition is also changed from reaching the phase trigger to crossing the phase trigger. Owing to those slight changes, a delay-free phase-continuous carrier frequency modulation becomes possible. In **Fig. 7**, the frequency switching process is given out.

III. Performance Evaluation and Parameter Design

According to the comparison above, the DDS can be a good candidate to generate the carrier for WPCFM. In order to assess the DDS comprehensively, analyses of the DDS including quantization error, frequency jitter, phase delay and voltage distortion are presented, and design formulas of the control parameters are given also. Furthermore, the design methods of the WPCFM control parameters are presented.

A. Quantization Error

Assuming that the DDS and full period modification (FPM) have the same N and f_c, and the frequency of the desired output signal is f_e (f_e<f_c/2). The control parameter K and M of the DDS and FPM can be calculated as

$$\begin{cases} K=\left\lfloor 2^N\dfrac{f_e}{f_c}+\dfrac{1}{2}\right\rfloor \\ M=\left\lfloor \dfrac{f_c}{f_e}+\dfrac{1}{2}\right\rfloor \end{cases} \tag{5}$$

The integral function in (5) is the cause of the quantization error. Supposing K^* and M^* are the ideal parameters without quantization error, and the actual frequencies of the signals which are generated by DDS and FPM are f_P and f_T by considering the quantization error. The absolute errors $\Delta f_P(f_e)$ and $\Delta f_T(f_e)$ of f_P and f_T with the expected frequency f_e can be given as

$$\begin{cases} \Delta f_P(f_e)=|f_e-f_P|=\left|\dfrac{f_c}{2^N}K^*-\dfrac{f_c}{2^N}K\right|=\dfrac{f_c}{2^N}\left|2^N\dfrac{f_e}{f_c}-\left\lfloor 2^N\dfrac{f_e}{f_c}+\dfrac{1}{2}\right\rfloor\right| \\ \qquad\le\dfrac{f_c}{2^N}\cdot\dfrac{1}{2}=\dfrac{f_c}{2^{N+1}} \\ \Delta f_T(f_e)=|f_e-f_T|=\left|\dfrac{f_c}{M^*}-\dfrac{f_c}{M}\right|=f_c\left|\left(\dfrac{f_c}{f_e}\right)^{-1}-\left(\left\lfloor\dfrac{f_c}{f_e}+\dfrac{1}{2}\right\rfloor\right)^{-1}\right| \\ \qquad\le f_c\left|\left(\left(\dfrac{f_c}{f_e}-\dfrac{1}{2}\right)\right)^{-1}-\left(\dfrac{f_c}{f_e}\right)^{-1}\right|=\dfrac{f_e^2}{2f_c-f_e} \end{cases} \tag{6}$$

According to (6), the upper bound functions of $\Delta f_P(f_e)$ and $\Delta f_T(f_e)$, which are $\Delta f_{P\inf}(f_e)$ and $\Delta f_{T\inf}(f_e)$, can be given as

$$\begin{cases} \Delta f_{P\inf}(f_e)=\dfrac{f_c}{2^{N+1}} \\ \Delta f_{T\inf}(f_e)=\dfrac{f_e^2}{2f_c-f_e} \end{cases} \tag{7}$$

Differentiating $\Delta f_{T\inf}(f_e)$ on f_e

$$\frac{\mathrm{d}\Delta f_{T\inf}(f_e)}{\mathrm{d}f_e}=\frac{2f_e(2f_c-f_e)+f_e^2}{(2f_c-f_e)^2}=\frac{-f_e(f_e-4f_c)}{(2f_c-f_e)^2} \tag{8}$$

As f_e<f_c/2 (based on Shannon sampling theorem), there has f_e<4f_c. Thus, according to (8), $\Delta f_{T\inf}(f_e)$ is monotonically increasing in period of (0, f_c/2). Considering $\Delta f_{P\inf}(f_e)$ to be a constant and the cross over point of $\Delta f_{T\inf}(f_e)$ and $\Delta f_{P\inf}(f_e)$ f_{ec} is positive， f_{ec} can be expressed as

$$f_{ec}=\frac{\sqrt{1+2^{N+4}}-1}{2^{N+2}}f_c\ \ ,\left\{f_{ec}\middle|0<f_{ec}<\frac{f_c}{2}\right\} \tag{9}$$

Considering any frequency within the modulation range, can be an expected frequency for system to response, if the lowest modulation frequency is larger than f_{ec}, $\Delta f_{P\inf}(f_e)$ is better than $\Delta f_{T\inf}(f_e)$. Assuming x = f_{ec}/ f_c (0<x<0.5), the describing equation of the control parameter N can be expressed as

$$\frac{\sqrt{1+2^{N+4}}-1}{2^{N+2}}=\frac{f_{ec}}{f_c}=x \tag{10}$$

According to (10), N can be calculated as (because N is a positive integer, top integral function is used)

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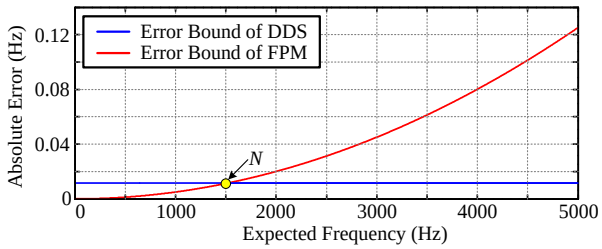

Fig. 8. The error comparison between the direct digital frequency synthesizer and the full period modification.

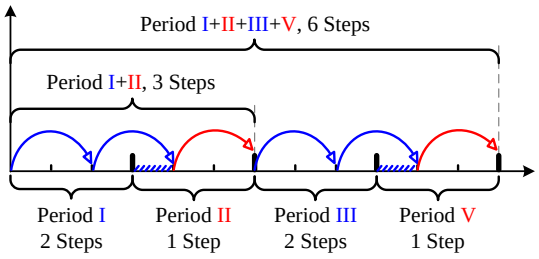

Fig. 9. The frequency jitter of the direct digital frequency synthesizer.

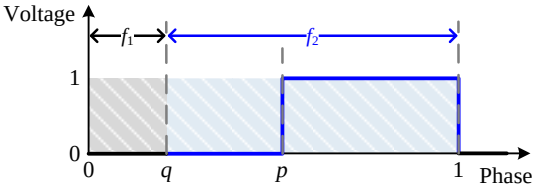

Fig. 10. The voltage distortion caused by the PWM frequency modulation.

$$N=\left\lceil \log_2\left(\frac{2-x}{x^2}\right)-1\right\rceil \tag{11}$$

Fig. 8 shows a the comparison $\Delta f_{Tinf}(f_e)$ and $\Delta f_{Pinf}(f_e)$ in the case of f_c=100 MHz, N=32.

B. Quantization Error

Because the interruption triggering condition of the DDS, in contrary to FPM, is the phase of the counter whether crosses the phase trigger or not, the frequency jitter might exist in the DDS-based carrier signal.

Ideally, the steps required to complete each counting period R^* can be expressed as

$$R^*=2^N/K \tag{12}$$

Actually, considering the influence of the discrete counting, when the initial value is zero, the steps required to complete each counting period R_+ can be expressed as

$$R_+=\left\lceil 2^N/K\right\rceil \tag{13}$$

However, if R^* is not an integer, the remaining margin will be accumulated to the next period, after each time the counting period is finished. Until these remaining numbers are accumulated to more than one complete step length, the steps required to complete each counting period R_+ changes to R_-, which can be expressed as

$$R_-=\left\lfloor 2^N/K\right\rfloor \tag{14}$$

In **Fig. 9**, the counting threshold is 3, the length of step is 2. Because the margin exists, the blue counting period need 2 steps, but 1 step is enough for red period. However, in general, 1.5 step is needed for one counting period.

Taking the frequency overlap effect [52], [53], the frequency of jitter f_R can be calculated as

$$f_{R(k\in N)}=\begin{cases}\left(R^*-k\right)\dfrac{K}{2^N}f_c & ,R^*\in[k,k+0.5)\\ \left(k+1-R^*\right)\dfrac{K}{2^N}f_c & ,R^*\in[k+0.5,k+1)\end{cases} \tag{15}$$

Because there is a periodic or random change of the carrier frequency in SSCG, the frequency jitter in DDS is acceptable, especially when f_e << f_c. It is also worth mentioning that the frequency jitter is the reason for why DDS has lower frequency error upper bound than FPM.

C. Phase Delay

In motor drives, the adjustment of the carrier frequency changes the switching frequency of the power device and the modulation frequency of PWM. Usually, the zero order holder (ZOH) model is widely used to analyze the delay of PWM [50], [54]. Taking the dual sample dual update (DSDU) method into consideration [50], the actual delay constant is half of the switching period. The transfer function of ZOH $G_h(s)$ can be given as (f_s is the switching frequency)

$$G_h(s)=\left.\frac{1-e^{-sT_h}}{s}\right|_{T_h=1/(2f_s)}=\frac{1-e^{-s/(2f_s)}}{s} \tag{16}$$

Substituting s=jω into (16) yields

$$G_h(\mathrm{j}\omega)=\frac{2e^{-\mathrm{j}\omega/(4f_s)}\left(e^{\mathrm{j}\omega/(4f_s)}-e^{-\mathrm{j}\omega/(4f_s)}\right)}{2\mathrm{j}\omega}=\frac{1}{2f_s}\cdot\frac{\sin\left[\omega/(4f_s)\right]}{\omega/(4f_s)}e^{-\mathrm{j}\omega/(4f_s)} \tag{17}$$

According to (17), the phase of $G_h(s)$ can be expressed as

$$\angle G_h(s)=\angle e^{-\mathrm{j}\omega/(4f_s)}=-\frac{\pi}{2}\cdot\frac{f}{f_s} \tag{18}$$

Assuming the initial carrier frequency of FFPWM is f_m, the increased phase lag percentage ΔP of the system when the switching frequency reduced by Δf can be given as

$$\Delta P=\frac{\Delta f}{f_s-\Delta f} \tag{19}$$

According to (19), if the acceptable maximum phase lag increment is ΔP_m, the lowest frequency f_L during the modulation process can be calculated as

$$f_L=f_s-\Delta f>\frac{f_s}{1+\Delta P_m} \tag{20}$$

It is worth mentioning that a wider modulation range also means a better EMI reduction effect on the premise of unfolding of the frequency. Thus, there is a trade-off between stability and performance, and a moderate modulation range is recommended.

D. Voltage Distortion

The DDS algorithm is able to response to new instructions directly and ensure that the whole process is phase continuous. However, because the output voltage of the PWM method comes from the time domain integral, the frequency switching

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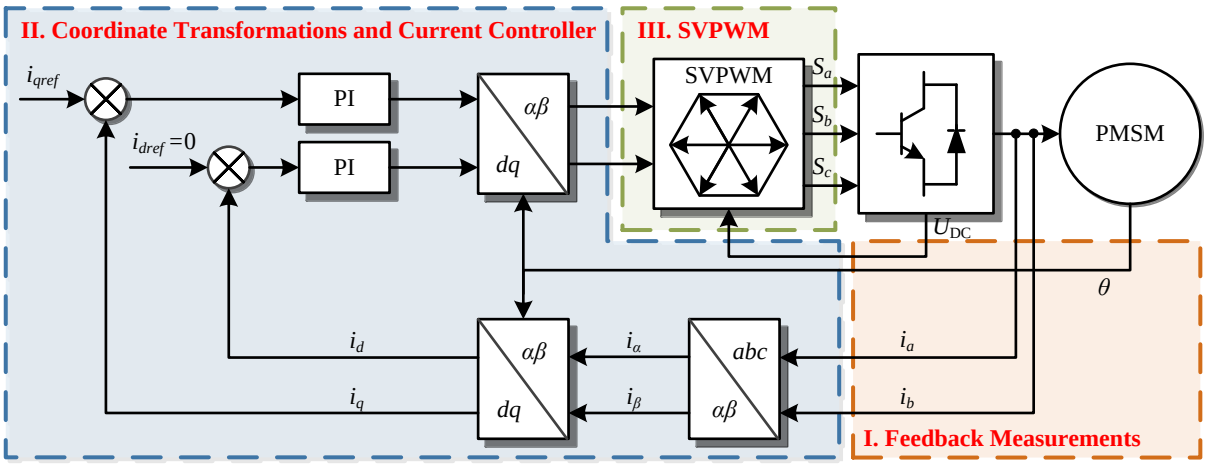

Fig. 11. The current control framework of the surface permanent magnet synchronous motor.

process leads to voltage distortion. In **Fig. 10**, a simple PWM model is built up to evaluate the voltage distortion in this part.

In **Fig. 10**, q represents the phase node of the frequency switching and p is the phase node of level conversion (from 0 to 1). Assuming the constraint of q and p can be given as

$$0 \le q \le p \le 1 \tag{21}$$

Suppose that f_1 and f_2 to represent the carrier frequency before and after the switching respectively, $T_1=1/f_1$, $T_2=1/f_2$, and that only one time of frequency switching exists in each period. The expected average voltage U_E and actual average voltage U_R can be expressed as

$$\begin{cases} U_E = 1-p \\ U_R = \dfrac{(1-p)T_2}{qT_1+(1-q)T_2} = \dfrac{(1-p)f_1}{qf_2+(1-q)f_1} \end{cases} \tag{22}$$

Through observations, it can be seen that a maximum voltage distortion appears in the case of $q = p$. Assuming that $f_2=f_1 \pm \Delta f$, the bound of actual average voltage U_{RB} can be given as

$$U_{RB} = \frac{(1-p)f_1}{p(f_1 \pm \Delta f)+(1-p)f_1} = \frac{(1-p)f_1}{f_1 \pm p\Delta f} \tag{23}$$

Also assuming that $\Delta U_m (0<\Delta U_m<1)$ represents the acceptable maximum voltage distortion ΔU_m, the constraint of Δf can be expressed as

$$\left|U_E - U_{RB}\right| = \left|(1-p) - \frac{(1-p)f_1}{f_1 \pm p\Delta f}\right| < \Delta U_m \tag{24}$$

Based on (24), by discussing the case of frequency increase and reduction separately, the design equations of Δf can be given as

$$\begin{cases} (1-p) - \dfrac{(1-p)f_1}{f_1 + p\Delta f} < \Delta U_m \\ \dfrac{(1-p)f_1}{f_1 - p\Delta f} - (1-p) < \Delta U_m \end{cases}, \{p \mid 0<p<1\} \cap \{\Delta U_m \mid 0<\Delta U_m<1\} \tag{25}$$

Using a reasonable scaling to eliminate the parameter p and assuming the modulation range of frequency to be $[f_L, f_U]$, (25) can be rewritten as

$$\begin{cases} \Delta f < \dfrac{-\Delta U_m}{p\left[p-(1-\Delta U_m)\right]} f_1 < \dfrac{4\Delta U_m}{(1-\Delta U_m)^2} f_L \\ \Delta f < \dfrac{-\Delta U_m}{p\left[p-(1+\Delta U_m)\right]} f_1 < \dfrac{4\Delta U_m}{(1+\Delta U_m)^2} f_L \end{cases}, \{\Delta U_m \mid 0<\Delta U_m<1\} \tag{26}$$

By preserving a minimum constraint in (26), the finally constraint of Δf can be given as

$$\Delta f < \frac{4\Delta U_m}{(1+\Delta U_m)^2} f_L \ , \{\Delta U_m \mid 0<\Delta U_m<1\} \tag{27}$$

The tuning of Δf based on (27) can limit the voltage distortion within a reasonable range and avoid excessive current fluctuation during the frequency switching process.

IV. SoC-Based WPCFM Implementation Method and Control Structures

A. Algorithm Implementation

The classical PI current control structure of the surface permanent magnet synchronous motor (SPMSM) can be shown as **Fig. 11**. According to sequential logic, the interruption of the algorithm can be divided into three groups as follows

I. Feedback Measurement: Detecting the phase currents, bus voltage and rotor position.

II. Coordinate Transformation and Current Controller: Dealing with feedback signal and obtaining voltage reference from PI controller.

III. SVPWM: Calculating the switching time of the power device and update the registers twice each period.

In the DSDU model, after updating the switching time in the control register, SVPWM generates six new phase triggers. Except the switching time, the phase triggers of other control interruptions are not changed. Since the adjustment of the switching time register only happens at the time when the half carrier is finished, no erroneous interruption exists during the whole process, which is one of the reasons that DDS can be applied into motor drives.

Based on the aforementioned classification, the typical control sequence on triangular carrier is illustrated in **Fig. 12**. The red, blue and green arrows are correspond with the

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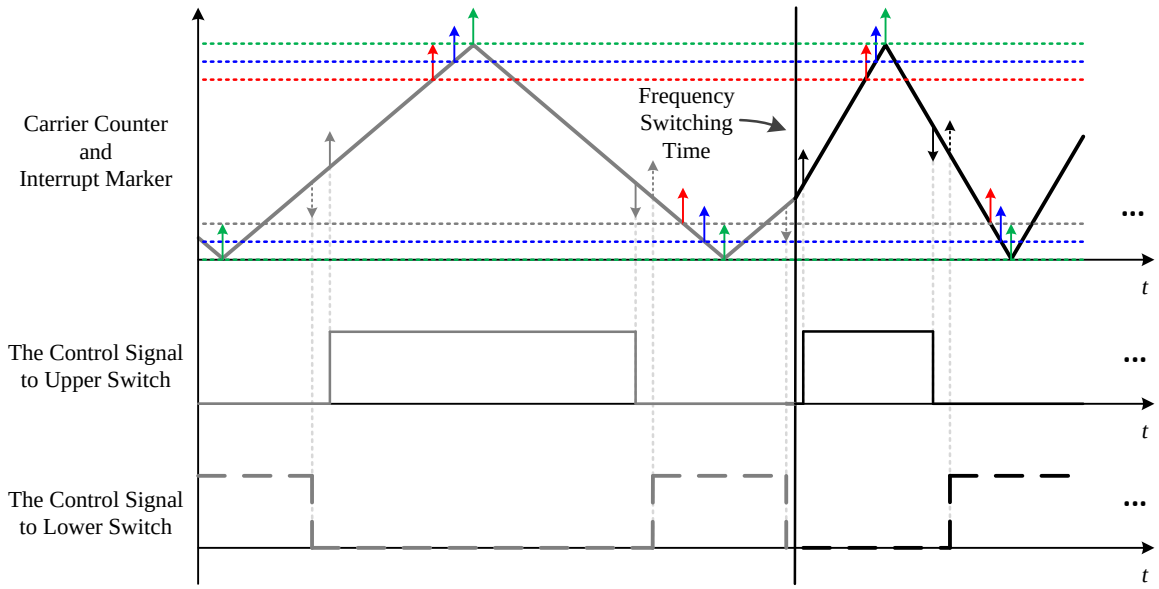

Fig. 12. The sequence diagram of the current control (The color of the interrupt marker is corresponding to the interruption in **Fig. 11**).

interruption I, II and III in **Fig. 11** respectively. Meanwhile, the gray and black arrows are the phase triggers of the switch device state reversal. Owing to the parallel operation mode of FPGA, the sampling of the current and voltage can be built as an independent module in order to simplify the control structure. Besides, the interruption phase of reading the rotor position need to take the communication delay of encoder into consideration. In this paper, a 2500 impulses/revolution incremental optical encoder is used in the experiment platform. The communication delay can be ignored. Thus, each time the interruption I happens, only a short clearance is needed for the measurement module to prepare the feedback signal for the next calculation. In interruption II, the coordinate transformations and current control can be finished within 40 steps (control clocks). Because the frequency of the control clock is 100 MHz, the whole process needs 0.4 us. The phase margin of trigger can be calculated based on the upper limit of the predetermined modulation frequency. As for interruption III, actually, the switching time calculation can also be finished in the program of interruption II. Thus, the FPGA only needs to update the switching time register when interruption III happens and control the state of power device during half of the next carrier period.

The generation of dead time has a phase margin problem either. There are two kinds of solutions. The first one is to give a conservative phase margin estimation of the dead time according to the upper limit of the predetermined modulation frequency like interruption II. However, an oversized dead time means a poor quality of the current and the extra torque ripple. Besides, the second method is to fix the step number of the dead time, which can be shown in **Fig. 13**.

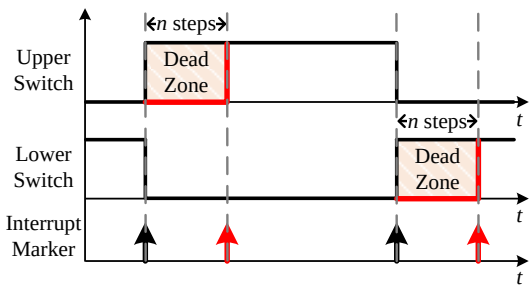

Fig. 13. The generation process of the dead time in a half-bridge in the inverter.

In **Fig. 13**, the turn off signal of the upper and lower switch is the original control signal, but there is fixed n steps delay in turn on action than initial signal. Hence, because the step number is related to the time length directly and it is fixed, whether the step length is changed or not, the delay time of dead time is fixed and the margin do not need to be too conservative.

B. Control Structures and Controller Design

The control structure of SoC-based (which integrates ARMs and FPGA into one chip) WPCFM motor drive is shown as **Fig. 14**. $G_{ASR}(s)$ is the transfer function of speed controller. $G_c(s)$ and $G_m(s)$ represent the transfer function of the current loop and mechanical part respectively. The output of $G_{ASR}(s)$ is the current reference in q-axis i_{qr}, and it is calculated from the difference between the speed reference ω_r and motor speed ω. The electromagnetic torque T_e comes from the $G_c(s)$ and it is used to drive motor. One ARM is responsible for speed loop control and the generation of frequency modulation instruction. In addition, the program in ARM is triggered by an external interrupt from the FPGA with a fixed frequency. Using this design, the traditional constant step length discrete control theory is still applicable for this control structure. Besides, the phase of the current and rotor position sampling is fixed in the carrier, which can guarantee the current vectors is precise and fully decoupled. Nevertheless, the controller in the ARM can also be triggered by the WPCFM. However, it needs to introduce a variable step length for applying discrete control theory and it increases programming burden. Thus, the

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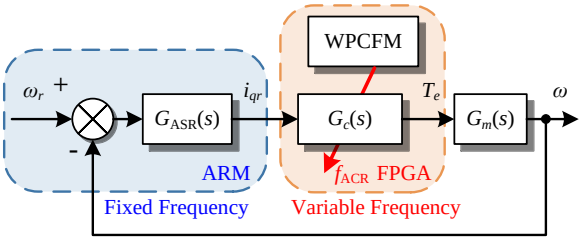

Fig. 14. The wait-free phase-continuous carrier frequency modulation strategy based control structure.

structure in **Fig. 14** is finally adopted in the experiment of this paper. Owing to the WPCFM, only one parameter, the step length in carrier generation, is needed for adjusting the switching frequency.

In addition, the classical PI structure based current and speed controller are selected for system dual closed-loop control. Based on the theory in [55], the transfer function of current controller $G_{ACR}(s)$ and speed controller $G_{ASR}(s)$ can be given as

$$\begin{cases} G_{ACR}(s)=K_{cp}(1+K_{ci}/s) \\ G_{ASR}(s)=K_{sp}(1+K_{si}/s) \end{cases} \tag{28}$$

in which K_{cp} and K_{ci} represent the proportional and integral gain of current controller, while K_{sp} and K_{si} are the proportional and integral gain of speed controller.

Next, in the situation that the expected closed-loop bandwidth of current loop ω_{cc} is much higher than that of speed loop ω_{sc}, the PI parameters in (28) can be calculated as

$$\begin{cases} K_{cp}=L\omega_{cc} \\ K_{ci}=R/L \\ K_{sp}=J\omega_{sc}/K_T \\ K_{si}=\omega_{sc}/5 \end{cases} \tag{29}$$

in which L and R represent the phase inductance and phase resistance of the SPMSM respectively; K_T is the torque constant and J is the moment of inertia. All of these values are constant and predetermined.

Setting T_{ACR} and T_{ASR} as the sampling period of current loop and speed loop, and applying Tustin transformation to discretize the PI controller in (29), the equations of controller parameters in discrete model can be expressed as

$$\begin{cases} K_{cpdis}=K_{cp}-\dfrac{K_{cp}K_{ci}T_{ACR}}{2}=L\omega_{cc}\left(1-\dfrac{R}{2L}T_{ACR}\right) \\ K_{cidis}=\dfrac{2K_{ci}T_{ACR}}{2-K_{ci}T_{ACR}}=\dfrac{2RT_{ACR}}{2L-RT_{ACR}} \\ K_{spdis}=K_{sp}-\dfrac{K_{sp}K_{si}T_{ASR}}{2}=\dfrac{J\omega_{sc}}{K_T}\left(1-\dfrac{\omega_{sc}T_{ASR}}{10}\right) \\ K_{sidis}=\dfrac{2K_{si}T_{ASR}}{2-K_{si}T_{ASR}}=\dfrac{2\omega_{sc}T_{ASR}}{10-\omega_{sc}T_{ASR}} \end{cases} \tag{30}$$

in which K_{cidis} and K_{cpdis} are the integral and proportional gain of current controller in z-domain; K_{sidis} and K_{spdis} are the integral and proportional gain of speed controller in z-domain.

Because the variation range of switching frequency is small (in most situation is from 9 kHz to 11 kHz) in this paper and the on-line adjustment of PI parameters increases the computing burden of FPGA, the parameters of PI current controller are fixed (setting $f_{ACR} \equiv 20$ kHz, $T_{ACR} \equiv$ 5e-5 s). Besides, taking the anti-windup of PI controllers into consideration, the incremental structure is used in current controller while the integration weakening PI regulation strategy is applied in speed controller.

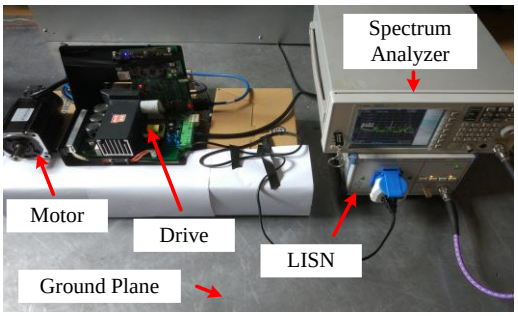

Fig. 15. Experimental setup.

TABLE I: MAIN PARAMETERS OF 750W SPMSM

Parameter	Value
Motor Power	750 W
Nominal Motor Torque	2.39 N·m
Nominal Motor Speed	3000 rpm
Nominal Current	3 A
Phase Inductance	3.9e-3 H
Phase Resistance	2.88 Ω
Poles	4
Motor Inertia	1.82×10^{-4} kg·m^2

V. EXPERIMENTAL RESULTS

Fig. 15 shows the EMI experimental setup of WPCFM. The specifications of the motor are presented in **Table I**. An impedance stabilization network (LISN, R&S ENV216) is connected between the power source and the drive. Considering the switching frequency is relatively low ($\leqslant$12 kHz), the EMI signal from LISN is measured on a spectrum analyzer (Agilent N9320B) which is set to peak mode with a 10 Hz resolution bandwidth (RBW). All instruments are placed on an earthed conductive plane and the structure is match with **Fig. 1**. In order to reduce Δf while keeping the modulation profile unchanged, the interruption frequency of ARM is raised to 10kHz (f_{ASR}) and the speed measurement method mentioned in [53] is used to improve the accuracy of speed feedback. The control chip is Xilinx Zynq series SoC, which integrates ARM (two Cortex-A9s but only one is used) and FPGA into one chip. The communication between ARM and FPGA is realized by advanced eXtensible interface (AXI) bus inside SoC. In addition, the random access memory (RAM) of Zynq is extended to 1 GB by adding external memory chip to record experiment data. In the experimental of WPCFM with periodic triangular wave, the f_c of FFPWM and WPCFM are both 100 MHz. The carrier frequency of FFPWM (equal to switching frequency f_s) is fixed as 10 kHz. The counting register of WPCFM is 32-bit. For verifying the effectiveness

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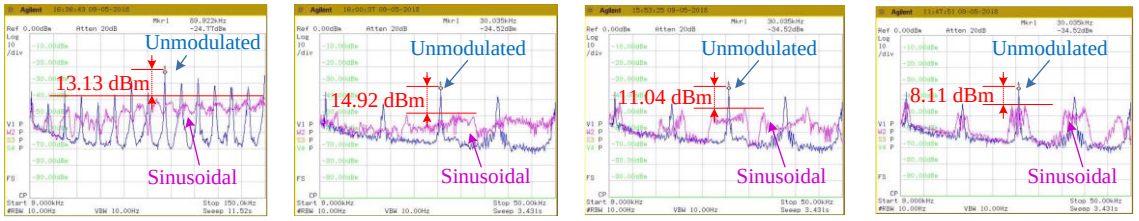
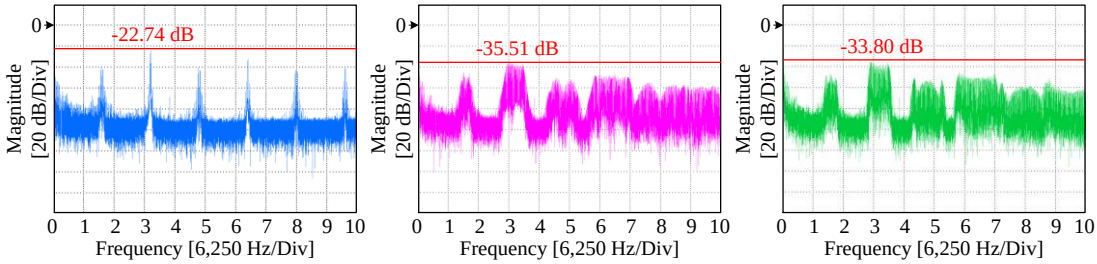
(a) Δf_s =1 kHz, f_m =100 Hz. (b) Δf_s =2 kHz, f_m =50 Hz. (c) Δf_s =1 kHz, f_m =100 Hz. (d) Δf_s =500 Hz, f_m =200 Hz.

Fig. 16. The performance of the WPCFM based triangular spread spectrum frequency modulation.



(a) Δf_s =1 kHz, f_m =100 Hz. (b) Δf_s =2 kHz, f_m =50 Hz. (c) Δf_s =1 kHz, f_m =100 Hz. (d) Δf_s =500 Hz, f_m =200 Hz.

Fig. 17. The performance of the WPCFM based sinusoidal spread spectrum frequency modulation.



(a) Unmodulated (b) Triangular (c) Sinusoidal

Fig. 18. PSD results of phase currents under different modulation schemes.

of the control structure in **Fig. 14**, the experiment drive system is working in the speed control mode with speed reference is 1000 rpm. Besides, three top and bottom insulated gate bipolar transistors (IGBTs) are switching on or off simultaneously around 50% duty ratio [15], [24] to maximized the conducted EMI by making motor work in no-load state.

A. EMI Reduction

Fig. 16 and **Fig. 17** are the performances of triangular and sinusoidal modulation profile based on WPCFM algorithm. The spectrum from 9 kHz to 150 kHz is recorded in **Fig. 16 (a)** and **Fig. 17 (a)**, while only the data from 9 kHz to 50 kHz is shown in others. Δf_s is the peak deviation of the switching frequency and f_m is the frequency of modulation profile. m_f (= Δf_s / f_m) is the modulation index. Using the 3rd harmonic of the 10 kHz central frequency as a symbol, its amplitude decreases with the increases of triangular and sinusoidal profile modulation index. **Fig. 16 (b)** and **Fig. 17 (b)** have the largest m_f and the most obvious attenuation of the conducted EMI harmonic peak (triangular: 15.68 dBm, sinusoidal: 14.92 dBm), but the overlap (which has been shown in **Fig. 2**) is appear earlier. In general, compared with sinusoidal profile, triangular profile has better spread spectrum performance. Overall, the dominant EMI clusters in power spectral density (PSD) of WPCFM based periodical spread spectrum frequency modulation (SSFM) are spread effectively which coincides with the spread spectrum theory and also proves WPCFM is a qualified carrier for SSFM.

B. Harmonic Currents Suppression

Because the switching frequency of motor drive inverter is smaller than 20 kHz, the noise caused by switching action and harmonic currents is also acoustic. The harmonic clusters in phase current can also be a reference value to judge the performance of SSFM [35], [56]. In this part of experiment, the phase current is recorded by an oscilloscope (YOKOGAWA, DLM2054) with 1.25 MHz sampling frequency, and analyzed offline by its software kit Xviewer. In addition, the triangular and sinusoidal profile modulation have the same constant Δf_s (=1 kHz) and f_m (=100 Hz).The PSD results of phase currents under different modulation schemes are shown in **Fig. 18**. For example, the 2nd harmonic of the 10 kHz central frequency decreases from -22.74 dB (unmodulated) to -35.51 dB (triangular profile) and -33.80 dB (sinusoidal profile) remarkably. The outline envelops of the current spectrum are also in accordance with the periodical SSFM. Overall, the measured current spectrum shows similar results with the previous EMI reduction experiments.

C. Closed-Loop Control Performance

In order to evaluate the speed control performance of the system with WPCFM control structure, in **Fig. 19**, the speed step response in time domain is recorded. The speed and

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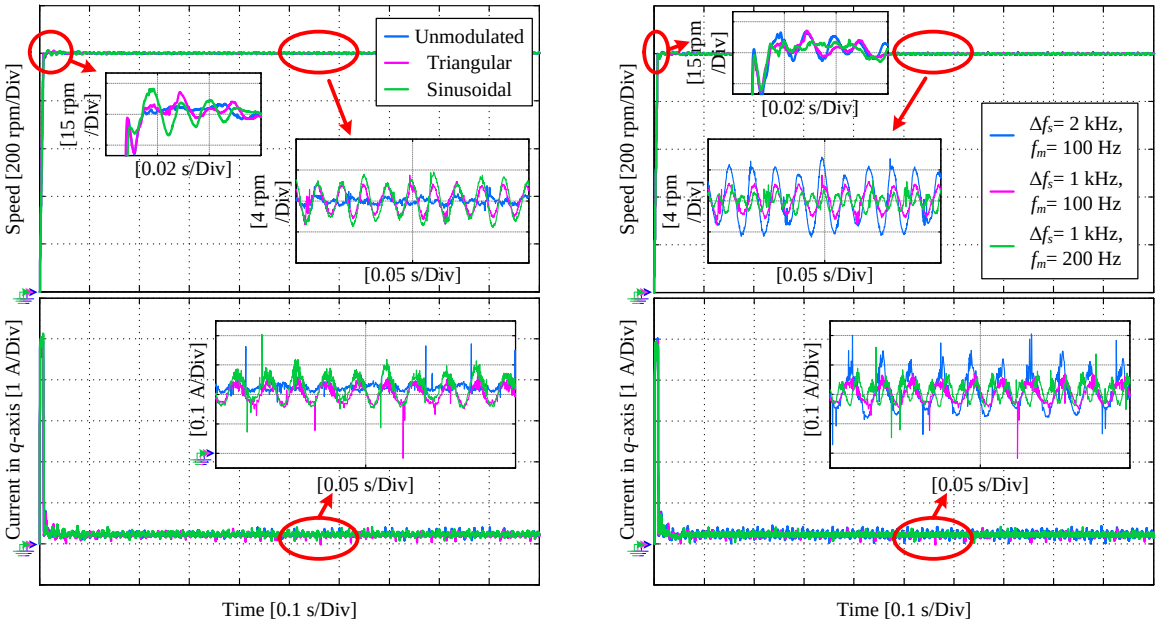

(a) Performance of systems with different modulation profiles (b) Performance of systems with different modulation parameters

Fig. 19. The speed step response of the system with the WPCFM control structure.

TABLE II: RMS VALUE OF THE MOTOR SPEED ERROR

Inertia Ratio J / J_m	Δf_s = 500 Hz, f_m = 50 Hz	Δf_s = 1000 Hz, f_m = 100 Hz	Δf_s = 1500 Hz, f_m = 150 Hz
1.00	1.902 rpm	1.854 rpm	1.554 rpm
3.84	0.644 rpm	0.571 rpm	0.538 rpm

current feedback of system with different modulation profile is shown in **Fig. 19 (a)**, the Δf_s and f_m of triangular and sinusoidal profile is also fixed as 1 kHz and 100 Hz respectively. The rise time of three kinds of modulation schemes is almost same, but the overshoot is larger after SSFM is adopted, especially under the sinusoidal profile modulation (nearly 15 rpm). The steady state fluctuation of sinusoidal profile ($\leqslant$4 rpm) is larger than that of triangular profile ($\leqslant$2.5 rpm) either, but the speed fluctuation frequency of this two kind of periodical SSFM is same (=100 Hz = f_m). Similar phenomenon is also exist in the q-axis current waveform. In **Fig. 19 (b)**, the comparison results under different control parameters are given out. Although a larger modulation index m_f commonly means better EMI reduction performance, the current and speed ripple also increase with the increase of m_f. There is an unavoidable trade-off between EMI reduction and a smooth output. Considering the EMI attenuation function with m_f is nonlinear [24], usually, a moderate m_f is preferred. Especially, in motor drive system, apart from current ripple, speed ripple is another important or even more priority index. Fortunately, the moment inertia of system can be regard as a self-equipped filter to damp the ripple impact caused by current to motor speed. According to **Fig. 19 (b)**, the ripple frequency of current is equal to the frequency of modulation profile f_m. More detailed, the root mean square (RMS) value of motor speed error under same m_f but different f_m is recorded in **Table II**. Considering motor has to equip with additional load inertia in most industrial applications, a set of comparison experimental results that under larger inertia is also given out (J_m is the inertia of motor itself). According to **Table II**, when m_f is fixed, the RMS of speed ripple decreases with the increase of inertia and f_m. It means, when inertia and m_f are fixed, the higher f_m can degrade the impact from the current ripple caused by SSFM and achieve smoother speed control performance.

To sum up, in the system with periodical SSFM, although the speed fluctuation is increased, the variation range is still acceptable. In order to avoid sharp current fluctuation, a moderate modulation index m_f ($10<m_f<20$) is recommended. Moreover, because the fluctuation frequency is equal to f_m, this disturbance can be absorbed by the inertia of system gradually when f_m becomes higher. Hence, when m_f is fixed, a higher f_m can reduce the ripple of motor speed. It also means that the WPCFM based SSFM is more suitable for wide band gap (WBG) motor drive systems (which can achieve higher f_s and f_m, but have more serious EMI pollution). Due to limitation of experiment platform, the verification of the proposed method on WBG devices (the platform is still being set up in our lab) will be our future focus.

D. Comparison of Wait and Wait-Free Algorithms

Owing to the redesign of carrier generation mode, the switching frequency adjustment order from SSFM can be executed without any delay using WPCFM. Compared with the wait algorithm, this wait-free method mainly has two advantages.

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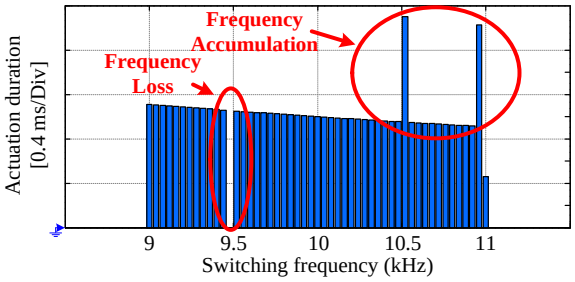
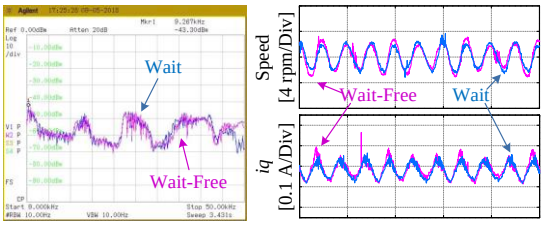


Fig. 20. The frequency accumulation phenomenon of the wait algorithm.



(a) EMI spectrum (b) Speed and current ripple

Fig. 21. Comparison results of wait and wait-free algorithms.

1) No frequency loss and accumulation: In **Fig. 20**, the frequency order update progress of the conventional wait method is simulated and the actuation time of different frequency orders during half of the triangular modulation period is recorded (f_c = 100 MHz, Δf_s = 1 kHz, f_s = 10 kHz, and f_m = 100 Hz). More detailed, the frequency order calculation frequency is 10 kHz and the order only can be updated at the beginning of each switching period. According to **Fig. 20**, due to the asynchrony between frequency order calculation and update, some orders are unable to be executed (frequency loss), and some orders are executed twice (frequency accumulation) probability during half of the modulation period. Although the switching frequency of conventional method is evenly distributed within a long time scale, the partial nouniform distribution still exists in some situations. As for wait-free algorithm, this problem is avoidable because the new frequency order can be executed immediately.

2) More feasible: After adding several order update judgement conditions and buffer registers, WPCFM can conveniently realize the switching between wait and wait-free mode. Moreover, users can randomly choose specific phase nodes on carrier wave to adjust the switching frequency. It means WPCFM is a more feasible algorithm. In additional, not only for EMI reduction, this DDS-based carrier frequency modulation strategy can also be used in other applications, like synchronous modulation, in which a larger range of on-line switching frequency adjustment is needed.

In **Fig. 21**, several comparison experiment results of wait and wait-free algorithms are given out. The Δf_s and f_m of wait and wait-free algorithms are fixed as 1 kHz and 100 Hz respectively, and the speed command of motor is 1000 rpm without any additional load inertia. The EMI reduction effects of wait and wait-free algorithms recorded by the spectrum analyzer are almost the same. Because within a long time scale, wait method can also achieve uniform distribution of switching frequency. Both wait and wait-free methods can spread the dominant clusters in frequency spectrum successfully. As for the current ripple of *q*-axis in **Fig. 21 (b)**, due to the voltage distortion caused by WPCFM (which have been discussed in Section. III), the fluctuation of wait-free method is slightly increased.

Overall, the proposed wait-free algorithm is more feasible and easy-implemented, but it has relatively larger current ripple than conventional method as a trade-off.

VI. Conclusion

In this paper, with the goal to reduce the delay of conventional variable carrier frequency SSCG, a DDS-based carrier generation method in a FPGA is adopted to replace the conventional interruption method in the microchip. The quantization error, frequency jitter, phase delay and voltage distortion of this strategy are modeled and analyzed comprehensively. Results show that the DDS-based carrier generation method can guarantee the phase continuity of waveform and no wait state is needed to update the instruction. In addition, this wait-free algorithm is more feasible and can be adjusted expediently according to the users' demands. Therefore, this paper has proposed an all-digital wait-free phase-continuous carrier frequency modulation strategy through reasonable current control logic and dead zone design. Besides, easily achieved algorithm and control structure are presented based on a SoC platform. The effectiveness of WPCFM is verified in several sets of experiments. Results prove that WPCFM is a qualified carrier for SSFM. To apply WPCFM to a wide band gap platform to fully demonstrate its advantages in higher switching frequency motor drive is the focus of future work.

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