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Investigation of Nonlinear Droop Control in DC Power Distribution Systems: Load Sharing, Voltage Regulation, Efficiency, and Stability

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***Abstract*— Linear droop faces the design trade-off between voltage regulation and load sharing due to cable resistances and sensing errors. Using a larger droop resistance improves load sharing, but requires a wider droop voltage range. In the nonlinear droop, droop resistance is a function of the converter's output current, and its value increases when the output current increases. As a result, the impacts from sensors and cables are reduced. In this paper, the design of nonlinear droop in dc power distribution systems is studied with special emphasis on load sharing, voltage regulation, system efficiency, and stability. After discussing the piecewise linear and nonlinear droop control, a generic polynomial expression is presented to unify different droop equations. The impact of droop on dc system efficiency is analyzed by evaluating cable and power converter losses. The converter's output impedance using nonlinear droop is modeled to analyze the system stability with constant power loads. The selection and design guidelines of nonlinear droop are summarized, considering both the static performance and interaction with load systems. The analysis is verified in 400-V multi-source dc systems. The nonlinear droop is fully distributed as it only needs local information.**

***Index Terms*—Constant power load, current sharing, dc microgrids, droop, efficiency, nonlinear, stability, voltage regulation.**

I. INTRODUCTION

Droop control has been broadly used in power module paralleling, ac microgrids, and dc microgrids. One main advantage of droop control is its ability to achieve load sharing among paralleled power sources without dedicated communication links; thus, distributed and reliable system control can be realized.

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In traditional ac power systems, the concept of droop has been adopted for sharing active and reactive power among numerous synchronous generators tied to the same power grid. Specifically, the active power is shared by frequency droop, while the reactive power is shared by voltage droop [1], [2].

Similarly, droop control has been used in dc power distribution systems for data centers, electric vehicles, and dc microgrids [3]–[8]. In the popular voltage-current droop (V-I droop), each power converter adjusts its output voltage when its output current changes; thus, a steady-state load sharing can be achieved. In addition, droop control has been designed with different voltage set-points to prioritize different energy sources, e.g., electric utility, renewable energy, and energy storage. The system energy management has been optimized for targets such as net-zero energy cost [9], [10]. A variety of power module paralleling methods are reviewed in [11], where droop methods are classified into five categories according to their implementations, i.e., 1) converters' inherent droop feature [12]; 2) series resistor; 3) output current feedback; 4) current mode with low dc gain; and 5) scheduling control via nonlinear gain [13].

In practice, discrepancies between power converters, sensors and cable resistances influence the droop performance. Traditional droop control, i.e., the linear droop, adopts a constant droop resistance and faces a design trade-off between voltage regulation stiffness and load sharing accuracy. Using a large droop resistance improves the load sharing but generates a large output voltage deviation under heavy load. Reducing the droop resistance improves the voltage regulation but sacrifices the load sharing. In practical systems, the system bus voltage needs to stay within a predefined range to ensure all sources and loads connected to the bus can function properly. Similar to ac utility that typically allows a 5 % to 10 % frequency variation, ref [14] suggests allowing a total of 10 % dc bus voltage variation. If half of the total variation range, i.e., 5 %, is reserved for line voltage drops, the usable voltage range for droop control is only 5 %. As a result, the maximum droop resistance is limited.

A great amount of research has been done to improve the load sharing and voltage regulation of droop control. Generally speaking, these improvements can be classified into communication-based and communication-less methods.

If there are communication links between the converters, the bus voltage can be restored by transmitting the voltage and current information. For example, the output current of each converter can be sent to a communication link to aggregate the

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global load. Based on this information, the voltage set point of each converter is adjusted to compensate for the voltage drop of droop control [15], [16]. A three-level hierarchical control structure for microgrids is discussed in [2], where the first-level control is the traditional droop control, and the second-level control compensates the voltage deviation by shifting the voltage set points for different converters. Although these methods only require low-speed communication, physical communication lines still exist between power sources. Compared with the communication-less control strategies, communication-based methods increase the system cost and complexity.

Improvements without communication have the advantage of robustness and low cost. In [13], a gain scheduling method is proposed to adjust the gain of the voltage loop controller based on load conditions. The gain is selected by looking at a group of droop curves and choosing the curve that has the desired dc gain for each discretized segment. This improves the load sharing and keeps the same droop voltage range for paralleled ac-dc converters. Gain scheduling and fuzzy control are combined in [17] to optimize the operation of dc microgrids. The gain scheduling is also applied in ac utility to synchronize multiple generators [18]. However, the application of the gain scheduling is limited to proportional controllers. If the controller contains an integrator, this method can no longer be applied.

Another communication-less improvement is introduced in [19], [20] by splitting the droop range into segments. When the load exceeds a threshold, the system begins to use a larger droop resistance. This method uses different slopes to suppress the current sharing error caused by voltage measurement errors. However, the switch between different modes is abrupt. The sudden output resistance change of power converters may lead to undesired transients and oscillations.

A nonlinear droop control method is proposed in [21]. The performance of different second-order droop expressions, e.g., droop using parabolic and elliptic equations, is compared with linear droop. Later in [22], the work is extended by introducing higher-order polynomial droop expressions and power bidirectional experiments. Each work demonstrated that nonlinear droop has better performance than linear droop in achieving voltage regulation and load sharing. However, they did not consider the impact of droop control on system efficiency, leading to an overemphasis on the load sharing under light-load conditions. Also, the discussion is limited to two-source systems; experiments were not conducted for multi-source systems. Moreover, the nonlinear droop control alters the output impedance of power converters, which impacts the dc system stability. These issues need to be addressed.

This paper focuses on the approach that does not require any communication. As a continuation of the work presented in [21], this paper investigates the design and benefits of nonlinear droop control. Section II provides a quantitative analysis and measurement results showing the impact from cables and sensors. Section III introduces the concept of piecewise linear and nonlinear droop control. A general form of nonlinear droop control is presented to unify different droop equations. Different second-order droop functions are compared. Section IV explores the performance of nonlinear droop in the steady state, including voltage regulation, load sharing, and system efficiency. Section V evaluates the impact of nonlinear droop control on system stability by modeling the converter's output impedance and applying Bode and Nyquist stability criteria. Section VI shows experimental results for two-source and three-source dc systems. Conclusion and design guidelines are given in Section VII.

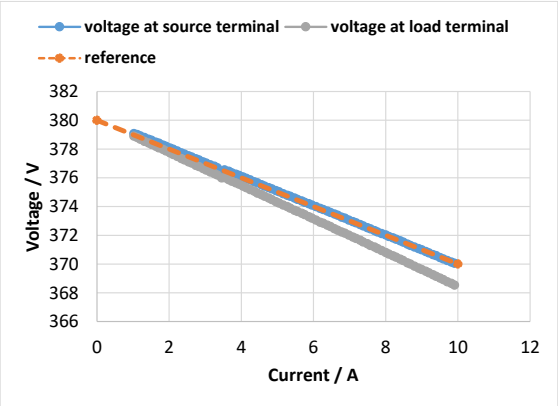

Fig. 1. Impact of line resistance on voltage distribution.

II. Factors Degrading Droop Performance

Cable resistance and sensing error are the main factors influencing the voltage regulation and load sharing in droop control. The impact from each of them is quantitatively analyzed in this section.

A. Cable Resistance

Cable resistance is inevitable in distributed systems. Considering the scale of dc systems, from telecommunication to dc microgrids, the cable can span from several meters to tens of meters. Common cable gauges in residential applications and their corresponding voltage drops have been listed in [14]. The data indicates a cable voltage drop of 2.5 % to 5 % for a dc grid spanning 50 meters, given cables are selected based on their current ratings. This cable voltage drop is comparable to the droop voltage range, i.e., 5 % of the nominal bus voltage.

Fig. 1 shows the measurement result of a 5-meter power loop using an AWG 18 cable for a 10 A current capacity. The total cable resistance is 0.2 Ω. A dc output power converter is connected to a load through this cable. The power converter follows a linear droop characteristic and outputs 380 V under no load. The droop resistance is 1 Ω so the droop voltage range is 10 V with a 10 A maximum current. The voltages are measured at both the source and load terminals. The reference curve is the designed droop characteristic; the voltage drops from 380 V to 370V when the current increases from 0 to 10 A. The measured curve at the source terminal matches the designed curve. However, due to cable resistance, the voltage at the load terminal deviates from the reference. The higher the output current is, the larger that difference will be.

Fig. 2(a) shows a two-source one-load dc system with cable resistances R_{line1} and R_{line2}. Both the load sharing and voltage distribution will be different from the case without cable resistances. If the designed droop resistances are R_{d1} and

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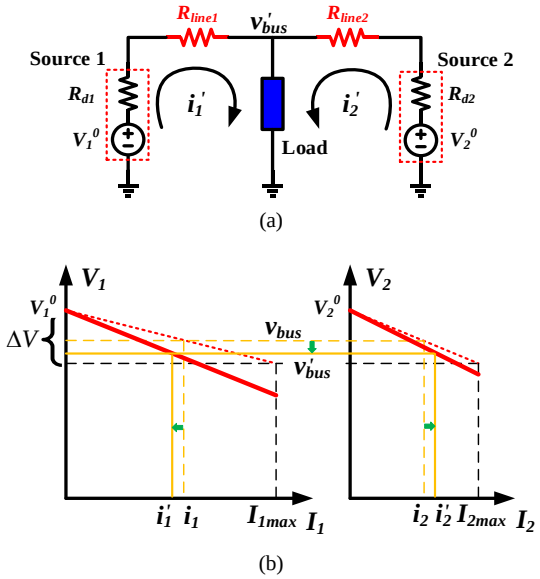

Fig. 2. Two sources droop with cable resistances. (a) Circuit schematic. (b) Operating points before and after including cable resistances.

R_{d2} for Sources 1 and Source 2 respectively, the total resistances from the two sources to the load are

$$R'_{d1} = R_{d1} + R_{line1} \tag{1}$$

$$R'_{d2} = R_{d2} + R_{line2} \tag{2}$$

For load current i_{load}, the operating point with cable resistances can be solved by

$$\begin{cases} v'_{bus} = V_1^0 - i'_1 R'_{d1} = V_2^0 - i'_2 R'_{d2} \\ i_{load} = i'_1 + i'_2 \end{cases} \tag{3}$$

where V_1^0 and V_2^0 are the voltage set points for the two sources under no-load conditions. v'_{bus}, i'_1 and i'_2 are the bus voltage and source currents with the consideration of line resistances.

If $V_1^0 = V_2^0$, the load sharing is

$$\frac{i'_1}{i'_2} = \frac{R'_{d2}}{R'_{d1}} = \frac{R_{d2} + R_{line2}}{R_{d1} + R_{line1}} \tag{4}$$

which deviates from the designed value R_{d2} / R_{d1}. Generally speaking, a larger line resistance difference leads to a bigger load sharing deviation when the droop resistance is fixed.

In Fig. 2(b), the dashed lines represent the steady-state operating point without cable resistances. The solid lines show the operating point with cable resistances. In the latter case, the bus voltage drops from v_{bus} to v_{bus}' and source currents shift from i_1 and i_2 to i_1' and i_2'.

Fig. 3 shows a numeric result with different droop resistances for the system in Fig. 2. In the plot, Source 1 and Source 2 are assumed identical and should share the load evenly. $V_1^0 = V_2^0 = 1$ pu. The maximum source current $I_{1max} = I_{2max} = 1$ pu, and the maximum system load current is 2 pu. The line resistance R_{line1} is 0.01 pu, and R_{line2} is 0. Fig. 3 shows the load sharing comparison between $R_{d1} = R_{d2} = R_d = 0.01$ pu and 0.04 pu, i.e., R_d is equal to, or four times the cable resistance. Clearly, a larger droop resistance improves load sharing, but

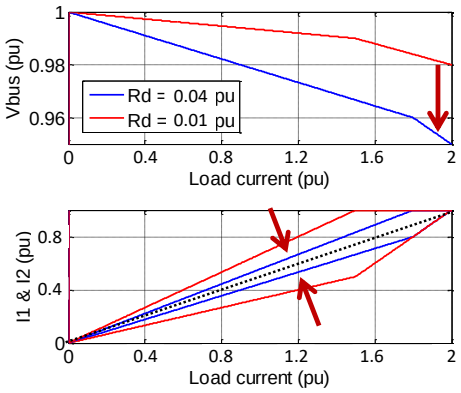

Fig. 3. Load sharing and voltage regulation with different droop resistances.

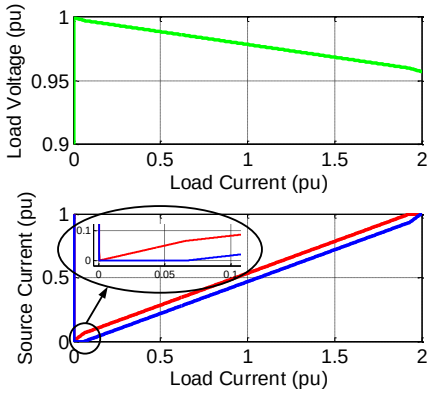

Fig. 4. Impact of voltage sensing error on load sharing without cable resistance.

leads to a larger voltage drop. Under a heavy load, this voltage deviation can be unacceptable.

B. Sensing Error

Another factor influencing the load sharing is the output voltage regulation error caused by measurement. Even if the final products are calibrated carefully to make the measurement error small, sensors drift when temperature changes. In the authors' experiments, a 1 V voltage drift is commonly observed for 380 V dc systems. Based on the datasheet, the adopted Hall effect voltage sensors, LV 25-P, have a static accuracy of around 1 % [23]. More errors are expected from the sensing resistors, signal conditioning circuits, and analog-to-digital converters. These errors always exist and cannot be eliminated.

Considering the system in Fig. 2 without cable resistance, when $V_1^0 = V_2^0$, $i_1 = \frac{R_{d2}}{R_{d1}} i_2$. If $V_1^0 \neq V_2^0$ due to the voltage measurement error, it can be derived that

$$i_1 = \frac{R_{d2}}{R_{d1}} i_2 + \frac{V_1^0 - V_2^0}{R_{d1}} \tag{5}$$

The second term is the load sharing error due to voltage sensing. Unlike the error from cable resistance, this error stays constant when the load current changes; it is only related to the sensor offset and droop resistance.

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In Fig. 4, when the load current increases from zero, the source with a higher output voltage will provide power first (red line). The other source (blue line) begins to output power after the bus voltage drops to a certain value that cancels out the sensing difference. Then, the two sources increase their output currents with the same slope.

In practical, the load sharing error is the result of both line resistances and measurement errors. The error from line resistances increases when the load increases; the error from measurement stays constant regardless of the load.

III. The Nonlinear Droop Control

A. The Benefits of Nonlinear Droop Control

From the above discussion, we know that a larger droop resistance has the advantage of better load sharing but sacrifices the voltage regulation. A smaller droop resistance requires a smaller droop voltage range but is more sensitive to the impact from cables and sensors. In the traditional droop design using a fixed droop resistance, trade-offs have to be made between voltage regulation and sharing accuracy.

If we consider the process of the traditional droop design for a power converter, it follows these steps:

1) Choose the droop curve start point as the no-load voltage set point.

2) Choose the droop curve end point based on the maximum source current and the lower limit of the dc bus voltage.

3) The straight line connecting the start and the end points will be the designed output droop curve.

In practice, the source rating and dc bus voltage range are predetermined by the system specifications. In other words, the start point and end point of the droop curve are predefined. The only degree of freedom that can be used for improvement is the trajectory that connects these two points.

In Fig. 5, the red line is the trajectory of linear droop, the orange line is a piecewise linear droop consisting of two linear segments with different slopes, and the blue line is a nonlinear droop curve. By examining the droop resistance, which is the slope of the tangent along the curves, the piecewise linear and nonlinear droop methods have the following features:

1) They have larger droop resistance R_{d_H} under heavy load, enabling better load sharing.

2) They have smaller droop resistance R_{d_L} under light load, enabling tighter voltage regulation.

3) Their droop curves are always above the linear droop, implying smaller voltage deviation from the voltage set point under all load conditions.

These features are the characteristics that designers are seeking in droop control. Under heavy loads, uneven load sharing leads to source saturation, uneven thermal stress, accelerated component aging, and increased bus voltage drop; therefore accurate load sharing is important. In contrast, accurate load sharing is less crucial under light loads; as long as the sources are working well within their limits, some sharing error is totally acceptable. In some cases, tighter voltage

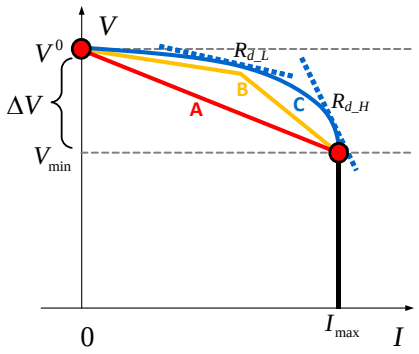

Fig. 5. Trajectories of (A) linear, (B) piecewise linear, and (C) nonlinear droop control.

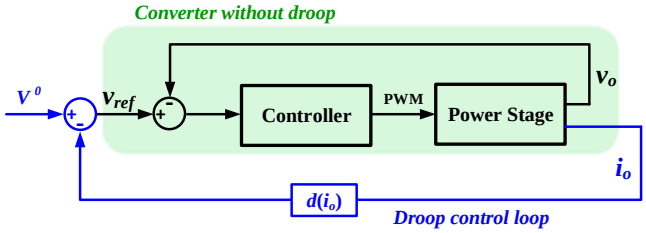

Fig. 6. General control structure to realize virtual droop resistance.

regulation with smaller droop resistance is beneficial because a higher bus voltage leads to smaller current and reduces the cable conduction loss [24].

To avoid loss on physical resistors, the droop characteristic is usually implemented by control loops in high power applications. In Fig. 6, the green shaded parts constitute a converter without droop. The output voltage v_o is sensed and compared with the reference v_{ref} to form a voltage feedback loop and regulate the output voltage. The blue parts form a droop loop where $d(i_o)$ is the droop function. V^0 is the no-load voltage set point. The output current i_o is sensed and fed back to adjust the voltage reference v_{ref} such that $v_{ref} = V^0 - d(i_o)$. In linear droop, $d(i_o)$ is a constant R_d and $v_{ref} = V^0 - i_o R_d$. In the piecewise and nonlinear droop, $d(i_o)$ is a function of i_o.

Since the nonlinear droop functions used in this paper are mainly multiplication and square root, they can be easily implemented in a digital processor with minimal extra calculation time. Taking Texas Instruments C2000 series DSP with a floating-point unit as an example, both addition and multiplication take just two clock cycles; the square root calculation takes 22 cycles [25]. These are very small amounts of time, considering the state-of-art processors usually have tens or hundreds of MHz clock frequency. Analog control is not as flexible as the digital, but the multiplication and square root can still be implemented with analog multipliers, operational amplifiers, or dedicated ICs, with some added cost.

B. Piecewise Linear Droop

As a bridge between linear and nonlinear droop, piecewise linear droop is analyzed. In the piecewise linear droop, the total droop voltage range is split into multiple segments. The droop resistance is different in each segment. As previously discussed, it is preferable to increase the droop resistance when the output current increases. As an example, a three-segment piecewise linear droop is shown in Fig. 7. The output droop resistance

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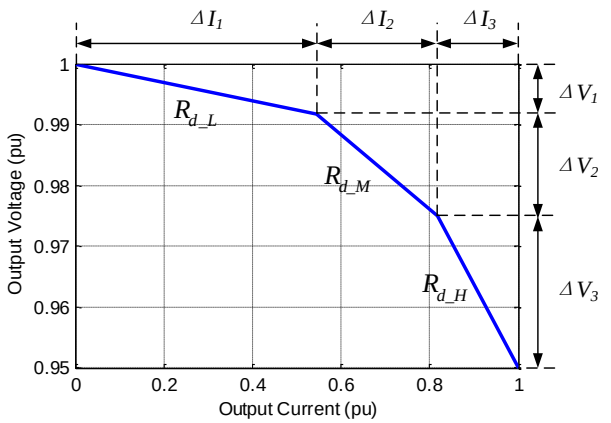

Fig. 7. Three-segment piecewise linear droop.

gradually increases from R_{d_L} (R_d under light load), to R_{d_M} (R_d under medium load), and to R_{d_H} (R_d under heavy load). Therefore, the load sharing improves when the output current increases. Clearly, there is certain freedom to choose the values of the piecewise droop resistances and their applicable voltage and current ranges. Two examples are given below to facilitate a fast design and other ways to customize the piecewise function can be further explored.

In the first design example, the desired values of R_{d_L}, R_{d_M} and R_{d_H} are already known. Based on the voltage and current relationship in Fig. 7, we have the following two equations:

$$\Delta I_1 + \Delta I_2 + \Delta I_3 = I_{\max} = 1\ pu \tag{6}$$

$$\Delta V_1 + \Delta V_2 + \Delta V_3 = \Delta I_1 R_{d\_L} + \Delta I_2 R_{d\_M} + \Delta I_3 R_{d\_H} = 0.05\ pu \tag{7}$$

Since there are two equations but three unknowns, one extra constraint can be added. For example, one can use $\Delta I_2 = 0.3 I_{\max}$ as the third equation to guarantee R_{d_M} applies to 30 % of the load range. Then the values of current and voltage segments can be solved sequentially.

In the second design example, the values of droop resistances are unknown, but there exists a desired ratio between the droop resistances in different segments, e.g., $R_{d\_L} : R_{d\_M} : R_{d\_H} = 1 : k_1 : k_2$, assuming

$$\Delta V_2 = \alpha_1 \Delta V_1, \Delta V_3 = \alpha_2 \Delta V_1 \tag{8}$$

$$\Delta I_2 = \beta_1 \Delta I_1, \Delta I_3 = \beta_2 \Delta I_1 \tag{9}$$

Then the droop resistance ratio satisfies

$$R_{d\_L} : R_{d\_M} : R_{d\_H} = 1 : \frac{\alpha_1}{\beta_1} : \frac{\alpha_2}{\beta_2} \tag{10}$$

To meet the required droop resistance ratio, there are two simple ways to choose the values of α and β. In the first method, we choose $\beta_1 = \beta_2 = 1$, then $\alpha_1 = k_1$, $\alpha_2 = k_2$. In other words, the total load range is evenly separated into three segments; the voltage range is unevenly distributed to achieve the desired droop resistances. The second way is choosing $\alpha_1 = \sqrt{k_1}$, $\alpha_2 = \sqrt{k_2}$, $\beta_1 = 1/\sqrt{k_1}$, $\beta_2 = 1/\sqrt{k_2}$, so both voltage range and current range are proportionally split to generate the desired droop resistances. In Fig. 7, the droop curve for k_1=4 and k_2= 9 is drawn. The resultant R_{d_L}, R_{d_M} and R_{d_H} are 0.0153 pu, 0.0611 pu, and 0.1375 pu, respectively. Compared with the 0.05 pu droop resistance in linear droop, the light-load droop resistance is reduced to 1/3 and the heavy-load value is increased by 2.75 times.

In summary, piecewise linear droop achieves the goal of changing the output impedance based on load current. However, it requires the selection of slopes and turning points for the piecewise segments. The sudden slope change between different segments might be an issue when the load switches between adjacent segments. Though this issue can be alleviated by using hysteresis at the segment transitions, a smooth droop curve is preferable. If we increase the number of segments to infinite, then the piecewise linear droop curve approaches a nonlinear droop curve.

C. A General Nonlinear Droop Polynomial Expression

Without loss of generality, the droop characteristics can be expressed in a the form shown in (11), where v and i are the output voltage and current, V^0 is the no-load voltage set point, and $d(i)$ is the droop function. When $i>0$, $d(i)>0$. The droop function in (11) needs to satisfy requirements from (12) to (15). Equations (12) and (13) ensure the no-load and full-load voltages are at the desired set points when the output current is zero and maximum. Equation (14) represents the droop resistance $R_d(i)$ as the derivative of the droop function $d(i)$. The droop resistance needs to be positive to guarantee the load sharing. Equation (15) is a new desired feature for the nonlinear droop. As discussed, it is preferable to have a larger droop resistance under heavier load conditions, so the derivative of $R_d(i)$ is also positive.

$$v = f(i) = V^0 - d(i) \tag{11}$$

subject to

$$d(0) = 0 \tag{12}$$

$$d(I_{\max}) = \Delta V \tag{13}$$

$$R_d(i) = d'(i) > 0 \tag{14}$$

$$R_d'(i) = d''(i) > 0 \tag{15}$$

For a current bidirectional converter, it is natural to extend the droop characteristic into the second quadrant in the V-I plane by using (16). When the current goes negative, the output voltage is above the no-load voltage V^0. To have a symmetric converter output characteristic around the no-load operating point at (0, V^0), the droop function $d(i)$ needs to be an odd function.

$$d(i) = -d(-i)\ when\ i < 0 \tag{16}$$

As there are infinite ways to draw curves between the droop start and end points, there are different ways to construct the droop function. One simple way is to use a polynomial equation as (17) where $d(i)$ is the sum of N power functions of current i.

$$v = V^0 - \sum_{n=1}^{N} K_n \cdot i^n \tag{17}$$

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If we normalize output voltage v and current i using the system nominal bus voltage V^0 and the source maximum current I_{max} as the base values in (18), the output voltage and current in per unit can be defined in (19).

$$V_{base} = V^0,\ I_{base} = I_{\max},\ R_{base} = V_{base} / I_{base} \tag{18}$$

$$v_{pu} = \frac{v}{V^0},\ \Delta V_{pu} = \frac{\Delta V}{V^0},\ i_{pu} = \frac{i}{I_{\max}} \tag{19}$$

Then (17) can expressed in the form of (20) using per unit variables.

$$v_{pu} = 1 - \Delta V_{pu} \sum_{n=1}^{N} K_n \left(i_{pu}\right)^n \ where \sum_{n=1}^{N} K_n = 1 \tag{20}$$

Clearly, (20) considers the power function of current i but does not include the power function of voltage v. Thus, an enhanced form is expressed in (21) which considers the power functions of both v and i. However, it consists of M terms of v and N terms of i expressions, making the selection of coefficients P_m and Q_n complicate.

$$\sum_{m=1}^{M} P_m \left(\frac{1 - v_{pu}}{\Delta V_{pu}}\right)^m = \sum_{n=1}^{N} Q_n \cdot \left(i_{pu}\right)^n \ where \sum_{m=1}^{M} P_m = \sum_{n=1}^{N} Q_n \tag{21}$$

To avoid the selection of coefficients in (21), another general droop expression in (22) is used. It is conceived based on the observation that when the current i_{pu} increases from 0 to 1 pu, the voltage v_{pu} drops from 1 pu to $1-\Delta V_{pu}$ pu. Though this expression includes only one power term of v_{pu} and one term of i_{pu}, it is capable of generating a cluster of curves with different slopes by tuning the parameters m and n; thus, the task to select parameters in (21) is greatly simplified. Another benefit of using this expression is its capability to cover the well-known second order functions like parabola and ellipse.

$$\left(\frac{v_{pu} - \left(1 - \Delta V_{pu}\right)}{\Delta V_{pu}}\right)^m + \left(i_{pu}\right)^n = 1 \tag{22}$$

By solving (22), v_{pu} can be derived as a function of i_{pu} as

$$v_{pu} = 1 - \Delta V_{pu} \left(1 - \sqrt[m]{1 - \left(i_{pu}\right)^n}\right) \tag{23}$$

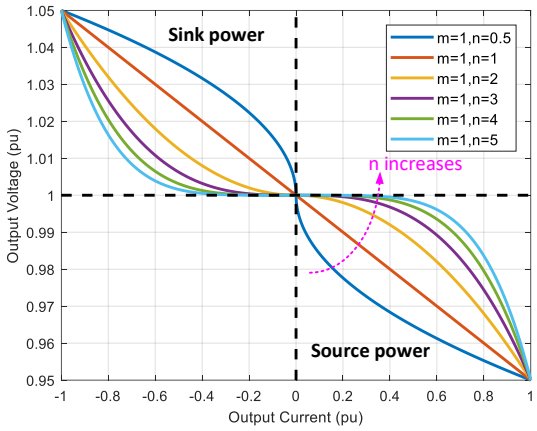
Specifically, when m=1, (23) becomes (24), which is a single term case of (20). If m=1 and n=1, it goes back to the traditional linear droop.

$$v_{pu} = 1 - \Delta V_{pu} \cdot \left(i_{pu}\right)^n \tag{24}$$

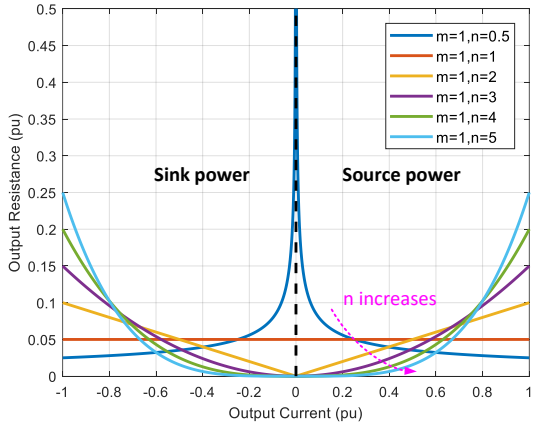
By calculating the derivative of (23), the droop resistance as a function of output current i_{pu} can be expressed as:

$$R_{d\_pu} = \left|\frac{dv_{pu}}{di_{pu}}\right| = \Delta V_{pu} \frac{n}{m} \left(1 - \left(i_{pu}\right)^n\right)^{\frac{1}{m}-1} \left(i_{pu}\right)^{n-1} \tag{25}$$

Specifically, when m = 1, the droop resistance expression simplifies into (26). The full-load droop resistance is $n \cdot \Delta V_{pu}$, which is n times higher compared to the linear droop.



(a)



(b)

Fig. 8. (a) Different droop curves and (b) Corresponding droop resistances (m =1, n is from 0.5 to 5).

$$R_{d\_pu} = n \cdot \Delta V_{pu} \cdot \left(i_{pu}\right)^{n-1} \tag{26}$$

D. Selection of Nonlinear Droop Parameters

In practice, lower-order systems are easier to implement. Fig. 8 shows the droop trajectories and resistances for a current bidirectional power converter as a function of n when m = 1. When i>0, the converter is outputting power; when i<0, the converter is sinking power. When $i = I_{\max}$, the source reaches its maximum current and switches to current-limiting mode, as drawn in Fig. 5.

When n increases from 0.5 to 5, the droop curves approach the x-axis under light-load conditions. When n>1, droop resistance increases when the output current increases; when n<1, droop resistance decreases when the output current increases; if n=1, the droop is the linear droop and the droop resistance is a constant regardless of the output current.

In Fig. 9, the second-order nonlinear droop trajectories and their droop resistances are plotted against linear droop. When n increases, the droop curve approaches the x axis when output power is small. When n = 2, the slope, i.e., the droop resistance, is zero under no load. Similarly, when m increases, the droop curve approaches vertical direction when the converter outputs full power. When m = 2, the droop resistance under full load is

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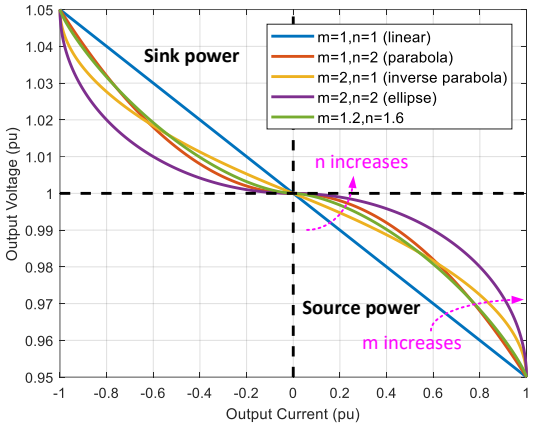
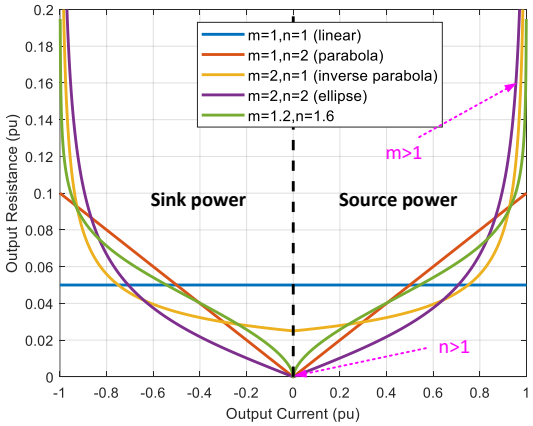


(a)



(b)

Fig. 9. (a) Linear and 2nd-order droop curves and (b) Corresponding droop resistances.

infinite. It should be noted that m and n do not have to be integers. The curve with m = 1.2 and n = 1.6 is drawn in the same figure as an example. As expected, its characteristic is between the adjacent m and n integers, so the droop curves are continuously adjustable by tuning the parameters m and n.

In summary, in order to achieve a large droop resistance under heavy load, the piecewise linear droop and nonlinear droop are preferred. Among different nonlinear droop equations, high-order polynomial (m = 1, large n), inverse parabola (m = 2, n = 1) and ellipse (m = 2, n = 2) are desired.

IV. Steady-State Performance Improvement

A. Load Sharing and Voltage Regulation

The two-source system in Fig. 10 is analyzed to compare the performance of linear and nonlinear droop methods. The two sources are assumed identical so they should share the load evenly, i.e., i_1=i_2. The no-load voltage set point is 400 V. The droop voltage range is 20 V. The maximum source current is 25 A and the corresponding cable gauge is AWG12 with 5.2 mΩ resistance per meter. The distance from Source 1 to the load is 20 meters, while Source 2 is next to the load. Droop resistance R_d is 0.8 Ω for linear droop and R_{line} is 0.2 Ω. The sensors are calibrated and do not impact the load sharing.

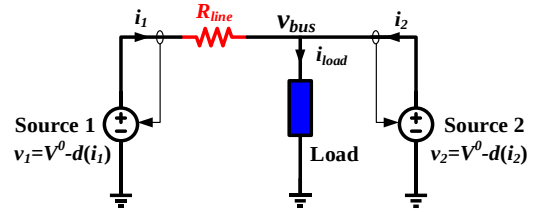


Fig. 10. Two sources droop with cable resistances.

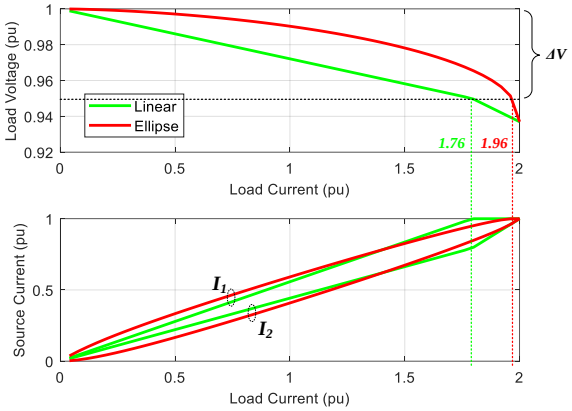


Fig. 11. Comparison of voltage regulation and load sharing for linear and nonlinear droop.

To make the discussion general, the no-load bus voltage is defines as 1 pu and the maximum current of each source is 1 pu. The maximum system load is 2 pu. The droop voltage range is 5 % of the bus voltage. Since the second quadrant operation is symmetric to the first quadrant, only positive source current is discussed.

When the load current is i_{load}, the bus voltage v_{bus} and source currents i_1 and i_2 can be calculated using (27), by substituting different linear and nonlinear droop equations. Solving the equation system with a ramping load current from 0 to 2 pu gives the bus voltage and source currents for all load conditions.

$$\begin{cases} v_{bus} = V^0 - d(i_1) - i_1 R_{line} = V^0 - d(i_2) \\ i_{load} = i_1 + i_2 \end{cases} \tag{27}$$

Using linear and elliptic droop, Fig. 11 shows the bus voltage at the load terminal and the source current. When the load current ramps up, the bus voltage drops, and the source current increases until it reaches the 1 pu limit. Compared to the linear droop, the elliptic droop has smaller voltage deviation from the voltage set point. It also has better load sharing under heavy load. More importantly, the elliptic droop is able to utilize 98 % (1.96 pu) of the system power rating while the linear droop can only use 88 % (1.76 pu) before the load node voltage drops below the designed droop voltage range due to cable voltage drop.

Fig. 12 compares the load sharing and bus voltage regulation performance of linear and different 2nd-order nonlinear droop profiles from light-load to full-load. Relating it with Fig. 9, we can draw the following conclusions: The linear droop has a fixed droop resistance under the entire load range. The parabola and ellipse have zero slope under no-load condition; thus, under very light load conditions, the line

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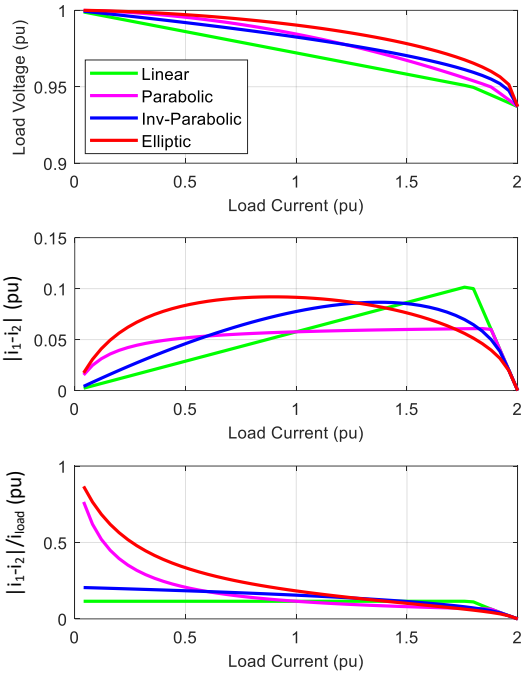

Fig. 12. Comparison of linear and different 2nd-order nonlinear droop.

resistance determines how the load is shared among sources. Under full-load conditions, the droop resistance of the parabola is a finite number, though the value is bigger than the linear droop. The inverse parabola and ellipse both have infinite droop resistance under full load, theoretically eliminating the impact from cables and sensing errors. The transition between voltage regulation mode and current-limiting mode is also smooth in these two methods because there is no abrupt slope change. The difference between the two methods is that the ellipse has zero resistance under no load while the inverse parabola has some limited value.

B. System Efficiency

For a dc power distribution system, the system loss consists of power conversion loss and transmission loss. The power conversion loss is the energy lost in power converters when transforming the electricity from ac to dc, or from one voltage to another. The transmission loss is the energy lost in cables when the electricity is delivered from one location to another. Since different droop control methods have different load sharing performance, their system-level efficiencies are also different.

Taking the two-source power system in Fig. 10 as an example, the power transmission loss, i.e., the line resistive loss, can be calculated as (28). The power conversion loss can be calculated using (29), where P_{in1}, P_{in2}, P_{o1}, and P_{o2} are the input and output power of Source 1 and Source 2, respectively; η is the converter efficiency, which is a function of the converter's output current. The power converters for Source 1 and Sources 2 are assumed identical and have the same efficiency characteristic.

$$P_{line} = i_1^2 R_{line} \tag{28}$$

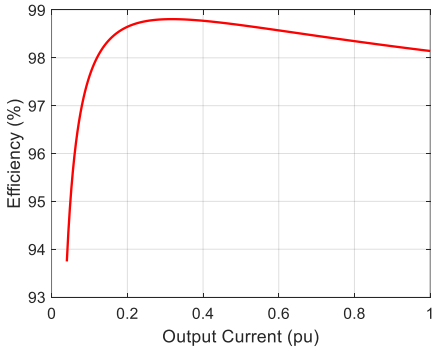

Fig. 13. Typical power converter efficiency curve. [26]

$$\begin{aligned} P_{conv} &= P_{in1} + P_{in2} - P_{o1} - P_{o2} \\ &= P_{o1}/\eta_1 + P_{o2}/\eta_2 - P_{o1} - P_{o2} \\ &\approx v_{bus}\left(i_1/\eta(i_1) + i_2/\eta(i_2) - i_1 - i_2\right) \end{aligned} \tag{29}$$

The system loss can be evaluated by combining the power transmission loss P_{line} and power conversion loss P_{conv}, so the total system loss P_{total} is

$$P_{total} = P_{line} + P_{conv} \tag{30}$$

In practice, the power conversion efficiency depends on the power converter design and optimization. It usually follows a shape like the curve shown in Fig. 13 that has a peak under medium to heavy load. The efficiency under light load is usually low. This can be improved by shutting down some sources under light loads, e.g., the phase shedding strategy broadly adopted in multi-phase buck converters. The ratio between cable and conversion losses also varies with system power and current ratings. Generally, the higher the current, the higher the transmission loss consumed on cables.

For certain load current i_{load}, infinite combinations of i_1 and i_2 satisfying $i_1 + i_2 = i_{load}$ exist. Each i_1 and i_2 combination leads to a corresponding system efficiency that can be calculated using (28)-(30). By sweeping all the combinations, the theoretical maximum and minimum system efficiency and corresponding source current can be obtained. Similarly, the efficiencies for different droop methods can be calculated after solving their source currents i_1 and i_2 using (27).

To get numerical results, the measured power converter efficiency shown in Fig. 13 is used as the efficiency curve for Source 1 and Source 2. The system efficiencies and corresponding source current i_1 and i_2 are drawn in Fig. 14. In addition to the theoretical maximum and minimum system efficiency from the sweep, linear droop (*L*) and inverse parabolic droop (*IP*) are included. Another benchmark curve is using stiff voltage regulation without droop control. In that case, Source 2 provides all the load current until it reaches saturation; then Source 1 starts providing current.

Examining the efficiency and load sharing curves, though the nonlinear droop provides better load sharing under heavier load, the efficiencies of linear and nonlinear droop control do not have substantial difference. Both of them approach the theoretical maximum efficiency. However, for the case without using any droop, the light to medium load efficiency suffers. This can be explained by the loss breakdown of P_{line} and P_{conv} in

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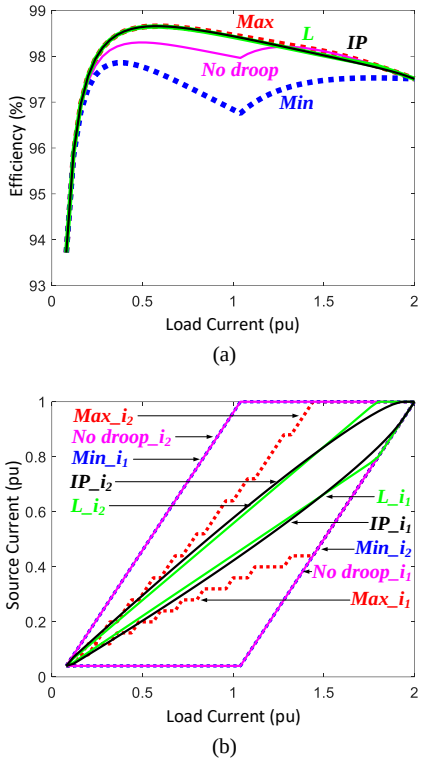

Fig. 14. (a) DC system efficiency and (b) Corresponding source current.

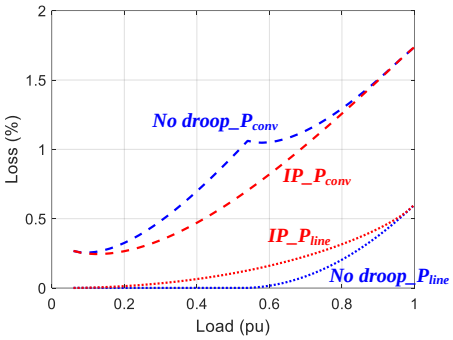

Fig. 15. Comparison of cable and power conversion losses.

Fig. 15. Without using droop, the cable decides how the load is shared between the sources. The closer source takes all the load current while the farther source takes none. With such load sharing, although the line resistance loss is naturally minimized, the power conversion loss is increased. In the analyzed case, the power conversion loss is much higher than the cable loss, so the overall loss is dominated by the power conversion loss. In high current applications, the cable loss could take a great portion; the trend of total loss might change and needs reevaluation.

In summary, droop control impacts the system efficiency by altering the source current allocation. In order to obtain quantitative results, case-by-case calculations are necessary by combining cable loss and power conversion loss.

V. Converter Output Impedance and DC System Stability

Droop control adds an extra control loop to the converter control system and changes the converter's dynamic performance. In addition to the steady-state analysis, dynamic analysis is necessary to ensure the system stability. Though the stability of dc and ac converter systems has been broadly studied, further work is needed for droop-controlled power converters.

State-space analysis and impedance-based analysis are two widely-used methods for stability analysis [27]. State-space analysis is broadly used in control system stability analysis by plotting the eigenvalues of system state-space equations. If all the poles are located in the left-half plane, the system is stable. However, this method requires the knowledge of all the power converter parameters, which is not always available for the system engineer.

The second method to analyze the dc system stability is the impedance-based criteria, e.g., the Middlebrook criterion [28]. To guarantee the stability for a cascaded power converter system, the magnitude of the source converter's output impedance Z_o must be much smaller than the magnitude of the load's input impedance Z_i, i.e.,

$$|Z_o| << |Z_i| \tag{31}$$

It should be noted that the Middlebrook criterion is a conservative condition that not only guarantees the system stability but also ensures the system dynamic performance is not changed. The system can still be stable even if this criterion is violated.

To get a more accurate stability judgment, some relaxed criteria have been proposed by considering both the magnitude and phase of the input and output impedances. One example is the gain margin phase margin (GMPM) criterion [29]. In this criterion, if the magnitude of the load input impedance is at least 6 dB higher than the source output impedance, then a 6 dB gain margin is guaranteed. Otherwise, the phase of the load system's input impedance has to stay within a 120° band around the phase plot of the source system's output impedance, to guarantee a 60° phase margin. The GMPM criterion can be also explained in the Nyquist plot where the contour of Z_o/Z_i should stay away from a forbidden area around point (-1, 0).

The impedance-based methods do not need all of the converter parameters since the converter's input and output impedances can be measured using a network analyzer. To use impedance-based criteria, the modeling and measurement of the output impedance of droop-controlled converters is critical.

A. Modeling the Output Impedance of Droop-Controlled Power Converters

Using a digital controlled buck converter as an example, the circuit and control diagram is drawn in Fig. 16. The controller includes an inner current loop, an outer voltage loop, and a droop loop. H_v and H_i are the voltage and current loop compensators. H_{filter} is the optional low-pass filter (LPF) in the voltage sensing circuit. H_{delay} represents the controller computation delay and modulator delay. F_m is the gain of the modulator. For a buck converter, the load current and inductor current have the same average value, thus the average inductor current obtained by synchronous sampling is used for droop to save the output current sensing circuit [30]. $d(i)$ is the droop function as introduced in (11).

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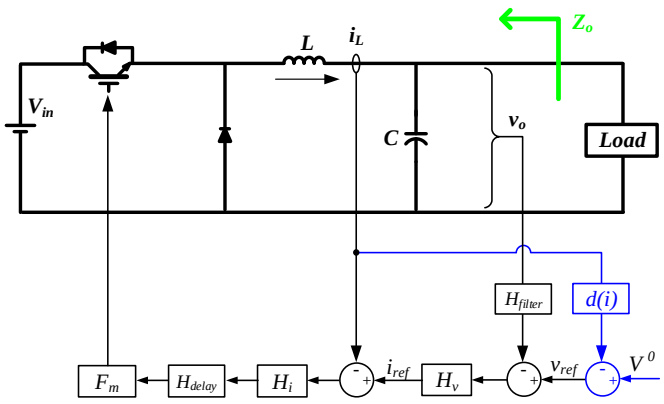

Fig. 16. Buck converter with droop control loop.

Using switching cycle average and replacing the circuit with transfer functions, Fig. 17 can be obtained for small-signal analysis. In the power stage part, G_{vd} and G_{id} are the transfer functions from the duty cycle to the output voltage and inductor current. Z_{o_OL} is the open-loop output impedance of the converter, and G_{iio} is the transfer function from the load current to the inductor current. These are all known transfer functions for basic converter topologies and can be found in textbooks. For the droop loop, the large signal droop function *d(i)* needs to be replaced with its derivative, which is the droop resistance R_d. R_d is a constant value for linear droop, but a function of current for the nonlinear droop.

The closed-loop output impedance of the droop-controlled converter can be derived by solving the control diagram using (32).

$$\begin{cases} \hat{i}_L = G_{id}\hat{d} + G_{iio}\hat{i}_o \\ \hat{v}_o = -Z_{o\_OL}\hat{i}_o + G_{vd}\hat{d} \\ \hat{v}_{ref} = -R_d\hat{i}_L \\ \hat{i}_{ref} = \left(\hat{v}_{ref} - H_{filter}\hat{v}_o\right)H_v \\ \hat{d} = \left(\hat{i}_{ref} - \hat{i}_L\right)H_iH_{delay}F_m \end{cases} \tag{32}$$

The closed-loop output impedance Z_o with droop control is as follows:

$$Z_o = -\frac{\hat{v}_o}{\hat{i}_o} = \frac{Z_{o\_OL} + \dfrac{F_mH_{delay}H_i\left(R_dH_v+1\right)G_{vd}G_{iio}}{1+F_mH_{delay}H_i\left(R_dH_v+1\right)G_{id}}}{1+\dfrac{F_mH_{delay}H_iG_{vd}H_vH_{filter}}{1+F_mH_{delay}H_i\left(R_dH_v+1\right)G_{id}}} \approx \frac{Z_{o\_OL}+\dfrac{G_{vd}G_{iio}}{G_{id}}}{1+\dfrac{G_{vd}H_vH_{filter}}{\left(R_dH_v+1\right)G_{id}}} \tag{33}$$

The assumption for the approximation in (33) is $F_mH_{delay}H_i\left(R_dH_v+1\right)G_{id} >> 1$. It means that the total loop gain of the current loop and droop loop is greater than 1, which is true within the control bandwidth of the current loop.

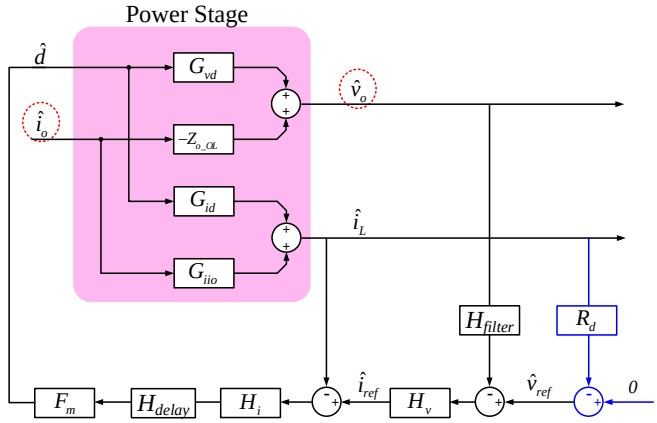

Fig. 17. Small-signal model of a droop-controlled voltage source converter.

For the nonlinear droop, R_d and Z_o vary depending on the output current. In order to solve Z_o under different load conditions, the value of R_d at each operating point needs to be solved and substituted into (33). R_d can be solved by combining the source output and load input equations. Taking the elliptic droop as an example, when the load is a resistor R_{load}, the converter output voltage and current satisfy (34) and (35). Then the output resistance as a function of output current can be solved in (36). The output resistances for linear and other nonlinear droop functions in pu are summarized in Table I.

$$v = V^0 - \Delta V + \Delta V\cdot\sqrt{1-\left(i/I_{\max}\right)^2} \tag{34}$$

$$v = i\cdot R_{load} \tag{35}$$

$$R_d(i) = -\frac{dv}{di} = \Delta V\cdot\frac{i}{I_{\max}^2\sqrt{1-\left(i/I_{\max}\right)^2}} \tag{36}$$

One important feature of (33) is that Z_o at a particular operating point, is only related to the small-signal droop resistance at this point regardless of the shape of the droop curve around it. Therefore, the stability with different droop resistance can be analyzed without worrying which nonlinear droop is used. In other words, the following discussion can be applied to either liner or different nonlinear droop methods, as long as the correct R_d value is substituted into (33). This is proved in Fig. 18 where the output impedances of elliptic droop and linear droop overlap when their droop resistances have the same value.

Though a buck converter is used as an example, this analysis can easily be applied to other topologies by adapting the system block diagram in Fig. 17 and using the corresponding transfer functions for the power stage.

B. The Impact of Droop Control on Output Impedance

As a benchmark, the output impedance without droop control is analyzed first. The current loop gain T_i, voltage loop gain T_v, input impedance Z_{in}, and output impedance Z_o are shown in Fig. 19, from 1 Hz (basically the dc value) to 10 kHz (half of switching frequency). The derivation of the input impedance for common converters can be found in [31], [32].

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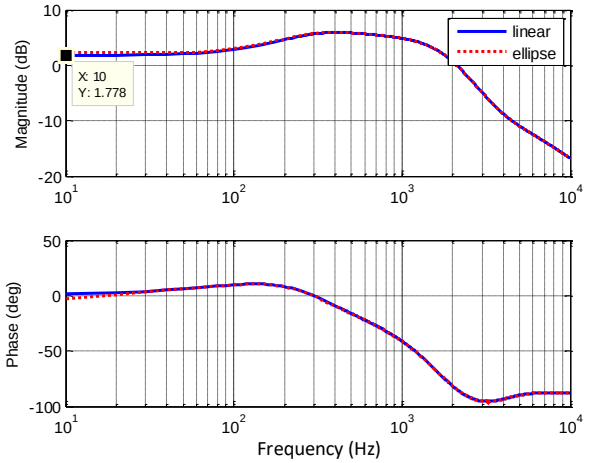

Fig. 18. Output impedance comparison between different droop trajectories when they have the same R_d value.

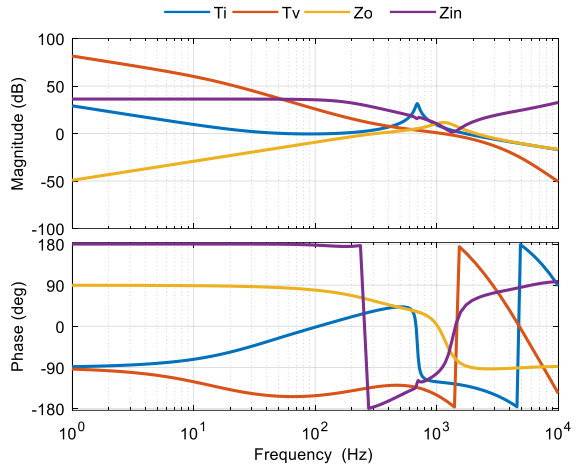

Fig. 19. Current, voltage loop gains and input, output impedances without droop control.

Both current and voltage loops have wide bandwidth at 1.7 kHz and 650 Hz, and Z_o is very small within the control bandwidth. As the converter tightly regulates its output voltage, its small-signal input impedance Z_{in} behaves as a negative resistance within the control bandwidth. Its dc magnitude equals to its load resistance R_{load} reflected to the input, i.e., R_{load}/D^2, where D is the duty cycle for the buck converter, but its phase angle is –180°.

After adding the droop control loop, the output impedance is changed. Two factors are considered. One is the impact of adding a LPF in the droop loop; the other is the value of the droop resistance. Looking at Fig. 20, the dc and low frequency output impedance is now behaving as a resistance; the phase angle is 0° and the magnitude is equal to the droop resistance. Comparing the output impedances with and without a 2nd-order LPF at 60 Hz, the implementation without LPF maintains a flat output resistance up to 400 Hz, while the one with LPF starts to deviate at the LPF crossover frequency. From the perspective of maintaining a wide droop characteristic, the implementation without LPF is preferred.

Fig. 21 compares the output impedances when R_d adopts difference values. When the converter operates without droop

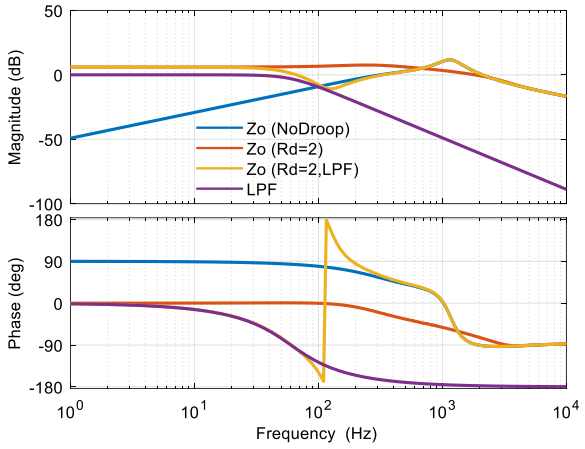

Fig. 20. Output impedances with and without LPF in the droop control loop.

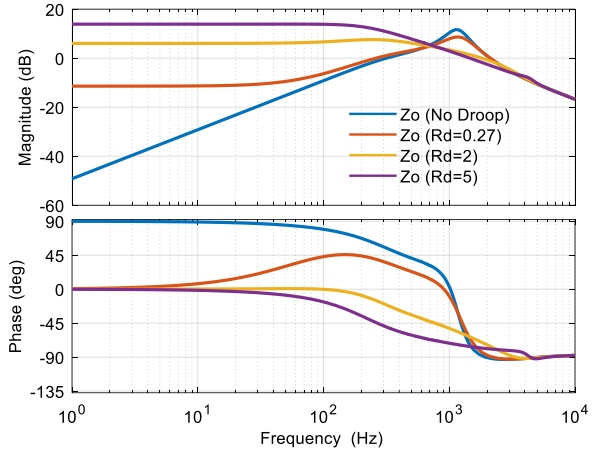

Fig. 21. Output impedance with different droop resistance R_d.

control, the output impedance is well below 0 dB within the control bandwidth. Thus, the converter has very good voltage regulation. When linear droop control is applied, the droop resistance is 20 V/10 A = 2 Ω, so its output resistance is 20 × log(2) = 6 dB. The output impedance is flat within the control bandwidth.

With nonlinear droop, when the load is light, the output impedance is well below 0 dB at –11 dB, indicating small output voltage deviation and strong voltage regulation. When the load increases, the magnitude of the output impedance also increases. Under heavy loads, the magnitude of the output impedance reaches 14 dB, and is much larger than the linear droop.

When R_d increases, the dc and low frequency output impedance increases in magnitude while the phase is always 0°. The large value of low frequency resistance is helpful for load sharing but could impact the stability. In particular, the magnitude of the load input impedance is also at its smallest value under full load condition. This condition gives the highest possibility of source and load interaction. The full-load source and load interaction is the most critical case for the stability analysis at low-frequency.

Another frequency range that needs attention is the resonant frequency, where the peak of the output impedance appears. The high output resistance of nonlinear droop helps damping the resonant peak around 1.2 kHz, which improves the

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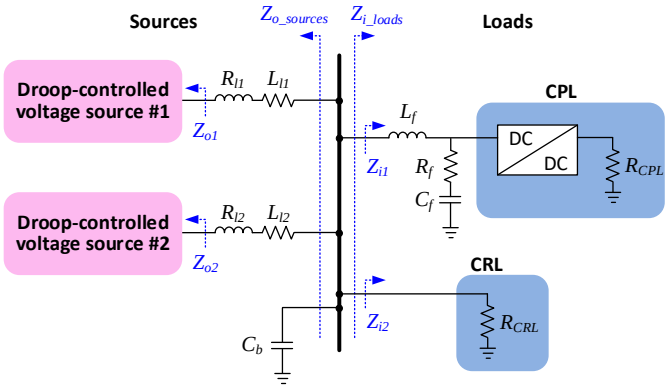

Fig. 22. Example dc power distribution system for stability analysis.

stability. This damping effect is also reported in [33]. Due to this two-fold effect, the total impact on stability needs to be systematically evaluated with the knowledge of the load system.

C. DC System Stability Analysis with Resistive and Constant Power Load

To make the discussion concise and representative, the two-source two-load system shown in Fig. 22 is used. In this system, all the source and load converters use the same parameters discussed previously, so the aforementioned input and output impedances can be readily used. The two paralleled source converters share the load by droop control. The constant power load (CPL) has negative small-signal input impedance. A constant resistive load (CRL) is also connected to the dc bus.

Besides the power sources and loads, extra elements are also included to make the system practical. L_f, C_f and R_f constitute the input filter for the load converter to reduce its EMI emission [32]. The value of L_f is 50 μH and C_f is 100 μF. Thus, their resonant frequency is 2.25 kHz (around 1/10 of the switching frequency). R_f is 0.5 Ω to damp the resonant peak of L_f and C_f. Cable inductances and resistances are also inserted between the source converters and system dc bus where R_{l1} = R_{l2} = 0.5 Ω, L_{l1} = L_{l2} = 100 nH. An 840μF, 0.25 mΩ bulky bus capacitor connects to the bus to provide the transient energy.

To investigate the stability, the system is separated into source section and load section. The input and output impedances at the section interface are examined using Nyquist criterion. Generally, the Nyquist plot needs to stay away from (-1, 0) to make the system stable.

The load system consists of CPL and CRL. Given a total system rating P_{total}, the load system input impedance varies with different ratio between these two kinds of load. To assist the analysis, penetration depth k is defined in (37) as the ratio between the power of CPL and total load power P_{total}.

$$k = P_{CPL} / P_{total}, 0 \le k \le 1 \tag{37}$$

The total load system small-signal input impedance at dc, i.e., input resistance, can be calculated as

$$Z_{i\_dc} = \left(-R_{CPL\_eq}\right) \| R_{CRL} = \frac{-R_{CPL\_eq} R_{CRL}}{-R_{CPL\_eq} + R_{CRL}} \tag{38}$$

where R_{CPL_eq} is the CPL load resistance R_{CPL} reflected to its input side. For a buck converter, R_{CPL_eq} = R_{CPL}/D^2 where D is

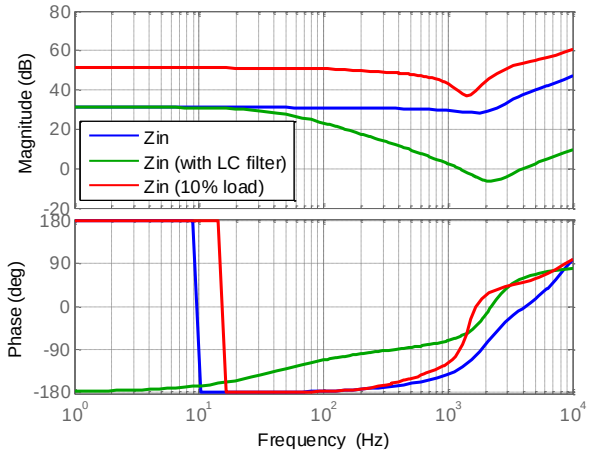

Fig. 23. CPL input impedance with and without input LC filter, and under different load conditions.

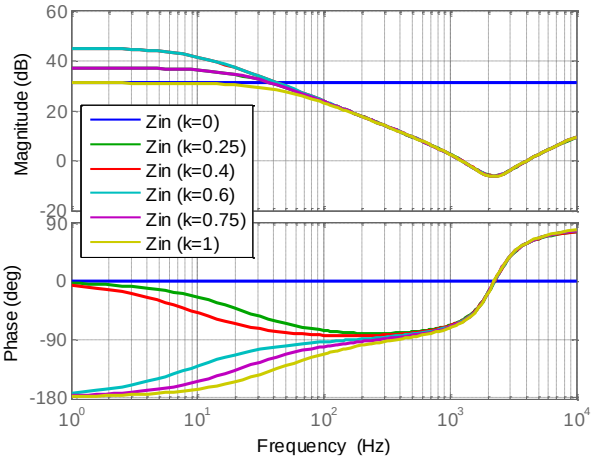

Fig. 24. Load system input impedance with a combination of CPL and CRL.

the converter duty cycle. R_{CRL} is the resistive load directly connected to the dc bus.

Clearly, when R_{CPL_eq} < R_{CRL}, i.e., P_{CPL} > P_{CRL}, the load system total input impedance Z_{i_dc} is negative at dc, representing a CPL dominant system. When R_{CPL_eq} > R_{CRL}, i.e., P_{CPL} < P_{CRL}, Z_{i_dc} is positive, representing a CRL dominant system.

Fig. 23 compares the input impedance of CPL under heavy load with and without an input LC filter. The impedance with only 10 % load is also drawn. Heavy load with an LC filter has the lowest input impedance magnitude and is used for the stability analysis.

The impact from penetration depth is investigated by sweeping k from 0 to 1. The result is shown in Fig. 24. When k = 1, the system only has CPL. The input impedance has the lowest magnitude and largest phase delay. This gives the worst condition for system stable operation.

For the source system, the total output impedance $Z_{o\_sources}$ is equal to the combination of source converters' output impedances, cable impedances, and dc bus capacitance, such that

$$Z_{o\_sources} = \left(Z_{o1} + Z_{line1}\right) \| \left(Z_{o2} + Z_{line2}\right) \| Z_{cbus} \tag{39}$$

where $Z_{line1} = R_{l1} + sL_{l1}$, $Z_{line2} = R_{l2} + sL_{l2}$, $Z_{cbus} = 1/\left(sC_{bus}\right)$.

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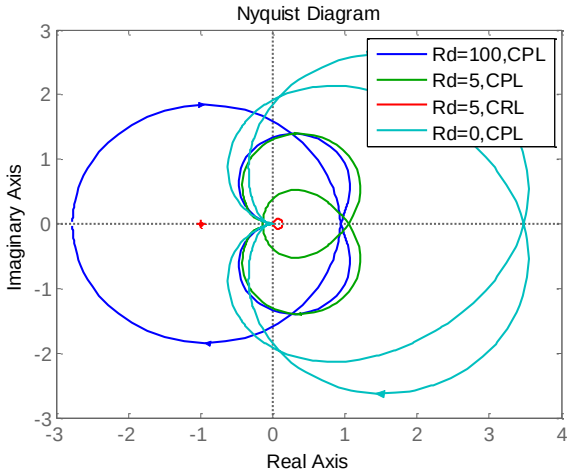

Fig. 25. System Nyquist plot without cable impedance and bus capacitance.

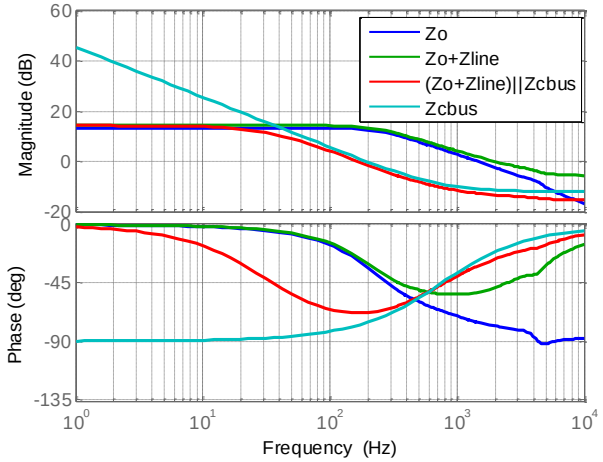

Fig. 26. Total source system output impedance.

Firstly, the system stability is investigated without considering the cable parameters and bus capacitor. The impedances of $Z_{o\_sources}$ and Z_{in_loads} are compared by scanning different droop resistance R_d using Nyquist plot. In Fig. 25, the minor loop gain T_{minor} = $Z_{o\_sources}$ / Z_{in_loads} is drawn. As predicted, if the load is pure CPL, the input behaves as a negative resistance. In such case, the droop resistance cannot be infinite. The blue contour encircles (-1, 0), and the system is unstable when R_d is 100 Ω. Thus, infinite droop resistance is only suitable for a CRL dominated system, i.e., k<0.5. This can be improved by using input impedance shaping techniques [34], [35]. Similar to droop control regulating output impedance, control loops can be used to regulate input impedance, so the input impedance is no longer a negative resistance.

On the other hand, if $|Z_{o\_sources}| < |Z_{in\_loads}|$ is satisfied, droop control can be used even with pure CPL. It can be observed that, the system stability is not impacted when R_d increases from 0 to 5 Ω with the same CPL. The green curve even has a larger phase margin than the cyan curve, due to the damping effect of the high droop resistance. If the load is CRL, the Nyquist plot covers a very small area far away from (-1, 0) regardless of the droop method, which implies a very sufficient stability margin.

Next, the system stability is investigated with pure CPL as this is the worst operating condition. The source system total output impedance is drawn in Fig. 26. Z_o is the converter output impedance. The impact from the extra components can be identified sequentially. By adding cable impedance Z_{line}, the high frequency output impedance rises due to the line inductance. The low frequency characteristic is barely changed. Since the bus capacitor is in parallel with the converter system, this capacitor can effectively lower the total output impedance if the impedance of the capacitance path (Z_{cbus}) is lower than the remaining source system (Z_o+Z_{line}). Hence, the dc bus capacitor helps to increase the stability margin. If one compares the blue and red contours in Fig. 27, the red contour is much farther away from point (-1, 0). The dc bus capacitor may even stabilize an unstable system if it is sufficiently large. The trade-offs are the extra cost, size, and stored energy in this bulky capacitor.

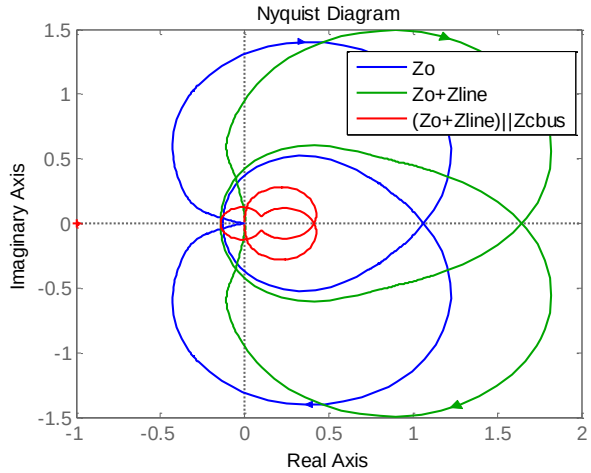

Fig. 27. System Nyquist plot after adding cable impedances and bus capacitance.

In summary, the stability analysis draws the following conclusions: If the load system is CRL dominant, the droop resistance can be infinite without introducing stability issues. If the load system is CPL dominant, the magnitude of the source system output impedance needs to be smaller than the load system input impedance. Thus, the droop resistance may not be infinite. For a pu system that has a minimum load resistance of 1 pu, the total source output impedance needs to be smaller than 1 pu. If the cable voltage drop is smaller than 0.05 pu, a droop resistance of 0.25 pu (e.g., the 5th-order droop) under full load is an acceptable value; it guarantees a 12 dB gain margin and minimizes the impact from cables on load sharing.

VI. Experimental Verification

A. Two-Source System with Ramping Load

The two-source system in Fig. 10 is used to compare the performance of the nonlinear droop and linear droop. In the experiment, Source 1 and Source 2 are buck and boost converters, respectively, to make the system more generally applicable. The current limit for the two sources is 7.5 A, and

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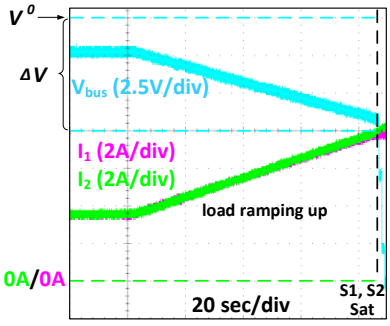

Fig. 28. Linear droop with negligible cable resistance.

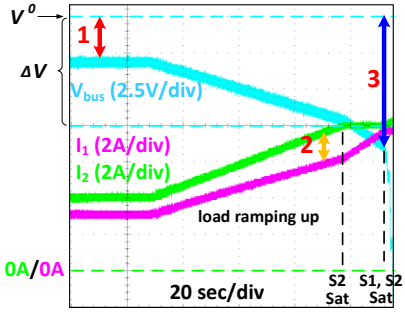

Fig. 29. Linear droop (ΔV = 7.5 V) with 0.2 Ω cable resistance.

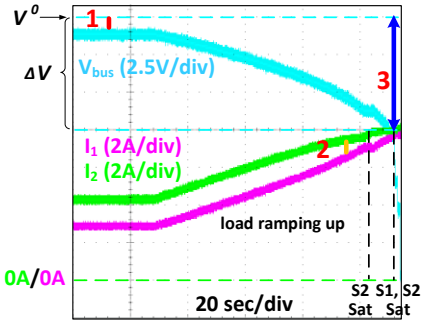

Fig. 30. Inverse parabola droop (ΔV = 7.5 V) with 0.2 Ω cable resistance.

the droop voltage range is 7.5 V. Programmable electronic loads are used to generate a linear ramping-up load current.

In the first test, the source converters are placed very close to the load with negligible cable resistance. The sensors are also calibrated so the sensor discrepancy is minimized. As shown in Fig. 28, after the start-up, the two sources reach a steady state and share the load evenly. Then, the load is triggered to ramp up. During the load ramping-up process, the two sources always share the same amount of load, which proves the effectiveness of droop control. When the load continues increasing, the sources finally become saturated, and the bus voltage collapses.

In the next experiment, a five-meter AWG 18 cable (0.2 Ω) is inserted between Source 1 and the load. Fig. 29 and Fig. 30 present the experimental waveforms using the linear and inverse parabola droop methods, respectively. As stated above, both droop methods are designed with a 7.5 V droop voltage range. Comparing Fig. 29 and Fig. 30, the advantages of the nonlinear droop can be observed. Under a light load (Point 1), the nonlinear droop has smaller voltage deviation. When the load current ramps up (Point 2), the current difference between Source 1 and Source 2 becomes larger in the linear droop but becomes smaller in the nonlinear droop. The sharing error decreases automatically when the load increases with the

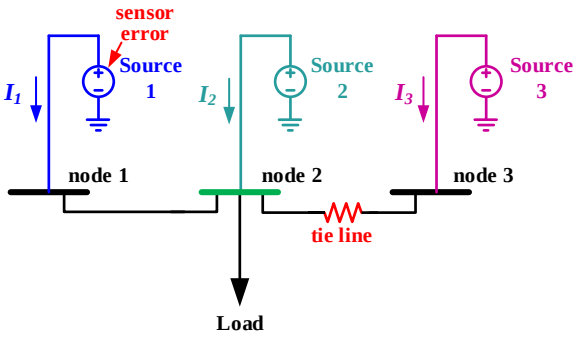

Fig. 31. Three-source dc system with tie-line resistance and measurement error.

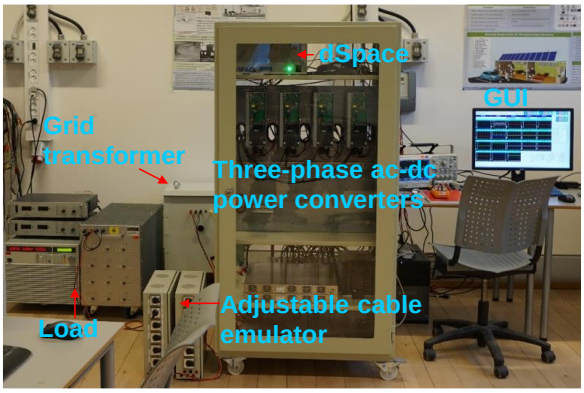

Fig. 32. DC microgrid testbed to evaluate different droop methods.

nonlinear droop. If we compare the voltage deviation from no load to the point where both sources are saturated (Point 3), the deviation for the nonlinear droop is within the designed 7.5 V droop voltage range, while it drops another 2 V below the 7.5 V for the linear droop.

B. Three-Source System with Cable Resistance and Sensor Offset

A three-source system shown in Fig. 31 and Fig. 32 is designed as the testbed to demonstrate the advantages of nonlinear droop control in multi-source systems with both cable resistances and sensor drifts. Three power sources are connected through adjustable cable emulators. The system load is connected to node 2. The tie-line resistance is zero from node 1 to node 2 and is 1 Ω from node 2 to node 3. Among the three sources, only Source 1 has a 1 V sensor offset. Thus, in the experiment, the current difference between Source 1 and Source 2 is caused by the sensor error; the difference between Source 2 and Source 3 is caused by the tie-line resistance.

In this test, the droop voltage range is 380 V to 400 V. The current rating for all the sources is 5 A. Linear droop and different 2nd-order droop profiles are tested. Fig. 33 and Fig. 34 show the droop performance under light and heavy loads, respectively. Within each figure, the load is fixed; the droop profiles for all three sources are identical and change simultaneously from linear to inverse parabola, to parabola, and to ellipse. By comparing the bus voltage deviation from the voltage set point and the current difference between the sources, the benefits of nonlinear droop are proven. According to the graphs, the output voltage from high to low are ellipse, parabola, inverse parabola and linear under light load. Under heavy load,

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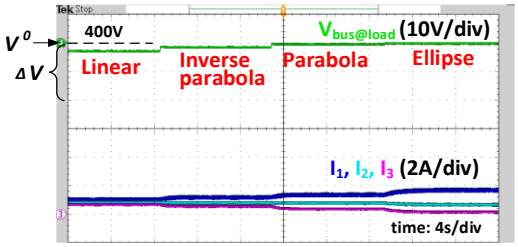

Fig. 33. Droop comparison under light load.

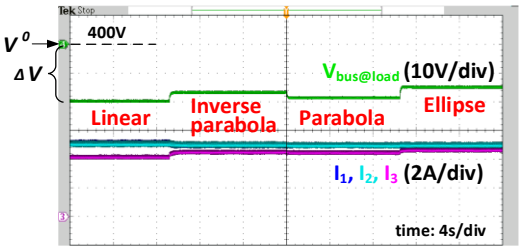

Fig. 34. Droop comparison under heavy load.

the parabola and inverse parabola switch sequences. The inverse parabola and ellipse have the smallest voltage deviation under light load and the smallest current deviation under heavy load.

C. Impedance Measurement

The output impedance of power converters is intrinsically the transfer function from the output current to the output voltage, which can be measured by injecting perturbation and measuring the response using a network analyzer. Since the measured units are high-power converters rated in the 5–10 kW range, a power amplifier is necessary to inject adequate perturbation signals. In the experiment, the bandwidth of the power amplifier is 20 Hz to 20 kHz. As the switching frequency is 20 kHz, the output impedance is measured from 20 Hz to 10 kHz. High-bandwidth voltage and current probes are placed at the converter output port to measure the voltage and current. The measurement setup is shown in Fig. 35.

The output impedance of a buck converter with linear and nonlinear droop control is measured under different load conditions. The droop voltage range is from 380 V to 400 V. The current rating is 10 A. The measurement results for elliptic droop are presented in Fig. 36. The load resistances are 300, 100, and 42 Ω to typify the converter output impedance at light

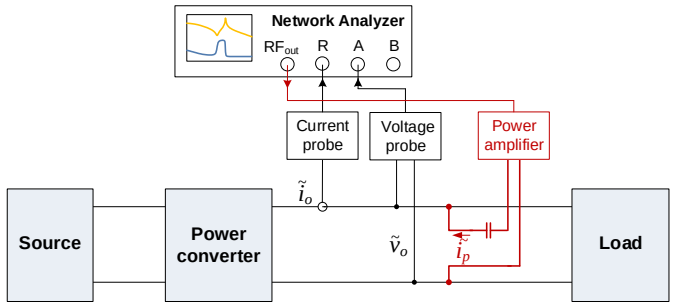

Fig. 35. Converter output impedance measurement setup.

load, medium load, and heavy load conditions (13 %, 40 %, and 93 % load respectively). In the graph, the blue curve consists of a series of measurement points from 20 Hz to 10 kHz. The red line is the modeled output impedance using (33). The measurement results prove the output impedance model is accurate from dc to half of the switching frequency for different droop resistances.

VII. Conclusion

Traditional linear droop faces the design trade-off between load sharing accuracy and bus voltage regulation due to cable resistances and sensing errors. Piecewise linear and nonlinear droop control features a varying droop resistance when the converter output current changes. This leads to a more balanced load sharing and tighter bus voltage regulation. A generic polynomial expression is presented to unify different droop equations.

By tuning the parameters of polynomial droop equations, the slope of the droop curves, i.e., the droop resistance, can be finely adjusted from no load to full load. Elliptic and inverse parabolic droop have small output resistance under light load and infinite output resistance under full load; thus, they achieve best load sharing under heavy loads. They can work with a CRL dominated system, but their infinite output resistance causes instability in a CPL dominated system. By increasing the order of current *i* in the droop equation, its full-load droop resistance can be increased. The 5th-order polynomial equation achieves 5 times the droop resistance than the linear droop and effectively minimizes the load sharing unbalance; it is also stable under full load with CPL.

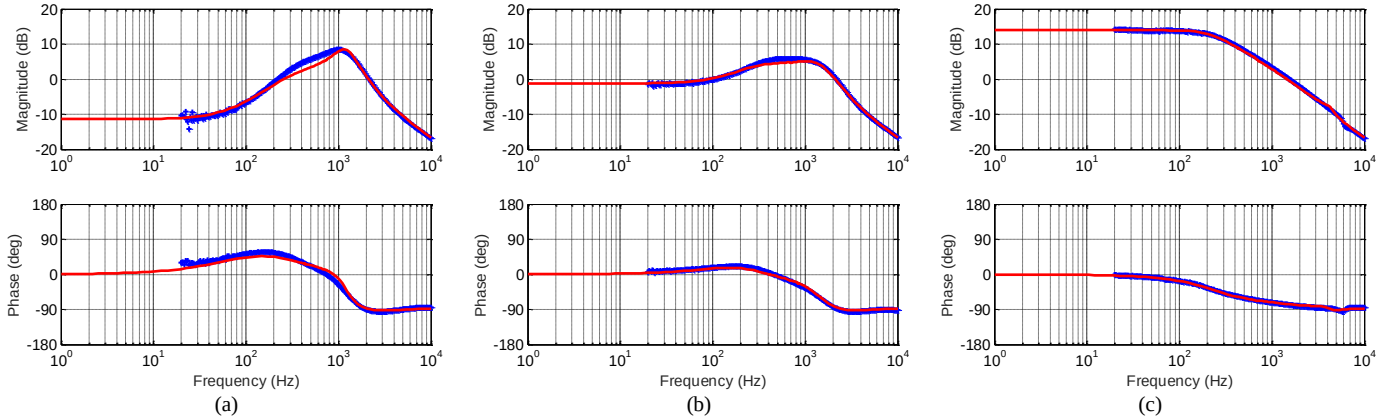

Fig. 36 Output impedance of the elliptic droop under (a) light load (b) medium load, and (c) heavy load.

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TABLE I
COMPARISON OF DIFFERENT DROOP PROFILES

Droop Profile	*m*	*n*	Droop Equation	R_d Expression	No-load and full-load R_d $(\Delta V_{pu} = 0.05pu)$	Remarks
Linear (L)	1	1	$v_{pu} = 1 - \Delta V_{pu} \cdot i_{pu}$	ΔV_{pu}	0.05 pu	Worst load sharing at full load.
Piecewise linear	1	1	*Example:* R_{d_L}: R_{d_M} : R_{d_H} = 1:4:9	R_{d_L} = 0.0153 pu R_{d_M}= 0.0611 pu R_{d_H} = 0.1375 pu	0.0153 pu, 0.1375 pu	Different droop resistances for different load ranges. Need attention on slope sudden change.
Parabola (P)	1	2	$v_{pu} = 1 - \Delta V_{pu} \left(i_{pu}\right)^2$	$2 \cdot \Delta V_{pu} \cdot i_{pu}$	0, 0.1 pu	2X R_d than linear at full load. No load sharing at no load.
5th-order Polynomial	1	5	$v_{pu} = 1 - \Delta V_{pu} \left(i_{pu}\right)^5$	$5 \cdot \Delta V_{pu} \cdot i_{pu}$	0, 0.25 pu	5X R_d than linear at full load. No load sharing at no load.
Inverse Parabola (IP)	2	1	$v_{pu} = 1 - \Delta V_{pu} + \Delta V_{pu} \sqrt{1 - i_{pu}}$	$\frac{\Delta V_{pu}}{2} \frac{1}{\sqrt{1 - i_{pu}}}$	0.025 pu, ∞	Best load sharing at full load. Some load sharing at no load. Unstable with heavy CPL.
Ellipse (E)	2	2	$v_{pu} = 1 - \Delta V_{pu} + \Delta V_{pu} \sqrt{1 - \left(i_{pu}\right)^2}$	$\Delta V_{pu} \frac{i_{pu}}{\sqrt{1 - \left(i_{pu}\right)^2}}$	0, ∞	Best load sharing at full load. No load sharing at no load. Unstable with heavy CPL.

The nonlinear droop changes the converter's output impedance at low frequency and resonant frequency. When R_d is large, it damps the resonant peak but increases the magnitude of low-frequency output impedance. When R_d is small, the low-frequency output impedance can be smaller than linear droop, but the damping effect is lost. Compared to linear droop, two extra cases need examination when using impedance-based stability criteria: the heavy-load low-frequency interaction and the light-load resonant-frequency interaction.

Table I summarizes different droop profiles. Their droop equations and corresponding droop resistances are listed. Piecewise and nonlinear droop control achieve better load sharing under heavy load and better voltage regulation under light load, due to the characteristic of a varying droop resistance. Their no-load and full-load droop resistances are calculated assuming a 5 % droop voltage range. Their stability performance is also noted.

The nonlinear droop control only uses the local current information and needs no communication, so the advantage of full distribution in droop control is preserved. Experiments for two-source and three-source systems verify the effectiveness of the nonlinear droop with cable resistances and sensing errors. The output impedance of a high-power dc-dc converter is measured and verifies the developed impedance model.

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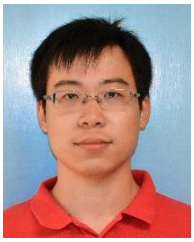

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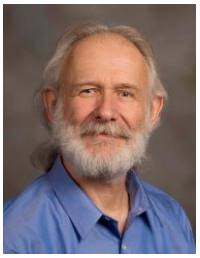

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