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Modulation for the AVC-HERIC Inverter to Compensate for Deadtime and Minimum Pulse Width Limitation Distortions

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***Abstract*– With the superiority in leakage current suppression, the active voltage clamping highly efficient and reliable inverter concept (AVC-HERIC) has become a promising candidate in low- and medium-power PV systems. In addition, the high power density and low system costs have been attained in the AVC-HERIC due to the removal of the isolation transformers. However, to maintain high efficiency and good power quality under reactive power injection, prior-art modulation methods for the AVC-HERIC should be modified. In this paper, a simple modulation scheme is proposed for the AVC-HERIC, which ensures bidirectional current flow at any time. An improved modulation scheme is implemented according to the reference voltage polarity, and it is integrated into the proposed scheme to enable flexible reactive power injection. Moreover, the improved modulation scheme can maintain the same high efficiency as adopting the unipolar pulse width modulation (UP-PWM) strategy. More importantly, the deadtime and minimum pulse width limitation (MPWL) distortions are compensated effectively by the proposed modulation, leading to a good power quality. Simulations and experimental tests are performed on a 3-kW AVC-HERIC, and the results verify the effectiveness of the proposed modulation.**

***Index Terms*– AVC-HERIC, deadtime, pulse width modulation (PWM), efficiency, power quality, reactive power injection, minimum pulse width limitation (MPWL).**

I. INTRODUCTION

SOLAR photovoltaic (PV), as a strong representative renewable energy source, plays an important role in power grid modernization [1], [2]. Owing to its inherent characteristics, e.g., the intermittency and regional difference, the low-power and medium-power PV generation systems are more attractive [3], [4]. Considering the entire system volume cost and efficiency, transformerless single-phase inverters are of high interest as the power interfaces in grid-connected PV systems with such power levels [5]. Transformerless inverters remove isolation transformers for higher efficiency, and yet, critical leakage currents may appear in practice [6], [7], posing a threat to other grid-connected systems and maintenance personnel. Thus, addressing the leakage current issue is a major task in transformerless PV applications [8], [9].

For the conventional two-level single-phase inverter, the bipolar pulse width modulation (BP-PWM) scheme can be employed to alleviate the leakage currents [10]. However, owing to its two-level output voltages, large output filters are required, and also high switching losses are associated with it. Alternatively, many topologies have been presented to tackle the leakage current issue, while increasing the power density with high efficiency [11]-[18]. Typically, such topologies can be categorized into two groups. One is to decouple the DC-link and full-bridge inverter by adding extra circuits at the DC side. Representative inverters in this group include the H5, H6 and passive-clamped H6 inverters [11]-[13]. In contrast, the other group adopts an AC-decoupling circuit to realize isolation when providing zero voltage levels, e.g., the AC-H6 topologies [14]-[16] and the HERIC [17]. When comparing the above topologies, it is known that the DC-decoupling-based inverters and AC-H6 topologies generate more conduction losses than the HERIC. This is due to that the current flows through three or four power switches to achieve positive or negative voltage levels in the DC-decoupling and the AC-H6 inverters; while the current only flows through two power devices under the same condition for the HERIC inverter. What's more, the switching frequency of the DC-decoupling switches is twice that of the other switches in the DC-decoupling transformerless inverters [11]-[13], resulting in unbalanced losses. Nevertheless, the above topologies can address the leakage current issue to a large extent.

Additionally, with the increase of the switching frequency, stray capacitances (i.e., the junction capacitance of the power device and capacitance between the switches and the heatsink) will negatively affect the leakage current suppression. Thus, many neutral-point-clamped topologies (i.e., active clamping and passive clamping) were introduced in the literature to clamp the common mode voltage (CMV) to a constant [18]. In this case, during the charging and discharging processes of the junction capacitance, the large capacitors of the clamping

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circuit ensure a constant CMV in contrast to the conventional solutions (i.e., without an extra clamping circuit, and the CMV is clamped only by the junction capacitances). Clearly, with the clamping structure, the leakage current can be suppressed more effectively. When compared to the passive clamping HERIC, [18] and [19] have thus emphasized that the Active Voltage Clamping HERIC (AVC-HERIC) topology has a better performance in terms of leakage current suppression.

In addition to the leakage current issue, the reactive power injection is also of importance in grid-friendly PV systems [9], [20]. For instance, the IEEE Std 1547-2018 clearly defines the minimum reactive power injection and absorption (i.e., 44% and 25% of the rated apparent power, respectively) for distributed energy resources [20]. To achieve so, modulation methods for the above transformerless inverters should be retrofitted [10], which in turn affects the efficiency and power quality performance. For example, the BP-PWM scheme can suppress the leakage current and enable the inverter to provide reactive power upon demand, but the efficiency is low [10]. Many attempts have thus been made to the retrofit of the modulation schemes, i.e., the strategy in [21], where the unipolar PWM (UP-PWM) and BP-PWM were combined for the H5 inverter. However, when the BP-PWM is in operation for the H5 inverter, additional switching power losses and large ripple currents appear. To solve this issue and enhance the reactive power controllability simultaneously, a modified modulation technique providing a bidirectional path during freewheeling periods was proposed for the H5 and HERIC topologies [22]. According to the concept in [22], modified modulation techniques were further introduced recently for several transformerless inverter variants (i.e., the H5, AC-H6, and AVC-HERIC topologies) to achieve reactive power injection [19]-[23]. Nevertheless, the above requires deadtime to prevent the inverter from short-circuit fault in a switching interval [24], [25]. Additionally, the minimum pulse width limitation (MPWL) should be considered to ensure the normal ON-state time for the power devices in operation. Then, the power quality may be enhanced.

Although the deadtime has a negligible impact on power losses, it will lead to high distortions in the output current if not well considered. Therefore, many deadtime compensation methods were proposed to improve the power quality [25], [26]. For instance, the sixth-order harmonic voltage, which is generated by the integrator output of the proportional–integral (PI) current regulator, was used to compensate the output voltage distortion caused by deadtime [26]. However, this voltage-fed deadtime compensation method is not specifically suitable for single-phase inverters. Then, a predicted current control method to achieve adaptive deadtime compensation was proposed in [27]. In this case, a nonlinear deadtime disturbance model should be established to generate a feed-forward compensation term, and the model parameters have to be updated in real time. This requires high-performance digital processors with powerful computation capability. To avoid the complexity and implementation burden, the compensation can be achieved by only modifying the modulation strategy. Doing so not only benefits the deadtime compensation, but also contributes to alleviating the MPWL effect. Accordingly, a hybrid modulation method for the HERIC inverter was introduced in [29] to simultaneously maintain high efficiency, proper reactive power injection as well as to compensate for the deadtime and MPWL distortions. Yet, the operation of the hybrid modulation method is complicated, and the operation modes are not suitable for the AVC-HERIC. In all, it calls for advanced modulation strategies for the AVC-HERIC inverter to maintain high efficiency, flexible reactive power injection and good power quality.

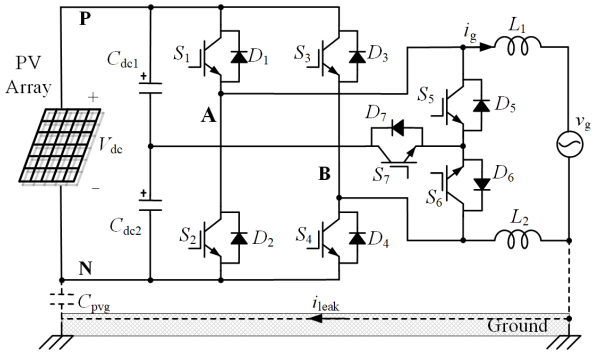

Fig. 1. Schematic of the grid-connected AVC-HERIC inverter system, where i_{leak} is the leakage current, C_{pvg} is the parasitic capacitance between the PV array and the ground, C_{dc1} and C_{dc2} are two capacitors at the DC-link, i_g is the grid current, v_g is the grid voltage, and L_1, L_2 are the output filter inductance with $L_1 = L_2 = L/2$.

In light of the above, a simple modulation scheme for the AVC-HERIC inverter is proposed in this paper, as an extension of [30]. The proposed modulation strategy can provide a bidirectional current path to obtain a zero-voltage level for reactive power injection as well as high efficiency. Furthermore, the deadtime and MPWL distortions are effectively compensated by the proposed modulation strategy, leading to an improved output power quality. The rest of this paper is organized as follows. In Section II, the deadtime and the MWPL effects on the power quality are analyzed. Following, the proposed modulation scheme is introduced, where the deadtime is properly inserted. The proposed compensation strategy for the MPWL effect is detailed in Section III. Simulations and experimental tests are carried on a 3-kW single-phase AVC-HERIC inverter system to validate the performance of the proposed modulation, and the results are presented in Section IV. Finally, concluding remarks are provided in Section V.

II. ANALYSIS OF THE DEADTIME AND MPWL

An AVC-HERIC inverter system with an L-type filter is shown in Fig. 1, where the full bridge part includes $S_{1\text{-}4}$ (with antiparallel diodes $D_{1\text{-}4}$), and three additional power devices $S_{5\text{-}7}$ (with antiparallel diodes $D_{5\text{-}7}$) are adopted to actively clamp the CMV to the midpoint of the DC-link (i.e., the midpoint of the two capacitors C_{dc1}, C_{dc2} in Fig. 1) [18]. For simplicity, the DC-link voltage V_{dc} is assumed to be constant. According to the Kirchhoff's Voltage Law (KVL), the dynamics for the inverter output can be described as

$$v_L(t) = L\frac{di_g(t)}{dt} = v_{AB}(t) - v_g(t) \tag{1}$$

where $L = L_1 + L_2$ with $L_1 = L_2$ being the output filter inductor, $i_g(t)$ is the grid-connected current, $v_g(t)$ is the grid voltage, and $v_{AB}(t)$ is the output differential-mode voltage.

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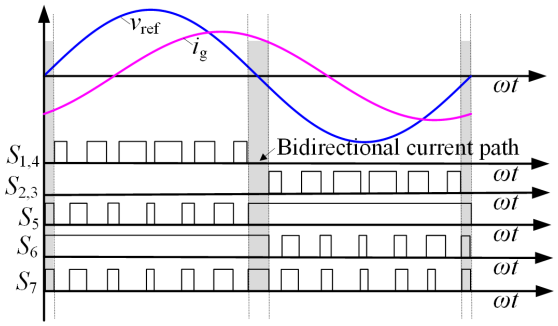

Fig. 2. Modulation scheme for the AVC-HERIC inverter, where v_{ref} is the reference voltage and i_g is the grid current. In the shaded areas, a bidirectional current path is provided.

A. Improved modulation strategy for the AVC-HERIC

According to the modulation concept in [19] and [22], an improved modulation scheme for the AVC-HERIC inverter is shown in Fig. 2. The operation mode is switched by judging the polarity of the desired output voltage v_{ref} (i.e. the ideal fundamental-frequency component of the voltage v_{AB}). When $v_{ref} \geq 0$, S_6 is always ON, and S_2, S_3 are in the OFF-state, as shown in Fig. 2. In this case, S_1, S_4 and S_5, S_7 operate at a high frequency to achieve the inverter output voltages of $+V_{dc}$ and 0. When $v_{ref} < 0$, S_5 is always ON in this period, and S_1, S_4 are in OFF-state, which is illustrated in Fig. 2. Similarly, S_2, S_3 and S_6, S_7 are switched at a high frequency to achieve the output voltages of $-V_{dc}$ and 0. As highlighted in Fig. 2 (shaded areas), $S_{5\text{-}7}$ are in ON-state to achieve the bidirectional current path.

Assuming that the grid voltage is $v_g(t) = V_m\sin(\omega t)$ and the grid current $i_g(t) = I_m\sin(\omega t\text{-}\alpha)$, where V_m and I_m are the amplitudes of the grid voltage and current, respectively, ω is the angular frequency of the grid voltage and α is the power factor angle. According to (1), it can be obtained that

$$v_{AB}(t) = V_m \sin(\omega t) + L\omega I_m \cos(\omega t - \alpha) \tag{2}$$

Neglecting the term of $L\omega I_m\cos(\omega t\text{-}\alpha)$ in (2), the duty cycle u of the improved modulation method is obtained as

$$u = \frac{V_m \sin(\omega t)}{V_{dc}} \tag{3}$$

where $v_{AB} = -uV_{dc}$ in one switching cycle. Then, the derivative of the desired grid current can be expressed as

$$\frac{di_g^*(t)}{dt} = \frac{-uV_{dc} - V_m \sin(\omega t)}{L} \tag{4}$$

As observed in (3), the improved modulation strategy is simple, but it can achieve a high efficiency like the UP-PWM method for the AVC-HERIC inverter at unity power factor. In addition, due to the bidirectional current path during the freewheeling period, the proposed modulation can flexibly achieve reactive power injection. However, the operation modes of the improved modulation method in practice should avoid the short-circuit phenomenon and ensure sufficient conduction time for power devices. This is achieved by adding the deadtime between the high-frequency switchover of the full-bridge inverter switches (i.e., $S_{1\text{-}4}$) and the AC-decoupling switches (i.e., $S_{5\text{-}7}$), as shown in Fig. 1. Moreover, the MPWL should be set when the duty cycle is too small or too large to achieve an effective conduction of power devices. Obviously, the deadtime and MPWL will lead to distortions in the grid current, and then, degrade the power quality. The distortion mechanism will be detailed in the following.

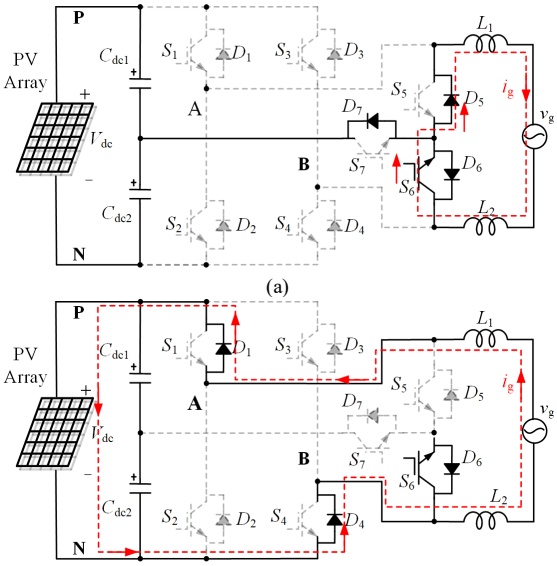

Fig. 3. Current path during the deadtime in different conditions for the AVC-HERIC inverter: (a) $v_{ref} > 0$, $i_g > 0$ and (b) $v_{ref} > 0$, $i_g < 0$.

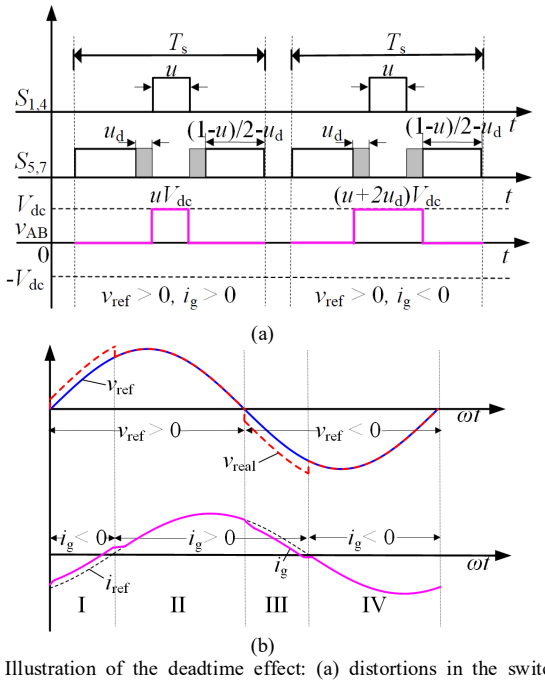

Fig. 4. Illustration of the deadtime effect: (a) distortions in the switching cycles when $v_{ref} > 0$ and (b) at non-unity power factor in one fundamental period, where I and III are the regions with reactive power output, while II and VI are the regions for active power generation.

B. Analysis of the deadtime effect

Considering the positive half cycle, the operation modes of the AVC-HERIC inverter with deadtime are shown in Fig. 3. Notably, the AVC-HERIC can clamp the CMV to a half of the DC-link voltage by the anti-parallel diode D_7 during the deadtime, as shown in Fig. 3(a). It is assumed that the deadtime is inserted in the freewheeling period, and thus only S_6 is in the ON-state, as demonstrated in Fig. 3. Observations

from Fig. 3(a) (i.e., $v_{ref} > 0$, $i_g > 0$) show that the grid current flows through S_6 and D_5 to achieve a zero voltage, i.e., $v_{AB} = 0$. When $v_{ref} > 0$, $i_g < 0$, the grid current flows through D_1 and D_4 to generate a positive voltage, i.e., $v_{AB} = +V_{dc}$ in the deadtime interval, as shown in Fig. 3(b). Correspondingly, the output voltage distortion in one switching cycle can be exemplified as shown in Fig. 4(a). Assuming that the turn-on (t_{on}) and turn-off (t_{off}) times are the same and the distorted voltage occurs with a duration u_d [25], the resultant distorted voltage Δv can be averaged as

$$\Delta v = \begin{cases} 0 & , v_{ref} > 0, i_g > 0 \\ 2u_d V_{dc} & , v_{ref} > 0, i_g < 0 \end{cases} \tag{5}$$

which implies that the real output voltage v_{real} is larger than the desired output voltage v_{ref} by $2u_dV_{dc}$. A similar analysis of the distorted voltage can be applied to the negative half cycle of the reference voltage v_{ref}, where v_{real} will be smaller than v_{ref} by $2u_dV_{dc}$ with $i_g > 0$. The distortions in v_{real} and i_g induced by the deadtime during one fundamental-frequency period are demonstrated in Fig. 4(b), and v_{real} can be expressed as

$$v_{real} = \begin{cases} v_{ref} & , v_{ref} i_g > 0 \\ v_{ref} + \mathrm{sgn}(v_{ref}) \cdot \Delta v & , v_{ref} i_g < 0 \end{cases} \tag{6}$$

The above analysis illustrates that the distorted voltage caused by the deadtime appears when generating reactive power (i.e., $\alpha \neq 0$). Unfortunately, the distorted voltage will propagate to the grid current i_g. According to (4), the distorted current Δi_g in one fundamental-frequency period can be obtained as

$$\begin{aligned} \Delta i_g &= \begin{cases} 0 & , v_{ref} i_g > 0 \\ \int_0^{\alpha} \dfrac{v_{real} - V_m \sin(\omega t)}{\omega L} - \dfrac{v_{ref} - V_m \sin(\omega t)}{\omega L} d\omega t & , v_{ref} i_g < 0 \end{cases} \\ &= \begin{cases} 0 & , v_{ref} i_g > 0 \\ \int_0^{\alpha} \dfrac{\mathrm{sgn}(V_{ref}) 2u_d V_{dc}}{\omega L} d\omega t & , v_{ref} i_g < 0 \end{cases} \\ &= \begin{cases} 0 & , V_{ref} i_g > 0 \\ \dfrac{\mathrm{sgn}(V_{ref}) 2\alpha u_d V_{dc}}{\omega L} & , V_{ref} i_g < 0 \end{cases} \end{aligned} \tag{7}$$

which indicates that the distorted current Δi_g is positively correlated with the deadtime duration u_d. In addition, it is implied in (7) that the distorted current Δi_g will increase when the reactive power output becomes larger. Besides, when the deadtime is inserted in the conduction period, the same distortions of the inverter voltage and the grid current will appear during outputting active power.

C. Analysis of the MPWL effect

As mentioned previously, the MPWL must be set to a suitable value to prevent from damaging the power devices. In practice, the MPWL exists when the duty cycle u is too small or too large. It means that when $u < u_M$ and $1 - u < u_M$, where u_M is the MPWL ratio in one switching cycle T_s, the distorted voltage will be generated at the voltage zero-crossing point and the voltage peak point, respectively. Generally, the state of $1 - u < u_M$ can be eliminated by increasing the DC-link voltage [25]. Therefore, only the condition of $u < u_M$ is discussed in this paper. The distortion region of the MPWL can be expressed as

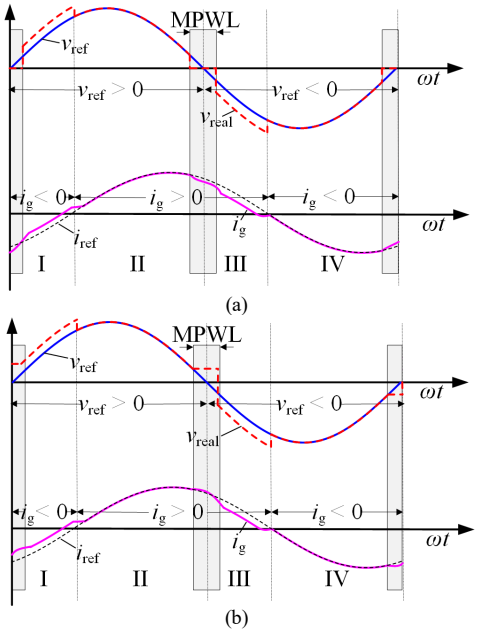

Fig. 5. Distortion of the inverter output voltage and grid current due to the MPWL and deadtime: (a) $u = 0$ during $u < u_M$ and (b) $u = u_M$ during $u < u_M$, where I and III are the regions for reactive power output, while II and VI are the regions for active power generation.

$$u_M = \left| \frac{V_m \sin(\omega t)}{V_{dc}} \right| \tag{8}$$

with

$$\omega t \in [-\theta_M, \ \theta_M], \quad \theta_M = \arcsin\left(\frac{u_M V_{dc}}{V_M}\right) \tag{9}$$

When the duty cycle $u < u_M$ (i.e., $\omega t \in (-\theta_M, \theta_M)$), there are two methods to set the MPWL. One is to let $u = 0$, and the other is to set $u = u_M$.

1) In the first method (i.e., $u = 0$ during the MPWL), the real current can be expressed as

$$\frac{di_g(t)}{dt} = \frac{0 - V_m \sin(\omega t)}{L} \tag{10}$$

and the desired current is shown in (4). Thus, the current distortion can be obtained by subtracting (10) with (4) as

$$\begin{aligned} |\Delta i| &= \int_{\pi - \theta_M/2}^{\pi} \frac{0 - V_m \sin(\omega t)}{\omega L} - \frac{-uV_{dc} - V_m \sin(\omega t)}{\omega L} d\omega t \\ &= \frac{uV_{dc}\theta_M}{2\omega L} \end{aligned} \tag{11}$$

2) In the second method (i.e., $u = u_M$ during the MPWL), the actual current can be expressed as

$$\frac{di_g(t)}{dt} = \frac{-u_M V_{dc} - V_m \sin(\omega t)}{L} \tag{12}$$

Similarly, according to (4), the grid current distortion can be obtained as

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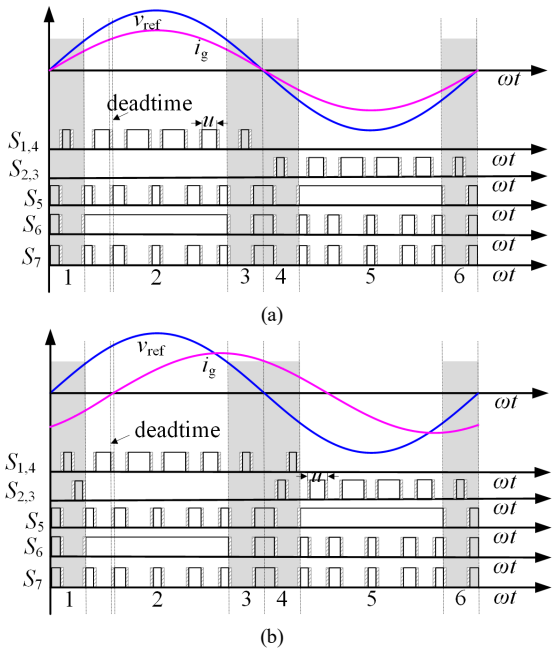

Fig. 6. Proposed modulation scheme for the AVC-HERIC inverter with the deadtime and MPWL compensation: (a) at unity power factor operation and (b) at non-unity power factor operation.

$$\begin{aligned}|\Delta i| &= \int_{\pi-\theta_M/2}^{\pi} \frac{-u_M V_{dc} - V_m \sin(\omega t)}{\omega L} - \frac{-u V_{dc} - V_m \sin(\omega t)}{\omega L} d\omega t \\ &= \frac{(u_M - u) V_{dc} \theta_M}{2\omega L}\end{aligned} \tag{13}$$

It is clear that grid current distortions will be induced by the MPWL in all cases. With the deadtime effect, the distorted voltage and grid current are demonstrated in Fig. 5. In all, the influence of the deadtime and MPWL on the AVC-HERIC inverter output is obvious in the improved modulation strategy. Notably, with the improved modulation scheme at the unity power factor operation, the grid current is affected only by the MPWL. When injecting reactive power, both the deadtime and the MPWL contribute to the current distortion. Therefore, a compensation modulation scheme should be adopted to eliminate the distortions in the AVC-HERIC.

III. PROPOSED MODULATION TECHNIQUE

In order to provide reactive power injection, improve the power quality as well as enhance the conversion efficiency, a simple modulation technique for the AVC-HERIC inverter is proposed in this section. The switching patterns for all the power devices are shown in Fig. 6. The modulation method can be divided into two parts:

1) *Improved modulation with deadtime compensation*: As shown in Regions 2 and 5 in Fig. 6, the proposed method adopts an improved modulation, which can provide a bidirectional current path, and thus leading to reactive power injection and a high efficiency. Moreover, in order to eliminate the deadtime distortions, a simple compensation method is proposed, which inserts the deadtime in different periods by judging the polarity of the output power.

2) *Compensation modulation for the MPWL*: In the shaded regions (i.e., Regions 1, 3, 4 and 6) in Fig. 6, the precise modulation methods are proposed to compensate for the distortions induced by the MPWL. When generating the active power, the MPWL is compensated by the output voltage during the deadtime. While providing the reactive power, the compensation voltage for the MPWL is achieved by operating the diagonal switches of the full-bridge inverter ($S_{1\text{-}4}$).

The operation principle of the proposed modulation for the AVC-HERIC is the elaborated in detail referring to Fig. 7:

Region 1, 3: (1) In regions 1 and 3 in Fig. 6(a) and region 3 in Fig. 6(b) (i.e., generating the active power), $S_{1,4}$ and $S_{5\text{-}7}$ are switched at a high frequency. As shown in Fig. 7(f), $S_{1,4}$ are in ON-state and the grid current i_g (i.e., denoted by the red solid arrow) flows through S_1 and S_4, and $v_{AB} = +V_{dc}$. While $S_{5\text{-}7}$ are ON (see Fig. 7(c)), the grid current i_g flows through S_6 and D_5, which gives $v_{AB} = 0$. Additionally, the deadtime should be inserted between the switchover transition of the above modes. During the deadtime, as shown in Fig. 7(h), the grid current i_g flows through D_2 and D_3 to obtain $v_{AB} = -V_{dc}$. (2) In region 1 of Fig. 6(b) (i.e., generating the reactive power), $S_{1,4}$, $S_{2,3}$ and $S_{5\text{-}7}$ are operating at a high frequency. The grid current i_g flows through S_1 and S_4 to obtain $v_{AB} = +V_{dc}$, when $S_{1,4}$ are ON, as denoted by the dotted blue arrow line in Fig. 7(f). Additionally, as shown in Fig. 7(c), and indicated by the dotted blue arrows, i_g flows through S_5 and D_6, and $v_{AB} = 0$. Moreover, as shown in Fig. 7(i), i_g flows through D_1 and D_4 to obtain $v_{AB} = +V_{dc}$. Therefore, $S_{2,3}$ should be ON to obtain the compensation voltage $v_{AB} = -V_{dc}$, where i_g flows through S_2 and S_3, as illustrated in Fig. 7(d), i.e., the red solid arrows.

Region 2: Operation principles in this region of Fig. 6(a) and (b) are the same. S_6 is ON, $S_{1,4}$ and $S_{5,7}$ are operated at a high frequency. The grid current i_g flows through S_1 and S_4 to obtain $v_{AB} = +V_{dc}$ when outputting the active power, while i_g flows through D_1 and D_4 to obtain $v_{AB} = +V_{dc}$ when generating the reactive power—see the red solid arrow line and blue dotted arrow line in Fig. 7(a), respectively. Moreover, the deadtime should be employed to avoid short-circuiting the DC side. As illustrated in Fig. 7(b), during the deadtime, i_g (the red solid arrow) flows through S_6 and D_5, leading to $v_{AB} = 0$ when outputting the active power. While generating the reactive power, i_g (i.e., the blue dotted arrow line in Fig. 7(b)) flows through the D_1 and D_4 to achieve $v_{AB} = +V_{dc}$.

Region 4, 6: (1) $S_{2,3}$ and $S_{5\text{-}7}$ are operated at a high frequency in regions 4 and 6 of Fig. 6(a) and region 6 of Fig. 6(b) (i.e., outputting the active power). When $S_{2,3}$ are ON as illustrated in Fig. 7(g), the grid current i_g (the red solid arrow line) flows through S_2 and S_3 to obtain $v_{AB} = -V_{dc}$. Then, when $S_{5\text{-}7}$ are in ON-state, the grid current i_g shown as the blue dotted arrow line in Fig. 7(c)) flows through S_5 and D_6 to achieve $v_{AB} = 0$. Obviously, during mode transitions where the deadtime is applied, the current i_g flows through D_1 and D_4 to obtain $v_{AB} = +V_{dc}$, as demonstrated in Fig. 7(i). (2) Similarly, if outputting the reactive power, $S_{2,3}$, $S_{1,4}$ and $S_{5\text{-}7}$ are switched at a high frequency in region 4 of Fig. 6(b). When $S_{2,3}$ are in ON-state, i_g flows through S_2 and S_3 to achieve $v_{AB} = -V_{dc}$, as shown in Fig. 7(g), i.e., the blue dotted arrow line. Otherwise, as it is shown in Fig. 7(c), i_g (the red solid arrow line) will flow through S_6 and D_5 to achieve $v_{AB} = 0$. Then, i_g flows through D_2 and D_3 to obtain $v_{AB} = -V_{dc}$ during the deadtime, as

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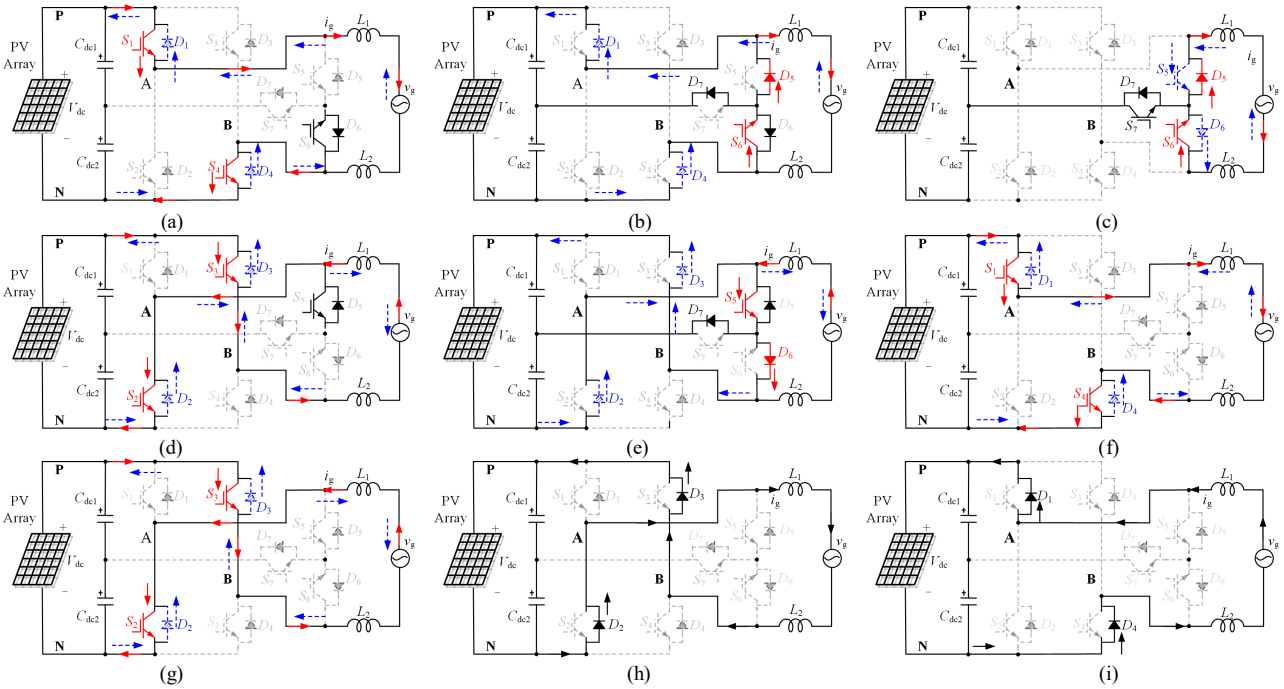

Fig. 7. Operation modes of the proposed modulation scheme for the AVC-HERIC inverter.

shown in Fig. 7(h). Therefore, to compensate the MPWL, $S_{1,4}$ should be operated to reach $v_{AB} = +V_{dc}$, where i_g (the red solid line) flows through S_1 and S_4, as shown in Fig. 7(f).

Region 5: This region in Fig. 6(a) and (b) has the same operation mode, which can provide a bidirectional current path when generating the zero voltage. More specifically, S_5 is ON, $S_{2,3}$ and $S_{6,7}$ are switched at a high frequency. The grid current i_g flows through S_2 and S_3 to obtain $v_{AB} = -V_{dc}$ being shown as the red solid arrow line in Fig. 7(d) to output active power. When generating the reactive power, i_g flows through D_1 and D_4 also to obtain $v_{AB} = +V_{dc}$, which is shown as the blue dotted arrow line in Fig. 7(d). To provide shoot-through protection, the deadtime is inserted between operation mode changes. During the deadtime, i_g flows through S_5 and D_6 to obtain $v_{AB} = 0$ to generate the active power, being shown as the red solid arrow line in Fig. 7(e). On the contrary, when generating the reactive power, i_g (i.e., the blue dotted arrow line in Fig. 7(e)) flows through D_2 and D_3 to achieve $v_{AB} = -V_{dc}$.

Therefore, a simple modulation strategy with the ability of free current commutation is demonstrated above. In the regions requiring the MPWL, the proposed modulation method obtains the desired output by generating three voltage levels (i.e., $+V_{dc}$, $-V_{dc}$ and 0) according to the operation modes. The following will further explain the deadtime insertion principle and the compensation strategy for the MPWL effect. The control strategy will also be presented.

A. Deadtime insertion principle

Obviously, the deadtime is employed in all operation modes. As it has been mentioned previously, the distortions of the output voltages during the deadtime are different for the active power and reactive power generation. When $v_{ref}i_g > 0$, the grid current path in the deadtime is like that in the freewheeling period. While $v_{ref}i_g < 0$, the current path during the deadtime is the same as in the conduction time. Thus, to eliminate the deadtime distortion, the compensation methods applied in regions 2 and 5 are: (1) when generating active power, the deadtime ratio u_d is included in the freewheeling time $1-u$, as shown in Fig. 6(a); (2) when outputting reactive power, the deadtime u_d should be included in the conduction time u, as illustrated in Fig. 6(b). Owing to the compensation for the MPWL distortion, which covers the deadtime effect in regions 1, 3, 4 and 6, the deadtime is only inserted in regions 2 and 5 in the proposed method.

B. Compensation for the MPWL

The analysis of the current distortion caused by the MPWL has been elaborated in the above. To compensate for the distortion, in the proposed method, $u = u + u_M$ is defined when $u < u_M$. Notably, the MPWL duration is usually two times longer than the deadtime for safety, which is determined by the turn-off transition interval time of the power device (i.e., $u_d > t_{off}$) [31] Next, the proposed compensation principle is illustrated referring to Fig. 8.

In the region of $v_{ref}i_g > 0$ shown in Fig. 8(a), the reverse desired voltage is generated during the deadtime period to compensate for the MPWL distortion. Thus, the output voltage can be obtained as

$$\begin{aligned} v_{AB}\big|_{T_s} &= (u+u_M)\times(\pm V_{dc}) + (1-u-2u_M)\times 0 + u_M(\mp V_{dc}) \\ &= \pm u V_{dc} \end{aligned} \tag{14}$$

By contrast, as shown in Fig. 8(b), the compensation method that can generate three voltage levels is adopted in the region of $v_{ref}i_g < 0$. In this case, the output voltage can be given as

$$\begin{aligned} v_{AB}\big|_{T_s} &= u_M\times(\pm V_{dc}) + (u+u_M)\times(\pm V_{dc}) + 2.5u_M\times(\mp V_{dc}) \\ &\quad + 0.5u_M\times(\pm V_{dc}) + (1-u-5u_M)\times 0 \\ &= \pm u V_{dc} \end{aligned} \tag{15}$$

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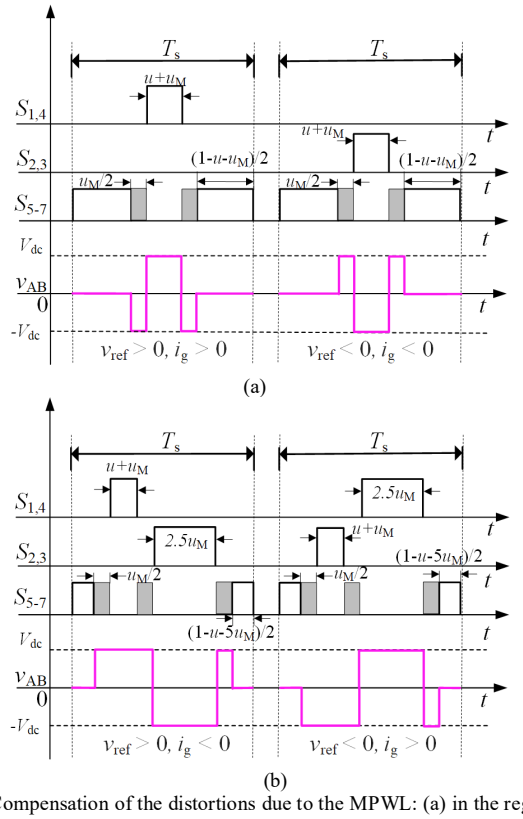

Fig. 8. Compensation of the distortions due to the MPWL: (a) in the region of $v_{ref} i_g > 0$ and (b) in the region of $v_{ref} i_g < 0$.

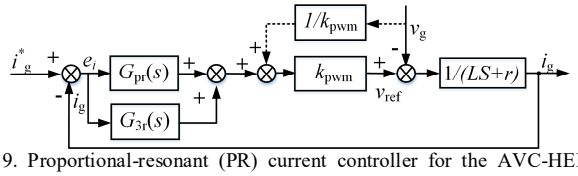

Fig. 9. Proportional-resonant (PR) current controller for the AVC-HERIC inverter, where a third-order resonant controller is adopted to mitigate the harmonics.

Consequently, the current distortion induced by the MPWL can be compensated effectively with the above modifications. In addition, the proposed compensation, which generates three voltage levels, will induce more ripple currents than the UP-PWM (i.e., generating two voltage levels 0 and $\pm V_{dc}$), but has less ripple currents than the BP-PWM (i.e., outputting two voltage levels $+V_{dc}$ and $-V_{dc}$). The ripple currents are relatively small and negligible, and thus, the compensation method will not significantly affect the current distortion.

C. Control of the AVC-HERIC inverter

Generally, the control of the grid-connected PV inverter consists of two cascaded loops (i.e., the outer voltage/power control loop and the inner current loop). Since only the modulation method of the AVC-HERIC inverter is discussed, the input PV voltage adopts a commercial DC power supply in this paper. Thus, only a current control loop is considered, as it is shown in Fig. 9. Firstly, the grid current i_g should be synchronized with the grid voltage v_g through a Phase-Locked Loop (PLL) [32]. A Proportional-Resonant (PR) controller $G_{pr}(s)$ is then adopted considering its good performance in terms of the zero-error tracking of AC variables in the fundamental-frequency [33]. Additionally, to compensate for the harmonics considering non-linear or induced by the grid voltage background distortion, Multi-resonant controllers can be employed to selectively reject harmonics of interest [34]. Furthermore, to simplify the parameters tuning process while maintaining the current quality, only one resonant controller, i.e., $G_{3r}(s)$ for the third-order harmonic component, is connected in parallel for the current loop in this paper, as it is shown in Fig. 9. Additionally, k_{pwm} is the inverter gain, which is equal to V_{dc} in this paper. In this way, the AVC-HERIC inverter with an L filter can still achieve a relatively low total harmonic distortion (THD) [35].

Furthermore, under the same hardware conditions (i.e., the same power semiconduction devices), the conduction losses are always positively related to the system loading. However, due to the difference in the voltage stress for power devices, the modulation methods will affect the switching losses [36], [37]. Notably, the proposed modulation strategy brings the same switching losses as the conventional the UP-PWM method in regions 2 and 5 in Fig. 6 due to the generation of two voltage levels (i.e., $+V_{dc}$ and 0 in region 2, and $-V_{dc}$ and 0 in region 5). Furthermore, the switching power losses generated during the MPWL is slightly larger than that under UP-PWM method because there are three voltage levels in one switching cycle (i.e., $+V_{dc}$, 0 and $-V_{dc}$) [29]. However, the MPWL regions (i.e., $\omega t \in (-\theta_M, \theta_M)$) have relatively short durations, and thus, the power losses due to the MPWL compensation are insignificant compared to the switching losses. Thus, the conversion efficiency of the AVC-HERIC with the proposed modulation scheme is close to that with the UP-PWM scheme. In a word, the proposed modulation scheme can achieve flexible reactive power injection, while maintaining good power quality and high efficiency.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Referring to Fig. 1, simulations and experimental tests have been performed on an AVC-HERIC inverter system to verify the proposed modulation scheme and the above analysis. Due to the lab availability, Infineon IKW3N65EL5 IGBT power devices with fixed deadtime, i.e., $t_d = 1.25\ \mu s$, are selected in the experiments. Additionally, a constant switching frequency is adopted ($f_s = 20$ kHz). This means that the deadtime ratio is $u_d = 1.25\ \mu s \times 20$ kHz $= 0.025$, and the MPWL u_M is equal to $2 \times u_d = 0.05$. Other parameters of the grid-connected inverter system are listed in Table I.

A. Simulation results

Fig. 10 shows the performance of the proposed modulation strategy at the unity power factor and at a non-unity power factor (i.e., $\cos\varphi = \pm 0.9$). Here, it is defined that $\cos\varphi = +0.9$ when i_g is leading v_g, while $\cos\varphi = -0.9$ when i_g is lagging v_g. It can be seen in Fig. 10 that the inverter output voltage v_{AB} is changed between 0 and V_{dc} (or between 0 and $-V_{dc}$). This is similar to the inverter with the UP-PWM. Thus, the AVC-HERIC inverter with the proposed modulation strategy has the same switching losses as that with the conventional UP-PWM. Only during the MPWL regions, v_{AB} has three voltage levels (i.e., $+V_{dc}$, $-V_{dc}$, and 0) at one switching cycle, which may induce additional power losses. This is in agreement with the previous discussions.

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TABLE I
PARAMETERS OF THE AVC-HERIC INVERTER SYSTEM.

Symbol	Parameter	Value
P	Output power	3 kW
V_{dc}	DC link voltage	360 V
V_g	Grid voltage (RMS)	220 V
f	Grid frequency	50 Hz
$C_{dc1} = C_{dc2}$	Input DC capacitor	5600 μF
$L_1 = L_2$	Filter inductor	1 mH
f_s	Switching frequency	20 kHz
t_d	Deadtime	1.25 μs

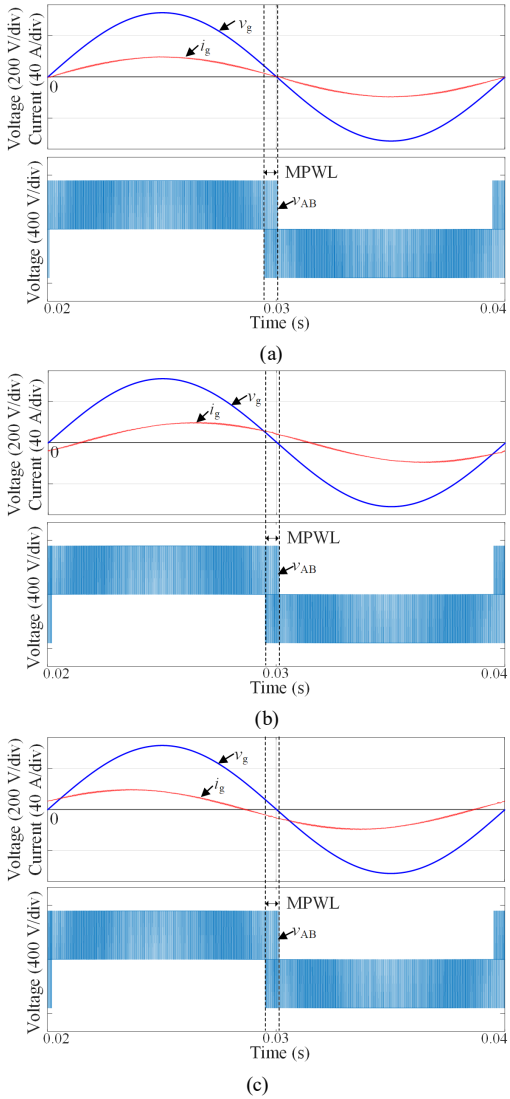

Fig. 10. Simulation results of the AVC-HERIC inverter system with the proposed modulation scheme: (a) at unity power factor, (b) at cosφ = +0.9, and (c) at cosφ = –0.9, where cosφ is the power factor.

Furthermore, the compensation strategy for the MPWL is demonstrated in Fig. 11, where v_{ref} is the desired output voltage and i_{ref} is the reference output current. It is illustrated in Fig. 11 that the compensation voltage is generated during the deadtime when the inverter generates active power (i.e., when $v_{ref} > 0$, $i_g > 0$ and $v_{ref} < 0$, $i_g < 0$). While generating reactive power (i.e., when $v_{ref} > 0$, $i_g < 0$ and $v_{ref} < 0$, $i_g > 0$), the opposite diagonal switches of the full-bridge part should be in ON-state for a suitable period to achieve a compensation voltage. For example, when $v_{ref} > 0$, $i_g < 0$, the desired voltage for compensation (i.e., $-V_{dc}$) is generated by switching-on S_2 and S_3. The results of the compensation strategy for the MPWL coincide with the analysis in Fig. 8. It is worth noting that the compensation operation modes are changed by judging the polarity of v_{ref}, instead of the grid voltage v_g. When comparing the results in Fig. 11(a) and (b), it is known that the grid current i_g follows well the desired current reference i_{ref} and it contains negligible ripple currents.

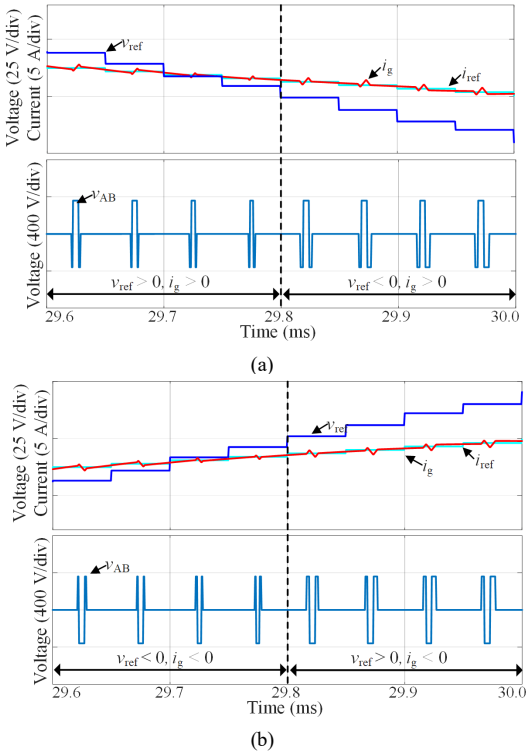

Fig. 11. Simulations of compensation operation during MPWL: (a) at $i_g > 0$, and (b) at $i_g < 0$.

In all, the simulation results in Figs. 10 and 11 have demonstrated that the AVC-HERIC inverter with the proposed modulation strategy can eliminate the effect of the MPWL. As a result, the AVC-HERIC can achieve a good performance in terms of power quality.

In addition, Fig. 12 compares the performance of the proposed modulation considering the dead-time and the MPWL effects with the proposed compensation strategy. The impact of the MPWL is zoomed-in in Fig. 12(a)-(c). As it can be observed in Fig. 12(a)-(c) that the grid current has large distortions that are caused by the deadtime and the MPWL at different power factors. The THD levels of the grid current i_g are 1.94%, 2.86%, and 2.89% at cosφ = 0, +0.9, and –0.9, correspondingly. As mentioned in previous discussions, only the MPWL distortion exists when operating at unity power factor, which is confirmed in Fig. 12(a). Moreover, the distortion caused by the deadtime will increase, when the power factor becomes larger (absorbing or sending reactive power). Thus, the current distortion is the smallest at unity

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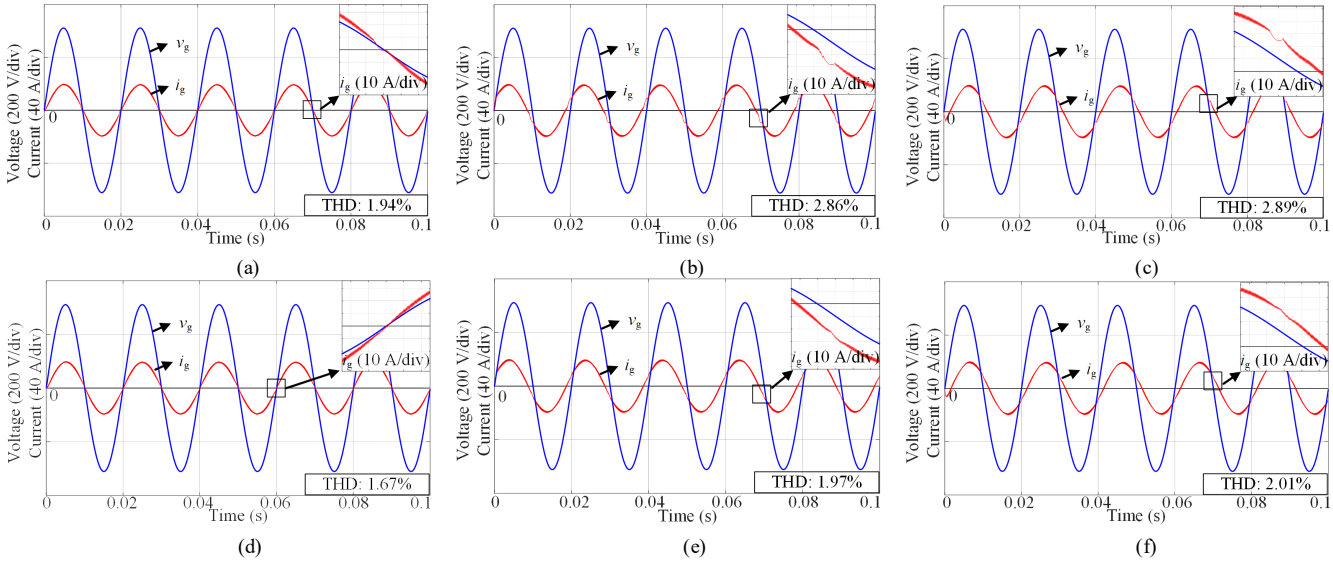

Fig. 12. Performance comparison of the AVC-HERIC inverter system with different modulation strategies: (a) under the effect of the deadtime and MPWL at unity power factor, (b) under the effect of the deadtime and MPWL at cosφ = +0.9, (c) under the effect of the deadtime and MPWL at cosφ = –0.9, (d) with the proposed compensation at unity power factor, (e) with the proposed compensation at cosφ = +0.9, and (f) with the proposed compensation at cosφ = –0.9, where cosφ is the power factor.

power factor with the conventional modulation providing a bidirectional current path. Through compensating for the distortions, the performance of the grid-connected AVC-HERIC system is improved, as shown in Fig. 12(d)-(f). In those cases, the resultant THD values of the grid current i_g are decreased to 1.67%, 1.97%, and 2.01% at cosφ = 0, +0.9, and –0.9, correspondingly. Furthermore, the zoomed-in views during the MPWL operation have illustrated that the compensation strategy can eliminate the distortions to a large extent. It is also confirmed that the switchover of the operation modes will increase the ripples of the grid current i_g, as shown in Fig. 12. In this case, the proposed compensation strategy generates three voltage levels (i.e., 0, $+V_{dc}$ and $-V_{dc}$), and the desired output inverter voltage is $uV_{dc} = (u + u_M)V_{dc} - u_M V_{dc}$ or $(u + 2.5u_M)V_{dc} - 2.5u_M V_{dc}$, where the duty cycle u during the MPWL operation and u_M are small. It means that the ripple currents make a minor contribution to the current distortion when compared to the BP-PWM method, where the desired output inverter voltage is $uV_{dc} = V_{dc}(1 + u)/2 - V_{dc}(1 - u)/2$. In all, the simulation results have confirmed that the power quality can be ensured for the AVC-HERIC inverter with the proposed modulation method.

B. Experimental results

To further verify the effectiveness of the proposed modulation strategy, a 3-kW AVC-HERIC inverter was built up. The setup is shown in Fig. 13. In the experiments, a Chroma PV simulator is adopted as the input power supply and a Chroma programmable AC grid simulator is employed at the AC side. Control systems and modulation algorithms are implemented on a TI TMS320F28335 floating-point digital signal processor (DSP) and the driver signals of the IGBT are generated by Altera EP2C8T144C8N FPGA systems. The measuring instruments include a Tektronix DPO3014 Oscilloscope and an HIOKI 3390 Power Analyzer (power quality and efficiency). For comparison, the parameters of the

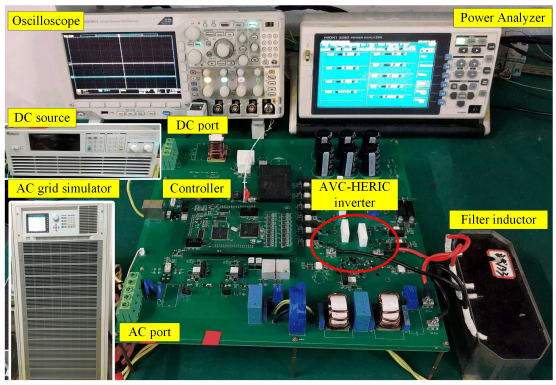

Fig. 13. Experimental setup of a 3-kW single-phase grid-connected AVC-HERIC inverter system.

experimental system are the same as those in the simulations, which are listed in Table I.

The performance of the AVC-HERIC inverter with the proposed modulation strategy is demonstrated in Fig. 14. It can be observed in Fig. 14 that the experimental results agree well with the simulation results shown in Fig. 10. Different power factors (i.e., cosφ = 0, +0.9, and –0.9) for the AVC-HERIC are also experimentally tested. The results shown in Fig. 14 further confirm that a bidirectional current path is provided by the proposed modulation scheme in regions 2 and 5 of Fig. 6, where the differential-mode voltage v_{AB} switches between 0 and $+V_{dc}$ (or 0 and $-V_{dc}$). In addition, the proposed compensation strategy is employed during the MPWL periods, where the inverter outputs three voltage levels (i.e., 0, $+V_{dc}$, and $-V_{dc}$). This is the same as the discussions and the experimental tests.

The compensation effects with the proposed method are detailed in Fig. 15, with $i_g > 0$ and $i_g < 0$, which is in a close agreement with the results in Fig. 11. The AVC-HERIC inverter can generate the compensation voltages as depicted in Fig. 8 in different conditions to improve the MPWL impact

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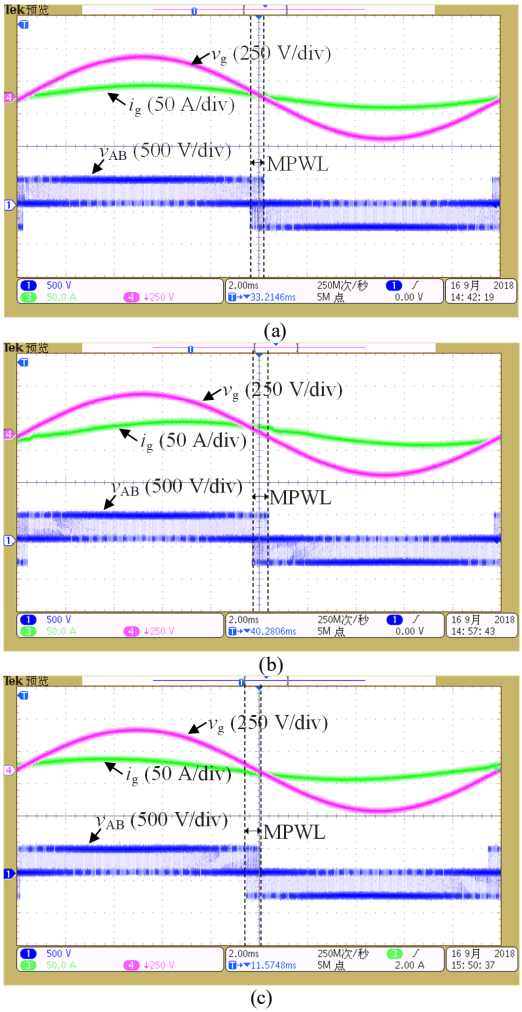

Fig. 14. Experimental results of the AVC-HERIC inverter system with the proposed modulation scheme (time: 2 ms/div): (a) at the unity power factor, (b) at cos φ = +0.9, and (c) at cos φ = –0.9, where cos φ is the power factor

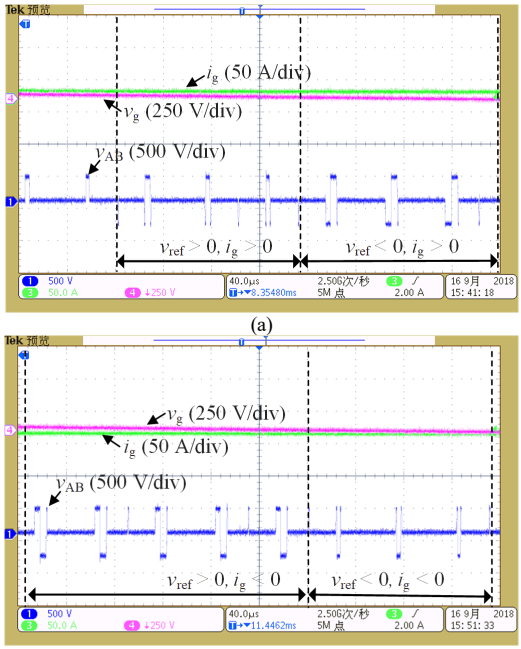

Fig. 15. Experimental results of the AVC-HERIC inverter system with the compensation operation during the MPWL (time: 40 μs /div): (a) $i_g > 0$ and (b) $i_g < 0$.

and thus to improve the power quality. It is also easy to find in Fig. 15 that there are certain negligible pulses of the inverter output voltage v_{AB}, which are generated during the operation mode transitions. In practice, to prevent the confusion during operation when the polarity detection of the grid current i_g occurs in the current zero-crossing point, the deadtime should be inserted between the mode changes. The experimental results in Fig. 15 have verified that the proposed modulation strategy can enable the AVC-HERIC to provide reactive power, and the compensation method can mitigate the deadtime and the MPWL distortions to a large extent.

The performance of the 3-kW AVC-HERIC inverter prototype is further shown in Fig. 16. In this case, the distortions induced by the deadtime and the MPWL are demonstrated in Fig. 16(a)-(c) under various power factors, i.e., cosφ = 0, +0.9, and –0.9. Similarly, the grid currents are zoomed-in for better visualization. The THD levels of the grid current i_g in those cases are measured by the HIOKI 3390 Power Analyzer, and the results are also shown in Fig. 16. The corresponding THD level of the grid current i_g is 2.14%, 3.05%, and 3.03% for the AVC-HERIC inverter, when the conventional method is adopted. It is known from the results that the current distortion when only generating active power is smaller than that when providing reactive power. The reason is that the quality of the grid current i_g with the conventional modulation is affected by the deadtime and the MPWL at non-unity power factor operation. To improve the power quality, the proposed compensation strategy is then applied to the AVC-HERIC system, and the results are shown in Fig. 16(d)-(f) with the power factor being cosφ = 0, +0.9, and –0.9, correspondingly. The measured THD levels of the grid current i_g in those three cases are 1.73%, 2.17%, and 2.15%. Additionally, the zoomed-in views of Fig. 16 have also confirmed that the power quality of the grid current i_g, i.e., Fig. 16(d)-(f) with the proposed method, is better than that shown in Fig 16(a)-(c) without the compensation strategy. The experimental results in Fig. 16 show consistency with the simulation results in Fig. 12. The above simulations and experimental tests have verified that the AVC-HERIC inverter can achieve a good output power quality with the proposed modulation method, where the deadtime and the MPWL distortions are effectively compensated.

To further verify the proposed modulation method, more results of the THD levels with different modulation methods have been compared in Table II. The modulation methods include the UP-PWM method, the BP-PWM, the proposed modulation method under the effect of the deadtime and the MPWL and the proposed modulation method with the compensation strategy. Conclusions can then be drawn from the benchmarking in Table II and the above simulation and experimental results: 1) the UP-PWM method has a relatively high efficiency, but it cannot provide reactive power injection; 2) the BP-PWM has reactive power injection capability, and yet, the performances in terms of the power efficiency and power quality are not satisfactory; 3) the modulation under the effect of the deadtime and the MPWL will generate distortions,

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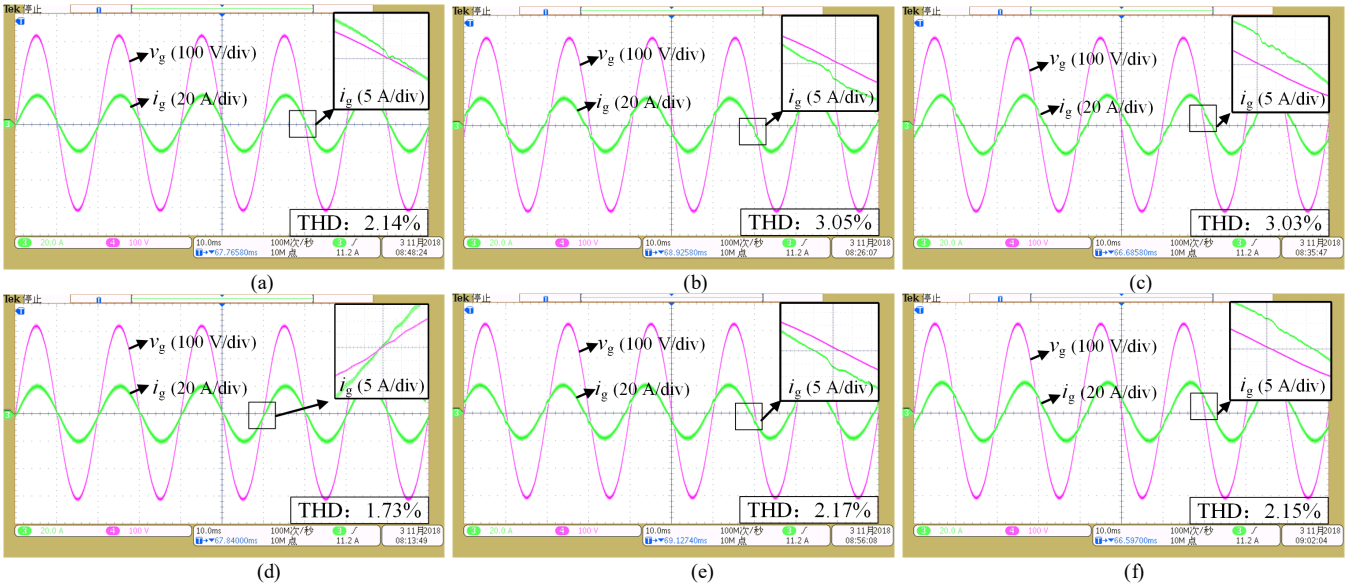

Fig. 16. Experimental results of the 3-kW single-phase grid-connected AVC-HERIC inverter system with different modulation methods (time: 10 ms/div): (a) under the effect of the deadtime and MPWL at the unity power factor, (b) under the effect of the deadtime and MPWL at cosφ = +0.9, (c) under the effect of the deadtime and MPWL at cosφ = –0.9, (d) with the proposed compensation at the unity power factor, (e) with the proposed compensation at cosφ = +0.9, and (f) with the proposed compensation at cosφ = –0.9, where cosφ is the power factor.

TABLE II
COMPARISON OF THD LEVELS WITH DIFFERENT MODULATION METHODS.

Modulation \ cosφ	1	+0.9	-0.9
Simulation results			
UP-PWM	1.90%	~	~
BP-PWM	2.51%	3.05%	3.12%
Modulation with deadtime and MPWL effect	1.94%	2.86%	2.89%
Proposed modulation	1.67%	1.97%	2.01%
Experimental results			
UP-PWM	2.15%	~	~
BP-PWM	2.90%	3.33%	3.43%
Modulation with deadtime and MPWL effect	2.14%	3.05%	3.03%
Proposed modulation	1.73%	2.17%	2.15%

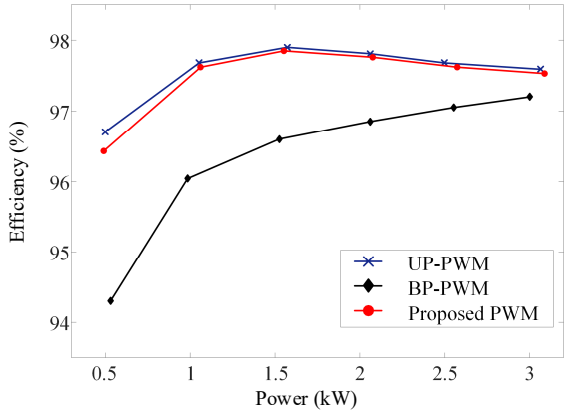

Fig. 17. Measured efficiency of the AVC-HERIC inverter with different modulation schemes.

affecting the power quality; 4) the proposed modulation with the compensation strategy for the AVC-HERIC can achieve a good power quality and flexible reactive power injection.

Additionally, Fig. 17 shows the experimental efficiencies of the AVC-HERIC inverter system with various modulation strategies. The HIOKI 3390 Power Analyzer is adopted to measure the input power and output power of the AVC-HERIC inverter system at the DC and AC side in a way that the conversion efficiency is calculated. That is, the power losses of the AVC-HERIC inverter system include the losses of the power devices, and the losses of the filter inductors. The results in Fig. 17 confirm that the efficiency of the AVC-HERIC inverter system with the proposed scheme is almost the same as the conventional UP-PWM under different power levels. However, a higher efficiency is achieved when the proposed modulation scheme is adopted, when comparing to the conventional BP-PWM, as shown in Fig. 17. This is in agreement with the analysis given in Section III.C, where it has been shown that the proposed modulation method can maintain high efficiency as the convention UP-PWM.

In all, the above simulations and experimental tests have verified the effectiveness of the proposed modulation strategy in terms of deadtime and MPWL distortions compensation, high efficiency, good power quality, and also provide reactive power injection. It is thus a promising modulation strategy for the AVC-HERIC to be applied in grid-friendly PV systems.

V. CONCLUSION

In this paper, a simple modulation method for the AVC-HERIC with the compensation for the deadtime and the MPWL distortions has been proposed. The proposed method can achieve a bidirectional current path to inject reactive power while maintaining high efficiency compared to the UP-PWM. The deadtime compensation in the proposed method

was implemented by judging the polarity of the output power. That is, the deadtime was inserted in different periods (i.e., only active power, it was inserted in freewheeling periods; otherwise, it was inserted in conduction periods). This eliminates the voltage distortions caused by the deadtime. Furthermore, regarding the MPWL issue, the proposed scheme can also effectively compensate for the MPWL distortion. This is achieved by generating three voltage levels according to different operation modes. Simulation and experimental results have verified the effectiveness of the proposed simple modulation strategy in terms of enhanced power quality, improved efficiency, and more importantly, flexible reactive power controllability only through modifying the modulation scheme. It should be pointed out that the proposed method can be extended to other transformerless inverters with minor algorithm modifications.

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