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Leakage Current Reduction of Three-phase Z-Source Three-level Four-Leg Inverter for Transformerless PV system

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***Abstract*—Leakage current reduction is one of the important issues for transformerless PV systems. Many interesting solutions have been reported to reduce the leakage current for three-phase PV inverters. However, most of them are limited to two-level inverters. Moreover, there is a potential risk of the over-current phenomenon. In order to solve the problem, a Z-source three-level four-leg inverter with a new modulation strategy is proposed in this paper. Firstly, the mathematical modeling of the three-level four-leg Z-source inverter for leakage current reduction is established for the first time. Secondly, a new carrier-based modulation strategy is proposed by utilizing the effective large, medium, small, and zero vectors, instead of the invalid vectors, to achieve the constant common mode voltage, as well as the leakage current suppression. Finally, the proposed solution is carried out on the TI (Texas Instruments) TMS320F28335 DSP + Xilinx XC3400 FPGA digital control hardware platform. The experimental results verify the effectiveness of the proposed solution.**

***Index Terms*—Z source inverter, three-level inverter, four-leg inverter, leakage current.**

I. INTRODUCTION

Due to environmental pollution and government incentives in renewable energy system, the PV power system has received widespread attention in recent years 1-5]. A transformer usually is installed for the conventional PV inverter to connect the grid. However, it increases the cost, size and decreases the efficiency of the overall system. That is the reason why the transformerless PV inverters are popular in recent years [6-7].

For integrating the transformerless PV inverter into grid, one of the most important issues is the leakage current attenuation. Generally, the solutions to the leakage current reduction can be classified into two groups: one is the single-phase solutions, and the other is the three-phase ones.

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Many interesting single-phase topologies have been presented to reduce the leakage current [8-15], such as H5, oH5, H6, Heric, and so on. They can reduce the leakage current effectively. However, there is a limitation of them due to the well-known twice fundamental frequency power oscillation. And an electrolytic capacitor has to be used, which is more prone to failure and the whole system's reliability is degraded [16-18]. Aside from that, integrating the single-phase inverter into grid leads to the power oscillations and unbalanced problems. Therefore, the VDE 4105 standard specifies that the capacity of single-phase grid-connected inverter should be less than 4.6 kVA, which limits the system capacity. On the other hand, there is no power oscillation and unbalanced problems in three-phase grid connected PV systems. For the leakage current attenuation in three phase three legs inverter, one possible solution is to use only the medium and zero vectors [19-21]. But the modulation index for those solutions is limited [22]. To increase the range of the modulation index, the large, medium and zero vectors are used to reduce the leakage current [23]. However, the common-mode voltage is not constant in [23], and the leakage current can reduced to a certain level. Another solution uses the modulation strategy with Boolean logic function for the leakage current attenuation [24-26]. It should be noted that the abovementioned solution is for three-leg inverters. For dealing with the unbalanced situation, the four-leg inverters are typically used [27-29]. For the leakage current reduction in three-phase four-leg inverter, a new algorithm is proposed in [30] to reduce the common-mode voltage. It has the advantage of high DC link utilization, low harmonic distortion, less switching losses. However, the common-mode voltage is not constant, and the leakage current is not well attenuated. In order to ensure the common-mode voltage constant, the method in [31] uses the six switching vectors to synthesize the reference vector, while another interesting solution with a common-mode filter is proposed in [32] to reduce the common-mode voltage. Besides, a new modulation strategy with Boolean logic function is proposed to achieve the constant common-mode voltage for the leakage current reduction [33]. However, the modulation index is also limited. Furthermore, it should be noted that most of

above-mentioned solutions are based on the voltage source inverters, and it is inherently a step-down converter. Besides, in practice, the PV panel voltage depends on many factors such as the weather conditions, which will cause the f output voltage variation of PV panel. In this case, a boost converter has to be installed to the low-voltage PV panel [34]. Due to the existence of the additional switch in the boost converter, the additional gating driver is needed. Also, both the switch and diode of the boost converter need the heat sink [35]. Moreover, there is a potential risk of overcurrent, which reduces the system reliability. In order to solve the problem, the Z-source inverter (ZSI), originally proposed by Peng, can be used [36]. The amplitude of the output voltages can reach high levels due to the step-up characteristic. Both the risk of the over-current phenomenon and additional boost switch circuit are avoided [37].

For leakage current reduction in ZSI, Bradaschia, *et al*, presented an improved modulation strategy for three-phase Z-source inverter [38], where three odd or even vectors were used to eliminate the high-frequency common mode voltage, so the leakage current can be well attenuated. However, the modulation index is limited. And it was pointed out in [39] that there is an undesired operation mode in [38], which could lead the system to instability. To solve this issue, a ZSI-S topology with two additional insulated gate bipolar transistors (IGBTs) is proposed in [39]. Meanwhile, to reduce the leakage currents, an improved PWM technique is presented to achieve the constant common-mode voltage. The undesired operation modes are avoided. However, two additional switches are needed, and the complexity of the control as well as the switching loss is increased. Another modified ZSI is presented in [40]. Only one additional switch is needed, compared with the conventional ZSI. And the leakage currents can be well suppressed due to dual-grounding structure. Besides, there are many other papers are devoted to reduce the leakage current for the Z-source and qZ-source inverter [41-44]. However, the above-mentioned topologies and modulation methods for ZSI are limited to three-leg inverters. For the leakage current reduction in the three phase four-leg Z source inverter, an interesting solution is presented in [45] to achieve the constant common mode voltage. However, it is limited to two-level inverter in nature. So far, the analysis and solution regarding the leakage current reduction of three-level four-leg Z-source inverter has not been explored in literature. That's the motivation of the paper to deal with this unsolved problem. The importance of the three-level four-leg Z-source inverter is listed as follows.

(1) For the three-level inverter, it has the advantage over two-level inverter in both high-power and low-power systems [46]. It can decrease the total harmonic distortion, voltage stress of dv/dt on switches, electromagnetic interference and improve the output waveform quality [47].

(2) For the four-leg inverter, it has the advantage over three-leg inverter for unbalanced deal capability and more flexible to achieve optimal objective [30].

(3) For the Z source inverter, it can avoid the potential risk of the over-current phenomenon of inverter and needn't install the additional boost converter [34].

The contributions of the paper are shown as follows. Firstly, the leakage current behavior for three-level four-leg Z-source inverter is established with a mathematical description. Secondly, a new carrier-based modulation strategy is proposed by utilizing the effective large, medium, small, and zero vectors, instead of the invalid vectors, to achieve the constant common mode voltage, as well as the leakage current suppression. Finally, the experimental evaluation of the conventional and proposed solution is presented.

The rest of the paper is organized as follows. Section II presents the operation principle of the Z-source three-level four-leg inverter. The common mode behavior is discussed in Section III. The conventional and proposed modulation strategies are presented in Section IV. The simulation and experimental results are provided in Section V. Finally, the conclusion is reached in Section VI.

II. Operation Principle

Fig.1 illustrates the schematic diagram of the three-phase Z-source three-level four-leg inverter for the transformerless PV system, where C_{PV} is the parasitic capacitance between the PV panel and ground. V_{dc} is the DC input voltage. The leakage current will arise on condition as the parasitic capacitor voltage or common mode voltage varies in a high-frequency way.

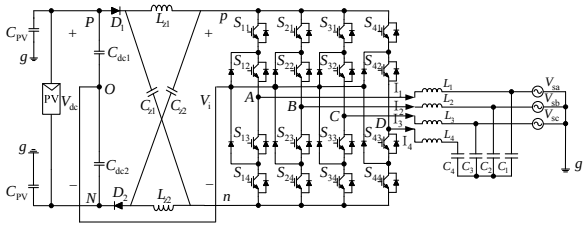

Fig.1 Schematic diagram of Z-source three-level four-leg inverter.

The system operation mode can be divided into two states. One is the shoot-through state, and the other is the non-shoot-through state. For simplicity of analysis, the capacitance C_{Z1} and C_{Z2} of the Z-source network are equal, and the capacitor voltage can be expressed as $V_{Cz1} = V_{Cz2} = V_{Cz}$. The inductance $L_{Z1} = L_{Z2}$, and inductor voltage can be expressed as $V_{Lz1} = V_{Lz2} = V_{Lz}$.

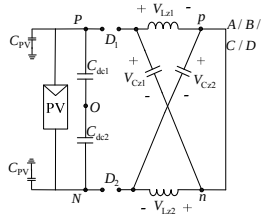

Fig.2 Shoot-through state.

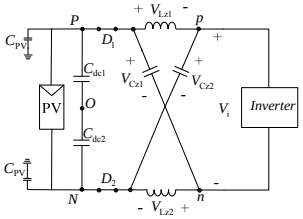

Fig.3 Non-shoot-through state.

During shoot-through states, the diodes of D_1 and D_2 are

reversely off, as shown in Fig. 2. During non-shoot-through state, as shown in Fig.3, the input voltage can be expressed as follows.

$$V_{Lz} = V_{dc} - V_{Cz} \tag{1}$$

$$V_i = V_{Cz} - V_{Lz} = 2V_{Cz} - V_{dc} \tag{2}$$

where V_{dc} is the DC input voltage and V_i is the Z-source voltage, respectively. It is defined that T_0 is the shoot-through period, T_1 is the non-shoot-through period, d is the shoot-through duty cycle. The average voltage of the inductor over one switching period of T_s should be zero, and thus

$$\frac{T_0 V_{Cz} + T_1 (V_{dc} - V_{Cz})}{T_s} = 0 \tag{3}$$

The voltage values of V_i , V_{Cz} and V_{Lz} can be derived from (1) to (3) as follows.

$$V_i = V_{Cz} - V_{Lz} = 2V_{Cz} - V_{dc} = \frac{T}{T_1 - T_0} V_{dc} = \frac{1}{1-2d} \cdot V_{dc} \tag{4}$$

$$V_{Cz} = B_B \cdot V_{dc} \tag{5}$$

$$V_{Lz} = (1 - B_B) \cdot V_{dc} \tag{6}$$

where $B_B = (1-d)/(1-2d)$.

III. Common Mode Behavior Analysis

In this section, the common mode behavior of Z-source three-level four-leg inverter is discussed. Firstly, the relationship between the switching states and output voltages is shown in (7), where S_{ij} =1 if the switch is on, while S_{ij} =0 if the switch is off. $X = A, B, C, D.\ i = 1,2,3,4.\ j = 1,2,3,4.$

$$V_{XN} = \begin{cases} B_B V_{dc} & S_X = 2 \quad S_{i1}=1,\ S_{i2}=1,\ S_{i3}=0,\ S_{i4}=0 \\ V_{dc}/2 & S_X = 1 \quad S_{i1}=0,\ S_{i2}=1,\ S_{i3}=1,\ S_{i4}=0 \\ (1-B_B)V_{dc} & S_X = 0 \quad S_{i1}=0,\ S_{i2}=0,\ S_{i3}=1,\ S_{i4}=1 \end{cases} \tag{7}$$

The phase voltage to ground for each leg of V_{Ag} , V_{Bg} , V_{Cg} and V_{Dg} can be derived from Fig. 1 as follows.

$$V_{Ag} = (B_B S_{11} S_{12} + \frac{S_{12} S_{13}}{2} + (1-B_B) S_{13} S_{14}) V_{dc} + (S_{11} S_{12} + S_{12} S_{13} + S_{13} S_{14}) V_{Ng} \tag{8}$$

$$V_{Bg} = (B_B S_{21} S_{22} + \frac{S_{22} S_{23}}{2} + (1-B_B) S_{23} S_{24}) V_{dc} + (S_{21} S_{22} + S_{22} S_{23} + S_{23} S_{24}) V_{Ng} \tag{9}$$

$$V_{Cg} = (B_B S_{31} S_{32} + \frac{S_{32} S_{33}}{2} + (1-B_B) S_{33} S_{34}) V_{dc} + (S_{31} S_{32} + S_{32} S_{33} + S_{33} S_{34}) V_{Ng} \tag{10}$$

$$V_{Dg} = (B_B S_{41} S_{42} + \frac{S_{42} S_{43}}{2} + (1-B_B) S_{43} S_{44}) V_{dc} + (S_{41} S_{42} + S_{42} S_{43} + S_{43} S_{44}) V_{Ng} \tag{11}$$

$$V_{Ag} = I_1 \cdot sL_1 + V_{sa} \tag{12}$$

$$V_{Bg} = I_2 \cdot sL_2 + V_{sb} \tag{13}$$

$$V_{Cg} = I_3 \cdot sL_3 + V_{sc} \tag{14}$$

$$V_{Dg} = I_4 sL_4 + \frac{2}{3} V_{c4} \tag{15}$$

The V_{Ng} is the voltage between positive (P) or negative (N) dc bus and ground point 'g'. V_{Lz} is the voltage across inductor of Z source network. V_{sa}, V_{sb} and V_{sc} are the grid voltages. L_1, L_2 , L_3 and L_4 are the filter inductances and L_1= L_2 = L_3= L_4=L. I_1, I_2 , I_3 and I_4 are the current shown in Fig.1. And s is the Laplace operator.

From the (8)-(11), it can be calculated as

$$V_{Ag} + V_{Bg} + V_{Cg} + V_{Dg} = aV_{dc} + bV_{Ng} \tag{16}$$

Where

$$\begin{aligned} a = {} & B_B S_{11} S_{12} + S_{12} S_{13}/2 + (1-B_B) S_{13} S_{14} + B_B S_{21} S_{22} \\ & + S_{22} S_{23}/2 + (1-B_B) S_{23} S_{24} + B_B S_{31} S_{32} + S_{32} S_{33}/2 \\ & + (1-B_B) S_{33} S_{34} + B_B S_{41} S_{42} + S_{42} S_{43}/2 + (1-B_B) S_{43} S_{44} \end{aligned}$$

$$\begin{aligned} b = {} & S_{11} S_{12} + S_{12} S_{13} + S_{13} S_{14} + S_{21} S_{22} + S_{22} S_{23} + S_{23} S_{24} \\ & + S_{31} S_{32} + S_{32} S_{33} + S_{33} S_{34} + S_{41} S_{42} + S_{42} S_{43} + S_{43} S_{44} \end{aligned}$$

From (12)-(15), it can be derived as follows.

$$\begin{aligned} V_{Ag} + V_{Bg} + V_{Cg} + V_{Dg} &= (I_1 + I_2 + I_3 + I_4) sL + 2V_{c4}/3 \\ &= V_{Ng} s^2 C_{PV} L + 2V_{c4}/3 \end{aligned} \tag{17}$$

The parasitic capacitor voltage V_{Ng} can be derived from (16)-(17) as follows

$$V_{Ng} = (aV_{dc} - \frac{2}{3} V_{c4}) / (s^2 L C_{pv} - b) \tag{18}$$

From Fig.1, V_{c4} can be calculated as

$$V_{c4} = (6 - 3s^2 L_Z C_{PV} - \frac{3}{2} s^2 L C_{pv}) V_{Ng} - 6V_{CM} + 6V_{LZ} \tag{19}$$

Substituting (19) in (18), the parasitic capacitor voltage V_{Ng} can be rewritten as follows.

$$V_{Ng} = \frac{1}{4 - 2s^2 L_Z C_{PV} - b} [aV_{dc} - 4V_{Lz} + 4V_{CM}] \tag{20}$$

From (20), it can be observed that the parasitic capacitor voltage V_{Ng} is mainly dependent on the following factors such as V_{dc} , V_{LZ} , V_{CM} , a and b. In general, the dc voltage of V_{dc} is constant. From (6), it can be seen that V_{LZ} depends only on the shoot-through duty cycle. When shoot-through duty cycle is constant, V_{LZ} would be constant. The coefficients a and b are depended on the switching states shown in (16) and can be constant through proper control of the switching states, it will be analyzed in the section IV. Therefore, V_{Ng} is mainly determined by the V_{CM}.

The common mode voltage V_{CM} for both shoot-through and non-shoot-through states are defined as

$$V_{CM} = (V_{AN} + V_{BN} + V_{CN} + V_{DN})/4 \tag{21}$$

In case of the shoot-through state, the diode is off, and the common mode circuit is switched off. The each phase voltages are

$$V_{AN} = V_{BN} = V_{CN} = V_{DN} = V_{Cz} + V_{D2} \tag{22}$$

The inductor voltage, capacitor voltage and diode voltage in the shoot-through state are

$$V_{Lz} = V_{Cz} = B_B \cdot V_{dc} \tag{23}$$

$$V_{D2} = \frac{V_{dc} - 2V_{Cz}}{2} = \frac{(1-2B_B)}{2} V_{dc} \tag{24}$$

With (21), (22), (23) and (24), the common mode voltage in the shoot-through state can be obtained.

$$V_{CM} = (V_{AN} + V_{BN} + V_{CN} + V_{DN})/4 = V_{dc}/2 \tag{25}$$

According to the above analysis, the V_{CM} is constant in the shoot-through state. Therefore, if the common mode voltage is also constant under non-shoot-through states, the leakage current will be effectively suppressed. Thus, it is important to find a modulation strategy to make the V_{CM} constant in the non-shoot-through, which will be discussed in the next section.

IV. Modulation Strategy

For three-level inverters, the modulation can be classified into two categories. One is the carrier-based modulation, and the other is the space vector modulation. In practice, the space vector modulation needs complex implementation procedure, where it is necessary to calculate the dwell time and select the sector of vector. Therefore the carried-based modulation is utilized in this paper.

A. Conventional Modulation

For the three-level four-leg inverter, the conventional way to generate the gating signal is the dual-carrier modulation strategy, as shown in Fig.4, where the gating signals of first three legs are generated by comparing the modulation wave with the carrier. While the gating signal of the fourth leg is generated by comparing the zero sequence component with the triangular carrier. Finally, the shoot-through signal is inserted in the each carrier cycle, as shown in Fig. 5.

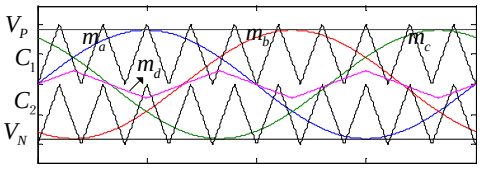

Fig.4 Conventional modulation.

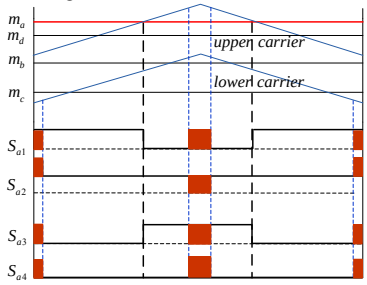

Fig.5 Switching states within a cycle for A phase.

However, as shown in Fig.6, the common mode voltage is time-varying with the conventional modulation. Therefore, the leakage current is not able to be suppressed due to the high frequency common mode voltage.

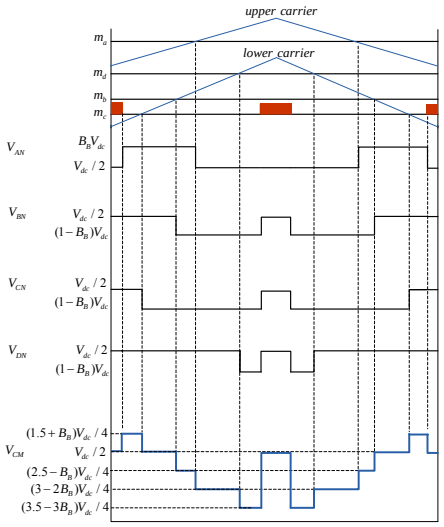

Fig.6 Phase voltage and V_{CM} with conventional modulation.

B. Proposed Modulation Strategy

As discussed in the previous section, the parasitic capacitor voltage in the conventional solution is time-varying in a high-frequency way. So the leakage current is not able to be effectively reduced. In order to solve it, a new modulation strategy is proposed by coordinating the switching states to achieve the constant common mode voltage. According to the aforementioned analysis in Section III, the common mode voltage is constant at $V_{dc}/2$ in case of shoot-through state. So the common mode voltage would be constant all the time on condition that it is controlled to be $V_{dc}/2$ in non-shoot-through state, which can be achieved by Eq. (26).

$$S_A + S_B + S_C + S_D = 4 \tag{26}$$

In order to simplify the implementation, the switching states of the fourth leg can be controlled in the following way.

$$S_D = 4 - S_A - S_B - S_C \tag{27}$$

In this way, the switching states and corresponding common mode voltage are listed in the Tab I.

TABLE I
COMMON MODE VOLTAGE AND SWITCHING STATES

	Vector		S_A	S_B	S_C	S_D	a	b	V_{CM}
non-shoot through state	Effective vectors	large vector	0	2	0	2	2	4	$V_{dc}/2$
			2	2	0	0	2	4	$V_{dc}/2$
			2	0	0	2	2	4	$V_{dc}/2$
			2	0	2	0	2	4	$V_{dc}/2$
			0	0	2	2	2	4	$V_{dc}/2$
			0	2	2	0	2	4	$V_{dc}/2$
		medium vector	1	2	0	1	2	4	$V_{dc}/2$
			2	1	0	1	2	4	$V_{dc}/2$
			2	0	1	1	2	4	$V_{dc}/2$
			1	0	2	1	2	4	$V_{dc}/2$
			0	1	2	1	2	4	$V_{dc}/2$
			0	2	1	1	2	4	$V_{dc}/2$
		small vector	1	2	1	0	2	4	$V_{dc}/2$
			1	1	0	2	2	4	$V_{dc}/2$
			2	1	1	0	2	4	$V_{dc}/2$
			1	0	1	2	2	4	$V_{dc}/2$

			1	1	2	0	2	4	$V_{dc}/2$
			0	1	1	2	2	4	$V_{dc}/2$
		zero vector	1	1	1	1	2	4	$V_{dc}/2$
	Invalid vectors	-	0	1	0	X	-	-	-
			2	2	1	X	-	-	-
			1	2	2	X	-	-	-
			1	0	0	X	-	-	-
			0	0	1	X	-	-	-
			2	1	2	X	-	-	-
			0	0	0	X	-	-	-
			2	2	2	X	-	-	-

Tab. I shows all the possible non-shoot-through states, the common mode voltages and the values of 'a', 'b' when the (27) is adopted, where X indicates that this state does not exist. In Tab I, there are two groups of vectors for non-shoot through state. One is the effective vector, and the other is the invalid vector. For the latter, Eq. (26) and (27) can't be satisfied no matter what the switching state of the fourth leg is. Besides, from (7), it can be observed that the S_D is limited, where the values of S_D only are three states: 0, 1, 2. Therefore, the states similar with $S_A = S_B = S_C = 0$, $S_D = 4$ and $S_A = S_B = S_C = 2$, S_D=-2 do not exist because of $S_D \notin 0,1,2$. On the other hand, for the effective vectors such as the large, medium, small and zero vector, there is always a switching state S_D of the fourth leg, which meet the requirement of (26) and (27). Fig.7 shows the effective vector distribution, which is for understanding the switching states distribution.

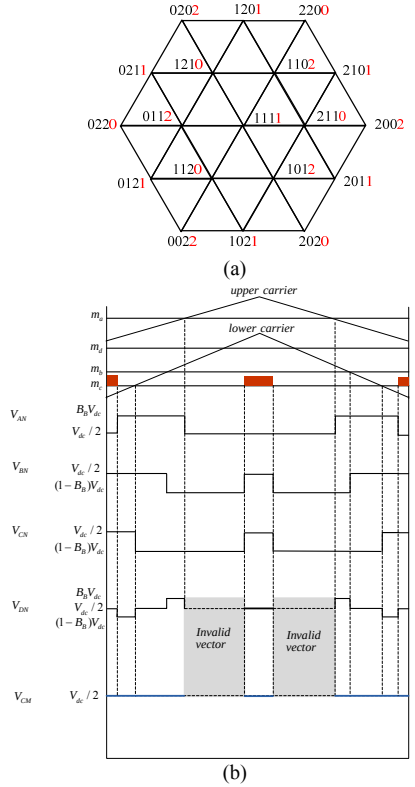

Fig.7 proposed method. (a) diagram of the effective vector distribution, and (b) Switching states and common mode voltage.

The common mode voltage of those effective vectors in Fig.7 is analyzed as follows. Take the 2101 as an example, the corresponding switching states are S_{11}=1, S_{12}=1, S_{13}=0, S_{14}=0, S_{21}=0, S_{22}=1, S_{23}=1 S_{24}=0, S_{31}=0, S_{32}=0, S_{33}=1, S_{34}=1, S_{41}=0, S_{42}=1, S_{43}=1, S_{44}=0. At this time, from the Eq.(7), V_{AN} , V_{BN}, V_{CN} and V_{DN} are B_BV_{dc}, $V_{dc}/2$, $(1\text{-}B_B)V_{dc}$ and $V_{dc}/2$, respectively. Then by (21), the common mode voltage V_{CM} can be calculated as $V_{CM}= V_{AN} + V_{BN}+ V_{CN} + V_{DN} =(B_BV_{dc}+ V_{dc}/2+(1\text{-}B_B)V_{dc}+ V_{dc}/2)/4= V_{dc}/2$. Similarly, the common mode voltages V_{CM} of other effective vectors in Fig. 7 are also $V_{dc}/2$. Therefore, the V_{CM} is constant when the equation (27) is adopted in non-shoot-through state. It is worth noting that, unlike the conventional method where only the medium and zero vectors are used to eliminate the high-frequency common mode voltage, the proposed solution uses all the effective vectors, that is, the large, medium, small, and zero vectors to control the common mode voltage constant. Compared Fig. 6 with Fig. 7 (b), it can be observed that there are 24 turn-on losses and turn-off losses in a carrier cycle for the traditional solution. While there are 26 turn-on losses and turn-off losses in a carrier cycle for the proposed solution. That is, there are two more turn-on losses and turn-off losses for the proposed solution than the traditional scheme in a carrier cycle. Although the number of switching for proposed solution is slightly increased than the traditional scheme, both the leakage current and the THD of grid current are reduced. Moreover, with the development of wide band gap semiconductor device, the switching loss can be further reduced. Therefore, it is an attractive solution. For the coefficients *a* and *b*, take the effective vectors 2101 as example, from (7), the corresponding switching states are S_{11}=1, S_{12}=1, S_{13}=0, S_{14}=0, S_{21}=0, S_{22}=1, S_{23}=1 S_{24}=0, S_{31}=0, S_{32}=0, S_{33}=1, S_{34}=1, S_{41}=0, S_{42}=1, S_{43}=1, S_{44}=0. As defined by (16), the coefficients *a* and *b* are 2 and 4, respectively. In a similar way, the coefficients *a* and *b* are calculated as 2 and 4 in other effective vectors. Therefore, *a* and *b* are also constant when the effective vectors in Table I and Fig. 7 are used.

In summary, because both the V_{CM} and coefficients *a*, *b* are constant, therefore, from (20), the parasitic capacitor voltage V_{Ng} is constant in the proposed solution. Fig. 8 shows the block diagram of the hardware implementation and control unit part.

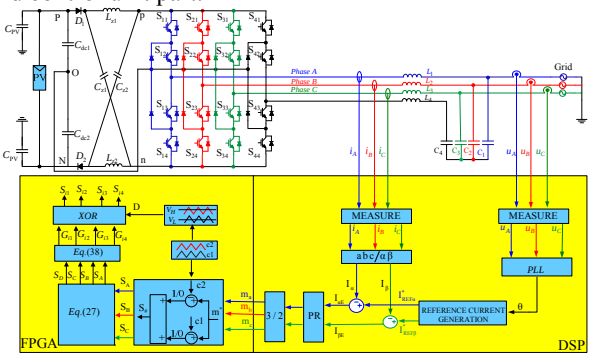

Fig. 8 Block diagram for implementation.

The grid voltages are measured by the transducers LV 28-P, and then through a PLL to generate the angle for the reference current. The transducer LA 55-P are used to measure the current, which is subtracted by the reference current. The error is regulated by the proportional-resonant (PR) controller and the inverse-Clarke transformation. And then the modulation wave m_a, m_b and m_c can be obtained. These control algorithms are implemented by a TMS320F28335 DSP control board, Considering that the switching state of the fourth leg S_D is generated by S_A, S_B, S_C, the logical operation is implemented by a Xilinx XC3400 FPGA.

In the Xilinx XC3400 FPGA, the logical signals S_{1a}, S_{2a}, S_{1b}, S_{2b}, S_{1c}, S_{2c} are obtained by compared the modulation wave m_a, m_b , m_c with the carriers c1, c2. When m_a is greater than c1, S_{1a} is 1, otherwise S_{1a} is 0. When m_a is greater than the carrier c2, S_{2a} is 1, otherwise S_{2a} is 0. In the Similar way, S_{1b}, S_{2b}, S_{1c}, S_{2c} can be obtained. Then S_A, S_B, S_C are calculated by $S_A = S_{1a}+S_{2a}$, $S_B = S_{1b}+S_{2b}$, $S_C = S_{1c}+S_{2c}$. S_D can be obtained by (27). And then the effective vectors are obtained by eliminating the invalid vectors. The 16 logical signals G_{11}-G_{44} are obtained by (38), where X = A, B, C, D. i =1, 2, 3, 4 . For example, when the S_A is 2, at this time, G_{11}, G_{12}, G_{13}, G_{14} are 1, 1, 0 and 0, respectively. Finally, the gating signals are generated by the 16 logical signals and shoot-through signals. V_H and V_L are the signals that control the shoot-through duty cycle.

$$\begin{cases} S_X = 2 & G_{i1}=1,\ G_{i2}=1,\ G_{i3}=0,\ G_{i4}=0 \\ S_X = 1 & G_{i1}=0,\ G_{i2}=1,\ G_{i3}=1,\ G_{i4}=0 \\ S_X = 0 & G_{i1}=0,\ G_{i2}=0,\ S_{i3}=1,\ G_{i4}=1 \end{cases} \quad (38)$$

V. Simulation and Experimental Results

A Simulation results

The time-domain test of conventional and proposed solutions is carried out in the Matlab/Simulink environment. The simulation parameters are listed in the Tab II, where the dc bus voltage is 470V. The capacitance and inductance of the Z-source network are 940uF and 3mH, respectively. The line-line voltage effective value of the grid is 380V/50Hz. The rated current is 10A. The switching frequency is 10 kHz. The output filter inductor is 7 mH. The parasitic capacitor is 300 nF, and the shoot-through duty cycle is 0.2.

TABLE II
Simulation and Experimental Parameters

Parameter	Simulation value	Experimental value
dc bus voltage V_{dc}	470V	120V
Capacitance of Z-source V_{Cz}	940 μH	940 μH
inductance of Z-source V_{Lz}	3 mH	3 mH
line-line voltage V_{AB}	380V/50Hz	98V/50Hz
rated current of grid	10A	8A
Filter inductance L	7mH	5mH
Filter capacitor C	9.4μF	9.4μF
parasitic capacitor C_{pv}	300nF	300nF
shoot-through duty cycle D	0.2	0.2
switching frequency f	10 kHz	10 kHz

Fig.9 shows the simulation results of the conventional solution. It observed that the output voltage of Z source network is in according to the theoretical analysis in section II. The line-line voltage shown in Fig.9 (b) is five-level, while output current shown in Fig.9 (c) is sinusoidal. The THD of grid current in traditional schemes is 4.61%. Fig9 (d) shows that the common mode voltage varies during one switching period, as predicted in Fig. 6. Accordingly, there are high-frequency components in the parasitic capacitor voltage shown in Fig.9 (e). Therefore, the leakage current can't be effectively suppressed, as shown in Fig.9 (f), where the peak and rms values are 880mA and 410mA, respectively. It is far beyond 300mA, which can't meet VDE-0126-1-1 standard.

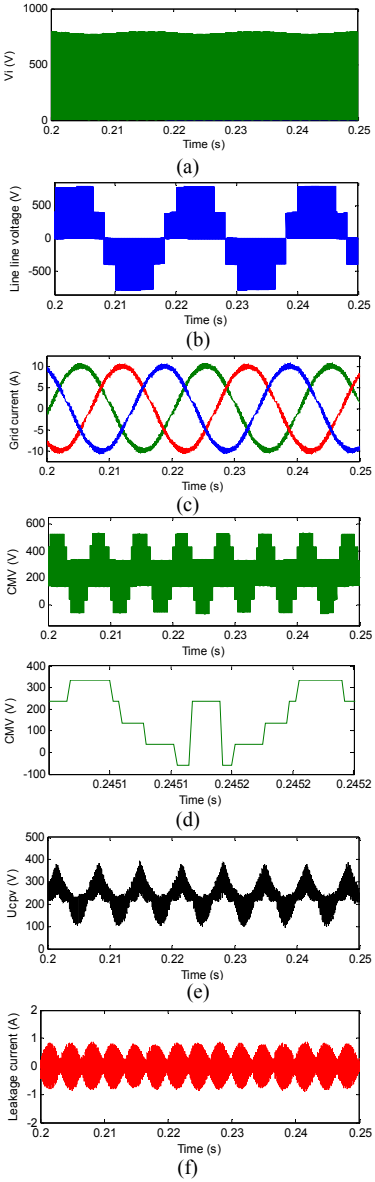

Fig.9 Simulation results of conventional solution.(a) Z-source output voltage V_i, (b) Line-line voltage, (c) Grid current, (d) Common mode voltage (CMV), (e) Parasitic capacitor voltage U_{cpv} , and (f) Leakage current.

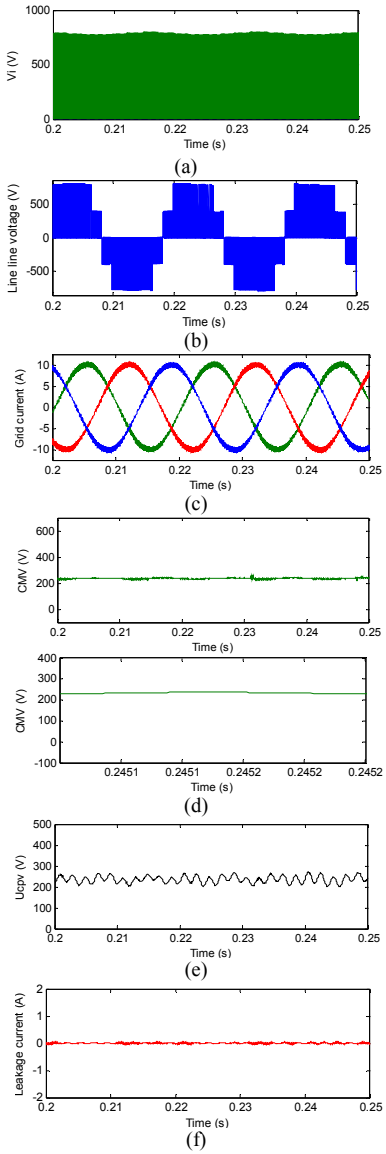

Fig.10 Simulation results of proposed solution.(a) Z-source output voltage V_i, (b) Line-line voltage, (c) Grid current, (d) Common mode voltage (CMV), (e) Parasitic capacitor voltage U_{cpv} , and (f) Leakage current.

Fig.10 shows the simulation results for the proposed solution. As predicted by (4), the output voltage of Z source network is 780V in the non-shoot-through state. The grid current is sinusoidal, and its THD is 4.38%.On the other hand, the common mode voltage is constant, and the parasitic capacitor voltage is free of high-frequency components. Therefore, the leakage current is significantly reduced as shown in Fig.10 (f), where the peak and rms values are 54mA and 17mA, respectively. It is well below 300mA, which complies with the VDE-0126-1-1.

The leakage current curve of simulation results with different parasitic capacitances for both the conventional and proposed modulations are shown in Fig. 11. The detailed data is listed in Tab. III, where I_{CM} is the leakage current, C_{pv} is the parasitic capacitance. From Fig. 10 and Tab. III, it can be observed the leakage current can be well attenuated with the proposed solution in case of different parasitic capacitances.

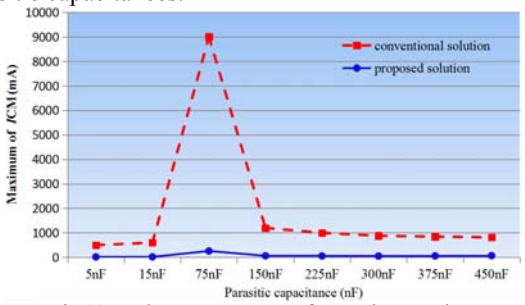

Fig.11 Leakage current curve for maximum value.

TABLE III
LEAKAGE CURRENT UNDER DIFFERENT PARASITIC CAPACITANCE

C_{pv}	maximum value of I_{CM}	
	conventional solution	Proposed solution
5nF	500mA	18mA
15nF	600mA	20mA
75nF	9000mA	260mA
150nF	1200mA	63mA
225nF	1000mA	57mA
300nF	880mA	54mA
375nF	848mA	58mA
450nF	815mA	70mA

B Experimental results

This section will present the experimental evaluation of the conventional and proposed solutions. The control algorithm is implemented in a TI (Texas Instruments) TMS320F28335 DSP plus Xilinx XC3S400 FPGA digital platform. The details are shown in Fig.8. The down-scaled system parameters are listed in the Tab II, where the dc bus voltage is 120 V. The grid voltage is 98/50Hz. The rated current is 8A. The rated power is 1kW. The switching frequency is 10 kHz. The capacitance and inductance of the Z-source network are 940uF and 3mH, respectively. The output filter inductor is 5 mH. The parasitic capacitor is 300 nF, and shoot-through duty cycle is 0.2.

Fig.12 shows the experimental results with traditional solution. Fig.12 (a) and Fig.12 (b) are the output voltage waveform of the Z source network and DC voltage, which shows the output voltage V_i of the Z source network is consistent with the theoretical analysis in the section II. Grid current and line-line voltage waveform are shown in Fig.12 (c) and Fig.12 (d), where the THD of grid current is 6.01%. The line-line voltage is five-level. Fig.12 (e) and Fig.12 (f) show the common mode characteristics and leakage current waveforms. On the other hand, the common mode voltage, as well as parasitic capacitor voltage is time-varying. Consequently, the leakage current is high as shown in Fig.12 (f), where the RMS and maximum value of the leakage current are 425mA and 251mA, respectively. It fails to comply with the VDE standard.

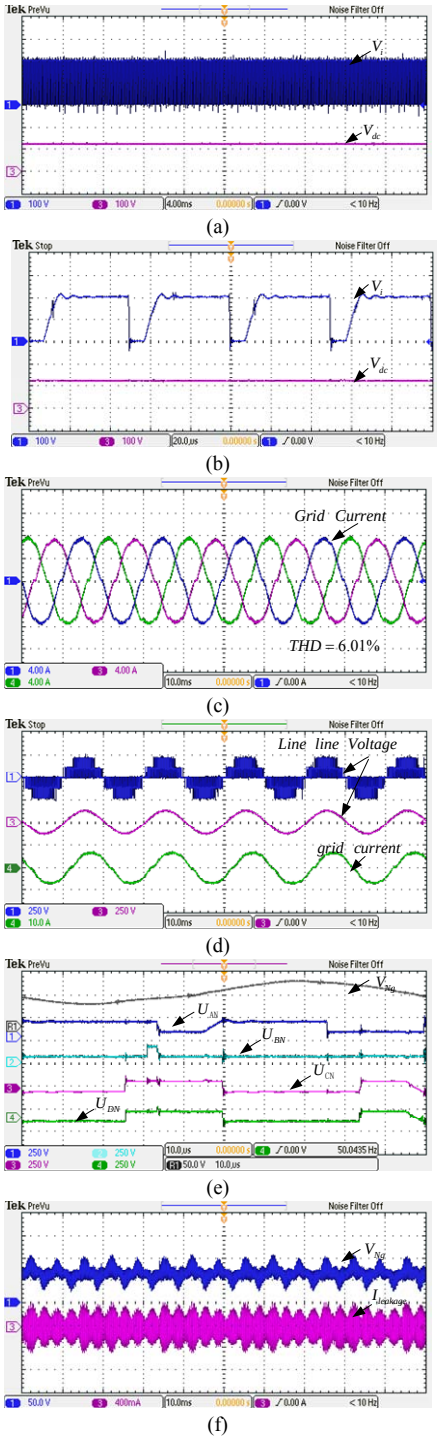

Fig.12 Experimental results with traditional solution. (a) (b) output voltage of the Z source network and DC voltage, (c) output current, (d) line-line voltage and output current, (e) Parasitic capacitor voltage and U_{AN}, U_{BN}, U_{CN},U_{DN}, and (f) Parasitic capacitor voltage and leakage current.

Fig.13 shows the experimental results with proposed solution. The grid current is sinusoidal, where the THD of grid current is 2.84%. On the other hand, with the proposed solution, the common mode voltage is constant, and the parasitic capacitor voltage is free of high-frequency component. Therefore, the leakage current is well suppressed. The maximum value and rms value of leakage current are 102mA and 28mA, respectively, which meets the VDE 0126-01-01 standard.

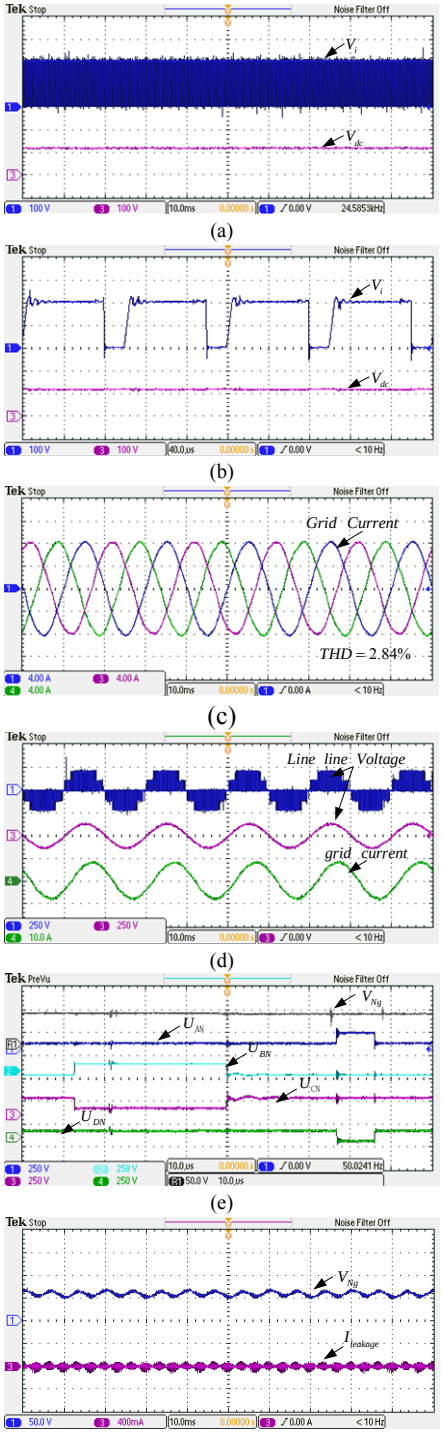

Fig.13 Experimental results with proposed solution. (a) (b) output voltage of the Z source network and DC voltage, (c) output current, (d)

line-line voltage and output current, (e) Parasitic capacitor voltage and U_{AN}, U_{BN}, U_{CN},U_{DN}, and (f) Parasitic capacitor voltage and leakage current.

VI. Brief Comparison

This section will present the brief comparison of the existing solutions to Z-source inverter for the leakage current reduction, where *m* is modulation index.

TABLE IV

COMPARISON OF RECENT THREE PHASE Z-SOURCE INVERTER FOR LEAKAGE CURRENT SUPPRESSION

	Z Source network				leg number	modulation index	voltage level	Fault tolerance capability
	S	D	C	L				
ZSI-D [38]	0	2	2	2	3	0<=m<=2/3	2	no
ZSI-S [39]	2	0	2	2	3	0<=m<=2/3	2	no
ZSI [40]	1	0	6	6	3	0<=m<=2/sqrt(3)	2	no
Proposed solution	0	2	2	2	4	0<=m<=2/sqrt(3)	3	yes

As shown in Tab. IV, it can be observed that the ZSI-S in [39] and ZSI in [40] have more switches (S) than ZSI-D in [38] and proposed solution. The number of diodes (D), capacitors (C), inductors (L) of ZSI-D in [38] is the same as that of the proposed solution. But the modulation index of ZSI-D in [38] is smaller than that of the proposed solution. Aside from that, the existing solutions in [38], [39] and [40] are two-level topologies, while the proposed solution is three-level topology. Furthermore, only the proposed solution has unique features of fault tolerance deal capability, which cannot be achieved with existing solutions in [38], [39] and [40]. It should be noted that this paper mainly focuses on the leakage current reduction, and the relevant research of zero-sequence deal is ongoing, and a comprehensive analysis and test results would be reported in a future paper.

VII. Conclusion

This paper has presented the analysis and experimental verification of a new solution for the leakage current reduction of a Z-source three-level four-leg PV inverter. Different from the previous insights, our findings indicate the parasitic capacitor voltage is dependent on not only the common mode voltage, but also the switching states, more specifically, the coefficients of a and b in (16) and (20). And the conventional solution fails to eliminate the high-frequency components of the parasitic capacitor voltage, and thus the leakage current can not be well suppressed. On the other hand, with the proposed solution, the parasitic capacitor voltage is free of high- frequency component. Consequently, the leakage current is effectively reduced. Also, the proposed solution is easy to implement in practice. Therefore, it is attractive for Z-source three-level four-leg PV inverters.

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