Aalborg Universitet

AALBORG UNIVERSITY
DENMARK

Fault-tolerant Oriented Hierarchical Control and Configuration of Modular Multilevel Converter for Shipboard MVDC System

Hong, Lerong; Xu, Qianming; He, Zhixing; Ma, Fu Jun; Luo, An; Ge Guerrero, Josep M.

Published in:
IEEE Transactions on Industrial Informatics

DOI (link to publication from Publisher):
10.1109/TII.2018.2879981

Publication date:
2019

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Hong, L., Xu, Q., He, Z., Ma, F. J., Luo, A., & Ge Guerrero, J. M. (2019). Fault-tolerant Oriented Hierarchical Control and Configuration of Modular Multilevel Converter for Shipboard MVDC System. *IEEE Transactions on Industrial Informatics*, *15*(8), 4525 - 4535. https://doi.org/10.1109/TII.2018.2879981

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

? Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
? You may not further distribute the material or use it for any profit-making activity or commercial gain
? You may freely distribute the URL identifying the publication in the public portal ?

Take down policy
If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

Fault-tolerant Oriented Hierarchical Control and Configuration of Modular Multilevel Converter for Shipboard MVDC System

Lerong Hong, Qianming Xu, *Member*, *IEEE*, Zhixing He, *Member*, *IEEE*, Fujun Ma, *Member*, *IEEE*, An Luo, *Senior Member*, *IEEE*, and Josep M. Guerrero, *Fellow*, *IEEE*

***Abstract*—Medium-voltage DC (MVDC) distribution system is considered as the promising power architecture of future shipboard power system. Fault-tolerance ability is of great importance for power system on ships. In this paper, zonal DC-DC conversion system based on modular multilevel converter (MMC) and three-phase bridge rectifier are proposed with its hierarchical fault-tolerant scheme. The topology configurations of the front-end MMC with multi-winding medium frequency transformer (MFT) under normal and post-fault circumstances are presented. The reconfiguration scheme and fault-tolerant control strategy are also proposed to ride-through sub-module (SM) level fault, phase level fault and bus level fault. Based on the hierarchical fault-tolerant scheme, redundant configuration of the MMC sub-module is further analyzed with the hierarchical reliability modelling. The effectiveness of the proposed control strategy is verified by the experimental results.**

***Index Terms*—Shipboard power system, Medium voltage DC (MVDC), Modular multilevel converter (MMC), Fault-tolerance, Redundant configuration.**

I. Introduction

Medium-voltage DC (MVDC) distribution system is thought to be the promising power architecture of future shipboard power system [1-2]. With MVDC bus, high-speed gas turbine generation and renewable energy generation devices can be integrated together to achieve fuel-efficient operation.

In consideration of specific on-board working conditions, the critical challenges of MVDC distribution system are fault management, power density, etc. [3-5]. The power architecture of zonal electrical distribution system (ZEDS), shown in Fig. 1, is a representative solution to fault-tolerant and reconfigurable shipboard power system [6-8]. In each electrical zone, the service loads, organized to make zonal load centers are fed from both port-side and starboard-side dc buses to enhance survivability [8].

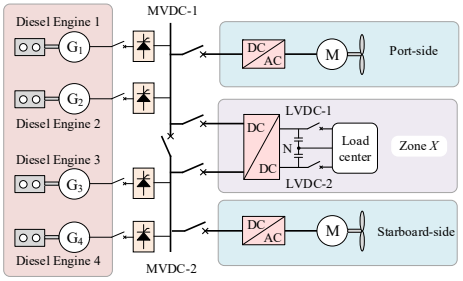

Fig. 1. Power architecture of shipboard zonal electrical distribution system.

In DC ZEDS, the interaction between the front-end MVDC bus and back-end low-voltage DC (LVDC) bus is usually governed by DC-DC converters, which provide fault management, galvanic isolation and voltage regulation [1][4][8]. Due to convenient maintenance and ease of power or voltage rating scaling, a modular design is more attractive for MV applications and there are several categories of isolated modular DC/DC converters: modular multilevel DC converter based on half-bridge (HB) or full-bridge (FB) and input-series output-parallel (ISOP) DC converter based on dual half bridge, dual active bridge (DAB), and series resonant converter (SRC) [9-15].

In [3], a MV resonant DC-DC converter based on single phase MMC with high-frequency transformer (HFT) is proposed. Isolated dual-MMC DC-DC converter with an MFT in the middle ac link is also designed in [4][11-13] for shipboard power system. In [13], a conventional three-phase MMC is used as the MVDC bus interface converter and a three-phase bridge PWM rectifier is connected to the MMC to form the back-end LVDC bus.

For high input-voltage and low output-voltage applications, ISOP DC converter is also a feasible choice [14-17]. Modeling and control of ISOP have been investigated in [15-16]. To disconnect fully from the MVDC bus, an improved ISOP type DC converter is proposed in [17] for MVDC power distribution application with the switched capacitor converter (like the arm of MMC) serving as the front-end interface of the ISOP.

Manuscript received July 7, 2018; revised September 26, 2018 and October 21, 2018; accepted October 30, 2018. Date of publication XX XX, 2018. This work was supported in part by the National Key R&D Program of China under Grant 2018YFB0904600 and in part by the National Natural Science Foundation of China under Grant 51807056. Paper no. TII-18-1761. (*Corresponding Author: Qianming Xu*)

L. Hong, Q. Xu, Z. He, F. Ma and A. Luo are with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail: hlr0908@163.com; hnuxqm@foxmail.com; hezhixingmail@163.com; mafujun2004@163.com; an_luo@126.com).

J. M. Guerrero is with the Department of Energy Technology, Aalborg University, 9220 Aalborg East, Denmark (e-mail: joz@et.aau.dk).

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

TABLE I
COMPARISON OF MMC-BASED DC CONVERTER AND SC-ISOP DC CONVERTER FOR MVDC APPLICATIONS

Item	MMC+PWM rectifier	SC-ISOP
Switch number	n*12, MVDC side 6*2(PWM*2), LVDC side	n*6, MVDC side n*4, LVDC side
Switch failure effect	SM bypassed (2 switches) with one switch failure	cell bypassed (10 switches, 1 HFT) with one switch failure
Control complexity	concentrated phase control for MMC; individual control for each PWM rectifier	independent control for SC; independent control for each DAB
Redundancy level	including SM, phase and LV bus level	only cell level
3-ph ac link access	yes	no
DC bus structure	monopolar-to-bipolar	monopolar
Industrial adoption	widespread adoption in industry	mature technology, already adopted

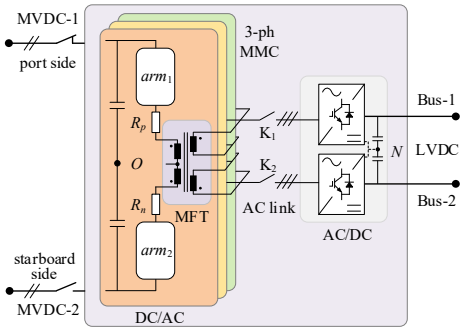

Fig. 2. MMC-based DC converter with four-winding MFT and dual LVDC bus.

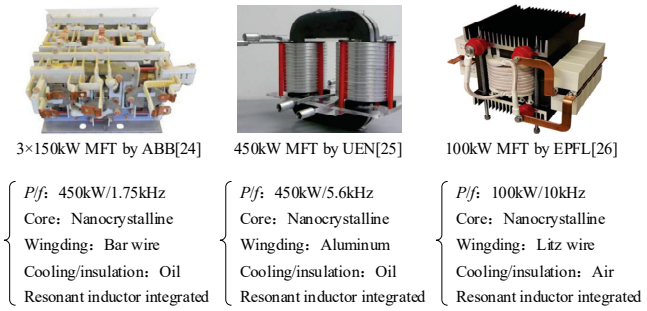

Fig. 3. Some existing MFT solutions by different companies and universities.

MMC-based DC converter and ISOP DAB are analyzed and compared in [9-10], and the resulting conclusion is that both of them are feasible topologies considering power density, survivability and reliability are of primary concerns in shipboard power system. ISOP-based dc-dc converters have higher power density and lower total device rating while MMC-based DC converters may have better energy storage ability and fault operation performance. Since numerous devices should be used in MMC and ISOP, the failure of submodule or cell is unavoidable. The mentioned DC-DC converters can achieve redundancy design to improve the reliability [9][10], which is important for on-board MVDC power distribution system because of the long maintenance cycle and harsh working conditions.

For the ISOP proposed in [17], each cell consists of one DAB (two H-bridges and one HFT) and one half-bridge based switched capacitor converter (SC). Both the DAB and SC should be healthy to maintain the normal operation of each cell. Meanwhile, when one switch fails, the whole cell should be bypassed so the impacts of switch failure on ISOP are more serious than that on MMC as shown in Table I. For MMC, only the faulty SM should be bypassed (or both the faulty SM and another one in the other arm of the same phase-leg) [18-21]. Hence, fault-tolerant capability of MMC is higher than ISOP to some extent. However, in practice, when the number of faulty SMs exceeds the designed tolerated number, the three-phase MMC usually should be disconnected or replaced with another backup MMC. Then the module utilization rate is low and the requirement of backup MMC means more space and investment, which are not economical for shipboard applications. Therefore, it is interesting to investigate the multidimensional fault-tolerant method to obtain the reliability as high as possible.

In view of the situation mentioned earlier, this work pro-poses a MMC-based DC converter as shown in Fig. 2 and its comparison results with the ISOP-based DC converter in [17] are shown in Table I [13][17][23]. In the MVDC side, the MMC is integrated with MFT to generate nearly constant three-phase ac power source [9][23]. In the LVDC side, two three-phase bridge converters with mutual stand-by are introduced to provide back-end dual LVDC bus, which has a bi-polar structure. In the middle ac link, the integrated trans-former can provide suitable voltage adaptation and galvanic isolation and merge the function of arm reactors into inherent leakage inductance with proper design of leakage inductance. Due to their multifunctional role, the design of MFT imposes certain challenges including inductance design, magnetic material selection, insulation coordination [24-25] and system optimization [26]. As illustrated in Fig. 3, some existing solutions of integrated MFT with different materials and structures, as well as novel model-based design optimization methodology have been proposed for power electronic transformer in [24-26].

Meanwhile, hierarchical redundant strategy and configuration scheme including SM-level, leg-level and LV bus level are designed to further improve the system fault-tolerant ability. With presented fault-tolerant control scheme, the MMC as zonal front-end interface can still provide three-phase ac power even though the SM or one phase-leg of MMC is failed. Moreover, reliability modeling of the MMC with proposed redundancy strategy is deduced to verify the effectiveness and help to determine suitable redundant configurations.

The paper is organized as follows: Section II presents the topology configuration and system modeling under normal and post-fault conditions. Section III proposes the hierarchical

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

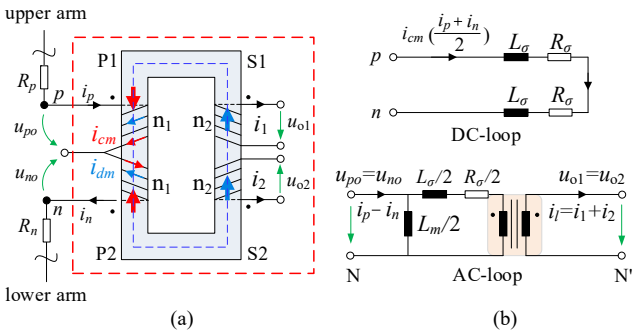

Fig. 4. Single-phase MFT. (a) Four-winding MFT. (b) Equivalent circuit.

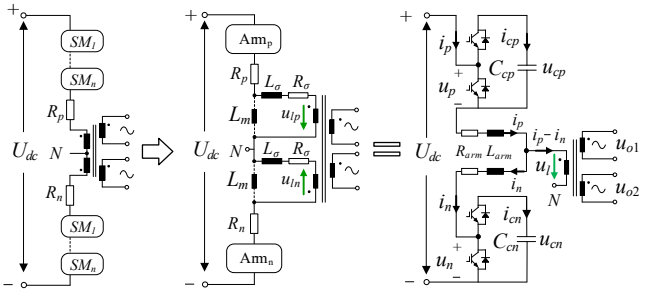

Fig. 5. MMC. (a) Topology of phase-leg. (b) Equivalent circuit.

fault-tolerant control scheme. Section IV gives the redundant configuration analysis of MMC with reliability consideration. Experimental results and the conclusion are presented in Sections V and Section VI, respectively.

II. Topology Configuration Under Normal and Post-Fault Conditions

A. Under normal operation

1) four-winding MFT

As illustrated in Fig. 2 and Fig. 4(a), the primary side of MFT is connected to the MMC and the upper arm current i_p and lower arm current i_n both flow through the primary windings. With the arm current decoupled into common and differential mode components, we have,

$$\begin{cases} i_p = i_{cm} + i_{dm} \\ i_n = i_{cm} - i_{dm} \end{cases} \tag{1}$$

In common current component case, for the same directions of common mode current i_{cm} but the opposite directions of upper and lower winding, the directions of the magnetomotive force for each other are opposite. In differential current case, the directions are the same. Hence, DC flux cancellation can be achieved and the problem of magnetic saturation of the ac transformer in [27] can be avoided in this arrangement.

Suppose the electrical parameters of the upper and lower windings of MFT are identical. The modeling of the MFT can be simplified as (2).

$$\begin{cases} L_{\sigma p} = L_{\sigma p1} = L_{\sigma p2}, L_{\sigma s} = L_{\sigma s1} = L_{\sigma s2} \\ R_{\sigma p} = R_{\sigma p1} = R_{\sigma p2}, R_{\sigma s} = R_{\sigma s1} = R_{\sigma s2} \\ L_\sigma = L_{\sigma p} + n^2 L_{\sigma s}/2, R_\sigma = R_{\sigma p} + n^2 R_{\sigma s}/2 \\ n_1 / n_2 = n, 2i_{dm} = i_p - i_n = (i_1 + i_2)/n \end{cases} \tag{2}$$

where $L_{\sigma p}$ and $R_{\sigma p}$ denote the leakage inductance and resistance of the primary windings while $L_{\sigma s}$ and $R_{\sigma s}$ denote that of the secondary windings. R_σ and L_σ are the equivalent leakage resistance and inductance, respectively. n_1 and n_2 denote winding turns and n is the turn ratio. i_1 and i_2 are the output ac current of the dual secondary windings.

Based on (2), the equivalent circuit can be obtained as Fig.4(b). It can be observed that the inherent leakage inductance of MFT could play the role of conventional arm reactors of MMC. Thus, proper design of leakage inductance offers the possibility of the removal of arm reactors. As presented in [24] and [26], the diameters and the spacing of the coils could be defined so as to reach the targeted value for the leakage inductance while withstanding the dielectric requirement and high leakage inductance value are easily reachable by HV winding interleaving and positioning.

2) three-phase MMC

Based on the MFT equivalent circuit in Fig. 4, topology and equivalent circuit of MMC leg integrated with four-winding MFT can be depicted in Fig. 5. Hence, conventional MMC modulation functions of upper arm (m_p) and lower arm (m_n) are also feasible.

$$\begin{cases} m_{pj} = 0.5 - 0.5k\sin(\omega t + x_j \frac{2}{3}\pi) \\ m_{nj} = 0.5 + 0.5k\sin(\omega t + x_j \frac{2}{3}\pi) \end{cases}, j = A, B, C \tag{3}$$

where x_A=1, x_B=0, x_C=1.

Suppose $L_m \gg L_\sigma$, then the equivalent arm resistance R_{arm} and inductance L_{arm} are obtained as,

$$\begin{cases} R_{arm} = R_p + R_\sigma \\ L_{arm} = L_\sigma \end{cases} \tag{4}$$

Applying KVL to each phase, we have,

$$\begin{cases} u_{lx} + u_{px} + R_{arm} i_{px} + L_{arm} \dfrac{di_{px}}{dt} = \dfrac{U_{dc}}{2}, \\ u_{lx} - u_{nx} - R_{arm} i_{nx} - L_{arm} \dfrac{di_{nx}}{dt} = -\dfrac{U_{dc}}{2}, \end{cases} x = a, b, c. \tag{5}$$

The average model of MMC arm can be described as

$$\begin{cases} C_{cp} = C_{sm} / N_{hp}, C_{cn} = C_{sm} / N_{hn} \\ u_{cp} = \dfrac{1}{C_{cp}} \int i_{cp} dt, u_{cn} = \dfrac{1}{C_{cn}} \int i_{cn} dt \\ i_{cp} = m_p i_p, i_{cn} = m_n i_n \end{cases} \tag{6}$$

where N_{hp} and N_{hn} denote the number of total remained healthy SMs of each arm. C_{sm} is the capacitance of SM. C_{cp} and C_{cn} are equivalent capacitance of upper and lower arm, respectively. u_{cp} and u_{cn} are the voltages of the upper and lower dc link while i_{cp} and i_{cn} represent the capacitor currents.

B. Under post-fault operation

1) SM level

To make full use of sub-module and ensure immediate redundancy, in this work, redundant SMs are designed to be hot-reserved. Redundant SMs are always inserted and operat-

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

ing in the same way as the other SMs. When SM failure occurs, only the failed SM is bypassed and the other all SMs keep working in the circuit. Thus, the equivalent capacitance of the faulty arm increases while the capacitive impedance decreases according to (6). Then the AC current is no longer evenly distributed between the upper and lower arm. With the consideration of asymmetrical AC current, the arm current i_p and i_n are expressed as,

$$\begin{cases} i_p = I_{dc} + 0.5 I_o \gamma_p \sin(\omega t + \varphi) \\ i_n = I_{dc} - 0.5 I_o \gamma_n \sin(\omega t + \varphi) \end{cases} \tag{7}$$

where I_{dc} is the dc current of each arm. φ and I_o are the phase angle and amplitude of output ac current while γ_p and γ_n are the unbalanced factors.

Then the sum of upper and lower arm voltage is deduced as,

$$\begin{aligned} & u_p + u_n = m_p u_{cp} + m_n u_{cn} = m_p \frac{1}{C_{cp}} \int m_p i_p dt + m_n \frac{1}{C_{cn}} \int m_n i_n dt \\ & = \underbrace{\frac{1}{2} N_{hp} \bar{u}_{cp} + \frac{1}{2} N_{hn} \bar{u}_{cn}}_{dc} + \underbrace{\frac{k^2}{64} \left(\frac{\gamma_p}{C_{cp}} - \frac{\gamma_n}{C_{cn}} \right) I_o \cos(3\omega t + \varphi)}_{3\omega} + \\ & \underbrace{\frac{k^2 + 8}{64} I_o \left(\frac{\gamma_n}{C_{cn}} - \frac{\gamma_p}{C_{cp}} \right) \cos(\omega t + \varphi) - \frac{k I_{dc}}{4} \cos(\omega t + \varphi) \left(\frac{1}{C_{cn}} - \frac{1}{C_{cp}} \right)}_{\omega} \\ & + \underbrace{\frac{3 k I_o}{8} \left(\frac{\gamma_n}{C_{cn}} + \frac{\gamma_p}{C_{cp}} \right) \sin(2\omega t + \varphi) - \frac{k^2 I_{dc}}{4} \sin(2\omega t) \left(\frac{1}{C_{cn}} + \frac{1}{C_{cp}} \right)}_{2\omega} \end{aligned} \tag{8}$$

Once the faulty SM bypassed, $\gamma_p \neq 1$, $\gamma_n \neq 1$, $C_{cn} \neq C_{cp}$. Then the fundamental and third harmonic components will be triggered in the dc loop. Hence, corresponding fault-tolerant control should be introduced to suppress the extra faulty components.

2) MMC phase level

When the number of failed SMs exceeds the designed tolerated number, it is considered as phase-level fault here. In practice, the MMC suffering phase-level fault should be shut down and replaced with another backup MMC but the backup MMC requires more space and investment. In this paper, to further improve its redundancy ability, the MMC is designed to ride-through phase level fault, which means the system operation can be ensured even with one disabled phase-leg.

As shown in Fig. 6, the upper and lower arms can be connected to the mid-point of the front-end MVDC bus by bidirectional switches, which can be realized by solid state switch based on IGBT in real applications [24]. When the phase-leg is broken, corresponding switches will be turned on to bypass the faulty leg and the IGBTs will be blocked.

Suppose the leg-B is failed, the switches S_B and S_b should be turned on to remove the faulty leg and the corresponding transformer as well. In this manner, the terminals of leg-B will be connected to the mid-point O. Therefore, as demonstrated in Fig. 6(b), the former arrangement of three transformers in Y-Y configuration will turn into V/V transformer configuration and its voltage phasor-diagram is presented in Fig. 7. Under symmetrical condition, the phase voltage of the secondary side can be expressed as,

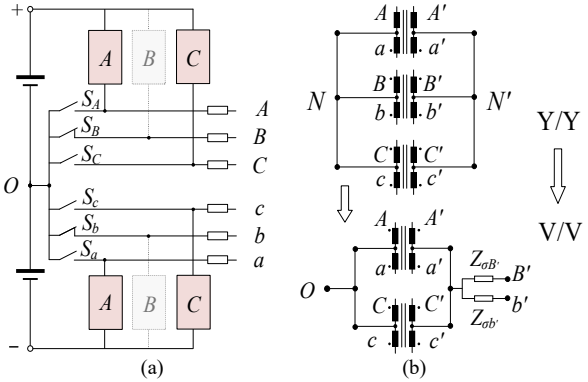

Fig. 6. Phase-level fault. (a) Topology reconfiguration. (b) MFT arrangement with phase-B bypassed.

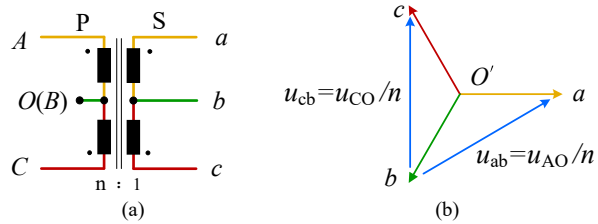

Fig. 7. Classical V/V transformer and its voltage phasor-diagram.

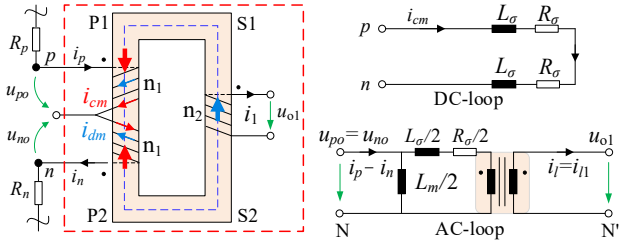

Fig. 8. MFT. (a) MFT with faulty bus removed. (b) Equivalent circuit.

$$\begin{cases} V_a = V_m \sin(\omega t + \theta) \\ V_b = V_m \sin(\omega t + \theta - 120°) \\ V_c = V_m \sin(\omega t + \theta + 120°) \end{cases} \tag{9}$$

where θ is the initial phase of each phase voltage. Then the phase voltage of the primary side can be obtained as (10) according to Fig. 7.

$$\begin{cases} V_{AO} = n V_m \sin(\omega t + \theta + 30°) \\ V_{CO} = n V_m \sin(\omega t + \theta + 90°) \end{cases} \tag{10}$$

Hence, unlike Y-Y transformer, the phase difference between two input voltages of the V/V transformer should be changed to 60 degrees instead of 120 degrees to obtain symmetrical ac power source in the secondary side. Thus, by reconfiguring the phase angles of the MMC modulation functions, normal three phase power source could be ensured. More details and the corresponding fault-tolerant strategy of control level will be discussed in the next section.

3) LVDC bus level

The short-circuit fault management of MVDC and LVDC buses is also critical issue for shipboard power system. In the proposed architecture, both primary and secondary converters can be blocked and the short-circuit current flowing through the converter can be avoided [9][10].

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

As shown in Fig. 2, in each electrical zone, the front-end MMC is connected to port-side and starboard-side MVDC buses to ensure MVDC bus redundancy. Back-end dual LVDC bus with bi-polar structure provides LVDC bus redundancy for the zonal load center.

With the ac circuit breaker in the middle ac stage, the fault of the LVDC level bus can be cleared and the services load can be shifted to the inherent standby LVDC bus. Assume that the ac circuit breaker is activated to achieve the clearance of LVDC bus fault and then the four-winding transformer turns into three-winding transformer as shown in Fig. 8(a). In this way, the modeling of the transformer can be deduced as,

$$\begin{cases} L_{\sigma}=L_{\sigma p}+n^2 L_{\sigma s}, R_{\sigma}=R_{\sigma p}+n^2 R_{\sigma s} \\ n_1 / n_2=n, 2i_{dm}=i_p - i_n = i_{l1} / n \\ u_{po} / u_{o1}=u_{no} / u_{o2} \approx n \end{cases} \tag{11}$$

Then the equivalent circuit of the transformer under fault conditions can be obtained as Fig. 8(b). Thus, the system can still maintain normal operation with the inherent standby bus taking over all connections from the faulty one. With the single-core structure, the direction of the magnetomotive force by common current component (highlighted as red arrow) are still of opposite direction. Thereby its magnetic flux will still not appear in the common iron core. DC flux cancellation can be still achieved in this case.

III. Fault-Tolerant Scheme of Control Level

The system fault-tolerant scheme consists of topology reconfiguration and fault ride-through control. The system hierarchical fault-tolerant scheme is shown in Fig. 9. Based on the topology reconfiguration scheme in the previous section, corresponding fault-tolerant control scheme will be discussed in this section.

A. SM-level fault-tolerant control

When the faulty SM is bypassed, extra fundamental and third harmonic components will appear in circulating currents. Since the third harmonic components are quite small compared with the fundamental ones, the main control objects of the circulating currents under faulty cases are the newly introduced fundamental components and the inherent second harmonic components.

To eliminate the faulty current components and the inherent second-order harmonic in circulating current, a multi-PR controller can be introduced here,

$$G_{\mathrm{PR}}(s)=K_p+\underbrace{\frac{2k_1\omega_1 s}{s^2+2\omega_1 s+\omega_0^2}}_{i_{cir\_\omega}}+\underbrace{\frac{2k_2\omega_2 s}{s^2+2\omega_2 s+(2\omega_0)^2}}_{i_{cir\_2\omega}} \tag{12}$$

where K_p is the proportional gain, k_1, k_2 and ω_1, ω_2 indicate the control gain and bandwidth.

As shown in Fig. 10, with the multi-PR controller, circulating current including faulty components can be suppressed without extra coordinate transformation [28]. Moreover, it is also feasible for symmetrical and asymmetrical AC system.

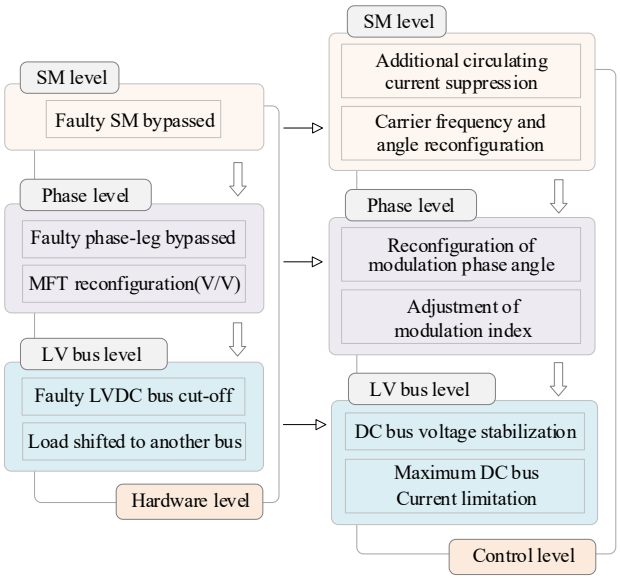

Fig. 9. Hierarchical fault-tolerant scheme of topology and control level.

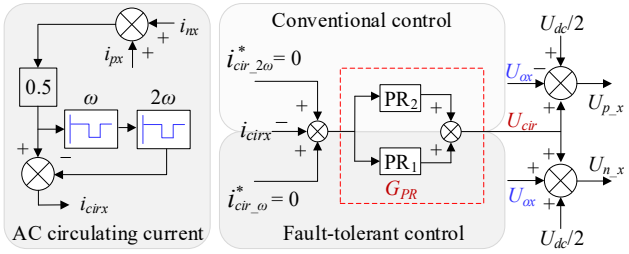

Fig. 10. SM-level fault-tolerant control.

Once N_f SMs (N_f<N_r) are bypassed, the capacitor voltages of the other SMs in the faulty arm should be increased to keep the energy balanced among different arms [20], which results in the transient charging process and the updated average capacitor voltage is,

$$V_c'=V_c\sqrt{\frac{N_n+N_r}{N_n+N_r-N_f}} \tag{13}$$

where V_c is the rated capacitor voltage when all the SMs are healthy. N_r and N_n are the number of redundant SMs and nominal SMs per arm. N_f is the number of faulty SMs per arm. Besides, when faulty SMs bypassed, the number of working SM reduces. Hence, the frequency and phase-shifting angles of the carriers will be reconfigured herein to mitigate distortions of the upper and lower arm current.

B. Phase-level fault-tolerant control

Based on the topology reconfiguration scheme mentioned above, the failed phase-leg will be bypassed and the transformer will work as V/V transformer.

To obtain a symmetrical ac power source, the phase difference between two input voltages of the V/V transformer should be modified as 60 degrees instead of 120 degrees. Hence, the MMC modulation functions should be reconfigured to ride-through phase-level fault.

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

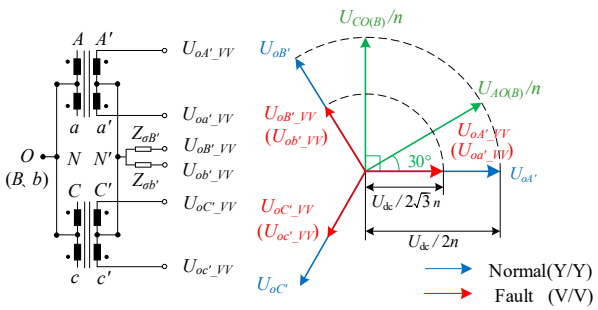

Fig. 11. Voltage phasor-diagram of MMC under phase-level fault.

TABLE II
MODULATION RECONFIGURATION

Faulty Leg	Phase Angle of Modulation Wave		
	Phase A	Phase B	Phase C
Leg A	/	150°	210°
Leg B	30°	/	90°
Leg C	-30°	-90°	/

According to (13), if the initial phase angle is zero (θ=0º), modulation angle of phase A and C should be changed to 30 and 90 degrees in the event of phase B fault. Similarly, the reconfiguration results in the cases of other phase-failure conditions are listed in Table II.

As shown in Fig. 11, the magnitude of the transformer output line-to line voltage under phase-level fault is equal to the magnitude of the output phase-voltage under normal conditions. Thus, the phase-voltage of the transformer is reduced to,

$$U_{oA'\_VV} = U_{oA'} / \sqrt{3} = U_{dc} / 2\sqrt{3}n \tag{14}$$

where $U_{oA'\_VV}$ and $U_{oA'}$ are the phase-voltages of the transformer under normal and fault-tolerant circumstances, respectively and U_{dc} is the MVDC bus voltage. It should be noted that the decreased transformer voltage is acceptable if the transformer current increases to maintain the constant power supply and LVDC bus voltage to load centers, which can be implemented by the power flow control of the PWM rectifier in the LVDC side. In addition, in order not to increase the current stress, modulation index of the MMC could be adjusted to increase the output voltage of the ac link and reduce the current to some degree at the same time.

C. DC bus-level fault-tolerant control scheme

The main control objects of the back-end rectifiers are voltage stabilization of the LVDC bus and maximum current limitation. With output power control and fault current limiting of MMC and back-end rectifiers as discussed in [4], the overload current of LVDC bus can be limited.

In this section, this work focuses on the clearance of faulty LVDC bus and the redundancy of zonal power supply. To clear the faults occurring in the secondary side, the IGBT blocking signals are enabled and the corresponding rectifier should be shut down. Moreover, ac circuit breakers (K1 or K2) of the middle ac stage will be turned off to isolate faults. Importantly, the zonal loads will be removed from the faulty bus and picked up by the other normal bus to maintain normal operation, which is the same case when one set of the secondary windings of the MFT in the ac link is removed due to some certain ac faults.

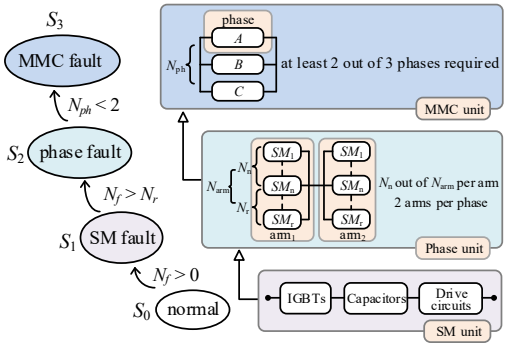

Fig.12. Hierarchical reliability modeling and fault transient of MMC.

IV. REDUNDANT CONFIGURATION WITH RELIABILITY CONSIDERATION

To quantify the effectiveness of the proposed fault-tolerant scheme and find out the suitable redundant configurations, simplified reliability modelling based on a statistical method will be discussed in this section.

A. Reliability modelling of MMC with the proposed hierarchical fault-tolerant control scheme

Based on the designed hierarchical fault-tolerant scheme, hierarchical reliability modeling and fault transient of MMC are shown in Fig.12.

When the number of faulty SMs (N_f) is less than that of redundant ones (N_r), the system turns into the first state S_1: SM-level fault. When the number of faulty SMs exceeds the tolerated number and the corresponding phase-leg would be bypassed, the system turns into the second state S_2: phase-level fault. When more phase legs are broken down, then the system turns to the third state S_3: MMC fault.

Based on the hierarchical reliability modeling, the reliability function of each level can be obtained. Assume that the submodule failure rate is denoted as λ, then its reliability function and failure function can be expressed as (15).

$$\begin{cases} R_{SM} = e^{-\lambda t} \\ F_{SM} = 1 - R_{SM} \end{cases} \tag{15}$$

For phase-leg level, both upper arm and lower arm should be healthy and at least N_n SMs of each arm are normal which is called k-out-of-n: G system in [29]. The phase-leg reliability function based on combinatorial theory is deduced as (16).

$$R_{ph} = R_{arm} = \left(\sum_{k=0}^{N_r} C_{N_n+N_r}^{k} R_{SM}^{N_n+N_r-k} F_{SM}^{k}\right)^2 \tag{16}$$

For the whole MMC, at least 2 out of 3 phases are required, then the MMC reliability is calculated as R_{MMC1} in (17) without the consideration of the remained healthy SMs in the bypassed phase-leg.

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

$$R_{\mathrm{MMC1}} = C_3^2 R_{\mathrm{ph}}^2 (1-R_{\mathrm{ph}}) + C_3^3 R_{\mathrm{ph}}^3$$
$$= C_3^2 (\sum_{k=0}^{N_r} C_{N_n+N_r}^k R_{\mathrm{SM}}^{N_n+N_r-k} F_{SM}^k)^2 [1-(\sum_{k=0}^{N_r} C_{N_n+N_r}^k R_{\mathrm{SM}}^{N_n+N_r-k} F_{\mathrm{SM}}^k)^2] \quad (17)$$
$$+ \underbrace{(\sum_{k=0}^{N_r} C_{N_n+N_r}^k R_{\mathrm{SM}}^{N_n+N_r-k} F_{\mathrm{SM}}^k)^6}_{R_{\mathrm{MMC2}}}$$

where R_{MMC2} is regarded as the reliability function of MMC with only SM redundancy but not phase-leg redundancy.

B. Reliability analysis and comparison of MMC with different redundant designs

The MMC applied for medium voltage applications usually require 4 to 10 basic SMs in each arm [18]. Considering reliability requirement of MMC, redundant SMs should be introduced. Reliability comparison results of MMC with and without redundancy are plotted in Fig. 13, where specific number of basic submodule and fixed submodule reliability are chosen to quantify the reliability evaluation.

The curve 1 and 2 show the reliability results of MMC with proposed hierarchical redundancy and only SM-level redundancy, while the curve 3 represents the MMC reliability with no redundancy. Compared with non-redundant designs, the introduction of one redundant SM improves the MMC reliability significantly. Compared with the redundant design of only SM-level, reliability of MMC with hierarchical redundant strategy is higher and decreases more slowly as the number of basic submodule increases.

However, with only one redundant SM, the reliability requirement is not met especially for the cases of lager submodule number. More redundant SMs are needed for reliability requirement. To make a trade-off between higher reliability and less redundant SMs, reliability index is defined here.

$$\xi(N_r) = R_{\mathrm{mmc}} / N_r \quad (18)$$

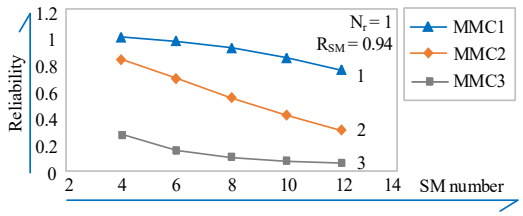

Fig.13. Reliability comparison of MMC with different redundancy.

TABLE III
RELIABILITY OF MMC WITH VARIABLE SUBMODULES

N_n	R_{sm}	N_r	N_{arm}	R_{arm}	R_{ph}	R_{mmc1}
4	0.92	1	5	0.946	0.894	0.969
		2	6	0.991	0.983	0.999
6	0.92	1	7	0.897	0.805	0.901
		2	8	0.979	0.958	0.995
8	0.92	1	9	0.842	0.708	0.795
		2	10	0.960	0.921	0.982
		3	11	0.991	0.983	0.999
10	0.92	1	11	0.782	0.611	0.664
		2	12	0.935	0.874	0.956
		3	13	0.984	0.968	0.997

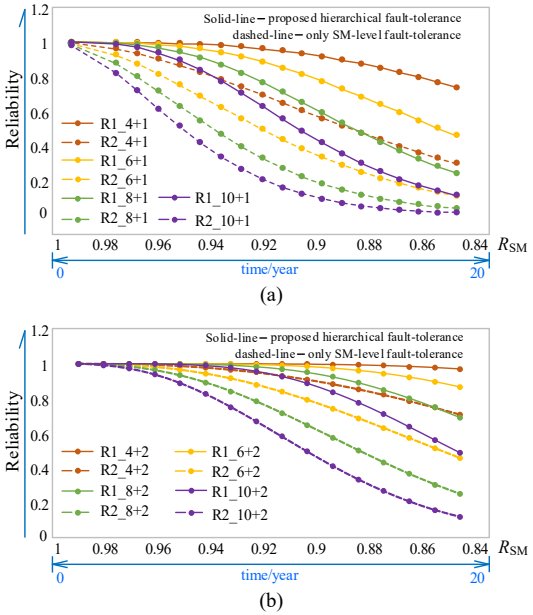

Fig. 14. Reliability comparison of MMC with different fault-tolerant strategies. (a) With only one redundant SM. (b) With two redundant SMs. R1_4+1: reliability of MMC (4 basic SMs and 1 redundant SMs) with proposed hierarchical redundant method. R2_4+2: reliability of MMC (4 basic SMs and 2 redundant SMs) with only conventional SM-level redundancy.

By comparing the changes of $\xi(N_r)$, reliable configuration of redundant SMs can be determined. When $\xi'(N_r) = 0$, the optimum interval of redundant SMs can be estimated.

Table III shows the reliability of MMC with variable basic SMs and redundant SMs. By adding the second redundant SM, relatively high reliability for all the four cases can be obtained. It may be enough to meet the system requirement for the MMC with 4 to 6 basic SMs while the optimal redundant SM number may be more than three for the case of 8 to 10 basic SMs.

To evaluate the MMC reliability over a time span of years, specific SM failure rate should be obtained. The time-varying reliability function of SM is approximately calculated as (19) with the failure rate λ=10^{-6} [29][30].

$$R_{\mathrm{SM}} = e^{-10^{-6}t} = e^{-8760*10^{-6}y} \quad (19)$$

The reliability comparison results of MMC with different fault-tolerant strategies over 20 years are presented in Fig. 14. The solid-line curves show the results of proposed redundant design while the dashed-line curves denote the reliability of MMC with only SM-level redundancy. According to Fig. 14, with the presented hierarchical redundant method, the inclusion of two redundant SMs can achieve system reliability requirement over a longer period. Compared with the MMC with only regular SM-level fault-tolerant control, the MMC in the same redundant configuration but with the proposed hierarchical control can achieve higher reliability and the reliability decreases more slowly with the using time increasing.

V. EXPERIMENTAL VERIFICATION

Experiments are conducted in the RT-LAB platform to verify the proposed architecture and the hierarchical fault-tolerant scheme of topology and control level. The control board based

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

TABLE IV
SYSTEM PARAMETERS

System Ratings	
MVDC bus voltage U_{MVDC}	800 V
LVDC bus voltage U_{LVDC}	600 V
Modulation frequency f	200 Hz
MMC Parameters	
Basic SMs N_{arm}	4
Redundant SMs N_r	2
MFT Parameters	
leakage inductance $L_{\sigma p}$ (primary)	0.5mH
leakage inductance $L_{\sigma s}$ (secondary)	50μH
leakage resistance $R_{\sigma s}$	1m Ω
Turn ration n_1:n_2	2:1
Load Parameters	
***RL* load**	
Load resistance R_L	1 Ω
Load inductance L_L	0.6 mH
PWM rectifier	
DC capacitance C_{dc}	5600μF
Load resistance R_{dc}	30 Ω

on DSP TMS320F2812 is connected to the signal acquisition and output boards of the RT-LAB machine. System parameters are demonstrated in Table IV.

A. Experimental Results under normal circumstances

The three-phase MMC integrated with the MFT is connected to the balanced three-phase *RL* loads and the experimental results with no circulating current control are presented in Fig.15. The MMC dc-link current, the upper and lower arm current and circulating current in phase A are shown in Fig.15(a). Fig. 15(b) shows the primary voltages u_{po}, u_{no} of MFT and the equivalent output current i_{sa} of MMC. Fig. 15(c) shows the load phase voltage and current in phase A. Fig. 15(d) shows the upper and lower arm capacitor voltage and total capacitor voltage, which are kept balanced. It can be observed that the proposed architecture can operate the typical MMC and provide two ac power interfaces.

B. Experimental Results under SM-fault circumstances

Experimental results of SM-level faults are shown in Fig. 16. The circulating current i_{za} contains both fundamental and second-order components as illustrated in Fig. 16(a). Fig. 16(b)

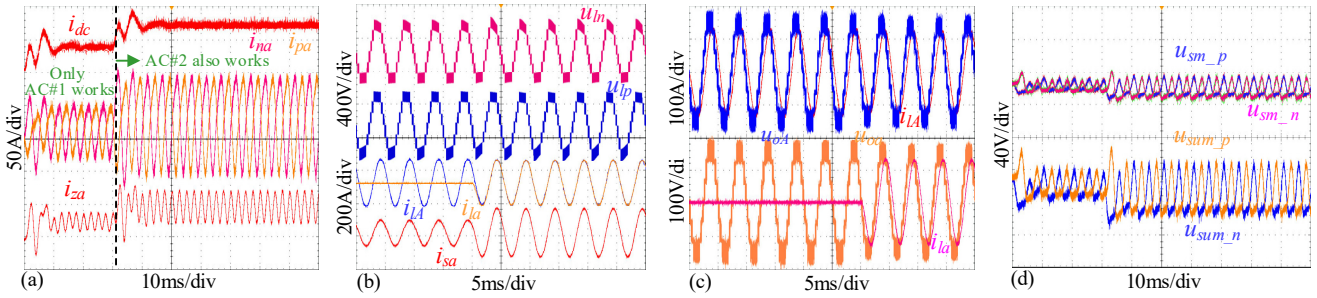

Fig. 15. Under normal cases. (a) DC bus current, arm currents and circulating current. (b) primary voltages of MFT and system current. (c) output voltages and currents. (d) SM capacitors voltages.

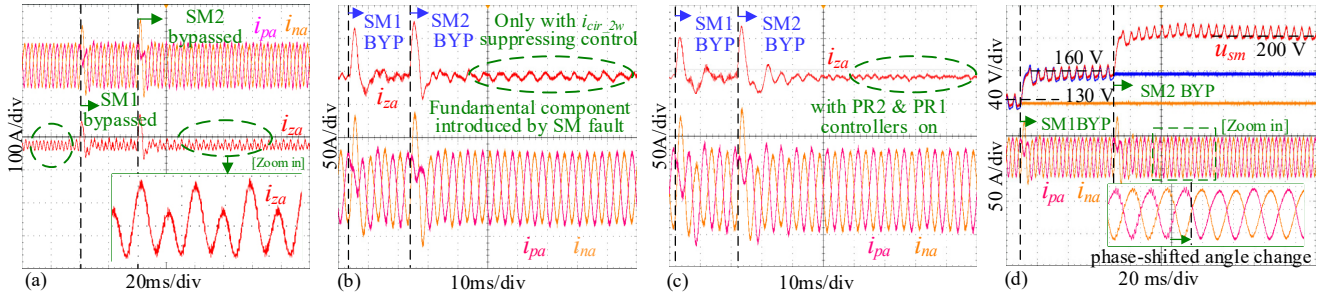

Fig. 16. SM fault. (a) without control. (b) with second-order circulating current control. (c) with fault-tolerant control. (d) SM voltages and arm currents.

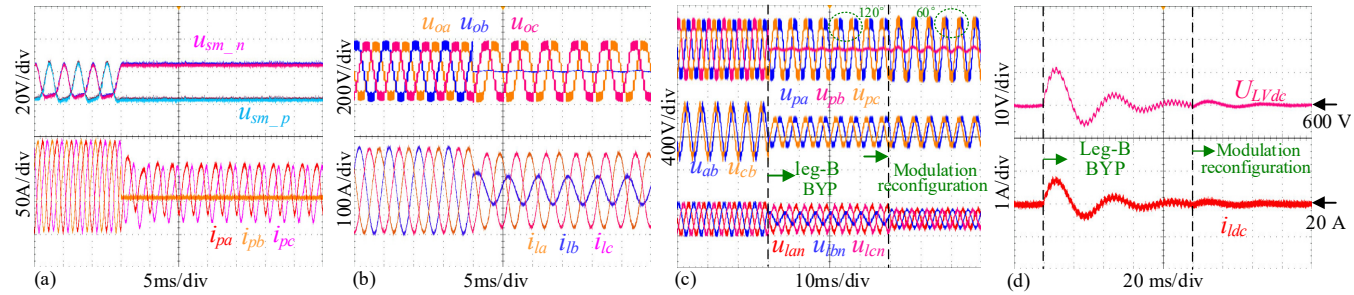

Fig. 17. Phase level fault. (a) SM voltage and arm current. (b) phase voltage and current. (c) arm voltages, line-to-line voltage and phase voltage. (d) dc-bus voltage and load current of back-end three-phase bridge rectifier.

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

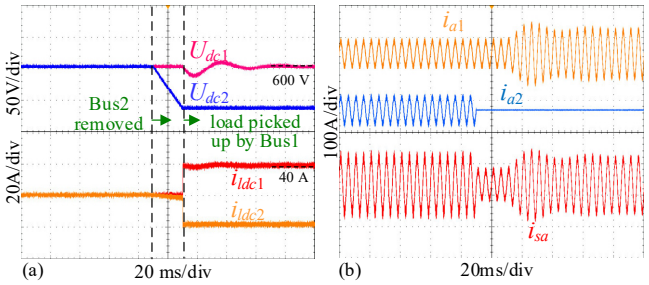

Fig. 18. Bus-level fault. (a) U_{LVDC} and i_{ldc}. (b) i_{ldc} and i_{sa}.

shows the extra fundamental components introduced by SM fault. However, as shown in Fig. 16(c), with the multi-PR controller activated, the faulty and inherent circulating current can be eliminated effectively. According to Fig. 16(d), it can be seen that after the faulty SMs are bypassed, the capacitor voltage of the healthy SMs will increase to keep the energy balanced among different arms. Besides, when faulty SMs bypassed, the number of working SM reduces. Hence, the frequency and phase-shifting angle and of the carriers will be reconfigured herein to mitigate distortions of the upper and lower arm current, as shown in the close-up image (bottom) of Fig. 16(d).

C. *Experimental Results under phase-fault circumstances*

As mentioned above, if the MMC leg is faulty and bypassed, the fault-tolerant operation requires topology and modulation reconfiguration. The experimental results of phase-B fault are shown in Fig. 17.

As illustrated in Fig. 17(a), when the MMC leg of phase-B is bypassed and all SMs in this phase are blocked, the three-phase system will suffer unbalance. In Fig. 17(b), the phase current and voltage of load-side are demonstrated. With the phase-B bypassed, the voltage of phase-B turns to zero and the currents become unbalanced. However, with the proposed modulation reconfiguration scheme, symmetrical three-phase source voltage can be restored again with reduced voltage level.

When two identical three-phase bridge rectifiers are connected to MMC, the voltage and current of the LVDC bus will fluctuate with the faulty leg-B bypassed as shown in Fig. 17(d). With modulation reconfiguration, the normal DC bus voltage and current can be obtained again.

D. *Experimental Results under Bus-fault in the LVDC side*

In this case, the three-phase MMC is connected to two PWM rectifiers to provide dual LVDC bus with bi-polar structure. Then the second PWM rectifier is removed via ac circuit breaker K2 shown in Fig. 2 to simulate the dc bus failure. As shown in Fig. 18(a), the dc link voltage U_{dc2} and load current I_{dc2} of the second PWM rectifier will decrease before its load is connected to bus1. When the bus1 pick up the load from bus2, the dc link voltage should keep the normal level with the current increasing to maintain normal power supply. Fig. 18(b) shows the input current of phase A of two PWM rectifiers and the output system current of phase A of the MMC. Hence, the system can work normally even when one of the dc buses fails.

VI. Conclusions

The power architecture and hierarchical fault-tolerant scheme of a DC/DC converter based on three-phase MMC and three-phase bridge converter are investigated in this work.

The four-winding MFT connecting the front-end MMC with two back-end rectifiers can save the MMC arm reactors with reasonable leakage inductance and provide a dual bus structure for redundancy improvement. The hierarchical topology and control reconfiguration schemes can ride-through SM fault, phase-leg fault and LVDC bus fault and improve the utilization rate of MMC and power reliability of the zonal load center. The hierarchical fault-tolerant scheme is proved to be effective with the reliability modeling for MMC and can meet the reliability requirement over a longer time span with reducing redundant SMs, which is beneficial to the shipboard applications.

Some solutions of MFT have been applied to power electronic traction transformers but the multifunctional role of MFT imposes certain challenges on its optimal design and still require future research. Meanwhile, for MMC on ships, protection coordination, possibility of efficiency improvement and multiple-function integration such as energy storage ability should be further studied in the future.

References

[1] Z. Jin, G. Sulligoi, R. Cuzner, L. Meng, J. C. Vasquez and J. M. Guerrero, "Next-Generation Shipboard DC Power System," *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 45–57, June 2016.

[2] Z. Jin, L. Meng, J. M. Guerrero and R. Han, "Hierarchical control design for a shipboard power system with dc distribution and energy storage aboard future more-electric ships," *IEEE Trans. Ind. Informat.*, vol. 14, no. 2, pp. 703–714, Nov. 2017.

[3] D. Dong *et al.*, "Control and operation of medium-voltage high-power bi-directional resonant DC-DC converters in shipboard dc distribution systems," in *Proc. IEEE Energy Convers. Cong. Expo. (ECCE)*, 2016, pp. 1–9.

[4] Y. Chen, S. Zhao, Z. Li, X. Wei, Y. Kang, "Modeling and Control of the Isolated DC–DC Modular Multilevel Converter for Electric Ship Medium Voltage Direct Current Power System," *IEEE J. Emerg. Sel. Topics in Power Electron.*, vol. 5, no. 1, pp. 124–139, 2017.

[5] J. S. Thongam, M. Tarbouchi, A. F. Okou; D. Bouchard, R. Beguenane, "All-electric ships- A review of the present state of the art," in *Pro. 8th International Conference Exhibition on Ecological Vehicles and Renewable Energies* (*EVER*), 2013, pp. 1–8.

[6] R. M. Cuzner and D. A. Esmaili, "Fault tolerant shipboard MVDC architectures," in *Proc. International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles* (*ESARS*), Aachen, 2015, pp. 1–6.

[7] R. Schmerda, R. Cuzner, R. Clark, D. Nowak and S. Bunzel, "Shipboard Solid-State Protection: Overview and Applications," *IEEE Electrification Magazine*, vol. 1, no. 1, pp. 32–39, Sept. 2013.

[8] Z. Jin, L. Meng, J. C. Vasquez, J. M. Guerrero, "Frequency-Division Power Sharing and Hierarchical Control Design for DC Shipboard Microgrids with Hybrid Energy Storage Systems", in *Proc. IEEE Appl. Power Electron. Conf. Expo.* (*APEC*), 2017, pp. 3661–3668.

[9] R. Xie, R. Mo, Y. Shi, H. Li, "Comparative Study of the DC-DC Power Conversion Module based on Dual Active Bridge Converter and Modular Multilevel Converter for Shipboard MVDC System," in *2017 IEEE Electric Ship Technologies Symposium* (*ESTS*), 2017, pp. 36–43.

[10] B. Zhao, Q. Song, J. Li, X. Xu, W. Liu, "Comparative Analysis of Multilevel-High-Frequency-Link and Multilevel-DC-Link DC-DC Transformers Based on MMC and Dual-Active-Bridge for MVDC Application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2035–2049, May 2017.

[11] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. De Novaes, "Isolated dc/dc structure based on modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89–98, Feb. 2014.

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2018.2879981, IEEE Transactions on Industrial Informatics

[12] A. Christe; D. Dujic, "Galvanically isolated modular converter", *IET Power Electron*., vol. 9, no. 12, pp. 2318-2328, 2016.

[13] J. Zhang, Z. Wang and S. Shao, "A Three-Phase Modular Multilevel DC–DC Converter for Power Electronic Transformer Applications," *IEEE J. Emerg. Sel. Topics in Power Electron*., vol. 5, no. 1, pp. 140–150, Mar. 2017.

[14] Y. Shi, R. Mo, H. Li and Z. Pan, "A novel ISOP current-fed modular dual-active-bridge (CF-MDAB) DC-DC converter with DC fault ride-through capability for MVDC application," in *Pro. IEEE Energy Conversion Congress and Exposition (ECCE),* 2017, pp. 4525–4530.

[15] L. Wang, A.Q. Huang and Q. Zhu, "Multi-objective optimization of medium voltage SiC DC-DC converter based on modular input-series-output-parallel (ISOP) architecture," *in Proc. 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia),* 2017, pp. 627–632.

[16] W. Chen, X. Jiang. W. Cao, J. Zhao, W. Jiang and L. Jiang, "A Fully Modular Control Strategy for Input-Series Output-Parallel (ISOP) Inverter System Based on Positive Output-Voltage-Amplitude Gradient," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2878-2887, May, 2017.

[17] B. Zhao, Q. Song, J. Li, W. Liu, G. Liu, and Y. Zhao, "High-frequency link dc transformer based on switched capacitor for medium-voltage dc power distribution application," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4766–4777, Jul. 2016.

[18] Y. Chen; Z. Li; S. Zhao; X. Wei; Y. Kang, "Design and Implementation of a Modular Multilevel Converter with Hierarchical Redundancy Ability for Electric Ship MVDC System," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 189–202, 2017.

[19] B. Li, S. Shi, B. Wang, and G. Wang, "Fault diagnosis and tolerant control of single IGBT open circuit failure in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3165–3176, Apr. 2016.

[20] K. Li; L. Yuan; Z. Zhao; S. Lu; Y. Zhang, "Fault-Tolerant Control of MMC With Hot Reserved Submodules Based on Carrier Phase Shift Modulation," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6778-6791, 2017.

[21] F. Deng; Y. Tian; R. Zhu; Z. Chen, "Fault-Tolerant Approach for Modular Multilevel Converters Under Submodule Faults", *IEEE Trans. Ind. Electron.*, vol.63, no.11, pp.7253-7263, 2016.

[22] M. Andresen, L. F. Costa, G. Buticchi, and M. Liserre, "Smart transformer reliability and efficiency through modularity," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, May 2016, pp. 3241–3248.s

[23] R. Xie, Y. Shi and H. Li, "Modular multilevel DAB (M^2DAB) converter for shipboard MVDC system with fault protection and ride-through capability," in *2015 IEEE Electric Ship Technologies Symposium (ESTS)*, 2015, pp. 427-432.

[24] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri and P. Stefanutti," Power electronic traction trans-former—Medium voltage prototype," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, July 2014.

[25] H. Hoffmann and B. Piepenbreier, "High voltage IGBTs and medium frequency transformer in DC–DC converters for railway applications," *in Proc. Int. SPEEDAM*, Pisa, Italy, 2010, pp. 744–749.

[26] M. Mogorovic, D. Dujic, "100kW, 10kHz medium frequency transformer design optimization and experimental verification," *IEEE Trans. Power Electron.*, Early access.

[27] H. Nademi, A. Das, R. Burgos and L. Norum "A new circuit performance of modular multilevel inverter suitable for photovoltaic conversion plants," *IEEE Trans. Emerg. Sel. Topics Power Electron.*,vol. 4, no. 2, pp. 393-404, Jun. 2016.

[28] L. Bede, G. Gohil, M. Ciobotaru, T. Kerekes; Remus. Teodorescu, V. G. Agelidis, "Circulating current control for parallel interleaved VSCs connected in whiffletree configuration," *IEEE 7th International Symposium on PEDG*, 2016, pp. 1–6.

[29] P. Tu, S. Yang, P. Wang, "Reliability and cost based redundancy design for modular multilevel converter," *IEEE Trans. Ind. Electron.*, Early access.

[30] Y. Xue, B. Ge, F. Peng, "Reliability, efficiency, and cost comparisons of MW-scale photovoltaic inverters," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*,2012, pp. 1627–163

Lerong Hong was born in Guangdong, China, 1993. He received the B.S. degree in Electrical Engineering and Automation from the College of Electrical and Information Engineering, Hunan University, Changsha, China, in 2016. He has been working toward the Ph.D. degree in Electrical Engineering in the College of Electrical and Information Engineering, Hunan University, Changsha since 2017.

His research interests include modular multilevel converter, power quality control and dc grid control.

Qianming Xu (M'17) was born in Henan, China, in 1989. He received the B.S. degree in electrical engineering and automation and the Ph.D. degree in electrical engineering from Hunan University, Changsha, China, in 2012 and 2017, respectively.

Since 2017, he has been an Assistant Professor with the College of Electrical and Information Engineering, Hunan University. His research interests include modular multilevel converter, power quality control, and dc grid control.

Zhixing He (M'17) was born in Hunan, China, in 1989. He received the B.S. degree in automation from Central South University, Changsha, China, in 2011, and the Ph.D. degree in electrical engineering from Hunan University, Changsha, China, in 2016.

He is currently a Postdoctoral Fellow with Hunan University. His current research interests include modular multilevel converter, model predictive control, and high-frequency link power conversion system.

Fujun Ma (M'15) was born in Hunan, China, 1985. He received the B.S. degree in Automation and Ph.D. degree in Electrical Engineering from Hunan University, Changsha, in 2008 and 2015, respectively.

Since 2013, he has been an Associate Professor with the College of Electrical and Information Engineering, Hunan University. His research interests include power quality managing technique of electrified railway, electric power saving, reactive power compensation, and active power filters.

An Luo (SM'09) was born in Changsha, China, in 1957. He received the B.S. and M.S. degrees in industrial automation from Hunan University, Changsha, China, in 1982 and 1986, respectively, and the Ph.D. degree in fluid power transmission and control from Zhejiang University, Hangzhou, China, in 1993.

Since 2003, he has been a Professor at Hunan University, where he also serves as the Chief of the National Electric Power Conversion and Control Engineering Technology Research Center. Dr. Luo was elected to the Chinese National Academy of Engineering in 2015. His research interests mainly include distributed generation, microgrid and power quality.

Josep M. Guerrero (FM'15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively.

Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program. From 2015 he is a distinguished guest Professor in Hunan University.

His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, smart metering and the internet of things for AC/DC microgrid clusters and islanded minigrids; recently specially focused on maritime microgrids for electrical ships, vessels, ferries and seaports.

1551-3203 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.