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Asymmetrical Reactive Power Capability of Modular Multilevel Cascade Converter (MMCC) based STATCOMs for Offshore Wind Farm

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***Abstract*— Modular Multilevel Cascade Converters (MMCC) are becoming attractive solutions as high voltage Static Synchronous Compensators (STATCOMs) for power plants in renewable energy generation, in order to satisfy the strict grid codes under both normal and grid-fault conditions. This paper investigates the performances of potentially used four configurations of the MMCC family for the STATCOM in large-scale offshore wind power plants, with special focus on asymmetrical Low Voltage Ride Through (LVRT) capability under grid faults. Specifications and the component sizing of each type of practical 80 MVar / 33 kV scaled MMCC-STATCOM are carefully designed and compared. The total cost and volume are compared based on total power semiconductor chip area and total energy stored of the passive components. Asymmetrical reactive power delivering operation of the MMCC family considering the dc-link capacitor voltage balancing method is solved mathematically in order to quantitatively understand the performance limitations and behaviors. The electro-thermal stress of the power modules used in each type of the MMCC for a practical 80 MVar /33 kV STATCOM is analyzed. The asymmetrical reactive power capability of the MMCC solutions is compared under different scenarios of grid faults, with the considerations of the device temperature limits and also voltage saturation. It is found that the MMCC configuration with Double Star Bridge Cells becomes the most attractive circuit configuration for the STATCOM application based on the obtained results.**

***Index Terms*— Static VAR compensators, Reactive power, Wind power generation, MMCC, STATCOM, Asymmetrical grid faults**

I. INTRODUCTION

THE capacity of renewable energy generation has continued to grow in the last decade, and it will become 2.5 TW in 2020 [1]. In accordance with constructions of large-scale renewable energy generation systems such as solar PV and wind power plants, stricter grid codes under both normal operation and grid fault conditions are demanded by Transmission System Operators (TSO) in most countries [2].

Offshore wind power plants have become one of the major renewable energy sources in Europe with strong wind conditions because of the advantages such as constant and high wind velocity as well as extensive offshore area. However, the generated electrical power has to be transmitted to the Point of Common Cupping (PCC) onshore by long-distance submarine cables, which arise a large amount of reactive power if Medium to High Voltage Alternative Current (MVAC-HVAC) transmission system is selected. In order to compensate enough reactive power and satisfy the grid codes, SVC or STATCOMs have to be installed on the onshore side of the wind power plant.

The Modular Multilevel Cascade Converters (MMCC) family could be suitable solutions in the case of the high-voltage and high-power STATCOM application. They have significant advantages, compared to the conventional two-level or three-level voltage source converters which have series-connected bipolar-power semiconductor devices, such as lower harmonic distortions, transformer-less configuration at medium voltage level, and modular/ redundancy design. Nevertheless, voltage-balancing for a large number of DC-link capacitors in converter cells are still challenging to be achieved for MMCCs, especially under asymmetrical grid faults [4-7].

MMCC solutions with Single Star Bridge Cells (SSBC) and Single Delta Bridge Cells (SDBC) have been reported to be used for STATCOM and battery energy management system application [8], [9]. They can keep operating under an asymmetrical grid fault by activating the voltage-balancing control methods for converter cells such as zero-sequence AC voltage injection method for SSBC [10], [11] and zero-sequence AC current injection method for SDBC [12]. However, in order to avoid the voltage saturation and over junction temperature, these voltage-balancing methods could result in increased voltage and current stress of the converters and thereby they may compromise the reactive power delivering capability of the MMCCs when they are practically designed for wind farms.

MMCC solutions with Double Star Chopper Cells (DSCC) and Double Star Bridge cells (DSBC) have been reported to be used for Back-to-Back converters such as Medium Voltage motor drive and High Voltage Direct Current (HVDC) transmission applications typically, but they can also be used for a STATCOM application. They can keep operating under

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asymmetrical grid faults by activating the voltage-balancing control using circulating dc current having two degrees of freedom [13-15]. This voltage-balancing method also results in increased current stress of the converters. However, this method may have higher reactive power delivering capability compared with an SSBC and SDBC because of more flexibility in the circulating dc current.

A lot of authors have proposed many useful control schemes and design methods for each type of MMCC solution until now. However, the optimum MMCC solution for the STATCOM application is still an open question because comprehensively comparison between four types of the MMCC solutions has not been done [16, 17, 28, 29]. In addition to total cost and volume of the MMCC solutions, the asymmetrical reactive power delivering capability under grid faults becomes more and more important for the STATCOM application.

This paper clarifies the performances of potentially used four configurations of the MMCC family with SSBC, SDBC, DSCC, and DSBC for the STATCOM in large-scale offshore wind power plants, with special focus on asymmetrical Low Voltage Ride Through (LVRT) capability under grid faults. In section II, the system configuration of typical offshore wind power plant and system grid fault scenarios are summarized. In section III, specifications and the component sizing of each type of practical 80 MVar / 33 kV scaled MMCC-STATCOM are carefully designed and compared. The total cost and volume are compared based on total power semiconductor chip area and total energy stored of the passive components. In section IV, the mathematical formulation for the STATCOM based on the MMCC solutions under asymmetrical compensation operation is developed which contributes to quantitative understanding of the performance limitations and circuit behaviors under the asymmetrical compensation. In section V, the electro-thermal stresses of actual power modules used in each type of the MMCC with practical controls are analyzed in detail. The asymmetrical reactive power capacity focusing on the MMCC solutions is compared under different scenarios of grid faults, with the consideration of device temperature limits and voltage saturations. Finally, in section VI, most attractive MMCC solution for the STATCOM application is suggested based on obtained results.

II. Typical Offshore Wind Plant and System Fault Scenarios

A. The system configuration for analysis

Fig. 1 shows the system configuration of a typical offshore wind power plant and an MMCC-based STATCOM. The generated active power from the offshore wind farm needs to be provided to the Point of Common Coupling (PCC) as *Bus* A (400 kV in this case) by an HVAC transmission system (220 kV in this case) with long distance submarine cables. Reactive power induced by the submarine cable is compensated by the full-scale converters of wind turbines, the shunt reactor, and the STATCOM connected to *Bus* B via a delta-star transformer. Other power generators and loads beside the wind power plant may also be connected to *Bus* A.

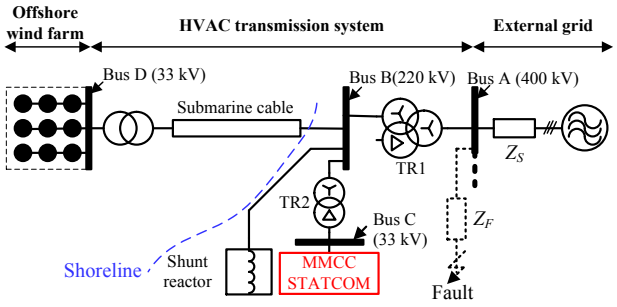
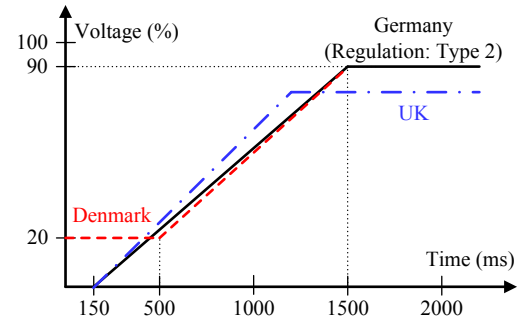
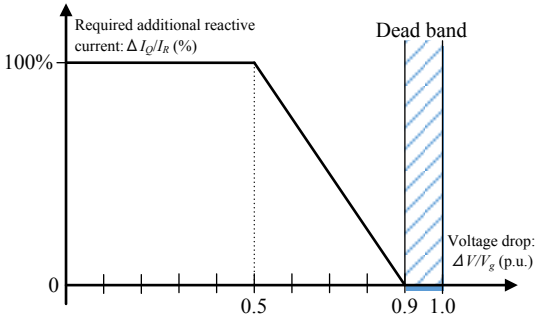


Fig. 1. A typical offshore wind power plant with an MMCC-STATCOM.



(a) LVRT requirement by different countries.



(b) Additional reactive current requirement during LVRT

Fig. 2. Reactive power requirements of large-scale generating plants under

B. Reactive power requirement under grid fault

Besides the normal operation, Transmission System Operators (TSOs) in different countries have issued strict grid supporting requirement for the growing large-scale renewable power plant such as the offshore wind power plant under grid fault which is specified in Fig. 2 [18], [19]. According to the grid codes, the offshore wind power plant has to keep the operation regarding the voltage sag under grid fault as shown Fig. 2 (a), and in the case of German and Danish codes should be able to inject additional reactive current to support the recovery of grid voltage sag which is also in Fig. 2 (b). The reactive current reference is only defined as positive-sequence component because recent grid codes do not require negative-sequence current to compensate the asymmetrical grid fault voltage recovering. However, this feature may become a future requirement [20]. In this paper, the positive sequence reactive current injection capabilities of each type of MMCC solution under grid faults are analyzed.

TABLE I
PHASOR DIAGRAM AND VECTOR DEFINITIONS OF DIFFERENT FAULT SCENARIOS ON PCC (*BUS* A)

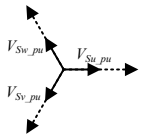
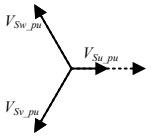
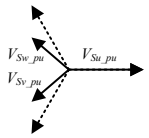
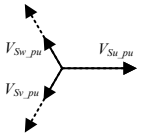
Fault types	Phasor diagram diffinitions	Vecter deffinitions
(a) Three-phase-to-ground fault		$V_{Su\_pu} = D$ $V_{Sv\_pu} = -\frac{1}{2}D - j\frac{\sqrt{3}}{2}D$ $V_{Sw\_pu} = -\frac{1}{2}D + j\frac{\sqrt{3}}{2}D$
(b) Single-phase-to-ground fault		$V_{Su\_pu} = D$ $V_{Sv\_pu} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$ $V_{Sw\_pu} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$
(c) Phase-to-phase short-circuit fault		$V_{Su\_pu} = 1$ $V_{Sv\_pu} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}D$ $V_{Sw\_pu} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}D$
(d) Two-phase-to-ground fault		$V_{Su\_pu} = 1$ $V_{Sv\_pu} = -\frac{1}{2}D - j\frac{\sqrt{3}}{2}D$ $V_{Sw\_pu} = -\frac{1}{2}D + j\frac{\sqrt{3}}{2}D$

TABLE II
SEQUENCE VOLTAGE AMPLITUDE DEFINITION OF DIFFERENT GRID FAULTS SCENARIOS ON *BUS* C (THE V_s IS THE RATED VOLTAGE ON *BUS* C)

Fault types	Each sequence voltage vector
(b) Single-phase-to-ground fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{D}{3} + \frac{2}{3} \\ \frac{D}{6} - \frac{1}{6} + j\left(\frac{D}{2\sqrt{3}} - \frac{1}{2\sqrt{3}}\right) \\ 0 \end{bmatrix}$
(c) Phase-to-phase short-circuit fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{D}{2} + \frac{1}{2} \\ -\frac{D}{4} + \frac{1}{4} + j\left(-\frac{\sqrt{3}D}{4} - \frac{\sqrt{3}}{4}\right) \\ 0 \end{bmatrix}$
(d) Two-phase-to-ground fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{2}{3}D + \frac{1}{3} \\ -\frac{D}{6} + \frac{1}{6} + j\left(-\frac{D}{2\sqrt{3}} + \frac{1}{2\sqrt{3}}\right) \\ 0 \end{bmatrix}$

C. *Grid fault scenarios*

Table I shows the representative grid fault voltage phasors and vectors corresponded to three-phase-to-ground fault, single-phase-to-ground fault, phase-to-phase short-circuit fault and two-phase-to-ground fault [21], [22]. It is assumed that the short-circuit faults happen somewhere on a feeder with the line impedance Z_F to *Bus* A (PCC) in Fig. 1. The line impedance from the PCC to the grid with a higher voltage level is Z_s. A voltage dip severity D is determined by the ratio of the Z_s and Z_F with positive-, negative- and zero-sequence impedance. In order to simplify the grid fault scenarios, the D is considered as a real part only and more details are explained and classified in [23], [24].

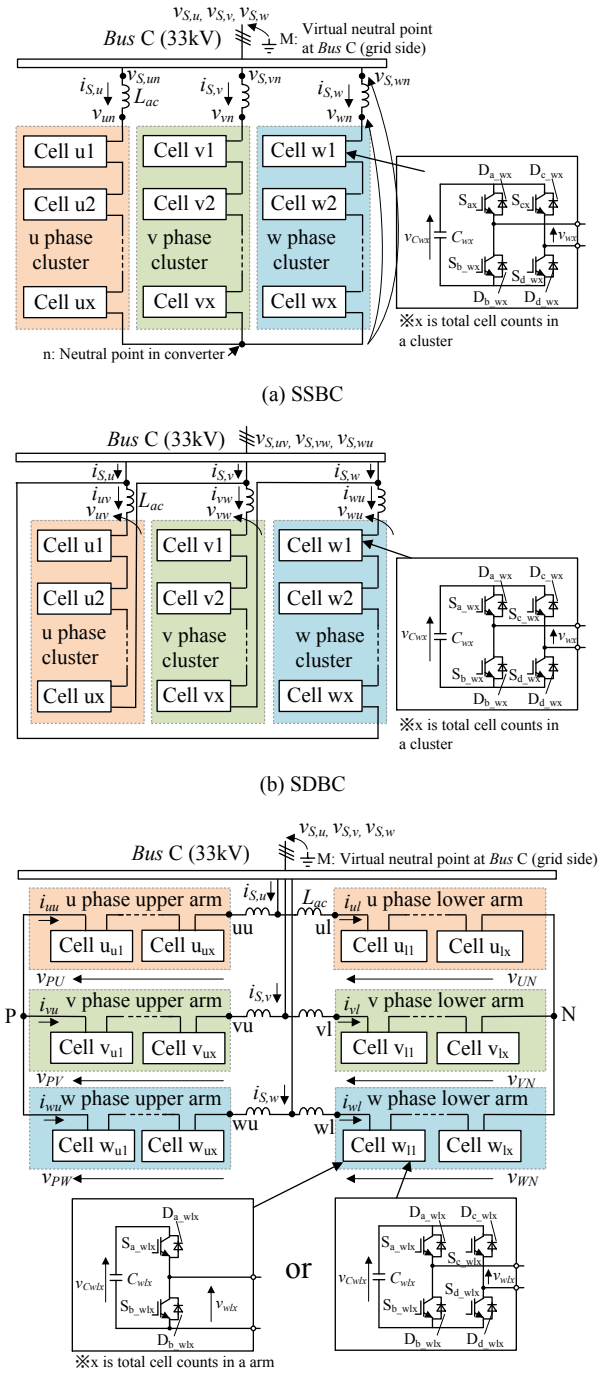


Fig. 3. Circuit configurations of the MMCC family for a STATCOM application

In this paper, three asymmetrical grid-fault scenarios are chosen as shown in Table I (b), (c) and (d). Where the asymmetrical grid fault voltage on *Bus* A propagated to *Bus* B, the *Bus* A and *Bus* B voltages do not appear significantly different due to the used neutral point grounded wye-wye-delta transformer TR1. However, the voltage on *Bus* B shows different characteristics, when it is propagated to *Bus* C, which

TABLE III
THE MMCC SPECIFICATIONS FOR THE CASE STUDY.

Circuit type of MMCC	SSBC	SDBC	DSCC	DSBC
Rated power Q_r	±80 MVA			
Rated line-to-line voltage V_s	33 kVrms (Source angular frequency ω_s : 2π×50 rad/s)			
Rated DC-link voltage each cell $V_{C,dc}$	2600 Vdc			
Nominal output voltage each cell	AC 1450 Vrms DC 0 Vdc		AC 725 Vrms DC 1300 Vdc	AC 1450 Vrms DC 0 Vdc
Equivalent switching frequency f_{eq_sw}	10 kHz (with Phase Shift PWM)			
Number of total cells N_{cell}	39 (13 cells/cluster)	69 (23 cells/cluster)	156 (26 series/arm)	78 (13 series/arm)
Number of total switching devices N_{sw}	156	276	312	312
Rated output current of each cell I_r	1400 Arms	808 Arms	700 Arms	700 Arms
Carrier frequency f_c	380 Hz	215 Hz	190 Hz	190 Hz
Total energy stored in interconnection inductor E_L	15 kJ (L_{ac} = 2.6 mH)	15 kJ (L_{ac} = 7.8 mH)	15 kJ (L_{ac} = 5.2 mH)	15 kJ (L_{ac} = 5.2 mH)
Total energy stored in dc-link capacitor E_C	1.6 MJ (C_x = 12 mF)	1.6 MJ (C_x = 7.0 mF)	6.3 MJ (C_x = 12 mF)	1.6 MJ (C_x = 6.0 mF)
IGBT module	MBN1500FH45F (4500V/1500A)	MBN900D45A (4500V/900A)	MBN800H45E2 (4500V/800A)	MBN800H45E2 (4500V/800A)

is seen by the STATCOM due to the used delta-wye transformer TR2. Table II shows the asymmetrical grid fault scenarios on *Bus* C corresponding with each grid fault. The $\dot{V}_{dq}^{+}, \dot{V}_{dq}^{-}$ and $\dot{V}^{0}$ are positive-, negative and zero-sequence component of the voltage, respectively, which are defined as scenarios used in this paper.

III. SPECIFICATIONS OF THE MMCC-STATCOMS FOR STUDY

An 80 MVar / 33 kV case study for a practical STATCOM application is chosen in this paper. Fig. 3 shows circuit configurations of the STATCOM based on MMCC with SSBC, SDBC, DSCC, and DSBC, respectively. Table III shows the specifications, the cell numbers, and key components. The design procedure is given below.

A. Basic structure and power semiconductor device

The rated DC-link voltage $V_{C,dc}$ of each converter cell in the four types of the MMCC solutions are designed to be the same at 2600 Vdc where widely used 4.5 kV IGBT modules are selected for each converter cell in this case study. The nominal output AC voltage each converter cell in the SSBC, SDBC and DSBC is designed at 1450 Vrms with the nominal modulation factor α_n = 0.8. The margin of the modulation factor (0.2) is determined by the voltage drop of the output impedance, current control dynamics, pulse width limitation due to dead time, and modular redundancy. However, the circuit configuration of the converter cell for the DSCC is chopper converter, which cannot output minus voltage. Because +/- output voltage is also required for the DSCC based STATCOM, the output voltage in each chopper converter cell is superimposed with the half value of the rated DC-voltage (i.e. 1300 Vdc). When the above design guideline is followed, the nominal output AC voltage each converter cell in the DSCC becomes AC 725 Vrms with the nominal modulation factor for AC component α_n = 0.8.

The cell converter counts N_{cell} of the MMCC solutions with SSBC, SDBC, DSCC, and DSBC are expressed by the equations in Table IV, respectively. Total number of switching devices N_{sw} for each MMCC topology is derived by each cell circuit type and N_{cell}.

Rated output currents I_r in each cell among the MMCC solutions are also expressed by the equations in Table IV, respectively. The current ratings of the IGBT modules in each of the cell converter among the MMCC solutions are selected depending on the I_r. It is worth to note that the N_{sw} and N_{cell} among the MMCC solutions are different. However, the equivalent total power semiconductor chip area calculated by the total IGBT module counts, the current capacity of each IGBT module and the rated voltage of each IGBT module, which strongly influence the total cost of the STATCOM, become same values approximately.

B. Modulation type and frequencies for PWM

Phase-shift PWM modulation is chosen because of the advantage that the electro-thermal stresses of the IGBT modules and capacitors are equally distributed among the cells in the same cluster (or arm). The equivalent switching frequency of the MMCC f_{eq_sw} is designed to be the same at 10 kHz. In this result, the carrier frequency f_c of the MMCC solutions with SSBC and SDBC are 380 Hz and 215 Hz, respectively. The carrier frequency f_c of the MMCC solutions with DSCC and DSBC are the same 190 Hz. It is noted that f_c of each MMCC solution should not be an integer multiple of the fundamental frequency in order to avoid diverging the

TABLE IV
THE KEY EQUATIONS FOR THE DESIGN OF THE MMCC SOLUTIONS

	SSBC	SDBC	DSCC	DSBC
The cell converter counts N_{cell}	$\frac{\sqrt{6}V_s}{\alpha_n V_{C,dc}}$	$\frac{3\sqrt{2}V_s}{\alpha_n V_{C,dc}}$	$\frac{4\sqrt{6}V_s}{\alpha_n V_{C,dc}}$	$\frac{2\sqrt{6}V_s}{\alpha_n V_{C,dc}}$
Rated output current of each cell I_r	$\frac{Q_r}{\sqrt{3}V_s}$	$\frac{Q_r}{3V_s}$	$\frac{Q_r}{2\sqrt{3}V_s}$	
The interconnection inductance L_{ac}	$\frac{Z_{pu}V_s^2}{\omega_S Q_r}$	$\frac{3Z_{pu}V_s^2}{\omega_S Q_r}$	$\frac{2Z_{pu}V_s^2}{\omega_S Q_r}$	
The DC-link capacitance of each cell C_x	$\frac{\sqrt{2}\alpha Q_r}{2\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}\alpha Q_r}{6\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}Q_r}{2\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}\alpha Q_r}{4\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$
Total energy stored in dc-link capacitor E_C	$\frac{\alpha Q_r}{2\alpha_n \Delta V_{C,pu}\omega_S}$		$\frac{2Q_r}{\alpha_n \Delta V_{C,pu}\omega_S}$	$\frac{\alpha Q_r}{2\alpha_n \Delta V_{C,pu}\omega_S}$

capacitor voltages among the cells when f_c is below several hundred Hz [25], [26].

C. Interconnection inductance

In this case study, the L_{ac} is designed as 6 % of the normalized impedance Z_{pu} based on 33 kV and 80 MVar operating condition of the converter. In this design rule, the L_{ac} of the MMCC solutions with SSBC, SDBC, DSCC, and DSBC is calculated by equations in Table IV, respectively. The total energy stored in the whole interconnection inductor E_L has the same value among the MMCC solutions in this designed case, which will strongly influence the total volume of the STATCOM.

D. DC-link capacitance

The DC-link capacitance of each cell C_x is designed as capacitor voltage ripple scaled by the rated DC-link voltage $V_{c,dc}$ (2600V). The voltage ripple $\Delta V_{c,pu}$ is designed to be 10% below nominal rated operation. The relationship between the voltage ripple and the capacitance C_x of the MMCC solutions with SSBC, SDBC, DSCC, and DSBC are also expressed by equations in Table IV based on an averaging model, respectively [12], [32]. Here, α is a modulation factor of a cell, which is set to be α=1 and assuming the largest voltage ripple in this case study. The total energy stored in all dc-link capacitors E_C among the MMCC solutions can be expressed as

$$E_C = \frac{N_{cell}}{2} C_x V_{C,dc}^2 \quad (1)$$

After the N_{cell}, C_x, and I_r as shown in Table IV are substituted for (1), the E_C among the MMCC solutions is updated to the formulation as shown in Table IV. It is noted that the E_C for SSBC, SDBC, and DSBC is the same. However, the E_c of the DSCC is 4 times larger than the others because of the used chopper cells. As an example, where the E_C of the DSCC is compared with the DSBC, both the N_{cell} and the C_x of the DSCC become twice higher than DSBC because of the used chopper cells with the output voltage including superimposed the half value of the rated dc-voltage $V_{C,dc}$. It should be noted that the E_C depends greatly on the total volume of the STATCOM.

IV. THEORETICAL OPERATION OF MMCC FAMILY UNDER ASYMMETRICAL REACTIVE POWER COMPENSATION

In this section, the theoretical operation of each MMCC solution is solved by a mathematical formula, focusing on the asymmetrical reactive power compensation. This analysis contributes to understanding the limitation of the asymmetrical compensation capability of the MMCC solutions. The asymmetrical three-phase systems are solved by using vector representation, where the method seems the simplest way to do it according to previous works [27-29].

A. The definition of the grid fault voltage and current on Bus C

The grid voltages and currents on *Bus* C are defined as

$$\begin{cases} v_{S,u} = V_S^+ \sin(\omega_S t) + V_S^- \sin(\omega_S t + \phi_{vn}) \\ v_{S,v} = V_S^+ \sin\left(\omega_S t - \frac{2\pi}{3}\right) + V_S^- \sin\left(\omega_S t + \phi_{vn} + \frac{2\pi}{3}\right) \\ v_{S,w} = V_S^+ \sin\left(\omega_S t + \frac{2\pi}{3}\right) + V_S^- \sin\left(\omega_S t + \phi_{vn} - \frac{2\pi}{3}\right) \end{cases} \quad (2)$$

$$\begin{cases} i_{S,u} = I_S^+ \sin(\omega_S t + \phi_{ip}) + I_S^- \sin(\omega_S t + \phi_{in}) \\ i_{S,v} = I_S^+ \sin\left(\omega_S t + \phi_{ip} - \frac{2\pi}{3}\right) + I_S^- \sin\left(\omega_S t + \phi_{in} + \frac{2\pi}{3}\right) \\ i_{S,w} = I_S^+ \sin\left(\omega_S t + \phi_{ip} + \frac{2\pi}{3}\right) + I_S^- \sin\left(\omega_S t + \phi_{in} - \frac{2\pi}{3}\right) \end{cases} \quad (3)$$

where V_S^+ is the amplitude of positive-sequence voltage, V_S^- and ϕ_{vn} are the amplitude and phase angle of negative-sequence voltage, I_S^+ and ϕ_{ip} are the amplitude and phase angle of positive-sequence current, I_S^- and ϕ_{in} are the amplitude and phase angle of negative-sequence current, respectively. After a dq transformation of (2) and (3), the grid voltage $\dot{V}_{S,dq}^+, \dot{V}_{S,dq}^-$ can be expressed as

$$\begin{cases} \dot{V}_{S,dq}^+ = V_{S,d}^+ + jV_{S,q}^+ \\ \dot{V}_{S,dq}^- = V_{S,d}^- + jV_{S,q}^- \end{cases} \quad (4)$$

The $V_{S,d}^+, V_{S,q}^+, V_{S,d}^-$ and $V_{S,q}^-$ are detected by dual-frame dq transformation scheme in an actual current controller [30]. It is noted that the $V_{S,q}^+$ has a zero value because the standard phase is set at the d-axis of the positive-sequence grid voltage by the PLL.

Similarly, the grid current $\dot{I}^{+}_{S,dq}, \dot{I}^{-}_{S,dq}$ on *Bus* C can be expressed as

$$\begin{cases} \dot{I}^{+}_{S,dq} = I^{+}_{S,d} + jI^{+}_{S,q} \\ \dot{I}^{-}_{S,dq} = I^{-}_{S,d} + jI^{-}_{S,q} \end{cases} \quad (5)$$

The $I^{+}_{S,d}, I^{+}_{S,q}, I^{-}_{S,d}$ and $I^{-}_{S,q}$ are supplied by the STATCOM. These reference values $I^{+}_{S,d,ref}, I^{+}_{S,q,ref}, I^{-}_{S,d,ref}$ and $I^{-}_{S,q,ref}$ can be defined as

$$\begin{cases} I^{+}_{S,d} = I^{+}_{S,d,ref} \equiv 0 \\ I^{+}_{S,q} = I^{+}_{S,q,ref} \\ I^{-}_{S,d} = I^{-}_{S,d,ref} \\ I^{-}_{S,q} = I^{-}_{S,q,ref} \end{cases} \quad (6)$$

where $I^{+}_{S,d,ref}$ is set to be zero value because of reactive power compensation operation. The $I^{+}_{S,q,ref}$ is given from the central control of the wind power plant under normal operation. In this result, the STATCOM has two operating modes which are inductive operation in case of $I^{+}_{S,q,ref} < 0$ and capacitive operation in case of $I^{+}_{S,q,ref} > 0$. When a grid fault happens, the additional amount of $I^{+}_{S,q,ref}$ may be required due to a recent published grid code of Transmission System Operators (TSOs). The $I^{-}_{S,d,ref}$ and $I^{-}_{S,q,ref}$ are set to be zero value according to the mentioned recent grid codes.

B. The MMCC-SSBC with zero-sequence AC voltage

Where the zero-sequence AC voltage with the same frequency as the phase-cluster current is injected, the zero-sequence voltage and the cluster current formulate the different active power between the clusters in the MMCC-SSBC. This phenomenon is used for the dc-link capacitor voltage balancing control between the phase-clusters under asymmetrical grid fault conditions, which value is solved as follows.

Each phase-cluster voltage of the MMCC-SSBC including the Back Electromotive Forces (BEFs) of the interconnection inductor L_{ac} can be expressed as

$$\begin{bmatrix} \dot{V}_{S,un} \\ \dot{V}_{S,vn} \\ \dot{V}_{S,wn} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} + \dot{V}^{0} \quad (7)$$

where $\dot{V}_{S,u}, \dot{V}_{S,v}$ and $\dot{V}_{S,w}$ are the grid voltage on *Bus* C, $\dot{V}^{0}$ is the zero-sequence voltage of the MMCC-SSBC, which is voltage difference between the point n and M as shown mentioned Fig. 3 (a). The $\dot{V}^{0}$ is defined as

$$\dot{V}^{0} = x_{SSBC} + jy_{SSBC} \quad (8)$$

where the x_{SSBC} is real part of the $\dot{V}^{0}$, the y_{SSBC} is imaginary part of the $\dot{V}^{0}$. The $\dot{V}_{S,u}, \dot{V}_{S,v}$ and $\dot{V}_{S,w}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} = \begin{bmatrix} \dot{V}^{+}_{S,dq} + \dot{V}^{-}_{S,dq} \\ \dot{V}^{+}_{S,dq} e^{-j2\pi/3} + \dot{V}^{-}_{S,dq} e^{j2\pi/3} \\ \dot{V}^{+}_{S,dq} e^{j2\pi/3} + \dot{V}^{-}_{S,dq} e^{-j2\pi/3} \end{bmatrix}$$

$$= \begin{bmatrix} (V^{+}_{S,d} + V^{-}_{S,d}) + j(V^{-}_{S,q}) \\ \left(-\frac{1}{2}V^{+}_{S,d} - \frac{1}{2}V^{-}_{S,d} - \frac{\sqrt{3}}{2}V^{-}_{S,q}\right) + j\left(-\frac{\sqrt{3}}{2}V^{+}_{S,d} + \frac{\sqrt{3}}{2}V^{-}_{S,d} - \frac{1}{2}V^{-}_{S,q}\right) \\ \left(-\frac{1}{2}V^{+}_{S,d} - \frac{1}{2}V^{-}_{S,d} + \frac{\sqrt{3}}{2}V^{-}_{S,q}\right) + j\left(\frac{\sqrt{3}}{2}V^{+}_{S,d} - \frac{\sqrt{3}}{2}V^{-}_{S,d} - \frac{1}{2}V^{-}_{S,q}\right) \end{bmatrix} \quad (9)$$

The grid currents $\dot{I}_{S,u}, \dot{I}_{S,v}, \dot{I}_{S,w}$ at *Bus* C can be expressed as

$$\begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix} = \begin{bmatrix} \dot{I}^{+}_{S,dq} + \dot{I}^{-}_{S,dq} \\ \dot{I}^{+}_{S,dq} e^{-j2\pi/3} + \dot{I}^{-}_{S,dq} e^{j2\pi/3} \\ \dot{I}^{+}_{S,dq} e^{j2\pi/3} + \dot{I}^{-}_{S,dq} e^{-j2\pi/3} \end{bmatrix}$$

$$= \begin{bmatrix} (I^{-}_{S,d}) + j(I^{+}_{S,q} + I^{-}_{S,q}) \\ \left(\frac{\sqrt{3}}{2}I^{+}_{S,q} - \frac{1}{2}I^{-}_{S,d} - \frac{\sqrt{3}}{2}I^{-}_{S,q}\right) + j\left(-\frac{1}{2}I^{+}_{S,q} + \frac{\sqrt{3}}{2}I^{-}_{S,d} - \frac{1}{2}I^{-}_{S,q}\right) \\ \left(-\frac{\sqrt{3}}{2}I^{+}_{S,q} - \frac{1}{2}I^{-}_{S,d} + \frac{\sqrt{3}}{2}I^{-}_{S,q}\right) + j\left(-\frac{1}{2}I^{+}_{S,q} - \frac{\sqrt{3}}{2}I^{-}_{S,d} - \frac{1}{2}I^{-}_{S,q}\right) \end{bmatrix} \quad (10)$$

The instantaneous active powers p_u, p_v, p_w of each phase-cluster of the MMCC-SSBC including the L_{ac} can be expressed as

$$\begin{bmatrix} p_u \\ p_v \\ p_w \end{bmatrix} = \begin{bmatrix} \frac{1}{2}\Re\left[\dot{V}^{*}_{S,un} \cdot \dot{I}_{S,u}\right] \\ \frac{1}{2}\Re\left[\dot{V}^{*}_{S,vn} \cdot \dot{I}_{S,v}\right] \\ \frac{1}{2}\Re\left[\dot{V}^{*}_{S,wn} \cdot \dot{I}_{S,w}\right] \end{bmatrix} \quad (11)$$

where $\dot{V}^{*}_{S,un}$ is the complex conjugate of the $\dot{V}_{S,un}$. By using (11), the $\dot{V}^{0}$ in order to make $p_u = p_v = p_w$, can be solved by

$$\dot{V}^{0} = \frac{V^{+}_{S,d}\left(I^{-}_{S,d}I^{-}_{S,d} - I^{-}_{S,q}I^{-}_{S,q} - I^{+}_{S,q}I^{-}_{S,q}\right) + V^{-}_{S,d}I^{+}_{S,q}\left(I^{+}_{S,q} + I^{-}_{S,q}\right) + V^{-}_{S,q}I^{+}_{S,q}I^{-}_{S,d}}{\left(I^{+}_{S,q}I^{+}_{S,q} - I^{-}_{S,d}I^{-}_{S,d} - I^{-}_{S,q}I^{-}_{S,q}\right)}$$
$$+ j\frac{V^{+}_{S,d}\left(I^{-}_{S,d}I^{-}_{S,q} + I^{-}_{S,d}I^{-}_{S,q} - I^{+}_{S,q}I^{-}_{S,d}\right) + V^{-}_{S,q}I^{+}_{S,q}\left(I^{-}_{S,q} - I^{+}_{S,q}\right) - V^{-}_{S,d}I^{+}_{S,q}I^{-}_{S,d}}{\left(I^{+}_{S,q}I^{+}_{S,q} - I^{-}_{S,d}I^{-}_{S,d} - I^{-}_{S,q}I^{-}_{S,q}\right)} \quad (12)$$

Each phase-cluster converter output voltage $\dot{V}_{un}, \dot{V}_{vn}, \dot{V}_{wn}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{un} \\ \dot{V}_{vn} \\ \dot{V}_{wn} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,un} \\ \dot{V}_{S,vn} \\ \dot{V}_{S,wn} \end{bmatrix} - \begin{bmatrix} \dot{V}_{L,u} \\ \dot{V}_{L,v} \\ \dot{V}_{L,w} \end{bmatrix} \quad (13)$$

where the $\dot{V}_{L,u}, \dot{V}_{L,v}$ *and* $\dot{V}_{L,w}$ are the BEFs of the L_{ac}. The $\dot{V}_{L,u}, \dot{V}_{L,v}$ and $\dot{V}_{L,w}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{L,u} \\ \dot{V}_{L,v} \\ \dot{V}_{L,w} \end{bmatrix} = j\omega_S L_{ac} \begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix}$$

$$= -\omega_S L_{ac} \begin{bmatrix} I^{+}_{S,q} + I^{-}_{S,q} - jI^{-}_{S,d} \\ \left(-\frac{1}{2}I^{+}_{S,q} + \frac{\sqrt{3}}{2}I^{-}_{S,d} - \frac{1}{2}I^{-}_{S,q}\right) + j\left(-\frac{\sqrt{3}}{2}I^{+}_{S,q} + \frac{1}{2}I^{-}_{S,d} + \frac{\sqrt{3}}{2}I^{-}_{S,q}\right) \\ \left(-\frac{1}{2}I^{+}_{S,q} - \frac{\sqrt{3}}{2}I^{-}_{S,d} - \frac{1}{2}I^{-}_{S,q}\right) + j\left(\frac{\sqrt{3}}{2}I^{+}_{S,q} + \frac{1}{2}I^{-}_{S,d} - \frac{\sqrt{3}}{2}I^{-}_{S,q}\right) \end{bmatrix}$$

where the resistance of the L_{ac} is neglected because the resistance is much smaller than the total impedance given by the inductance. Then maximum phase-cluster peak voltage V_{max_pu} between the three-phases standardized by peak rated phase grid voltage $\sqrt{2/3}V_S$can be expressed as

$$V_{\max\_pu} = \frac{\max(|\dot{V}_{un}|, |\dot{V}_{vn}|, |\dot{V}_{wn}|)}{\sqrt{\frac{2}{3}}V_S} \quad (15)$$

The maximum phase-cluster r.m.s current I_{max_pu} between the three-phases normalized by the rated phase current $\sqrt{2}I_r$ of the STATCOM can be expressed as

$$I_{\max\_pu} = \frac{\max(|I_u|, |I_v|, |I_w|)}{\sqrt{2}I_r} \quad (16)$$

Fig. 4 with line graphs show calculated result of the normalized maximum phase-cluster peak voltage and r.m.s current of the MMCC-SSBC under the different types of the

grid fault scenarios as a function of the voltage dip severity D using (15) and (16). The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given by the mentioned Table II. The normalized inductance of the L_{ac} is set at 6% with reference to the model mentioned in Table III. In the case of a single-phase fault, the maximum-phase-cluster peak voltage reaches the voltage saturated level of the designed STATCOM when D = 0.45. On the other hand, the maximum-phase-cluster r.m.s. current does not increase as a function of grid fault conditions. The marks in Fig. 4 indicate simulation results using PLECS software, which conditions are shown in the next chapter. The calculation values correspond reasonably well with the PLECS simulations based on the given STATCOM configurations.

C. The MMCC-SDBC with zero-sequence AC current

Where the zero-sequence AC current with the same frequency as the cluster output voltage is injected, the zero-sequence current and the cluster output voltage formulate the different active power between the clusters in the MMCC-SDBC. This phenomenon is used for the dc-link capacitor voltage balancing control among the phase-clusters under asymmetrical grid fault conditions, which value is solved as follows.

For the configuration of MMCC-SDBC, the phase-cluster current $\dot{I}_{uv}, \dot{I}_{vw}, \dot{I}_{wu}$ can be expressed as

$$\begin{bmatrix} \dot{I}_{uv} \\ \dot{I}_{vw} \\ \dot{I}_{wu} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} \dot{I}_{S,dq}^{+} e^{j\pi/6} + \dot{I}_{S,dq}^{-} e^{-j\pi/6} \\ \dot{I}_{S,dq}^{+} e^{-j\pi/2} + \dot{I}_{S,dq}^{-} e^{j\pi/2} \\ \dot{I}_{S,dq}^{+} e^{j5\pi/6} + \dot{I}_{S,dq}^{-} e^{-j5\pi/6} \end{bmatrix} + \dot{I}^0$$

$$= \begin{bmatrix} \left(x_{SDBC} - \frac{I_{S,q}^{+}}{2\sqrt{3}} + \frac{I_{S,q}^{-}}{2\sqrt{3}} + \frac{I_{S,d}^{-}}{2}\right) + j\left(y_{SDBC} + \frac{I_{S,d}^{+}}{2} + \frac{I_{S,q}^{-}}{2} - \frac{I_{S,d}^{-}}{2\sqrt{3}}\right) \\ \left(x_{SDBC} + \frac{\sqrt{3}I_{S,q}^{+}}{3} - \frac{I_{S,q}^{-}}{3}\right) + j\left(y_{SDBC} + \frac{\sqrt{3}I_{S,d}^{-}}{3}\right) \\ \left(x_{SDBC} - \frac{I_{S,q}^{+}}{2\sqrt{3}} + \frac{I_{S,q}^{-}}{2\sqrt{3}} - \frac{I_{S,d}^{-}}{2}\right) + j\left(y_{SDBC} - \frac{I_{S,d}^{+}}{2} - \frac{I_{S,q}^{-}}{2} - \frac{I_{S,d}^{-}}{2\sqrt{3}}\right) \end{bmatrix} \quad (17)$$

where $\dot{I}^0$ is the zero-sequence current circulated in the MMCC-SDBC. The $\dot{I}^0$ can be expressed as

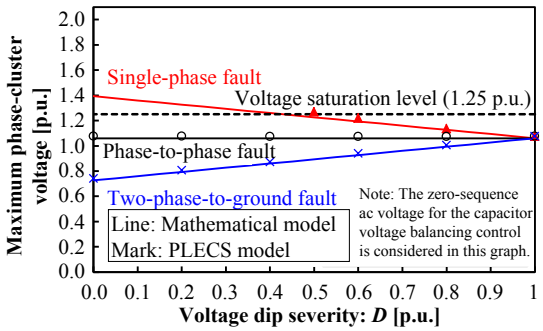
$$\dot{I}^0 = x_{SDBC} + jy_{SDBC} \quad (18)$$

where the x_{SDBC} is real part of the $\dot{I}^0$, the y_{SDBC} is imaginary part of the $\dot{I}^0$. Each line-to-line voltage $\dot{V}_{S,uv}, \dot{V}_{S,vw}, \dot{V}_{S,wu}$ of the MMCC-SDBC including the BEFs of the L_{ac} can be expressed as

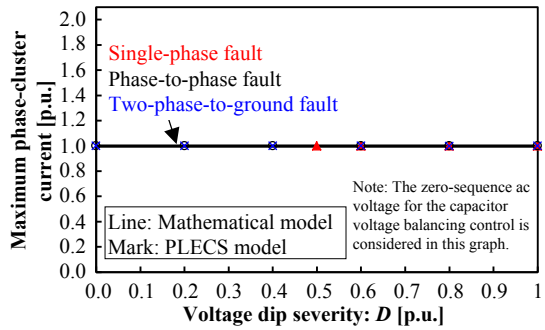
$$\begin{bmatrix} \dot{V}_{S,uv} \\ \dot{V}_{S,vw} \\ \dot{V}_{S,wu} \end{bmatrix} = \sqrt{3} \begin{bmatrix} \dot{V}_{S,dq}^{+} e^{j\pi/6} + \dot{V}_{S,dq}^{-} e^{-j\pi/6} \\ \dot{V}_{S,dq}^{+} e^{-j\pi/2} + \dot{V}_{S,dq}^{-} e^{j\pi/2} \\ \dot{V}_{S,dq}^{+} e^{j5\pi/6} + \dot{V}_{S,dq}^{-} e^{-j5\pi/6} \end{bmatrix}$$

$$= \begin{bmatrix} \frac{\sqrt{3}}{2}\left\{\left(\sqrt{3}V_{S,d}^{+} + \sqrt{3}V_{S,d}^{-} + \sqrt{3}V_{S,q}^{-}\right) + j\left(V_{S,d}^{+} - V_{S,d}^{-} + \sqrt{3}V_{S,q}^{-}\right)\right\} \\ \sqrt{3}\left\{-V_{S,q}^{-} + j\left(-V_{S,d}^{+} + V_{S,d}^{-}\right)\right\} \\ \frac{\sqrt{3}}{2}\left\{\left(V_{S,q}^{-} - \sqrt{3}V_{S,d}^{+} - \sqrt{3}V_{S,d}^{-}\right) + j\left(V_{S,d}^{+} - V_{S,d}^{-} - \sqrt{3}V_{S,q}^{-}\right)\right\} \end{bmatrix} \quad (19)$$

The $\dot{I}^0$ in order to make the instantaneous active powers between the phase-clusters to have the same value can be expressed as follows [24]:



(a) Maximum-phase-cluster peak voltage



(b) Maximum-phase-cluster r.m.s. current

Fig. 4. Maximum-phase-cluster output of the MMCC-SSBC corresponding to various grid fault scenario

$$\dot{I}^0 = \frac{I_{S,q}^{+}\left(V_{S,d}^{-}V_{S,d}^{-} - V_{S,d}^{-}V_{S,d}^{+} - V_{S,q}^{-}V_{S,q}^{-}\right) + I_{S,q}^{-}V_{S,d}^{+}\left(V_{S,d}^{+} - V_{S,d}^{-}\right) - I_{S,d}^{-}V_{S,d}^{+}V_{S,q}^{-}}{\sqrt{3}\left(V_{S,d}^{-}V_{S,d}^{-} - V_{S,d}^{+}V_{S,d}^{+} + V_{S,q}^{-}V_{S,q}^{-}\right)}$$
$$+ j\frac{I_{S,q}^{+}\left(V_{S,d}^{-}V_{S,q}^{-} + V_{S,d}^{-}V_{S,q}^{-} + V_{S,d}^{+}V_{S,q}^{-}\right) + I_{S,d}^{-}V_{S,d}^{+}\left(V_{S,d}^{+} + V_{S,d}^{-}\right) - I_{S,q}^{-}V_{S,d}^{+}V_{S,q}^{-}}{\sqrt{3}\left(V_{S,d}^{-}V_{S,d}^{-} - V_{S,d}^{+}V_{S,d}^{+} + V_{S,q}^{-}V_{S,q}^{-}\right)} \quad (20)$$

Each phase-cluster converter output voltage $\dot{V}_{uv}, \dot{V}_{vw}, \dot{V}_{wu}$ of the MMCC-SDBC can be expressed as

$$\begin{bmatrix} \dot{V}_{uv} \\ \dot{V}_{vw} \\ \dot{V}_{wu} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,uv} \\ \dot{V}_{S,vw} \\ \dot{V}_{S,wu} \end{bmatrix} - \begin{bmatrix} \dot{V}_{L,uv} \\ \dot{V}_{L,vw} \\ \dot{V}_{L,wu} \end{bmatrix} \quad (21)$$

where the $\dot{V}_{L,uv}, \dot{V}_{L,vw}$ and $\dot{V}_{L,wu}$ are the BEFs of the L_{ac}. The $\dot{V}_{L,uv}, \dot{V}_{L,vw}$ and $\dot{V}_{L,wu}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{L,uv} \\ \dot{V}_{L,vw} \\ \dot{V}_{L,wu} \end{bmatrix} = j\omega_S L_{ac} \begin{bmatrix} \dot{I}_{S,uv} \\ \dot{I}_{S,vw} \\ \dot{I}_{S,wu} \end{bmatrix}$$

$$= -\omega_S L_{ac} \begin{bmatrix} \left(y_{SDBC} + \frac{I_{S,q}^{+}}{2} + \frac{I_{S,q}^{-}}{2} - \frac{I_{S,d}^{-}}{2\sqrt{3}}\right) + j\left(-x_{SDBC} + \frac{I_{S,d}^{+}}{2\sqrt{3}} - \frac{I_{S,q}^{-}}{2\sqrt{3}} - \frac{I_{S,d}^{-}}{2}\right) \\ \left(y_{SDBC} + \frac{\sqrt{3}I_{S,d}^{-}}{3}\right) + j\left(-x_{SDBC} - \frac{\sqrt{3}I_{S,q}^{+}}{3} + \frac{I_{S,q}^{-}}{3}\right) \\ \left(y_{SDBC} - \frac{I_{S,q}^{+}}{2} - \frac{I_{S,q}^{-}}{2} - \frac{I_{S,d}^{-}}{2\sqrt{3}}\right) + j\left(-x_{SDBC} + \frac{I_{S,d}^{+}}{2\sqrt{3}} - \frac{I_{S,q}^{-}}{2\sqrt{3}} + \frac{I_{S,d}^{-}}{2}\right) \end{bmatrix} \quad (22)$$

where the resistance of the L_{ac} is neglected. The maximum-phase-cluster peak voltage and r.m.s. current of the MMCC-SDBC can be calculated in the same way as the MMCC-SSBC.

Fig. 5 with line graphs show the normalized maximum-phase-cluster peak voltage and r.m.s. current of the MMCC-SDBC under the different types of the grid fault scenarios in respect to the voltage dip severity D. The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is

given by the mentioned Table II. The normalized inductance of L_{ac} is set at 6% with reference to the model mentioned in Table III. It is noted that the maximum-phase-cluster peak voltage does not increase regarding grid fault conditions. The maximum-phase-cluster r.m.s. current increases rapidly when $D < 0.5$ below under the phase-to-phase short-circuit fault and two-phase-to-ground fault, and reach the over current level (1.25) decided by over junction temperature of the IGBT model, which will be discussed in the next chapter. When D approaches 0 under these faults, the current approaches to infinity value while the denominator of the (20) is close to zero. When D is zero under these fault voltages, there is no solution of the zero-sequence current, and it is claimed to be the major problem of the MMCC-SDBC for the STATCOM application [9], [29]. The marks in Fig. 5 indicate simulation results using PLECS software and the condition is shown next chapter. The calculation values correspond reasonably well with the PLECS simulation values based on the practical scaled STATCOM model.

D. The MMCC-DSCC with circulating DC current and DC voltage between terminal P and N

The DSCC has two neutral points P and N in each single star connection. The differential voltage V_{PN} between P and N is normally 50 % of the rated dc-link voltage each converter cell in the DSCC in order to output AC voltage using the chopper converter cells. Where the circulating dc current is injected in each leg of the DSCC, the circulating current and the V_{PN} formulate the independent active power between the legs in the MMCC-DSCC. This phenomenon is used for the dc-link capacitor voltage balancing control among the legs under asymmetrical grid fault conditions, which value is solved as follows.

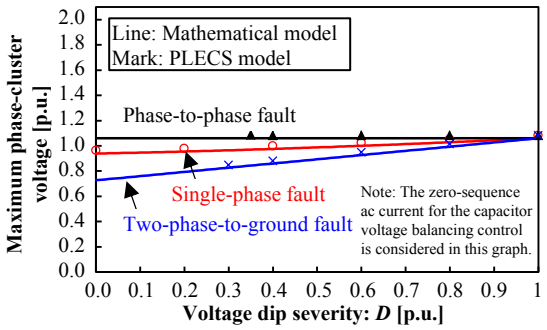
The instantaneous active power on αβ0 frame $p_{S,\alpha}$, $p_{S,\beta}$, $p_{S,0}$ of the MMCC-DSCC arising from asymmetrical reactive power supply can be expressed as

$$\begin{bmatrix} p_{S,\alpha} \\ p_{S,\beta} \\ p_{S,0} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} \frac{1}{2}\Re\left[\dot{V}_{S,u}^{*} \cdot \dot{I}_{S,u}\right] \\ \frac{1}{2}\Re\left[\dot{V}_{S,v}^{*} \cdot \dot{I}_{S,v}\right] \\ \frac{1}{2}\Re\left[\dot{V}_{S,w}^{*} \cdot \dot{I}_{S,w}\right] \end{bmatrix} \tag{23}$$

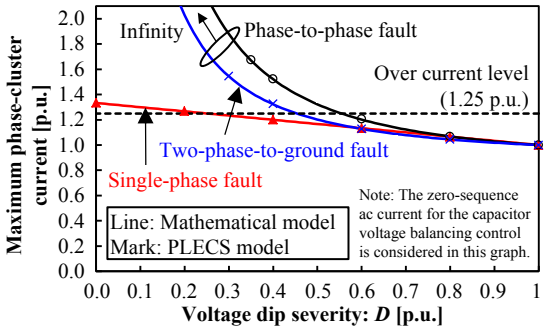
where the $\dot{V}_{S,u}, \dot{V}_{S,v}$ and $\dot{V}_{S,w}$, are the same as (9), the $\dot{I}_{S,u}$, $\dot{I}_{S,v}$ and $\dot{I}_{S,w}$ are the same as (10). It is noted that the $p_{S,\alpha}$and $p_{S,\beta}$ are the instantaneous active power imbalances among the phases. The $p_{S,0}$ shows the instantaneous active power of the three-phase MMCC-DSCC. Normally, each converter cell of the MMCC-DSCC has injected dc-bias voltage with 50% of modulation factor in order to output AC (+/-) voltage using chopper cells which dc-bias voltage appears to be the differential voltage V_{PN} between P and N terminal. The V_{PN} can be expressed as

$$V_{PN} = 2\sqrt{\frac{2}{3}}V_s\alpha_{mgn} \tag{24}$$

where α_{mgn} is the ratio between maximum converter output voltage and rated grid voltage and as a used design margin. The circulating currents of each of the leg $i_{z,u}$, $i_{z,v}$ and $i_{z,w}$ can be expressed as



(a) Maximum-phase-cluster peak voltage



(b) Maximum-phase-cluster r.m.s. current

Fig. 5. Maximum-phase-cluster output of the MMCC-SDBC corresponding to various grid fault scenario

$$\begin{bmatrix} i_{z,u} \\ i_{z,v} \\ i_{z,w} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} i_{uu} + i_{ul} \\ i_{vu} + i_{vl} \\ i_{wu} + i_{wl} \end{bmatrix} \tag{25}$$

Based on (23) and (24), the circulating currents to cancel out the instantaneous active power imbalance among the phases arising by the asymmetrical reactive power output operation can be expressed as

$$\begin{bmatrix} i_{z,u} \\ i_{z,v} \\ i_{z,w} \end{bmatrix} = \frac{1}{V_{PN}}\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} P_{S,\alpha} \\ P_{S,\beta} \end{bmatrix} \tag{26}$$

The AC component of each arm output voltages $\dot{V}_{PU,ac}$, $\dot{V}_{PV,ac}$, $\dot{V}_{PW,ac}$, $\dot{V}_{NU,ac}$, $\dot{V}_{NV,ac}$ and $\dot{V}_{NW.ac}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{PU,ac} \\ \dot{V}_{PV,ac} \\ \dot{V}_{PW,ac} \\ \dot{V}_{UN,ac} \\ \dot{V}_{VN,ac} \\ \dot{V}_{WN,ac} \end{bmatrix} = \begin{bmatrix} -\dot{V}_{S,u} \\ -\dot{V}_{S,v} \\ -\dot{V}_{S,w} \\ \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} - \begin{bmatrix} \dot{V}_{L,uu} \\ \dot{V}_{L,vu} \\ \dot{V}_{L,wu} \\ \dot{V}_{L,ul} \\ \dot{V}_{L,vl} \\ \dot{V}_{L,wl} \end{bmatrix} \tag{27}$$

where the $\dot{V}_{L,uu}, \dot{V}_{L,vu}, \dot{V}_{L,wu}, \dot{V}_{L,ul}, \dot{V}_{L,vl}$ *and* $\dot{V}_{L,wl}$ are BEFs of the L_{ac}. The $\dot{V}_{L,uu}$, $\dot{V}_{L,vu}$, $\dot{V}_{L,wu}$, , $\dot{V}_{L,ul}$, $\dot{V}_{L,vl}$ and $\dot{V}_{L,wl}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{L,ul} \\ \dot{V}_{L,vl} \\ \dot{V}_{L,wl} \end{bmatrix} = -\begin{bmatrix} \dot{V}_{L,uu} \\ \dot{V}_{L,vu} \\ \dot{V}_{L,wu} \end{bmatrix} = j\frac{\omega_S L_{ac}}{2}\begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} \dot{V}_{L,u} \\ \dot{V}_{L,v} \\ \dot{V}_{L,w} \end{bmatrix} \tag{28}$$

where the resistance of the L_{ac} is neglected. The $\dot{V}_{L,u}, \dot{V}_{L,v}$ and $\dot{V}_{L,w}$ were given in (14). The maximum arm output peak voltage V_{max_pu} between the arm-converters normalized by rated grid voltage $\sqrt{2/3}V_S$ can be expressed as

$$V_{\max\_pu} = \frac{V_{PN}+\max(|\dot{V}_{PU,ac}|,|\dot{V}_{PV,ac}|,|\dot{V}_{PW,ac}|,|\dot{V}_{UN,ac}|,|\dot{V}_{VN,ac}|,|\dot{V}_{WN,ac}|)}{\sqrt{\frac{2}{3}}V_S} \quad (29)$$

Each arm output r.m.s. current $i_{uu,rms}$, $i_{vu,rms}$, $i_{wu,rms}$, $i_{ul,rms}$, $i_{vl,rms}$ and $i_{wl,rms}$ can be expressed as

$$\begin{bmatrix} i_{uu,rms} \\ i_{vu,rms} \\ i_{wu,rms} \end{bmatrix} = \begin{bmatrix} i_{ul,rms} \\ i_{vl,rms} \\ i_{wl,rms} \end{bmatrix} = \begin{bmatrix} \sqrt{\left(\frac{|i_{S,u}|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,u}}{2}\right)^2} \\ \sqrt{\left(\frac{|i_{S,v}|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,v}}{2}\right)^2} \\ \sqrt{\left(\frac{|i_{S,w}|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,w}}{2}\right)^2} \end{bmatrix} \quad (30)$$

The maximum arm output r.m.s current I_{max_pu} normalized by the rated arm current of the STATCOM $1/2I_r$ can be expressed as

$$I_{\max\_pu} = \frac{\max(i_{uu,rms},i_{vu,rms},i_{wu,rms})}{I_r/2} \quad (31)$$

Fig. 6 with line graphs show the calculated result of the normalized maximum arm output peak voltage and r.m.s. current of the MMCC-DSCC under the different types of the grid fault scenarios regarding of the voltage dip severity D by using (29) and (31). The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given by the mentioned Table II. The normalized inductance of L_{ac} is set to be 6%, the α_{mgn} is set at 1.127 with reference to the practical scale model in mentioned Table III. It is noted that the maximum arm output peak voltage and r.m.s current do not increase significantly under different grid fault conditions. The marks in Fig. 6 plot the simulation result using the PLECS software, which simulation conditions are shown in the next chapter. The calculated values correspond reasonably well with the PLECS simulation values based on the practical scaled STATCOM model.

E. The MMCC-DSBC with circulating DC current and DC voltage between terminal P and N

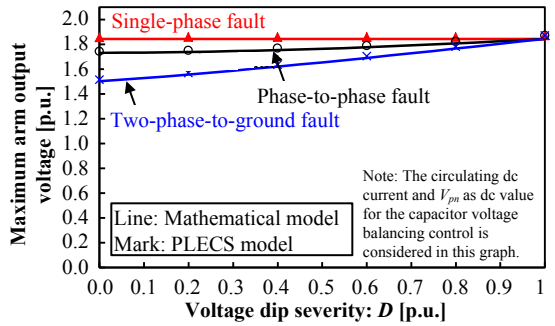
The operation principle of the MMCC-DSBC is almost the same as the MMCC-DSCC. The only difference is the amplitude of the V_{PN}. In the case of the MMCC-DSBC, each of the arms is able to supply AC (+/-) voltage without the V_{PN} because of the used H-Bridge converter cells. However, due to the voltage balancing control, the V'_{PN} is required, which can be expressed as

$$V'_{PN} = \alpha_{DSBC}V_{PN} \quad (32)$$

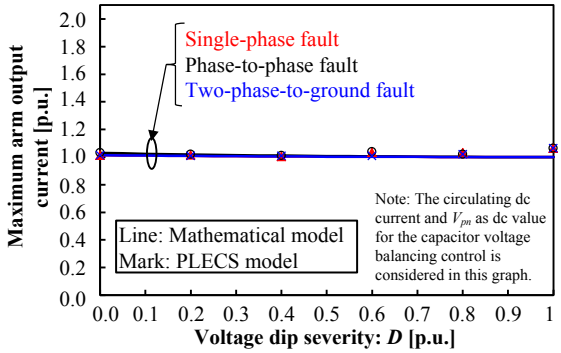
where α_{DSBC} is the amplitude ratio of the differential voltage between terminal P and N of the DSCC to the DSBC. The injectable α_{DSBC} is normally less than 20% in order to avoid the voltage saturation when the DSBC is designed practically. The Maximum value of the α_{DSBC} considering the grid fault condition can be expressed as

$$\alpha_{DSBC} = \frac{\sqrt{\frac{2}{3}}V_s\alpha_{mgn}-\max(|\dot{V}_{PU,ac}|,|\dot{V}_{PV,ac}|,|\dot{V}_{PW,ac}|,|\dot{V}_{UN,ac}|,|\dot{V}_{VN,ac}|,|\dot{V}_{WN,ac}|)}{\sqrt{\frac{2}{3}}V_s\alpha_{mgn}} \quad (33)$$

where the $\dot{V}_{PU,ac}, \dot{V}_{PV,ac}, \dot{V}_{PW,ac}, \dot{V}_{UN,ac}, \dot{V}_{VN,ac}$ and $\dot{V}_{WN,ac}$ were mentioned in (27). It is noted that the circulating dc current of the DSBC becomes larger than the DSCC because the V_{PN}' for the DSBC becomes smaller than the DSCC. The maximum arm

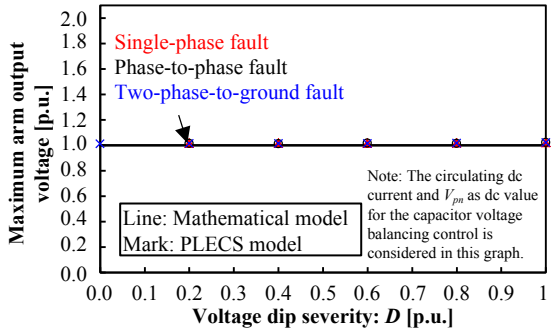


(a) Maximum arm output peak voltage

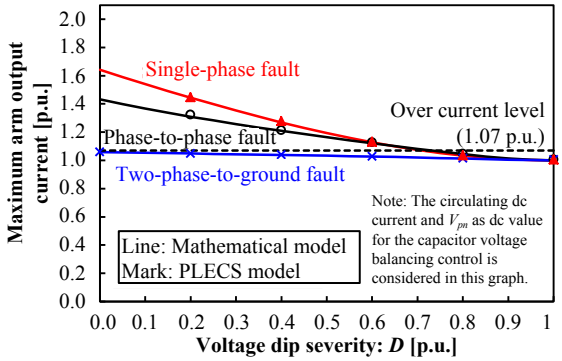


(b) Maximum arm output r.m.s. current

Fig. 6. Maximum arm output of the MMCC-DSCC corresponding to various grid fault scenario



(a) Maximum arm output peak voltage



(b) Maximum arm output r.m.s. current

Fig. 7. Maximum arm output of the MMCC-DSBC corresponding to various grid fault scenario

output voltage and current can be solved in the same way as the MMCC-DSCC.

Fig. 7 with line graphs show the calculated result of the normalized maximum arm output peak voltage and r.m.s. current of the MMCC-DSBC under the different types of the grid fault scenarios in respect to the voltage dip severity *D*. The I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given by the mentioned Table II. The normalized inductance of L_{ac} is set to 6%, the α_{mgn} is set at 1.127 with reference to the practical scale model given in Table III. The marks are the practical scaled simulation results, which test conditions will be shown next chapter. It is noted that the maximum arm peak voltage tracks 1 p.u. by the injected V'_{PN} as the designed maximum value. The maximum arm r.m.s. current increases moderate in respect to the *D*, but reach the over current level (1.07) which is decided by the over junction temperature of the IGBT module, which is shown next chapter. The arm current becomes larger than the DSCC because of lower the V'_{PN}. The over current level becomes lower than the SDBC because the current distribution between the IGBT modules in a converter cell increases by injected dc voltage and current for the capacitor voltage balancing method. The marks in Fig. 7 show the simulation result using PLECS software, which conditions are given in the next chapter. The calculated values correspond reasonably well with the PLECS simulation values based on practical scale STATCOM model.

V. Performance Benchmark of MMCC Solutions

A. Electrical and thermal simulation modeling

In this paper, the LVRT capability of a STATCOM which is based on the MMCC with SSBC, SDBC, DSCC, and DSBC is simulated by using the software PLECS. The three types of grid fault voltage are given by the mentioned voltage vector as shown in Table II. The voltage is applied at the *Bus* B side of the TR2 as shown in mentioned Fig. 2, as discussed in section II. In order to fix the standard voltage vectors applied to the MMCC, the impedance of the TR2 is neglected. The specifications of the MMCC with SSBC, SDBC, and DSCC are assembled based on the parameter in Table III. The reactive current reference is set to rated 1 p.u. of the positive-sequence only as recent grid codes do not require negative sequence current to compensate for the asymmetrical grid voltage.

The modulation scheme for the MMCC with SSBC, SDBC, DSCC, and DSBC are selected widely-used Phase Shift PWM as mentioned in sub-section III-B. The output current is controlled by a dual-frame control scheme with sequence decoupling using a notch filter [30]. The capacitor voltage control method for SSBC is selected [11] with a zero-sequence AC voltage injection. The capacitor voltage control method for SDBC is selected [12] with a zero-sequence AC current injection. The capacitor voltage control method for DSCC is selected [13] with a circulating DC currents injection method. The capacitor voltage control method for DSBC is selected [15] using a circulating DC current injection method.

The electrical losses and junction temperatures on each power semiconductor module are simulated by thermal simulation function on the PLECS. The electrical losses of the power semiconductor modules consist of the conduction loss of the IGBTs, turn on / off loss of the IGBTs, conduction loss of the Diodes, and recovery loss of the Diodes in the power modules. The electrical loss parameters depending on the flowing currents, applied voltages, and junction temperatures are selected from the datasheets for the power modules in mentioned Table III [31]. The thermal network between the power semiconductor chip and heatsink for power module are constructed by Foster RC network as shown in Fig. 8. Here, p_S is power loss of IGBT chip; p_D is power loss of Diode chip; T_{S_j} is junction temperature of IGBT; T_{D_j} is junction temperature of Diode; T_c is the case temperature in the power semiconductor module; T_h is heat sink temperature; $R_S(j\text{-}cn)$, $\tau_D(j\text{-}cn)$, $R_S(j\text{-}cn)$ and $\tau_D(j\text{-}cn)$ are thermal parameters for the Foster RC network of the power semiconductor module (n:1-4). The thermal impedances of the power modules are also selected from the datasheets. The heat sink temperature based on liquid cooling system is considered as a constant value at 60 ℃ in this simulation model because the temperature of the heatsink is normally much lower and more stable compared with the junction temperature in a properly designed converter system.

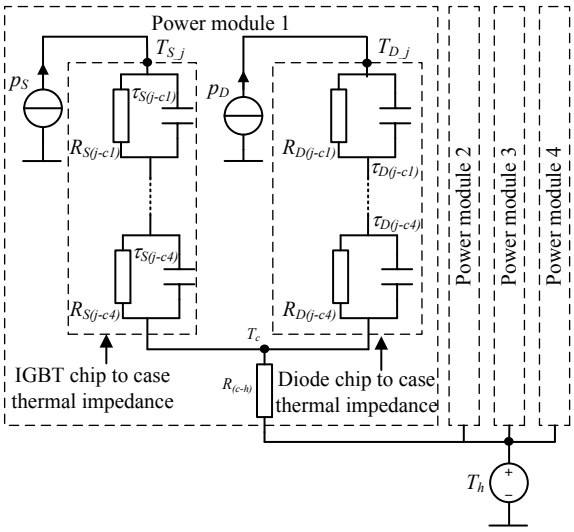


Fig. 8. Thermal network between power semiconductor chip and heat sink on each cell converter.

B. Electrical and thermal simulation of the MMCC-SSBC

Fig. 9 shows the key waveforms of the MMCC-SSBC under the single-phase-to-ground fault with the dip severity *D* of 0.5 p.u.. It can be seen that the peak value of the voltage reference increases by 22% maximum on w phase cluster under the single-phase-to-ground fault in order to inject zero-sequence voltage v_{zero} to balance the DC-link capacitor voltages of the converter cells. Here, the injected zero-sequence voltage is expressed by (34) when all capacitor voltages are balanced.

$$v^*_{zero} = \frac{v^*_{u1} + v^*_{v1} + v^*_{w1}}{3} \tag{34}$$

Fig. 10 shows the junction temperatures of four IGBTs and diodes in each cell of u1, v1 and w1 under the same simulation conditions. The peak junction temperature of the IGBT and Diode are the same, 115℃ and 109℃ respectively among the different cluster cells. The temperatures are below the limit of 128 ℃ by considering a 15 % margin for the IGBT modules

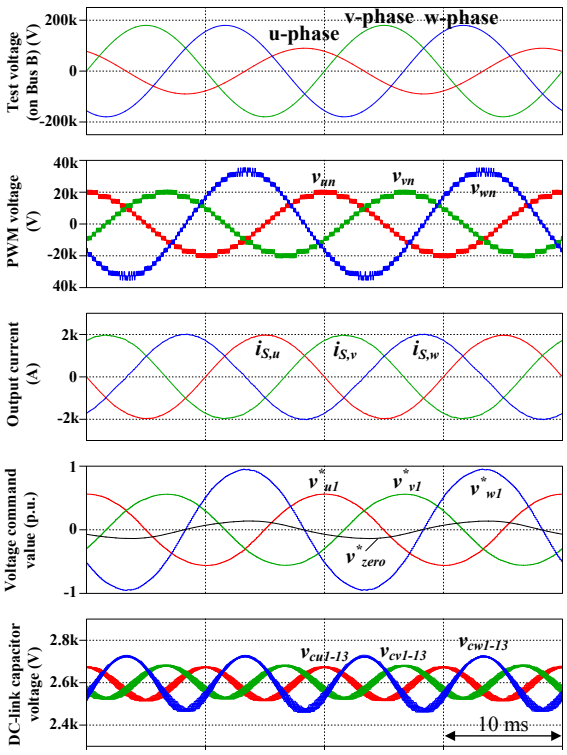
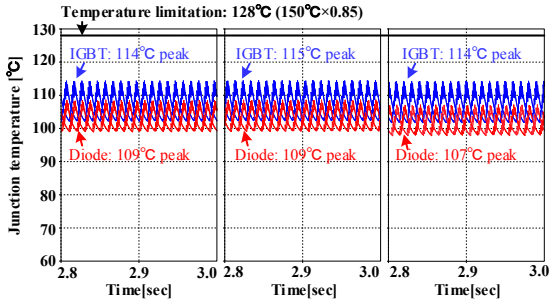


Fig. 9. Key waveforms of the MMCC-SSBC under single-phase fault with a dip severity D of 0.5 p.u.



(a) u1-cell (b) v1-cell (c) w1-cell

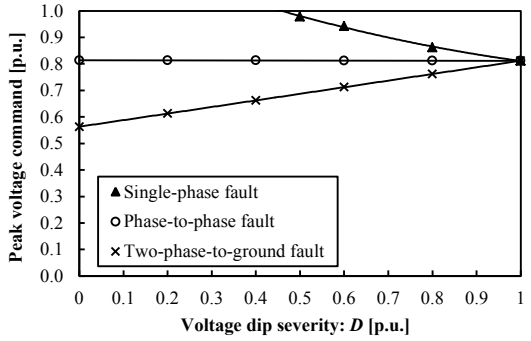
Fig. 10. Thermal distribution of the MMCC-SSBC under single-phase fault with dip severity D of 0.5 p.u.

with the absolute maximum rating of the junction temperature defined by the manufacturers.

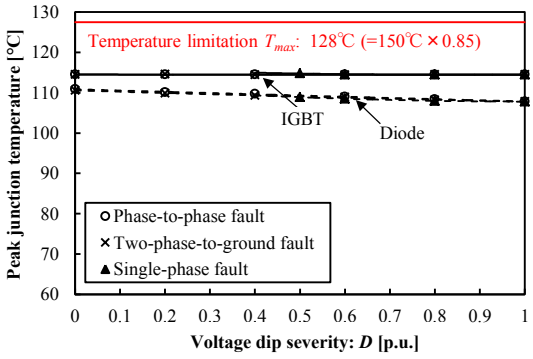
Fig. 11 shows the maximum peak voltage command and the peak junction temperature of the IGBT and Diode among the cells in respect to the dip severity D under various grid fault scenarios. It can be noted that the peak voltage command saturates with the single-phase-to-ground fault at D = 0.5 p.u.. The maximum peak junction temperature of the IGBT and Diode are approximately 115 °C and 109 °C, respectively, regardless the grid conditions.

C. *Electrical and thermal simulation of the MMCC-SDBC*

Fig. 12 shows the simulated key waveforms of the MMCC-SDBC under the phase-to-phase fault with the dip severity D = 0.4 p.u.. It can be noted that the peak value of the cluster current increases by maximum 52% at the v and w cluster under the phase-to-phase fault in order to inject zero-sequence current i_{zero} to balance the DC-link capacitor



(a) Peak voltage command



(b) Peak junction temperature

Fig. 11. Electrical-thermal simulations of the MMCC-SSBC at different dip severities.

voltages of the converter cells. Here, the injected zero-sequence current is expressed by (35).

$$i_{zero} = \frac{i_{uv} + i_{vw} + i_{wu}}{3} \tag{35}$$

Fig. 13 shows the junction temperatures of four IGBTs and diodes in the cells u1, v1, and w1 under the same condition. The peak junction temperatures increase to maximum 121℃ and 114℃ at the diodes and IGBTs of the v1 and w1 cells. These temperatures are over the limit of 106℃ by considering a 15 % margin for the IGBT modules with the absolute maximum rating of junction temperature defined by the manufacturer.

Fig. 14 shows the maximum peak voltage command and peak junction temperature among the cells for different dip severities D under the various grid fault scenarios. It can be noted that the peak voltage command does not saturate in the various grid fault scenarios. The peak junction temperatures increase quickly with phase-to-phase fault and two-phase-to-ground fault conditions and reach an upper limit temperature of 106℃ when the voltage dip is 0.55 and 0.45 p.u., respectively.

D. *Electrical and thermal simulation of the MMCC-DSCC*

Fig. 15 shows the simulated key waveforms of the MMCC-DSCC under the phase-to-phase fault with dip severity D = 0 p.u.. It can be noted that the arm currents (i.e. i_{uu}, i_{ul}, i_{vu}, i_{vl}, i_{wu}, and i_{wl}) contain both half value of the output phase current and the circulating DC current i_{zu}, i_{zv} and i_{zw} for the dc-link capacitor voltage balancing under asymmetrical grid fault conditions. Here, the circulating current is defined as

$$i_{Zu} = \frac{i_{uu} + i_{ul}}{2},\ i_{Zv} = \frac{i_{vu} + i_{vl}}{2},\ i_{Zw} = \frac{i_{wu} + i_{wl}}{2} \tag{36}$$

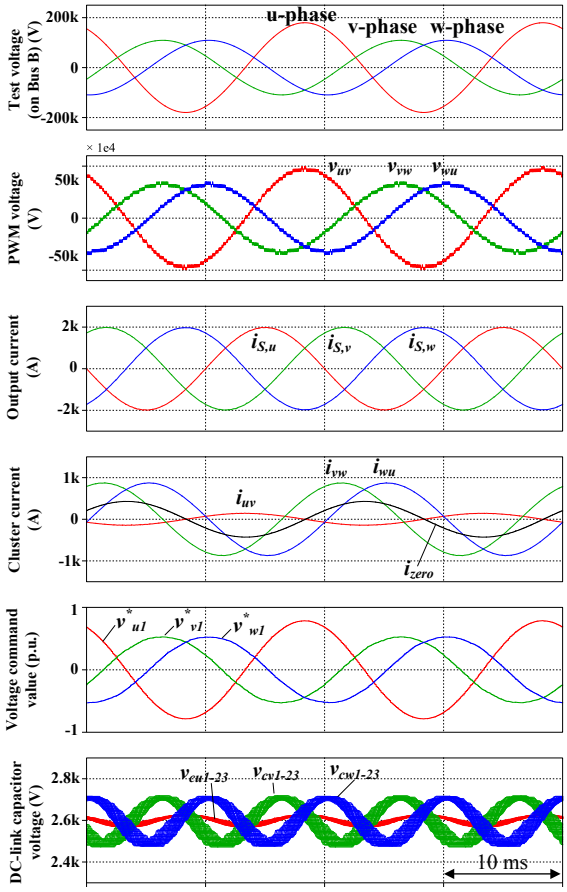
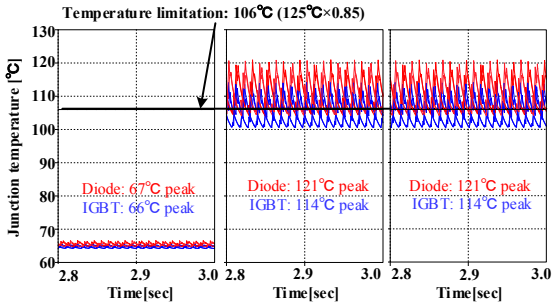


Fig. **12** Key waveforms of the MMCC-SDBC under phase-to-phase fault with a dip severity *D* of 0.4 p.u.

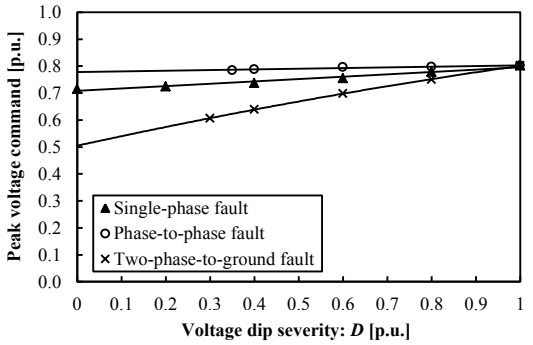


(a) u1-cell (b) v1-cell (c) w1-cell

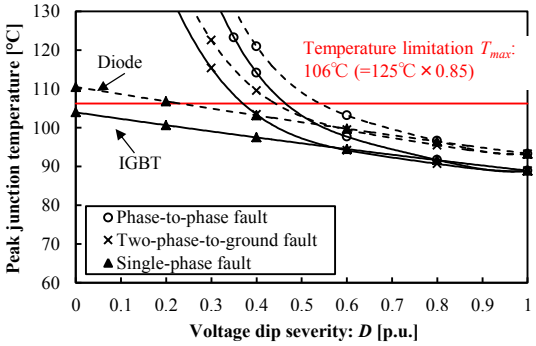
Fig. 13. Thermal distribution of the MMCC-SDBC under phase-to-phase fault with the dip severity *D* of 0.4 p.u.

It is noted that the r.m.s. value of the arm current increases by only a few % under the phase-to-phase fault.

Fig. 16 shows the junction temperatures of IGBTs and diodes in the chopper converter cells uu1, vu1, wu1, ul1, vl1 and wl1 under the same condition. The junction temperatures are widely distributed among the arms compared with the other MMCC types because the chopper converter cells are used with different modulation factor among the arms. The peak junction temperature increases to maximum 104 ℃ at the diodes of u1 cells. This temperature is below the limit of 106 ℃ by considering a 15 % margin for the IGBT modules with the absolute maximum rating of junction temperature defined by the manufacturer.



(a) Peak voltage command



(b) Peak junction temperature

Fig. 14. Electrical-thermal simulations of the MMCC-SDBC at different dip severities

Fig. 17 shows the maximum peak voltage command value and peak junction temperature among the arms regarding the voltage dip severity *D* under the various grid fault scenarios. It can be noted that the peak voltage command does not saturate in the various grid fault scenarios. The peak junction temperature does not reach the temperature limitation in the various grid fault scenarios.

E. Electrical and thermal simulation of the MMCC-DSBC

Fig. 18 shows the simulated key waveforms of the MMCC-DSBC under the single-phase-to-ground fault with dip severity $D = 0.4$ p.u.. It can be noted that the arm currents and PWM output voltage of each arm contain the dc component as well as the DSCC. However, the amplitude of the PWM output voltage with dc-component is smaller than the DSCC because of avoiding the voltage saturation of each cell output voltage command. In this result, the circulating DC current increases for the capacitor voltage balancing control.

Fig. 19 shows the junction temperatures of IGBTs and diodes in the chopper converter cells uu1, vu1, wu1, ul1, vl1 and wl1 under the same conditions. The junction temperatures are widely distributed among the arms compared with the MMCC-SDBC because injected dc-component with different modulation factor among the arms. The peak junction temperature increases to maximum 104 ℃ at the diodes of uu1 cells. This temperature is below the limit of 106 ℃ by considering a 15 % margin for the IGBT modules with the absolute maximum rating of junction temperature which is defined by the manufacturer.

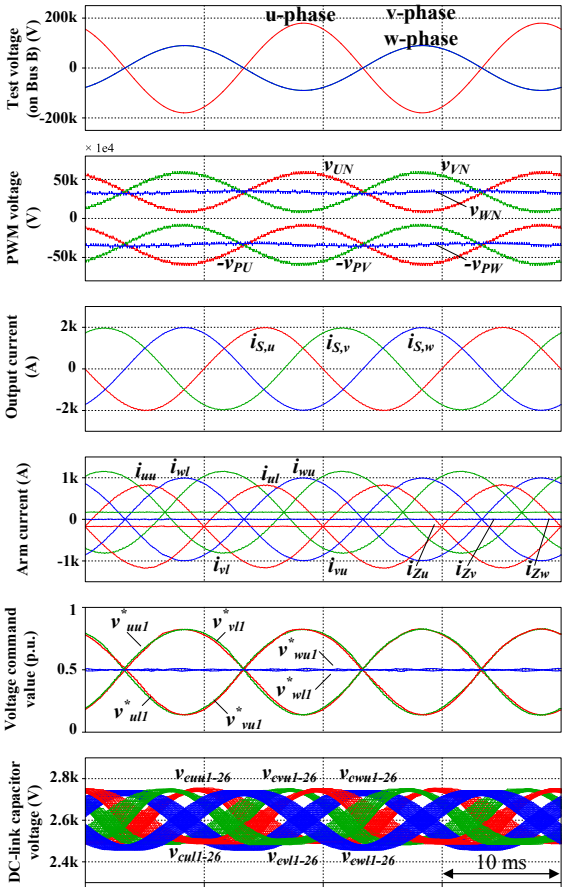


Fig. 15. Key waveforms of the MMCC-DSCC under phase-to-phase fault with a dip severity *D* of 0 p.u.

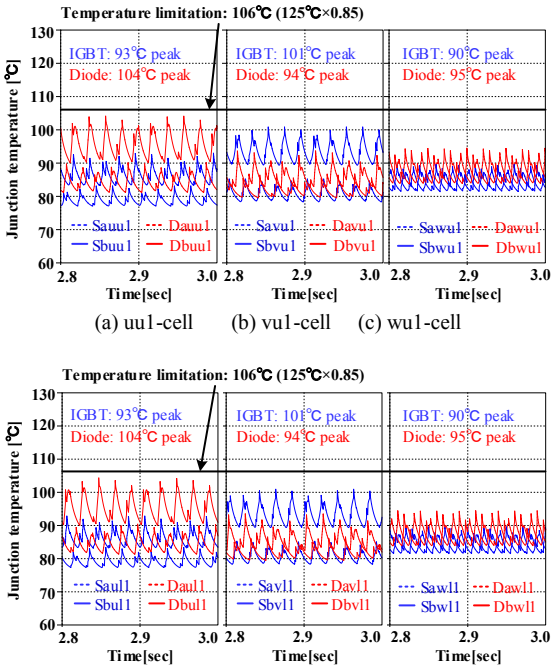


Fig. 16. Thermal distribution of the MMCC-DSCC under phase-to-phase fault with a dip severity *D* of 0 p.u.

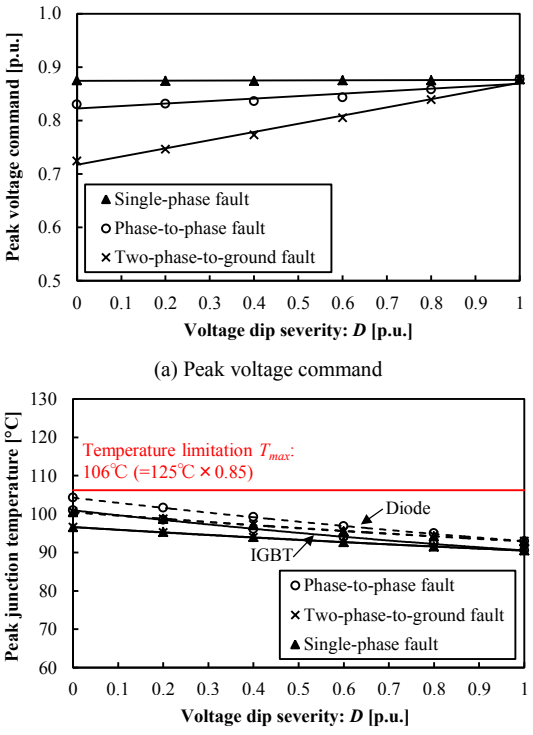


Fig. 17. Electrical-thermal simulations of the MMCC-DSCC at different dip severities

Fig. 20 shows the maximum peak voltage command value and peak junction temperature among the arms regarding dip severity *D* under the various grid fault scenarios. It can be noted that the peak voltage command keeps same value under the various grid fault conditions with the different voltage dip severity because the VPN is injected maximum value to minimize the amplitude of the circulating DC current. The peak junction temperatures exceed the limitation value when *D* is lower than 0.6. However, the slope is moderate compared with the SDBC.

F. Performance Comparison between the MMCC family

Fig. 21 (a) shows the reactive current compensation capability for the MMCC solutions with SSBC, SDBC, DSCC and DSBC to enable a proper voltage-balancing under the different dip severity *D* with various grid faults. The compensation capability limits of MMCC family are determined by the modulation saturation point and maximum junction temperature. The (b) and (c) plot the peak voltage command and peak junction temperature of the IGBT modules in the whole converter cells corresponding to the operating conditions on the (a). The peak voltage command and junction temperature are normalized by instantaneous dc-link voltage each cell converter and temperature limitation value decided by the manufacturer as mentioned in the sub-section V-B, C, and D. The MMCC family can continue to supply the rated reactive current when the dip severity of the grid voltage is higher than 0.7 p.u., but the reactive current compensation capability shows different characteristics for the dip severity lower than 0.7 p.u. as discussed below.

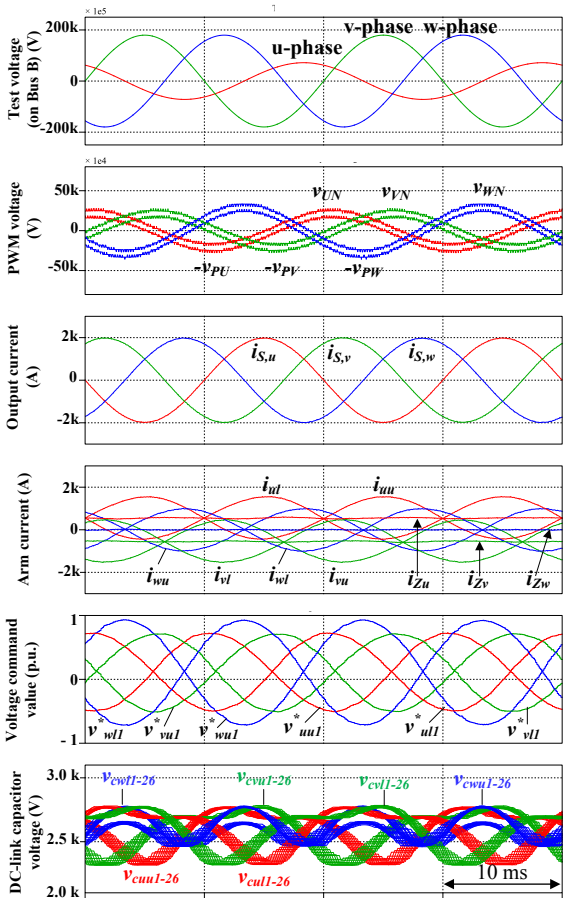


Fig. 18. Key waveforms of the MMCC-DSBC under single-phase-to-ground fault with a dip severity *D* of 0.4 p.u.

1) The MMCC-SSBC: It reveals that the SSBC can supply the rated reactive current under phase-to-phase fault and two-phase-to-ground fault condition regardless of the dip severity. However, the reactive current capability decreases steeply at a voltage dip severity of 0.4 p.u. under single-phase-to-ground fault and it cannot operate anymore even if the current derating because of the saturation of peak voltage command by the zero-sequence AC voltage injection. It seems that this characteristic is problem in practical use.

2) The MMCC-SDBC: The SDBC can supply the reactive current by a few percentages of reactive current derating under single-phase-to-ground fault to avoid over junction temperature by slightly increased zero-sequence AC current. The SDBC can also keep the operation under phase-to-phase short fault and two-phase-to-ground fault by larger reactive current derating, which characteristics seem better than the SSBC. However, the required zero-sequence current is dramatically increased toward infinity value when the voltage dip severity approach zero under the phase-to-phase short circuit fault and two-phase-to-ground fault, as mentioned theoretically in paragraph III.

3) The MMCC-DSCC: The DSCC could be injected circulating dc current having two degrees of freedom to balance the DC-link capacitor voltages under asymmetrical grid fault conditions. The amplitude of the circulating DC current becomes smaller than the zero-sequence AC current for the SDBC, which has only one degree of freedom. In this result, the DSCC can supply the reactive current under all grid fault scenarios without reactive current derating in this STATCOM case.

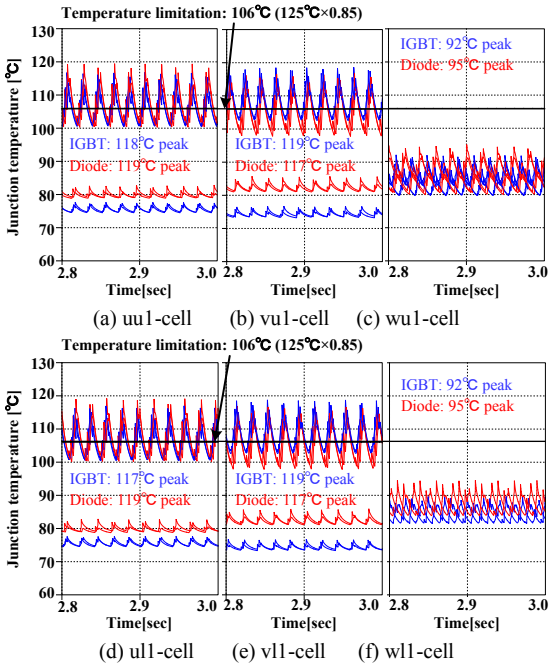


Fig. 19. Thermal distribution of the MMCC-DSBC under single-phase-to-ground fault with a dip severity *D* of 0.4 p.u.

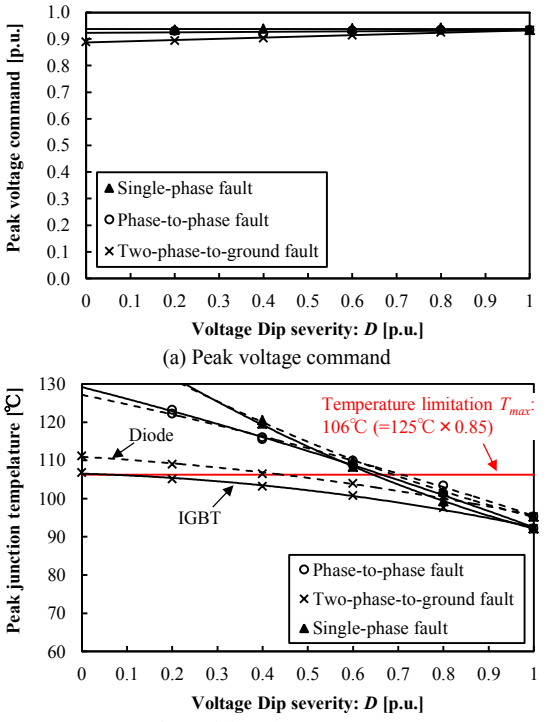


Fig. 20. Electrical-thermal simulations of the MMCC-DSBC at different dip severities

4) The MMCC-DSBC: The DC-link capacitor voltage balancing method for the DSBC similar to the DSCC. However, the amplitude of the circulating DC current on the DSBC becomes larger value compared with the DSCC in compensation for lower injectable DC voltage capability between terminal P and N. The DSBC can keep the operation

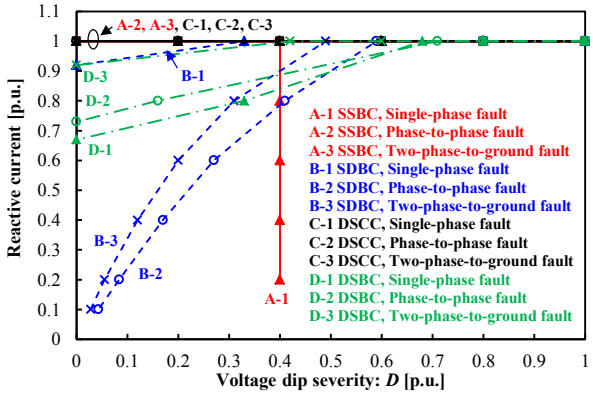
under all grid fault scenarios with a maximum 35% current derating to avoid the over junction temperature, which characteristics are worse than the DSCC, but much better than the SSBC and SDBC.

VI. Conclusion

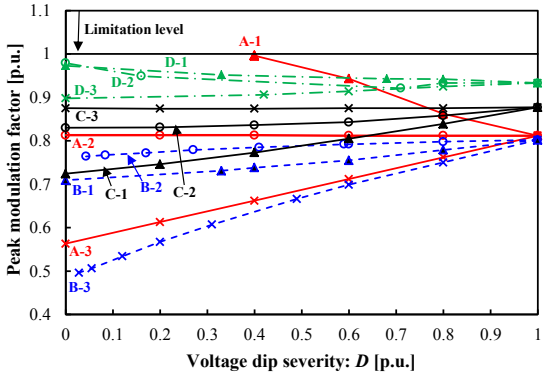
This paper investigates the performances of four configurations of the MMCC family with SSBC, SDBC, DSCC, and DSBC for the STATCOM in large-scale offshore wind power plants, with special focus on asymmetrical Low Voltage Ride Through (LVRT) capability under grid faults. The sizing of the key components, number of cells, electro-thermal analysis, mathematical analysis under asymmetrical reactive power output condition considering the DC-link capacitor voltage balancing control, and reactive current capability of a practical 80 MVar / 33 kV scale MMCC based STATCOM are presented.

The practical designed SSBC and SDBC have unavailable Low Voltage Ride Through operating conditions under some of the grid fault condition because of the dc-link capacitor voltage control. The DSCC can keep the operation in all grid fault scenarios for the whole voltage dip severity without any current derating. However, the total volume of the MMCC-DSCC seems larger than other MMCC solutions because the total energy stored in the capacitors becomes larger for using chopper converter cells. The DSBC can keep the operation in all grid fault scenarios for the whole dip severity with maximum 35% current derating in this case study. The total cost and volume of the DSBC seem similar to SSBC and SDBC because of similar total power semiconductor chip area and total energy stored of the passive components. The present result suggests that the DSBC becomes the most attractive solution for the STATCOM application on the MMCC family.

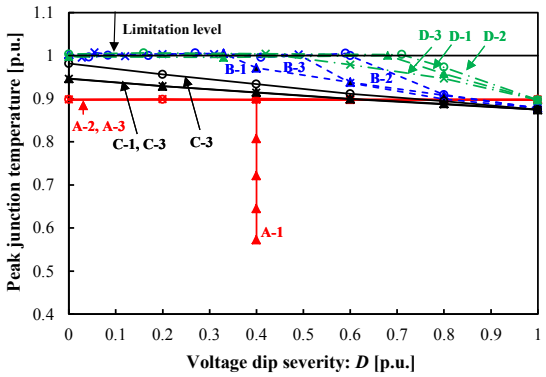
As a future work, asymmetrical faulty grid voltage recovering performance of the DSBC based STATCOM by negative-sequence reactive current injection will be studied, which becomes most advanced requirement emerging in a European country as an optional code.



(a) Reactive current capability



(b) Voltage command according to the reactive current



(c) Junction temperature according to the reactive current

Fig. 21. Reactive current compensation capability of the MMCCs for different dip severities.

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