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**PLANNING AND CONTROL OF
EXPANDABLE MULTI-TERMINAL
VSC-HVDC TRANSMISSION SYSTEMS**

**BY
RONI IRNAWAN**

DISSERTATION SUBMITTED 2018



AALBORG UNIVERSITY
DENMARK

PLANNING AND CONTROL OF EXPANDABLE MULTI-TERMINAL VSC-HVDC TRANSMISSION SYSTEMS

Ph.D. Dissertation

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AALBORG UNIVERSITY
DENMARK

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To my wife Desi
and our daughter Aurora

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CURRICULUM VITAE

Roni Irnawan was born in Bantul, Yogyakarta, Indonesia in 1985. He received the Sarjana Teknik (Bachelor's) degree in electrical engineering from Gadjah Mada University, Indonesia, in 2007, and the M.Sc. degree in electrical and power engineering from Chalmers University of Technology, Sweden, in 2011.

His employment experiences include Gadjah Mada University, Indonesia, from 2008 to 2011, where he was a junior lecturer at the Department of Electrical Engineering. From 2012 to 2015, he was a Modeling and Simulation Engineer with ABB HVDC, Sweden.



Throughout his Ph.D. study (from 2015 to 2018) at the Department of Energy Technology, Aalborg University, he taught two Ph.D./industrial lectures and co-supervised three master theses and one semester project on the field of HVDC transmission system. In the summer of 2017, he spent three months at the Power Systems Research Group, University of Manitoba in Winnipeg, Canada and on several occasions between 2015 and 2018 at the Intelligent Electrical Power Grids (IEPG) Group, Delft University of Technology in Delft, the Netherlands as a guest researcher.

His current research interests include control and protection of HVDC transmission systems, power system components modeling and simulation, and computer-aided power system analysis.

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ABSTRACT

Multi-terminal HVDC (MTDC) transmission systems provide more flexibility and reliability at a lower cost to capture renewable energies and transport them to load centers, as compared to several point-to-point (PtP) HVDC transmissions. Furthermore, MTDC systems widen the cross-border power market, from a bilateral connection into a regional electricity market. Moreover, concerning technology, the voltage-sourced converter (VSC) is the preferred technology to be used in the DC grids due to its ability to reverse power without changing the voltage polarity and each converter within the system can be controlled independently.

In an area where there are already VSC-HVDC links in operation, it is more likely that an MTDC system will develop step-by-step, i.e. starting by interconnecting neighboring PtP links one to another or by connecting a new converter into an existing PtP link. In line with this, COBRACable (a DK-NL HVDC interconnection), is planned to be operated as an MTDC system in the future by connecting an additional offshore wind farm (OWF) converter to its cable. Therefore, this Ph.D. project aims to provide methodologies to allow a smooth transition from a PtP link into MTDC operation or to enable the expansion of an existing MTDC system.

The power flows in an MTDC system are a result of the DC voltage differences and the impedances between the nodes within the system. Therefore, each of the converters within this MTDC system needs to be operated within a specific DC voltage operating limits for different power flow conditions. The challenge arises when an existing system (e.g. a PtP link) is expanded by adding a new converter. Changing the operating limits to have uniformity within the new system might not be favorable because it might require adjustment or even replacement in some equipment of the existing system. In this thesis, the impact of adding a new converter into an existing system, while keeping the existing equipment, to the operating limits of the MTDC system is explained. Moreover, a method to estimate the operating points of the new system is proposed. The proposed method can then be used to evaluate or appraise the expansion plan of an existing system or to establish a requirement for the additional converter to be connected.

After finding the operating limits where all the converters within an MTDC system should be operated, the next step is to coordinate the converter controls to ensure these limits are fulfilled. Depending on the dispatched power flow, each of the non-islanded converters in an MTDC system might be operated in either DC voltage control (*UdcCtrl*), active power control (*PacCtrl*), or DC voltage droop control (*DroopCtrl*) mode. So, each of the converters should have the control structures to

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represent each of these control modes. When a PtP link is expanded into MTDC operation by interconnecting an additional converter, its control systems likely needs to be upgraded because *DroopCtrl* is not common in the PtP link installation.

Furthermore, in the case where the existing MTDC system is expanded by adding more terminals, each converter vendor has their *DroopCtrl* solution, which makes it incompatible with others. Since the control system of HVDC is usually protected as intellectual property rights (IPR), the changes can only be made by the same vendor as the one who built the existing system, i.e. monopolized by a single vendor.

In this thesis, a new control layer is introduced to interface between the centralized MTDC control and localized converter control. The non-islanded converters are operated in *UdcCtrl* mode all the time, while the interface (IFC) units give the DC voltage reference. The DC voltage reference from the IFC unit is provided in such a way that the converter operating point lies along a specified droop line characteristic. This means that as seen from the MTDC control, each of the non-islanded converters within the MTDC system can be operated in different control modes by merely changing the droop line, e.g. zero droop constant means *UdcCtrl* mode, while a straight vertical droop line results in *PacCtrl* mode.

By using the IFC unit, the changes in the existing converter control system can be avoided. In addition to that, different vendors can interconnect their converters without the need to adjust the control system to be compatible with other converters, because the *UdcCtrl* structure is usually available in each non-islanded converter. Furthermore, when DC grid control coordination strategy is changed, e.g. from a single slope droop control to a multi-slope droop control, the changes only happen in the IFC unit while the converter control system is unaltered.

In addition to the droop line tracking, a phase compensator is embedded inside the IFC unit to adjust the time response of the existing *UdcCtrl*. So, the behavior of the existing *UdcCtrl* can be modified externally. Moreover, the IFC unit can work with the HVDC auxiliary control functions, such as frequency, power oscillation damping (POD), and emergency power controls. Simulations in power system analysis tools like PSCADTM/EMTDCTM and DIgSILENT PowerFactory are performed to demonstrate the capabilities of the IFC unit.

The methodologies proposed in this thesis are expected to simplify the process for realizing multi-vendor MTDC transmission systems. At first, the studies needed to examine the feasibility of expansion proposal of an existing HVDC system (either a PtP link or an MTDC system) can be simplified. If this proposal is feasible, the non-islanded converters from various vendors within the new MTDC system can be coordinated by using the IFC unit. After having the coordinated system, the next step is to define the DC protection strategies to secure this system, which is considered as the future work of this Ph.D. project.

RESUMÉ

Multi terminale HVDC (MTDC) transmissionssystemer giver mere fleksibilitet og pålidelighed til en lavere pris til at indfange vedvarende energi og transportere den til lagringscentraler, sammenlignet med flere point-to-point (PtP) HVDC transmissioner. Derudover udvider MTDC-systemer elmarkedet på tværs af landegrænser fra en bilateral til et regionalt elektricitetsmarked. Desuden, voltage-sourced converter (VSC) den foretrukne teknologi, til HVDC-net på grund af dens evne til at tilbageføre energi uden at ændre spændingens polaritet, og hver converter inden for systemet kan styres uafhængigt af hinanden.

På et område hvor der allerede er VSC-HVDC forbindelser i drift, er der bedre mulighed for at udvikle MTDC-systemet trin for trin, dvs. startende med at sammenkoble en nærliggende PtP-forbindelser en til en anden eller ved at tilslutte en ny converter til en eksisterende PtP-forbindelser. I denne er COBRACable (DK-NL HVDC forbindelser), planlagt til at blive drevet som et MTDC-system i fremtiden ved tilslutning af en ekstra offshore vindmøllepark (OWF) converter til sin kablet. Det er derfor sigtet med dette ph.d.-projekt at finde metoder til at sikre en problemfri overgang fra PtP-link i MTDC drift eller at muliggøre en udvidelse af et eksisterende MTDC-system.

Elektricitetsstrømmene i et MTDC-system er et resultat af DC spændingsforskel og impedans mellem knudepunkter i systemet. Det skal således sikres, at hvert af convertere inden for dette MTDC-system kan operere inden for en bestemt DC-spænding grænser under forskellige strøm betingelser. Udfordringen opstår, når et eksisterende system (f.eks. en PtP forbindelser) udvides med en ny converter. Det er ugünstigt at ændre de operationelle grænser for at få ensartethed inden for det nye system, fordi det kan kræve justering eller endda udskiftning af udstyr i det eksisterende system. I denne afhandling forklares det, hvordan tilføjelse af en ny converter virker i et eksisterende system. Ligeledes redegøres for det eksisterende udstyr. Desuden foreslås en metode til at vurdere de operationelle punkter i det nye system. Den foreslåede metode kan derefter bruges til at evaluere eller gennemgå ekspansionsplanen for et eksisterende system eller til at indføre et krav om, at yderligere converteren skal tilsluttes.

Når de operationelle grænser inden for hvilke alle convertere i MTDC-system er bør drives er fundet, er næste skridt at koordinere styringen af converter for at sikre, at disse grænser overholdes. Afhængigt af den udsendte strøm kan hver af de ikke ødrift omformere i et MTDC-system betjenes i enten DC spændingstyring (*UdcCtrl*), aktiv magt styring (*PacCtrl*), eller DC spænding hænge styring (*DroopCtrl*) tilstand. Således skulle hver af converter have styringsstrukturer, der repræsenterer hver af disse styringsformer. Når en PtP forbindelse udvides i MTDC-drift ved tilslutning

RESUMÉ

af en yderligere konverter, skal dens styringssystemer sandsynligvis opgraderes, fordi at *DroopCtrl* ikke er almindelige i PtP-forbindelse installationer. Desuden, i tilfælde hvor det eksisterende MTDC-system er udvidet ved at tilføje flere terminaler, har hver konverter sælger har deres egen *DroopCtrl* løsning, som gør den uforenelig med andre. Da systemet til overvågning af HVDC normalt er beskyttet som intellektuel ejendom (IPR), foretages ændringer kun af den samme leverandør som den, der først har bygget eksisterende systemet, dvs. at systemet er monopoliseret af en enkelt leverandør.

I denne afhandling er et nyt styringslag indført til at kommunikere mellem den centraliserede MTDC-styring og den lokaliserede konverterstyring. De ikke ødrift konvertere køres i *UdcCtrl* mode hele tiden, mens interface (IFC) enheder giver DC spændingsreference. DC spændingsreference fra IFC er fastsat på en sådan måde, at konverterens styringspunkt ligger langs en nærmere angivet hænge linje karakteristisk. Det betyder, at - set fra MTDC-styringen - hver af de ikke ødrift konvertere i MTDC-systemet kan betjenes i forskellige styringstilstande ved at blot ændre linjen hænge, fx. nul hænge konstant betyder *UdcCtrl* tilstand, mens en lige lodret hænge linje resulterer i *PacCtrl* tilstand.

Ved hjælp af IFC kan ændringer i det eksisterende konverter styringssystem undgås. Desuden kan forskellige leverandører sammenkoble deres omformere uden at skulle justere styringssystemet til at være kompatibelt med andre. Desuden, når koordineringen af styringsstrategien for DC-forsyningsnettet er ændret, fx. fra en enkelt hældningshængestyling til mange hældningshængestyling, kan ændringerne kun ske i IFC enheden, mens konverterstyringssystemet er uforandret.

Endvidere er en fasekompensator indlejret i IFC til at justere tidsreaktionen af den eksisterende *UdcCtrl*. Således kanden eksisterende *UdcCtrl*'s upførsel ændres eksternt. Desuden kan IFC-enheden arbejde med HVDC ekstra styringsfunktioner, fx. frekvens, power svingning dæmpning (POD) og styring af nødstrøm. Simuleringscases i PSCADTM/EMTDCTM og DIGSILENT PowerFactory bruges til at demonstrere IFC's kapabilitet.

De metoder, der foreslås i denne afhandling, forventes at forenkle processen for at realisere flere leverandører til MTDC transmissionssystemer. I første omgang kan de undersøgelser, der skulle undersøge gennemførligheden af ekspansionsforslaget til et eksisterende HVDC-system (enten en PtP-forbindelse eller et MTDC-system) forenkles. Hvis dette forslag er gennemførligt, kan ikke ødrift omformere fra forskellige leverandører inden for det nye MTDC-system koordineres ved hjælp af IFC. Efter det koordinerede system er næste skridt at fastlægge strategier for DC-beskyttelse for at sikre dette system, der betragtes som det fremtidige arbejde i dette ph.d.-projekt.

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Roni Irnawan
Aalborg Øst, Denmark
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NOMENCLATURE

$\dots,0$	Origin of the DC voltage droop
\dots,ref	Reference value
\dots,max,\dots,min	Maximum and minimum value
$\dots,meas$	Measured value
\dots,nom	Nominal value
\dots,N	Normalized value
ΔP_{ac}	Deviation in active power
ΔU_{dc}	Deviation in DC voltage
θ	DC voltage droop slope angle, i.e. $k_{droop} = \tan(\theta)$ with $0 \leq \theta \leq \frac{\pi}{2}$
$\Delta U_{dc,ij}$	DC voltage drop between node i and j
CFG_{dc}	MTDC configuration id number
$DBLK_i$	Deblock status of converter i
e_{pos}	Perpendicular distance between the measured condition of the converter from the designated droop line
I_{dc}	DC current measured at DC terminal
i_d, i_q	AC current in dq -axis
k_{DC-AC}	Conversion factor from DC to AC current value
k_{droop}	DC voltage droop constant
$P_{ac,i}$	AC active power flow measured at the PCC of converter i
$P_{dc,i}$	DC active power flow measured at DC terminal of converter i
$P_{diff,Hubk}$	The difference between active power production and demand forecasts at DC Hub k
R_{dc}	DC line resistance
T_{ld}, T_{lg}	Lead and lag time constants for the phase compensator component of the IFC

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$U_{ac,i}$	AC voltage measured at the PCC of converter i
$U_{dc,i}$	DC voltage measured at node i within the DC networks or the DC terminal of converter i
X_{PWL}, Y_{PWL}	Droop line xy -coordinate pairs
<i>DroopCtrl</i>	DC voltage droop control mode
<i>IslCtrl</i>	Islanded control mode
<i>PacCtrl</i>	Active power control mode
<i>QacCtrl</i>	Reactive power control mode
<i>UacCtrl</i>	AC voltage control mode
<i>UdcCtrl</i>	DC voltage control mode
DLT	Droop line tracking
EMT	Electromagnetic transient
HB-MMC	Half-bridge topology of MMC
HVAC	High voltage alternating current
HVDC	High voltage direct current
IFC	Primary control interface
ISE	Integral square error
MMC	Modular multilevel converter
MTDC	Multi-terminal HVDC
OE-EMT	Optimization-enabled EMT simulation
OF	Optimization function
OWF	Offshore wind farm
PCC	Point of common coupling
PI	Proportional-integral
POD	Power oscillation damping
PtP	Point-to-point
PWL	Piecewise linear

RMS	Root mean square, also referred as phasor quantities
SM	Submodule of MMC
STATCOM	Static synchronous compensator
StS	Shore-to-shore
TSO	Transmission system operator
VSC	Voltage-sourced converter
WAMS	Wide area monitoring system

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CHAPTER 1. INTRODUCTION

1.1. BACKGROUND

Europe continues to move away from oil-, coal-, and nuclear-powered electricity and is increasing its generation capacity from renewable sources such as wind and solar photovoltaics (PV) [1]. From the year 2000 to 2016, there was a total of 90.4 GW oil-, coal-, and nuclear-powered capacity that has been reduced, while wind power and solar PV capacity has grown by 142.5 GW and 101.2 GW respectively. By the end of 2016, wind power overtook coal as the second largest electric power source (after natural gas) with 153.7 GW of installed capacity.

Around 8% of the total installed wind power generation capacity in 2016 came from offshore [2]. This capacity has put Europe as the central point of offshore wind power deployment having more than 88% of global offshore wind power capacity [3]. Among the other European regions, the North Sea has become the most utilized region in which 72% (9.1 GW) of Europe's offshore wind turbines are installed.

The advantages of going offshore are mainly due to the wind speed and the free area in the sea [4, 5]. As the wind turbine location is farther from the shore, the wind speed is much stronger and more stable. Thus, larger wind turbine sizes can be installed, e.g. the first 8 MW turbine has been installed in 2016 [2]. Furthermore, several large turbines can be installed in one area of the sea increasing the wind farm capacity without having the same visual and noise impact as onshore. As reported in [2], the average offshore wind farm size has increased by 12% to 380 MW as compared to the year 2015.

In general, there are two ways to transmit power from an offshore wind farm (OWF) to an onshore AC grid, i.e. via HVAC or HVDC submarine cables. As compared to conventional HVAC, power transmission using HVDC gives lower losses for long distance transmission, although the investment cost is higher. The break-even distance between HVDC and HVAC technologies varies from 60 to 100 km, e.g. as reported in [6–8]. However, newer research reveals that for a 1000 MW OWF capacity the break-even distance is between 120 and 160 km or 200 km for an OWF with a capacity between 250 and 500 MW [9].

By the year 2020, it is expected that there will be 9 HVDC links in operation to connect several OWFs in the North Sea to the onshore AC grid with the total capacity of nearly 7 GW located farther than 130 km from the shore [10, 11]. Figure 1.1 shows

this projection with the data given in Table 1.1.

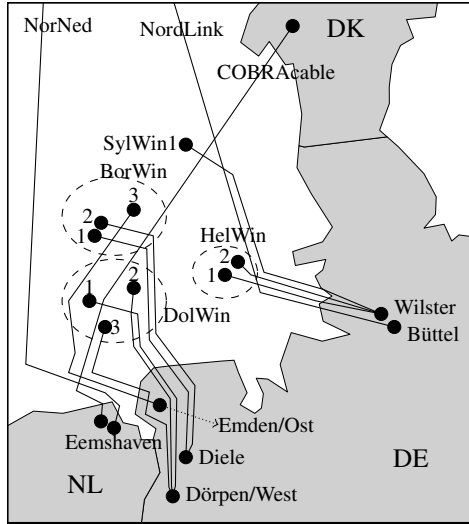


Fig. 1.1: The expected condition of HVDC links in the south-eastern part of North Sea by the end of 2020 [11]. There are more than one converter stations located in Wilster, Diele and Dörpen/West, which are not interconnected.

Table 1.1: HVDC links data for Figure 1.1 [11].

Name	Country	Length (km)	Power (MW)	DC voltage (kV)	Year	Type	Vendor
NorNed	NL-NO	580	700	± 450	2009	LCC	ABB
BorWin1	DE	200	400	± 150	2012	VSC	ABB
DolWin1	DE	165	800	± 320	2015	VSC	ABB
BorWin2	DE	200	800	± 300	2015	VSC	Siemens
SylWin1	DE	205	864	± 320	2015	VSC	Siemens
HelWin1	DE	130	576	± 250	2015	VSC	Siemens
HelWin2	DE	130	690	± 320	2015	VSC	Siemens
DolWin2	DE	135	900	± 320	2016	VSC	ABB
DolWin3	DE	160	900	± 320	2018	VSC	Alstom
BorWin3	DE	200	900	± 320	2019	VSC	Siemens
COBRACable	DK-NL	325	700	± 320	2019	VSC	Siemens
NordLink	DE-NO	623	1400	± 525	2020	VSC	ABB

It is predicted that by 2030 the OWF capacity will grow to more than 70 GW (more than 20% share of total wind power generation capacity in Europe), which is expected to meet at least 13% of Europe's electricity demand [12, 13]. An offshore DC grid has been considered for transmitting this massive offshore wind power across Europe, instead of building several individual point-to-point (PtP) HVDC links to connect remote OWFs with an adjacent onshore AC grid. A DC grid offers more flexibility and security of supply as compared to PtP transmission systems [10].

Apart from this, less cable is needed in a DC grid, which means lower investment

cost and better environmental impact as compared to a PtP solution [14, 15]. Furthermore, a DC grid can also be used for cross-border electricity trading and AC grid reinforcement [16].

Several studies have been performed to evaluate the design of the future North Sea DC grid [14, 15, 17–19]. Some of these proposals were discussed and compared in [20]. Ultimately, 10 North Sea countries have signed a Memorandum of Understanding (MoU) to form the North Sea Countries' Offshore Grid Initiative (NSCOGI) at the end of the year 2010, which was reaffirmed in 2016 [21, 22]. The main aim of NSCOGI is to coordinate these North Sea countries to plan the necessary steps required for the offshore DC grid development.

It is expected that the North Sea DC grid will grow organically, i.e. started as offshore radial multi-terminal HVDC (MTDC) systems and then at a later stage to expand these systems into a fully-meshed DC grid [16, 23]. As an example, by teeing-in a new German OWF into the existing COBRACable to form a 3-terminal HVDC system, which was found beneficial for saving the costs [22]. Furthermore, it is also expected that the DC grid will be based on voltage-sourced converter (VSC) technology due to its ability to reverse the power without changing the DC voltage polarity, which allows a flexible operation of the system [16]. Therefore in this thesis, the term HVDC refers to VSC-HVDC.

Converter coordination within the MTDC system to achieve a new steady-state condition after a disturbance becomes one of the challenging factors that hinders the development of offshore DC grid [16, 24, 25]. Different vendors might be involved at different stages in the development process of the MTDC system. Since VSC technology is still advancing and different vendors have their vision on the development, different technologies might be used. Moreover, the lack of operational experience of VSC-based MTDC transmission (so far only 2 VSC-MTDC systems in operation [26, 27]) and the intellectual property rights (IPR) issues have restrained the vendors to come into agreement.

1.2. EXPANDABLE MTDC SYSTEMS

COBRACable is a 325 km sub-sea PtP HVDC link between Eemshaven (the Netherlands) and Endrup (Denmark), which is rated at ± 320 kV, 700 MW, and ± 230 MVar at each converter station side [28]. This project was started in 2016 and is expected to be in operation by 2019. The converters are supplied by Siemens, which use the latest VSC technology (half-bridge modular multilevel converter (HB-MMC) topology), while the DC cables are supplied by Prysmian [29]. This link is the first HVDC interconnection project between Denmark and the Netherlands, which increases the exchange of wind power trading between both countries [30, 31].

At a later stage, COBRACable is expected to be expanded into an MTDC transmission system by interconnecting one or more additional converters along its existing cables. This plan puts COBRACable as an expandable MTDC system and can be expected to be the first stepping stone towards the development of the North Sea offshore DC grid [30,32].

A possible future expansion of COBRACable by interconnecting an OWF converter is depicted in Figure 1.2. This plan is based on the potential development of wind farm near the COBRACable route. Furthermore, by interconnecting this wind farm to the existing COBRACable system, complexities to build an onshore connection (such as studies related to a new AC landing point and permission to lay the cable to onshore) are reduced [11]. However, up until this thesis is written, there is no specific plan on the future MTDC operation of COBRACable.

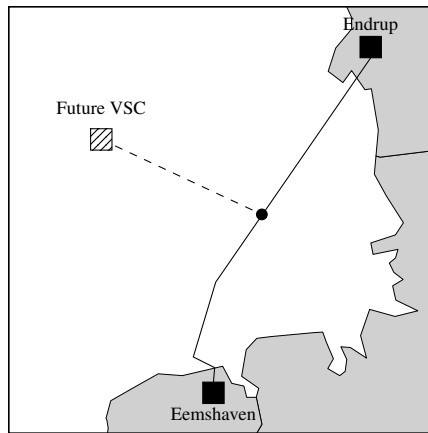


Fig. 1.2: Offshore MTDC operation of COBRACable. Dashed box and line represents a possible future expansion of COBRACable.

There are several PtP HVDC link projects expected to be operated as MTDC systems, such as Caithness-Moray HVDC link (northern Scotland), the SouthWest link (Syd-Västlänken in southern Sweden), Tres Amigas Superstation (southwest US), and FAB link (between France and Great Britain) [33,34]. The first two projects were planned as MTDC systems. However, due to circumstances, only two stations (PtP HVDC link) were built. The Tres Amigas Superstation was planned to become a 3-terminal HVDC system, which was initially built as a back-to-back HVDC station and then at a later stage a new converter will be interconnected to form a *folded back-to-back* topology. As for FAB link, the tender process was started in the late 2017 and during this process, the vendors need to ensure that the FAB converters can be coordinated with an additional converter to form a 3-terminal HVDC system.

As compared to the aforementioned projects, the expansion plan of COBRACable is

unique. COBRACable is currently being built as an ordinary PtP HVDC link without any specific design being implemented for MTDC operation. A research project is being commenced in parallel with the installation of COBRACable to identify the details on how the future interconnection can be achieved without any significant modification in the existing system [28, 30, 31].

The COBRACable research project involves collaboration between universities, i.e. Aalborg University (AAU) and Delft University of Technology (TUD), and industry, i.e. Energinet and TenneT TSO BV. In general, AAU's research focus is on the DC-side impact of the COBRACable expansion, while its influence on the adjacent AC grids will be studied by TUD. AAU's research project covers the coordination between each converter within the system and the MTDC protection system. This Ph.D. project deals with the first part, while the latter part will be done as a separate project.

Although this Ph.D. project concentrates on offshore DC grids, started as part of the COBRACable project, the application in onshore DC grids should be feasible. The same problems occur as well when an onshore PtP link is expanded into an MTDC system with overhead lines (OHLs) connecting the converters, or even combination of offshore and onshore DC grids.

1.3. MOTIVATION AND PROBLEM FORMULATION

In a DC system, active power flow between two nodes depends on the DC voltage difference and resistance between these nodes. This means that depending on the power flow, each converter within the MTDC system might have a different DC voltage operating level. So, each converter within the MTDC system needs to be coordinated in such a way that the fluctuation of the DC voltage operating level of each converter within the system stays within a specific band, e.g. as depicted in Figure 1.3 [35, 36].

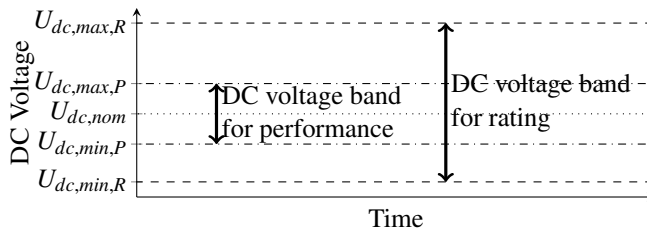


Fig. 1.3: DC voltage steady-state operational ranges [36]. The band between $U_{dc,max,P}$ and $U_{dc,min,P}$ represents the performance range while between $U_{dc,max,R}$ and $U_{dc,min,R}$ represents the DC voltage band for rating. Nominal DC voltage is denoted as $U_{dc,nom}$.

Ideally, when the MTDC system is planned, the operational range of the system is determined by the results from all the possible power flow scenarios. This range is then used to determine the main circuit parameters for each converter within the MTDC

system. However, in the case of a PtP HVDC link expansion, the steady-state operational range of the existing converters are acquired from the PtP operation. This means that the limits were set by considering the DC voltage profiles for power flow between two stations.

Changing these limits might be complicated since it could end up by replacing some parts of the existing installation, e.g. by replacing the DC cables to withstand a higher voltage level or changing a transformer's tap-changer to be able to operate with a lower DC voltage level. Hence, it might be undesirable for the existing system to adapt its steady-state DC voltage operational range whenever an additional converter is connected. Therefore, the influence of the interconnection on the existing steady-state DC voltage operational range should be evaluated. After determining the operational range of the MTDC system, the limits should be reflected in the DC grid control, such that the converters' operating points are within the ranges [36, 37].

In terms of DC grid control, there is a resemblance between DC voltage in a DC system and frequency in an AC system, such that both can be used as the active power balance indicator [36, 38]. Any mismatch in the AC-DC active power exchange might increase/decrease of DC voltage value. Therefore, the DC grid control is designed to mimic the frequency control for AC grid, i.e. it consists of DC grid secondary (coordinated MTDC control) and primary (converter) controls [16, 35, 38–41]. Although the DC grid control concept has been widely discussed, e.g. in [16, 35, 39, 42–47] among others, its implementation in the expandable MTDC system is still challenging. The converter control might need to have a unique control function, which could not be found in the PtP system, i.e. the DC voltage droop control mode [48].

Furthermore, the MTDC system can be operated with all the converters up and running or only several of them in operation. This creates different system behavior after a disturbance, e.g. an AC fault at one of the terminal or loss of one or more converters. Therefore, depending on the configuration of the system, the existing converter control should get the appropriate gains, such that the system behaves as expected, e.g. the rise time and overshoot of DC voltage. However, adjusting the existing control system might be difficult because different vendors might use different control approaches, which are usually protected as intellectual property rights (IPR) and makes them incompatible between each other.

Or, even if the existing and additional systems were supplied by the same vendor, the vast development of HVDC technologies may result in different control versions. It might happen that the older version becomes obsolete and incompatible with a new one. Hence, expanding the PtP link into an MTDC system might end up by replacing the whole control system.

The same thing happens also when the existing MTDC system is further expanded by interconnecting more converters. The control systems of the additional converters

should follow the existing control structures that have already been used. This might limit the option to build a multi-vendor MTDC system for the same IPR issue. Therefore, a generalized DC grid control concept for expandable MTDC systems, which uses the existing converter control system and facilitates a multi-vendor solution, is required.

1.4. PROJECT OBJECTIVES

This Ph.D. project aims to shed light on the methods for planning and coordinate the converters when an existing PtP link is expanded into an MTDC system. Unlike building an MTDC system from scratch, where all the components have been prepared for MTDC operation, the existing PtP link needs to be adjusted when this link is expanded. However, replacing the existing components of the link in order to achieve MTDC operation, might not be a good option, since it means building the system all over again.

Therefore, the *plug and play* principle is considered for expanding the existing PtP link. This means that not only the existing systems should be used without the need to replace them, they should be able to be coordinated with the new converter(s) from various vendors (to reach a multi-vendor MTDC system). To achieve this aim, the following research questions have been defined:

1. How to characterize the changes in the steady-state DC voltage operational range of a PtP link when this link is expanded?
2. How will this new operational range impact the operation of the system?
3. How should the DC grid control be configured to allow the expansion of the system?
4. How should the DC grid control be implemented to ensure interoperability between various vendors?
5. How to implement a generalized converter control, to achieve *UdcCtrl*, *PacCtrl*, and *DroopCtrl* modes, by employing the existing converter control mode?
6. How to externally adjust the existing converter control response?
7. How to expand the proposed DC grid control method to include auxiliary control functions?

1.5. LIMITATIONS OF THE THESIS

This Ph.D. project focuses on the development of offshore DC grids. Hence, the MTDC system considered in this thesis is connected via submarine DC cables. However, the methods proposed in this thesis might also be applied in the onshore MTDC system as well by e.g. changing the submarine DC cables into underground DC cables or OHLs. In this thesis, the method for determining the steady-state DC voltage operational range of the system is only analyzed using the DC cable. For OHL, some differences should be further investigated since higher steady-state margins are expected.

Furthermore, this thesis discusses up to how the expanded PtP link can be controlled to reach steady-state after some disturbances. The DC protection system is considered as the next step of this Ph.D. project. Therefore, the studies involving DC faults (e.g.: fault detection and localization methods) and DC protection devices (e.g. high-speed DC breaker) are not performed in this thesis.

More and more VSC-HVDC projects are planned to use state of the art half-bridge modular multilevel converter (HB-MMC) technology [49]. In fact, all the VSCs except BorWin1 in Table 1.1 were built based on this technology. Therefore, this thesis is focused on this technology and further in this thesis the term HVDC or VSC refers to it.

In an MTDC system, which has one or more loops/meshes within the system, the current flow magnitude in each branch cannot be directly controlled by manipulation of the DC voltage [39]. A DC/DC converter can be used to mitigate this problem, i.e. act as DC power flow control (DCPFC). However, this component is currently not available in the market, therefore this device is not considered in this thesis [10].

1.6. THESIS OUTLINE

The layout of this thesis is depicted in Figure 1.4. The overall introductions of this Ph.D. project including the background, project objectives, and limitations are described in the first chapter of this thesis.

Following the introduction part, the reader can choose to read the part regarding the planning of HVDC link expansion (Chapter 2) or the one regarding DC grid control system (Chapter 3) that is suitable for expandable MTDC transmission systems. Chapter 2 discusses the approaches that need to be taken into account when expanding an existing PtP link into an MTDC system. The key is how to define the steady-state operation limits when additional converters are interconnected with an existing PtP link. Different factors influencing the width of the MTDC operational range are presented.

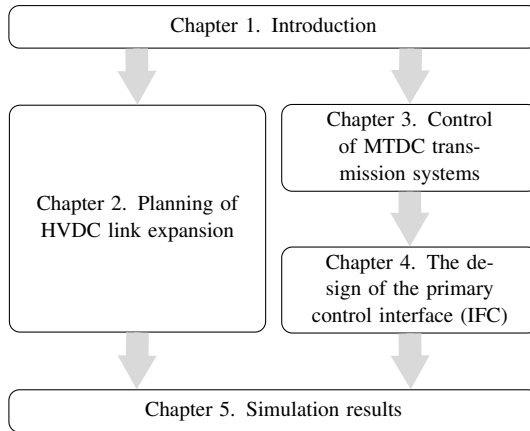


Fig. 1.4: Thesis layout and the relation between chapters.

In Chapter 3, the DC grid control concept is explained. A hierarchical approach similar to the one used in AC frequency control is presented. In this chapter, the DC grid control layers are covered in detail. A new DC grid control concept with a new control layer is proposed, i.e. the primary control interface (IFC).

The design of the IFC is addressed in Chapter 4. The IFC has three functionalities: droop line tracking, phase compensator, and droop line shift. These different functionalities of the IFC are explained in this chapter. Furthermore, in order to show these functionalities, the IFC is tested using a single converter instead of directly putting it into an MTDC system. Although unrealistic, a simulation with this approach is considered because the influence from the other converter can be eliminated. Hence, the ideal behaviors of the IFC can be shown.

The methods proposed in this thesis are tested in a more realistic test systems in Chapter 5. A 4-terminal HVDC system built as a result of interconnecting two PtP links is considered. At first, the steady-state range of the newly build MTDC system is evaluated. After that, EMT and RMS simulations are performed to demonstrate the behavior of the system with the IFC in each of the onshore converters. Furthermore, a 9-terminal HVDC system is also used to show the IFC functionalities. This test system represents a more complex DC grid structure since it has a mesh within the DC grid and is constructed by various converters with different ratings.

Lastly, Chapter 6 summarizes the thesis and some future paths of the study are given.

1.7. LIST OF PUBLICATIONS

Parts of this thesis have been published in the following articles:

- R. Irnawan, F. M. F. da Silva, C. L. Bak, and T. C. Bregnhøj, “An initial topology of multi-terminal HVDC transmission system in Europe: A case study of the North-Sea region,” in *2016 IEEE International Energy Conference (ENERGYCON)*, Leuven, Belgium, Apr. 2016, pp. 1–6.
- R. Irnawan, F. M. F. da Silva, C. L. Bak, and T. C. Bregnhøj, “A categorization of converter station controllers within multi-terminal DC transmission systems,” in *2016 IEEE/PES Transmission and Distribution Conference and Exposition (T&D)*, Dallas, TX, May 2016, pp. 1–5.
- R. Irnawan, F. M. F. da Silva, C. L. Bak, and T. C. Bregnhøj, “DC power flow control for radial offshore multi-terminal HVDC transmission system by considering steady-state DC voltage operation range,” in *The 13th IET International Conference on AC and DC Power Transmission*, Manchester, UK, Feb. 2017, pp. 1–6.
- R. Irnawan, F. M. F. da Silva, C. L. Bak, and T. C. Bregnhøj, “Evaluation of half-bridge modular multilevel converter model for VSC-HVDC transient stability studies,” in *The 13th IET International Conference on AC and DC Power Transmission*, Manchester, UK, Feb. 2017, pp. 1–6.
- R. Irnawan, F. M. F. da Silva, C. L. Bak, and T. C. Bregnhøj, “Steady-state operational range evolution from a two-terminal to a multiterminal HVDC transmission system,” in *CIGRÉ Symposium Dublin 2017*, Dublin, Ireland, May 2017.
- R. Irnawan, F. M. F. da Silva, C. L. Bak, A. M. Lindefelt, and A. Alefragkis, “A droop line tracking control for multi-terminal VSC-HVDC transmission system,” *Electric Power Systems Research*, 2018, under review.
- R. Irnawan, F. M. F. da Silva, C. L. Bak, A. M. Lindefelt, and A. Alefragkis, “DC grid control concept for expandable multi-terminal HVDC transmission systems,” in *CIGRÉ Session 2018*, Paris, France, Aug. 2018.
- R. Irnawan, F. M. F. da Silva, A. M. Gole, C. L. Bak, A. M. Lindefelt, and A. Alefragkis, “Phase compensator for DC node voltage control in multi-terminal VSC-HVDC transmission system,” 2018, manuscript prepared for publication.

CHAPTER 2. PLANNING OF HVDC LINK EXPANSION

2.1. INTRODUCTION

At the planning stage of a PtP HVDC link project, feasibility studies are performed to establish technical specifications of the link. Since the primary purpose of the link is to transfer power between its stations, power flow studies are carried out to study the behavior of the link for different active power transfer conditions [50]. The active power flow between stations in a PtP HVDC link depends on the voltage difference and DC cable resistance (as mentioned earlier and discussed further in this chapter).

So, these power flow studies will give a picture of the operating range of the link, e.g. how much the DC voltage deviates, how much power losses are expected for the anticipated power transfer capability, or how much a reserved margin should be considered for the auxiliary control functions. Apart from this, the suggestions from HVDC vendors regarding the available HVDC components (converter, DC cable, protective devices, etc.) on the market and the experience from other HVDC projects are also considered when defining the rating of the link.

Ideally, the same process should be performed when planning an MTDC transmission system. The power flow cases might be larger since in MTDC system there are possibilities to operate only with some active converters. Therefore, the MTDC components are rated to fulfill all the possible power flow scenarios within the MTDC system.

When a PtP link is expanded into an MTDC system, the planning process becomes challenging. The rating of the existing PtP link has been defined and optimized for PtP operation. Interconnecting an additional converter to the existing link might influence the operational range of the existing system. Changing the range such that it could satisfy all power flow possibilities might not be favorable since it might require some additional components or some parts of the existing system need to be changed or replaced with the new ones [51].

Therefore, expanding a PtP link into MTDC system might result in limited power transfer capability to ensure a safe operation of the system [36, 37]. The influence of interconnecting a new converter with the existing PtP system to the operating range of the system is discussed in this chapter, which is based on the studies performed in [36, 37]. An analytical method to estimate the new operating range of the expanded system

is also explained. The new operating range is then used as a guidance to operate the system during a specific power flow condition. An approximation approach for determining the operating points of the expanded system is proposed, which could simplify the power flow analysis.

2.2. DC SYSTEM POWER FLOW

The power flow between node i and j in a DC system is illustrated in Figure 2.1, which is then formulated in (2.1) as:

$$P_{dc,ij} = U_{dc,i} \frac{U_{dc,i} - U_{dc,j}}{R_{dc,ij}} \quad (2.1)$$

where $P_{dc,ij}$ denotes the active power transmission from node i towards j , $U_{dc,i}$ and $U_{dc,j}$ are the DC voltage measured at node i and j respectively, while $R_{dc,ij}$ refers to the DC resistance between these nodes. The active power flow from node j towards i , $P_{dc,ji}$ in Figure 2.1, can be calculated by exchanging the subscripts of (2.1). Moreover, the DC voltage drop between node i and j , $\Delta U_{dc,ij}$, can be formulated as:

$$\Delta U_{dc,ij} = I_{dc,ij} R_{dc,ij} \quad (2.2)$$

where $I_{dc,ij}$ is the magnitude of DC current flowing through the DC link.

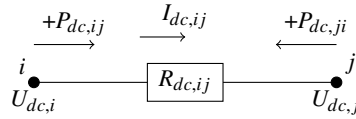


Fig. 2.1: DC power flow between node i and j .

In AC-DC networks, the DC power flow is solved by using an iterative process either simultaneously (explained e.g. in [52]) or sequentially (described e.g. in [53]) with AC power flow. Depending on the known/unknown parameters, the nodes in the DC system can be categorized into 4 types as given in Table 2.1. The first three types are referred to as the converter node, i.e. the DC node that is linked with the AC network through the HVDC converter, while the last type refers to the DC interconnection point or hub that does not have any connection to the AC system. These three converter node types are related to the converter control modes, which are explained in detail in Subsection 3.2.2.

The amount of P_{dc} of the P -type node is known before the DC power flow iteration and is directly related to the measured power at the AC-side. While for the U_{dc} -type node, the amount of P_{dc} is unknown before the DC power flow iteration. This node keeps U_{dc} constant, which is used as the voltage reference for the rest of the nodes in

Table 2.1: DC node types based on the known/unknown parameters.

node type	known	unknown
power (P)	P_{dc}	U_{dc}
voltage (U_{dc})	U_{dc}	P_{dc}
droop	$P_{dc,0}, U_{dc,0}, k_{droop}$	P_{dc}, U_{dc}
intermediate or hub	-	P_{dc}, U_{dc}

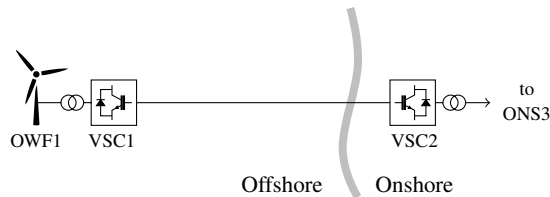
the DC system. Therefore, the U_{dc} -type node can be considered as the slack node for the DC system [38].

In case of a droop-type node, this node is only prevalent in an MTDC system. The droop-controlled converter usually has three known parameters: setpoints for DC voltage and active power ($U_{dc,0}$ and $P_{dc,0}$) and a voltage droop coefficient, k_{droop} [38]. Furthermore, the power flow iteration can be started by considering this node as U_{dc} -type node with $U_{dc,0}$ as the reference [54]. The deviation of active power from the origin ($P_{dc,0}$) should satisfy the droop constant, which is basically the ratio of the DC voltage and active power deviation. In the next iteration, the DC voltage reference is corrected until there is no change between two iteration cycles (convergence).

Regarding power flow direction, there is a fundamental difference between a PtP link and an MTDC system. In a PtP link the power always flows from one converter node to another, while in an MTDC system the power might flow from one converter to several converters or from several converters to one converter (multi-directional). The power flow direction characteristic is explained further in the following subsections.

2.2.1. UNIDIRECTIONAL

In a unidirectional DC system, the active power is expected to flow only in one direction, e.g. from offshore to onshore in an OWF link or from onshore to offshore in a link that is used to power an offshore oil/gas platform. Although a reverse power condition may happen, this is only for a short duration (e.g. during start-up process of the link). An example of this unidirectional DC system is depicted in Figure 2.2.


Fig. 2.2: An example of a unidirectional DC system.

In these applications, the onshore converter is usually operated in DC voltage control ($U_{dc}Ctrl$) mode (U_{dc} -type node). This means that the onshore converter determines the operating points of the system for different power flow conditions. The operating points of the system are shown in Figure 2.3 as dots and a line connecting these two operating points represents the DC voltage profile along the link.

The offshore converter is often operated in the islanded control ($IslCtrl$) mode, because the offshore AC system has a very low short circuit capacity (SCC) level (comparable with the rated power of the offshore converter). In the $IslCtrl$ mode, the offshore converter has the main role to control the AC voltage magnitude at its AC terminal (usually at PCC bus) and to define the offshore AC system frequency [55]. Therefore, the offshore converter can be considered as P -type node since the active power is deduced from the AC power demand (oil rig) or production (OWF link) [48].

An example of the operational range for an OWF link is shown in Figure 2.3. The onshore converter terminal (VSC2) is assumed to maintain the DC voltage at its nominal value, $U_{dc,nom}$. However, in reality, the DC voltage can also be controlled by considering the value in the offshore terminal (VSC1) as well [37].

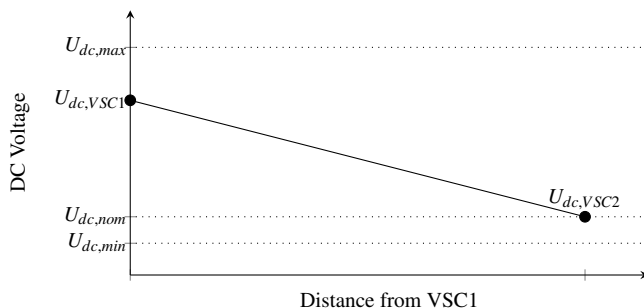


Fig. 2.3: The steady-state DC voltage deviation of a unidirectional link VSC1-VSC2 [36].

The steady-state maximum and minimum DC voltage limits, i.e. $U_{dc,max}$ and $U_{dc,min}$, reflect the DC voltage band for rating. The DC voltage limits for performance, i.e. depicted in Figure 1.3, are not considered for simplicity. In fact, if it is necessary to guarantee the performance, these limits can be used to get a tighter DC voltage deviation limits at the converter's terminal. During transients, the DC voltage can deviate beyond these limits up to a certain time, e.g. for COBRACable project the DC voltage can reach 1.25 per unit for up to 50 ms [28]. However, this transient range should not be confused with the steady-state range in this chapter.

Both converters in Figure 2.2 are assumed to have the same steady-state DC voltage rating. However, it might be the case that the onshore converter has a lower steady-state DC voltage rating than the offshore one (unidirectional link with asymmetric rating) [56]. This is because the offshore converter is subjected to wider DC volt-

age deviation depending on the OWF power production, while the onshore converter stays at $U_{dc,nom}$. However, there is no report indicating the use of an OWF link with asymmetric rating. Furthermore, as it will be explained later, this will give negative impact when this link is expanded into an MTDC system. Hence, the OWF link with asymmetric rating is not considered in this thesis.

2.2.2. BI-DIRECTIONAL

Most of the PtP HVDC links are used to interconnect two onshore AC systems and the power is expected to flow in both directions [36]. Figure 2.4 illustrates an example of the bi-directional DC system with a typical DC voltage deviation depicted in Figure 2.5.

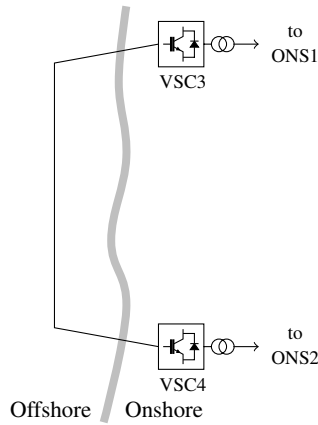


Fig. 2.4: An example of a bi-directional DC system.

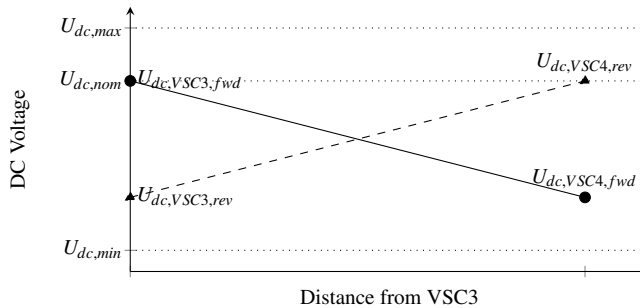


Fig. 2.5: The steady-state DC voltage deviation of a bi-directional link VSC3-VSC4. Forward power direction (from VSC3 to VSC4) is denoted by subscript *fwd* , solid line, and circular markers. While reverse power direction (from VSC4 to VSC3) is denoted by subscript *rev* , dashed line, and triangular markers [36].

In a bi-directional DC link, both converter nodes can interchange the ability to keep

U_{dc} constant. In Figure 2.5, VSC3 kept the DC voltage to its nominal value when the power flows from VSC3 to VSC4 (forward direction). When the power flow is reversed, it also assumed that the U_{dcCtrl} station is exchanged, i.e. VSC4 keeps the DC voltage to its nominal value.

By operating the inverter in U_{dcCtrl} and the rectifier in active power control ($PacCtrl$), the system can be ensured to be operated at the highest DC voltage level, regardless the power flow level through the link. However, for some other links, the operating mode of each converter is independent of the power flow direction. If the U_{dcCtrl} station is located at the inverter, the referred DC voltage should be close to the minimum limit instead of the maximum one depicted in Figure 2.5.

In a PtP link, since both terminals are experiencing the same voltage deviation, both converter stations have the same ratings. However, when this link is expanded into an MTDC system, each of the terminals might experience different voltage deviation. This is explained in more details in section 2.4. Furthermore, if all converters within an MTDC system are capable of being operated as rectifier and inverter, then this MTDC system can be considered as a bi-directional DC system as well.

2.2.3. MULTI-DIRECTIONAL

A multi-directional DC system only appears in an MTDC system, i.e. defined as a mix of one or more bi-directional and unidirectional links in one system. As an example is the 4-terminal HVDC system as depicted in Figure 2.6, which is the interconnection of a unidirectional OWF link (VSC1–VSC2) with a bi-directional link (VSC3–VSC4). The power flow between VSC1 and Hub1 is unidirectional, i.e. the same power flow direction as its original PtP operation. However, the power flow between Hub1 and VSC2 becomes bi-directional, which the same as with VSC3 and VSC4.

Therefore, the DC voltage deviation profile of the OWF link (VSC1–VSC2) is changed from unidirectional to multi-directional shown in Figure 2.7. This means that the measured DC voltage at the offshore station is always higher or equal to the one measured at the hub (unidirectional characteristic). However, this does not apply to the DC voltage measured at the onshore station, i.e. can be higher, lower, or equal to the one measured at the hub (bi-directional characteristic).

It should be noted that to achieve the condition depicted in Figure 2.7, VSC2 becomes the DC slack bus, while VSC3 and VSC4 are in active power control ($PacCtrl$) or become P -type converter nodes. The VSC2 controls the DC voltage such that the DC voltage measured at VSC1 stays the same for different power flow conditions between VSC3 and VSC4.

However, if either VSC3 or VSC4 becomes the DC slack bus, the measured DC volt-

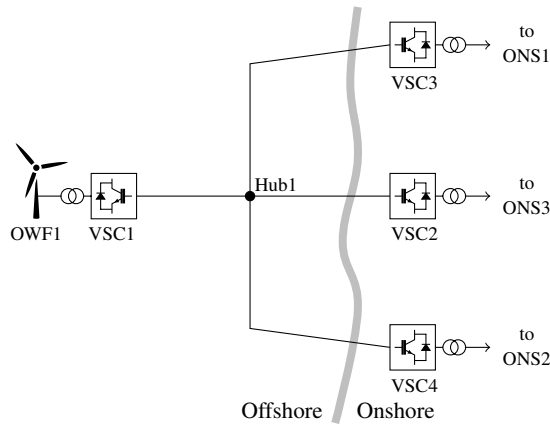


Fig. 2.6: Example of a 4-terminal HVDC system formed by interconnecting two PtP links. The DC voltage is measured at the DC terminal of the converter, i.e. VSC1 is the DC terminal of VSC1, VSC2 is the DC terminal of VSC2, and so on. ONS1, ONS2, and ONS3 represent onshore AC networks, while OWF1 is the offshore wind farm.

age value at Hub1 depends on the power flow condition between these two converters. Hence, the DC voltage deviation profile in Figure 2.7 might be shifted up or down depending on the power flow condition between VSC3 and VSC4.

In the case where VSC1–VSC2 is an OWF link with asymmetric rating, i.e. the onshore converter has lower rating than the offshore one, the possibility of expanding this link into an MTDC system becomes limited. This is because when VSC2 is operated as the rectifier, the operation point of VSC2 depicted in Figure 2.7 needs to be shifted down in order to keep $U_{dc,VSC2}$ around the nominal value ($U_{dc,nom}$). This operation might result in an under voltage condition of the offshore converter.

Another example of a multi-directional DC system is the expansion of COBRACable into an MTDC transmission system, as depicted in Figure 1.2. The power flow from the offshore converter to the hub is unidirectional, while the two onshore converters can be operated as either rectifier or inverter.

2.3. THE STEADY-STATE OPERATING RANGE OF AN EXPANDED HVDC LINK

When the operating characteristics of a PtP HVDC link are known, i.e. by considering all the possible power flow scenarios, the ratings of the HVDC link components can be defined. It is a matter of optimizing the needs of the DC transmission system operator (DC-TSO) and the available technologies provided by the vendor [51]. The

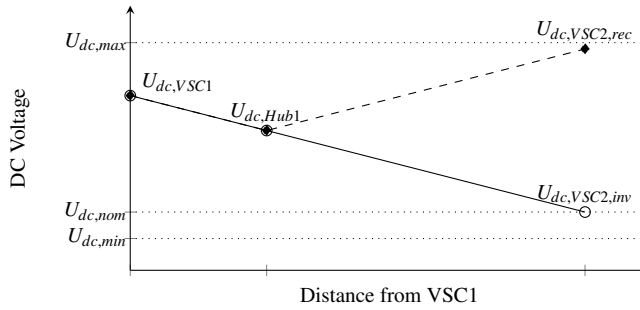


Fig. 2.7: The steady-state DC voltage operating points of an OWF link after being expanded into an MTDC system. There are two possible power flow scenarios in VSC2: *inv* indicates when VSC2 is operated as the inverter, while *rec* when VSC2 is operated as the rectifier. It is assumed that VSC2 controls the DC voltage such that the measured DC voltage at VSC1 is the same for both scenarios.

operating range of a PtP HVDC link is then similar to the one depicted in Figure 2.3 or Figure 2.5.

As further explained in [51], in the case of a future expansion plan of a PtP HVDC link, the future condition (MTDC operation) needs to be considered as well to determine the operating range of the PtP link. The Caithness-Moray link in Northern Scotland is an example of a PtP link where all the components are rated for MTDC operation [57]. The rating of the converter located in Moray is larger (1200 MW) as compared to the one in Caithness (800 MW). This is because it is expected that the future third converter provides power to the Moray side.

If the link is already operated nearly at the end of its lifetime, it makes more sense to replace the system with a new one, which considers the future expansion plan. However, most of the links in the south-eastern part of the North Sea were built between 2009–2016 (as given in Table 1.1). Therefore, the only feasible option to build an offshore MTDC system by interconnecting some of these links soon is to keep the existing system unaltered. The new operating range for this MTDC system is then determined from the operating limits of the existing system and the additional one(s).

The expanded MTDC system is most likely to be a radial system without any loop or mesh on it, which can be considered as the first step towards a fully-meshed DC grid [16]. Furthermore, by looking at the condition in the North Sea region (depicted in Figure 1.1), COBRACable’s path is crossing several OWF links. Therefore, the radial configuration might look like the one depicted in Figure 1.2, Figure 2.6, or even Figure 2.8. The last configuration illustrates another example of this radial configuration, i.e. by adding 2 additional OWF links (VSC5–VSC6 and VSC7–VSC8) to the 4-terminal system depicted in Figure 2.6. It should be noted that the possibility to interconnect two or more expanded shore-to-shore (StS) links is not considered in this thesis since it represents one ahead after the expansion of a link.

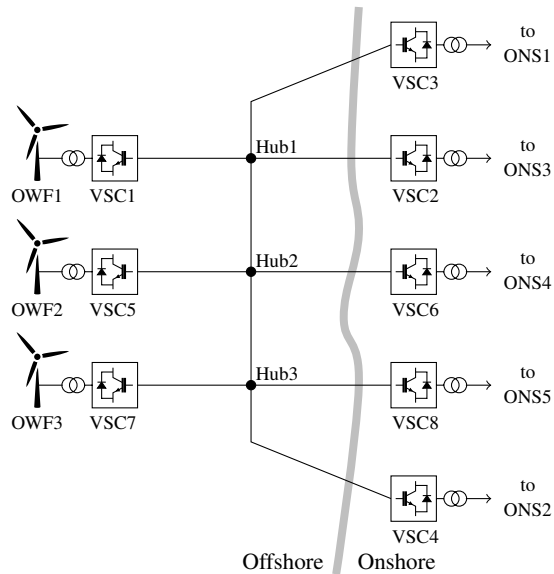


Fig. 2.8: Example of 8-terminal HVDC system formed by interconnecting two more OWF links into the 4-terminal HVDC system depicted in Figure 2.6.

In the aforementioned examples, a StS link (like COBRACable) becomes the host link of the interconnection. This means that the StS link is the link where to which additional converters are interconnected to. Furthermore, this host link is originally a bi-directional link and stays a bi-directional link when this link is expanded into an MTDC system. Hence, the capability of becoming a DC slack node can be interchanged between the stations of this link.

By adjusting the DC voltage profile along this host link, the operation of the MTDC system can be insured to be within a safe range. The idea is to limit the DC voltage deviation in each interconnection hubs along the StS link such that it can reflect the operating range of the additional converters. In the following subsection, an analytical method to estimate the MTDC system operating range by using the StS link operational limits is discussed, based on the work presented in [36].

2.3.1. ESTIMATION OF THE EXPANDED MTDC SYSTEM'S OPERATING RANGE

The following steps can be considered to determine the new operating range of the StS link to reflect the expanded MTDC system's operating limits.

Step 1. Reflect the maximum and minimum allowable DC voltage variation at the additional converter's terminal to the hub. As mentioned in Subsection 2.2.3, if one of the host link converters becomes the DC slack bus, the DC voltage deviation measured at the DC hub depends on the power flow along the host link. Therefore, by limiting the deviation of DC voltage at the hub, the additional terminals can be ensured to be within their limits.

The maximum and minimum limits of the DC voltage deviation at an interconnection hub, $Hubk$, is formulated in (2.3):

$$\begin{aligned} U_{dc,Hubk,max} &= \min\{U_{dc,host,max}, U_{dc,Hubk-VSCi,max}\}, \quad \forall i \in \{1, \dots, n\} \\ U_{dc,Hubk,min} &= \max\{U_{dc,host,min}, U_{dc,Hubk-VSCi,min}\}, \quad \forall i \in \{1, \dots, n\} \end{aligned} \quad (2.3)$$

with

$$\begin{aligned} U_{dc,Hubk-VSCi,max} &= U_{dc,VSCi,max} - \Delta U_{dc,Hubk-VSCi} \\ U_{dc,Hubk-VSCi,min} &= U_{dc,VSCi,min} + \Delta U_{dc,Hubk-VSCi} \end{aligned} \quad (2.4)$$

where subscript i and n represent the index and the number of additional converters connected to the StS link at $Hubk$. The maximum and minimum limits of the i -th converter connected at $Hubk$ are given as $U_{dc,VSCi,max}$ and $U_{dc,VSCi,min}$, respectively, while $U_{dc,host,max}$ and $U_{dc,host,min}$ represent the existing maximum and minimum limits of the host link. The DC voltage drop between $Hubk$ and $VSCi$ ($\Delta U_{dc,Hubk-VSCi}$) can be deduced from (2.2) by considering the maximum current flow between these two, which gives the largest DC voltage drop (worst case scenario).

From (2.3), regardless if it is only one converter or several converters (from one or several OWF links) connected at a particular hub, the DC voltage deviation limits for this hub should be the lowest maximum and the highest minimum values. As an example, a 4-terminal HVDC system depicted in Figure 2.6 is considered. By assuming that all the converters have the same DC voltage rating, only the OWF link determines the limits for the interconnection hub. Both onshore and offshore converters of the OWF link determine the maximum limit of the DC voltage deviation at the interconnection hub (as can be seen in Figure 2.7). However, only the power flow between the onshore converter and the interconnection hub determines the minimum limit. This is because the power flow between the offshore and the hub is unidirectional, hence DC voltage at the hub is always lower than or equal to the one at the offshore converter's terminal.

Step 2. Redesign the new operating range of the host link, which reflects the MTDC system operating limits. The calculated DC voltage deviation limits for each interconnection hub along the StS link are then used to redesign the operating range of the StS link. Figure 2.9 illustrates the new operating range of the StS link (indicated as the grayed area) when this link is expanded into an MTDC system with one interconnection hub as depicted in Figure 2.6.

The operating limits of Hub1 in Figure 2.9 is calculated from the previous step. The new DC voltage range for each of the StS link's converters is calculated using (2.2) by considering the nominal current flowing between Hub1 and each of the StS link's converters. The calculated maximum and minimum limits of the DC voltage deviation is then compared with the existing limits of the StS link (represented in Figure 2.9 by the dashed line). Similar to the previous step, the narrowest DC voltage operating band should be considered as the new DC voltage range for each of the StS link's converters.

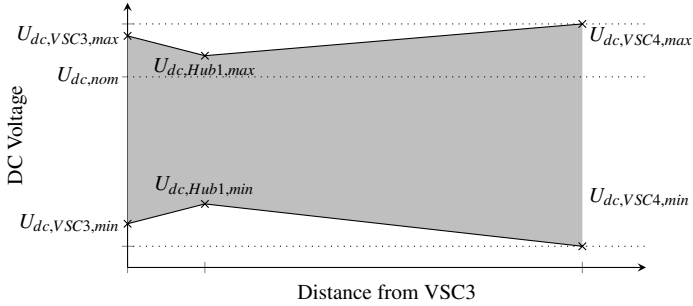


Fig. 2.9: The new steady-state DC voltage operating range (grayed area) for a radial MTDC system with one interconnection hub.

Figure 2.10 shows another example of the new steady-state DC voltage operating range for a radial MTDC system with 3 interconnection hubs depicted in Figure 2.8. In this case, the DC voltage range of VSC3 is influenced by Hub1's operating range, while the one for VSC4 is influenced by Hub3's operating range.

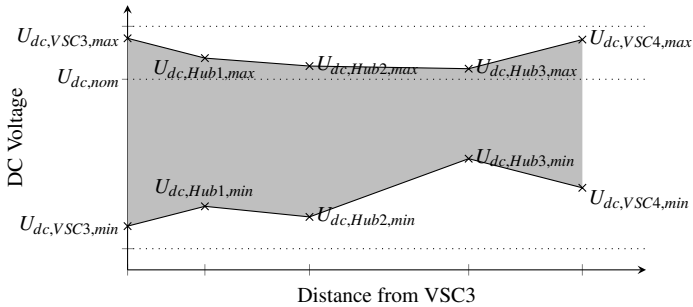


Fig. 2.10: The new steady-state DC voltage operating range (grayed area) for a radial MTDC system with three hubs [36].

Both Figure 2.9 and Figure 2.10 have been generated by considering full power transmission between the additional converters and the hub. If this power flow is zero, the DC voltage measured at both the additional converter and the hub are equal. So, the DC voltage limits at the hub are the same as the limits for the additional converters.

Thus, the DC voltage deviation limits for the hub become wider than the ones calculated in the previous step. This means that this condition becomes the prerequisite for operating with a broader operating range. So, instead of considering each precondition for different power flow conditions in the MTDC system, the new operating range (e.g., as depicted in Figure 2.9 or Figure 2.10) shows the worst situation such that the operating points within this range are acceptable for all power flow conditions within the MTDC system.

2.4. INFLUENCING FACTORS FOR THE EVOLUTION OF A PTP LINK'S OPERATIONAL RANGE

The aforementioned steps to estimate the operational range of the MTDC system is applied for COBRACable project, i.e. an StS link is expanded by interconnecting with only an additional converter along its cable to form a 3-terminal HVDC system. The intention is to show how the operational range of the StS link can change when a new onshore or offshore converter with different ratings, interconnection hub locations, and the distance from the hub is connected. The results determined in this section are the base to build an MTDC system with more interconnection hubs (e.g. as depicted in Figure 2.10)

The StS link (VSC3–VSC4 link depicted in Figure 2.4) is assumed to have the same data as used in COBRACable project. The nominal DC voltage is equal to $\pm 320 \text{ kV}^1$, with a maximum deviation of $\pm 3\%$ at each DC terminal, the power rating of 700 MW, and the DC cables length of 325 km (with $0.0221 \text{ } \Omega/\text{km}$ resistance) [36, 37]. The operational range of this link is depicted in Figure 2.11.

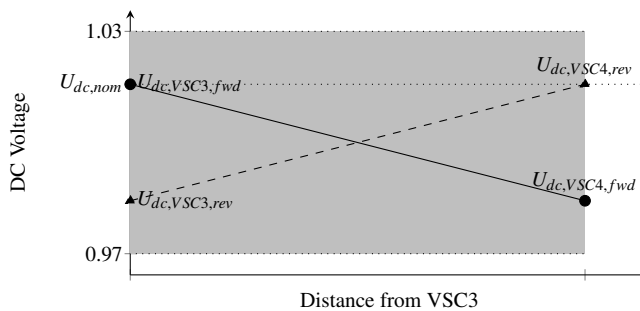


Fig. 2.11: The steady-state DC voltage operational range (grayed area) of the StS link [36].

The additional converter has the same DC voltage rating, but various power ratings have been considered. These power rating and DC cable data alternatives are given in

¹ In this thesis, the \pm sign refers to a symmetric-monopolar converter system, unless defined differently.

Table 2.2. Furthermore, three different options of DC voltage range of this converter are also considered, i.e. $\pm 2\%$, $\pm 3\%$, and $\pm 4\%$ from the nominal value. Apart from these, the type of the additional converter based on its power flow directions, the location of the DC hub, and the distance between this converter to the hub, are also varied.

Table 2.2: The additional terminal's converter and cable ratings [37]. The cable data is taken from [58].

P_{dc} nominal (MW)	I_{dc} nominal (kA)	Conductor area (mm ²)	R_{dc} (Ω /km)
400	0.625	300	0.0601
700	1.094	800	0.0221
1300	2.031	2200	0.0080

For simplicity, each converter station in the 3-terminal HVDC system is assumed to be lossless such that the measured active power at the point of common coupling (PCC) is equal with the one measured at the DC terminal. Furthermore, it is also assumed that the three terminals are always interconnected (T-junction connection), i.e. no DC breaker is installed at the DC hub. The influence of the aforementioned expansion alternatives to the evolution of the StS link's operational range is explained in the following subsections.

2.4.1. INFLUENCE OF ADDING AN OWF CONVERTER

The additional converter is assumed to be an OWF converter (VSC1), hence the power flow between this converter to the hub is unidirectional. Furthermore, it is assumed that the DC hub is located in the middle of the StS link cable and VSC1 is located 162.5 km from it. Figure 2.12 depicts the configuration of the 3-terminal HVDC system with an OWF converter. The steady-state DC voltage limits at the DC hub for various 3rd terminal data, given in Table 2.2, are calculated using the steps explained in Subsection 2.3.1 and then the results are given in Table 2.3.

Table 2.3: DC voltage limits (in per unit) at Hub1 ($U_{dc,Hub1}$) for a 3-terminal HVDC system with an OWF converter depicted in Figure 2.12 for various VSC1 DC voltage ranges and power ratings [37].

VSC1's U_{dc} range	400 MW		700 MW		1300 MW	
	Max.	Min.	Max.	Min.	Max.	Min.
$\pm 2\%$	1.0009	0.9800	1.0077	0.9800	1.0117	0.9800
$\pm 3\%$	1.0109	0.9700	1.0177	0.9700	1.0217	0.9700
$\pm 4\%$	1.0209	0.9700	1.0277	0.9700	1.0300	0.9700

The minimum limit of the DC voltage deviation for Hub1, $U_{dc,Hub1,min}$, is always equal to the minimum limit of VSC1. This is because during power flow condition, $U_{dc,Hub1}$

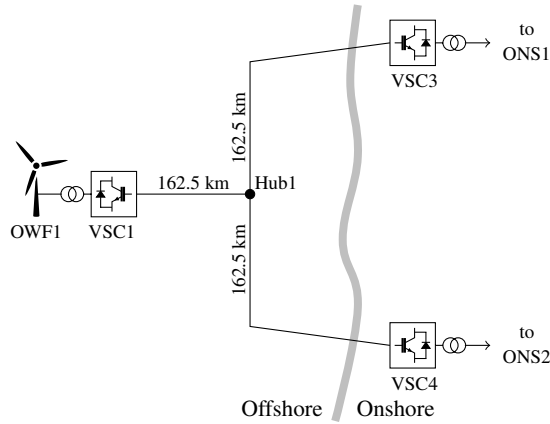


Fig. 2.12: Interconnection of an OWF converter (VSC1) to the StS link.

is always lower than $U_{dc,DCT1}$. Hence, VSC1 operating DC voltage can be ensured to be above its minimum limit.

The maximum limit of the DC hub voltage, given in Table 2.3, reflects the maximum allowable voltage at the DC terminal of VSC1. This means that the operating points of the StS link should be set such that $U_{dc,Hub1}$ does not reach beyond this value. The highest maximum Hub1 voltage limit occurs when an offshore converter with 1300 MW power rating and $\pm 4\%$ operational range is connected. This is due to a combination of lower DC voltage drop (lower DC cable resistance) and wider operational range. The StS link's operating limits are kept as they are for this MTDC configuration.

Figure 2.13 shows an example of the new operational range for the StS link when it is interconnected with an OWF converter with the same power rating and DC voltage deviation limits. In the case of different DC voltage operational range for VSC1, the $U_{dc,Hub1}$ becomes larger if this converter's DC voltage operational range is wider, and vice versa for narrower operational range ($\pm 2\%$ of nominal DC voltage) than the one illustrated in Figure 2.13.

2.4.2. INFLUENCE OF ADDING AN ONSHORE CONVERTER

In the case of an MTDC system with the 3rd terminal located onshore (VSC2), depicted in Figure 2.14, the additional onshore station can be operated as rectifier or inverter (bi-directional node). So, the additional onshore station can have either higher or lower DC voltage as compared to the one measured at Hub1. Furthermore, it is assumed that the distance between Hub1 and VSC2 is 162.5 km. The steady-state DC

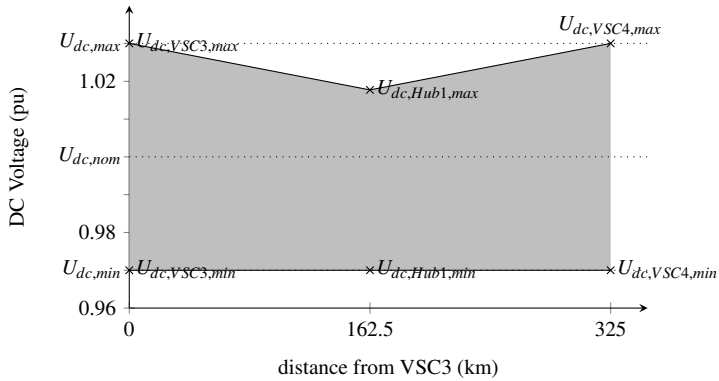


Fig. 2.13: The steady-state DC voltage operational range of a 3-terminal HVDC system with an OWF converter as depicted in Figure 2.12 [37].

voltage limits at the DC hub for various 3rd terminal data are then given in Table 2.4.

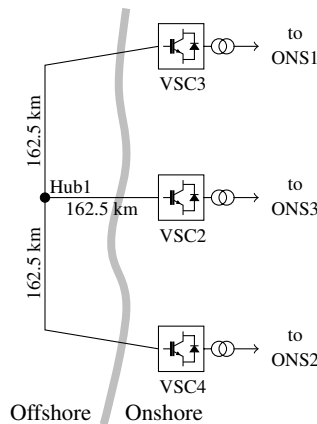


Fig. 2.14: Interconnection of an onshore converter (VSC2) to the StS link.

As can be seen in Table 2.4, the lowest maximum limit of the Hub1's voltage is now dictated by the maximum limit of VSC2 when operated as a rectifier, i.e. similar as in the previous subsection. The minimum limit of the Hub1's voltage is determined by the minimum limit of VSC2 when operated as an inverter. Hence, a narrower band as compared to Figure 2.11 or Figure 2.13.

The narrowest $U_{dc,Hub1}$ deviation limits occur when VSC2 has a lower power rating and narrower DC voltage range as compared to the StS link. Moreover, when VSC2 has a power rating of 400 MW and $\pm 2\%$ DC voltage range, the interconnection plan might be unfeasible, because the DC hub voltage range becomes less than 0.01 per unit.

Table 2.4: DC voltage limits (in per unit) at Hub1 ($U_{dc,Hub1}$) for a 3-terminal HVDC system as depicted in Figure 2.14 for various VSC2 DC voltage ranges and power ratings [37].

VSC2's U_{dc} range	400 MW		700 MW		1300 MW	
	Max.	Min.	Max.	Min.	Max.	Min.
$\pm 2\%$	1.0009	0.9991	1.0077	0.9923	1.0117	0.9883
$\pm 3\%$	1.0109	0.9891	1.0177	0.9823	1.0217	0.9783
$\pm 4\%$	1.0209	0.9791	1.0277	0.9723	1.0300	0.9700

Figure 2.15 depicts the operational range of the 3-terminal HVDC system with all converters having the same power rating and DC voltage limits. As compared to Figure 2.13, the minimum DC hub voltage in Figure 2.15 becomes higher. Hence, the operational range becomes narrower.

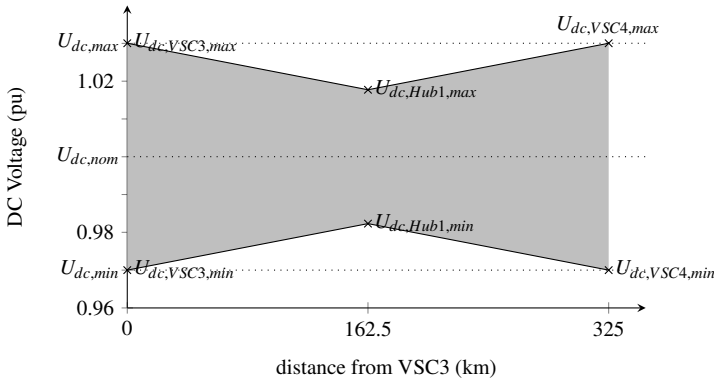


Fig. 2.15: The steady-state DC voltage operational range of a 3-terminal HVDC system with all onshore converters as depicted in Figure 2.14 [37].

2.4.3. INFLUENCE OF THE INTERCONNECTED DISTANCE

One of the important factors that affecting DC voltage drop between the 3rd terminal and DC hub is the resistive distance between these two points. In Subsection 2.4.1 and Subsection 2.4.2, the additional converter distance from Hub1 is 162.5 km. Here, this distance is varied, e.g. 65 km and 260 km with the DC hub is located in the middle of the StS link's cable. The steady-state DC voltage limits at Hub1 for the 3-terminal HVDC system depicted in Figure 2.14 for various onshore 3rd terminal data and locations are then given in Table 2.5.

As explained in Subsection 2.4.1, the DC hub operational range of the MTDC system with an OWF converter depicted in Figure 2.12 has the same maximum DC voltage limit as given in Table 2.5, while the minimum limit can be considered the same as

Table 2.5: DC voltage limits (in per unit) at Hub1 ($U_{dc,Hub1}$) for a 3-terminal HVDC system as depicted in Figure 2.14 for various VSC2 DC voltage ranges, power ratings, and locations [37].

VSC2's U_{dc} range	Distance (km)	400 MW		700 MW		1300 MW	
		Max.	Min.	Max.	Min.	Max.	Min.
$\pm 2\%$	65	1.0124	0.9876	1.0151	0.9849	1.0167	0.9833
	260	0.9895	1.0105	1.0004	0.9996	1.0068	0.9932
$\pm 3\%$	65	1.0224	0.9776	1.0251	0.9749	1.0267	0.9733
	260	0.9995	1.0005	1.0104	0.9896	1.0168	0.9832
$\pm 4\%$	65	1.0300	0.9700	1.0300	0.9700	1.0300	0.9700
	260	1.0095	0.9905	1.0204	0.9796	1.0268	0.9732

the StS link's minimum voltage limit.

For interconnecting a long distance low power (400 MW located at 260 km from the DC hub), the maximum DC hub voltage limit becomes less than 1.0 per unit. This condition might not be feasible. Therefore, for interconnecting a long distance low power converter, a higher converter voltage range and/or a lower DC cables resistance should be used.

As indicated in [36, 37], ideally the DC voltage drop should be less than half of the additional converter's voltage range, e.g. the DC voltage drop should be below 2% for a converter with $\pm 2\%$ range. In Table 2.5, for 400 MW converter, the drop reaches 3.05% for transmitting 0.625 kA through 260 km cables. This means that the option of having a 400 MW additional converter with $\pm 2\%$ and $\pm 3\%$ voltage ranges are not feasible because the DC hub voltage range could not be determined.

Table 2.6 shows an overview of how wide the DC hub voltage range is for 3-terminal MTDC with all onshore converters, using data from Table 2.5. As can be seen in Table 2.6, for the same 3rd onshore terminal's voltage range, having higher power rating helps to ease the DC hub limitation, because of the cable resistance is lower for a higher power rating.

Figure 2.16 shows an example of the operational range of the MTDC system with all onshore converter and the additional converter is located 260 km from the DC hub. Hence, to interconnect a long distance onshore converter with an existing PtP link, the onshore converter should have a higher power rating (less cable resistance) and/or wider DC voltage limits.

Table 2.6: The width of DC hub voltage limits (in %) for a 3-terminal HVDC system as depicted in Figure 2.14 for various VSC2 DC voltage ranges, power ratings, and locations [37]. A graded color code is used to represent the range condition, i.e. red means too narrow (2% or less), green means wide enough range (4% or larger), and yellow is in between these two ranges.

VSC2's U_{dc} range	Interconnected length (km)	400 MW	700 MW	1300 MW
		$U_{dc,Hub1}$ range	$U_{dc,Hub1}$ range	$U_{dc,Hub1}$ range
$\pm 2\%$	65	2.48%	3.02%	3.34%
	162.5	0.18%	1.54%	2.34%
	260	N/A	0.08%	1.36%
$\pm 3\%$	65	4.48%	5.02%	5.34%
	162.5	2.18%	3.54%	4.34%
	260	N/A	2.08%	3.36%
$\pm 4\%$	65	6.00%	6.00%	6.00%
	162.5	4.18%	5.54%	6.00%
	260	1.90%	4.08%	5.36%

2.4.4. INFLUENCE OF THE DC HUB LOCATION

In the previous parts, Hub1 is always assumed to be located in the middle of the StS link. In this part, this location is varied, e.g. 32.5 km (10% of the StS link's length) and 97.5 km (30% of the StS link's length) from VSC3. A DC hub location close to VSC4 is not considered since it will give the same effect as the one close to VSC3 (mirroring effect). The additional terminal is assumed to be located 162.5 km from the DC hub, so the DC hub voltage limits are the same as described in Subsection 2.4.1 or Subsection 2.4.2. Figure 2.17 illustrates the operational range of the MTDC system with all onshore converters, which have the same power rating and DC voltage limits.

When the DC hub is located closer to either one of the StS link sides, the operating range of the StS link's converters become different one from another. As shown in Figure 2.17, the operating limits of VSC3 becomes narrower as compared to VSC4 because Hub1 is located closer to VSC3. Furthermore, if the location of Hub1 becomes closer to VSC3, the operating range of this station also gets narrower. In case of the 3-terminal MTDC with an OWF converter, only the maximum DC voltage limit of the converter is affected.

2.5. ESTIMATING THE OPERATING POINTS OF THE EXPANDED MTDC SYSTEM

By having the new steady-state DC voltage operating range of the StS link, which reflects the operating range of the MTDC system, the DC voltage profile along the

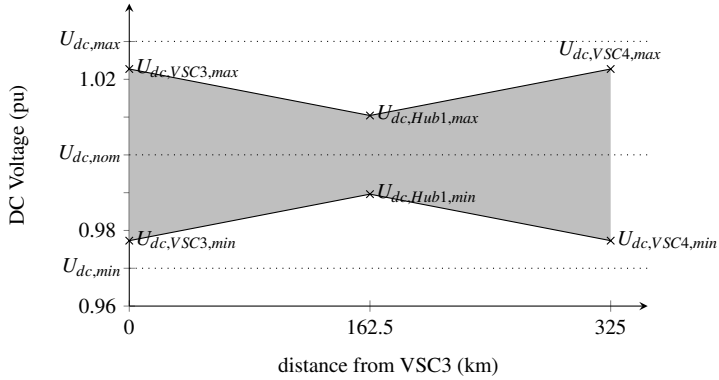


Fig. 2.16: The steady-state DC voltage operational range of a 3-terminal HVDC system with all onshore converters and the 3rd terminal is located at 260 km from Hub1 [37].

StS link for different power flow scenarios should be ensured to stay within this new range. Power flow analysis performed in various tools can be used to determine the exact DC voltage profile along the StS link, especially when there are several converters connected at different hubs. The new StS link's operating range provides a guidance to adjust the DC voltage level at the *UdcCtrl* converter for a specific power flow condition. Furthermore, it might happen that for a specific power flow condition the amount of power transmitted through the StS link needs to be limited since one of the offshore converter goes beyond its steady-state DC voltage limits.

Instead of having the power flow analysis to determine the DC voltage profile along the StS link, an estimation approach based on the produced and demanded power forecasts in each converter can also be used. To show the analysis, a 3-terminal HVDC system with an OWF converter depicted in Figure 2.12 is considered. Furthermore, all the converters have the same rating and steady-state DC voltage deviation limits, i.e. the operational range depicted in Figure 2.13. Two random power flow cases, given in Table 2.7, are used.

Table 2.7: Power flow forecasts of a 3-terminal HVDC system with an OWF converter. The negative sign represents inverter operation or power flow from DC- towards AC-side.

Station	Case 1 (MW)	Case 2 (MW)
VSC1	700.0	300.0
VSC3	-140.0	400.0
VSC4	-560.0	-700.0

In Case 1, the power production from the OWF is split between VSC3 and VSC4 with a ratio of 20/80. The DC voltage drop from Hub1 to each end is estimated by

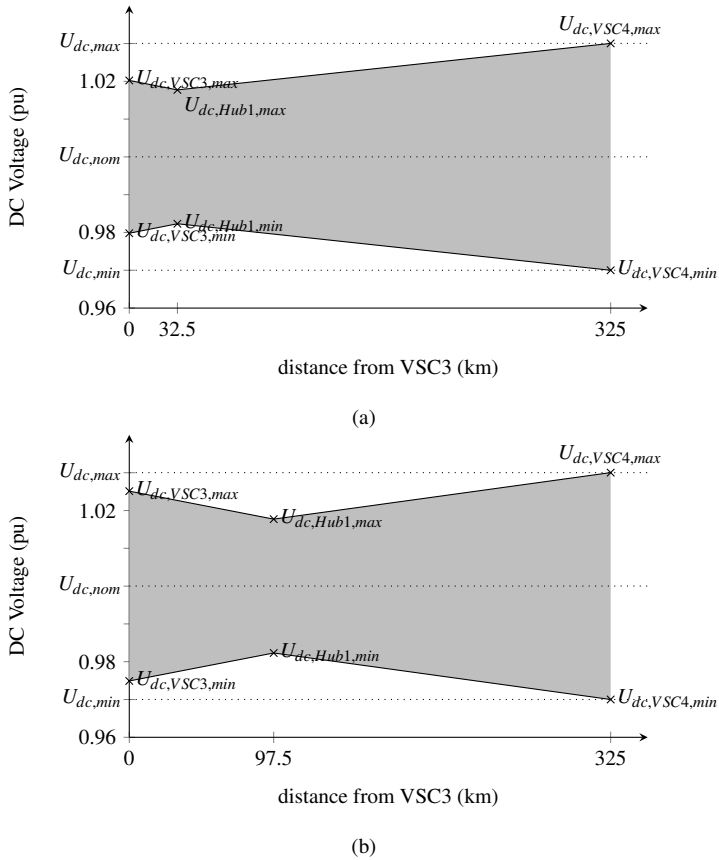


Fig. 2.17: The steady-state DC voltage operational range of a 3-terminal HVDC system with all onshore converters and DC hub location of (a) 32.5 km and (b) 97.5 km from VSC3 [37].

considering this ratio and the nominal DC current. This results in a 0.25% DC voltage drop between Hub1–VSC3 and 0.98% drop for Hub1–VSC4. If it is assumed that VSC4 becomes the DC slack node (setting the DC voltage to 1 per unit), the operating points of the 3-terminal HVDC system for Case 1 is depicted in Figure 2.18.

For Case 2, there are two rectifiers in the MTDC system, i.e. VSC1 and VSC3. The power production from the OWF is summed up with the one from VSC3 to fulfill a 700 MW demand transmitted from VSC4 to the AC side. The nominal DC current is used to estimate the DC voltage drop between Hub1 and VSC4, while a fraction of it (400/700) is used to estimate the drop between Hub1 and VSC3. Furthermore, VSC3 is considered as the DC slack node with a setpoint of 1 per unit. Hence, the operating points is illustrated as the dashed red line in Figure 2.18.

To compare the validity of this approximation method, power flow analysis has been

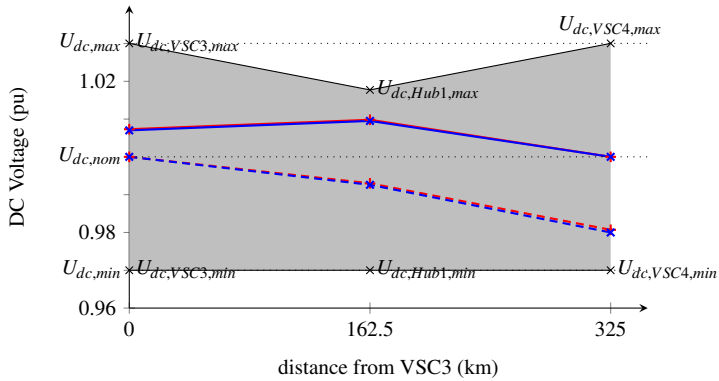


Fig. 2.18: The steady-state DC voltage operating points for Case 1 (solid line) and Case 2 (dashed line) of a 3-terminal HVDC system with an OWF converter depicted in Figure 2.12. The red lines with '+' sign represent the estimated results while the blue lines with 'x' sign represent power flow analysis results. Both colored lines are almost on top of each other.

performed for both cases in PowerFactory software. The results of the power flow analysis for the two cases are also plotted in Figure 2.18, represented by the blue lines. As can be seen in Figure 2.18, although the DC power losses is not considered in the estimation approach, the results are comparable with the power flow analysis results [36]. Therefore, the expansion plan of a PtP link can be evaluated using the estimation approach. Hence, an extensive power flow analysis during the feasibility studies can be avoided.

2.6. SUMMARY

In this chapter, the influence of a PtP link expansion plan in the steady-state DC voltage operational range has been described. Since the existing components are to be kept as they are when this link is expanded into MTDC system, the operation of the new MTDC system might be limited, in order to keep a safe operation of the system. An analytic method to determine the new operating point of the expanded PtP link has been proposed. This method reflects the operational range of the additional converter into the operational range of the interconnection point or hub. The new operational limits of the existing StS link, when operated as MTDC system, can then be determined by considering the maximum and minimum allowable DC voltage deviation in the hub. Hence, when the operating limits of the StS link is fulfilled, all the converters within the MTDC system can be ensured to operate within their limits.

Based on this method, the influencing factors of adding a new converter to an existing link's operational range, such as: ratings, location of the new converter, the location of the hub, and the distance of the new converter from the hub, have been demonstrated.

By knowing the impact of each of these factors to the new operational range of the system, the process for planning or appraising the expansion proposal of a PtP link can be simplified. Or in another hand, the additional converter(s) can be specified such that the impact to the existing operational range is minimized.

The operating points of the expanded MTDC system for a particular power flow can then be estimated using the aforementioned operational range and the power flow forecast for the MTDC system. A power flow analysis has been performed and confirmed the estimated operating points.

CHAPTER 3. CONTROL OF MTDC TRANSMISSION SYSTEMS

3.1. INTRODUCTION

After determining the steady-state operational range of the MTDC system (described in Chapter 2 for the expansion of a PtP link), all the converters within the system should be checked to ensure that they satisfy this range. Furthermore, the system should achieve a new steady-state condition following a disturbance by coordinating the converters that are not connected to an islanded AC system (OWF). Therefore, a DC grid control is employed to regulate the MTDC system.

Based on the frequency control in AC grids, a DC grid control can be divided into a similar hierarchy, e.g. the DC grid primary control (local converter station control) and secondary control (coordinated MTDC control) depicted in Figure 3.1. This hierarchy is based on the similarities between DC voltage in the DC network and frequency in the AC network. This means that a mismatch in power balance will result in a frequency deviation in an AC network or similarly a DC voltage deviation in a DC network [16, 35, 38–41, 59]. In this chapter, the DC grid control layers are described in more detail.

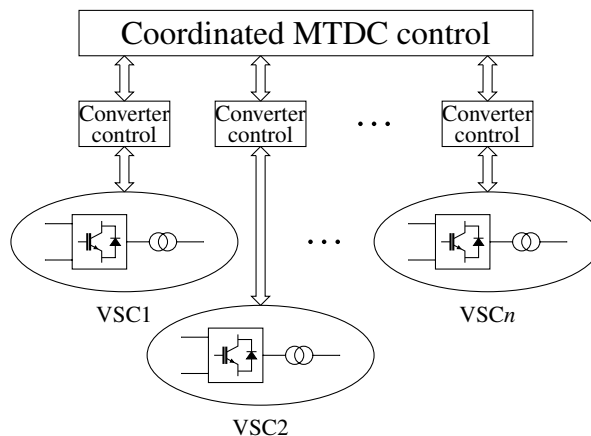


Fig. 3.1: Hierarchy structure of the DC grid control [38,40].

The DC grid control is considered as an inherent part of an MTDC transmission system topology. This means that the DC grid control system is designed to work only

with a specific number of DC terminals, i.e. the expansion plan of an MTDC system is not considered. Furthermore, expanding a PtP link into an MTDC system by interconnecting this link with an additional converter or another PtP link might require the DC grid control to be built on top of the existing control system, which might require changes in the existing converter control system.

Therefore, a new DC grid control concept is described in the last section of this chapter. With this new concept, the changes in the existing converter control system to achieve coordination among the converters in the system can be avoided. This concept uses a new control layer between the DC grid primary and secondary control, which acts as an interface between them.

3.2. THE DC GRID CONTROL CONCEPT

In order to avoid overcomplexity, a control system is usually divided into several layers. Each layer serves different purposes, scopes, and time responses [48, 60]. This conception also applies to the DC grid control hierarchy depicted in Figure 3.1, which is expected to be a common concept accepted by different stakeholders (TSOs, vendors, and researchers) [16, 43, 61, 62].

Regarding the time response of each DC grid control layers, Figure 3.2 illustrates the typical value of it. The DC grid secondary control has a typical time response within 1 second until 1 minute, while the converter control (the outer/RMS controls described in Subsection 3.2.2) has an average time response of 20–500 ms [39, 40, 61].

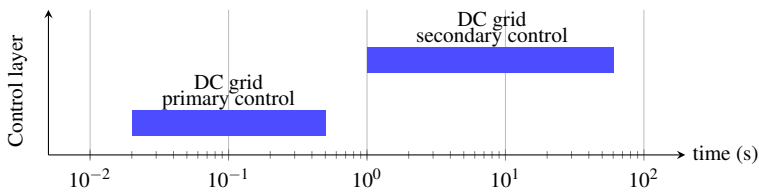


Fig. 3.2: Typical DC grid control operating time range [39, 40, 61].

The coordinated MTDC control (DC grid secondary control) is a global control that looks at the condition of both the AC- and DC-side of each converter within the MTDC system and comes up with the power dispatch order or DC voltage reference for each converter within the DC grid that is actively involved in maintaining the DC system, i.e. not connected to an islanded AC system like the AC network of the offshore oil/gas platform or wind farm collector system. Furthermore, this control layer relies on the communication with each converter station as well as the AC grids (adjacent networks where the converter is connected).

Each of the converters within the MTDC system works locally at its station (autonomously). When a disturbance happens, the converter control (DC grid primary control) should be able to determine a new stable operating point before the DC grid secondary control gives the new setpoints [35]. Therefore, in order to ensure that the converters are still coordinated when a disturbance occurs, the setpoints provided by the DC grid secondary control should be determined by considering all possible disturbances in the DC system, e.g. an advanced converter control mode represented by a piecewise linear (PWL) line (depicted later in Figure 3.7). Further explanations on this matter and detailed discussion of both DC grid control layers are given in the following subsections.

3.2.1. DC GRID SECONDARY CONTROL

The main objective of the DC grid secondary control is to provide the setpoints for each non-islanded converter within the MTDC system. It should be noted that in this thesis, the MTDC system is used to transmit power between AC networks, i.e. the existence of DC power storage and DC generation is not considered. So, the changes in the power flow pattern within the MTDC system has a direct impact on the AC networks where this MTDC system is connected to. Hence, this control involves a wide area monitoring system (WAMS) to retrieve the AC-DC network conditions. The following list of parameters are the ones typically retrieved by the coordinated MTDC control as the inputs to define the setpoints for all non-islanded converters [39]:

1. Scheduled power transfer
 - Scheduled power at PCC bus
 - The forecasted power production of power plants (conventional and renewable) directly connected to the MTDC system
 - The forecasted power consumption of islanded power system directly supplied by the MTDC system
2. AC networks
 - Active and reactive power limits
 - Active and reactive power ramp up and down limits
3. MTDC system topology
 - DC disconnectors status (open/close)
 - DC breakers status (open/close)
4. DC branches and hub conditions

- DC voltage and current measurement
- DC voltage and current steady-state and temporary limits

5. Converter stations

- Status indication (in operation, ready for operation, etc.)
- Measurement of e.g.: AC and DC voltages, active and reactive powers, AC and DC currents, and AC frequency.
- Steady-state and temporary limits of voltage and current
- Control setpoints limits
- Power reduction method operation
- Actual control mode and setpoints

Using the aforementioned parameters, a power flow program is then executed to calculate the setpoints. This program for AC networks has already been used by TSOs to determine a production plan together with consumption and contingency analysis. For an MTDC system, there have been several approaches to include the DC network in the power flow program, e.g. explained in [52, 53].

Furthermore, an optimal power flow algorithm can also be used as well to determine optimal operating points of the MTDC system. An example is to minimize the transmission losses while fulfilling the network constraints such as: to avoid network congestion, all voltages to be kept within limits, no violations of AC network constraints, and a pre-defined security margin of the system is maintained [39, 63–67].

3.2.2. DC GRID PRIMARY CONTROL

The implementation of converter controls usually employs a cascaded control structure, i.e. lower-level and upper-level controls [48, 60]. The lower-level controls are responsible for generating firing pulses for the IGBTs. While there are two types of upper-level controls: islanded (*IslCtrl*) and non-islanded controls. In *IslCtrl* mode, the converter's primary operation purpose is to control the voltage magnitude and frequency at the AC point-of-common coupling (PCC) bus. Hence, the voltage orders for the lower-level controls come from an AC voltage control with the angle reference generated by an oscillator [48].

For non-islanded converters, the upper-level controls consist of the inner or current and the outer or RMS controllers as depicted in Figure 3.3 [68]. The outer controls include controllers of AC voltage (*UacCtrl*), DC voltage (*UdcCtrl*), active power (*PacCtrl*), and reactive power (*QacCtrl*). The active and reactive powers can be controlled independently by e.g. implementing the current vector control method [48]. A synchronous rotating frame, with the AC voltage and the direct (*d*) axis aligned, can be

enforced. Hence, the active power or DC voltage can be controlled by adjusting the d -axis current reference, $i_{d,ref}$, which flows from/to the AC grid. While the quadrature (q) current reference, $i_{q,ref}$, can be used to control the reactive power or AC voltage. Both $i_{d,ref}$ and $i_{q,ref}$ are then linked with the inner controllers to generate the voltage orders for the lower-level controls.

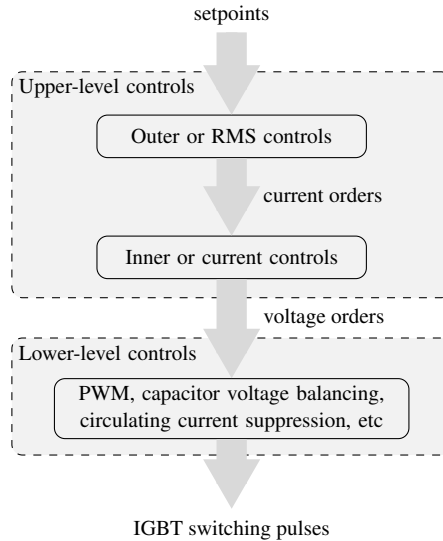


Fig. 3.3: A non-islanded converter control structure [48, 68].

The independent active (P_{ac}) and reactive (Q_{ac}) power control enables the converter to be operated in different P_{ac} - Q_{ac} quadrant. However, the converter power capability curve is not a full circle, but it is constricted by the physical limits of the converter (e.g.: converter currents and voltages). Figure 3.4 illustrates a typical power capability curve of a converter. Three limits are usually considered: maximum current limit of the IGBT (red line), upper converter voltage limit (blue line), and lower converter voltage limit (green line) [69, 70].

The gray area in Figure 3.4 shows the guaranteed capability of the converter, e.g. the converter capability limits are -1.0 to 1.0 per unit active power and -0.25 to 0.25 per unit reactive power [69, 70]. This way, the converter is able to transmit a full active power and 25% reactive power at the same time. If more reactive power flow is required (beyond the gray area), the active power might be limited such that the current flowing through the IGBTs is ensured below the limit. Furthermore, although the rated current is within the limit, the AC voltage at the converter might become too high or too low if more reactive power needs to be injected or absorbed from the AC network.

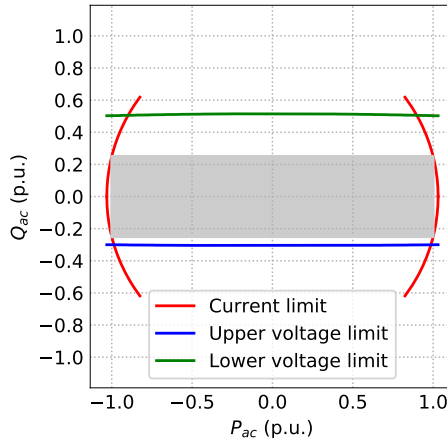


Fig. 3.4: A typical power capability curve of a VSC-HVDC converter [69, 70]. The positive power direction refers to a flow from the AC grid to the converter (rectifier and/or under excited operation), while the negative one refers to a flow from the converter to the AC grid (inverter and/or over-excited operation). The gray area refers to the guaranteed capability of the converter.

The DC voltage level in a DC network can be maintained by adjusting the AC–DC power flow exchange through the converter, while the q -axis control modes maintain the reactive power or AC voltage level in the PCC bus. Therefore, only these d -axis controllers, i.e.: $PacCtrl$ and $UdcCtrl$, considered as the important control modes for MTDC operation. Furthermore, these controls are the ones referred as the DC grid primary control.

In addition to these $PacCtrl$ and $UdcCtrl$, DC voltage droop control ($DroopCtrl$) mode can be considered as the DC grid primary control as well. In an MTDC system with OWF converter(s), $DroopCtrl$ mode becomes the common converter control mode to be used in the onshore stations to share the power production from OWF, i.e. power balancing responsibility can be shared among these onshore converters [38, 39, 45]. In a real system, the application of $DroopCtrl$ mode has been proven in Nan’ao MTDC project [27].

In theory, these three converter control modes can be represented by a single slope droop line as depicted in Figure 3.5(a)–(c) [38, 40]. As can be seen in Figure 3.5(a)–(c), these three converter control modes can be accomplished by changing the slope of the line, i.e. $DroopCtrl$ mode has a negative gradient (since a negative power flow means inverter operation), $UdcCtrl$ mode has a zero gradient and $PacCtrl$ has a straight vertical droop line (an infinite gradient) [38]. Furthermore, the converter ratings should also be represented in the droop line to limit the operation of the converter, e.g. in Figure 3.5 $U_{dc,max}$ and $U_{dc,min}$ represent the maximum and minimum allowed DC voltage level, while $P_{ac,max}$ and $P_{ac,min}$ represent the maximum and minimum active power.

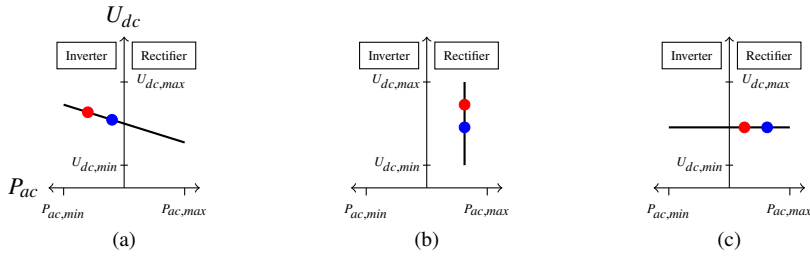


Fig. 3.5: Converter control modes represented by a single slope DC voltage (U_{dc}) and AC active power (P_{ac}) relationship: (a) *DroopCtrl*, (b) *PacCtrl*, and (c) *UdcCtrl* mode [38,40]. The pre-disturbance operating point of the converter is indicated by the red dot, while blue dot represents the post-disturbance operating point.

The setpoints sent from the DC grid secondary control to these converters then depends on the converter control mode, i.e. a DC voltage reference value for the converter in *UdcCtrl* mode and an active power reference value for the converter in *PacCtrl* mode. While for the converter in *DroopCtrl* mode, at least three signals are transmitted, i.e. droop constant, and both DC voltage and active power references as the origin of the droop slope [38, 40]. However, since the *DroopCtrl* is still emerging and there are several concepts that have been proposed in the literature, which might require different signals to be supplied by the DC grid secondary control. These different droop concepts are described in the following subsection.

DC VOLTAGE DROOP CONTROL TYPES

Several concepts of *DroopCtrl* have been proposed in literature, which can be categorized as follows (based on the work of [38]):

DC voltage relation In general, the *DroopCtrl* in P_{ac} - U_{dc} relationship can be formulated in (3.1) [48, 54, 71–73]:

$$U_{dc,ref} = U_{dc,0} - k_{droop,P-U}(P_{ac,meas} - P_{ac,0}) \quad (3.1)$$

where reference values are indicated by the subscript *ref*, while subscript *meas* indicates measured value. Furthermore, $k_{droop,P-U}$ is the droop constant for P_{ac} - U_{dc} relationship, and subscript 0 represent the origin of the droop slope. Since this *DroopCtrl* method measures the deviation in active power and calculate the new reference for the DC voltage, this method is referred as the U_{dc} -based droop method.

On the other hand, by rearranging (3.1) and measuring the DC voltage deviation, the active power reference is given in (3.2):

$$P_{ac,ref} = P_{ac,0} - \frac{1}{k_{droop,P-U}}(U_{dc,meas} - U_{dc,0}) \quad (3.2)$$

Since (3.2) gives a new active power reference, it is referred as the P_{ac} -based droop method.

The $P_{ac}-U_{dc}$ relationship is analogous to the frequency droop control in AC grid, i.e. active power in the x -axis and frequency in the y -axis. This makes the $P_{ac}-U_{dc}$ droop more intuitive to be used in the MTDC systems. However, the relationship between $P_{ac}-U_{dc}$ is not linear as compared to the DC current and voltage ($I_{dc}-U_{dc}$) relationship.

Therefore, another *DroopCtrl* formulation, which benefits from this linear relationship, can be formulated by using DC current (I_{dc}) instead of active power. Hence, the current-based droop control formulated in (3.3) [27, 74, 75]:

$$I_{dc,ref} = I_{dc,0} - \frac{1}{k_{droop,I-U}} (U_{dc,meas} - U_{dc,0}) \quad (3.3)$$

where $k_{droop,I-U}$ is the droop constant for the current-based droop method. The benefit of using the current-based is that the sum of the DC currents equal to zero, while in $P_{ac}-U_{dc}$ relationship, the DC system losses (and converter losses) need to be considered when determining the droop slope. This current-based *DroopCtrl* method is currently implemented in Nan'ao MTDC project [27].

Apart from the aforementioned $P_{ac}-U_{dc}$ and $I_{dc}-U_{dc}$ relationships, based on the power-balance equation across a DC capacitor, $P_{ac}-U_{dc}^2$ relationship has been used in [25]. The droop control is then formulated in (3.4):

$$P_{ac,ref} = P_{ac,0} - \frac{1}{k_{droop,P-U^2}} (U_{dc,meas}^2 - U_{dc,0}^2) \quad (3.4)$$

where $k_{droop,P-U^2}$ is the droop constant for the $P_{ac}-U_{dc}^2$ droop method.

The droop constant in (3.2), (3.3), and (3.4) represents a gradient in the droop slope when plotted in the corresponding droop plane. As an example, for $P_{ac}-U_{dc}$ relationship, the deviation in active power equals to the changes in DC voltage. Hence, when these changes are plotted in the $P_{ac}-U_{dc}$ plane, a straight line can be projected. However, when the changes in active power are converted to DC current and plotted in $I_{dc}-U_{dc}$ the changes become nonlinear anymore.

In order to show the conversion between different droop relationships, a droop line which connect converter's maximum and minimum rating is considered (active power limits of ± 800 MW and DC voltage limits of $\pm 5\%$ from ± 200 kV). Furthermore, the converter is assumed lossless, so the DC current limits can be calculated by directly dividing the active power limits with the DC voltage limits. These values along with the droop constant for each droop relationship are given in Table 3.1.

By assuming that the value of x_{min} and y_{min} in Table 3.1 equal to the droop line origin and increasing the y -axis value from y_{min} until it reaches y_{max} , the new value of active

Table 3.1: Calculated droop constant for different droop relationships. The subscript *max* and *min* represent the maximum and minimum value for the *x*- and *y*-axis of the droop plane. The droop constant, k_{droop} is calculated from these values using (3.2), (3.3), and (3.4) for $P_{ac}-U_{dc}$, $I_{dc}-U_{dc}$, and $P_{ac}-U_{dc}^2$ relationships, respectively.

Parameters	$P_{ac}-U_{dc}$		$I_{dc}-U_{dc}$		$P_{ac}-U_{dc}^2$	
	value	unit	value	unit	value	unit
x_{max}	800.000	MW	2105.263	A	800.000	MW
x_{min}	-800.000	MW	-1904.762	A	-800.000	MW
y_{max}	420.000	kV	420.000	kV	176.400	GV ²
y_{min}	380.000	kV	380.000	kV	144.400	GV ²
k_{droop}	0.025	kV/MW	0.010	kV/A	0.020	GV ² /MW

power can be calculated using (3.2) and (3.4) for $P_{ac}-U_{dc}$ and $P_{ac}-U_{dc}^2$ relationships, respectively. While the value of DC current can be calculated using (3.3) for $I_{dc}-U_{dc}$ relationship.

After the values of the active power for different DC voltage deviations are known, these values are then converted to DC current by simply dividing them with the DC voltage values. Likewise, the active power values can be retrieved by multiplying DC current from (3.3) with the DC voltage values. These values are then plotted in the corresponding droop plane, i.e. illustrated in Figure 3.6.

As can be seen in Figure 3.6, the values from a droop relationship become linear if they are plotted in the same plane as the droop relationship, e.g. $P_{ac}-U_{dc}$ relationship in $P_{ac}-U_{dc}$ plane. But if the values are converted from different relationships, the projections become parabolic due to the non-linear relationship of active power with DC current or DC voltage with the square of it.

However, this deviation becomes smaller for a shorter droop line. Thus, different droop relationships can be enforced in the same DC system and will result the same as having all the converters adopting the same droop relationship, which is shown later in Subsection 4.2.8.

Piecewise linear representation A piecewise linear (PWL) function can be used to represent the *DroopCtrl* characteristic. Each segment of the PWL line represents a droop control mode that is defined by some margins/limits. As an example, the basic droop control characteristics depicted in Figure 3.5(a) actually have two control operation modes: normal and limited operation mode. In normal operation mode, i.e. when P_{ac} is within the active power capability limits ($P_{ac,max}$ and $P_{ac,min}$), the converter is operated in *DroopCtrl* with a certain droop constant. As soon as the active power beyond the limits (limited operation mode), the converter is switched to *PacCtrl*. In the case of $I_{dc}-U_{dc}$ relationship, the DC current limits and measurement are used instead

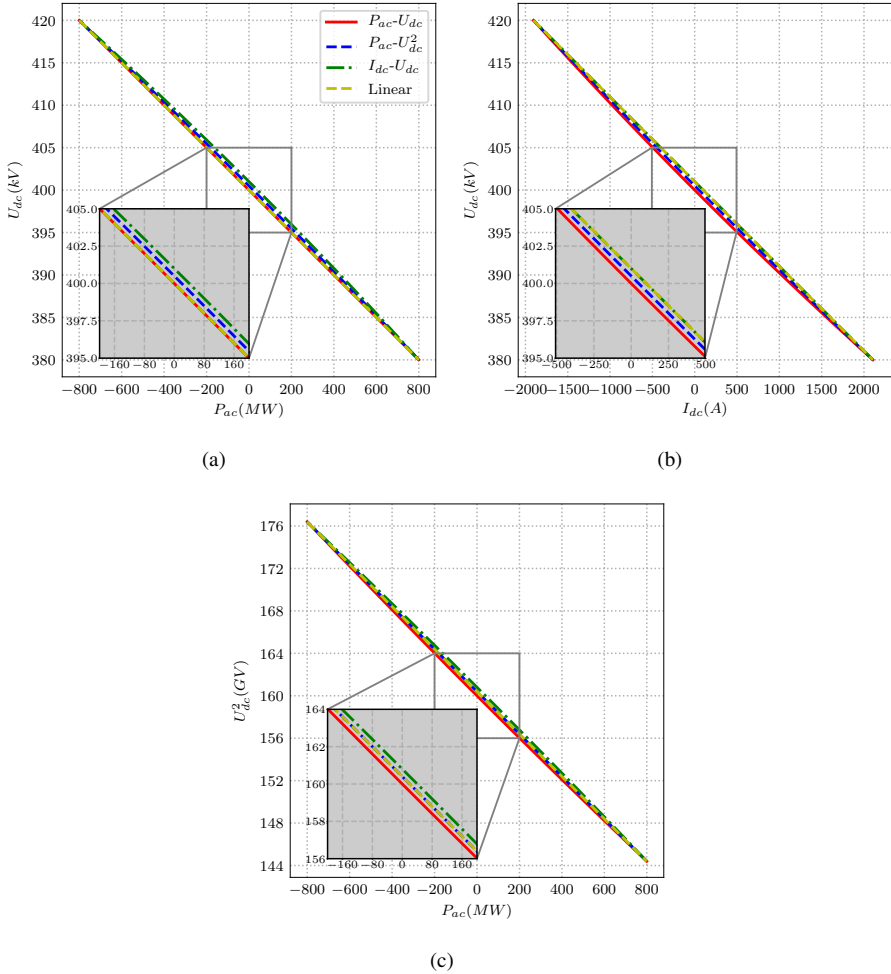


Fig. 3.6: The comparison of droop relationships when the DC voltage is ramped-up from the minimum to maximum value. The calculated results for each $P_{ac}-U_{dc}$, $I_{dc}-U_{dc}$, and $P_{ac}-U_{dc}^2$ relationships are plotted in: (a) $P_{ac}-U_{dc}$, (b) $I_{dc}-U_{dc}$, and (c) $P_{ac}-U_{dc}^2$ plane. The yellow dashed lines (Linear) represent straight lines from (x_{min}, y_{max}) to (x_{max}, y_{min}) .

of the active power [74, 76].

Furthermore, a PWL droop line can be used also to define a more advanced type of *DroopCtrl* mode [16, 27, 73, 77–84], e.g. depicted in Figure 3.7. In this case, different converter control modes can be stacked on top of each other depending upon the operating conditions of the converter. Either DC voltage (Figure 3.7(a), (b) and (d)) or active power (Figure 3.7(c)) or a combination of both can be used to indicate

in which mode the converter should be operated.

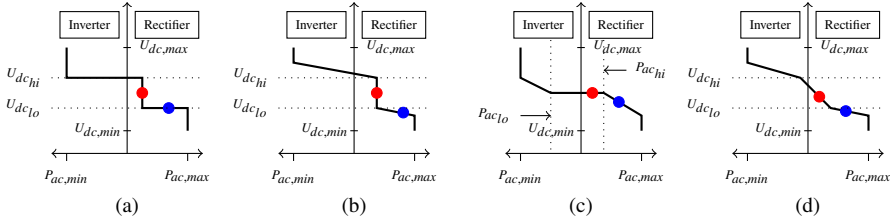


Fig. 3.7: Advanced converter control modes: (a) voltage margin method, (b) constant power dead-band, (c) constant voltage dead-band, (d) 3-stage droop [38, 40]. The pre-disturbance operating point of the converter is indicated by the red dot, while blue dot represents the post-disturbance operating point.

As an example, if one converter is operated in *PacCtrl* mode (straight vertical line), the DC grid secondary control should also give the maximum and minimum DC voltage margins apart from providing the power dispatch order. This is because when there is a disturbance that leads to deactivation of the DC slack bus, this converter changes its control mode to *UdcCtrl* when the measured DC voltage hits either of the limits. This DC grid control strategy is known as the voltage margin method (VMM), which is depicted in Figure 3.7(a) [16, 38, 73, 77, 78].

Another example of an advanced converter control is the dead-band droop control, i.e. depicted in Figure 3.7(b) and (c) [27, 73, 79]. During the normal condition, the converter is operated either in *PacCtrl* mode for Figure 3.7(b) or *UdcCtrl* mode for Figure 3.7(c). Beyond the dead-band, the converter is switched to *DroopCtrl* mode. A variation of dead-band *DroopCtrl* is the 3-stage droop control (Figure 3.7(d)), i.e. the converter has different priority to participate in balancing the active power depending on the level of DC voltage deviation [80].

Control implementation The structure of the *DroopCtrl* can be formed in two ways:

1. Direct implementation

In this structure the output of *DroopCtrl* method is used directly to calculate the *d*-axis current reference for the inner controller, i.e. by dividing the $P_{ac,ref}$ in the *Pac*-based droop method with AC terminal voltage [54]. Another example is to use the current-based droop method and use the conversion factor from DC to AC value (k_{DC-AC}) to calculate the *d*-axis current reference, i.e. as illustrated in Figure 3.8 [27, 54, 72, 73, 85, 86].

2. Indirect implementation

As an alternative, the droop control can be integrated with another *d*-axis outer controllers: *PacCtrl* or *UdcCtrl* loop. In this case, U_{dc} - and *Pac*-based droop methods calculate the new reference for the *UdcCtrl* and *PacCtrl*, respectively

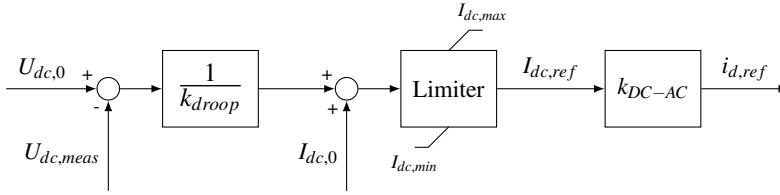


Fig. 3.8: An example of direct implementation of the current-based *DroopCtrl*.

[87–89]. Another alternative is by using the deviation of DC current to modify the DC voltage reference of the *UdcCtrl* [48, 66, 90–92]. Figure 3.9 illustrates the implementation of this *DroopCtrl* method. An advanced droop control can also be implemented as an extension of the existing *UdcCtrl* mode, e.g. explained in [76, 83].

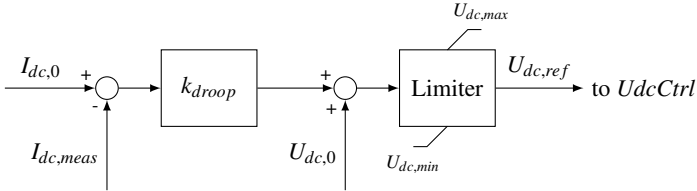


Fig. 3.9: Indirect implementation of U_{dc} -based *DroopCtrl*.

DC voltage measurement location The aforementioned explanations consider the DC voltage value measured at the DC terminal of the converter. However, this value varies for different converter terminal locations within the MTDC system, which depends on the power flow condition within the MTDC system. Following a disturbance it might happen that the converter closest to the disturbance point becomes more violated than the other converters, which means this converter might contribute more to balance the power mismatch.

As an alternative of the local DC voltage measurement in each converter, a common DC voltage measurement can be used to distribute the same DC voltage mismatch to all the converters within the systems [93–96]. Hence, the contribution to power imbalance will depend only on the droop constant. This type of droop control is referred to as the pilot voltage droop control, which can be formulated by replacing the locally measured and referred DC voltages in (3.2) with the pilot ones as formulated in (3.5):

$$P_{ac,ref} = P_{ac,0} - \frac{1}{k_{droop,pilot}} (U_{dc,pilot,meas} - U_{dc,pilot,0}) \quad (3.5)$$

where subscript *pilot* refers to the measured and referred value at a specific point in the DC system or as an average of several converter voltages. A communication system is

needed to spread the $U_{dc,pilot,meas}$ value to all the converters within the MTDC system, which becomes the main drawback of this concept. However, in [97, 98] methods to mitigate communication latencies and outage were proposed by combining local and common measurements to get a more reliable control.

3.3. THE DC GRID CONTROL CONCEPT FOR EXPANDABLE MTDC SYSTEMS

Figure 3.10 illustrates the aforementioned DC grid control concept applied to a 4-terminal HVDC system. This 4-terminal HVDC system is a multi-directional DC system formed by interconnecting 2 PtP links, i.e. VSC1–VSC2 with VSC3–VSC4 mentioned in Subsection 2.2.3. In this MTDC system, 3 onshore converters (VSC2, VSC3, and VSC4) are actively involved in the DC grid control strategy. Meanwhile, VSC1 is connected to an OWF system and operated in *IslCtrl* mode, i.e. the coordinated MTDC control could not specify the active power or DC voltage reference for this converter.

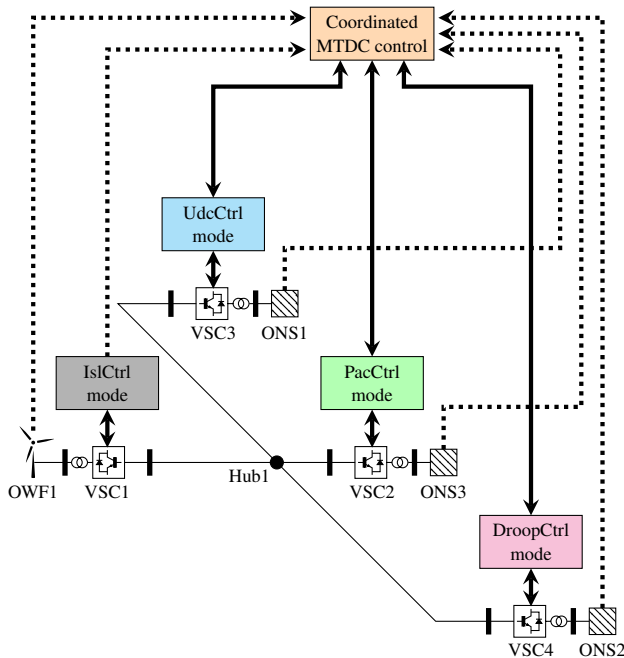


Fig. 3.10: The conventional DC grid control concept [40]. The solid lines represent two-way communication link, while dashed lines symbolize one-way communication link.

It is assumed that for a particular power flow condition, VSC2 is operated in *PacCtrl*

mode, while VSC3 is in *UdcCtrl* mode, and VSC4 is in *DroopCtrl* mode. Since VSC1–VSC2 link is initially an OWF link, the onshore converter might not have both *PacCtrl* and *DroopCtrl* structures available. Similarly, VSC3–VSC4 link might only have the *PacCtrl* and *UdcCtrl* structures available. These additional converter controls for the MTDC operation are referred as the converter’s MTDC specific controls.

3.3.1. SINGLE-VENDOR APPROACH

When VSC1–VSC2 and VSC3–VSC4 are interconnected, their converter control system might need to be upgraded to achieve the operational condition depicted in Figure 3.10. In Figure 3.11, these MTDC specific controls becomes the additional control structures for the existing converter control. It should be noted that Figure 3.11 only illustrates the DC grid control levels and the parameters exchanged between them (represented by the arrows). However, the parameters required by the coordinated MTDC control also include other parameters, e.g. measurement from the AC-side and conditions of the OWF converter (explained in Subsection 3.2.1).

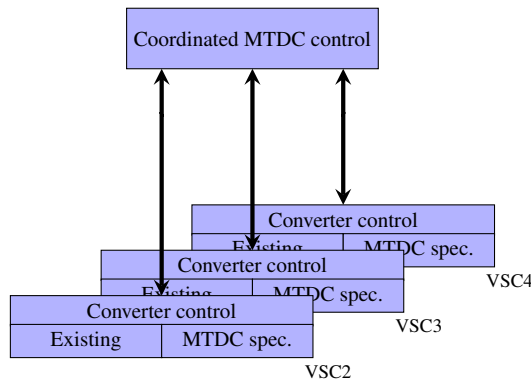


Fig. 3.11: The DC grid control implementation for a 4-terminal MTDC system depicted in Figure 3.10 with only one vendor (*blue*) involved.

The DC grid control in Figure 3.11 is implemented only by one vendor: *blue*. This means that the coordinated MTDC control and the upgrade of the existing converter control system are provided by the same vendor. This approach has been adopted in the realization of the Nan’ao MTDC project in China [27], which was built from scratch. Most of the research in MTDC system have favored that the DC grid control is built by one vendor [38]. This is because the existing converter control has been supplied by the same vendor, which has all the knowledge on how to make some necessary changes to implement the DC grid control.

Furthermore, if the links were installed at different time, the rapid advancement of HVDC technology might result in different converter control versions, which make

the older one obsolete. The replacement of the obsolete part, while leaving the rest unaltered, can only be performed by the same vendor, since they have the details of the converter control that has been implemented.

However, if both links were not supplied by the same vendor, the upgrade process becomes complicated. This is because different vendors might use different control algorithms, which are usually protected by patents. This means that the existing converter control systems might need to be replaced by a new one, to implement the MTDC specific controls.

Another drawback of the single-vendor approach depicted in Figure 3.11 happens when the MTDC system shown in Figure 3.10 is expanded by interconnecting another non-islanded/onshore converter. This new converter should follow the same converter control approach used by the existing system. Therefore, this condition creates a strict requirement for the additional converter and might restrict the expansion to only for the same vendor as the one already built the system.

Moreover, if a new DC grid control strategy is applied, e.g. from single slope to an advanced converter control, the changes applied in both the DC grid primary and secondary controls become challenging. The DC grid secondary control needs to be upgraded to be able to send the multi-slope droop characteristics. Whereas the control system of VSC2, VSC3, and VSC4 need to be upgraded to implement the advanced converter control structures. All of these activities can only be performed by the same vendor who has built the system.

3.3.2. MULTI-VENDOR APPROACH

As can be seen in Figure 1.1 and Table 1.1, all the three major HVDC vendors in Europe have installed their links across the North Sea. Furthermore, for the links with the voltage rating of ± 320 kV, since majority of the links are rated at this level, these links are located close to each other or even the cable routes for some of the links are crossing each other. Therefore, building a multi-vendor MTDC system by interconnecting some of these links become more feasible [11]. Furthermore, a multi-vendor approach provides equal opportunity for other vendors to connect their converter with the existing system. This has been a common practice in the AC grids, where different equipments from various vendors have been interconnected to the same system [16].

Figure 3.12 illustrates the multi-vendor implementation of the 4-terminal HVDC system depicted in Figure 3.10. It is assumed that there are three vendors involved, i.e. one supplies the DC grid secondary control and the other two are the vendor of the links. Different colors are used in Figure 3.12 to represent these vendors.

As explained in Section 3.2, the coordinated MTDC control should be able to receive

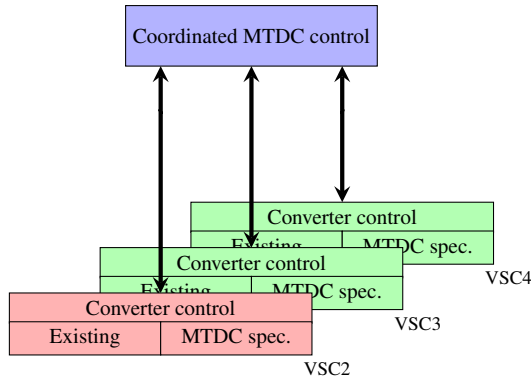


Fig. 3.12: A multi-vendor implementation of the DC grid control for a 4-terminal MTDC system depicted in Figure 3.10. There are three vendors involved in the implementation: vendor *blue*, which supplies the coordinated MTDC control system; vendor *red*, which supplies VSC1–VSC2 link; and vendor *green*, which supplies VSC3–VSC4 link.

the measured conditions of each converter within the MTDC system. On the other hand, each of the non-islanded converters within the MTDC system should be able to reach the setpoints given by the secondary DC grid control. Hence, there should be common understanding between the coordinated MTDC control vendor and each of the converter vendor on what signals should be exchanged between their system. Two European projects (the CLC/TC8X/WG 06 of CENELEC and the BEST PATHS project) have recommended a set of parameter list to enable the communication between the coordinated MTDC control and all the non-islanded converters [99, 100].

Table 3.2 summarizes the parameters exchanged between the DC grid primary and secondary control layers. It should be noted that the parameters in Table 3.2 are the ones necessary for the d -axis controls explained in Subsection 3.2.2, while the complete parameters, e.g. including the q -axis controls parameters and measurements, are given further in [99, 100]. In Figure 3.12, each converter control should be modified such that it could provide and retrieve the parameters given in Table 3.2. This means that the converter control structures might be vendor specific (and protected by the patents), but some of their parameters (e.g. given in Table 3.2) are accessible and available for other vendors.

With this approach, although different vendors can use different converter control approaches, the functionalities (e.g.: control modes and droop control representation) and signals to be exchanged shall be exactly the same. This means that apart from the MTDC specific controls, the existing converter control might also need to be replaced in order to comply with the specification. As an example, an integer number of 0, 1, or 2 is used to define the converter control modes in Table 3.2 to represent the *UdcCtrl*, *PacCtrl*, and *DroopCtrl* mode, respectively. However, the existing converter control

Table 3.2: Parameters for the d -axis outer/RMS controls being sent/received by the converter [100].

Parameter	Type	Unit
Control mode (<i>PacCtrl</i> , <i>UdcCtrl</i> , or <i>DroopCtrl</i>)	input	-
Active power reference	input	MW
Active power reference ramp rate limitation	input	MW/s
DC voltage reference	input	kV
DC voltage droop slope	input	kV/MW
DC voltage reference ramp rate limitation	input	kV/s
DC voltage dead-band where <i>PacCtrl</i> is not applicable	input	kV
Active power measurement at AC-side PCC	output	MW
Pole-pole DC voltage measurement at DC terminal	output	kV
DC current measurement at either positive or negative pole	output	ampere

might use different numbering format and might also include other modes (e.g. the frequency control function defined in [62]).

In order to loosen this strict interconnection requirement, an interface is introduced, which is illustrated in Figure 3.13. This interface is not another control layer, but it decouples the implementation of each converter control with the one required for the DC grid control [101]. For the aforementioned example, the interface will adjust the converter control mode signal given by the coordinated MTDC control such that it corresponds to the vendor specific convention. Furthermore, by using the interface, MTDC system expansion (adding more non-islanded converters to the system) becomes less complicated since the additional converter control does not need modification to comply with the existing DC grid control.

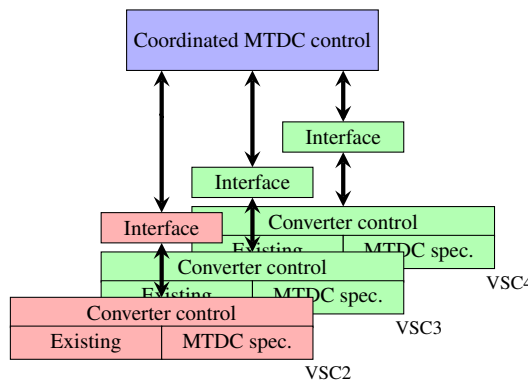


Fig. 3.13: A multi-vendor DC grid control with interface for a 4-terminal MTDC system depicted in Figure 3.10.

However, the existing converter control in both Figure 3.12 and Figure 3.13 are still

need to be altered in order to implement the MTDC specific controls. This is also similar to the single-vendor approach depicted in Figure 3.11. Or in other words, the existing non-islanded converter control must be enforced with the MTDC specific controls before this converter can be part of the MTDC system.

3.3.3. MULTI-VENDOR APPROACH WITH THE PRIMARY CONTROL INTERFACE (IFC)

The common denominator of the control modes used by non-islanded converters in Figure 3.10 is the *UdcCtrl* mode. This is because in a PtP link at least one station should be in *UdcCtrl* mode. In a unidirectional link (VSC1–VSC2), its onshore converter usually maintains the DC voltage. While in a bi-directional DC system (VSC3–VSC4), the *UdcCtrl* mode is usually interchangeable between both stations. This means that by operating all non-islanded converters in *UdcCtrl* mode with a specific reference, a particular power flow condition within an MTDC system can be achieved.

The converter operating point can be expressed by a droop curve, e.g. depicted in Figure 3.5. Furthermore, as explained in Subsection 3.2.2, the implementation of *DroopCtrl* might also follow an indirect approach, i.e. as an extension of the existing *d*-axis control. By considering the same idea, the MTDC specific controls can be implemented as the extension of the existing control (*UdcCtrl*), such that the existing converter control is unaltered. This extension is referred as the primary control interface (IFC), i.e. illustrated in Figure 3.14 [40].

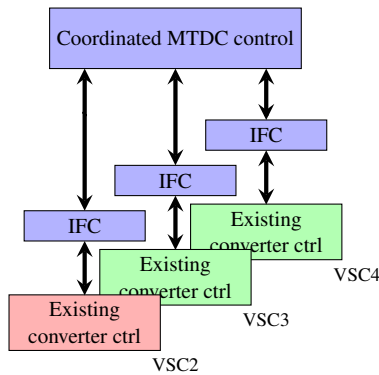


Fig. 3.14: A multi-vendor DC grid control with primary control interface (IFC) for a 4-terminal MTDC system depicted in Figure 3.10. Notice that the MTDC specific controls are not implemented in the converter control as in the previous approaches.

As compared to the interface in Figure 3.13, the MTDC specific controls, the *PacCtrl* and *DroopCtrl* modes, are realized within the IFC. Hence, the DC grid primary con-

trol now consists of two control layers, i.e. the IFC and the existing converter control in *UdcCtrl* mode. So, the IFC provides the appropriate DC voltage reference for VSC2, VSC3, and VSC4 in such a way that depending on their conditions, the pre-defined characteristic (a droop curve) as enforced by the coordinated MTDC control can be followed, i.e. illustrated in Figure 3.15. Or in other words, as seen from the DC grid secondary control, each of the converters in Figure 3.15 operates in the same mode like the one in Figure 3.10 (the line in the IFC represents the droop line characteristics).

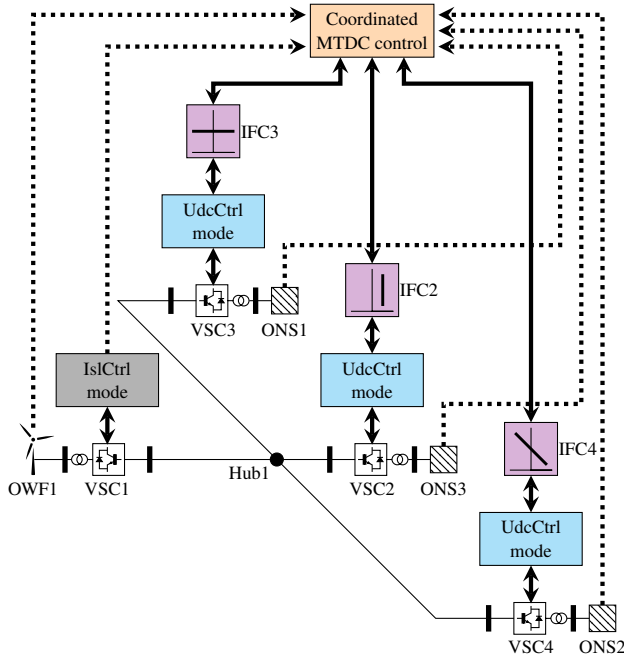


Fig. 3.15: DC grid control concept with primary control interface (IFC) approach [40].

By using the IFC, when another DC grid control strategy is applied, the coordinated MTDC control sends a new operating characteristic for each of the non-islanded converters, e.g. by choosing one from either Figure 3.5, Figure 3.7, or other different droop types mentioned in Subsection 3.2.2. Upgrade in the IFC might be needed in order to comply with the new DC grid control strategy. However, all the non-islanded converters are unaltered and always operated in *UdcCtrl* mode, regardless of the DC grid control strategy applied.

THE STRUCTURE OF IFC

The structure of IFC is shown in Figure 3.16. The input retrieved from the DC grid secondary control is an array of the droop curve's knee points xy -coordinate and an integer indicates the droop relationship of the curve. Figure 3.17 illustrates an example of the droop curve given to the IFC in $P_{ac}-U_{dc}$ plane. This droop curve is constructed by several PWL segments, which includes the operating limits of the converter, i.e. $\pm 5\%$ limits from a ± 200 kV DC voltage level and 800 MW active power rating. So, the X_{PWL} and Y_{PWL} in Figure 3.16 refer to the coordinate of the knee points indicated with squares in Figure 3.17.

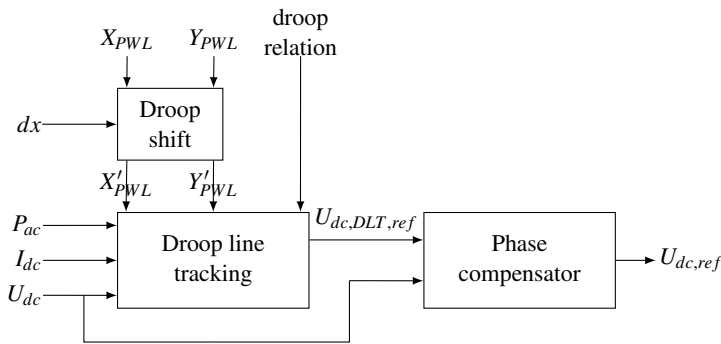


Fig. 3.16: The structure of the primary control interface (IFC) [40]. The inputs from the left represent locally originated signals while the inputs from the above are the received signals from the secondary DC grid control. Further details on each process inside the IFC is explained in Section 4.4.

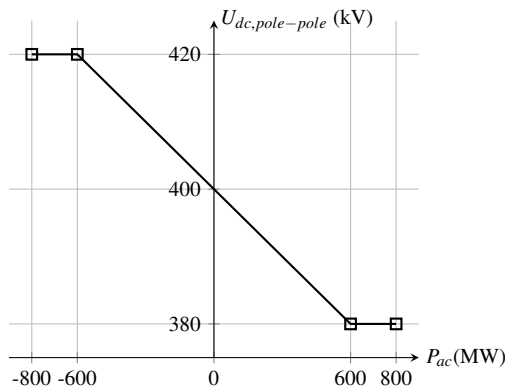


Fig. 3.17: An example of the droop line reference given to the IFC. A list of the knee points coordinates represented by \square becomes the input for the IFC (X_{PWL}, Y_{PWL}).

The droop curve shown in Figure 3.17 represents all of the parameters from the DC grid secondary control given in Table 3.2, except the ramp rate limits. This means that

instead of sending the parameters individually, the IFC receive them as coordinates, which can be constructed back as a droop curve. The IFC then generate a specific DC voltage reference for the converter, such that the measured active power (P_{ac}) and DC voltage (U_{dc}) of the converter lies along this curve. The component responsible for generating this reference is referred as the droop line tracking (DLT) unit in Figure 3.16 [102].

In order to switch between different converter control modes ($UdcCtrl$, $PacCtrl$, and $DroopCtrl$), different droop slopes are used, e.g. depicted in Figure 3.5. In Figure 3.17, the converter is expected to be operated in $DroopCtrl$ mode when the measured active power is between -600 and 600 MW. If it is required for the converter to be operated in $PacCtrl$, then a straight vertical line at the reference point (e.g. 600 MW) is used instead of a slope in Figure 3.17. When the DC voltage at the terminal reaches either its maximum or minimum limit, the DLT output ($U_{dc,DLT,ref}$) will be equal to either of these values to avoid over or under DC voltage operation.

A ramp rate limiter can be applied separately to limit the changes in each X_{PWL} and Y_{PWL} before it is given as the IFC's input. The changes in the droop curve can be slowed down to avoid a transient in the system. As an example, with the ramp rate limiter in the X_{PWL} , the active power step received from the DC grid secondary control (perceived as a shift in the droop curve along the x -axis) is translated as a ramp with up to some MW/s by the rate limiter. This also applies for the changes in the DC voltage (Y_{PWL}). The application of this ramp rate limiter will be demonstrated later in Section 5.2.

Another advantage of using the DLT method is because it can simplify the implementation of the advanced converter control, e.g. depicted in Figure 3.7. As mentioned earlier, the DLT produces the DC voltage reference ($U_{dc,DLT,ref}$) such that the converter operating point lies along the droop curve. Therefore, the advanced converter control can be implemented by simply giving more slopes in the droop curve, which can be achieved by adding more points into X_{PWL} and Y_{PWL} . Further details on the DLT is given later in Section 4.2.

Furthermore, different droop relationships explained in Subsection 3.2.2, can also be implemented using the DLT. The same principle applies by simply changing the X_{PWL} to represent the DC current or Y_{PWL} to represent the square of the DC voltage. This means that the droop relationship input in Figure 3.16 is used to match the referred droop curve units with the required measurement signals.

The DLT enables the converter to be operated in different control modes by using the same converter control structure, i.e. the existing $UdcCtrl$ mode. So, the time response of the converter operated in different control modes emulated using the DLT will depend on the existing $UdcCtrl$ response. Since the existing $UdcCtrl$ is optimized when this converter is operated as a PTP link, it might need readjustment for the MTDC op-

eration. The phase compensator component in Figure 3.16 is introduced to externally adjust the time response of the existing *UdcCtrl*. This means that the time response of the existing *UdcCtrl* can be adjusted without altering the parameters of it. The design of this is explained later in Section 4.3.

Apart from the aforementioned functionalities, the IFC can also be used to integrate the auxiliary converter control functions: power oscillation damping (POD), frequency control, and emergency control. These auxiliary functions are usually part of the PtP link control feature [39]. Therefore, in order to keep these functionalities when the PtP link is expanded, the droop shift part in Figure 3.16 is introduced. The output of these auxiliary control functions are connected to the dx in Figure 3.16. As the name implies, this component give a shift along the x -axis to the droop curve (to give a *Pac* step up or down) given by the DC grid secondary control. The details of this part of IFC is described later in Section 4.4.

MODULARITY OF IFC

A modular design approach has been adopted such that the IFC is implemented as an external part of the existing converter control as depicted in Figure 3.15. The implementation of the IFC in power system simulation tools is described in Appendix D. The IFC is intended to be integrated with the vendor specific (black-box) converter control model used during the dynamic studies.

Therefore, by using the IFC, the dynamic studies performed to e.g. measure the feasibility of the expansion plan of a PtP link can be done as early as possible. During the completion of a PtP link installation, the vendor is also deliver black-box models for different studies will be performed by the TSO [50]. Up until now, there is no standard signal lists have been defined for the black-box models such that they can communicate with the outside world. Hence, in order to achieve the multi-vendor DC grid control implementation approaches depicted in Figure 3.12 and Figure 3.13, the TSO is required to clearly define the parameters from the converter control (e.g. given in Table 3.2) to be communicated with the DC grid secondary control. This means that the DC grid control method needs to be defined before the parameters can be defined. Then, ask the converter vendors to send a new model which complies with this requirement before the TSO could perform the studies [100]. If another DC grid control method needs to be tested, which might change the parameters required, another new model should be provided.

With the IFC, the only requirements for the existing control are it should be autonomous and its DC voltage reference can be adjusted. If the model satisfy these requirements, the TSO can start their studies without the need to request the converter vendor to adjust their black-box model. In the case when different DC grid control

method should be applied, the same black-box model can be used. This work flow is depicted in Figure 3.18 and has been adopted for COBRACable research project. Some simulation cases have been performed and the results show a successful implementation of the IFC together with the vendor specific black-box model. However, due to confidentiality, the simulation results using the black-box model for COBRACable research project cannot be shown.

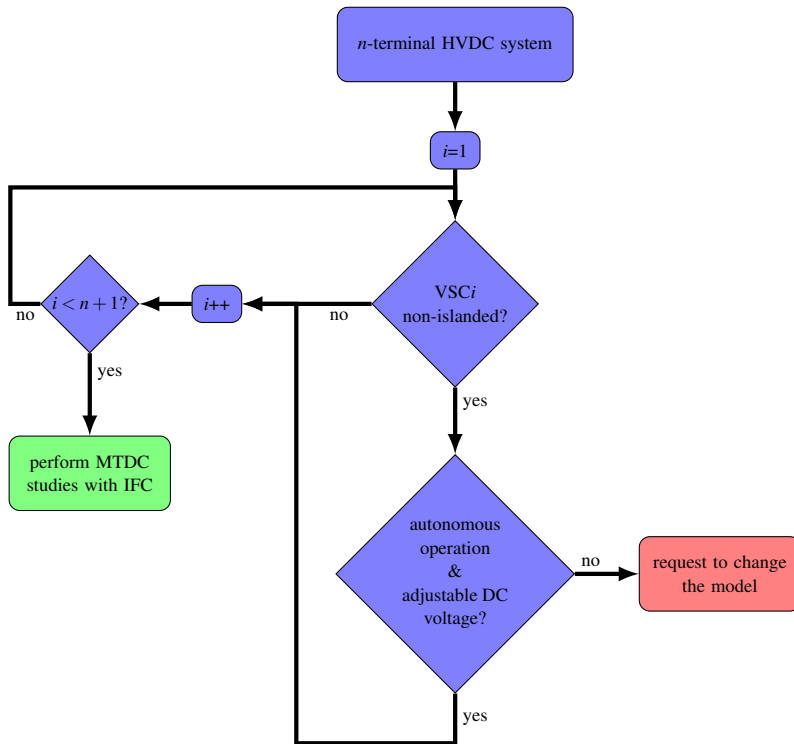


Fig. 3.18: The work flow to evaluate if the existing black-box model can be used for the expansion studies.

3.4. SUMMARY

The conventional DC grid control concept has been explained in this chapter. Challenges to implement the DC grid control in the expandable MTDC system have also been discussed. A new control layer is introduced in the DC grid primary control, i.e. the primary control interface (IFC), to reduce complexity when interconnecting two existing PtP links into MTDC system or expanding an existing MTDC system by adding more converters. As an interface, the IFC separates the implementation of the DC grid primary control and the converter control. Therefore, different DC grid control strategies can be applied, while the converter control stays in the *UdcCtrl*

mode.

There are three functionalities of the IFC, i.e.: droop line tracking (DLT), phase compensator, and droop shift. The DLT is used to produce the appropriate DC voltage reference such that the converter is operated along a predefined droop curve. The phase compensator is used to adjust the time response of the existing *UdcCtrl*. The droop shift is used to integrate the auxiliary control functions, i.e. by shifting along the x -axis the predefined droop curve received from the DC grid secondary control.

The IFC is implemented adopting a modular design approach. Hence, the IFC can be directly integrated with the black-box model to perform MTDC dynamic studies. Further details of the IFC is going to be explained in Section 4.4.

CHAPTER 4. THE DESIGN OF THE PRIMARY CONTROL INTERFACE (IFC)

4.1. INTRODUCTION

In the previous chapter, the primary control interface (IFC) has been introduced, which is used as an additional layer between the DC grid secondary and primary controls. The design of IFC is discussed further in this chapter.

The main aim of the IFC is to provide the DC voltage reference value for the existing *UdcCtrl*, such that the existing PtP link control can be used for the MTDC operation. This can be achieved by employing a droop line tracking (DLT) method [102]. In principle, the DLT method uses the similar algorithm as the one used in a line-follower robot, e.g. as explained in [103]. Hence, the name droop line tracking is adopted.

By using the DLT method within the IFC, the DC voltage reference for the existing *UdcCtrl* is adjusted such that the converter follows a droop curve, i.e. the one depicted either in Figure 3.5 or Figure 3.7. Unlike the conventional droop control, this reference is calculated based on the displacement error (the shortest distance) between the droop line and the measured condition of the converter (active power and DC voltage).

Furthermore, a phase compensator component is also implemented inside the IFC. This component is used to adjust the time response of the existing *UdcCtrl* externally. A lead-lag filter, that is commonly found in the excitation system of the synchronous generator (e.g. in [104]), becomes the main component of this phase compensator.

Another feature of the IFC is the ability to integrate the auxiliary control functions, which are retained from the existing PtP link control. In general, the output signal of these auxiliary functions is a power increase/decrease order calculated based on the AC grid condition where the converter is connected [39, 67, 104]. Therefore, these control functions can be integrated by shifting the droop curve received from the DC grid secondary control along the x -axis (changes in the active power reference) [40].

In other words, by using the IFC the following advantages can be achieved:

- Different converter control modes can be achieved by merely changing the droop line reference given to the IFC. This means that the converter can be operated in *PacCtrl*, *UdcCtrl*, or *DroopCtrl* mode with a single control structure.

- The droop line tracking method within the IFC also simplifies the implementation of the advanced converter control, e.g. the one depicted in Figure 3.7.
- The response of the existing converter control can be adjusted externally by using the phase compensator within the IFC.
- It allows the integration of the auxiliary control functions.
- Modular implementation is adopted, which means that the IFC is implemented as an extension of the existing converter control. Hence, the existing converter control is unaltered to implement the aforementioned features.
- Can be integrated with the black-box models to perform the dynamic studies during the design phase of the MTDC system.

However, since the IFC relies on the existing *UdcCtrl* structure, the IFC can only be realized when the DC voltage reference of the existing control is available. Furthermore, the behavior of the *PacCtrl* and *DroopCtrl* will rely on how fast the existing *UdcCtrl* response to a disturbance. This becomes the main drawback of the method. The phase compensator can be used to adjust the performance of the existing control. However, this feature is limited by the time response of the other controllers, e.g. inner or current control.

In the following sections, the components of the IFC (i.e. depicted in Figure 3.16) are explained. Whereas, the implementation of the IFC for the power system simulation software is described in Appendix D.

4.2. DROOP LINE TRACKING (DLT) METHOD

The $P_{ac}-U_{dc}$ relationship is considered to explain the DLT method. This is due to the analogy with the frequency control used in AC grids. However, the same explanation can be performed as well using different droop relationships. The comparison of various droop relationships is shown later in Subsection 4.2.8.

4.2.1. THE CONVENTIONAL DROOP CONTROL METHOD

As explained in Section 3.3, the most suitable approach to implement the DC grid control for the expanded PtP link is by extending the existing non-islanded converter control system. This approach allows the existing control system unaltered, while ensuring the interoperability with another vendor. Furthermore, since the *UdcCtrl* can be found in every PtP link installation, the converter control extension is applied to this control mode. In order to apply the *DroopCtrl* mode as an extension of the existing

UdcCtrl mode, the new DC voltage reference can be calculated using (3.1), i.e. the DC voltage deviation equals to the droop constant (k_{droop} in MW/s) multiplied with the deviation of the measured active power (P_{ac}) from its reference or origin ($P_{ac,0}$). This *DroopCtrl* implementation (U_{dc} -based droop method) is referred as the conventional method.

In principle, the *DroopCtrl* aims to ensure that the converter operation condition lies along a specified droop line. This means that, if a deviation in operating point occurs, either the DC voltage or the active power, the new reference is calculated in such a way that the working condition of the converter moves along the droop line. This situation can be illustrated in Figure 4.1 when the measured condition of the converter, *meas* ($P_{ac,meas}, U_{dc,meas}$), is off the droop lines due to a disturbance. Three droop curves are considered in Figure 4.1: the one having the slope of θ , θ' , and θ'' .

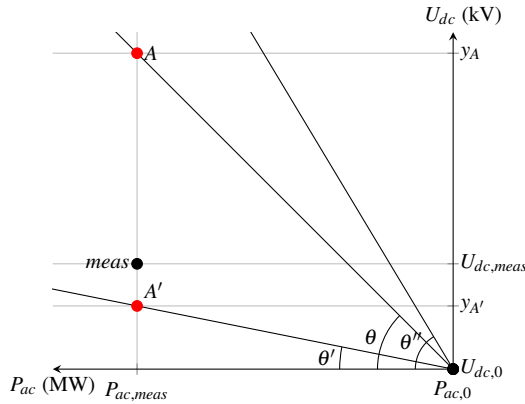


Fig. 4.1: Illustration of *DroopCtrl* mode in P_{ac} - U_{dc} plane. The red dots represent the new reference points.

For the deviation depicted in Figure 4.1 and $k_{droop} = \tan(\theta)$, the new reference is given as point *A*. This new reference can be calculated in (4.1), i.e. the y -axis coordinate is derived from (3.1).

$$\begin{aligned} x_A &= P_{ac,meas} \\ y_A &= U_{dc,0} - \Delta P_{ac} \tan(\theta), 0 < \theta < \frac{\pi}{2} \end{aligned} \quad (4.1)$$

where ΔP_{ac} is the deviation in active power, which equals to $P_{ac,meas} - P_{ac,0}$. Furthermore, the droop slope angle (in radians) is limited between 0 and $\frac{\pi}{2}$, i.e. when θ is zero the converter is operated in a constant DC voltage (*UdcCtrl*) mode, while θ of $\frac{\pi}{2}$ means a constant active power (*PacCtrl*) operation. The value of y_A calculated in (4.1) is then used as the new $U_{dc,ref}$ value.

When a lower droop constant is considered, i.e. the droop slope equals to θ' in Figure 4.1, the new reference for the existing *UdcCtrl* is denoted as point *A'*. The coordi-

nated of this point can be calculated using (4.1) with the angle θ' . Since $\theta' < \theta$, the deviation in the DC voltage origin, $U_{dc,0}$, is lower for θ' although ΔP_{ac} is the same. Hence, point A' is closer to $U_{dc,0}$.

When a higher droop constant value is used, i.e. the droop slope equals to θ'' in Figure 4.1, the new DC voltage reference for the existing *UdcCtrl* lies outside the drawing plane, i.e. above point A. This is because the value of $\tan(\theta'')$ in (4.1) makes a higher deviation from the DC voltage origin for the same deviation in active power (ΔP_{ac}) as compared to the one with a lower droop constant (a flatter curve).

This means that as the droop constant is increased, the existing *UdcCtrl* is expected to allow higher deviation from its origin, $U_{dc,0}$. This might end up with an unstable condition because the reference point goes beyond the operational limit of the converter, i.e. $U_{dc,ref}$ becomes very high, hence saturating the control system. In the following subsection, the limitations of the conventional droop method is assessed.

LIMITATIONS OF THE CONVENTIONAL DROOP METHOD

In order to show the limitations of the conventional *DroopCtrl* method, a droop curve step simulation is considered. An increase in the active power origin is performed such that the operating point of the converter lies on the left side of the droop curve, i.e. similar condition as illustrated in Figure 4.1.

Furthermore, the simplified test system in Figure 4.2 is considered. The DC resistances in Figure 4.2 is calculated to mimic the behavior of an MTDC system. Further description about this simplified test system can be found in Section E.3. The simulation is performed in PSCAD software with a simulation time step of 50 μ s.

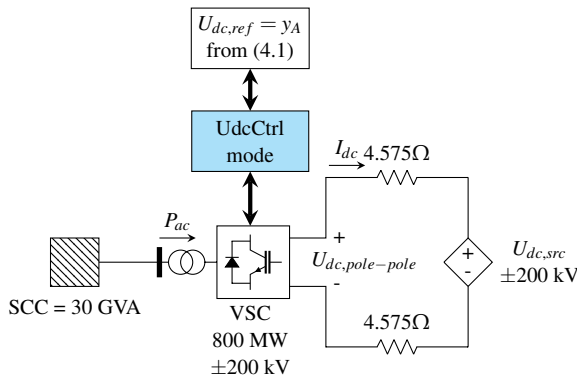


Fig. 4.2: The test system for droop step response test. The converter data is given in Section A.1.

The conventional *DroopCtrl* method formulated in (4.1) has been implemented in the

converter to calculate the new DC voltage reference for the existing *UdcCtrl*. Several droop constants ranging from 0.01 to 4 kV/MW are considered in the test having the same origin at 0 MW and ± 200 kV, i.e. depicted in Figure 4.3. A droop step is performed by changing the active power origin from 0 to 300 MW at 0.65 s (the test system takes 0.6 s to reach a steady-state).

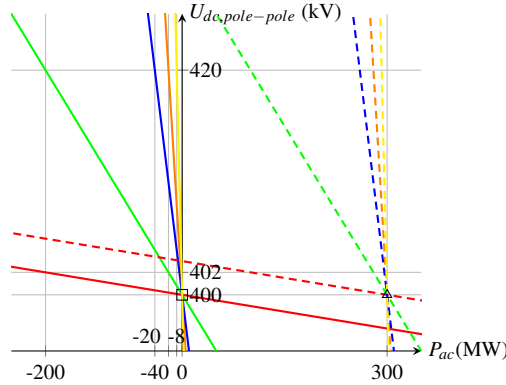


Fig. 4.3: The droop curve references for the step test. Five droop slopes have been considered: 0.01 (red), 0.1 (green), 0.5 (blue), 1 (orange), and 2.5 kV/MW (yellow). The solid and dashed lines represent the droop curves before and after the step, respectively. The step is performed by changing the droop origin from \square to \triangle .

As mentioned earlier, for a larger droop constant value, the new DC voltage reference by the *DroopCtrl* might be beyond the operational limits of the converter. Therefore, a hard limiter is also used to limit the new DC voltage reference, i.e. the operational limit of the converter is limited up to $\pm 5\%$ from the nominal value, ± 200 kV. The results with and without this hard limiter are given in Figure 4.4 for the droop constant of 0.01 to 1 kV/MW and Figure 4.5 for the droop constant of 2.5 kV/MW.

At 0.65 s, the converter condition is similar to the one depicted in Figure 4.1, i.e. on the bottom-left of the droop curve. The new DC voltage reference is then calculated by using this deviation and the droop constant. As an example, in Figure 4.4(a) ($k_{droop} = 0.01$ kV/MW), the DC voltage reference is increased from ± 200 kV to ± 201.5 kV. Therefore, for a droop constant value larger than 0.67 kV/MW, the new DC voltage reference becomes higher than the operating limits of the converter, i.e. can be seen in Figure 4.4(b)–Figure 4.4(d) and Figure 4.5.

With the new DC voltage reference, the existing *UdcCtrl* will adapt the converter's operating point to the referred value. As the DC voltage of the converter is increased, the active power injected to the DC grid is also increased. This means that the operating point of the converter moves to the right towards the new droop curve, i.e. illustrated in Figure 4.6(a) for $k_{droop} = 0.01$ kV/MW.

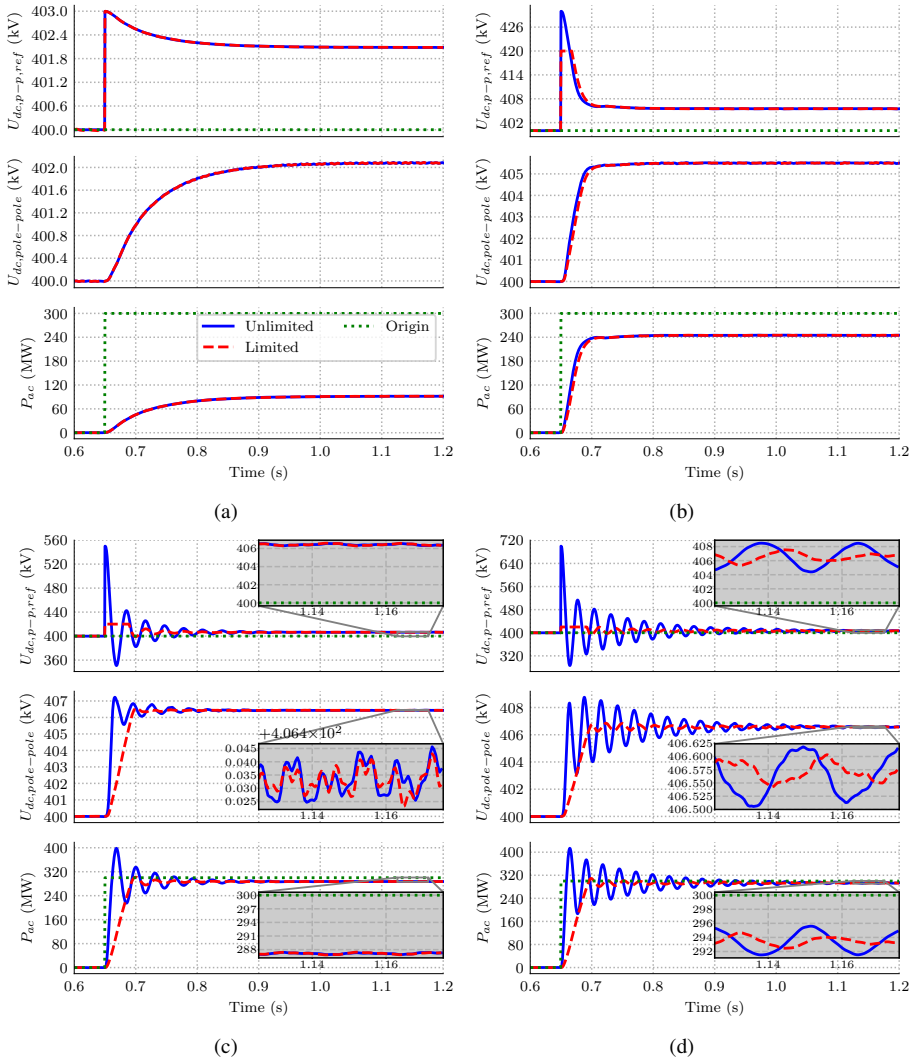


Fig. 4.4: The conventional *DroopCtrl* step test results for the droop constant of: (a) 0.01, (b) 0.1, (c) 0.5, and (d) 1 kV/MW. The blue waveforms represent the results when the new DC voltage reference is not limited, while the red ones represent the limited reference. The new DC voltage reference is shown in the top plot together with the DC voltage origin, while the measured DC voltage is shown in the middle plot. The bottom plot shows the measured and the origin or reference of the active power.

The higher the DC voltage reference step, the faster the converter responses. In Figure 4.4(a), the converter sees a 3 kV (pole-pole) step up when the active power origin is changed to 300 MW, and the rise time (time duration from 10% to 90% of the new level) of the DC voltage is around 0.1 s. Whereas in Figure 4.4(b), the new DC voltage

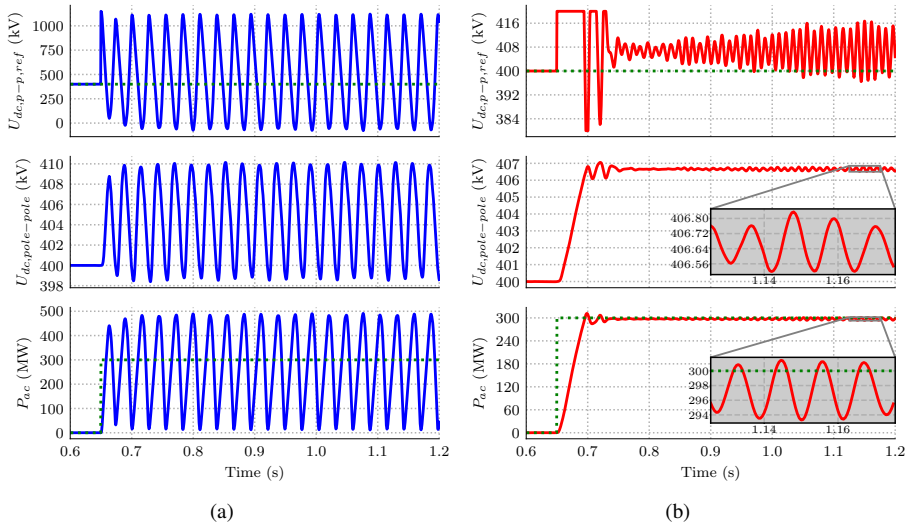


Fig. 4.5: The conventional *DroopCtrl* step test results for the droop constant of 2.5 kV/MW. The new DC voltage reference is: (a) unlimited, and (b) limited.

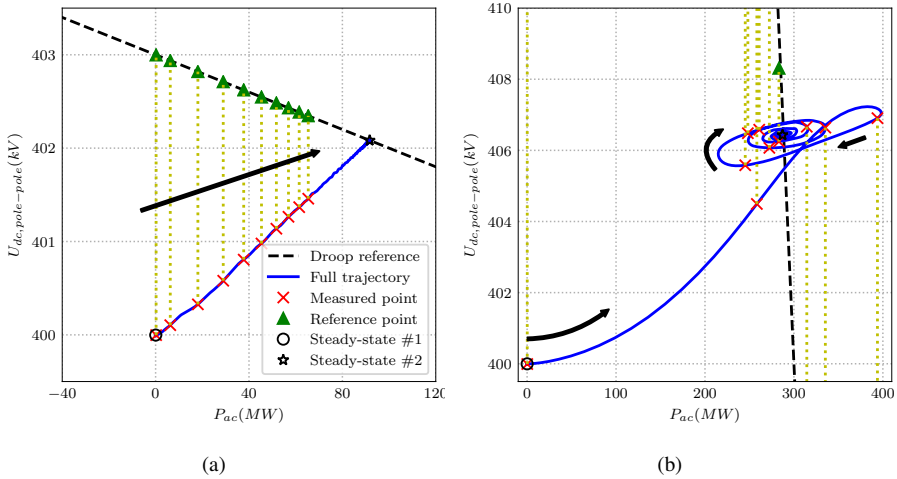


Fig. 4.6: The converter’s operating points trajectory when a 300 MW active power step is applied for the origin of a droop curve with a slope of: (a) 0.01 (Figure 4.4(a)) and (b) 0.5 kV/MW (Figure 4.4(c)). The trajectory direction is indicated by the arrows. The points denoted with Δ and \times represent the measured and referred DC voltage value at 0.65–0.74 s sampled every 0.01 s. The yellow dotted lines connect these measured and referred values. The operating points denoted with \circ and \star represent the steady-state condition before and after the droop curve is changed.

reference deviates 30 kV (pole-pole) from its previous value, and the rise time of the

DC voltage becomes half of the previous one (the one in Figure 4.4(a)).

The rise time in the DC voltage waveform is also reflected in the rise time of active power curve, i.e. the steeper the droop curve the faster the changes in the active power (with unlimited DC voltage reference). This can be seen in the blue waveforms of Figure 4.4(c)–Figure 4.4(d) and Figure 4.5(a).

For a droop value of 0.01 kV/MW (depicted in Figure 4.4(a)), the converter response is slow enough such that the operating points are always in the left side of the droop curve, i.e. depicted Figure 4.6(a). The deviation in the DC voltage reference from its origin is reduced as the operating point move closer to the droop curve.

However, for a steeper droop curve, the converter might experience oscillations. This is because the fast response of the converter might produce overshoot in the active power, which might pushes the operating point to the other side (right hand position) of the droop curve. Since, the new operating point is on the right of the droop curve, the new DC voltage reference is located below the measured one, which pushes the operating point back to the left side of the droop curve. This is depicted in Figure 4.6(b) and Figure 4.7, which shows the trajectory of the converter's operating points for $k_{droop} = 0.5$ kV/MW (Figure 4.4(c)).

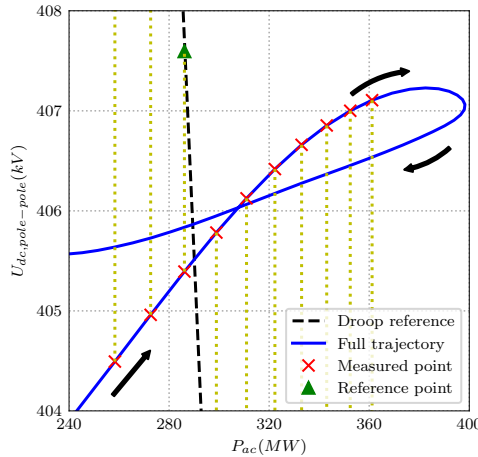


Fig. 4.7: The magnified plot of Figure 4.6(b). The trajectory direction is indicated by the arrows. The points denoted with \triangle and \times represent the measured and referred DC voltage value at 0.66–0.6645 s sampled every 500 μ s (the simulation time step is 50 μ s). However, most of the DC voltage references are outside the drawing plane and the yellow dotted lines connect these points with the measured ones.

Although by limiting the DC voltage reference might help reducing the oscillations, e.g. in Figure 4.4(c), the performance of the *DroopCtrl* for a higher droop constant still unstable, i.e. as can be seen in Figure 4.4(d) and Figure 4.5(b). The main reason

is because the new DC voltage reference changes rapidly although the operating point is located close the droop curve, which pushed the operating point back and forth from the left side to right side of the droop curve.

From the simulation results, there are some regions between the droop curve and the y -axis of the $P_{ac}-U_{dc}$ plane in which this mode could not be operated (unstable), i.e. droop curve with k_{droop} larger than 0.5 kV/MW. Therefore, the conventional *DroopCtrl* method could not be used to represent the *PacCtrl* mode, i.e. a straight vertical droop slope as depicted in Figure 3.5. This limitation also appear when the *DroopCtrl* mode is implemented as an extension of the existing *PacCtrl* mode (P_{ac} -based *DroopCtrl* method), i.e. the *DroopCtrl* could not be used to represent the *UdcCtrl* mode ($k_{droop} = 0$ kV/MW), explained in Appendix F. This is consistent with the explanation given in [40]:

"This control mode (the *UdcCtrl* mode) relates to a proportional control gain of infinity (in MW/kV). This of course is unrealistic and will lead to instability. Constant voltage control is therefore in reality not realized with an infinite gain, but with a PI controller. In theoretic steady state the outcome is the same, but due to dynamic reasons, the infinite control gain is not viable."

4.2.2. THE PRINCIPLE OF DLT

In theory, by changing the droop slope, a different converter control mode can be achieved, i.e. as depicted in Figure 3.5. However, as revealed in the previous subsection, when the value of k_{droop} for the conventional *DroopCtrl* method is increased, the control becomes more aggressive. This leads to instability of the conventional *DroopCtrl* method for a high value of droop constant. This is mainly because the inability of the DC voltage reference calculator, formulated in (4.1), to adjust the reference based on the distance of the operating point from the droop curve. Therefore, even if the operating point is close to the droop curve, the new DC voltage reference for a high k_{droop} value is far from the measured converter condition.

Furthermore, in the P_{ac} -based *DroopCtrl* method, the instability occurs for a low value of droop constant, to represent the *UdcCtrl* mode, which is consistent with the explanation given in [39]. Other disadvantages of the conventional *DroopCtrl* method especially related to the multi-slope droop control method are discussed in Subsection 4.2.7.

In order to mitigate this instability issue, the droop line tracking (DLT) method is proposed. This method is inspired by the line-follower robot, i.e. the robot movement is controlled in such a way that it can follow the designated line. The control of this

robot is realized by measuring the position of the robot from the designated track. Based on this distance the motors are actuated to keep straight or turn to any sides [103].

In DC system, the track is given as the droop line, while the converter acts like the robot controlled to follow this line. However, unlike the actuators in the line-follower robot, which can make the robot maneuver freely to any sides, the movement of the converter is only in one dimension and depends on the new DC voltage reference. This is because the changes in the AC–DC active power balance (x -axis movement) can be reflected as the changes in the DC voltage (y-axis movement) and vice versa (explained in Section 2.2). This means that the movement of the converter in the Cartesian plane is controlled by modifying the DC voltage reference ($U_{dc,DLT,ref}$) for the existing $UdcCtrl$ formulated in (4.2):

$$U_{dc,DLT,ref} = U_{dc,meas} + e_{pos} \quad (4.2)$$

where e_{pos} is the perpendicular distance of the converter "position" from the designated droop line.

The perpendicular distance is considered for the DLT method, because this is the closest distance between the converter's operating point and the droop curve. In Figure 4.8, e_{pos} can be calculated as the distance from the measured converter condition, $meas$ ($P_{ac,meas}, U_{dc,meas}$), to point C along the droop curve with a slope of θ .

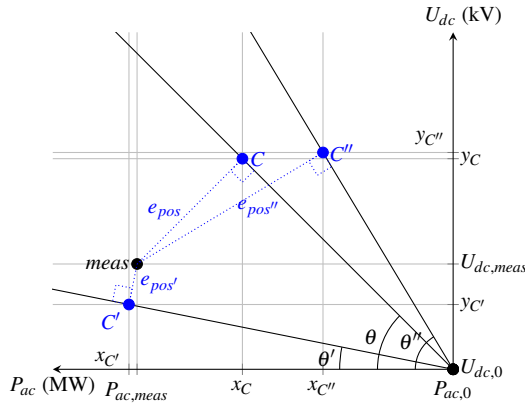


Fig. 4.8: The purpose of the DLT method is to reduce the displacement error (blue lines) such that the converter is operated along the designated droop line [102].

In order to calculate the perpendicular distance, the xy -axes should be converted such that they have the same length. This is because the DC voltage range is narrower and always has the same sign as compared to the active power, which can go from a negative to a positive value (power reversal possibility). This process is referred as the normalization process, which can also be seen as the translation of x -axis deviation

into y -axis movement. As an example, for a converter with ± 20 kV DC voltage deviation limits and ± 800 MW active power range, when this converter is operated in the *PacCtrl* mode using the DLT method, 800 MW power step increase is perceived as 20 kV increase in the DC voltage.

As compared to the conventional *DroopCtrl* method depicted in Figure 4.1, the new reference point using the DLT method is always within the converter's DC voltage operating limits regardless of the droop slope. In the conventional method, for θ'' , point A'' in Figure 4.1 is located high beyond the drawing plane (beyond the DC voltage operating limits). While in Figure 4.8, the reference point using the DLT is defined as point C'', which is the perpendicular projection of the measured operating point to the droop curve with slope angle θ'' . Figure 4.9 illustrates the comparison between the reference points generated using the conventional and DLT methods for various droop lines.

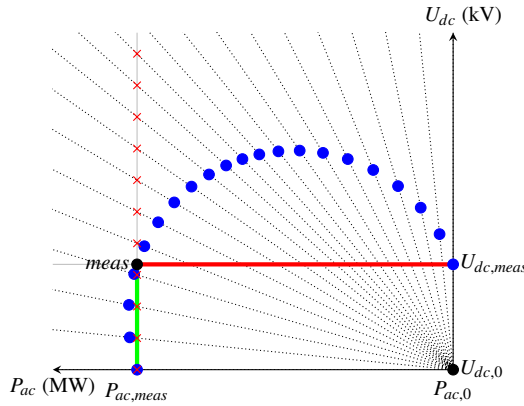


Fig. 4.9: The reference points generated using the conventional (red crosses) and DLT methods (blue dots) for various droop lines ($0 \leq \theta \leq \frac{\pi}{2}$). Some of the reference points generated using the conventional method are located beyond the drawing plane. The green line represent the perpendicular distance between the measured point to the droop line with $\theta = 0$, while the red one represents the distance to the droop line with $\theta = \frac{\pi}{2}$.

As can be seen in Figure 4.9, a high value of DC voltage reference can be avoided using the DLT method. Unlike the conventional droop method, the droop constant value is not used directly in the DLT method for calculating the new DC voltage reference for the converter, i.e. formulated in (4.2). Therefore, the DLT method is expected to cover a larger *DroopCtrl* region ($0 \leq \theta \leq \frac{\pi}{2}$) as compared to the conventional droop method.

When θ is zero (a constant DC voltage control), the perpendicular distance of the measured point to the droop line is illustrated as the green line in Figure 4.9. The value of e_{pos} is equal with the one calculated with the conventional droop method, i.e.

equals to the deviation in DC voltage (ΔU_{dc}) from $U_{dc,0}$.

In the case when $\theta = \frac{\pi}{2}$ (a constant active power control), the perpendicular distance of the measured point to the droop line is illustrated as the red line in Figure 4.9. At this condition, e_{pos} value equals to the deviation in active power (ΔP_{ac}) from $P_{ac,0}$. The DC voltage reference given to the existing *UdcCtrl* is adjusted such that ΔP_{ac} is reduced by converting this deviation into the y-axis movement. With the normalization process, the new DC voltage reference will never be beyond the limits, which will be explained in the following subsection.

For θ between zero and $\frac{\pi}{2}$, the converter is operated in the *DroopCtrl* mode. The *DroopCtrl* mode operates between the *UdcCtrl* and *PacCtrl* modes, e.g. the steeper the droop line slope means the *PacCtrl* mode behavior becomes more dominant and vice versa.

4.2.3. DC VOLTAGE REFERENCE DETERMINATION

In the DLT method, the new DC voltage reference following a disturbance is calculated based on the perpendicular distance (e_{pos}) between the converter's operating point with the droop curve. The processes to determine the new DC voltage reference are depicted in Figure 4.10.

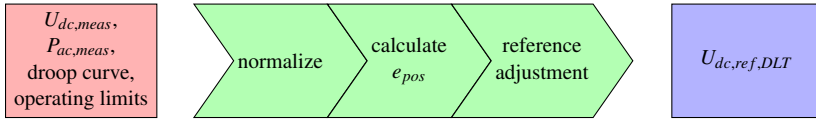


Fig. 4.10: The processes (green arrows) to determine the DC voltage reference (blue box) from the measured conditions and the droop curve (red box).

As the inputs for the DLT method, Figure 4.11 illustrates the droop curve along with the condition of the converter after a disturbance. Two new points are introduced for the purpose of calculating the perpendicular distance between the converter's operating point and the droop curve (e_{pos}). These points are represented by the red dots in the Figure 4.11. Normally, the droop curve is given as the droop constant (k_{droop}), the DC voltage, and active power origins. If the droop curve is used to represent the *PacCtrl* mode, the value of k_{droop} becomes infinite. Therefore, to avoid this infinite input, the droop curve is given to the DLT in the form of coordinates. It should be noted that in this subsection, only the single-slope droop concept is considered, while the multi-slope *DroopCtrl* method is explained later in Subsection 4.2.6.

The processes behind the DLT method are explained as follows:

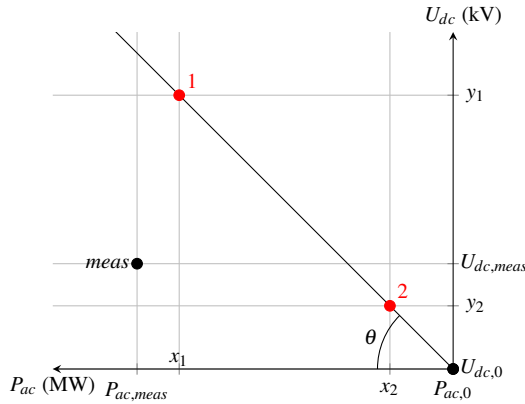


Fig. 4.11: The operating point (*meas*) of the converter following a disturbance. The droop curve is assumed to have a slope angle of θ . The two red dots are the new points introduced to represent the droop curve with a slope angle of θ .

NORMALIZATION

The normalization process is simply converting the xy -axes in the droop plane into a range of values between 0 to 1. By using the normalized values, the closest distance from the measured values to the droop line becomes independent from the droop slopes, e.g. in Figure 4.12 the same displacement distance is denoted as $e_{pos,N}$ for a straight vertical, a straight horizontal, and an ordinary droop slopes.

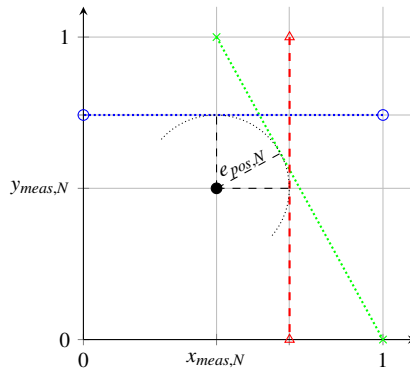


Fig. 4.12: An example of normalized droop characteristics with measured values at time t . Different droop slopes are represented by solid lines with different colors.

The value of 0 and 1 represent the limits of the converter, i.e. a normal operation beyond of these values is not expected. This means that in the x -axis, a value of 0 represents the maximum amount of the active power that can be injected by the con-

verter to the AC system (inverter operation), while a value of 1 defines the maximum amount of the active power that can be injected to the DC side (rectifier operation). For the y -axis, 0 and 1 represent the converter's maximum and minimum DC voltage operating limits.

Equation (4.3) formulates the normalization process for the points in Figure 4.11 ($meas$, 1, and 2) [102]:

$$\begin{aligned} x_{i,N} &= \frac{x_i - x_{min}}{l_x}, i = meas, 1, 2 \\ y_{i,N} &= \frac{y_i - y_{min}}{l_y}, i = meas, 1, 2 \end{aligned} \quad (4.3)$$

where x_{meas} and y_{meas} represent the measured active power and DC voltage, respectively, and l_x and l_y as the length of the x and y axis given in (4.4):

$$\begin{aligned} l_x &= x_{max} - x_{min} \\ l_y &= y_{max} - y_{min} \end{aligned} \quad (4.4)$$

where x_{max} and x_{min} represent the maximum and minimum active power that the converter can transmit, while y_{max} and y_{min} are the converter's maximum and minimum DC voltage deviation limits. Figure 4.13 illustrates an example of the normalized condition of the condition depicted in Figure 4.11.

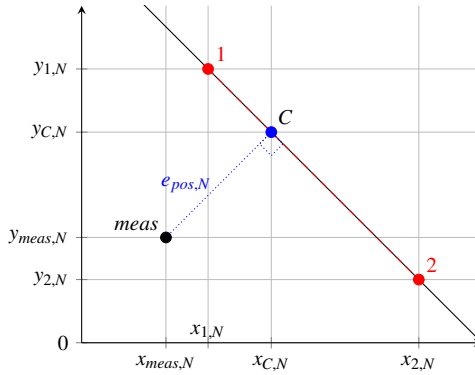


Fig. 4.13: Converter's condition depicted in Figure 4.11 is transformed into the normalized plane. Two additional points (red dots) are used to represent the droop curve (black line). The perpendicular projection of the measured values to the droop line is represented by the blue dot.

PERPENDICULAR DISTANCE CALCULATION

The coordinate of the perpendicular reflection of $meas$ to the droop curve (point C) can be determined using (4.5):

$$\begin{aligned} x_{C,N} &= \begin{cases} \frac{x_{meas,N} + ky_{meas,N} + k^2x_{1,N} - ky_{1,N}}{k^2 + 1} & \text{if } x_{2,N} \neq x_{1,N} \\ x_{1,N} & \text{if } x_{2,N} = x_{1,N} \end{cases} \\ y_{C,N} &= \begin{cases} y_{1,N} + k(x_{C,N} - x_{1,N}) & \text{if } x_{2,N} \neq x_{1,N} \\ y_{meas,N} & \text{if } x_{2,N} = x_{1,N} \end{cases} \end{aligned} \quad (4.5)$$

with k is given in (4.6):

$$k = \frac{y_{2,N} - y_{1,N}}{x_{2,N} - x_{1,N}} \quad (4.6)$$

The value of $e_{pos,N}$ can be calculated as the distance between $meas$ and point C , which can be formulated in (4.7):

$$e_{pos,N} = \sqrt{(x_{meas,N} - x_{C,N})^2 + (y_{meas,N} - y_{C,N})^2} \quad (4.7)$$

From (4.7), the value of $e_{pos,N}$ is always positive. However, in order to initiate the movement of converter's operating point, this value should be either positive or negative. The sign of $e_{pos,N}$ can be determined by considering the power flow between node i and j as formulated in (2.1). If it is assumed that node j is a U_{dc} -type node (DC slack node), an increase in DC voltage at node i means an increase of power flow towards node j . This can be seen as a movement towards the upper-right side of the droop plane. On the other hand, if the DC voltage at node i is reduced, the active power injected to the AC network through this node becomes larger, i.e. a movement towards the lower-left side of the plane.

Therefore, if the measured condition of a converter is in the lower-left side of the droop line, this converter needs to increase its DC voltage reference such that it can come closer to the droop line. Vice versa, this converter needs to decrease its DC voltage reference when the measured condition is in the upper-right side of the droop line. An example of this movement is shown in Figure 4.6(a) where the DC voltage reference is increased in order for the converter to come closer to the droop line. Hence, the sign convention of e_{pos} in (4.2) is formulated by (4.8) [102]:

$$\text{sign}(e_{pos,N}) = \begin{cases} + & \text{if the measured value below or left of the droop line} \\ - & \text{if the measured value above or right of the droop line} \end{cases} \quad (4.8)$$

REFERENCE ADJUSTMENT

Since $e_{pos,N}$ is a normalized value, it needs to be converted back into either the per unit or real value to be used as input for the existing $UdcCtrl$. In this thesis, it is assumed that the real value in kV is used as the input reference for the existing $UdcCtrl$. Therefore, the following equations formulate the conversion process:

$$e_{pos,kV} = e_{pos,N} l_y \quad (4.9)$$

where $e_{pos,kV}$ is the value of deviation (in kV) used to calculate the DC voltage reference, $U_{dc,base}$ equals to the DC voltage base value (in kV), and l_y is formulated in (4.4).

The value of DC voltage reference is then calculated by simply adding $e_{pos,kV}$ with the measured DC voltage, i.e. formulated in (4.2). This way, the existing $UdcCtrl$ is used to eliminate $e_{pos,kV}$, such that the operating point of the converter lies along the droop line.

4.2.4. THE DLT PERFORMANCE

In order to show the performance of the $DroopCtrl$ mode using the DLT method, the test system in Figure 4.14 is considered. This test system is similar to the one depicted in Figure 4.2, except that the DC voltage reference for the converter is generated by the DLT method (within the IFC box). This test system is implemented as well in PSCAD and a simulation time step of $50 \mu s$ is considered. The DLT method explained earlier is implemented as an external function in PSCAD. Further details in this matter are explained in Appendix D.

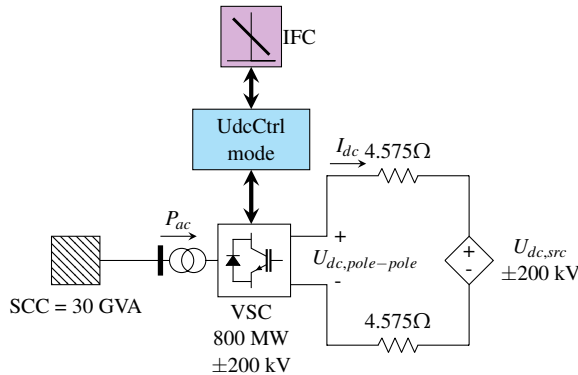


Fig. 4.14: The test system for droop step response test using the DLT method (purple box). The converter data is given in Section A.1.

Different droop constants ranging from 0.005 to ∞ kV/MW are considered, i.e. the droop line is formed by two points located at the edge of the operating limits of the converter. As an example in Figure 4.15, two points are considered: (-200,420) and (200,380), which represent a droop line with $k_{droop} = 0.1$ kV/MW. The y-coordinate of these points are the DC voltage limits of the converter. Different droop slopes are achieved by rotating the droop line in Figure 4.15 with (0,400) as the center of rotation. Hence, the x-coordinate of the two points for a low value of droop constant, e.g. (-800,411) and (800,395) for $k_{droop} = 0.01$ kV/MW, are the active power limits of the converter.

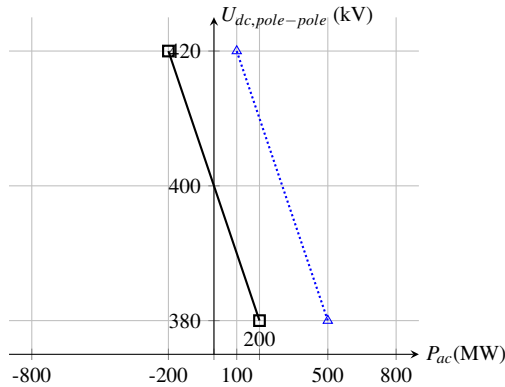


Fig. 4.15: The droop line reference ($k_{droop} = 0.1$ kV/MW) for the DLT in Figure 4.14. At 0.65 s, a 300 MW active power step up is applied at the droop line origin (0 MW and ± 200 kV), i.e. shifting the droop line from solid black (\square points) to dotted blue (\triangle points) line.

In Subsection 4.2.1, a 300 MW step is performed in the active power origin to show the performance of the conventional *DroopCtrl* method. Using the DLT, this can be perceived as shifting the droop line reference along the x -axis, e.g. depicted in Figure 4.15 for a droop constant of 0.1 kV/MW. The simulation results of the *DroopCtrl* step with various droop constants are shown in Figure 4.16. Furthermore, the trajectory in $P_{ac}-U_{dc}$ for some of these droop constants are shown in Figure 4.17.

As can be seen in Figure 4.16, the behavior of the converter with the DLT is similar to the conventional droop method operated with a low droop constant value (Figure 4.4(a)). Furthermore, the DC voltage reference generated by the DLT method never goes beyond the limits like in the conventional droop method. This is because the new DC voltage reference is not directly calculated based on the droop constant, like in the conventional method, but it is calculated based on the displacement distance from the droop curve. Therefore, the step response for different droop constants using the DLT method are quite similar to each other (having the same rise time of the DC voltage or active power).

The reference point (point C) pertains the projection of the converter's operating point

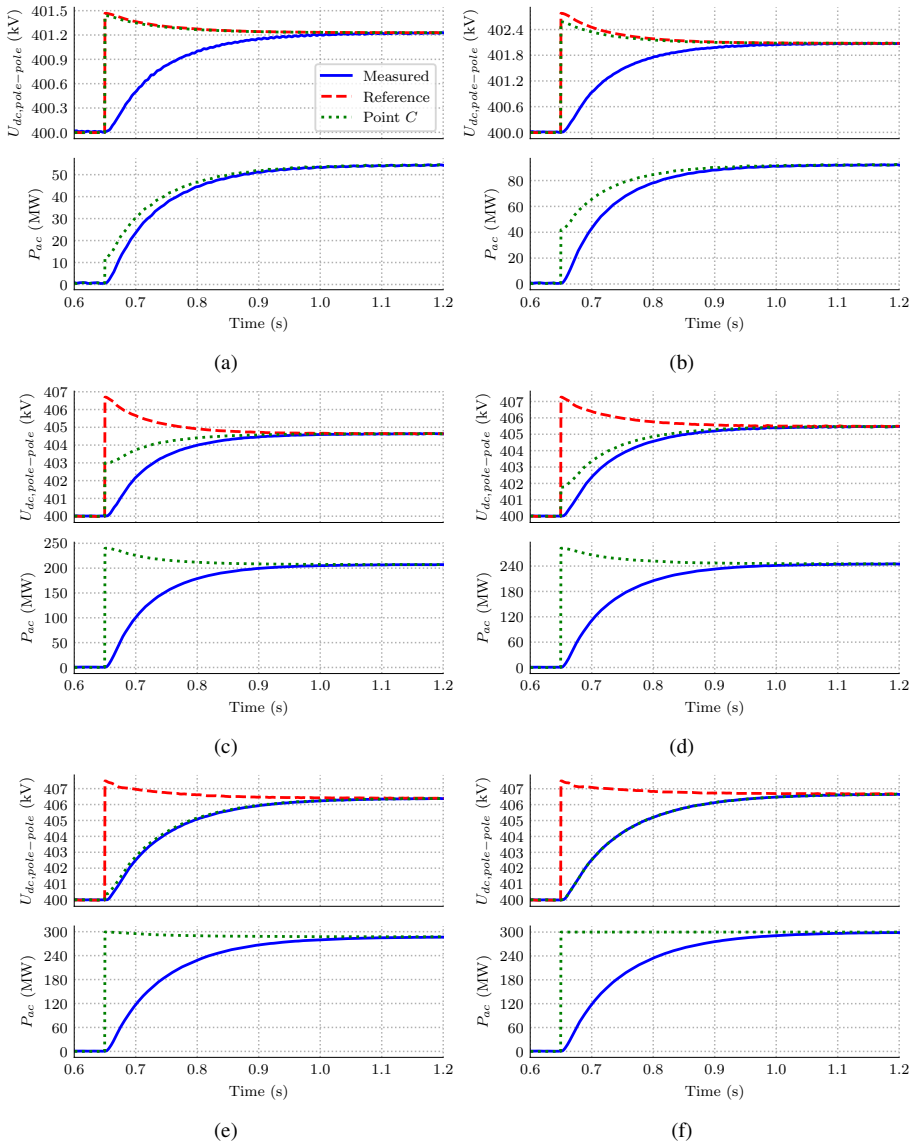


Fig. 4.16: The step test results of the *DroopCtrl* with the DLT method for the droop constant of: (a) 0.005, (b) 0.01, (c) 0.05, (d) 0.1, (e) 0.5, and (f) ∞ kV/MW. The blue waveforms represent the measured values, while the red ones represent the DC voltage reference given by the DLT. The perpendicular projection coordinates of the measured value to the droop line (point C) are shown by the green waveform.

to the droop line. Therefore, the location of point C changes depending on the droop slope. For a low k_{droop} value (e.g. Figure 4.16(a)), the location of point C is above of the measured condition of the converter. Therefore, the y-coordinate of point C

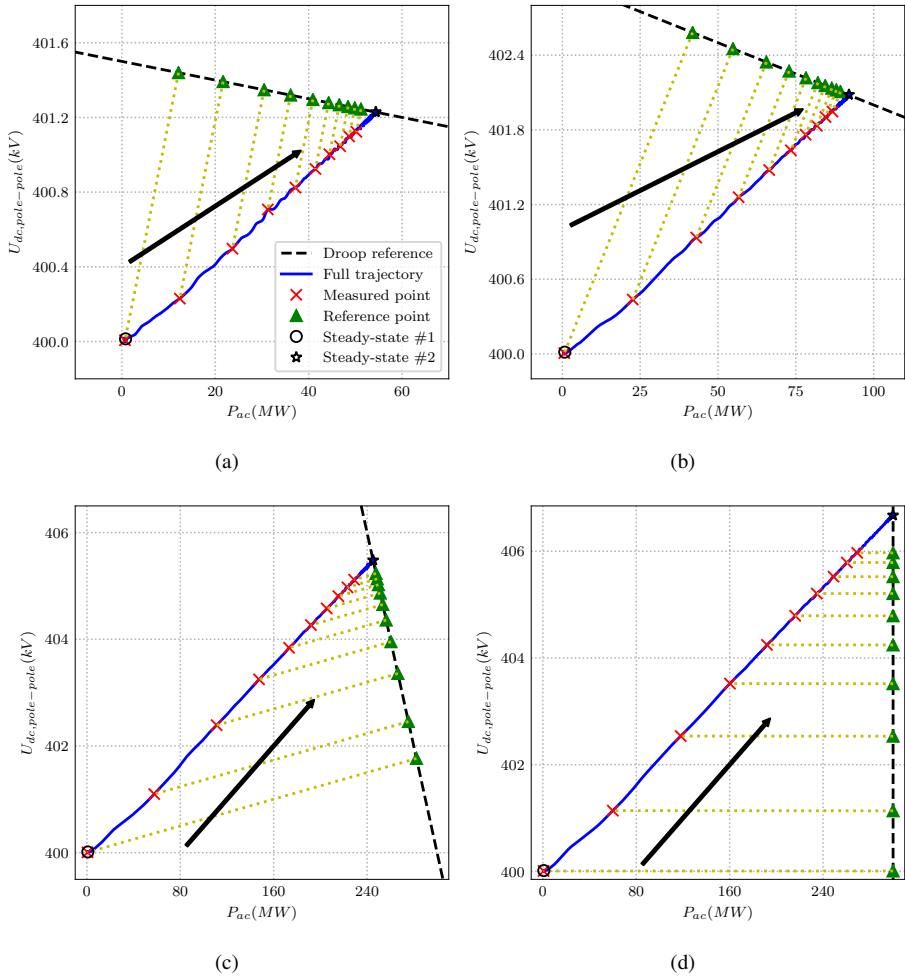


Fig. 4.17: The simulation results plotted in the P_{ac} - U_{dc} plane for the droop constant of: (a) 0.005, (b) 0.01, (c) 0.1, and (d) ∞ kV/MW. The trajectory direction is indicated by the arrows. The points denoted with \triangle and \times represent the measured and referred DC voltage value at 0.65–0.875 s. The yellow dotted lines connect these measured and referred values every 0.025 s. The operating points denoted with \circ and \star represent the steady-state condition before (0.6 s) and after the step (1.2 s).

(the green waveform in the first plot of Figure 4.16(a)) is almost equal to the new DC voltage reference (the red waveform in Figure 4.16(a)).

As the droop constant is increased, the location of point C is rotated from above to the right of the converter's operating point, which is consistent with the one depicted in Figure 4.9. This also means that the y-coordinate of point C becomes closer to the measured DC voltage, i.e. formulated in (4.5). Hence, the gap between the red and

green waveforms in the top plot of Figure 4.16(b)–Figure 4.16(f).

The highest DC voltage reference is reached when the converter is operated in the *PacCtrl* mode, i.e. $k_{droop} = \infty$ depicted in Figure 4.16(f). This is because point *C* lies on the right of the converter’s operating point, i.e. the same *y*-coordinate. The value of e_{pos} for this condition equals to 7.5 kV, which is calculated using (4.7) and (4.9). Hence, the new DC voltage reference is calculated as 407.5 kV (by employing (4.2)), which is well within the converter’s DC voltage limits and a lot lower as compared to the one from the conventional droop method.

The existing *UdcCtrl* is used to eliminate the displacement distance. This is shown in Figure 4.17, where the displacement distance is reduced as the converter’s operating point moves close to the droop line. Unlike in the conventional droop method, which could not recognize the distance from the measured converter condition to the droop curve, the DLT method uses this distance to calculate the new DC voltage reference. This means that the back and forth oscillation across the droop line like in the conventional droop method can be avoided.

Therefore, the existing *UdcCtrl* can be operated in the *DroopCtrl* and *PacCtrl* modes by using the DLT method. These different control modes can be achieved by simply changing the droop slope, which confirms the theory depicted in Figure 3.5. Furthermore, since the new DC voltage reference calculated using the DLT method is always within the limits, the converter performance operated in different control modes following a disturbance is quite similar.

***UdcCtrl* MODE**

In order to see the step response of the *UdcCtrl* mode, the test system depicted in Figure 4.18 is considered. By using this system, the DC current is always kept constant (zero), hence the DC voltage step response represent only the behavior of the *UdcCtrl* without the influence from the DC system. Further details on this test system can be found in Section E.1. This system has been implemented in PSCAD software with the same configuration as the one used before.

As same as in the previous simulation cases, this test system takes 0.6 s to reach steady-state. At 0.65 s, the DC voltage reference is increased from ± 200 kV to ± 205 kV, i.e. by shifting the droop line up as depicted in Figure 4.19 as the input for the DLT method. This step up value of the DC voltage reference is chosen in such a way that the response can be measured without saturating the controls. The simulation results is shown in Figure 4.20, i.e. by comparing the step performed only using the existing *UdcCtrl* (without the DLT) and when the DLT is used.

As can be seen in Figure 4.20, the DC voltage step response of both DLT and the

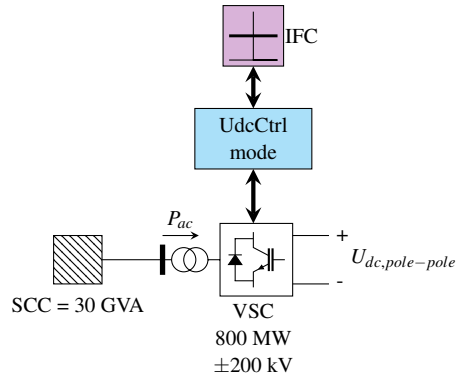


Fig. 4.18: The test system for U_{dc} step response test. The converter data is given in Section A.1.

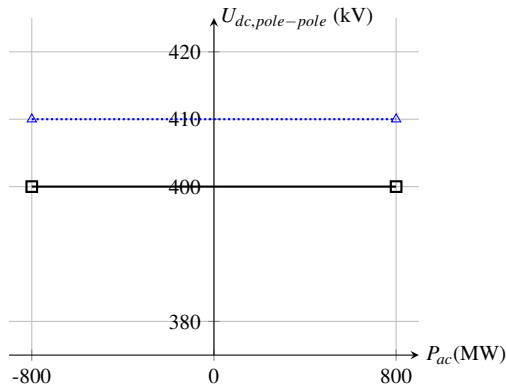


Fig. 4.19: The DLT method's droop line reference for U_{dc} step response test. At 0.65 s, a 10 kV DC voltage step is applied, i.e. shifting the droop line up from solid black (\square points) to dotted blue (\triangle points) line.

conventional method have exactly the same response. This is expected since in this case, the droop curve is a straight horizontal, so the perpendicular distance between the curve and the operating point equals the difference between the measured and the referred DC voltage. Hence, the exact same error is determined by both the DLT and the conventional method. For the DLT method, the calculated displacement error in the beginning of the step confirms (4.9), i.e. $e_{pos,kV}$ equals to 10 kV.

PacCtrl MODE PERFORMANCE

With the DLT method, the existing *UdcCtrl* can be used to mimic the behavior of the *PacCtrl*. The DLT provides an appropriate DC voltage reference such that the converter operating point lies along a straight vertical droop line. The existing *UdcCtrl*

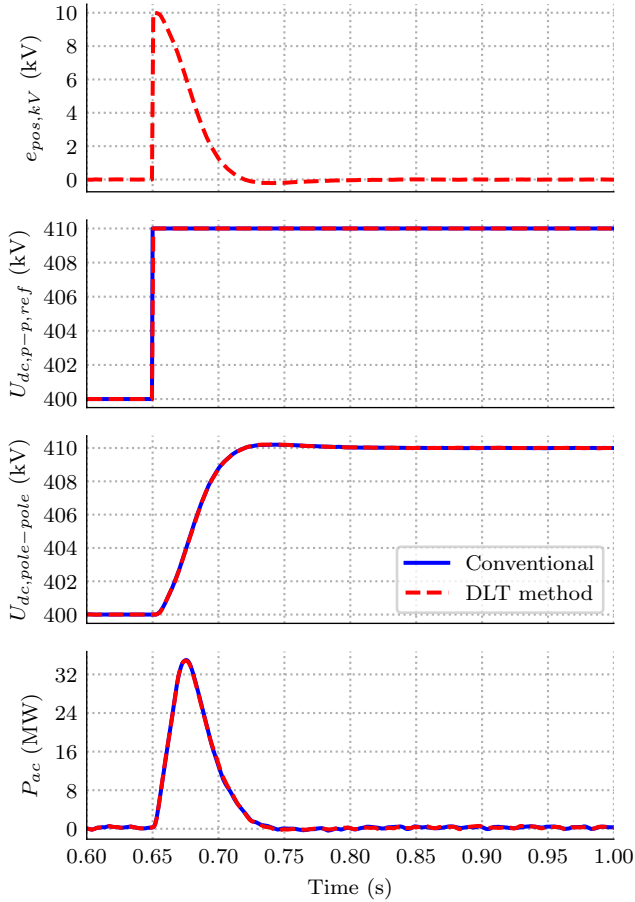


Fig. 4.20: DC voltage step response results. The top plot is the $e_{pos,kV}$ calculated using (4.9). The middle plots are the referred and measured DC voltage, while the bottom plot is the measured AC active power response. The blue and red waveforms represent the results acquired using the existing $UdcCtrl$ and the DLT method, respectively.

then adjusts the operating point of the converter based on the referred DC voltage given by the DLT. Hence, the time response of the $PacCtrl$ mode relies on how fast the existing $UdcCtrl$ changes its operating point.

In order to see the step response of the $PacCtrl$ mode, the test system depicted in Figure 4.21 is considered. By using this system, the DC voltage is always kept constant, hence no additional energy is stored in the converter capacitance such that the converter is isolated from the DC-side non linearities. Further details on this test system can be found in Section E.2. This system has been implemented in PSCAD software with the same configuration as the one used before.

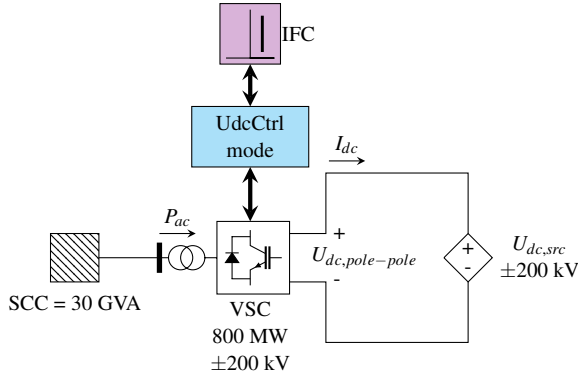


Fig. 4.21: The test system for P_{ac} step response test. The converter data is given in Section A.1.

With this test system, the $PacCtrl$ mode using the DLT method is compared with the realistic $PacCtrl$ implementation (the one used in Figure E.7). The active power step test is performed for comparing both $PacCtrl$ approaches. For the DLT method, this can be perceived by shifting the droop line to the right as depicted in Figure 4.22.

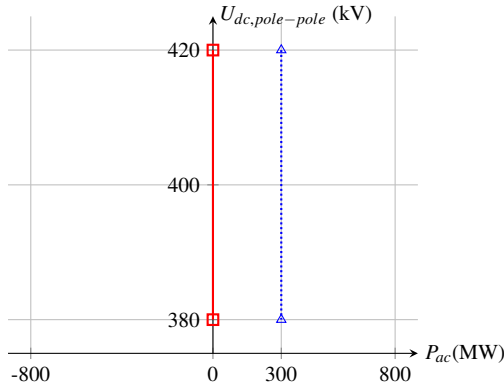


Fig. 4.22: The DLT method's droop line reference for P_{ac} step response test. At 0.65 s, a 300 MW active power step is applied, i.e. shifting the droop line from solid red (\square points) to dotted blue (\triangle points) line.

In general, the design of the outer control loops is based on the assumption that the inner controls can be comprised as a first-order system [24]. The tuning of $PacCtrl$ is more straightforward, i.e. the gains of the controller are determined to regulate the first-order (current control) system. While, in $UdcCtrl$, the DC system capacitance needs to be considered (described in Subsection 4.3.1) in determining the controller gains. The gains of the "real" or conventional $PacCtrl$ (given in Table A.3) are tuned such that the $PacCtrl$ has the same step response as the $UdcCtrl$. This can be seen by comparing the results shown in Figure E.2 for $UdcCtrl$ with the ones shown in Figure E.8 for $PacCtrl$. When using the $UdcCtrl$ gains for $PacCtrl$ and a scaled-down

error value, the *PacCtrl* might experience an under-damped behavior, i.e. shown in Figure 4.23.

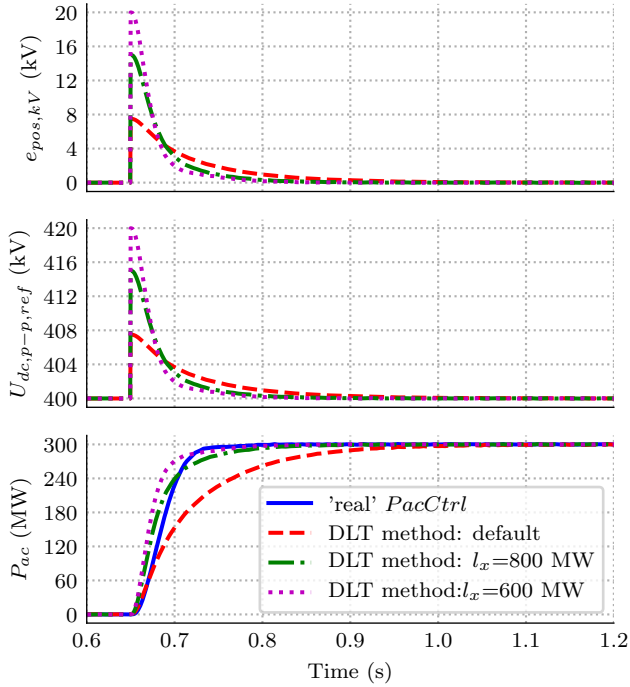


Fig. 4.23: Comparison of active power step response between the DLT method against the existing *PacCtrl* (blue line). The *basic* setting of the DLT method is represented by the red line, while the green and magenta lines represent the operation of the DLT method with reduced l_x .

The conversion of the perpendicular error into y-axis movement is formulated in (4.3). When the active power limits of the converter are reduced (l_x value in (4.4) is reduced), the $e_{pos,kV}$ value becomes larger. Hence, the converter becomes more sensitive to the changes in the x -axis direction. This can be seen in Figure 4.23 as the green and magenta line, where the value of l_x is reduced from 1600 MW (default) to 800 and 600 MW, respectively.

Although by reducing the value of l_x improves the time response of the *PacCtrl* mode using the DLT, this approach can only be applicable when the expected active power deviation of the converter is limited. This is because the operating limit of the converter is reduced to a smaller value than what the converter could achieve. Therefore, it might end up with a high $U_{dc,DLT,ref}$ value beyond the operating limits of the converter, when the active power deviates beyond the l_x value. Therefore, the behavior of the converter might be different if l_x value is modified.

4.2.5. CONVERTER CONTROL MODE SHIFT

Due to instability when the U_{dc} -based droop method to represent the *PacCtrl* mode, or P_{ac} -based droop method to represent the *UdcCtrl* mode, both *UdcCtrl* and *PacCtrl* modes should be made available in the converter. Each of these control modes might use PI-control to eliminate the error between measured and referred values [48]. Therefore, switching from one control mode to another might become a complicated process since it involves the shift of the PI-control state. If the state is not properly shifted, a transient might occur.

To illustrate this condition, a test system depicted in Figure 4.24 is considered. This test system is similar to the one shown in Figure 4.14, except that the value of the DC resistors is changed. The value is changed such that when the DC voltage different between the converter terminal and $U_{dc,src}$ reaches 10 kV for each pole, the active power transmission level reaches approximately 800 MW.

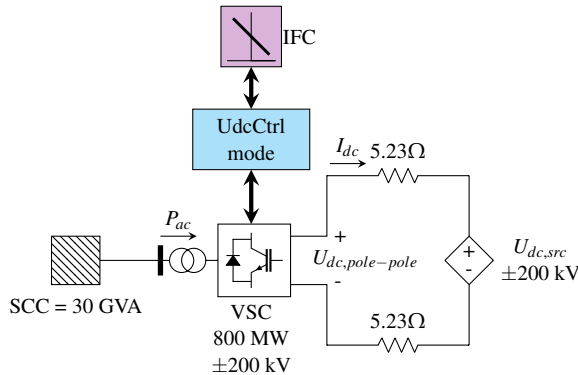


Fig. 4.24: The test system for droop step response test using the DLT method (purple box). The converter data is given in Section A.1.

Furthermore, it is also assumed that the P_{ac} -based droop (explained in Appendix F) is considered instead of the U_{dc} -based droop method used before. In this case, the DC voltage source, $U_{dc,src}$ is ramped-up from ± 200 to ± 206 kV with a ramp speed of 10 kV/s, e.g. to simulate an increase of OWF production in an offshore MTDC system. When the $U_{dc,src}$ voltage is increased, the converter is operated in *DroopCtrl* mode. However, when there is no surplus of power, the converter stays in *UdcCtrl* mode. Furthermore, the maximum DC voltage deviation is assumed to be ± 205 kV. Hence, the events listed in Table 4.1.

The simulation results using the P_{ac} -based *DroopCtrl* method are depicted in Figure 4.25. However, during the start-up process, the converter is operated in *UdcCtrl* mode, instead of the P_{ac} -based *DroopCtrl* mode, with the reference of ± 200 kV. Although it might be operated directly in P_{ac} -based *DroopCtrl* mode, this step is not

Table 4.1: The droop line variations events.

Time	Event	Corresponding droop in Figure 4.26
0.00	Start-up process, $UdcCtrl$ mode is active	red line
0.65	DroopCtrl is active with $k_{droop} = 0.5$ kV/MW	blue line
1.20	$DroopCtrl$ is active with $k_{droop} = 0.125$ kV/MW	green line
1.30	$U_{dc,src}$ is ramped-up to ± 206 kV for 1.2 s	-
3.10	$UdcCtrl$ is active with $U_{dc,ref} = \pm 205$ kV	yellow line

considered since it increases the duration of the start-up process.

At 0.65 s, the converter control is shifted from the $UdcCtrl$ to the P_{ac} -based $DroopCtrl$ mode, which creates overshoot in both U_{dc} and P_{ac} . The overshoot happens since the existing converter control does not have the capability to properly update the states between the $UdcCtrl$ and $PacCtrl$ modes. It was found that a k_{droop} of 0.5 kV/MW is needed in order for the system to reach a new steady-state after this overshoot. If a lower value of droop constant is used (e.g. $k_{droop} = 0.125$ kV/MW), the system becomes unstable after this overshoot.

Another overshoot occurs when the converter mode is shifted back to $UdcCtrl$ at 3.1 s. This overshoot becomes more prominent because the $UdcCtrl$ state is not updated correctly when the new DC voltage reference is enforced, i.e. ± 205 kV.

For the DLT method, the events in Table 4.1 can be represented by different droop lines. Similar to the previous test, the droop lines are formed by two points, which are located at the edge of the operating limits of the converter illustrated in Figure 4.26.

When the DLT method is used, the converter stays in $UdcCtrl$ mode, although the operation is changed according to the events listed in Table 4.1. This can be seen in Figure 4.25 where there is no control mode shift required when DLT is activated. To achieve different control mode, the droop line reference for the DLT method is changed, i.e. as depicted in Figure 4.26. Hence, a seamless control mode shift can be achieved using the DLT method.

At 1.3 s, the $U_{dc,src}$ voltage is increased, hence increase in power transmitted from the DC system to the AC system. Since the converter is in $DroopCtrl$ mode, the deviation in active power results in deviation of DC voltage, which can be achieved by using both the P_{ac} -based droop and the DLT methods. However, since the DLT method has a slower response as compared to the existing $PacCtrl$ mode (described in Subsection 4.2.4), the static error during the ramping process is larger in the DLT method compared to the P_{ac} -based droop method. As can be seen in Figure 4.25, the difference from the P_{ac} -based droop method is around 0.15 kV and 6 MW. Figure 4.27

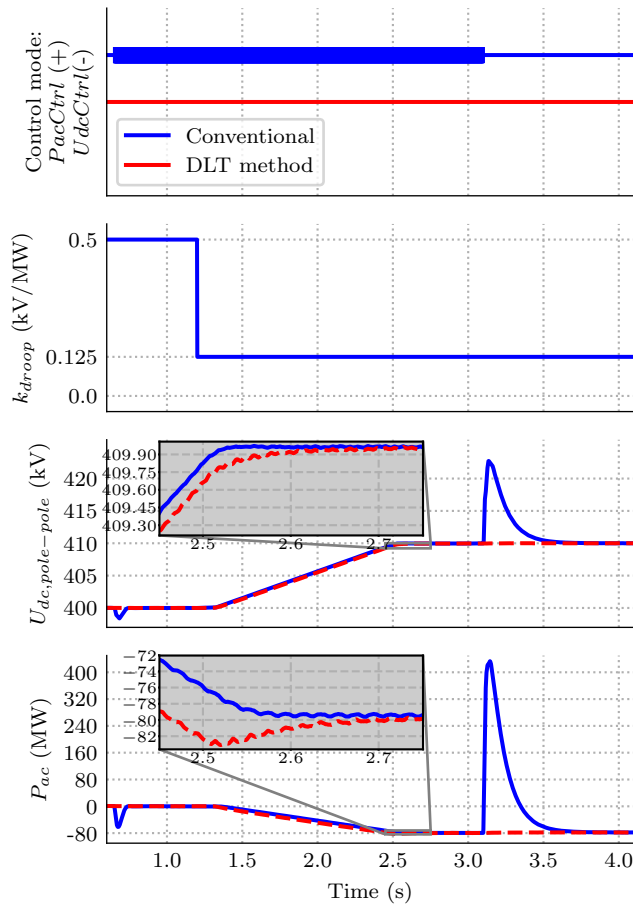


Fig. 4.25: Converter control mode shift results comparison between the conventional and DLT methods. In the top most plot, the $PacCtrl$ mode activation is indicated by the bold line, while a thinner line reflects $UdcCtrl$ mode operation.

confirms the difference between the two methods during the ramping process.

4.2.6. GENERALIZED DLT METHOD

The advanced converter control mode can be implemented using the DLT method by merely changing the single slope droop line with the multi-slope droop line, i.e. the ones depicted in Figure 3.7. The new DC voltage reference given by the DLT method after a disturbance is used to drive the converter to operate along the PWL droop line. This way, the DLT method calculates the new DC voltage reference by measuring the displacement distance from either one of the PWL line segments.

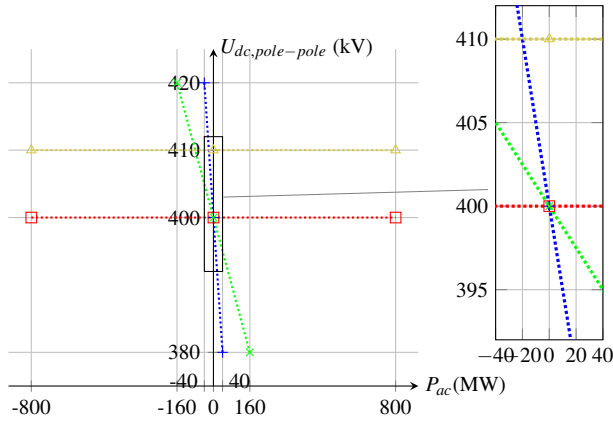


Fig. 4.26: Droop line variations for DLT method. The droop characteristics of the converter are varied from the red to blue to green and then to yellow lines, i.e. as listed in Table 4.1.

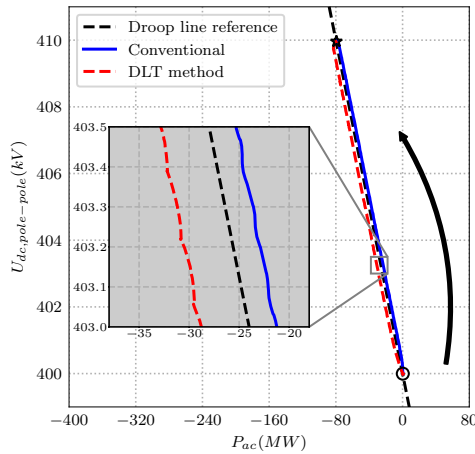


Fig. 4.27: Control mode shift results plotted in $P_{ac}-U_{dc}$ plane. The dashed black line represents the droop line characteristics, while the arrow points the movement direction. The points marked with \circ and \star represent measured values for both methods at 1.25 s and 2.85 s respectively.

Therefore, more points (represent a PWL line’s knee points) are given as the input for the DLT method to get a generalized solution for the basic (a single slope) and advanced converter control modes. The PWL line coordinate pair, (X'_{PWL}, Y'_{PWL}) , is received from the droop shift component in Figure 3.16, i.e. if dx is zero then the coordinate pair is equal to the one coming from the DC grid secondary control, (X_{PWL}, Y_{PWL}) . In this thesis, the input of coordinate pairs for the DLT method is limited to a maximum of 7 pairs, which can be used to represent 6 PWL line segments. This number is

chosen based on the example given in [16]. If more segments are required, the size of the (X_{PWL}, Y_{PWL}) from the DC grid secondary control is simply increased.

Due to the power flow sign convention, these pairs are sorted in such a way to represent the droop line from the top-left to the bottom-right corners of the droop plane. The first PWL line coordinate represents the converter's minimum active power and maximum DC voltage limits, while the last one represents the maximum active power and minimum DC voltage limits.

In addition to the PWL line segments, another feature of the DLT method is the ability to be operated for different droop relationships. Although the explanation of the DLT concept considers only the $P_{ac}-U_{dc}$ relationship, the same explanation can be made with the other relationships as well. This is because, the principle of the DLT method is to provide the appropriate reference such that the converter's operating point lies along the curve. This reference is calculated based on the distance between the operating point of the converter to the droop line. By using the normalized values, the calculation is performed unit less. Hence, the complete structure of the DLT method, which allows different droop relationships and advanced control implementation, is depicted in Figure 4.28. Further explanations of each component are given as follows:

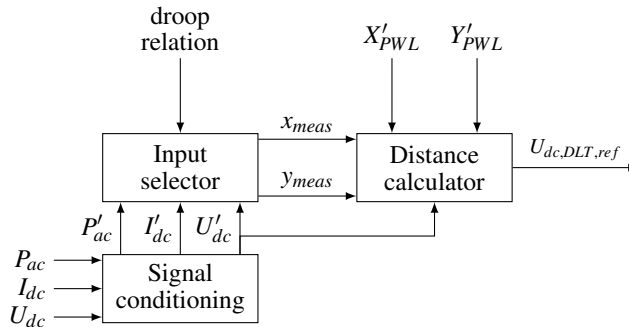


Fig. 4.28: The DLT method structure. This structure is the one inside the DLT box depicted in Figure 3.16.

SIGNAL CONDITIONING

In this component, the measurement signals are processed by amplification, filtering, or other necessary processes, e.g. to filter out the noise from the measurement units. Furthermore, this component prepares the measured active power and DC current to have the same convention as the one used by the DC grid control. As in [16, 35, 43, 102], the following sign convention used in this thesis for I_{dc} and P_{ac} is as follows:

- positive \Rightarrow rectifier operation

- negative \Rightarrow inverter operation

This part is not used in the previous tests, because it is already assumed that the measurement signals follow the same convention used by the DLT method and have been filtered to remove the measurement noise with a low-pass filter having a time constant of 0.02 s (1-cycle of the AC frequency).

INPUT SELECTOR

This component selects the corresponding measurement signals pair (x_{meas} and y_{meas}) depending upon the droop relationship, i.e. described in Subsection 3.2.2 and formulated in (4.10).

$$\begin{aligned} x_{meas} &= \begin{cases} P'_{ac} & \text{if } P_{ac}-U_{dc} \text{ or } P_{ac}-U_{dc}^2 \text{ active} \\ I'_{dc} & \text{if } I_{dc}-U_{dc} \text{ active} \end{cases} \\ y_{meas} &= \begin{cases} U'_{dc} & \text{if } P_{ac}-U_{dc} \text{ or } I_{dc}-U_{dc} \text{ active} \\ (U'_{dc})^2 & \text{if } P_{ac}-U_{dc}^2 \text{ active} \end{cases} \end{aligned} \quad (4.10)$$

where the apostrophe indicates the post-processed signals from the measurement units. Furthermore, the unit for both measurement and droop line coordinate pairs should match, i.e. U_{dc} in kV, I_{dc} in amperes, and P_{ac} in MW. When $P_{ac}-U_{dc}^2$ is used, the y-axis is in GV^2 .

Generally, the droop relationship for a particular converter is kept unchanged during the operation of the system. Furthermore, as mentioned earlier and shown later in Subsection 4.2.8, the dynamic responses of different droop relationships are the same. Therefore, each converter within the MTDC system might use the same or different droop relationship [79].

DISTANCE CALCULATOR

The principle of this component has been explained in Subsection 4.2.3. The changes to allow a generalized solution are listed as follows:

Normalization The normalization are performed using (4.3) for every coordinate listed in X'_{PWL} and Y'_{PWL} . Furthermore, since the converter operating limits are included in the X'_{PWL} and Y'_{PWL} , the value of x_{min} , y_{max} , x_{max} , and y_{min} for (4.4) are the first and the last PWL knee points' coordinates.

Perpendicular distance calculation In Subsection 4.2.3, only two points are considered to reflect the droop slope. In this generalized DLT approach, the multi-slope droop curve is considered, i.e. several droop segments stacked into a PWL line. However, the DLT method used for the multi-slope droop curve still has the same principle as explained in Subsection 4.2.3, i.e. to bring the converter operating point along the referred droop line by considering the closest distance from the measured converter's condition to the droop curve.

Therefore, the first step is to determine which droop segment is the closest one to the operating point of the converter. This can be achieved by determining the closest knee point of the PWL line from the measured converter's condition. This step can be performed by replacing point C in (4.7) for each of the droop knee points to evaluate the perpendicular distance from the converter's operating point.

In order to give an example, the condition depicted in Figure 4.29 is utilized. Two converter's operating points are considered, i.e. $meas1$ and $meas2$. These operating points reflect the converter's conditions following two distinct disturbances.

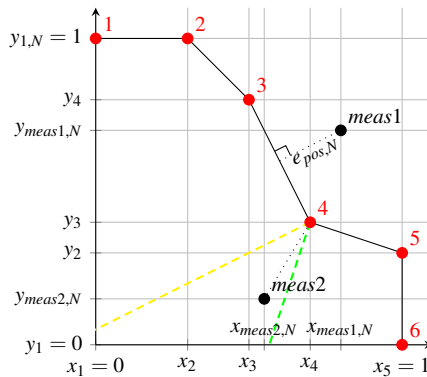


Fig. 4.29: An example of a normalized multi-slope droop characteristic with two measured converter conditions, i.e. $meas1$ and $meas2$. The subscript N represents the normalized value. The red numbers represent the droop knee point index. The dashed yellow line is the perpendicular line of segment 3–4 from point 4, while the dashed green line is the one of segment 4–5. The perpendicular reflection of $meas2$ to the droop curve can not be determined, since it lies below-right of the dashed yellow line and above-left of the dashed green line.

It should be noted that the evaluation of the closest knee point is performed from the top-left PWL point to the bottom-right. So, point 3 is considered as the closest knee point from $meas1$, although point 4 also has the same distance from $meas1$. Whereas for $meas2$, point 4 is the closest knee point from it.

After knowing the closest droop knee point, the value of $e_{pos,N}$ can then be calculated using the same procedure formulated in (4.5)–(4.7), i.e. explained in Subsection 4.2.3. The location of the reference point (point C), determined using (4.5), is between this

closest knee point and the knee point before or after it. For *meas1*, point *C* is located in segment 3–4 instead of 2–3, so the value of $e_{pos,N}$ is then calculated using (4.7) by considering this PWL line segment.

However, the perpendicular reflection from *meas2* cannot be determined. This is because the location of *meas2* is below-right of the yellow line and above-left of the green line in Figure 4.29. The yellow line represents the boundary of the perpendicular reflection to PWL segment between point 3 and 4, while the green one represents the boundary of the perpendicular reflection to segment 4–5.

This condition reflects the transition between one droop segment to another one, which does not exist in the single-slope droop line discussed in Subsection 4.2.3. Therefore, when the perpendicular point cannot be determined, the absolute distance between the operating point to the closest PWL knee point is then directly given as the value of $e_{pos,N}$, e.g. the absolute distance from the *meas2* to point 4.

The typical trajectory of the converter's measured condition following a droop step is from the bottom-left to the upper-right corner, e.g. depicted in Figure 4.17. Therefore, although $e_{pos,N}$ is given as the absolute distance from the *meas2* to point 4, this does not necessarily mean that the new steady-state point after the step lies in point 4. It might happen that after given this value, the new converter condition goes below segment 4–5, i.e. the perpendicular reflection can be determined.

As can be seen in Figure 4.29, the largest region where the perpendicular reflection point cannot be determined happens for the "L"-shaped PWL segments. This means that, when the measured converter's condition located at the bottom-left of this "L"-shaped PWL segments (similar to *meas2*), the transition between the *UdcCtrl* to *PacCtrl* (or the way around) is realized by giving the knee point of this "L"-shaped PWL segments for calculating the value of $e_{pos,N}$.

However, if the measured condition is located at the upper-right of the "L"-shaped PWL segments, the perpendicular reflection of the measured condition exists in each segment of this "L"-shaped PWL segments. In this case, the shortest distance between the operating point to each of them is the one considered as the value of $e_{pos,N}$. This condition will be shown later in Subsection 4.2.7.

Reference adjustment The conversion of $e_{pos,N}$ to the kV value formulated in (4.9) can be used for both for the $P_{dc}-U_{dc}$ and $I_{dc}-U_{dc}$ relationships. However, for the $P_{dc}-U_{dc}^2$ relationship, the y-axis unit is in GV^2 . Therefore, the following equation should be considered:

$$e_{pos,kV} = \begin{cases} e_{pos,N} l_y & \text{if } P_{ac}-U_{dc} \text{ or } I_{dc}-U_{dc} \text{ active} \\ \sqrt{(e_{pos,N} l_y) \times 10^3} & \text{if } P_{ac}-U_{dc}^2 \text{ active} \end{cases} \quad (4.11)$$

where l_y is formulated in (4.4).

4.2.7. THE ADVANCED CONVERTER CONTROL

The converter control mode shift explained in Subsection 4.2.5 becomes the basis of an advanced converter control mode. With this control, the converter is operated in either *PacCtrl*, *UdcCtrl*, or *DroopCtrl* mode depending on the condition of the converter, e.g. depicted in Figure 3.7. A state machine is used in [76] to detect the DC voltage condition of the converter and activate the appropriate converter control mode. However, this approach fails to consider a constant voltage dead-band characteristics, i.e. as depicted in Figure 3.7(c). This is because the state machine only monitors the changes in DC voltage to shift between different control modes. Furthermore, an oscillation has been revealed during the transition from one to another control mode [76].

In [83], a cascaded control structure is used to represent a two-stage voltage droop control. Similar to the one used in the converter's RMS control, two control layers have been used, i.e. *outer* and *inner* control. However, instead of using the output of the *outer* control as the input for the *inner* control, the output of the *outer* control is used to limit the *inner* control. So, the shift between two control modes is achieved by saturating the *inner* control loop. If the PWL segments are increased, there should be another control loop implemented. Thus, the control structure becomes more complicated.

When the DLT method is used, the control structure is not changed, but only the input droop line coordinates that are changed to represent a PWL line. Figure 4.30 shows a 6-segment PWL line characteristic to represent the advanced converter control operation.

To test the DLT behavior, the same test system as in Subsection 4.2.5 (as depicted in Figure 4.21) is considered. The $U_{dc,src}$ value is varied according to the events given in Table 4.2. The simulation results of the advanced droop control operation are depicted in Figure 4.31.

Table 4.2: Ramp-up events of the $U_{dc,src}$.

Time	Event
0.00	Start-up process, $U_{dc,src} = \pm 200$ kV
0.65	$U_{dc,src}$ is ramped-up to ± 205 kV for 1.0 s
2.50	$U_{dc,src}$ is ramped-up to ± 210 kV for 1.0 s

As can be seen in Figure 4.31, by using the DLT method, the converter can be operated

Chapter 4. The design of the primary control interface (IFC)

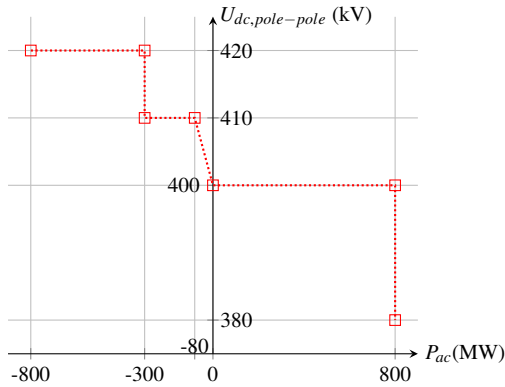


Fig. 4.30: The droop line characteristics for the advanced converter control operation.

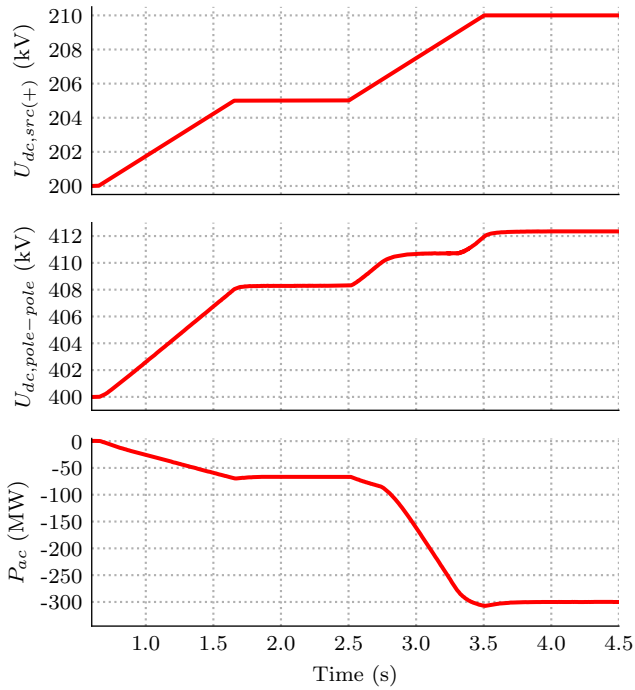


Fig. 4.31: The advanced converter control operation results.

in three different modes, i.e. *UdcCtrl*, *PacCtrl*, and *DroopCtrl*. Started from 0.65 until 1.65 s, the converter is in the *DroopCtrl* mode with $k_{droop} = 0.125$ kV/MW. Therefore, at the end of the first $U_{dc,src}$ voltage ramp, the measured active power and DC voltage equal to -66 MW and 408.25 kV.

When the second $U_{dc,src}$ voltage ramp is initiated, the converter is still operated in the *DroopCtrl* mode. However, when its U_{dc} value reaches ± 205 kV, the converter is operated in the *UdcCtrl* mode, i.e. can be seen in Figure 4.31 from 2.8 s until 3.3 s. At 3.3 s, P_{ac} reaches -300 MW, so the converter starts to be operated in *PacCtrl* mode. The converter stays in this mode until the second $U_{dc,src}$ voltage ramp is over.

The trajectory of the measured active power and DC voltage for the aforementioned conditions is depicted in Figure 4.32. The deviation from the droop line reference becomes more prominent when the converter is in *UdcCtrl* mode. This is because the changes in $U_{dc,src}$ are much faster than the changes that could be cope by the *UdcCtrl* mode.

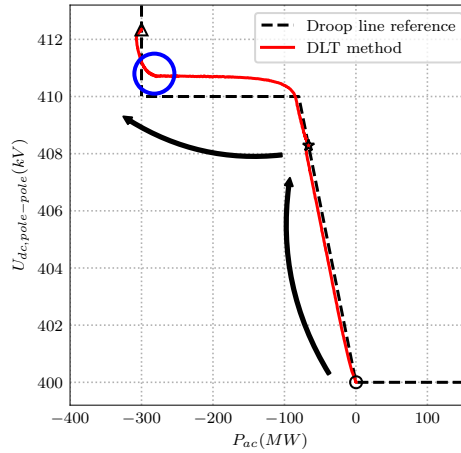


Fig. 4.32: The advanced converter control operation results (red line) plotted in P_{ac} - U_{dc} plane. The dashed black line represents the droop line characteristics, while the arrows point the movement direction. The points marked with \circ , \star , and Δ represent measured values at 0.6 s, 2.5 s, and 4.5 s respectively. The blue circle represents the transition from *UdcCtrl* to *PacCtrl*, due to the closeness of the converter "position" from the droop line.

The transition from the *UdcCtrl* to *PacCtrl* mode is indicated in Figure 4.32 with a blue circle. When the measured active power of the converter changes from -100 to -280 MW, the DLT method drives the converter to follow the constant DC voltage at ± 205 kV. As soon as the converter comes closer to the straight vertical line at -300 MW, then the new DC voltage reference for the converter is calculated from the perpendicular distance from the constant active power operation.

4.2.8. COMPARING VARIOUS DROOP RELATIONSHIPS

As mentioned in Subsection 3.2.2, apart from $P_{ac}-U_{dc}$ relationship there are $I_{dc}-U_{dc}$ and $P_{ac}-U_{dc}^2$ relationships as well. In principle, the DLT method calculates the displacement error regardless of the type of the droop relationship. Therefore, when the droop knee points are translated from one droop relationship to another, the same converter behavior should be expected.

To show the converter behavior with different droop relationships, the same simulation case as in Subsection 4.2.7 has been considered. The droop knee points, depicted in Figure 4.30, have been translated into $I_{dc}-U_{dc}$ and $P_{ac}-U_{dc}^2$ relationships, i.e. given in Table 4.3. The simulation results for $I_{dc}-U_{dc}$ and $P_{ac}-U_{dc}^2$ relationships are shown in Figure 4.33. As comparison, the simulation results for $P_{ac}-U_{dc}$ relationship depicted in Figure 4.32 are also shown in Figure 4.33.

The conversion of the knee points from $P_{ac}-U_{dc}$ to $P_{ac}-U_{dc}^2$ relationship is straightforward, i.e. only the voltage values that are squared and divided by 1000 (from kV to GV²). However, when converting the knee points from $P_{ac}-U_{dc}$ to $I_{dc}-U_{dc}$ relationship, the converter losses and the DC resistance in Figure 4.21 need to be considered when converting from P_{ac} to I_{dc} . The values for the $I_{dc}-U_{dc}$ relationship in Table 4.3 were retrieved from power flow simulations to get the same knee point values in the $P_{ac}-U_{dc}$ plane. Furthermore, the same knee point for the DC current is used for point number 2 and 3 in Table 4.3 instead of the ones from the power flow result, in order to achieve a constant DC current control.

Table 4.3: Translation of droop knee points depicted in Figure 4.30 from $P_{ac}-U_{dc}$ to $I_{dc}-U_{dc}$ and $P_{ac}-U_{dc}^2$ planes.

Knee points	$P_{ac}-U_{dc}$		$I_{dc}-U_{dc}$		$P_{ac}-U_{dc}^2$	
	X_{PWL} (MW)	Y_{PWL} (kV)	X_{PWL} (A)	Y_{PWL} (kV)	X_{PWL} (MW)	Y_{PWL} (GV ²)
1	-800.0	420.0	-1930.0	420.0	-800.0	176.4
2	-300.0	420.0	-735.9	420.0	-300.0	176.4
3	-300.0	410.0	-735.9	410.0	-300.0	168.1
4	-80.0	410.0	-196.1	410.0	-80.0	168.1
5	0.0	400.0	0.0	400.0	0.0	160.0
6	800.0	400.0	1973.0	400.0	800.0	160.0
7	800.0	380.0	2055.0	380.0	800.0	144.4

As can be seen in Figure 4.33, the same behavior for different droop relationships can be achieved by using the DLT method. Therefore, different droop types can be used in the same MTDC system as long as the coordinate pairs are adequately translated from one to another droop relationship, which is consistent with the findings in [79].

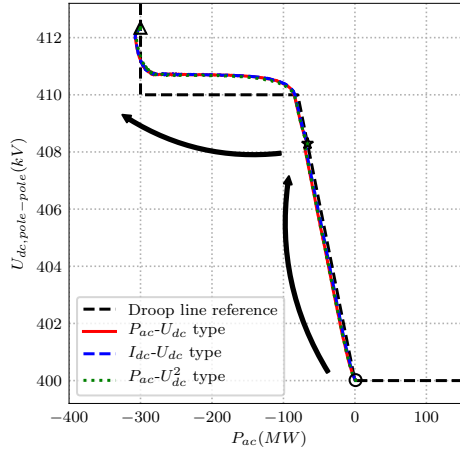


Fig. 4.33: The results of the simulation using different droop relationships plotted in P_{ac} - U_{dc} plane. The dashed black line represents the droop line characteristics, while the arrows point the movement direction. The points marked with \circ , \star , and \triangle represent measured values for the three types at 0.6 s, 2.5 s, and 4.5 s respectively.

4.3. PHASE COMPENSATOR

In the following subsections, the phase compensator part of the IFC is explained, i.e. the rightmost box in Figure 3.16. The input for the phase compensator is the DC voltage reference from the DLT method ($U_{dc,DLT,ref}$) and the output is the new DC voltage reference given to the existing $UdcCtrl$ ($U_{dc,ref}$).

4.3.1. DC SYSTEM DYNAMICS

In order to explain the DC system dynamics, the average value model (AVM) of HB-MMC and Π -equivalent model for DC cable are considered. The DC-side of the converter is represented as a current source and the submodules (SMs) capacitor can be lumped as an equivalent capacitor (C_{eq}), which is the same as the one depicted in Figure C.1. These conditions can be fulfilled by assuming that all the internal MMC variables is perfectly controlled, i.e. a balance voltages on all SMs and circulating currents are suppressed [105].

Furthermore, it is assumed that the AC-side of the converter is connected to a strong AC system, therefore both active and reactive power behavior can be properly decoupled. For $UdcCtrl$ design and tuning, it is enough to use these models, although these models do not offer the best accuracy for system studies as compared to a more

detailed one [48, 68, 105]. The inaccuracy of the AVM occurs because the low-level controls of the converter are not presented and assumed to be ideal, which leads to a slight deviation as compared to a detailed model during AC-side fault [105]. This model also does not properly replicate the DC-side fault condition, it gives a higher DC current peak value during a pole-pole DC fault. However, the converter control is supposed to be operated near the steady-state value of the converter, so these limitations can be disregarded during the design of the outer converter control.

Figure 4.34 shows the DC-side equivalent circuit for a monopole PtP link. Since the typical converter losses are around 1% for nominal power transfer, it can be assumed for simplicity that the converter is lossless, such that the coupling with the AC system can be formulated by (4.12) [48].

$$I_{dc,src_x} = \frac{P_{dc_x}}{U_{dc_x}} \quad (4.12)$$

where x represents the converter station number (1 or 2 in Figure 4.34) and $I_{dc,src}$ is the equivalent current source to represent the DC-side of the converter.

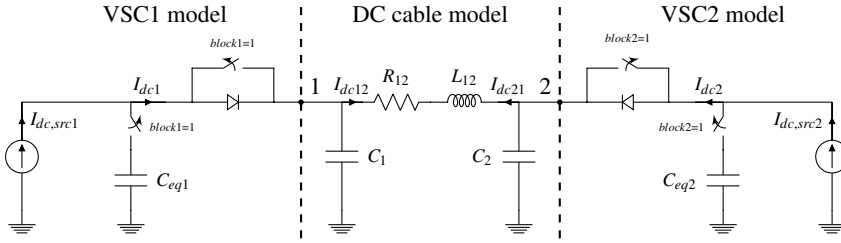


Fig. 4.34: DC equivalent circuit of a monopole PtP HVDC link [106].

The DC voltage dynamic equation at node 1 (U_{dc1}) can be formulated as given in (4.13):

$$\frac{dU_{dc1}}{dt} = \frac{I_{dc,src1} - I_{dc12}}{C_{eq1} + C_1} \quad (4.13)$$

where C_{eq1} is the equivalent capacitance for converter 1 and C_1 equals half of the DC cable capacitance (C_{cable}). The dynamic equation for node 2 can be retrieved in the same way using (4.13) and replacing the values for station 2, i.e. $I_{dc,src2}$, C_{eq2} , and I_{dc21} . The magnitude of I_{dc12} and I_{dc21} are the same with opposing sign and the dynamics can be formulated in (4.14).

$$L_{12} \frac{dI_{dc12}}{dt} = (U_{dc1} - U_{dc2}) - I_{dc12} R_{12} \quad (4.14)$$

Typically, the value of C_{SM} is rated such that the SM energy storage is ranged between 30–40 kJ per MVA rating of the converter to keep the SM voltage ripple within $\pm 10\%$

range [107]. Although the C_{SM} value is quite significant (some millifarads), the C_{eq} value is less than C_{SM} value since the number of submodule (n_a) is usually high, e.g. 38 SMs/arm for a ± 320 kV converter with ABB's HVDC Light technology and 200 SMs/arm for a ± 200 kV converter with Siemens' HVDC Plus technology [108]. As an example, the C_{eq} for an 800 MVA converter with ± 200 kV and 200 SMs/arm, the electrical data is given in Table A.1 is 0.3 mF.

However, as compared to the DC cable capacitance, the converter capacitance is still dominant e.g. 1000 km cable is almost equal to one converter equivalent capacitance, while in the North Sea, NordLink is the longest PtP link having 623 km DC cables [11, 48]. Furthermore, this DC cable capacitance is distributed along the cable length, i.e. not concentrated in one place like in the converter. Therefore, the DC voltage dynamics are mainly influenced by the converter capacitance.

For the system in Figure 4.34, it is assumed that VSC1 is in the *UdcCtrl* mode, while VSC2 is in the *PacCtrl* mode. When a DC voltage reference step is applied, the DC voltage controller of VSC1 modulates the active power exchange formulated in (4.12) in such a way that the DC voltage at node 1 follows the new reference. This means that $I_{dc,src1}$ value in (4.13) is changed to charge/discharge the capacitance until the U_{dc1} equals to the reference.

The changes in U_{dc1} leads to current flow dynamics through the DC cable as formulated in (4.14), which will charge/discharge C_2 and C_{eq2} and leads to DC voltage dynamics formulated in (4.13) for VSC2. However, since VSC2 is in active power control, the active power is kept the same by changing $I_{dc,src2}$ in (4.12) for varying U_{dc2} value.

When the PtP system depicted in Figure 4.34 is expanded into an MTDC system, the DC dynamic equations ((4.13) and (4.14)) are then transformed into a matrix equation to represent the condition of each DC nodes within the MTDC system [109]. The DC dynamics follow the same principle as in the PtP link, but with more terminals to be considered.

4.3.2. CASCADE COMPENSATION

As formulated in (4.13), the larger the DC system capacitance, the longer the time required to achieve the same DC voltage change. Blocking/deblocking some converters in an MTDC system might change the DC system capacitance significantly. Hence, the behavior of the *UdcCtrl* changes depending on the number of active converters within the MTDC system.

To show the changes in the *UdcCtrl* mode response, a 4-terminal HVDC system is considered. All the converters within this MTDC system has the same rating, i.e.

800 MW and ± 200 kV. However, instead of considering all the terminals, a simplified test system is used to perform the step, i.e. depicted in Figure 4.35. The DC capacitors in Figure 4.35 reflect the total converter capacitance of the additional 3 terminals (0.9 mF). Further explanations about this simplified test system is given in Subsection E.1.1. The DC voltage step results of one and 4-terminal (simplified) HVDC system are shown in Figure 4.36.

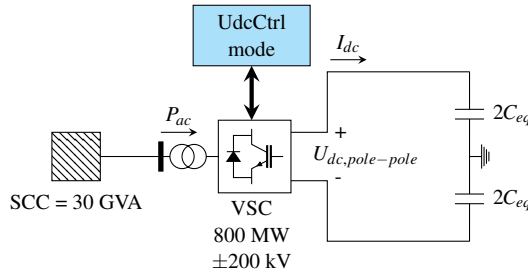


Fig. 4.35: The test system for testing the $U_{dc}Ctrl$ mode. The converter data is given in Section A.1.

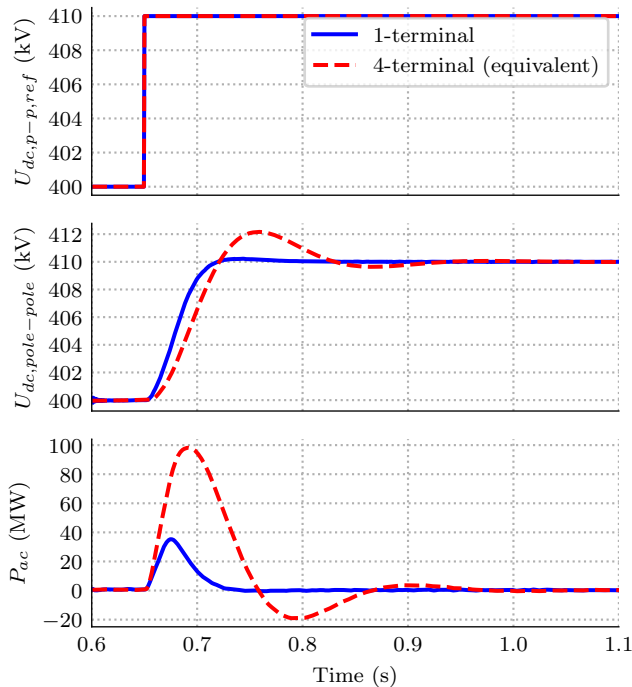


Fig. 4.36: DC voltage step response comparison when only one and 4 converters are active. The top and middle plots represent the referred and measured DC voltage, while the bottom plot shows the measured active power.

As can be seen in Figure 4.36, although the rise time does not change so much (around 40 ms), the settling time (time to reach within 5% band) of the 4-terminal (equivalent) system is 100 ms slower. Furthermore, since the DC system capacitance increases 3 times than before, the active power spike for this system becomes 3 times higher.

In order to meet the same control requirements (e.g.: rise time, settling time, and overshoot magnitude), the controller gains need to be updated whenever the DC system configuration is changed. However, the implementation of a gain-scheduled control (to schedule the gain depending on the DC system configuration) becomes challenging in the case where the MTDC system is built in steps by different vendors. This is because the existing control concept is usually kept secret and protected by IPR, which makes it impossible for another vendor to modify the existing control built by another vendor [48, 50].

Therefore, a compensation unit is needed to externally adjust the performance of the existing *UdcCtrl*. The block diagram of the system with a compensation unit is depicted in Figure 4.37, which is given in frequency domain with Laplace variable s . This cascade compensation has been commonly used in the power system application, e.g. in the exciter system of the synchronous generator [104]. Furthermore, the cascade compensation is chosen apart from feedback compensation due to the simplicity of the cascade compensation and there is a risk of infinite steady-state error when the feedback compensation is given a ramp input [110].

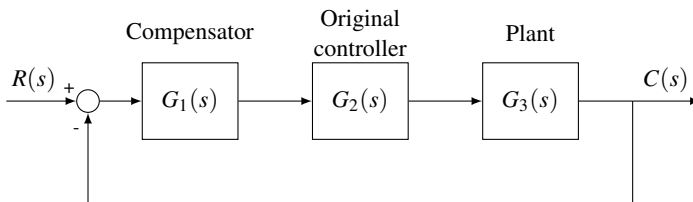


Fig. 4.37: The cascade compensation structure [111]. The input reference is denoted as $R(s)$, while the output of the system is given as $C(s)$. Each block diagram represents the transfer function in frequency domain of the compensator, original controller, and plant.

The *UdcCtrl* structure is represented as $G_2(s)$ in Figure 4.37, while $G_3(s)$ is the Laplace transform of DC system dynamics formulated in (4.13). Ideally, when $G_3(s)$ is changed (by adding more converter into the DC system), the parameters of $G_2(s)$ need to be updated. However, by using the compensator ($G_1(s)$) in Figure 4.37 the closed-loop transfer function of the system can be adjusted while keeping the same $G_2(s)$ parameters.

A lead-lag filter is used as the compensator in Figure 4.37. This unit could be used to adjust both the frequency response and the steady-state error [111, 112]. In general, the lead-lag filter time constants are tuned to get the expected system performance. If

the lead time constant, T_{ld} , is higher than the lag time constant, T_{lg} , the filter provides phase lead at high frequencies which in turn improve the response and stability of the control. On the other hand, if T_{ld} is lower than T_{lg} , the filter gives phase lag at low frequencies, which reduces the steady-state error. Therefore, since this unit gives phase lead or lag, it is referred as a phase compensator unit. However, if both T_{ld} and T_{lg} have the same value, this unit gives a constant gain of 1 (compensation is disabled).

The implementation of the phase compensator within the IFC is depicted in Figure 4.38. The output of this lead-lag filter is then added with the measured DC voltage and then send to the existing $UdcCtrl$. This is because, PI-control is normally used in the $UdcCtrl$ to eliminate the difference between the measured and referred DC voltage [48]. Hence, the structure of the existing $UdcCtrl$ with phase compensator unit becomes the same as the one depicted in Figure 4.37.

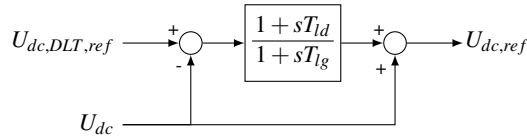


Fig. 4.38: The phase compensator structure.

The phase compensator can be activated with or without the DLT method explained in Section 4.2. An example of having the phase compensator without the DLT is for realizing a gain-scheduled control, i.e. the gains of the phase compensator is adjusted depending on the system conditions such that the DC voltage control performance can be optimized for each condition of the system (AC-, or DC-side, or even both). This gain-scheduled control is explained further in Subsection 4.3.4. When the DLT method is also activated with the phase compensator, the performance of the DLT method can be improved by increasing the time response of the existing $UdcCtrl$ control.

4.3.3. TUNING OF THE PHASE COMPENSATOR

The lead-lag filter time constants can be determined by deriving the dynamic equations of the system. This means that the transfer function of the existing controller ($G_2(s)$ in Figure 4.37) and the converter ($G_3(s)$ in Figure 4.37) need to be known. The time constants for the lead-lag filter are tuned to fit the new control requirements. Different design methods, e.g. via the root locus or frequency response technique, can be employed to determine these time constants [111, 112].

However, since the converter is a complex structure with different control layers, this approach might not be practical. For the same IPR issue, the information of the existing control and signal processing methods are usually not provided by the ven-

dor [48, 50]. Furthermore, different MTDC configurations might require different transfer functions that need to be derived.

On the other hand, project-specific black-box models are usually delivered during the commissioning of an HVDC system. These models are available to the contractor for mainly three purposes, i.e.: operational planning, post-disturbance analysis, and various network planning related studies [50]. Usually, both electromagnetic transient (EMT) and transient stability (RMS) models are provided by the vendor. These models have been validated against the real system installation for different dynamic events.

Therefore, the project-specific black-box model can be used to determine the time constants of the lead-lag filter for different conditions of the DC system by employing an optimization-enabled EMT (OE-EMT) simulation method [113]. With this method, the expected behavior of the control is represented as an objective function (OF) then the EMT simulation is performed to evaluate this OF in such a way that the control parameters are optimized.

Integral square error (ISE) is commonly used to measure the behavior of the control, which can be represented as the integral of the squared difference between the measured (x) and reference (x_{rs}) signals as formulated in (4.15):

$$ISE(x) = \int_{t=T_0}^{T_1} (x(t) - x_{rs}(t))^2 dt \quad (4.15)$$

where T_0 and T_1 represent the time duration for performing the ISE calculation. The reference signal (x_{rs}) represents the expected behavior of the control system specified by some factors e.g.: rise time, peak overshoot magnitude, and settling time of the signal. This reference signal can be generated e.g. by a signal generator representing the expected step response of the control or from a measured signal with the expected behavior. The optimization algorithm is then used to choose the best values for the control parameters such that these factors are compromised.

In the following subsection, the OE-EMT simulation method is used to determine the phase compensator gains for different conditions of the DC system.

4.3.4. THE GAIN-SCHEDULED CONTROL

As mentioned earlier, the amount of the active converter within the MTDC system will influence the performance of the *UdcCtrl* mode. The capacitance of the DC cables can be considered constant by assuming that there is no breaker installed in the interconnection hub, so the DC cable to the hub is not disconnected when the converter is blocked. Therefore, the gains for this control need to be adjusted depending

on the configuration of the MTDC system. Hence, a gain-scheduled *UdcCtrl* method.

By using the phase compensator, the gain-scheduled control can be implemented without altering the existing *UdcCtrl* structure. The performance of the existing *UdcCtrl* can be adjusted externally by using this unit depending on the configuration of the DC system. This means that in order to achieve a certain *UdcCtrl* performance depending on the status of each converter in the MTDC system, the time constants of the phase compensator component are scheduled [106].

A lookup table is employed to schedule these time constants by comparing with the MTDC configuration signal, CFG_{dc} . Each of the converters within the MTDC system sends its status to the DC grid secondary control, and then the DC grid secondary control will send back this CFG_{dc} , i.e. as formulated in (4.16):

$$CFG_{dc} = \sum_{i=1}^n 2^{i-1} \times DBLK_i \quad (4.16)$$

where i is the station number index for an MTDC system with n -number of terminals, while $DBLK$ is a binary signal which represents the blocking status of the converter (0 means VSC_i is blocked or out of service). By using (4.16), CFG_{dc} becomes a unique number, e.g. as given in Table 4.4 for a 4-terminal HVDC system.

Table 4.4: Examples of CFG_{dc} values for the 4-terminal HVDC system.

CFG_{dc}	$DBLK$				Total C_{eq} (mF)
	VSC1	VSC2	VSC3	VSC4	
1	1	0	0	0	0.3
2	0	1	0	0	0.3
3	1	1	0	0	0.6
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
15	1	1	1	1	1.2

The phase compensator is tuned using the OE-EMT simulation method for each CFG_{dc} value given in Table 4.4. The optimization function is formulated in (4.17):

$$OF(T_{Id}, T_{Iq}) = ISE(U_{dc}) \quad (4.17)$$

where the ISE function is formulated in (4.15) with the reference signal is given as the expected step response behavior of the existing *UdcCtrl*.

At first, it is assumed that the reference signal for ISE function is the DC voltage measured for 1-terminal value, i.e. compensating the 4-terminal operation to act like the 1-terminal. A phase lead is needed to increase the time response of the 4-terminal operation ($CFG_{dc} = 15$) such that the step response becomes equal to the 1-terminal

operation ($CFG_{dc} = 1$ or 2, 4, 8). The OE-EMT simulation results using the Nelder-Mead/Simplex algorithm in PSCAD software are given in Table 4.5, while the step response results are depicted in Figure 4.39.

Table 4.5: The phase compensator's gains obtained using OE-EMT simulation for compensating the 4-terminal operation ($CFG_{dc} = 15$).

Run #	T_{ld} (s)	T_{lg} (s)
1 (initial)	0.0900	0.0900
35 (final)	0.0614	0.0273

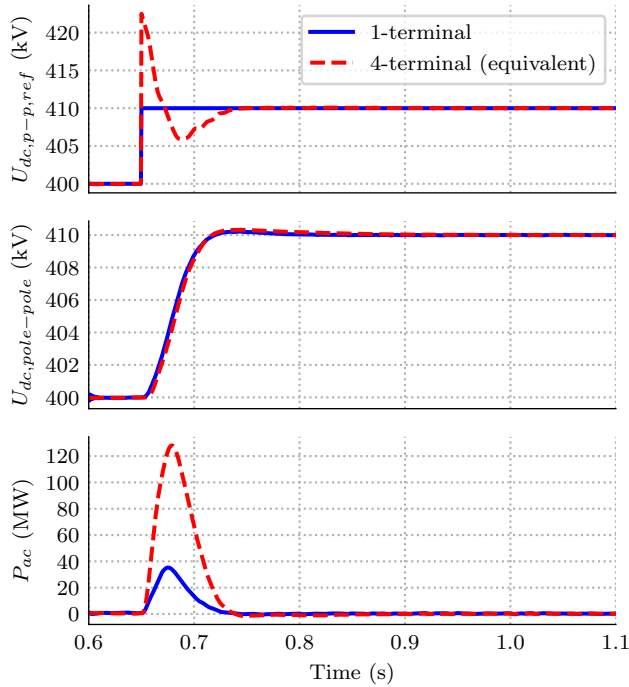


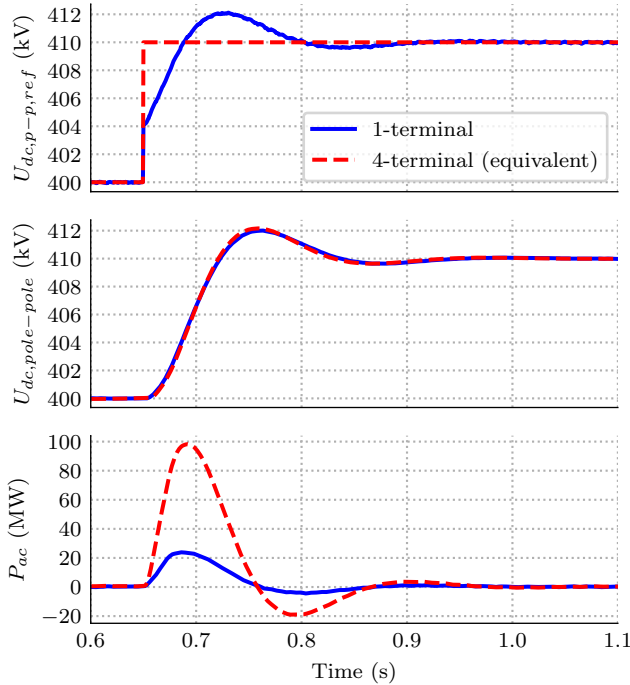
Fig. 4.39: DC voltage step response comparison when the 4-terminal (equivalent) system response is compensated. The top and middle plots represent the referred and measured DC voltage, while the bottom plot shows the measured active power.

On the other hand, if the 4-terminal operation becomes the DC voltage step response reference for the MTDC system, i.e. compensating the CFG_{dc} values lower than 15, the results of the OE-EMT simulation to determine the phase compensator gains for 1-terminal operation is given in Table 4.6. By using these gains, which gives a phase lag to the system, the step response of the 1-terminal operation can be slowed down to match the behavior of the 4-terminal operation as depicted in Figure 4.40.

As can be seen in both Figure 4.39 and Figure 4.40, the phase compensator component

Table 4.6: The phase compensator's gains obtained using OE-EMT simulation for compensating the 1-terminal operation ($CFG_{dc} = 1$).

Run #	T_{Id} (s)	T_{Ig} (s)
1 (initial)	0.0900	0.0900
43 (final)	0.0371	0.0910


Fig. 4.40: DC voltage step response comparison when the 1-terminal (equivalent) system response is compensated. The top and middle plots represent the referred and measured DC voltage, while the bottom plot shows the measured active power.

within the IFC can be used to adjust the behavior the existing $UdcCtrl$ externally. This is achieved by adjusting the reference given to the existing $UdcCtrl$. A faster response time can be achieved by giving a derivative behavior to the DC voltage reference during the step (depicted in Figure 4.39). While, a slower response can be achieved by giving an integrator behavior (depicted in Figure 4.40).

When the step response of the $UdcCtrl$ mode is changed, the peak overshoot of the active power is also changed. The active power response might be more important when the converter is connected to a weaker AC grid. However, since the focus of this thesis is in the DC-side performance when a PtP link is expanded into an MTDC

system, this case is not covered in this thesis. It is suggested that the CFG_{dc} values in Table 4.4 should be expanded to also include the AC grid strength, e.g. by detection some AC lines or generator outage. Furthermore, the AC dynamic behavior might be put as another term for the OF in (4.17) and different weighting factors to decide how much influence of the corresponding term to the objective function might be used [113].

4.4. DROOP SHIFT

The droop shift component is located in Figure 3.16 as the first component before the new DC voltage reference for the existing $UdcCtrl$ is calculated and compensated. This component is used to facilitate the auxiliary control functions, e.g. the frequency, power oscillation damping (POD), and emergency power controls, which are usually found in the PtP link installation [39]. Depending on the input of either of these functions, the droop curve reference received from the DC grid secondary control is adjusted [40].

The main idea of this component is to provide a fast adjustment of the converter following an AC-side disturbance before the DC grid secondary control provides a new droop curve reference. This is possible since the typical operating time range of these auxiliary controls is between 0.2–2 s [39, 40]. This means that as compared to the DC grid control layers, the auxiliary control functions lie between the DC grid primary and secondary controls, i.e. depicted in Figure 4.41.

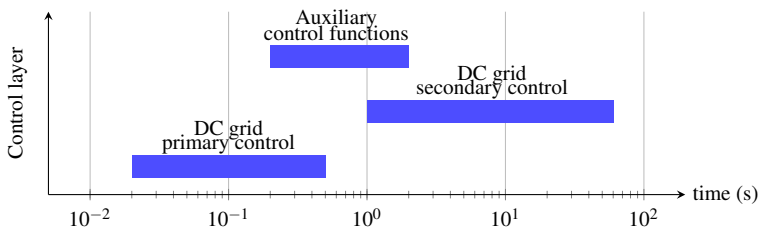


Fig. 4.41: Typical operating time range of the DC grid controls with auxiliary control functions [40].

As an example of the auxiliary function for a PtP link, in the Mackinac VSC project (a back-to-back link in Michigan, US), an automatic runback function has been installed and used to avoid instability following a disturbance (e.g. tripping of an AC line) [114]. This automatic runback function relies on the AC line emulation function, which monitors the voltage angle across the converters and calculates the power reference based on the angle difference, i.e. similar to active power flow calculation between two AC nodes. Similar functionality has also been installed in the INELFE project between Spain and French [115].

Another example of the auxiliary function is the frequency control, which gives a new active power reference when the AC frequency condition is beyond the threshold [116,117]. This function is similar to the emergency power control, i.e. the converter's active power reference is changed abruptly from its steady-state value whenever the converter detects an emergency condition in the grid, e.g. disconnection of an AC line near to the converter [118].

The POD control is another HVDC auxiliary control function that the converter can provide. The possibility of a line-commutated converter (LCC) HVDC link to provide a damping for an inter-area oscillation has been described in [104], which can also be used in a VSC-HVDC installation. Typically, for the POD control, a modulated signal is generated to counter the oscillation that happens in the AC grids [40].

Therefore, since these auxiliary control functions provide a power increase/decrease in order to support the AC network, this can be perceived as the movement of the droop line along the x -axis. Figure 4.42 illustrates how the droop line is shifted to the left/right by providing the dx value in Figure 3.16, i.e. similar to giving a droop step as performed in Subsection 4.2.4. The output of the droop shift component is a new set of knee points coordinate, (X'_{PWL}, Y'_{PWL}) . It should be noted that if the I_{dc} - U_{dc} relationship is enforced, the power order from the auxiliary control functions needs to be adjusted, i.e. as discussed in Subsection 4.2.8.

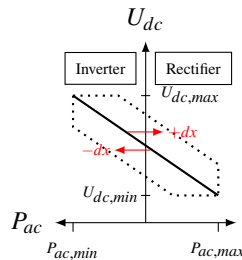


Fig. 4.42: The droop line (solid) is shifted by dx (red arrows indicate the movement) [40]. The dotted lines represent the boundaries of the changes.

4.4.1. THE PERFORMANCE OF IFC WITH THE AUXILIARY CONTROL FUNCTIONS

Because of the slow time range of these auxiliary control functions, the transient stability analysis tool has been considered to simulate the performance of the IFC with the auxiliary control functions. The development of HVDC model for transient stability (RMS) simulation is covered in Appendix C. The IFC has also been implemented as an external function that can be called from both PSCAD (running the EMT simulation) and DIgSILENT PowerFactory (running the RMS simulation) described in

Appendix D.

Since the focus of this subsection is on the integration of the auxiliary control functions into the DC grid control system, the design of the auxiliary control functions is not covered, i.e. covered e.g. in [104, 114–116, 116–118] among others. Furthermore, the aim of this subsection is to demonstrate that the IFC method can be operated together with the auxiliary control functions. Therefore, a signal generator is used as the input for the IFC to emulate the auxiliary control functions output. Hence, a simplified test system depicted in Figure 4.21 is considered such that the need to have feedback from the AC networks and to create an AC-side disturbance to initiate the functions can be avoided. A test which involves the model of a more realistic auxiliary control connected to 2-area AC systems is performed in Chapter 5.

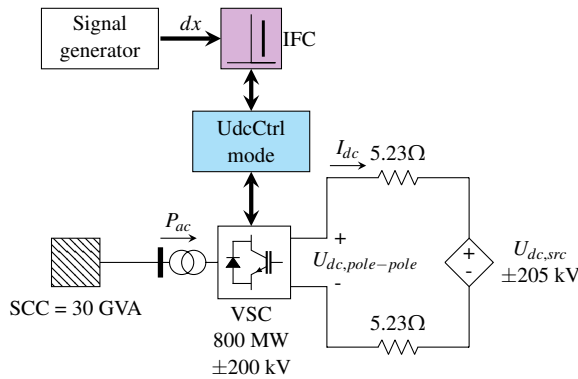


Fig. 4.43: The test system for testing the integration of the auxiliary control functions. A signal generator is used to represent the behavior of these auxiliary control functions. The converter data is given in Section A.1.

The test system depicted in Figure 4.43 has been implemented in PowerFactory software. The $U_{dc,src}$ value is set to ± 205 kV such that the converter is operated in inverter mode with a steady-state power of -400 MW at ± 200 kV. Two droop line references for the IFC which represent *PacCtrl* and *DroopCtrl* modes have been considered and depicted in Figure 4.44.

Since both frequency and emergency power control are used to modify the power reference of the converter to a particular value, these controls can be emulated by giving a delayed-step input to the droop shift component. On the other hand, the POD gives a modulated power reference to the converter, i.e. emulated as an oscillatory input. The following subsections show the PowerFactory simulations results for these two input types with 0.001 s simulation step time.

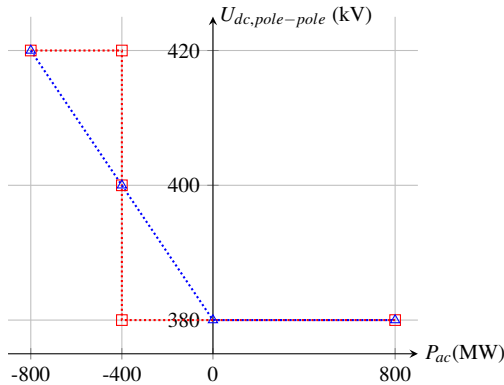


Fig. 4.44: The IFC droop line reference for droop shift test. The red line represents the *PacCtrl* operation of the converter, while the blue one represents the *DroopCtrl* operation with $k_{droop} = 0.05 \text{ kV/MW}$.

DELAYED-STEP INPUT

A step input of 20 MW is given to a second-order transfer function, $\frac{\omega_0^2}{s^2 + 2\zeta\omega_0s + \omega_0^2}$, with a damping (ζ) of 0.74 and a characteristic frequency (ω_0) of $2\pi \text{ rad/s}$. This gives an output signal that has 3% overshoot and a rise time of 2.2 s, i.e. depicted in the first plot of Figure 4.45. This signal becomes the dx input of the IFC. Therefore, the droop line reference used inside the IFC (the values of X'_{PWL} and Y'_{PWL}) is the droop line reference depicted in Figure 4.44, but shifted to the right depending on the value of dx . As soon as the PWL coordinates are shifted along the x -axis, the converter follows this new reference. The simulation results are depicted in Figure 4.45 in the time plane and Figure 4.46 in the $P_{ac}-U_{dc}$ plane.

When the converter is in *PacCtrl*, the new steady-state value is the same as the dx value. However, when the *DroopCtrl* is activated, the new steady-state value becomes lower as compared to the dx value. This is because, when the converter is in the *DroopCtrl* mode, its active power cannot be fixed, i.e. depends on the deviation of the DC voltage. Therefore, the converter control mode should be considered during the design of the frequency control to get the proper response of the system.

OSCILLATORY INPUT

To emulate the output of a POD control, an impulse signal with the magnitude of 400 MW and a width of 100 ms is used as the input for the second-order transfer function. By having a second-order transfer function with a ζ of 0.06 and a ω_0 of 3.7699 rad/s (or 0.6 Hz), the output of the transfer function becomes oscillatory. Fur-

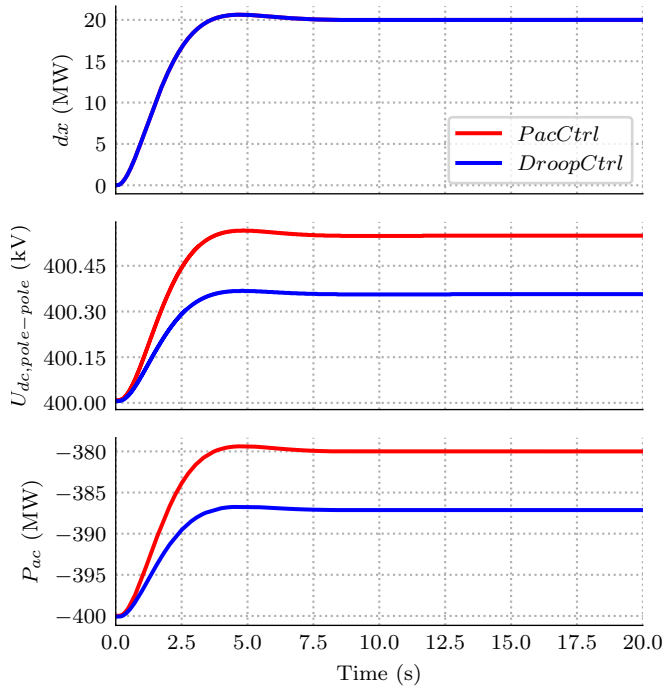


Fig. 4.45: The simulation results when dx is given a delayed-step input signal. Two converter control modes have been considered: *PacCtrl* (red) and *DroopCtrl* (blue).

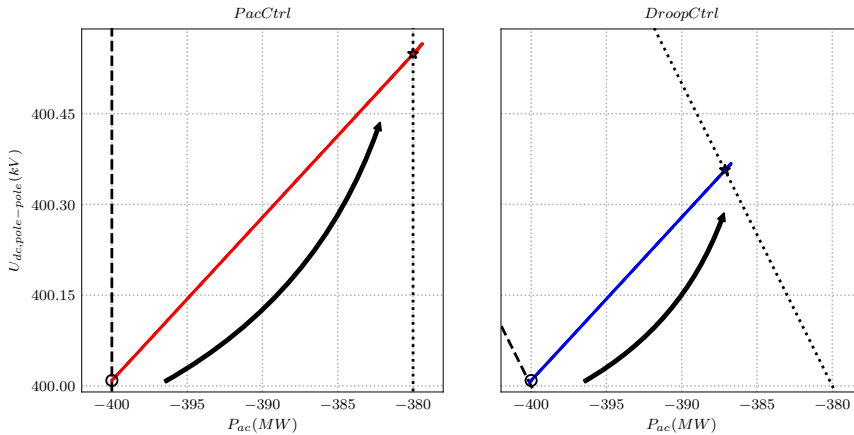


Fig. 4.46: The results in Figure 4.45 plotted in $P_{ac}-U_{dc}$ plane. The dotted black line represents the new steady-state droop line characteristics. The points marked with \circ and \star represent measured values at 0.0 s and 20.0 s respectively. The movement direction is indicated by the arrow.

therefore, a ± 25 MW limiter is used to limit the output from the POD control [104].

The output signal of the second-order transfer function and the limiter mimics the POD output, which is depicted later in Figure 4.47. This signal is then connected to dx input of the IFC. This means that the droop line references depicted in Figure 4.44 are shifted to the left and right following the oscillation of the simulated POD output. The simulation results in P_{ac} - U_{dc} plane are depicted in Figure 4.48.

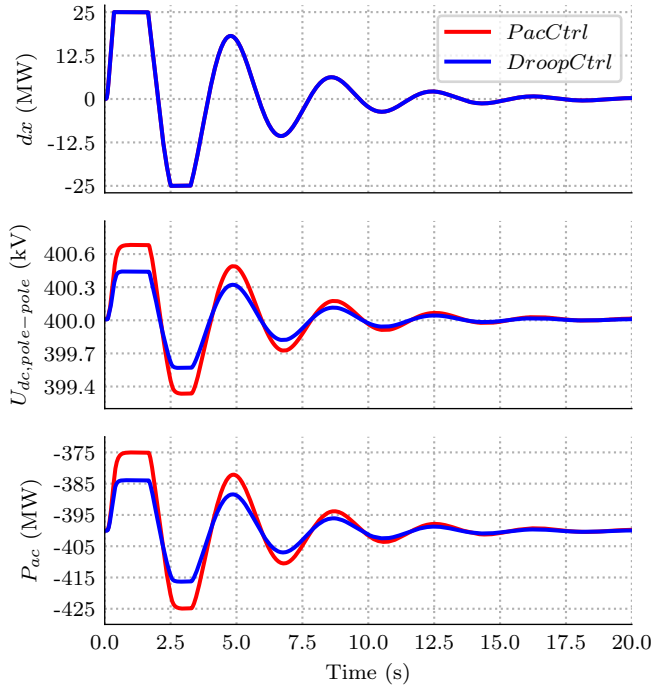


Fig. 4.47: The simulation results when dx is given a delayed-step input signal. Two converter control modes have been considered: *PacCtrl* (red) and *DroopCtrl* (blue).

Regarding the *DroopCtrl* mode, the same phenomena also happen, i.e. the changes in the active power are not the same as the one given by dx . So, the converter mode needs to be considered during the design of the POD control.

4.5. APPLICABILITY OF THE IFC

By using the DLT method, the converter can be operated in different modes without the need to change the existing converter control system. The only requirements to implement the IFC are that the existing converter control system needs to be operated autonomously in *UdcCtrl* and the DC voltage reference should be adjustable. The

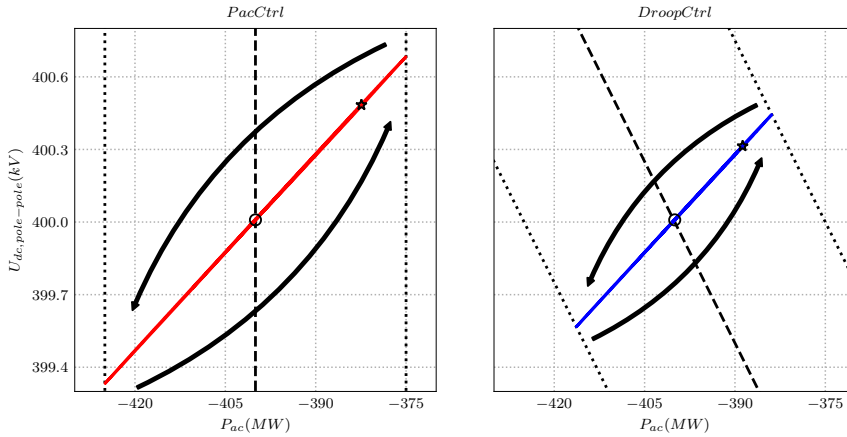


Fig. 4.48: The results in Figure 4.47 plotted in $P_{ac}-U_{dc}$ plane. The dotted black lines represent the limits of the droop line reference oscillations, while the arrows point the movement direction. The points marked with \circ and \star represent measured values at 0.0 s and 5.0 s respectively.

aforementioned IFC functionalities can be activated in different ways, i.e. as given in Table 4.7.

Table 4.7: The possible activation combinations of each IFC component.

No	Droop line tracking	Phase compensator	Droop shift
1	On	Off	Off
2	Off	On	Off
3	On	Off	On
4	On	On	Off
5	On	On	On

In the case of an OWF link, where the onshore converter is usually operated in $UdcCtrl$, the DLT method can be used to mimic the operation of $PacCtrl$ mode. However, since it uses the existing $UdcCtrl$ structure, the behavior of $PacCtrl$ mode using the DLT depends on the behavior of the existing $UdcCtrl$ mode.

In the standalone application of the phase compensator, the phase compensator is used to adjust the behavior of the existing $UdcCtrl$, e.g. depending on the MTDC system configuration explained in Subsection 4.3.4. When it is used with the DLT method, this component might be used to change the behavior of the DLT method when it is used to mimic the $PacCtrl$ mode.

The operational range of the phase compensator depends on the time range of the other control layers. As it shown in Figure 4.39, the phase compensator is used such

that a faster response of the existing *UdcCtrl* can be achieved for a 4-terminal (equivalent) MTDC system. In this configuration, speeding up the response of the existing *UdcCtrl* even more might not be possible and might even lead to instability, because the bandwidth of the compensated *UdcCtrl* overlaps with the inner/current control. Furthermore, this step response improvement is achieved by providing an impulse to the DC voltage reference, which in turn pushing the value beyond the converter limits (shown in Figure 4.39). Therefore, if the DC voltage reference input for the existing *UdcCtrl* is limited to be less than $\pm 5\%$ from the nominal DC voltage, the phase compensator might fail to increase the response of the existing *UdcCtrl*.

Similar behavior also happens when the droop shift is activated and the phase compensator is tuned to give a slower *UdcCtrl* response (depicted in Figure 4.40). The time range of the compensated *UdcCtrl* might overlap with the HVDC auxiliary control functions. Therefore, the time range of the control layers, e.g. depicted in Figure 4.41, should be known before the phase compensator can be applied.

As explained in Section 4.4, the droop shift works by changing the droop line reference given to the DLT method. Therefore, the droop shift can only be activated with the DLT method. The HVDC auxiliary control functions can then be applied using the droop shift when the converter is either in *PacCtrl* or *DroopCtrl* mode. However, when the converter is in *DroopCtrl* mode, a compensation factor might be needed in the auxiliary control functions to get a comparable behavior as when the converter is in *PacCtrl*.

4.6. SUMMARY

In this chapter, the design of the primary control interface (IFC) has been discussed. The IFC contains three main components: the droop line tracking (DLT), phase compensator, and droop shift components.

The DLT method is a new approach to implement DC voltage droop control mode, which uses the displacement distance between the converter measured condition to the designated droop line reference for calculating the new DC voltage reference for the converter. As it was shown in some example cases, the DLT method makes the implementation of a generic converter control possible, i.e. the converter can be operated in three different modes (e.g.: *PacCtrl*, *UdcCtrl*, and *DroopCtrl*) using the same control structure. This means in the OWF link, the onshore converter, which might not have a *PacCtrl* structure implemented, can be operated in this mode using the DLT method.

By using the DLT method, the converter can be serve larger droop constant range as compared to the conventional droop methods, which become unstable when operated

with a high value of droop constant. Furthermore, a shift between the three converter control modes can be achieved seamlessly using the DLT method. However, since the DLT method relies on the existing *UdcCtrl*, there is some deficiency when this method is used to mimic the *PacCtrl* mode.

In addition to these advantages, the DLT method simplifies the implementation of an advanced converter control or a multi-slope droop control method. A simulation results have also been shown that different droop relationships, i.e.: $P_{ac}-U_{dc}$ to $I_{dc}-U_{dc}$ and $P_{ac}-U_{dc}^2$, can be achieved using the DLT method.

The phase compensator is used to externally modify the behavior of the existing *UdcCtrl*. A lead-lag filter becomes the main component to compensate the time response of the existing *UdcCtrl*. An example of the application of phase compensator is for realizing a gain-scheduled control, which adjusts the response of the *UdcCtrl* to match a specific requirement for different system configurations. An OE-EMT simulation is used to determine the gains of the phase compensator for each MTDC system configuration.

The HVDC auxiliary control functions usually exist in the PtP link, which gives a new power reference to the converter. This can be perceived by shifting the droop line reference along the x -axis. So, by using the droop shift component, these auxiliary functions can be retained when this PtP link is expanded into MTDC system. Simulation cases, which mimic the behavior of the frequency, emergency power, and POD controls have been shown to demonstrate how the IFC can be used together with the auxiliary control functions.

All in all, the main advantage of using the IFC is that the existing converter control is unaltered to achieve the aforementioned benefits. So, during the design phase of the interconnection, the vendor-specific black-box models can be used directly with the IFC to perform the dynamic studies.

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CHAPTER 5. SIMULATION RESULTS

5.1. INTRODUCTION

In this chapter, the methods proposed earlier are applied for two test systems. The first test system is a 4-terminal HVDC system, while the second one is a more complex 9-terminal HVDC system.

The 4-terminal HVDC system is used to represent the interconnection of two existing PtP HVDC links (VSC1–VSC2 and VSC3–VSC4) shown earlier in Figure 2.6. Furthermore, the configuration of the system is the same as the one used as an example in Section 3.3, i.e. VSC1–VSC2 is an OWF link while VSC3–VSC4 is a shore-to-shore link. Each converter in these links is a symmetric-monopole converter rated at 800 MW and ± 200 kV. At first, the evaluation of the interconnection plan between these links is performed by using the method explained in Chapter 2.

The IFC is then implemented in each of the non-islanded converters within the 4-terminal HVDC system and used for coordinating these converters. Several dynamic cases have been considered, i.e.: the startup process of the MTDC system, changing the droop line reference, applying a three-phase AC fault, OWF power ramp up, and a loss of a converter station. For the first two cases, the IFC received the input as a single-slope droop line characteristic. For the rest of the cases the multi-slope and pilot voltage droop control method are used. Furthermore, comparisons with the conventional converter control method are also performed for some of the simulation cases.

Whereas, the 9-terminal HVDC test system comes from the CIGRÉ’s DCS3 DC grid test system [48, 119]. This MTDC system has a mix of the symmetric monopole (± 200 kV) and the bipole (± 400 kV) converters with various power ratings. An ideal DC/DC converter is used to transform the voltage from one level to another. Furthermore, as compared to the 4-terminal HVDC system, this test system has a mesh within the DC system.

In this test system, the IFC is also implemented in all non-islanded converters and used to represent the *UdcCtrl*, *DroopCtrl*, and *PacCtrl* modes. An emergency power action is applied in one of the converter, which rapidly ramp down the active power in this converter. Furthermore, the implementation of a gain-scheduled control is also evaluated using this test system. A simultaneous outage of two nearby converters initiate the scheduling of the phase compensator’s time constants. The impact of having a communication delay is shown as well.

These simulations are performed in two software packages, i.e. PSCAD and PowerFactory. The simulations of the MTDC system subjected to a fast dynamic disturbance, e.g.: a three-phase AC fault, the startup process of the MTDC system, and a rapid change in the active power level of one or more converters within the system, is performed in PSCAD with a simulation time step of $50\mu\text{s}$. A detailed equivalent converter model (Type 4) is used in this software, which offers an accurate behavior of the system [48, 120]. Since the focus of the studies is within the MTDC system, an equivalent AC system (in this thesis Thévenin and Norton sources) is used.

Whereas, the root mean square (RMS) simulations in PowerFactory are used to perform a slow dynamic events like a slow ramp up of OWF power and inter-area oscillations. In this thesis, the RMS simulations is performed with a time step of 1 ms. The fundamental frequency model of the converter is implemented in this software, i.e. described in Appendix C. Furthermore, for the POD integration case, a more detailed AC networks representation is used.

Although the simulations are performed in two different software packages with different simulation time steps, exact the same IFC source code is used. This can be achieved because the IFC is implemented in a modular way, i.e. explained in Appendix D.

5.2. THE 4-TERMINAL HVDC SYSTEM

Figure 5.1 depicts the configuration of the 4-terminal HVDC system. The electrical parameters of the converters and DC cables are given in Appendix A. The onshore 380 kV AC systems are represented as Thévenin sources with a short circuit capacity of 30 GVA. Whereas the 150 kV OWF system is implemented as a simplified wind farm model, i.e. represented by a current source explained in Section B.1.

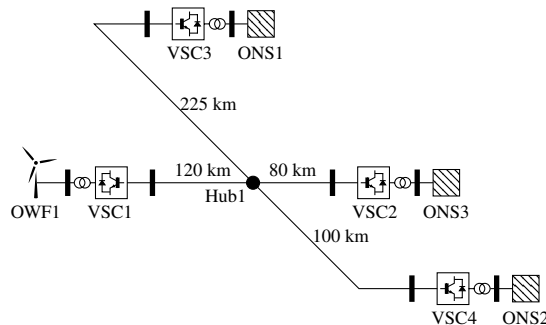


Fig. 5.1: A 4-terminal HVDC test system.

VSC1 is operated in the *IslCtrl* mode, i.e. controls the voltage magnitude and fre-

quency of the offshore AC grid. Furthermore, since all the non-islanded converters (VSC2, VSC3, and VSC4) are connected to a strong AC network, the converter is in reactive power control mode with a reference of 0 MVA, instead of AC voltage control mode. These control modes and their gains are described in Section A.1.

5.2.1. STEADY-STATE RANGE EVALUATION

As the first step of interconnecting the two HVDC links, the steady-state range of the interconnected system should be evaluated. It is assumed that VSC1 and VSC2 links have $\pm 3\%$ DC voltage deviation limits, while VSC3 and VSC4 have $\pm 5\%$ limits. At nominal DC current¹ (2 kA for both links), the DC voltage drop for the 325 km DC cables is 3.58%, whereas for the 200 km cables it is 2.20%.

As explained in Section 2.3, the DC voltage steady-state limits for the interconnected system can be reflected as the limits of the host link, i.e. VSC3–VSC4. The new DC voltage steady-state limits along VSC3–VSC4 are given in Table 5.1 and plotted in Figure 5.2, which are derived from the steps explained in Section 2.3.

Table 5.1: DC voltage limits (in per unit) at the terminal of VSC3, Hub1, and VSC4.

Location	Max. limit (pu)	Min. limit (pu)
VSC3	1.0416	0.9540
Hub1	1.0168	0.9788
VSC4	1.0278	0.9678

The DC voltage limits in VSC1 has more influence to the maximum DC voltage limit at Hub1 compared to VSC2, because VSC1 experiences a higher voltage drop when injecting the nominal DC current to the DC grid. Furthermore, since VSC1 is unidirectional, the influence in the minimum limit is not as much as the bidirectional link (VSC2) (explained in Section 2.4).

When VSC1–VSC2 and VSC3–VSC4 links are interconnected, the steady-state DC voltage limits for both VSC3 and VSC4 are not equal. VSC4 has a narrower band since this station is closer to Hub1. Therefore, the operating points of this link need to be adjusted to avoid overvoltage operation in the other two stations (VSC1 and VSC2).

As an example, an 800 MW active power transmission from VSC3 to VSC4 can still be done by keeping the DC voltage at VSC4 at 1.0 pu, when the OWF power is transmitted directly to VSC2. This condition is referred as the PtP power flow condition of the MTDC system. However, when the power direction is reversed from VSC4 to

¹The nominal DC current is calculated by dividing the rated active power with the nominal DC voltage per pole.

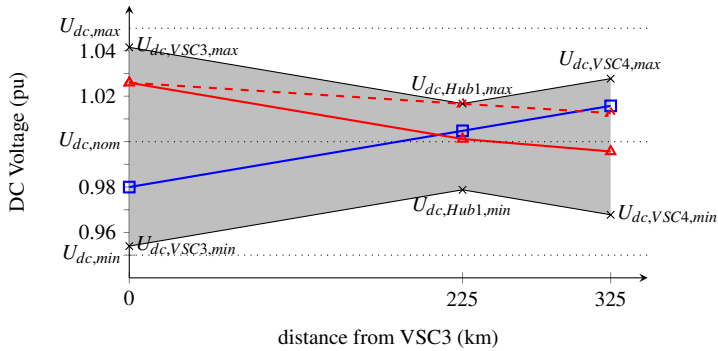


Fig. 5.2: The steady-state DC voltage operational range of a 4-terminal HVDC system depicted in Figure 5.1. The blue line represents the estimated operating points of an 800 MW power flow from VSC4 to VSC3, while the red lines represent the operating points for the power flow given in Table 2.7 (solid) and when VSC2 is out of service (dashed).

VSC3 (illustrated in Figure 5.2 as the blue line), the DC voltage at VSC3 should be set below the nominal DC voltage to keep the voltage at VSC4 below the new limit. This is done to avoid overvoltage operation in VSC1 and VSC2, especially during a full power transmission from VSC1 to VSC2.

Another example is given in Table 5.2, which reflects the power production and demand forecasts for the converters within the 4-terminal HVDC system. It should be noted that the power losses in the converter and DC system are not considered. The operating points for this power flow condition are depicted in Figure 5.2 as the solid red line.

Table 5.2: Power flow forecasts for the 4-terminal HVDC system.

Station	Power forecast (MW)
VSC1	100
VSC2	-500
VSC3	800
VSC4	-400

It is assumed that VSC3 controls the DC voltage (becomes the DC system slack). When VSC2 is blocked (e.g. due to an AC fault), the active power injected from VSC3 to the DC grid is reduced. By setting the DC voltage at 1.025 in VSC3 all the converters within the 4-terminal HVDC system are operated well within limits in case of an VSC2 outage. This condition is depicted in Figure 5.2 as the dashed red line.

All possible power flow conditions should be analyzed to project the operational points

of the links when they are operated as an MTDC system, i.e. by ensuring them to be within the grayed area in Figure 5.2. If the new operational constraints are accepted, then the interconnection of VSC1–VSC2 with VSC3–VSC4 is feasible. Otherwise, changes might need to be done before these links can be interconnected, e.g. changing the converter transformer, number of submodules of the converter, increasing the DC cable rating, etc.

Assuming that the steady-state DC voltage can be fulfilled by the existing PtP links when they are operated as MTDC system, the next step is to coordinate each of the non-islanded converters within the system. As mentioned in Chapter 3, these converters should be able to receive a control order from the coordinated DC grid control and operate autonomously (independent of other converter operation). It is assumed that the existing PtP links depicted in Figure 5.1 fulfill the aforementioned requirements. The IFC is then applied in VSC2, VSC3, and VSC4, i.e. illustrated in Figure 3.15. The design of the IFC follows the description in Chapter 4.

5.2.2. MTDC STARTUP PROCESS

For simulating the startup process of the 4-terminal HVDC system depicted in Figure 5.1, PSCAD software is used. The startup sequence of the MTDC system is given in Table 5.3. A smaller value of pre-insertion resistor (100 Ω) is used in VSC3 to accelerate the charging process of the DC network. Furthermore, during this process, a DC pre-insertion resistor is used to connect VSC1, i.e. used to limit the current flow to the OWF system when VSC1 is deblocked [28].

Table 5.3: The MTDC startup sequence.

Time	Event
0.00	The closing of AC breaker of VSC1
0.10	The closing of AC breaker of VSC3
0.50	The closing of AC breaker of VSC2 & VSC4
1.00	The deblock of VSC3 (<i>UdcCtrl</i> @ ± 200 kV)
1.30	The deblock of VSC2 (<i>PacCtrl</i> @0 MW)
2.00	The deblock of VSC4 (<i>PacCtrl</i> @0 MW)
2.10	The deblock of VSC1 (<i>IslCtrl</i>)

When the DC system is charged (the first second of the simulation), all the converters are still not active. So, there is no difference in the behavior of the converters with or without the IFC implemented. The simulation results during this process are shown in Appendix G.

After the first second, the converters are deblocked one by one, i.e. started with VSC3 at 1.0 s, VSC2 at 1.3 s, VSC4 at 2.0 s, and lastly VSC1 at 2.1 s. In general, the

sequence can be changed, but keep in mind that this process should be started with the *UdcCtrl* station as the DC slack bus and ended with the OWF station to minimize the voltage spikes and active power (or current) surges [121].

The DC voltage reference for VSC3 is set at ± 200 kV, while an active power reference of 0 MW is given in each VSC2 and VSC4. As mentioned earlier, these three converters also control the reactive power at the PCC to stay at 0 MVar. The comparisons when the conventional control method is used in these three converters and when the IFC is activated are depicted in Figure 5.3 for converters VSC3 and VSC4, and Figure 5.4 for converters VSC1 and VSC2.

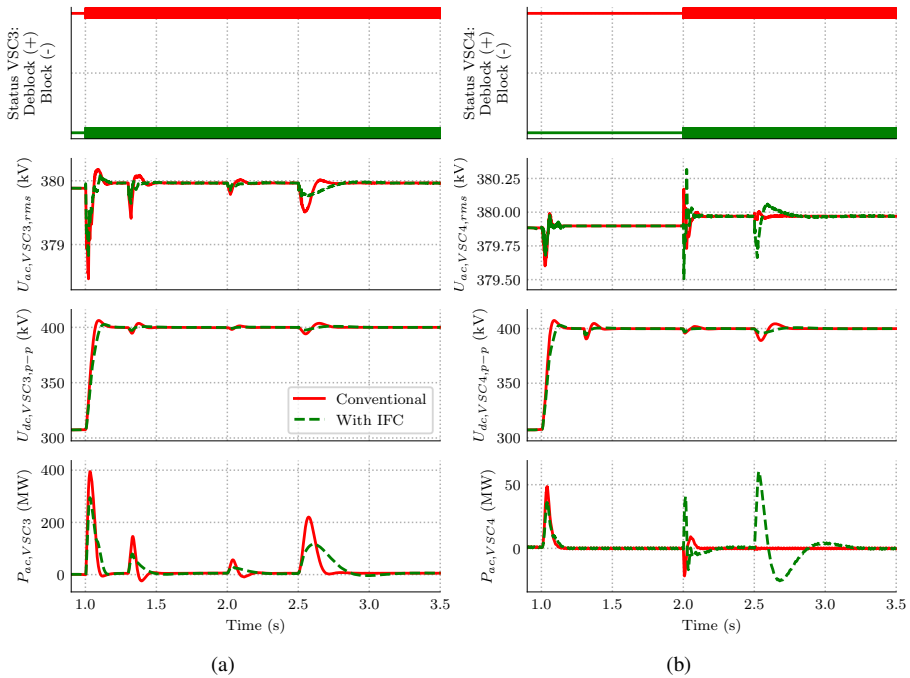


Fig. 5.3: Simulation results of (a) VSC3 and (b) VSC4 when the MTDC system is started. *Conventional* refers to the condition when the conventional controls is activated, while *with IFC* represents the condition when the IFC is activated along with *UdcCtrl* mode in each of the non-islanded converter.

When VSC3 is deblocked at 1.0 s (shown in Figure 5.3(a)), this station starts to control the DC voltage to reach the referred value. It is expected that the behavior of *UdcCtrl* with and without the IFC is the same as described in Subsection 4.2.4. However, it turns out that the behavior during the startup is different. This is because, when VSC3 is deblocked, the DC voltage is below the converter’s minimum DC voltage limit (± 190 kV), i.e. the DC system is charged up to ± 150.81 kV. When the DC voltage is below the limit and the active power is zero, the closest knee point is the bottom-right knee point, which represents the maximum power and minimum DC voltage limit of

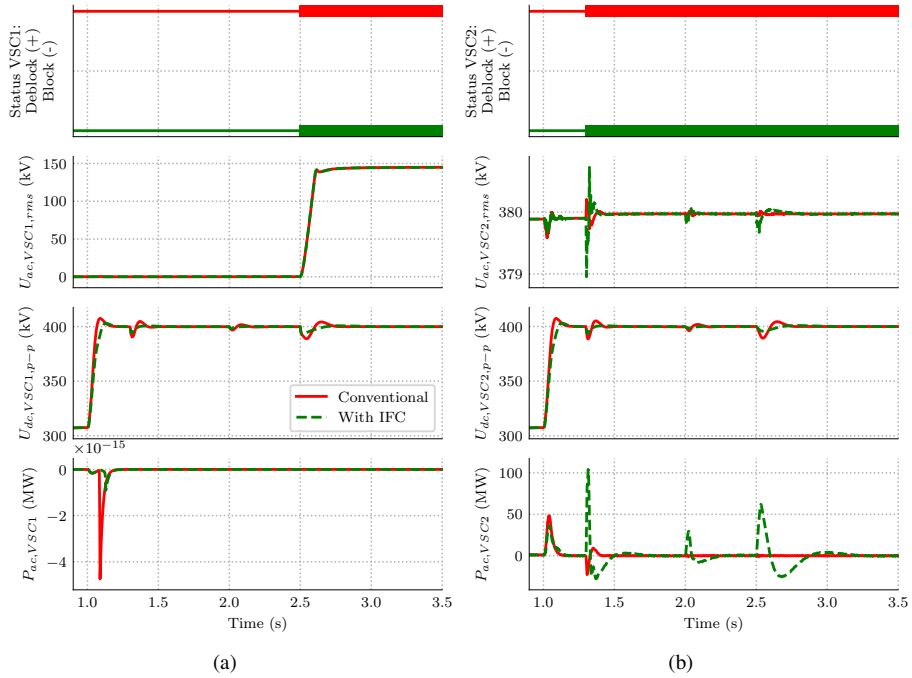


Fig. 5.4: Simulation results of (a) VSC1 and (b) VSC2 when the MTDC system is started.

the converter (described in Subsection 4.2.6). Therefore, the IFC tries to regulate the DC voltage to be first within the limit and then follows the given reference (± 200 kV).

This process makes the DC voltage within the MTDC system build up a bit slower to reach ± 200 kV level as compared to the one with the conventional control. However, the active power spike measured at the PCC of VSC3 becomes lower. This becomes the drawback of the IFC due to the slowness, but at the same time a benefit due to the reduced magnitude of the spike during the deblocking process of the converter.

As can be seen in Figure 5.3(b) and Figure 5.4(b), a positive active power spike occurs when each of VSC4 and VSC2 is deblocked. This is because the state of the control is not properly initiated. With the IFC, the spike is larger since the IFC is using the existing *UdcCtrl* structure. The controller's state activation problem has also been shown previously in Subsection 4.2.5.

Furthermore, as can be noticed from Figure 5.3 and Figure 5.4, the difference between using the IFC to mimic the *PacCtrl* mode and the conventional or "real" *PacCtrl* mode is that by using the IFC the converter becomes more sensitive to the changes in the DC voltage. As shown in Figure 5.4(b), the deblocking of VSC4 at 2.0 s affects the active power transmission through VSC2 when the IFC is used. While if the conventional

PacCtrl is used instead, the active power of VSC2 is kept constant at 0 MW regardless the condition of the DC terminal.

Another example of this drawback, during the deblocking of VSC1 (at 2.5 s), with the conventional *PacCtrl*, the active power measured in the AC terminal of VSC2 and VSC4 is not affected by this process. Meanwhile with the IFC method, the deblocking of VSC1 introduces active power dynamics in VSC2 and VSC4. On the positive side, the DC voltage changes in the system become less severe when the IFC is used, since more converters contribute to balance the power as compared if the conventional *PacCtrl* mode is used.

5.2.3. LIMITING THE RATE OF CHANGES IN THE DROOP LINE

From Figure 5.3 and Figure 5.4, the MTDC system reaches steady-state after 3 s regardless if the IFC is used or not. Once the system reaches steady-state, it is ready for power transmission. It is assumed that a 200 MW power should be transmitted from VSC3 to VSC4 and the MTDC system should also be prepared for accepting offshore wind power. Therefore, VSC3 and VSC4 are assumed to be operated in *DroopCtrl* mode with the droop line given in Figure 5.5, i.e. VSC3 has a droop constant of 0.08 kV/MW while VSC4 has a droop constant of 0.05 kV/MW. These values are chosen such that the OWF power is shared between VSC3 and VSC4 with a ratio of 35:65, which will be tested later in the following subsections.

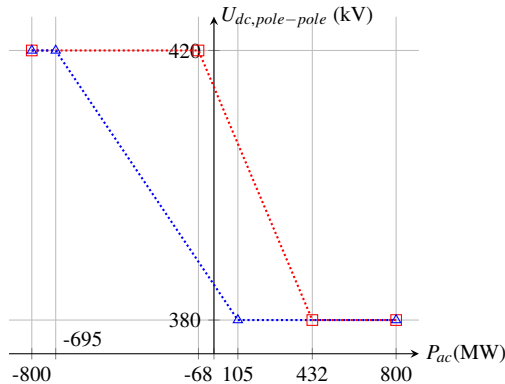


Fig. 5.5: The new droop line reference for realizing a 200 MW power transfer from VSC3 to VSC4. The red line represents the reference for VSC3 ($k_{droop} = 0.08$ kV/MW), while the blue one represents the reference for VSC4 ($k_{droop} = 0.05$ kV/MW).

As explained in Subsection 4.2.5, a seamless shift between converter control modes can be achieved by merely changing the droop line reference given to the IFC. In this

case, the droop line is changed from a straight horizontal and vertical lines, which are used during the startup process, to the ones depicted in Figure 5.5. Furthermore, to be able to make the transition smoother, ramp limiters are used and placed in front of the IFC. By using these ramp limiters the PWL coordinates change, when the setpoints from the DC grid secondary control are changed, becomes gradual.

It is assumed that the changes in the active power, which is usually dictated by the AC grid, are limited to 200 MW/s. This value is chosen to simulate a worst case scenario, whereas a much lower value is expected for starting the transmission, in order not to create a transient in the adjacent AC network. In order to keep the same ratio as the converter's ratings, this active power ramp limit is translated to a DC voltage ramp limit of 5 kV/s. Hence, the ramp limiters are set to 200 MW/s limit for x -axis and 5 kV/s limit for y -axis movement. The simulation results are depicted in Figure 5.6.

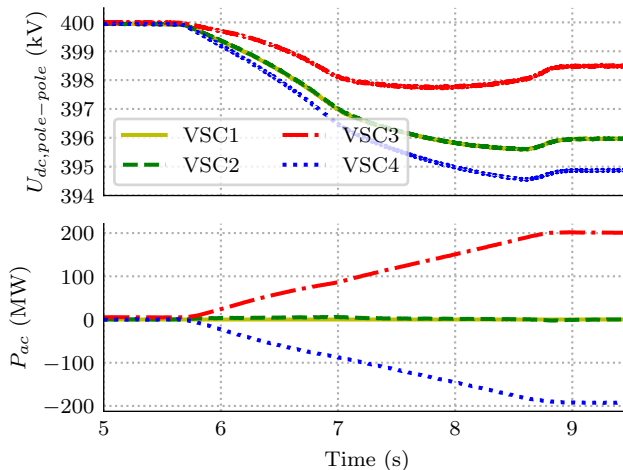


Fig. 5.6: Simulation results when the control mode of VSC3 and VSC4 are changed to *DroopCtrl* mode. The animated plots for these results are shown in Figure I.1.

At 5.1 s the droop line references for each IFC in VSC3 and VSC4 are changed to the one depicted in Figure 5.5. This means that after startup condition shown in Subsection 5.2.2 (no power flow in the DC system), the converters are operated to achieve 200 MW power flow from VSC3 to VSC4. However, since there are ramp limiters which limit the changes in the xy -axis of the droop line reference, these converters do not go directly to the droop line reference given in Figure 5.5.

Until 5.7 s, both converters operate near their original steady-state point, i.e. 0.0 MW and ± 200 kV. This is because the new droop line ends (the output of the rate limiters) move at the same rate, which can be seen as a rotation of the droop curve within the operating limits of the converter with the original steady-state point as the center of rotation. This can be seen in Figure 5.7, in which the new droop reference for each of

these converters still has the same droop origin.

Once either one of the new droop line ends reaches a stable position, both VSC3 and VSC4 start to depart from their steady-state condition. These converters reach a new steady-state condition, i.e. 200 MW active power transfer from VSC3 to VSC4, after around 3 seconds. The trajectories of the changes are depicted in Figure 5.7.

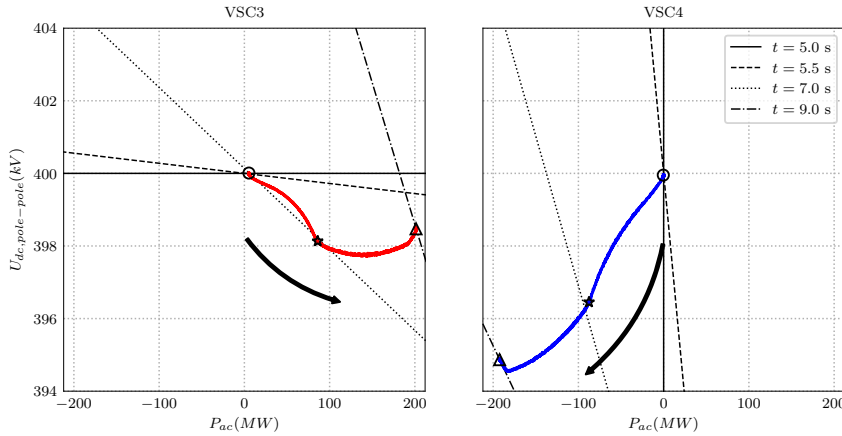


Fig. 5.7: The results in Figure 4.47 for VSC3 and VSC4 are plotted in P_{ac} - U_{dc} plane. The solid, dashed, dotted, and dash-dot black lines represent the droop line references for various times. The points marked with \circ , $*$, and \triangle represent measured values at 5.0 s, 7.0 s, and 9.0 s respectively. The arrows point the movement direction. The animated plots for these results are shown in Figure I.1, which is only available in the digital version of this thesis.

5.2.4. DYNAMIC RESPONSE OF THE MTDC SYSTEM

After reaching a 200 MW transmission from VSC3 to VSC4 shown in Subsection 5.2.3, the following dynamic events are assumed to happen in the MTDC system:

1. At 10.1 s, the OWF power production is ramped up to 200 MW with the power rate change of 100 MW/s.
2. At 11.0 s, VSC2 active power reference is changed from 0 MW to -150 MW with the ramp rate of 200 MW/s.
3. At 12.5 s, a 100 ms bolted three-phase AC fault occurs in the PCC terminal of VSC4.

In Subsection 4.3.4, the phase compensator component inside the IFC is used to modify the behavior of the existing $UdcCtrl$. If it is assumed that the phase compensator

with the gains given in Table 4.5 is considered, the comparison of the system behavior when subjected to the aforementioned dynamic events with (denoted as *fast*) and without (denoted as *slow*) the phase compensator is depicted in Figure 5.8.

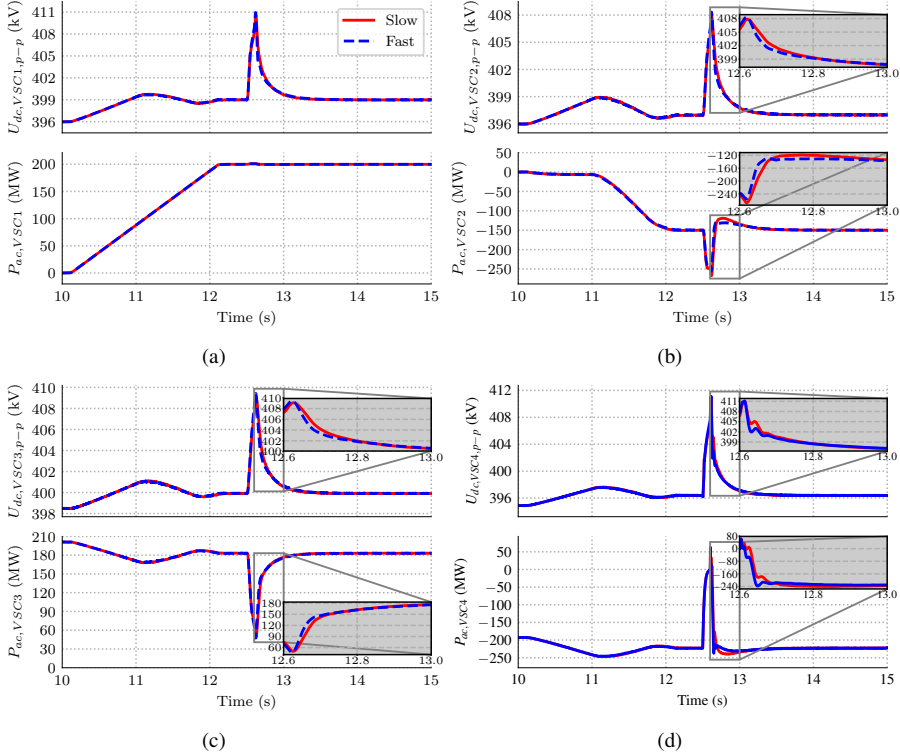


Fig. 5.8: Measured active power at PCC and pole-pole DC voltage during a ramp-up of OWF power production, a ramp-down of VSC3 power reference, and a three-phase AC fault at VSC4, for: (a) VSC1, (b) VSC2, (c) VSC3, and (d) VSC4.

As can be seen in Figure 5.8, the behavior of the system during the power ramping with and without the phase compensator activated within the IFC is quite similar. However, during the three-phase AC fault event, the difference in the system behavior becomes more visible.

When the phase compensator is used, the existing *UdcCtrl* has better settling time as compared to the one without the phase compensator. This can be seen in the inset of Figure 5.8(b)–Figure 5.8(d), where the magnitude of overshoot of the active power is reduced and the responses are faster (approximately 20 ms faster). Hence, the speed of *UdcCtrl* is only affecting the behavior during a fast transient of the system, i.e. in this case an AC fault.

5.2.5. ADVANCED CONVERTER CONTROL

Both droop line references depicted in Figure 5.5 used in Subsection 5.2.3 and Subsection 5.2.4 can be considered as the single-slope droop line, i.e. only one droop slope within the converter's limits. During the steady-state, a 200 MW power is transmitted from VSC3 to VSC4. When the OWF starts to produce power (shown in Figure 5.8), the active power absorbed by VSC3 is reduced, whereas for VSC4 the active power injected to the AC grid is increased.

In this subsection, an advanced converter control represented by the multi-slope droop line reference is used in VSC3. With this multi-slope droop line, VSC3 can be operated in different control modes such that different level of OWF power variations can be treated differently by VSC3 and VSC4 (assuming that VSC2 has 0 MW reference). As an example, the following criteria are considered:

1. For a low OWF power production ($P_{ac,VSC1} < 150$ MW), both VSC3 and VSC4 are operated in the *DroopCtrl* mode with the same droop constant as used before. This means that the power deviation from the OWF is shared between VSC3 and VSC4 with a ratio of 35:65.
2. If the OWF power production continues to increase, VSC3 control mode is switched to the *PacCtrl*, i.e. VSC3 is always operated as rectifier with a minimum power of 150 MW.
3. For a large OWF power deviation (above 250 MW), VSC3's control mode is switched to the *UdcCtrl* such that VSC3 has a priority as compared to VSC4 to handle the power deviation. It assumed that this condition is unlikely to happen.

The new droop line references, which represent the aforementioned criteria, are depicted in Figure 5.9. An upper margin of ± 204 kV is used in the droop reference for VSC3 to represent the third criteria and avoid overvoltage condition in VSC1, when this converter is injecting a full power to the DC grid.

In order to show the behavior of the system when the advanced converter control mode is used, the same OWF power ramp up event as in Subsection 5.2.4 is considered. This simulation case has been implemented in PowerFactory software as a preparation for the transient stability studies performed later in Subsection 5.2.8. Therefore, the behaviors of the 4-terminal HVDC system when subjected to disturbances are known before it is connected to the more detailed AC networks.

Similar to the the OWF system modeled in PSCAD software, the OWF system in PowerFactory is represented as a current source (explained in Appendix B). The active power ramp up is achieved in the same way as in PSCAD software, i.e. by changing

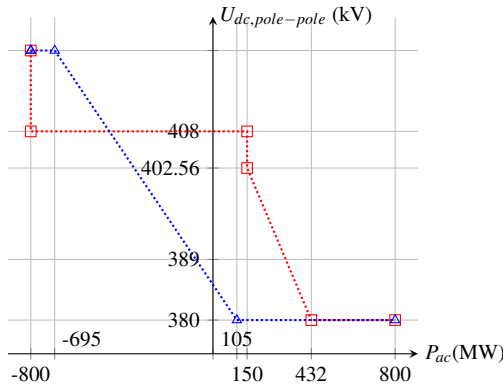


Fig. 5.9: The new droop line reference for realizing a 200 MW power transfer from VSC3 to VSC4 and different OWF power deviation sharing criteria. The red line represents the reference for VSC3 and the blue one represents the reference for VSC4.

the active (d -axis) current. However, the ramp up speed of the OWF power in PowerFactory software is set slower than the one used in Subsection 5.2.4, i.e. 20 MW/s, and started at 0.1 s. The simulation results with the simulation time step of 1 ms are depicted in Figure 5.10.

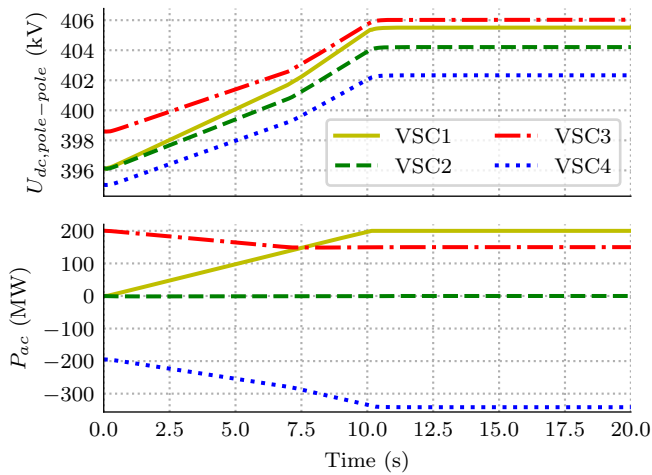


Fig. 5.10: Simulation results when the OWF is ramped up with advanced converter control in VSC2, VSC3, and VSC4. The animated plots for these results are shown in Figure I.2.

In the RMS software, the simulation is started by solving the power flow of the system, i.e. 200 MW transfer from VSC3 to VSC4. Similar to Figure 5.8, when the OWF increases its power production, the power increment is shared as expected, i.e. 35:65 between VSC3 and VSC4.

When the active power absorbed by VSC3 reaches 150 MW, this station switches its control mode from the *DroopCtrl* to the *PacCtrl* mode, i.e. keeping the power level constant at 150 MW. Figure 5.11 shows the trajectory of the DC voltage and active power measured at VSC2, VSC3, and VSC4. From Figure 5.10 and Figure 5.11, it is evident that the system acts as expected during the OWF power ramp up event.

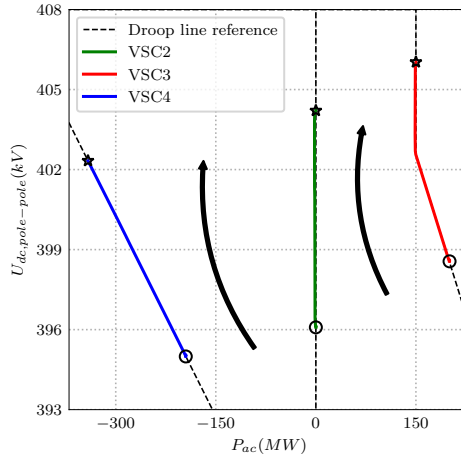


Fig. 5.11: Figure 5.10 results for VSC2, VSC3, and VSC4 plotted in P_{ac} - U_{dc} plane. The dashed black lines represent the droop line references, while the arrows point the movement direction. The points marked with \circ and \star represent measured values at 0.0 s and 20.0 s respectively. The animated plots for these results are shown in Figure I.2.

In this subsection, the OWF power is not assumed to go beyond 200 MW. If the OWF power production reaches more than 250 MW, VSC3 switches from the *PacCtrl* to the *UdcCtrl* mode. This condition is shown in Appendix G. However, as it will be described later in the following subsection, this condition might end up in an overvoltage at VSC1 when VSC4 is out of service (e.g. due to an AC fault).

5.2.6. LOSS OF A CONVERTER STATION

The advanced converter control can also be used to define a new steady-state point after a severe transient event. A sudden loss of a converter station, e.g. initiated by a permanent AC fault at the terminal of the converter, can be considered as an example of this severe transient event. Since the active power cannot be transmitted through this converter, the power flow pattern within the MTDC system is changed and the remaining converters should maintain the operation of the system. With the advanced converter control, a new steady-state condition can be set up before the DC grid secondary control sends the new setpoints for the remaining stations.

In this subsection, a permanent bolted AC fault is applied at the terminal of VSC3 or VSC4 (one at a time). This fault appears at 20.1 s, i.e. after the MTDC system reaches a new steady-state following a 200 MW ramp of OWF power production shown in Subsection 5.2.5. Figure 5.12 depicts the simulation results in time plane, while Figure 5.13 shows the results in the P_{ac} - U_{dc} plane.

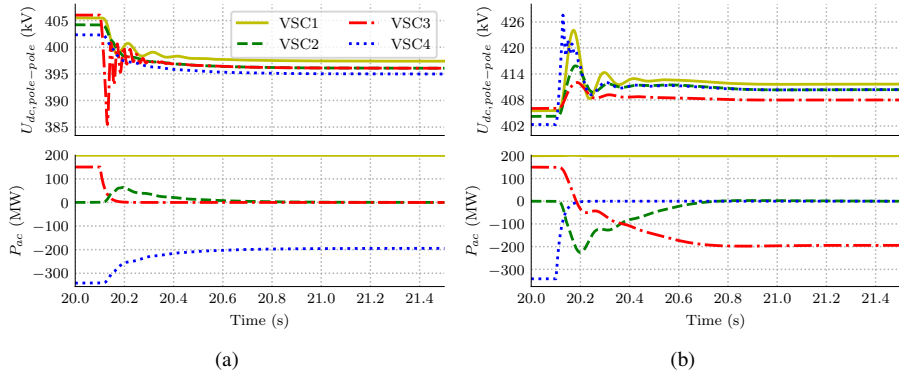


Fig. 5.12: The measured pole-pole DC voltage (top) and active power at PCC (bottom) during a permanent AC fault at the terminal of: (a) VSC3 and (b) VSC4.

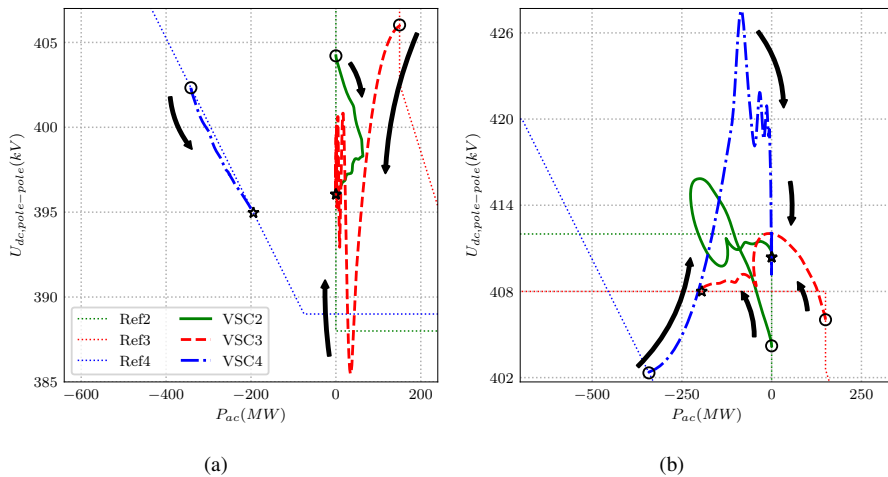


Fig. 5.13: The droop plane plots of VSC2, VSC3, and VSC4 for a permanent AC fault event at the terminal of: (a) VSC3 and (b) VSC4. The dotted lines represent the droop line characteristics, i.e. Ref2 for VSC2, Ref3 for VSC3, and Ref4 for VSC4. The points marked with \circ and \star represent the steady-state operating point of each converter before and after the fault inception, respectively. The arrows point the movement direction. The animated plots for these results are shown in Figure I.5 and Figure I.7.

As can be seen in Figure 5.12, an abrupt change in the power flow leads to a severe DC voltage transient. In Figure 5.12(a), the power flow from the AC-side of VSC3 to the

DC grid (rectifier operation) is suddenly interrupted due to the AC fault. Therefore, the DC voltage at the system starts to decrease due to a power deficit condition within the MTDC system. The most severe DC voltage transient happens at the terminal of VSC3 since this converter is the origin of the disturbance (abrupt change in the active power).

The DC voltage reference generated by the IFC in VSC4 is adjusted such that this converter follows the designated droop line, i.e. the new steady-state power for this converter is reduced by 150 MW. As can be seen in Figure 5.13(a), the trajectory of the VSC4's operating conditions to reach the new steady-state point is quite close to the referred droop line.

The IFC in VSC2 is used to mimic the *PacCtrl* mode. As described in subsection 5.2.2, the condition in the DC-side affects the behavior of this converter. Hence, VSC2 could not maintain a constant power at 0 MW during the transient, i.e. the active power increases up to 64 MW. As same as VSC4, VSC2 reaches a new steady-state condition approximately 0.5 s after the fault inception. The comparison between the conventional *PacCtrl* with the one implemented using the IFC will be shown later.

When the AC fault occurs in the terminal of VSC4, which is operated as the inverter, the DC voltage transient becomes more prominent, i.e. depicted in Figure 5.12(b). During the transient, the DC voltage measured at VSC4 reaches ± 213.75 kV or almost 7% above the nominal DC voltage value, due to a surplus of active power in the DC grid. However, the total duration of the DC voltage above the maximum limit (105% of the nominal) is less than 100 ms.

Furthermore, both VSC2 and VSC3 adjusted their power as the consequence of having an active power surplus in the MTDC system. However, since VSC3 is operated as the rectifier, this converter needs to be switched as the inverter to maintain the power balance in the DC grid (VSC2 keeps a constant active power at 0 MW). This power reversal process leads to a high DC voltage transient, which is higher than the previous case (AC fault at VSC3).

The trajectory of VSC3's operation conditions in the $P_{ac}-U_{dc}$ plane is depicted in Figure 5.13(b). Since during the transient the measured DC voltage goes beyond the upper margin of VSC3, i.e. ± 204 kV depicted in Figure 5.9, this converter changes its mode from the *PacCtrl* into the *UdcCtrl* mode. Since OWF power equals to 200 MW, this upper margin is enough to ensure the remaining converters to be within their operational limits. However, if the power injected from the OWF is more than 200 MW, the upper margin of VSC3 should be reduced, otherwise an overvoltage condition occurs in VSC1.

During the transient, the active power injected to the AC grid from VSC2 reaches 225 MW. As can be seen in Figure 5.13(b), the closest droop line segment from the

VSC2's operating point is changed into the straight horizontal line at ± 206 kV (3% margin) during this condition. Therefore, this converter switches to the *UdcCtrl* from the *PacCtrl* mode. When this converter tries to maintain the DC voltage (along with VSC3), the active power flow magnitude through this converter is increased. As soon as, the active power magnitude goes below 35 MW, the closest droop line from the VSC2's operating point changes to the straight vertical line, which changes the converter operating mode into the *PacCtrl* mode again.

As can be seen in Figure 5.13, the remaining converters are able to find a new steady-state point after the disturbance, which is along their designated droop curve depicted in Figure 5.9. Furthermore, a seamless transfer between different converter control modes can be achieved by using the IFC without introducing another disturbance for the MTDC system.

COMPARISON WITH THE CONVENTIONAL ACTIVE POWER CONTROL

As shown in Subsection 5.2.2, when the IFC is used to mimic the *PacCtrl* behavior, the active power can not be kept constant during the transient in the DC grid (i.e. the deblocking process of other converters). During the startup process described in Subsection 5.2.2, the transient in the DC voltage within the MTDC system is not as abrupt and severe as losing one of the converter station shown in subsection 5.2.6. Therefore, in order to clearly show the behavior of the system when the conventional *PacCtrl* is used, the previous permanent AC fault cases are considered. The simulation results with the conventional *PacCtrl* implemented in VSC2 are depicted in Figure 5.14.

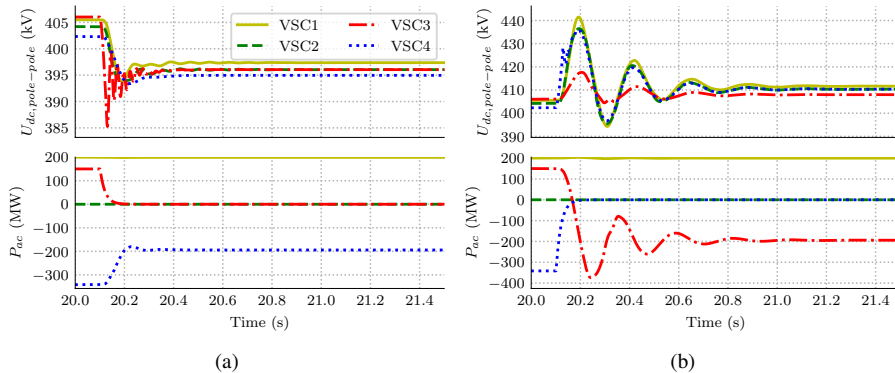


Fig. 5.14: The measured pole-pole DC voltage (top) and active power at PCC (bottom) when the conventional *PacCtrl* is used in VSC2 and during a permanent AC fault at the terminal of: (a) VSC3 and (b) VSC4. The conventional *PacCtrl* mode is implemented in VSC2.

With the conventional *PacCtrl* applied in VSC2, this converter is able to maintain a

constant active power at 0 MW. This means that the AC-side of VSC2 is not influenced with the loss of one converter in the MTDC system. As can be seen in Figure 5.14(a) (AC fault is applied at VSC3), the power loss is only mitigated by VSC4. Therefore, the active power injected by VSC4 to the AC grid is reduced faster than the one depicted in Figure 5.12(a) to balance the power loss.

The similar thing happens when the AC fault is applied at the terminal of VSC4 (Figure 5.14(b)), i.e. the DC voltage spike becomes a lot larger than the one depicted in Figure 5.12(b) as the result of the rapid power change. Furthermore, since the conventional *PacCtrl* is not enforced with the DC voltage dependent power order limiter, which adjusts the active power reference for the converter when the DC voltage goes beyond the limits, the MTDC system experience several overvoltage conditions for approximately 350 ms (three times longer than the one depicted in Figure 5.12(b)).

Therefore, on the positive side, the conventional *PacCtrl* can avoid the disturbance in the MTDC system to spread over to the AC-side of the converter operated in this mode. However, on the other hand, this might aggravate the condition in the DC grid. Furthermore, the risk of overvoltage might become prominent when the DC voltage dependent power order limiter is not implemented in the conventional *PacCtrl* structure.

5.2.7. PILOT VOLTAGE DROOP CONTROL METHOD

In the previous subsections, the DC voltage measurement used by the IFC is located at the converter's terminal. However, as mentioned in Subsection 3.2.2, another alternative of the *DroopCtrl* mode can be employed, i.e. the pilot voltage *DroopCtrl* method. With this method, a common DC voltage measurement value is used by all the non-islanded converters.

In principle, the IFC method can be used as well to implement the pilot voltage *DroopCtrl* method. The measured DC voltage and the Y_{PWL} inputs of the IFC are given as the remote bus condition in order to represent this method. This means that the displacement error calculated in (4.7) is based on the DC voltage condition at the common point within the MTDC system. The sum of the e_{pos} value and the measured DC voltage at the converter terminal (local) is then used as the new DC voltage reference for the existing *UdcCtrl* mode.

In order to show the behavior of the pilot voltage *DroopCtrl* method, the same simulation case as in Subsection 5.2.5 and Subsection 5.2.6 are considered. The DC voltage measured at Hub1 is considered as the common DC voltage value. Hence, the droop line references for VSC3 and VSC4 become the ones illustrated in Figure 5.15. This droop line references are used to realized a 200 MW power transfer from VSC3 to VSC4 and 150 MW limit of the rectification for VSC3.

The same converter active power and DC voltage limits are used in Figure 5.15 due to the same converter ratings. However, the DC voltage upper and lower margins are equal for all the onshore converters, i.e. the steady-state DC voltage limits for the hub depicted in Figure 5.2.

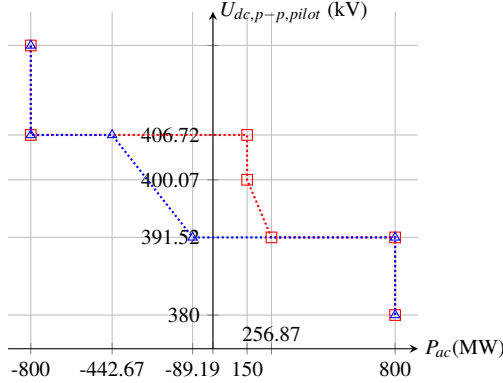


Fig. 5.15: The pilot droop line reference for realizing a 200 MW power transfer from VSC3 to VSC4. The red line represents the reference for VSC3 and the blue one represents the reference for VSC4.

The droop slope segment for VSC3 between 150 and 256.87 MW represent the same slope as the one depicted in Figure 5.9, i.e. 0.08 kV/MW. The slope for VSC4 is then adjusted such that it gives a 35:65 power sharing between VSC3 and VSC4 when there is an increase in the OWF power production.

Ideally, the measured signal of the DC voltage at the interconnection hub is sent to the IFC used in the non-islanded converters. However, since the MTDC system considered in this subsection is a radially-connected system (depicted in Figure 5.1), the pilot DC voltage measurement can be estimated by using the DC voltage and current measured at the converter's terminal, i.e. as formulated in (5.1):

$$U_{dc,VSCi,pilot} = U_{dc,meas} - \Delta U_{dc,VSCi-Hub1} \quad \forall i \in \{2, 3, 4\} \quad (5.1)$$

where the $U_{dc,VSCi,pilot}$ is the DC voltage pilot signal for VSC2, VSC3, and VSC4. The DC voltage drop between the converter and Hub1 ($\Delta U_{dc,VSCi-Hub1}$) is calculated using (2.2) by considering the measured DC current (positive pole) and the DC resistance between the converter and Hub1.

The simulation results of the OWF power ramp up event are depicted in Figure 5.16. As can be seen in Figure 5.16(a), the same active power sharing between VSC3 and VSC4 as the one in Subsection 5.2.5 can be achieved using the pilot *DroopCtrl* method. The only difference between the pilot and local *DroopCtrl* is the y-axis measurement. With the pilot *DroopCtrl* method, the DC voltage reference for each onshore converter is generated by considering the DC voltage measured at Hub1, which is the same for all the onshore converters.

Therefore, as can be seen in Figure 5.16(b), the y-axis movement of VSC2, VSC3, and VSC4 becomes synchronized one to another. Since, the y-axis value used by the IFC is the same for all the onshore converters, the power sharing between them depends solely on the droop slope, i.e. formulated in (3.5). This behavior is expected, since the aim of having the pilot *DroopCtrl* method is to mimic the AC frequency behavior, i.e. common frequency value seen by different parts of the AC system.

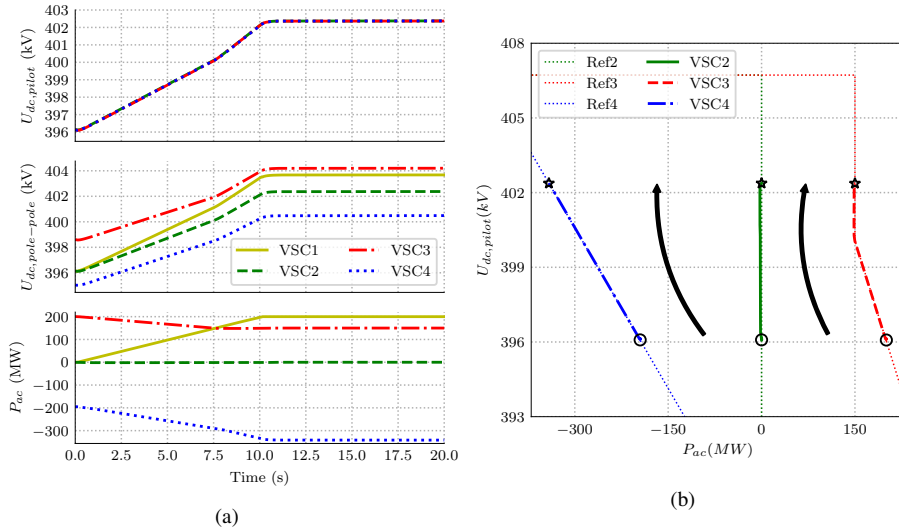


Fig. 5.16: Simulation results of the OWF ramp up event with the pilot *DroopCtrl* method, plotted in (a) time and (b) droop planes. The time plane plot (a) consists of: the estimated Hub1 voltage, the measured DC voltage at the converter’s terminal, and the measured active power at the PCC. The dotted lines in (b) represent the droop line characteristics, i.e. Ref2 for VSC2, Ref3 for VSC3, and Ref4 for VSC4. While, the points marked with \circ and \star represent the measured values of each converter at 0 and 20 s, respectively. The arrows point the movement direction. The animated plots for these results are shown in Figure I.4.

Figure 5.17 depicts the result for the permanent AC fault case, i.e. the same case as in Subsection 5.2.6. As can be seen in Figure 5.17(a), the same behavior can be achieved with the pilot *DroopCtrl* method as using the local measurement. The MTDC system reaches a new steady-state condition also at the same time as the one with the local measurement.

However, when the AC fault occurs at the terminal of VSC4, the MTDC system reaches a new steady-state condition approximately 4 s after the fault initiated. This is because the upper DC voltage margin for the pilot *DroopCtrl* method is lower as compared to the one with local measurement. As can be seen in Figure 5.17(b), right after the fault is applied, VSC3 power reduces to 0 MW, while for VSC2 the power changes to -240 MW (loss of VSC4, i.e. an inverter). The DC voltage for both of the converters go beyond the upper margin of the droop slope, i.e. ± 203.36 kV.

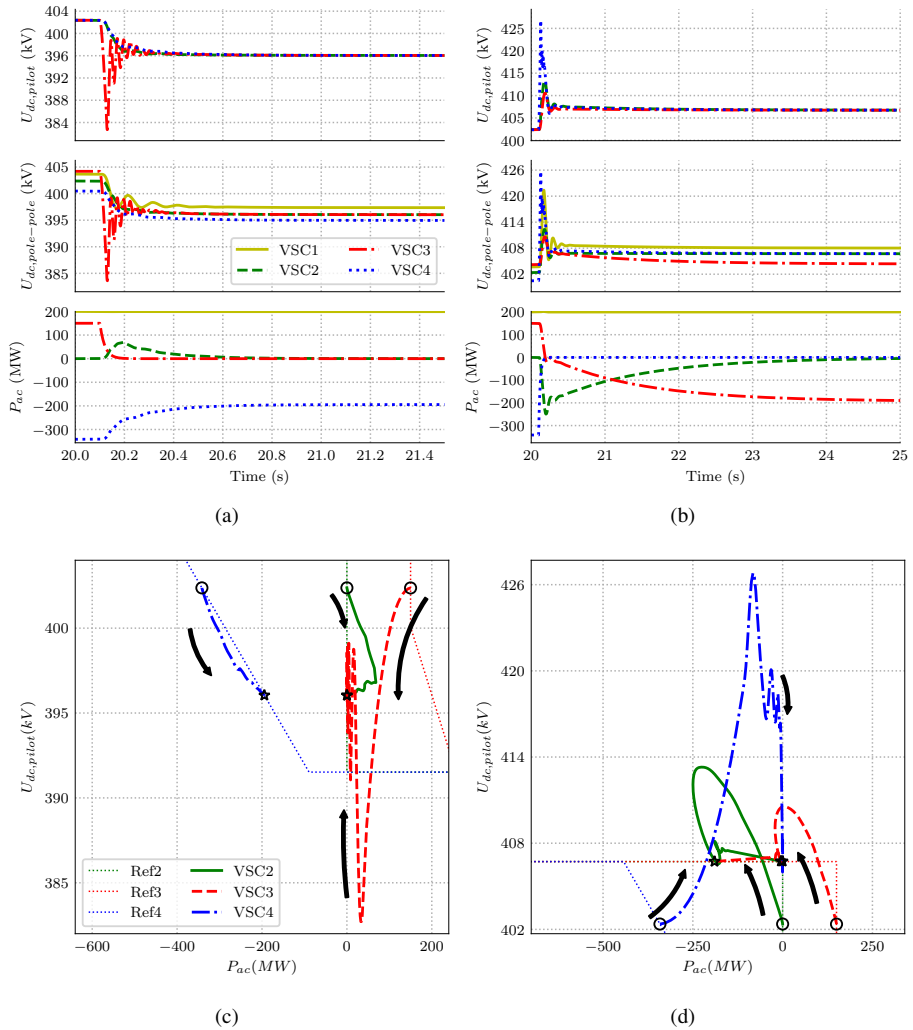


Fig. 5.17: Simulation results of a permanent AC fault with the pilot *DroopCtrl* method. The results for the AC fault located in VSC3 are plotted in (a), (c), while for the one in VSC4 are plotted in (b), (d). The time plane plot (a) and (b) consists of: the estimated Hub1 voltage, the measured DC voltage at the converter's terminal, and the measured active power at the PCC. The dotted lines in (c) and (d) represent the droop line characteristics, i.e. Ref2 for VSC2, Ref3 for VSC3, and Ref4 for VSC4. While, the points marked with \circ and \star represent the steady-state point before and after the fault inception, respectively. The arrows point the movement direction. The animated plots for these results are shown in Figure I.6 and Figure I.8.

The DC voltage transient condition in the P_{ac} - U_{dc} plane, depicted in Figure 5.17(d), can be seen as the trajectories above the upper margin. During this condition, the shortest droop segment is the upper margin itself. Therefore, both VSC2 and VSC3 are operated in the *UdcCtrl* mode. When both converter controls the DC voltage at Hub1,

the power flow through these converters is deduced from the resistance between each of the converters and Hub1. The new equilibrium point (zero e_{pos} value) is reached when the power at VSC2 is zero.

5.2.8. INTEGRATION OF THE POD CONTROL

For showing the capability of the IFC to integrate the auxiliary control functions, the test done in Subsection 4.4.1 is performed again with a realistic POD control. The 4-terminal HVDC system is interconnected with a two-area test system, hence a new test system depicted in Figure 5.18.

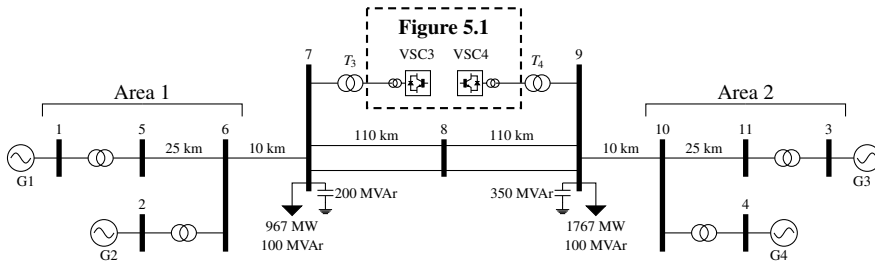


Fig. 5.18: The MTDC system depicted in Figure 5.1 is integrated into a two-area test system [104]. The dashed box indicates the interconnection with the MTDC test system. The parameters for the two-area system is given in Section B.2.

The Thévenin equivalent sources which represent the AC grids of ONS1 and ONS2 in Figure 5.1 has been replaced with the lossless step-up transformers T_3 and T_4 with a voltage ratio of 230/380 kV. These transformers are used to interconnect VSC3 with bus 7 and VSC4 with bus 9 in the two-area system. The details parameters for the two-area test system, e.g.: the parameters of the synchronous generators together with their governor, automatic voltage regulator and power system stabilizer, can be found in Section B.2.

A 400 MW active power is transmitted from Area 1 to Area 2. This power transfer is equally shared between the DC cables (VSC3-VSC4) and the two parallel AC lines. Hence, the MTDC system has the same steady-state condition as in the advanced converter control simulation case (Subsection 5.2.5).

At 1 s a bolted three-phase AC fault is applied at bus 9 and released after 150 ms, which leads to inter-area oscillations [104]. A POD control, depicted in Figure 5.19, has been connected with the IFC of VSC3 to mitigate this problem. The design of this POD control is given in [104]. Although the design process is performed for the LCC-HVDC system, the same POD model can be used for the VSC system. This is because the aim of this POD control is to modulate the power transfer through the HVDC converters between the two areas, which can be achieved by modulating the

power reference of the converter regardless the converter types.

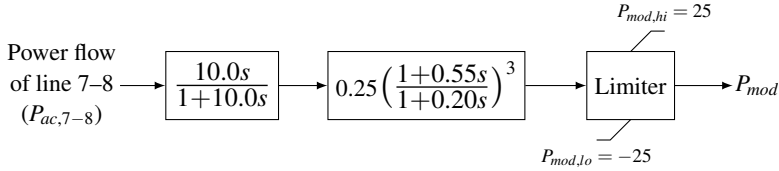


Fig. 5.19: The POD control structure for VSC3 station with parameters retrieved from [104]. The output P_{mod} is connected with dx in the IFC for VSC3.

The simulation of the system depicted in Figure 5.18 has been performed using PowerFactory software with a simulation time of 20 s and time step of 1 ms. The following scenarios have been considered, i.e.:

1. The POD control is not active, i.e. by setting the gain of the first lead-lag filter in Figure 5.19 to zero.
2. The POD control is active but without any disturbance in the DC system, i.e no ramp up action in the OWF power production.
3. This is the same as the previous scenario, but before the AC fault is applied, the power production of OWF is ramped-up at 0.1 s.
4. This is the same as the previous scenario, but at 8 s VSC2's power reference is reduced to -150 MW with a ramp speed of 20 MW/s.

In this subsection, the local measurement is used instead of the pilot *DroopCtrl* method. Therefore, the MTDC system has the same setting as used in Subsection 5.2.5. Since in the behavior of the pilot *DroopCtrl* method is similar to the one with the local measurement (describen in Subsection 5.2.7), the same behavior is expected when the POD control is integrated with the pilot *DroopCtrl* method. The simulation results with the pilot *DroopCtrl* method are shown in Appendix G.

From Figure 5.20, when the POD control is disabled (Scenario 1), the inter-area oscillations occur with a damping (ζ) of 0.026 and a frequency of 0.61 Hz. By activating the POD control (Scenario 2), these inter-area oscillations can be damped to a ζ of 0.081 and a frequency of 0.63 Hz. The POD is realized by modulating the droop line reference along the x -axis for the IFC used in VSC3, i.e. shown in Figure 5.21.

From Figure 5.21, the movement path of VSC3's operating points is from bottom-left towards upper-right corner, while for VSC2 and VSC4, the movement follows the referred droop line. This difference occurs because the droop line is shifted in VSC3, which changes the condition in the DC grid. So, to keep up with the movement of the

Chapter 5. Simulation results

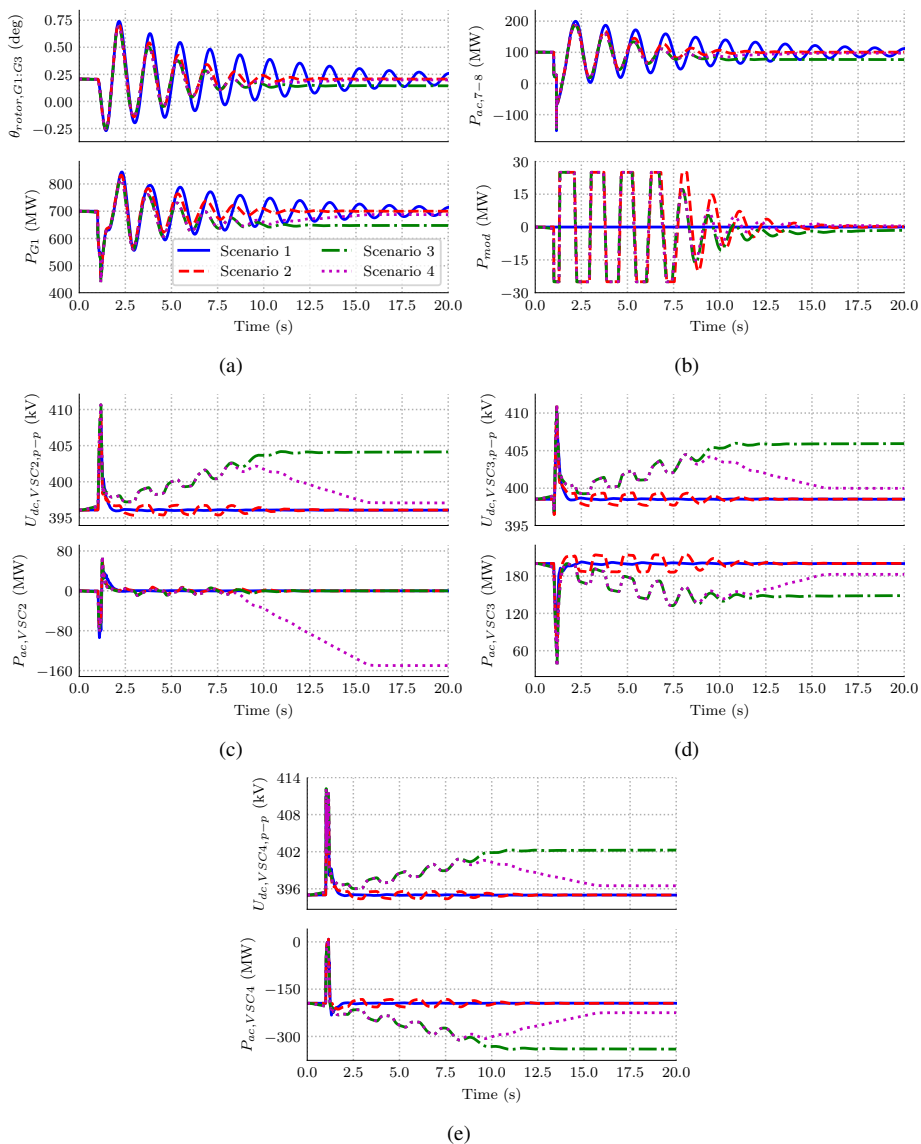


Fig. 5.20: Simulation results with the POD control is placed in VSC3. (a) Measured rotor angle of G1 relative to G3 ($\theta_{rotor,(G1:G3)}$), the active power output of G1 (P_{G1}), (b) AC tie-line power flow ($P_{ac,7-8}$), and POD control output (P_{mod}). (c), (d), (e) Pole-pole DC voltage and active power measured at the terminal of VSC2, VSC3, and VSC4. The blue, red, green, and magenta lines represent the results for Scenario 1, Scenario 2, Scenario 3, and Scenario 4, respectively.

droop line, the DC voltage of VSC3 might need to be increased, which also means an increase of power injection towards DC-side (more power rectification). Hence, in the

droop plane, this can be illustrated as a movement towards the upper-right side of the Cartesian plane. Whereas for VSC2 and VSC4, the droop line is not modulated as the one for VSC3, i.e. VSC2 and VSC4 follows the designated droop line when the DC voltage condition changes.

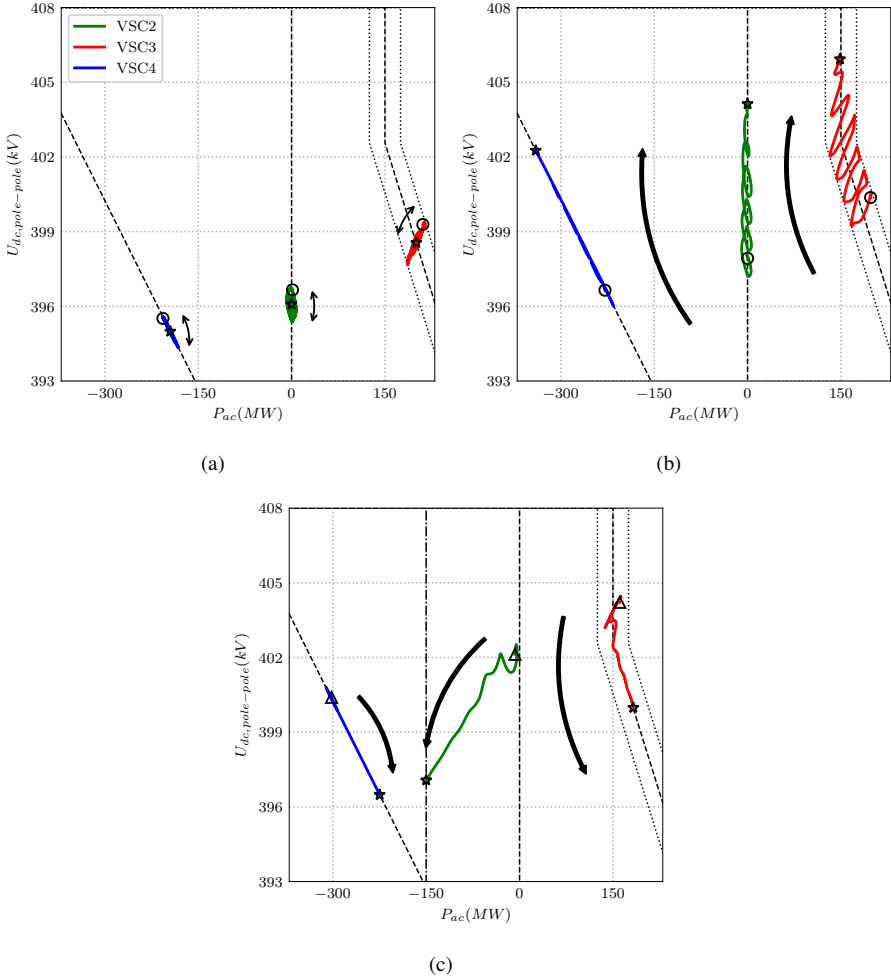


Fig. 5.21: The droop plane plots of VSC2, VSC3, and VSC4 for: (a) Scenario 2, (b) Scenario 3, and (c) Scenario 4. The bold black lines represent the droop line characteristics. The dotted lines in VSC3 represent the maximum and minimum changes of the droop line, while the dash-dot line in (c) represents the droop line at the end of VSC2 ramp. The arrows point the movement direction. The points marked with \circ , $*$, and Δ represent measured values at 2.0 s, 8.0 s, and 20 s respectively. The animated plots for these results are shown in Figure I.9–Figure I.13.

When the OWF power is increased, both VSC3 and VSC4 start to react. This behavior is similar to the one presented in Subsection 5.2.5. The simulation results

in Figure 5.20 for Scenario 3 shows the combination of the behavior of VSC3 and VSC4 shown in Figure 5.10 with the one for Scenario 2 (POD is active). It looks like pulling the trajectory of the operating points depicted in Figure 5.21(a) along the droop line, due to OWF ramp up event (Figure 5.11); hence the trajectory depicted in Figure 5.21(b). Furthermore, the inter-area oscillations become more damped for Scenario 3 as compared to Scenario 2. For Scenario 3, the inter-area mode ζ becomes 0.1 with a frequency of 0.63 Hz.

Changes in the VSC2 (Scenario 4) do not give so much impact in the inter-area oscillations as compared to Scenario 3. This is because the active power is increased at 20 MW/s instead of a sudden change as the one during AC fault event. If the changes in active power happen very fast, it might initiate other inter-area oscillations [40].

5.3. THE 9-TERMINAL HVDC SYSTEM

Figure 5.22 depicts the CIGRÉ's DCS3 DC grid test system, which has in total 11 converter terminals but is separated into 3 different zones [106,119]. As can be seen in Figure 5.22, Zone 1 is isolated from the rest of the system and act as a standalone PtP system, whereas Zone 2 is interconnected with Zone 3. Hence, a 9-terminal HVDC test system which is comprised by all the converters in Zone 2 and Zone 3. The modeling approach and parameters of the converters, DC cables, overhead lines, and DC/DC converters are given in Appendix A.

Zone 1 and Zone 3 consist of symmetric-monopole converters rated at ± 200 kV, while Zone 2 consists of bipolar converters rated at ± 400 kV. The bipolar converter is built as a series connection (DC-side) between two asymmetric-monopole converters (each rated at 400 kV). An ideal DC/DC converter (Cd-E1) is used to interconnected these two zones. This means that a lossless voltage conversion is achieved by keeping a constant ratio between both ends, i.e. with a transformation ratio of 2 for Cd-E1. The modeling approach of this DC/DC converter is described in Section A.3.

The rating, control mode, and setpoints of each converter in the DCS3 test system are given in Table 5.4. The power transfer between Zone 2 and 3 is dictated by Cb-A1 and Cm-B2, which act as the DC slack nodes for each zone (operated in *UdcCtrl* mode). In steady-state condition, the power transfer from Zone 2 to Zone 3 is approximately 200 MW.

Furthermore, the IFC is implemented in all converters within the 9-terminal HVDC system, except in Cm-E1 which is operated in the *IslCtrl* mode. Each bipole converter is consisted of two monopole converters connected in series (in the DC-side). Therefore, two converter control units are used, i.e. one for each pole. Hence, two IFC units are also used in each of these converters. The droop line reference for each of the IFC

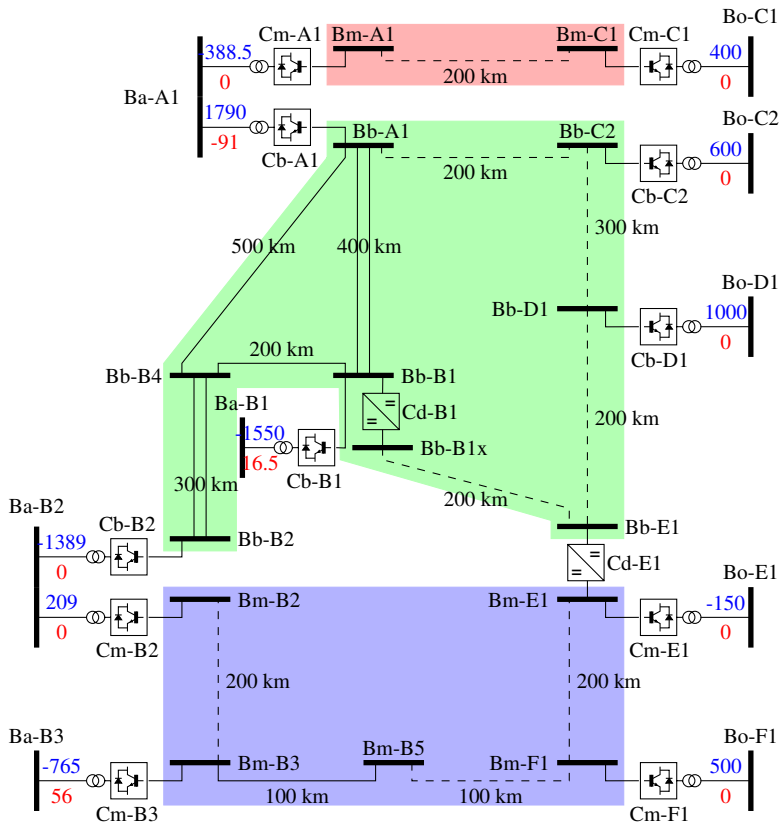


Fig. 5.22: CIGRÉ's DCS3 DC grid test system [106, 119]. The dashed lines represent DC cable while solid line represents overhead line. Bipole converters (± 400 kV) are indicated by Cb while Cm indicates symmetric monopole converters (± 200 kV). Colored areas show different DC zones, i.e.: Zone 1 (red), Zone 2 (green), and Zone 3 (blue). By considering Table 5.4, the steady-state power flow condition of the system is given in blue (active in MW) and red (reactive in MVar) numbers with positive values refer to a flow towards the DC-side. The electrical parameters for each of these converters are given in Table A.2.

unit is given to realize the control mode given in Table 5.4 with $\pm 5\%$ limits from the nominal DC voltage.

Each of the Ba buses in Figure 5.22 is connected to a Thévenin source with a short circuit capacity of 30 GVA. Whereas a short circuit capacity of 4 GVA is used for the Thévenin source connected to each Bo buses except Bo-E1. A three-phase 150 MW load is connected to Bo-E1, instead of voltage source.

Furthermore, these test cases have been implemented in PSCAD software and the simulations were performed with a simulation time step of $50 \mu\text{s}$. It takes approximately 6 s to finish the start-up process and reach a steady-state condition. The power

Table 5.4: The control modes, ratings, and setpoints of the converters in the DCS3 test system [48]. Positive power refers to a power flow towards the DC-side. The bipole converters in Zone 2 are comprised of two asymmetric-monopole converters with the same rating. The setpoints for the *DroopCtrl* mode is given as the values of $P_{ac,0}$, $U_{dc,0}$, and k_{droop} . The electrical parameters for each of these converters are given in Table A.2.

DC zone	Station	Rating	Control modes	Setpoints
Zone 1 (± 200 kV)	Cm-A1	800 MW	<i>UdcCtrl</i> <i>QacCtrl</i>	± 200 kV 0 MVar
	Cm-C1	800 MW	<i>PacCtrl</i> <i>QacCtrl</i>	400 MW 0 MVar
Zone 2 (± 400 kV)	Cb-A1	2x1200 MW	<i>UdcCtrl</i> <i>UacCtrl</i>	± 404 kV 380 kV
	Cb-B1	2x1200 MW	<i>DroopCtrl</i> <i>UacCtrl</i>	-1500 MW; ± 400 kV; 0.067 kV/MW 380 kV
	Cb-B2	2x800 MW	<i>DroopCtrl</i> <i>UacCtrl</i>	-1400 MW; ± 400 kV; 0.1 kV/MW 380 kV
	Cb-C2	2x400 MW	<i>PacCtrl</i> <i>QacCtrl</i>	600 MW 0 MVar
	Cb-D1	2x800 MW	<i>PacCtrl</i> <i>QacCtrl</i>	1000 MW 0 MVar
	Cm-B2	800 MW	<i>UdcCtrl</i> <i>QacCtrl</i>	± 200 kV 0 MVar
Zone 3 (± 200 kV)	Cm-B3	1200 MW	<i>DroopCtrl</i> <i>UacCtrl</i>	-800 MW; ± 200 kV; 0.067 kV/MW 380 kV
	Cm-E1	200 MW	<i>IslCtrl</i>	145 kV; 50 Hz; with a 3-phase 150 MW load
	Cm-F1	800 MW	<i>PacCtrl</i> <i>QacCtrl</i>	500 MW 0 MVar

flow during the steady-state is given in Figure 5.22. After the MTDC system reaches steady-state, two events are performed and analyzed in the following subsections, i.e.: the emergency power order, and the gain-scheduled control implementation. The startup process of the system and other additional cases, which are similar to the ones presented in Section 5.2, are shown in Appendix H.

5.3.1. EMERGENCY POWER ORDER

An emergency power control can be activated by the operator to rapidly change the active power transfer between the converter and the AC grid. This action can be executed, e.g. by quickly change the active power reference of the converter to zero. In the case when the IFC is used, this action can be achieved by changing the dx input to the IFC (discussed in Section 4.4).

In order to simulate the emergency power control action and its impact on the MTDC system, the active power reference of Cb-D1 in Figure 5.22 is reduced from 1000 MW to 0 MW in 1 second. Since Cb-D1 is operated as rectifier, the reduction causes a shortage of power in the MTDC system. Hence, the DC voltage tends to reduce, which is shown in Figure 5.23.

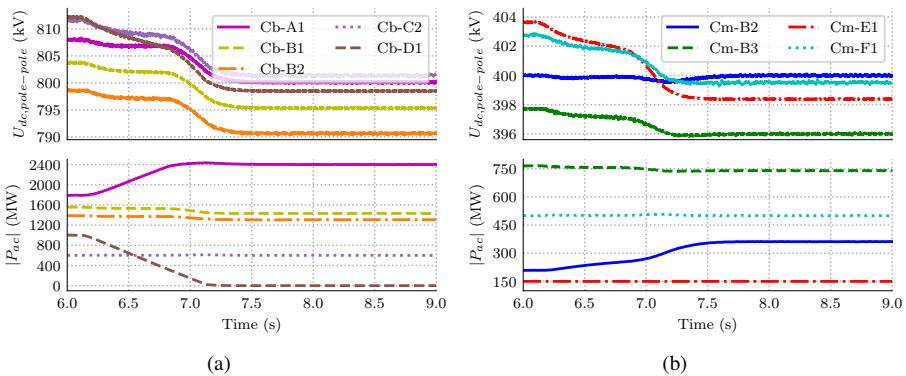


Fig. 5.23: The pole-pole DC voltage and the absolute value of active power measured for the terminals in: (a) Zone 2, (b) Zone 3. The absolute values of active power are used since there is no power reversal during the emergency power order in Cb-D1. Thus, the power directions are the same as the ones shown in Figure 5.22.

Since Cb-A1 and Cm-B3 are operated in the *UdcCtrl* mode, these two converters are the ones mainly responsible for balancing the power in the MTDC system. As can be seen in Figure 5.23(a), the DC voltage in Cb-A1 is controlled at ± 404 kV level by increasing the active power transferred from the AC grid. The similar behavior can also be seen as well for Cm-B2 in Figure 5.23(b), i.e. controlled at ± 200 kV level. A slight deviation around this number is caused by the dynamic response of the existing *UdcCtrl*.

However, the active power transfer through Cb-A1 is limited up to $\pm 2 \times 1200$ MW, i.e. given in Table 5.4. At 6.8 s, Cb-A1 shift its control mode to the *PacCtrl* in order to keep the active power within the limits (shown in Figure 5.23(a)). Hence, as soon as Cb-A1 shifts its control mode, Cm-B2 becomes the only converter in the MTDC system that is still in the *UdcCtrl* mode. The DC voltage in Cb-A1 starts to drop

rapidly due to the power shortage in the DC grid, which affects the DC voltage in Zone 3. Therefore, the ramp speed in active power through Cm-B2 increases in order to balance the power in the DC grid (depicted as the blue curve in Figure 5.23(b)).

The converters in the *DroopCtrl* mode (Cb-B1, Cb-B2, and Cm-B3) are also affected by the emergency power order in Cb-D1, because these converters are also involved in maintaining the DC voltage. Since in steady-state they are operated as inverter, their active power transfer from the DC grid is reduced when this event happens. As can be seen in Figure 5.23(b), the active power reduction measured at Cb-B1 is larger than the one at Cb-B2, i.e. due to a lower droop constant used in Cb-B1 (given in Table 5.4).

Since the *PacCtrl* in Cb-C2 and Cm-F1 is realized using the IFC, the changes in the DC grid affect the active power condition of these converters. In Cm-F1 the maximum deviation in the active power equals to 8.46 MW, whereas for Cb-C2, it equals to 13.72 MW.

Lastly, the converter in the *IslCtrl* mode (Cm-E1) is not affected by the emergency power order in Cb-D1. Although the DC voltage measured at the terminal of Cm-E1 changes, the active power transfer through this converter is kept constant, because the transfer is driven by the three-phase AC load.

It can be seen in Figure 5.23, the IFC used in all non-islanded converters within the 9-terminal HVDC system can bring the converters to a new steady-state condition after the emergency power order in Cb-D1. The new steady-state of the MTDC system is achieved 0.4 s after the active power at Cb-D1 reaches 0 MW. The behavior of these converters during this process is also as expected. A comparison of the system's behavior without the IFC (conventional converter control) for this particular case is also shown in Appendix H.

5.3.2. GAIN-SCHEDULED CONTROL IMPLEMENTATION

From Subsection 5.2.4, it was found that the phase compensator within the IFC makes a prominent difference when there is an abrupt change in the DC system. Therefore, in this subsection, a similar event (a simultaneous trip of both Cb-B2 and Cm-B2) has been considered for a 9-terminal HVDC system to evaluate the gain-scheduled control implementation discussed in Subsection 4.3.4.

At 6.1 s, both Cb-B2 and Cm-B2 are tripped and removed from both AC- and DC-side, which result in approximately 1180 MW power surplus in the DC system. Furthermore, Cb-A1 becomes the only DC-side slack converter for Zone 2 and Zone 3. However, since Cb-B1 and Cm-B3 are operated in *DroopCtrl* mode, the responsibility to balance the power in the DC grid is shared between these converters and Cb-A1.

When both Cb-B2 and Cm-B2 are tripped, each of the converter control of these converters sends out $DBLK = 0$ signal to the DC grid secondary control. The DC grid secondary control then sends out an updated value of CFG_{dc} . The remaining converters in either the $UdcCtrl$ or the $DroopCtrl$ are only Cb-A1, Cb-B1, and Cm-B3. The CFG_{dc} value is then received by these converters and used to schedule T_{ld} and T_{lg} values for the phase compensator in them. Furthermore, since these converters have the same rating and the same time response of the existing $UdcCtrl$, the same T_{ld} and T_{lg} values can be applied.

The same design procedures (using the similar test system and OE-EMT method explained in subsection 4.3.4 to speed up the $UdcCtrl$ responses) have been performed to obtain the time constants for the phase compensator. From Table 5.4, the total capacity of the remaining converters after the trip event equals to 10400 MW, i.e. 3.2 times larger than the 4-terminal HVDC system. Hence, a larger equivalent capacitance as compared to the equivalent 4-terminal HVDC system used in subsection 4.3.4.

These design procedures can reflect both bipole (Cb-A1 and Cb-B1) and symmetric-monopole (Cm-B3) converters, because each of these bipole converters uses the same two asymmetric-monopole converters with the same rating as the Cm-B3 converter. Hence, the tuning of the phase compensator in Cm-B3 can be used to get the same behavior for Cb-A1 and Cb-B1. The OE-EMT simulation results are given in Table 5.5.

Table 5.5: The DLT component controller's gains obtained using OE-EMT simulation.

Run #	T_{ld} (s)	T_{lg} (s)
1 (initial)	0.0900	0.0900
31 (final)	0.1076	0.0269

For simplicity, the lookup table for the gain-scheduled control is similar to this table, i.e. the first row represents the condition without the compensation, while the second row represents the condition when phase compensator inside the IFC is active. For comparison, both simulation results with and without gain-scheduled control implemented in Cb-A1, Cb-B1, and Cm-B3 are depicted in Figure 5.24.

As compared to the 4-terminal HVDC system (shown in Figure 5.8), the improvement of having controller gains scheduled for different MTDC configuration becomes more evident. This is because the phase-lead given by the phase compensator is a lot larger due to a higher total converter's equivalent capacitance value than the 4-terminal HVDC system.

In general, the deviation in the DC voltage is reduced when the phase compensator gains are scheduled. In Figure 5.24(b) and Figure 5.24(d), the DC voltage overshoot magnitude is reduced by 4 kV (pole-pole) when the phase compensator is activated. In Figure 5.24(a) and Figure 5.24(c), the largest difference in DC voltage with and

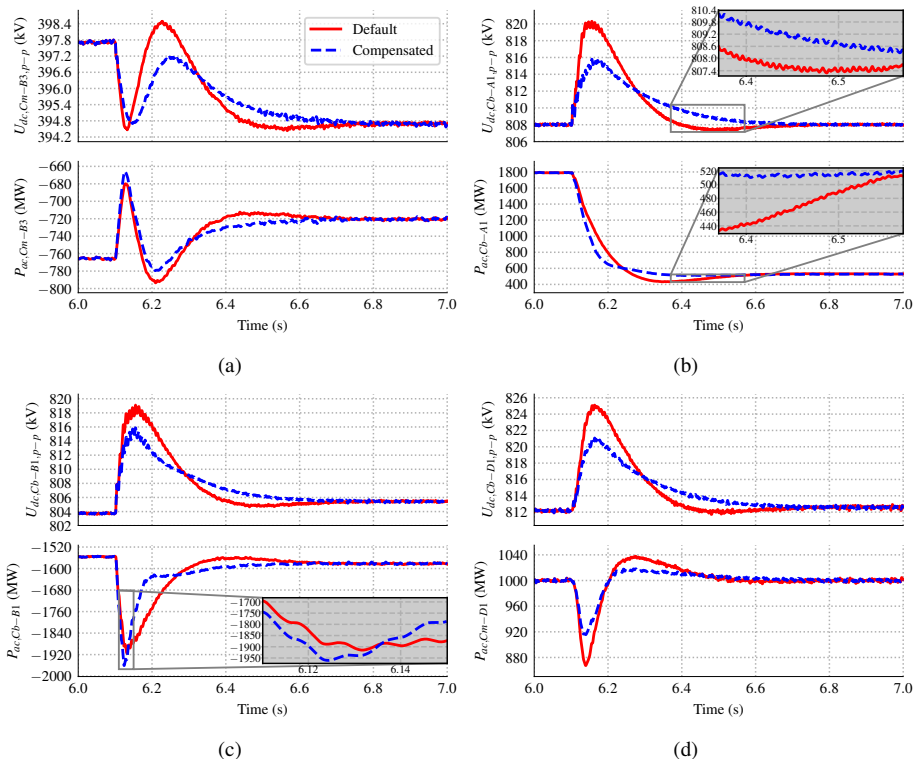


Fig. 5.24: The pole-pole DC voltage and active power measured at the terminal of: (a) Cm-B3, (b) Cb-A1, (c) Cb-B1, and (d) Cb-D1, with and without the phase compensator. The red lines represent the condition without the phase compensator, whereas the blue lines represent the condition with the phase compensator activated.

without the phase compensator is 1.2 and 2 kV (pole-pole), respectively. This improvement happens because the time response of the DC voltage for Cb-A1, Cb-B1, and Cm-B3 is increased.

Since Cb-A1 is operated in the *UdcCtrl* mode, this converter takes the biggest part in balancing the power in the DC system. As can be seen in Figure 5.24(b), the power transfer of Cb-A1 is reduced by approximately 1200 MW to compensate the loss of Cb-B2 and Cm-B2. Some portions of the power balancing responsibility is shared between Cb-B1 and Cm-B3, which are operated in the *DroopCtrl* mode. Before the trip event, Cb-B2 is operated as inverter. Therefore, when Cb-B2 is blocked, the voltage at Cb-B1 started to increase due to a surplus of active power in the DC system. Hence, Cb-B1 injects more power to the AC grids as before (depicted in Figure 5.24(c)). Whereas CmB2 is operated as rectifier before the trip of Cm-B2. Hence, Cm-B3 injects less power to the AC grids (depicted in Figure 5.24(a)).

The rest of the converters in the 9-terminal HVDC system are operated in the *PacCtrl* mode (except for Cm-E1, which is in the *IslCtrl* mode). The gains for the existing *UdcCtrl* is not scheduled in these converters. Therefore, the IFC is only used to mimic the *PacCtrl* mode behavior. As mentioned earlier, the magnitude of the overshoot in the active power correlates with the deviation in the DC voltage, i.e. shown in Figure 5.24(d).

GAIN-SCHEDULED CONTROL IMPLEMENTED ONLY IN CB-A1

As can be seen in Figure 5.24, when the controller gains are scheduled (using the phase compensator within the IFC), Cb-A1 has the largest impact as compared to Cb-B1 or Cm-B3. This happens because Cb-A1 acts as the DC slack bus of the system, which maintains a constant DC voltage for Zone 2 and Zone 3. This means that the DC voltage response of the system when Cm-B2 and Cb-B2 are blocked might depend on the behavior of Cb-A1 alone. So, in this subsection, only Cb-A1 that has the phase compensator, whereas the rest of the non-islanded converters in the 9-terminal HVDC system only activate the DLT method within the IFC. The simulation results with only one gain-scheduled control is implemented are depicted in Figure 5.25.

Figure 5.25(b) confirms that the behavior of the system during the disturbance will depend on the Cb-A1. The influence of the converters operated in the *DroopCtrl* mode to the DC voltage behavior measured at Cb-A1 terminal becomes insignificant. Furthermore, as shown in Figure 5.25(a) and Figure 5.25(c), although there are slight changes in the behavior when the phase compensator is deactivated in Cm-B3 and Cb-B1, the difference is not as substantial as the behavior when the phase compensator is deactivated in all the converters.

Therefore, for the 9-terminal HVDC system, which has a combination of converters in the *UdcCtrl* and *DroopCtrl* modes, it might be enough to implement the gain-scheduled control in the converter operated in the *UdcCtrl* mode. This is because the influence of the gain-scheduled control for the *DroopCtrl* mode is not as significant as the one in the *UdcCtrl* mode. This might be beneficial especially when the delay to send the CFG_{dc} is considered (discussed in the following subsection).

For the case which has several converters operated in the *UdcCtrl* mode, the converter closest to the disturbance source has more impact as compared to the others (similar as the behavior from the previous subsection). However, further contingency studies are needed to decide how the gain-scheduled control should be implemented.

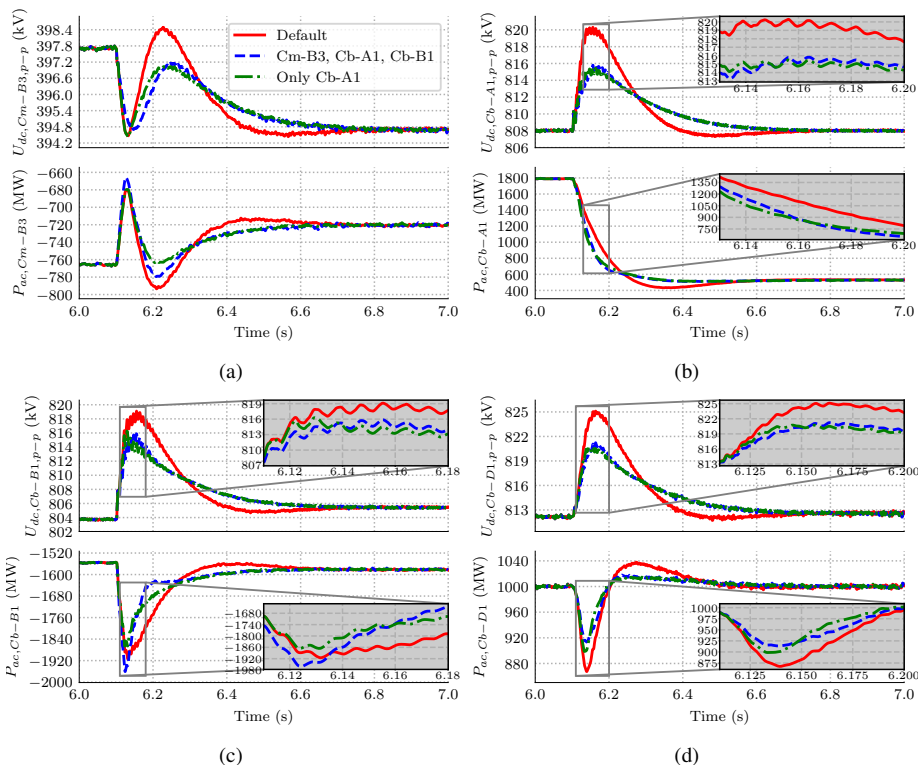


Fig. 5.25: The pole-pole DC voltage and active power measured at the terminal of: (a) Cm-B3, (b) Cb-A1, (c) Cb-B1, and (d) Cb-D1. The red lines represent the condition without the phase compensator, the blue lines represent the condition with the phase compensator activated in Cm-B3, Cb-A1, and Cb-B1, whereas the magenta lines represent the condition with the phase compensator activated only in Cb-A1.

THE INFLUENCE OF COMMUNICATION DELAY

As discussed in Section 3.2, a communication medium is required between the DC grid secondary and each primary controls within an MTDC system. This communication medium can be based on either a fiber optic, radio, power line communication, or even a combination of these. The gain-scheduled method requires the DC grid primary controls to send their status to the secondary one, and then based on the status of the system, the DC grid secondary control sends the appropriate CFG_{dc} signal back to the converters. Therefore, it is important to consider the impact of communication latency on the speed to schedule the gains of the DC grid primary controls.

Three delay values of 10 ms, 30 ms, and 100 ms, are considered for receiving the updated CFG_{dc} signal from DC grid control are considered. It should be noted that 100 ms is an exaggerated value since the practical delay is between 10–30 ms [122].

The simulation results are then depicted in Figure 5.26.

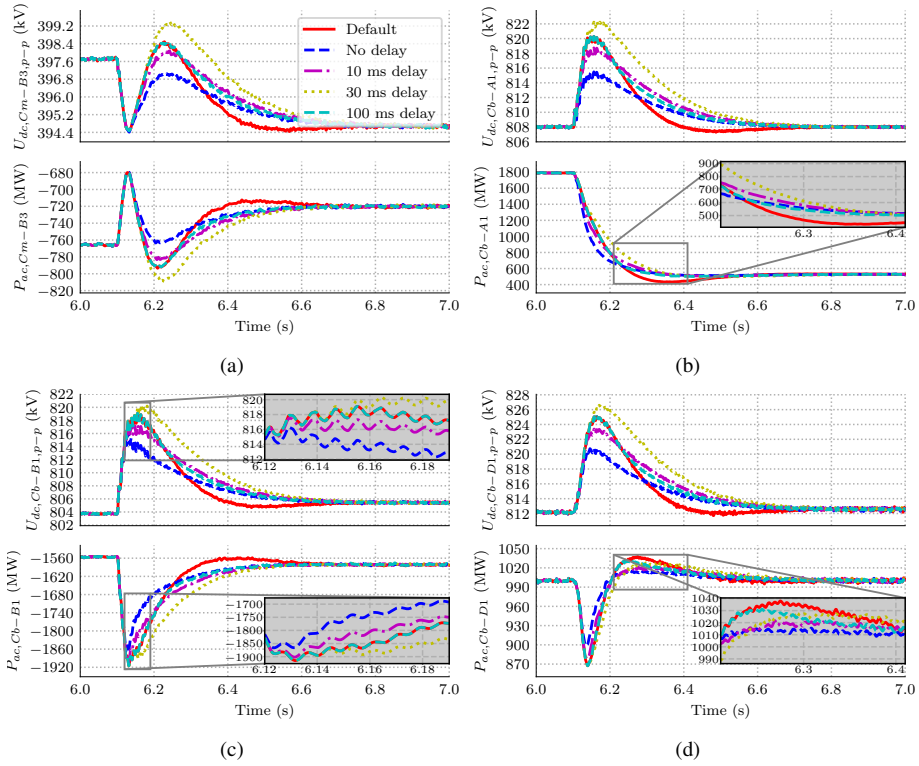


Fig. 5.26: The pole-pole DC voltage and active power measured at the terminal of: (a) Cm-B3, (b) Cb-A1, (c) Cb-B1, and (d) Cb-D1. The red lines represent the condition without the phase compensator, the blue lines represent the condition with the phase compensator activated in Cb-A1. The magenta, yellow, and cyan lines represent the condition when the phase compensator is activated with 10, 30, and 100 ms communication delay, respectively.

From Figure 5.26, it can be seen that the longer the time delay to receive a new CFG_{dc} value, the longer Cb-A1 scheduled its controller gains. As a consequence, the behavior of the system after the trip of Cb-B2 and Cm-B2 becomes closer to the *default* case. This can be seen in the overshoot of the DC voltage. Even worse, when the communication delay of 30 ms, the overshoot DC voltage becomes higher than the *default* case. This is because the DC voltage reaches its peak overshoot 30 ms after the trip and the phase compensator gets the new time constants when it sees the highest DC voltage deviation.

For the converters operated in the *PacCtrl* or the *DroopCtrl* mode, the active power transfer is related to the deviation of the DC voltage. So, for these converters, the impact of the communication delay is directly related with the active power performance.

Therefore, a high speed communication (below 30 ms delay) between the converters and the DC grid secondary control is needed. This could be achieved since in practice the latency is expected to be in the range of 10–30 ms [122].

5.4. SUMMARY

In this chapter, two test systems have been used to demonstrate the proposed methods in this thesis. The first test system is a 4-terminal HVDC system, which is formed as interconnection of an OWF link and a shore-to-shore link. The steady-state range evaluation for the interconnection of these links were performed, which result in a new operational range of the interconnected system. Some examples of the operating points for two power flow scenarios have been shown.

The IFC has been implemented in all onshore converters of the 4-terminal HVDC system. The following simulation cases have been performed to evaluate the performance of system when the IFC is activated:

1. Startup of the MTDC system. By using the IFC, the converter can be operated in the *PacCtrl* mode. Furthermore, a lower spike in active power behavior using the IFC can be expected during the startup of the *UdcCtrl* station, since the DC voltage builds up in a slower rate as compared to the conventional control.
2. Smooth transition between two droop references. The rate limiters have been used before the new droop reference is given to the IFC unit. The MTDC system can achieve a new steady-state condition at a slower rate shown by the simulation results.
3. Phase compensator performance. Two dynamic events were considered, i.e. OWF power ramp up and a bolted three-phase AC fault with a duration of 100 ms. It was found that the phase compensator makes a difference when there is an abrupt change in the system (AC fault).
4. Advanced converter control. A multi-slope droop reference is given to one of the onshore converters. It was shown that the IFC enables the converter to be operated in different converter control modes depending on the condition of the DC voltage and active power.
5. Loss of a converter. With the advanced converter control, a new steady-state condition following a fast and severe disturbance in the DC system (e.g. loss of a converter) can be set up. The simulation results indicated that the new steady-state condition can be achieved in less than 0.5 s after the disturbance.
6. Pilot voltage droop control test. The implementation of the pilot *DroopCtrl*

method has been tested. It was found that the behavior of the system following a disturbance is similar to the one with the local measurement.

7. Integration of POD control. It was shown that the MTDC system at the same time can both controlling the DC grid, by sharing the OWF power production, and damping the oscillations in the AC grid, by integrating the POD control with the IFC. This proves that the IFC can enable the converter to perform AC and DC grid control simultaneously.

The second test system was a 9-terminal HVDC system, which has one mesh within the DC grid. Hence, a more complex network. The IFC has been applied to 8 converters to achieve different control modes. As a first test, an emergency power order has been enforced in one of the converter, by modifying the dx input of the IFC used in this converter. The behavior of the converters were as expected, which proves the ability of the IFC to operate the converter in *UdcCtrl*, *PacCtrl*, and *DroopCtrl* modes.

The gain-scheduled control implementation has been evaluated as well using the 9-terminal HVDC system. It was found that by scheduling the time constants of the phase compensator, the behavior of the system, after the trip of two converters, can be improved. Furthermore, the gain-scheduled control can be applied only in the converter operated in *UdcCtrl* mode, since the behavior of the MTDC system depends on the behavior of this converter. However, when a time delay was introduced for scheduling the time constants, the benefit of having the gain-scheduled control was reduced.

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CHAPTER 6. CONCLUSIONS

6.1. CONCLUSIONS

In areas where several HVDC links are in operation, it is more likely to build an MTDC system by interconnecting some of these links or expand an existing link by connecting it with an additional converter. The COBRACable project is currently being constructed as a PtP link connecting Denmark and the Netherlands, but in the future, it is expected to be operated as an MTDC system by hosting one or more converters along its cable so that it becomes part of the North Sea DC grid.

When expanding an existing PtP link, it is likely that the existing components are kept as they are. Especially if the operational life of the link is still long, replacement of the existing system with the new one, to enable the expansion, might be avoided. Hence, a *plug and play* principle is proposed in this thesis. This means that when a PtP link is expanded into an MTDC system, the existing converters should not be replaced with new ones to satisfy the MTDC operation.

In this thesis, the expansion plan of a PtP link has been discussed. The steady-state DC voltage operational range becomes the first checkpoint to evaluate the plan. Furthermore, a new control layer between the DC grid primary and secondary control has been introduced to allow coordination between the converters of the expanded system. These methods can be summarized in the following as the answers to the key objectives defined in Chapter 1.

The changes in the steady-state DC voltage operational range of a PtP link when this link is expanded. In Chapter 2, an analytical method has been proposed to estimate the new steady-state DC voltage operational range when new converter(s) is interconnected with the existing PtP link. The sensitivity of several factors to the shape of the new operation range for the MTDC system have been analyzed. These factors are: the ratings and location of the new converter, its distance from the DC hub, and the location of the DC hub from either of the PtP link stations.

The impact of the new operational range to the operation of the system. From the new steady-state operational range of the system, the decision of expanding the PtP link can then be justified. It might happen that the MTDC system operation might become limited to ensure operating points of the system within the range. Thus, if the operational constraints are accepted, the expansion of the link can be considered feasible, or specifications for the additional converter(s) can be drawn in order to avoid these constraints.

The DC grid control concept that allows expansion of the system. After knowing the operational range of the system, the next step is to coordinate the converters within the MTDC system to reach a steady-state condition following a disturbance. Chapter 3 describes a hierarchy structure of DC grid controller, which is based on to the frequency control in the AC grid due to the similarities between DC voltage in DC grid with frequency in the AC grid. However, the implementation of this concept in the expandable PtP link might be complicated. This is because the converter control systems are vendor specific and usually protected by patents or even if they came from the same vendor, they might become obsolete because of a rapid development in the VSC technologies. Therefore, in the last part of Chapter 3, a new control layer has been proposed to ease the implementation of the hierarchical concept of DC grid control. This additional layer becomes the interface between the DC grid secondary and primary control. By using this interface (IFC), the converter is always operated in *UdcCtrl* mode and receives the reference from the IFC. As seen from the DC grid secondary control, each of the converters can be operated in different control modes (*UdcCtrl*, *PacCtrl*, and *DroopCtrl*) by merely changing the input to the IFC. Thus, simplifying the requirements for a converter to be involved in the DC grid control to: (a) *UdcCtrl* mode is available, and (b) the DC voltage reference is externally adjustable. The design of the IFC is discussed in Chapter 4 along with its functionalities. In general, the IFC has three main features, i.e. droop line tracking (DLT), phase compensator, and droop shift.

The interoperability between various vendors. With the IFC, the converter only needs to provide the DC voltage reference to be available, while the measurement signals required by the IFC can come from the existing systems or the new ones. Furthermore, the IFC is implemented by considering a modular approach, which means that the method becomes an external function for the existing system. A realistic example is during the feasibility studies performed using the converter models from various vendors. The existing vendor-specific (black-box) models can be used directly as long as the DC voltage reference for each model is adjustable. Or in other words, these black-box models with the DC voltage reference input is sufficient to perform the studies, without the need to ask the vendor to change their model, such that it follows the predefined prerequisites (e.g. some measurement signals and control parameters to be exchanged). Hence, the IFC eases different vendors to build a multi-vendor MTDC system.

A generalized converter control. The DLT method is inspired by a line-tracking robot, thus the DC voltage reference for converter is adjusted such that it follows a designated droop line. Using the DLT, the three control modes can be simply achieved by changing the slope of the droop line reference. Furthermore, an advanced converter control, i.e. represented by a piecewise linear (PWL) line, can be implemented using the same control structure.

External adjustment of the converter control response. When the DC system configuration is changed, e.g. by blocking/deblocking the converters within the MTDC system, the existing converter control behavior is affected by how many converters are active within the DC system. Hence, a gain-scheduled control is needed to adjust the behavior of the system depending on the MTDC configuration. The phase compensator within the IFC facilitates the implementation of this gain-scheduled control, by giving a phase-lead or phase-lag such that the existing converter control acts as expected. This means that by using the IFC, the existing control structures are unaltered to realize this gain-scheduled control.

Integration of auxiliary control functions. The existing PtP link might already have the auxiliary control functions in place. This means that if this link is expanded into an MTDC system, these auxiliary functions might need to be retained. In principle, the auxiliary control functions modify the active power reference of the converter. Hence, this can be perceived by shifting the droop reference. Therefore, the auxiliary functions can be integrated easily using the IFC. The IFC also gives benefit when a new auxiliary control function needs to be implemented, i.e. the function can be implemented without the need to alter the existing control system.

Lastly, in Chapter 5, two test systems have been considered for demonstrating how the IFC can enable the control coordination within the MTDC system. The first test system is a 4-terminal HVDC system, which is constructed by interconnecting a PtP link with an OWF link. The evaluation of the steady-state operation range when these links are interconnected has been performed. EMT simulations in PSCAD software have been performed to show the startup process, changing the control mode of the converter, and dynamic behavior of the system under AC fault and power ramping. RMS simulations in PowerFactory software have also been performed to show the integration of a POD control.

The second test system is a 9-terminal HVDC system, which has a mesh and is constructed from various converters with different ratings. The IFC is used in all 8 non-islanded converter to represent *UdcCtrl*, *PacCtrl*, and *DroopCtrl* mode. An emergency power order in one of the station and its impact to the DC grid were evaluated. Furthermore, the gain-scheduled control implementation was studied. Both EMT and RMS simulations performed using both test systems have shown that the results are as expected demonstrating the usability of the IFC.

6.2. MAIN CONTRIBUTIONS

The main contributions of the study can be summarized as follows:

- An analytical method to estimate the new DC voltage operating range when a

PtP link is expanded into an MTDC system, i.e. by interconnecting additional converters into the existing PtP link. Based on this method, different factors influencing the steady-state operational range of the system are identified.

- A method to estimate the operating points of an MTDC system is proposed. The estimation is based on the power supply and demand forecast, without considering the losses in the converter and DC system.
- A new DC grid control layer (primary control interface), which ensures system expandability, is proposed. The modular approach also ascertains that the existing control systems remain unaltered when the PtP link is interconnected with another link or a new converter is added. Hence, this new layer enables the *plug and play* principle for developing a multi-vendor MTDC system.
- A new way of implementing DC voltage droop control by using the DLT method is proposed. Unlike the conventional droop control, the DLT method uses displacement error to calculate the new (DC voltage) reference. Hence, the converter can be operated in three different converter control modes (*PacCtrl*, *UdcCtrl*, and *DroopCtrl*) by merely changing the droop line reference.
- A phase compensator is proposed for adjusting the behavior of the existing *UdcCtrl* externally. A potential application of this component is for implementing a gain-scheduled control.
- Integration of auxiliary control functions into the converter control are discussed. By using IFC, the auxiliary control functions can be integrated by simply shifting the droop line reference along the x -axis.

6.3. FUTURE WORK

In this thesis, the possibility to coordinate the converters within the MTDC system by using the IFC has been demonstrated. The simulation results have revealed possible future paths that might need further investigations to prepare the expansion of an existing HVDC link. Some of these paths are explained as follows.

In this thesis, the POD control has been used in one converter of the 4-terminal HVDC system integrated with the two-area system to damp the inter-area oscillations. The simulation results indicate that different damping impact can be achieved when the MTDC system is subjected to changes in the OWF power production. Furthermore, since the POD (and the other auxiliary control functions) give an active power modulation input to the converter, it has also been shown that the converter control mode (the *PacCtrl* or *DroopCtrl* mode) might give different impact as well. Therefore, the design of the auxiliary control functions by considering the control mode of the converter and OWF power production is currently under investigation.

Apart for the DC voltage, the droop control concept is usually applied as well for the AC voltage. The AC voltage droop control is applied in the converter to avoid control hunting, i.e. when the converter is located close to another AC voltage controlling equipment (e.g. generator or HVDC converter). Since it is believed that the same droop line tracking (DLT) approach can be adopted, a research project is currently in progress to implement the AC voltage droop control using the DLT method. Hence, it will simplify the implementation of the q -axis controls.

The IFC has been implemented as a separate function for the existing converter control. In this thesis, both EMT and RMS simulations have been performed by using this function. The test using the black-box model for COBRACable research project has also been separately conducted. The next step is to implement the IFC in a control hardware and test it in a real-time environment. This needs further studies to determine the communication protocol used by various vendors, which could make the IFC more generic. Furthermore, a hardware in the loop (HIL) test involving converter control replicas from different vendors might also be considered.

The control coordination part of the MTDC system has been covered in this thesis. Furthermore, the simulations performed in this thesis do not involve any DC fault case. Therefore, DC grid protection coordination studies of the expandable MTDC system should be performed. Further analysis on the relation between different MTDC configurations with the over current or over voltage waveform is needed to define the protection strategy of the DC system.

Two test systems has been considered in this thesis, i.e. the 4-terminal HVDC system to represent the condition when the offshore DC grid is emerged and the 9-terminal HVDC system to represent the condition at a later stage. The study performed in this thesis might be extended by considering a radial configuration with more terminals or even a mixed installation of LCC- and VSC-based converters. Furthermore, the IFC method can also be tested using a DC system with more meshes.

In the 9-terminal HVDC system, two ideal DC/DC converters have been considered. This means that the DC/DC converter is a lossless system without any control implemented. In a meshed DC grid, the DC/DC converter can also be used as the DC power flow control (DCPFC). Since the power deviation sharing within an MTDC system is determined by the droop characteristic of each non-islanded converter within the system, this functionality can be extended by also considering the DCPFC component. Therefore, the possibility to incorporate this component with the IFC can be explored further.

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APPENDIX A. DC SYSTEM PARAMETERS

A.1. CONVERTER PARAMETERS

A.1.1. ELECTRICAL PARAMETERS

A half-bridge modular multilevel converter (HB-MMC) type has been considered in this thesis. The structure of HB-MMC is depicted in Figure A.1. A bipole configuration is achieved by cascading two asymmetric-monopole converters, such that from AC-side they are connected in parallel, while connected in series from DC-side.

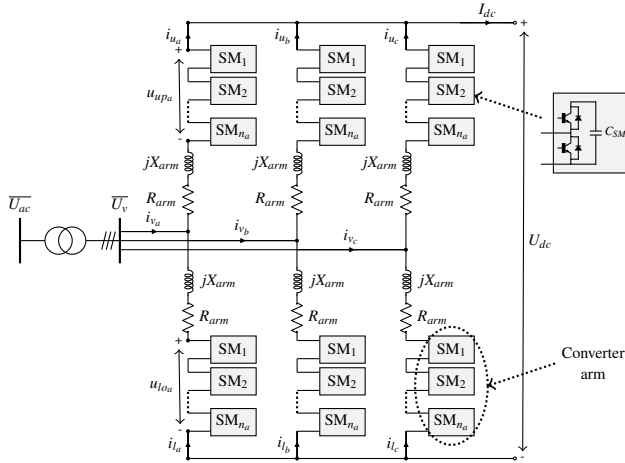


Fig. A.1: The structure of HB-MMC with n_a submodules (SMs) per converter arm [68].

The electrical parameters for an 800 MW converter used in Chapter 4 and the 4-terminal HVDC system depicted in Figure 5.1 are given in Table A.1. While the converter data for the 9-terminal HVDC system depicted in Figure 5.22 are given in Table A.2.

The detailed equivalent model (type 4) has been used in PSCAD software. This means that the submodules in each converter arm has been reduced into a Thévenin equivalent circuit [123]. The PSCAD module of this detailed equivalent model has been retrieved from [120].

The average value model (type 6) has been considered for PowerFactory software. The conversion of the EMT model into the RMS model is explained in Appendix C.

Appendix A. DC system parameters

Table A.1: The electrical parameters of the 800 MW converter system [48, 119].

Component	Data	Data id	Value	Unit
Transformer	Type	1	YNd11	
	PCC-side voltage	2	380.0	kV
	Converter-side voltage	3	220.0	kV
	Magnetizing current	4	1.0	%
	Leakage reactance (X_{xfr})	5	0.18	pu
	Copper losses (R_{xfr})	6	0.006	pu
	No-load losses	7	0.0	pu
Star point reactor	Inductance	8	5.0	kH
	Resistance	9	5.0	k Ω
Arm reactor	Arm inductance (L_{arm})	10	29.0	mH
	Arm resistance (R_{arm})	11	0.0	Ω
Submodules	n_a	12	200.0	
	C_{SM}	13	10.0	mF
	Conduction resistance	14	1.316	m Ω

Table A.2: The electrical parameters of the converters within the CIGRÉ's DCS3 DC grid test system depicted in Figure 5.22 [48, 119]. The data for all the bipole converters (Cb converters) are given as their pole data.

Data id	Cm-E1	Cb-C2	Cm-A1, Cm-B2, Cb-B2	Cm-C1, Cm-F1 Cb-D1	Cb-A1, Cb-B1 Cm-B3	Unit
1	YNd11	YNd11	YNd11	YNd11	YNd11	
2	145.0	145.0	380.0	145.0	380.0	kV
3	220.0	220.0	220.0	220.0	220.0	kV
4	1.0	1.0	1.0	1.0	1.0	%
5	0.18	0.18	0.18	0.18	0.18	pu
6	0.006	0.006	0.006	0.006	0.006	pu
7	0.0	0.0	0.0	0.0	0.0	pu
8	5.0	5.0	5.0	5.0	5.0	kH
9	5.0	5.0	5.0	5.0	5.0	k Ω
10	116.0	58.0	29.0	29.0	19.0	mH
11	0.0	0.0	0.0	0.0	0.0	Ω
12	200.0	200.0	200.0	200.0	200.0	
13	2.5	5.0	10.0	10.0	15.0	mF
14	5.445	2.722	1.316	1.316	0.908	m Ω

It should be noted that the star point reactor is not implemented in the RMS model.

A.1.2. CONTROL SYSTEM PARAMETERS

A cascaded approach has been considered to realize the control system of the converter, i.e. depicted in Figure A.2 [48]. Each of the converters used in this thesis has the same control structure depicted in Figure A.2. The upper-level controls consist of the islanded and the non-islanded controls. Whereas the lower-level controls consist of circulating current suppression control, modulation, and capacitor balancing algorithm. The upper-level controls are available in both the EMT and RMS models, while the lower-level control are only applicable in the EMT model. Further details of these control levels are given as follows.

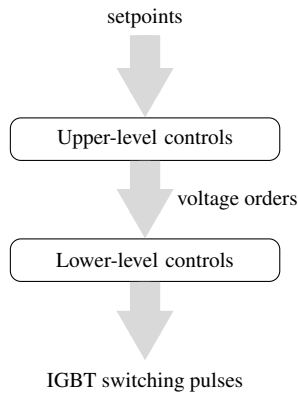


Fig. A.2: The converter control levels [48, 68].

ISLANDED CONTROL

The islanded control is used in e.g. VSC1 of the 4-terminal HVDC system depicted in Figure 5.1 and Cm-E1 of the 9-terminal HVDC system depicted in Figure 5.22. Both of these converters are either connected with an AC system with a very low SCC or a 3-phase load with no generation. Therefore, the main aim of this control is to enable the converter to take an active part in the AC system frequency control. The structure of the islanded control implemented in this thesis is depicted in Figure A.3.

The AC system frequency reference is denoted in Figure A.3 as f_0 (in Hz). This signal is then used to generate the reference angle (θ_{ref}) for the inverse Park transformation, i.e. dq rotating frame to three-phase static frame quantities. The reference angle is generated by the voltage-controlled oscillator (VCO) box, which produces a ramping θ_{ref} value with a rate of change equals to f_0 [124].

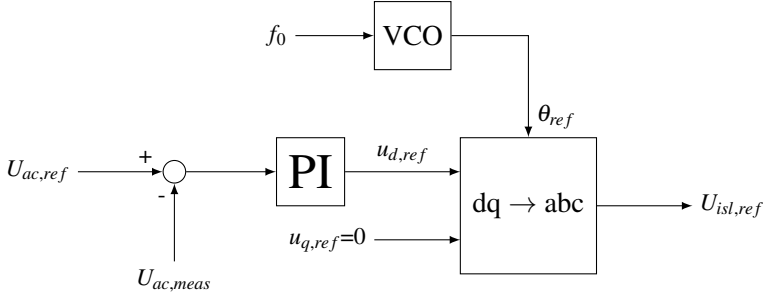


Fig. A.3: The islanded control (*IslCtrl*) structure [48]. The measured and referred AC voltages ($U_{ac,meas}$ and $U_{ac,ref}$) are given in the per unit value. Whereas the frequency reference (f_0) is given in hertz and the output angle reference (θ_{ref}) is given in radians.

As can be seen in Figure A.3, the *IslCtrl* is also enforced with an AC voltage controller. The parameters for this controller is the same as the one used in the RMS control given in Table A.3.

NON-ISLANDED CONTROLS

For the non-islanded operation, the current vector control concept has been adopted. As compared to the *IslCtrl*, the angle reference is generated by a phase-lock loop (PLL), which synchronize the converter with the AC voltage at the PCC. The non-islanded control structure is depicted in Figure 3.3, which has two levels: outer/RMS and inner/current controls.

In general, the control structure for each of the outer controllers is depicted in Figure A.4. It consist of a PI control with the parameters given in Table A.3 for each control modes, i.e. denoted as X . These parameters are retrieved from [48].

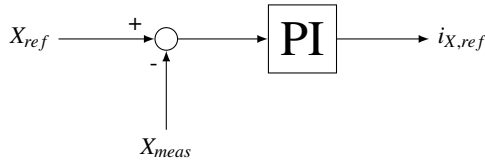


Fig. A.4: The PI controller used in each of the outer controls. The outer control mode is denoted by X . The measured and referred values (X_{meas} and X_{ref}) are given in the per unit value.

The outputs of the outer controllers are the current order ($i_{d,ref}$ and $i_{q,ref}$) as the input for the current controllers. Since the d -axis of the rotating frame is aligned with the AC voltage at the PCC, the value of $i_{pac,ref}$ and $i_{Udc,ref}$ become the alternatives for the $i_{d,ref}$ value. However, on the q -axis side, the *UacCtrl* and *QacCtrl* are cascaded, i.e.

the value of $i_{Uac,ref}$ becomes one of the options for the $Q_{ac}Ctrl$ inputs. So, when the converter is in the $UacCtrl$ mode, the reactive power reference ($Q_{ac,ref}$) equals to the value of $i_{Uac,ref}$.

Table A.3: The PI-control parameters for the RMS controls.

Control mode (X)	Gains	Value
Active power control (P_{ac})	Proportional ($k_{p,Pac}$)	0.0
	Integral ($k_{i,Pac}$)	33.0
DC voltage control (U_{dc})	Proportional ($k_{p,Udc}$)	8.0
	Integral ($k_{i,Udc}$)	272.0
Reactive power control (Q_{ac})	Proportional ($k_{p,Qac}$)	0.0
	Integral ($k_{i,Qac}$)	33.0
AC voltage control (U_{ac})	Proportional ($k_{p,Uac}$)	1.0
	Integral ($k_{i,Uac}$)	10.0

The structure of the inner/current controllers are depicted in Figure A.5. The same PI gains have been used for both d and q axes controls, i.e. $k_{p,d} = 0.48$ and $k_{i,q} = 150$.

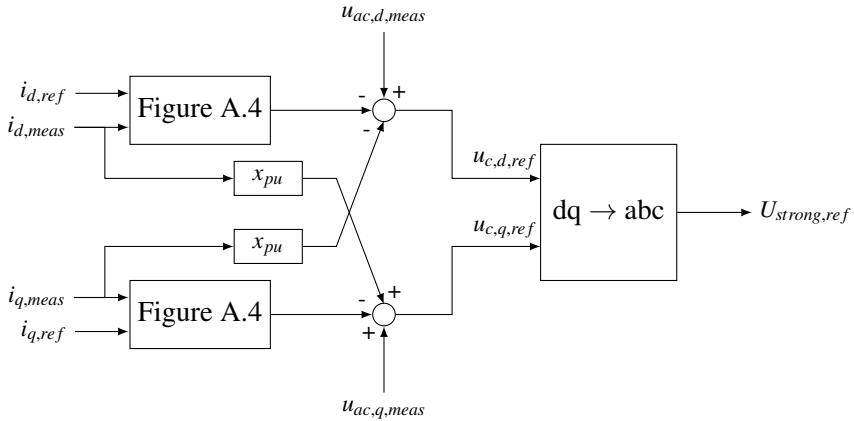


Fig. A.5: The inner/current controls structure. The measured and referred currents and voltages are given in the per unit value. Furthermore, x_{pu} represents the per unit reactance between the valve and the PCC.

LOWER LEVEL CONTROLS

The aim of the lower level controls is to generate the switching pulses for each of the MMC valves. The voltage orders from the upper-level controls are used as the reference for generating these pulses. The lower-level controls hierarchy is depicted in Figure A.6. It should be noted that this control level is only realized in PSCAD software for the EMT simulations.

Appendix A. DC system parameters

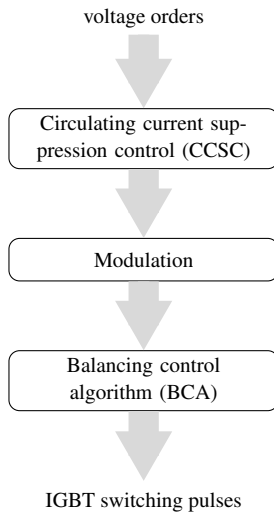


Fig. A.6: The lower-level control hierarchy [48].

The inequality of the arm voltage of the MMC leads to a current flow between each phase unit. This current is known as the circulating current. Although it does not affect the converter's AC- and DC-side current, it will distort the arm current waveform and might increase the rated current through the submodules. The CCSC component in Figure A.6 is used to eliminate this circulating current. A dq -frame CCSC (CCSC $d-q$) method is used in each of the converters used in this thesis [48]. The output of the CCSC is used to modify the reference voltages (a three-phase sinusoidal waveform) from the upper-level controls.

The nearest level control (NLC) is the modulation technique used in the model [105]. With this method, the reference voltages are discretized by the number of the submodules [48]. The output of this method is the number of submodules to be turned on for each arm of the MMC.

The firing of the valves within the submodules is managed by the BCA component in Figure A.6. At first, the capacitor voltages are measured and sorted. Based on these values, the current flow direction, and the order from the NLC, the BCA selects which valve should be turned on or off (insert or bypass), i.e. charging or discharging the capacitor. Hence, the capacitor voltage in each valves can be balanced [123].

A.2. DC LINE PARAMETERS

All the lines in the 4-terminal HVDC system are constructed by underwater DC cables. Whereas for the 9-terminal HVDC system, a mix of DC cables and overhead lines is used. The parameters for the cables and the overhead lines are given as follows:

A.2.1. DC CABLE PARAMETERS

XLPE cable has been considered in this thesis. The cable data are based on a ± 320 kV which has been adapted for ± 200 kV and ± 400 kV [48]. Table A.4 summarized the DC cable data for load flow and RMS simulation, i.e. represented as an equivalent Π -model. While, for EMT simulation, a more detailed representation, implemented as a frequency dependent phase model with their geometry depicted in Figure A.7 and Figure A.8.

Table A.4: The ± 200 kV DC cable data for load flow and RMS simulation.

Data	Value	Unit
Resistance (R_{cable})	0.0110	Ω/km
Inductance (L_{cable})	2.6150	mH/km
Capacitance (C_{cable})	0.2185	$\mu\text{F}/\text{km}$
Conductance (G_{cable})	0.0550	$\mu\text{S}/\text{km}$

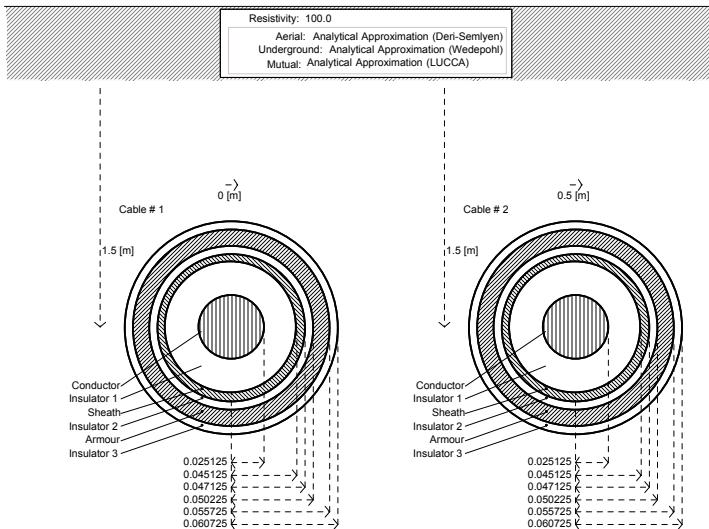


Fig. A.7: The ± 200 kV DC cable structure implemented in PSCAD software.

Appendix A. DC system parameters

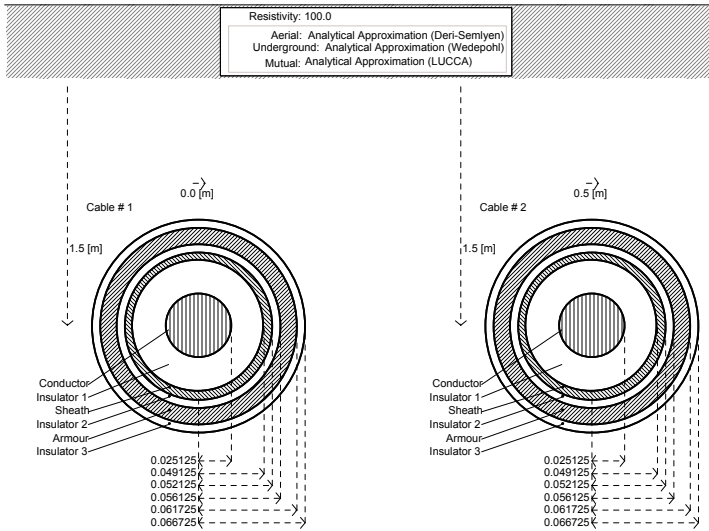


Fig. A.8: The ± 400 kV DC cable structure implemented in PSCAD software.

A.2.2. DC OVERHEAD LINE PARAMETERS

Similar to the DC cable, the DC OHL is represented as a frequency dependent phase model in PSCAD model [48]. The geometry of the DC OHL is depicted in Figure A.9 for ± 200 kV and Figure A.10 for ± 400 kV.

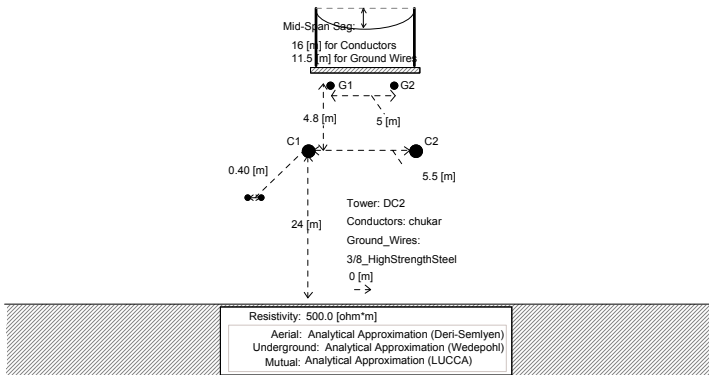


Fig. A.9: The ± 200 kV DC OHL structure implemented in PSCAD software.

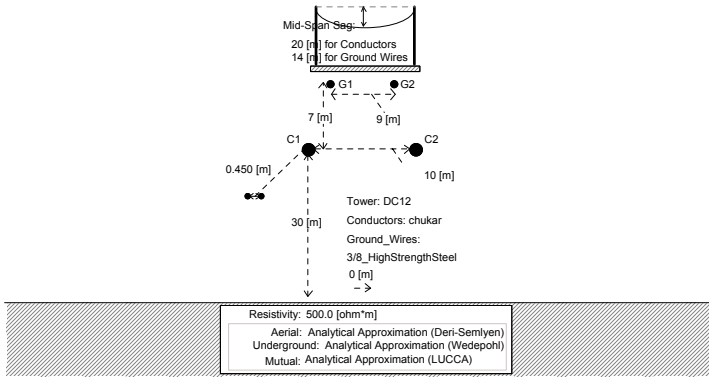


Fig. A.10: The ± 400 kV DC OHL structure implemented in PSCAD software.

A.3. DC/DC CONVERTER

An ideal DC/DC converter is used in the 9-terminal HVDC system depicted in Figure 5.22. This means that this component only transform the DC voltage from one level to another, without any representation of the losses or control. In PSCAD, this component is modeled using a single-phase transformer. The equivalent circuit of this transformer is depicted in Figure A.11. The primary and secondary voltages in Figure A.11 are given as the RMS values (not sinusoidal ones). Hence, when the terminal is used within the MTDC system, the DC voltage value can be transformed into another level.

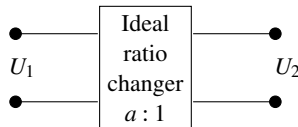


Fig. A.11: The transformer equivalent circuit [124]. In this circuit, the magnetizing current is neglected, and the value of a is given as the turn ratio of the transformer, i.e. the ratio between the primary and secondary voltages (U_1 and U_2).

For the 9-terminal HVDC system depicted in Figure 5.22, there are two DC/DC converters:

1. Cd-B1, which has a ratio of $\pm 400 : \pm 400$.
2. Cd-E1, which has a ratio of $\pm 200 : \pm 400$.

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APPENDIX B. AC SYSTEM PARAMETERS

B.1. THE OFFSHORE AC SYSTEM

In the 4-terminal HVDC system depicted in Figure 5.1, VSC1 is connected to an offshore wind farm system, OWF1. This system is represented as a Norton source equivalent depicted in Figure B.1.

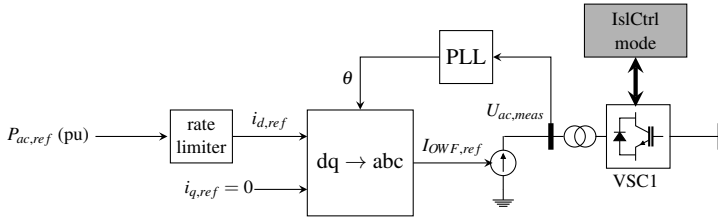


Fig. B.1: The representation of the OWF system used in the 4-terminal HVDC system depicted in Figure 5.1. The user input active power reference is given in the per unit value, i.e. the same base power used by the three-phase current source (800 MW). Therefore, the rate limiter parameter is also given in per unit/second.

There are no representation of the wind turbine generator systems nor the offshore AC collection systems implemented in both PSCAD and PowerFactory softwares. This is because the aim of the OWF system is to ramp up the power injected to the DC grid, i.e. there is no study performed inside the OWF system.

B.2. THE TWO-AREA SYSTEM PARAMETERS

The two-area system used in subsection 5.2.8 is defined in [104] to perform the inter-area oscillations study. Each of the synchronous generators in Figure B.2 is rated at 900 MVA and 20 kV, while each of the transformers in is rated at 900 MVA and 20/230 kV with an impedance of $0.0 + j0.15$ pu. Furthermore, each of the transmission lines is considered as a Π -link with a resistance of $0.0529 \Omega/\text{km}$, an inductance of $1.6839 \text{ mH}/\text{km}$, and a capacitance of $0.0105 \mu\text{F}/\text{km}$.

The power flow result for the system depicted in Figure 5.18 is as follows:

1. G1: $P_{G1} = 700 \text{ MW}$, $Q_{G1} = 160.84 \text{ MVAr}$, $U_{G1} = 1.03 \angle 6.3^\circ$
2. G2: $P_{G2} = 700 \text{ MW}$, $Q_{G2} = 176.39 \text{ MVAr}$, $U_{G2} = 1.01 \angle -3.3^\circ$

Appendix B. AC system parameters

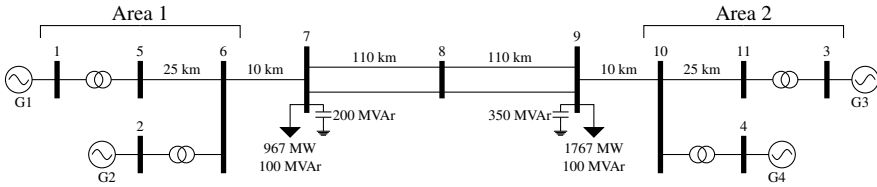


Fig. B.2: Kundur's two-area test system [104].

3. G3: $P_{G3} = 707$ MW, $Q_{G3} = 176.39$ MVA_r, $U_{G3} = 1.03 \angle -6.8^\circ$
4. G4: $P_{G4} = 700$ MW, $Q_{G4} = 112.79$ MVA_r, $U_{G4} = 1.01 \angle -16.6^\circ$

where P , Q , and U are the active power, reactive power, and AC voltage measured at the generator terminal.

B.2.1. SYNCHRONOUS GENERATOR PARAMETERS

The synchronous generator is represented in dq -axis and modeled as a single mass, round rotor type, with no saturation. The parameters for this model is given in Table B.1. Each of the generators in the two-are system depicted in Figure 5.18 is equipped with a governor system, an AC excitation system, and a power system stabilizer (PSS). Further details are given as follows:

Table B.1: Synchronous generator parameters used in the two-area system.

Component	Data	Value	Unit
Generator	Inertia constant (H) for G1 and G2	6.5000	s
	Inertia constant (H) for G3 and G4	6.1750	s
	Stator resistance	0.0025	pu
	Stator reactance	0.2000	pu
	d -axis synchronous reactance	1.8000	pu
	q -axis synchronous reactance	1.7000	pu
	d -axis transient reactance	0.3000	pu
	q -axis transient reactance	0.5500	pu
	d -axis transient time constant	8.0000	s
	q -axis transient time constant	0.4000	s
	d -axis subtransient reactance	0.2500	pu
	q -axis subtransient reactance	0.2500	pu
	d -axis subtransient time constant	0.0300	s
	q -axis subtransient time constant	0.0500	s

SPEED GOVERNOR MODEL

The governor model used in this thesis is based on the IEEE Type 1 speed-governing (IEEEG1) model, which consists of the generic governor (GOV1) and turbine (TUR1) models [124, 125]. The simplified transfer functions are depicted in Figure B.3 and Figure B.4, i.e. the blocks with zero gain have been disregarded [104, 126].

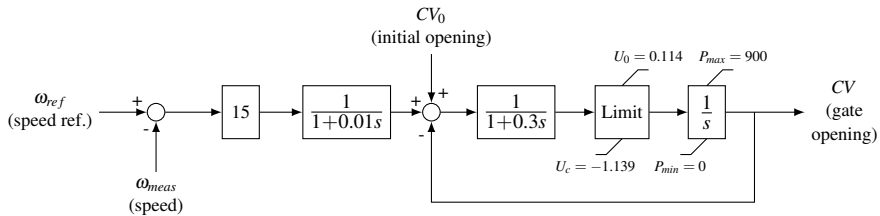


Fig. B.3: The transfer function of the approximate mechanical-hydraulic control model [126].

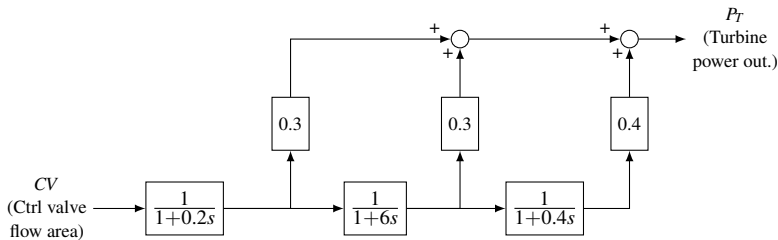


Fig. B.4: The transfer function of the generic turbine model used [126].

EXCITATION SYSTEM MODEL

The excitation system model used in this thesis is based on the 1981 IEEE Type AC4 excitation system (EXAC4) model [127]. The simplified transfer function of this model is depicted in Figure B.5 [104].

The input of the exciter model is the measured AC voltage at the terminal of the generator (in per unit). Apart from the voltage setpoint, this model also receive the voltage reference generated by the PSS (U_{PSS}), described later. The output field voltage reference from this model becomes one of input for the synchronous generator model.

POWER SYSTEM STABILIZER MODEL

The power system stabilizer (PSS) model used in this thesis is based on the speed sensitive stabilizing (STAB1) model [124]. The simplified transfer function of this

Appendix B. AC system parameters

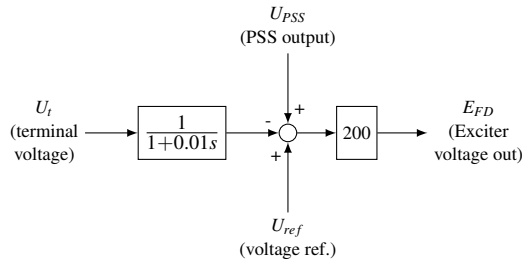


Fig. B.5: The transfer function of the exciter model [104].

model is depicted in Figure B.6 [104].

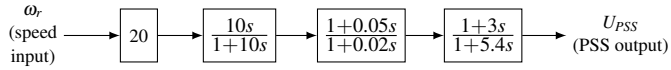


Fig. B.6: The transfer function of the PSS model [104].

Depending on the rotor speed of the generator, the PSS model generates the voltage input for the exciter, such that the damping of power system oscillations through the exciter is enhanced. The washout filter is used to reject the steady-state input, while passing the transient input, i.e. makes the PSS sensitive to a speed change. The phase compensation system is represented by the two lead-lag filters in Figure B.6 [104].

APPENDIX C. MODELING OF HB-MMC FOR TRANSIENT STABILITY STUDIES

C.1. ELECTRICAL REPRESENTATION

To analyze the slow dynamic interaction (study period of few seconds until several minutes) between the converter and the AC grids where this converter is connected, the converter is usually simplified and represented similarly to a two-level VSC-HVDC converter [48, 68, 128, 129]. Furthermore, the power electronic switches can be neglected by assuming that sinusoidal voltage can be synthesized at the converter AC-side terminal, e.g. explained in [48, 128–132] among others. Therefore, the converter depicted in Figure A.1 can be represented as a voltage-controlled source in the AC-side while the DC-side can be seen as current-controlled source conserving active power balance between AC and DC sides, i.e. depicted in Figure C.1.

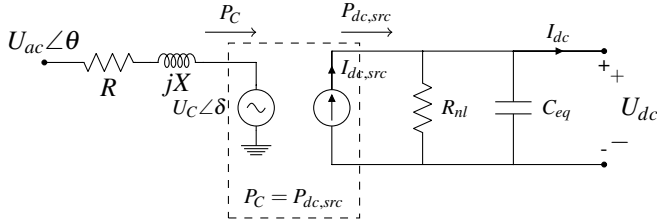


Fig. C.1: The equivalent circuit of an HVDC converter in RMS program [68].

The equivalent circuit depicted in Figure C.1 relies on the assumption that the voltage on all SM capacitors is always a balance, i.e. the circulating current equals to zero. Therefore, a virtual voltage $\overline{U_C}$ can be formulated in (C.1) [68, 128]:

$$\overline{U_C} = \frac{\overline{U_{lo}} - \overline{U_{up}}}{2} \quad (C.1)$$

where $\overline{U_{up}}$ and $\overline{U_{lo}}$ are the upper and lower arm voltages respectively. Furthermore, the voltage drop between the point of common coupling (PCC) and this virtual voltage is given in (C.2) as [68, 128]:

$$\overline{U_C} = \overline{U_{ac}} - \overline{I_v} \left(R_{xfr} + \frac{R_{arm}}{2} \right) - j \overline{I_v} \left(X_{xfr} + \frac{X_{arm}}{2} \right) \quad (C.2)$$

where the overlines represent phasor quantities. R_{xfr} and X_{xfr} are the converter transformer's resistance and leakage reactance, while R_{arm} and X_{arm} are the arm resistance

and reactance values. In Figure C.1, the arm and transformer impedances are lumped as R and X values. Hence, the current flowing across these impedances is denoted as I_v .

The coupling between the AC and DC side of the converter is done by conserving the active power balance between these two sides ($P_C = P_{dc,src}$). Hence, the DC current source, $I_{dc,src}$, can be formulated in (C.3):

$$I_{dc,src} = \frac{\text{Re}(\overline{U_C I_v^*})}{U_{dc}} \quad (\text{C.3})$$

The voltage $\overline{U_C}$ is limited by the DC voltage value such that the modulation index magnitude m is less than 1, i.e. formulated in (C.4)

$$\overline{m} = \frac{2\sqrt{2} \overline{U_C}}{\sqrt{3} U_{dc}} \quad (\text{C.4})$$

Furthermore, a parallel DC resistance R_{nl} is added in Figure C.1 to represent the no-load losses of the converter, while the capacitance C_{eq} corresponds to the equivalent capacitance of the SMs capacitance and can be derived in (C.5) [48]:

$$C_{eq} = \frac{6C_{SM}}{n_a} \quad (\text{C.5})$$

where C_{SM} is the SM capacitance and n_a is the number of submodules per converter arm depicted in Figure A.1. When the converter is blocked, e.g. during AC or DC fault conditions, the high magnitude current flow is bypassed through the freewheeling diode or thyristor to avoid destruction of the IGBTs. Therefore, the HVDC converter can be represented as a three-phase diode bridge. As compared to two-level technology, the energy stored in each SM capacitor is not discharged to the faulty point, hence less fault inrush current and faster system recovery in DC faults transient when HB-MMC is used [24]. In RMS model, this condition can be modeled by disconnecting C_{eq} in Figure C.1.

C.2. CONTROL REPRESENTATION

The most common implementation of the HVDC controls is by employing a cascaded control structure, i.e. usually consisted of higher- and lower-level controls [48]. The lower-level controls, i.e. also referred as the MMC controls, are responsible for generating firing pulses for the power electronics. However, since power electronics are not considered in the RMS model (represented as a controlled-voltage source), the lower-level controllers can be ignored.

The output of the upper-level controls is the converter voltage order $\overline{U_{Cref}}$. The magnitude and angle of this voltage determine the AC current injected (or absorbed) by the converter. It is common to represent the AC voltage and current using their equivalent reference frame that rotates synchronously with $\overline{U_{ac}}$. Rewriting Equation C.2 in the d - q synchronous reference frame and separating real and imaginary part result in two equations:

$$\begin{aligned} U_{C,d} &= U_{ac,d} - I_{v,d}R + I_{v,q}X \\ U_{C,q} &= U_{ac,q} - I_{v,q}R - I_{v,d}X \end{aligned} \quad (C.6)$$

The d -axis reference frame is aligned with the AC voltage, i.e. the AC voltage in q -axis equals to zero. By considering this, the d -axis current order, I_{vref}^d , can be produced by either *PacCtrl* or *UdcCtrl*, while the q -axis current order, I_{vref}^q , is produced by either the reactive power (Q_{ac}) or AC voltage (U_L) controller.

The same higher-level controls structures and parameters can be used for both EMT and RMS models. However, as mentioned in [68], the inner or current controller can be simplified since the time response of this control falls below the simulation time step, i.e. a quarter or half a cycle of the nominal AC frequency. The converter voltage order, $\overline{U_{Cref}}$, can then be calculated by directly replacing the measured current, I_v with the reference current from the outer control in Equation C.6.

Furthermore, the IFC is implemented as another converter layer above the high-level controls. Therefore, the IFC can be implemented as same as the one in PSCAD. Appendix D discuss in more details regarding the implementation of the IFC.

C.3. VERIFICATION OF RMS MODEL

The same test system depicted in Figure E.1 has been implemented in DiGSILENT PowerFactory software. The simulation time step used is 1 ms, therefore the same higher-level controls as implemented in PSCAD can be used. The DC voltage step response (with the IFC unit) results are depicted in Figure C.2 More cases, including the comparison without the inner or current control, are given in [68].

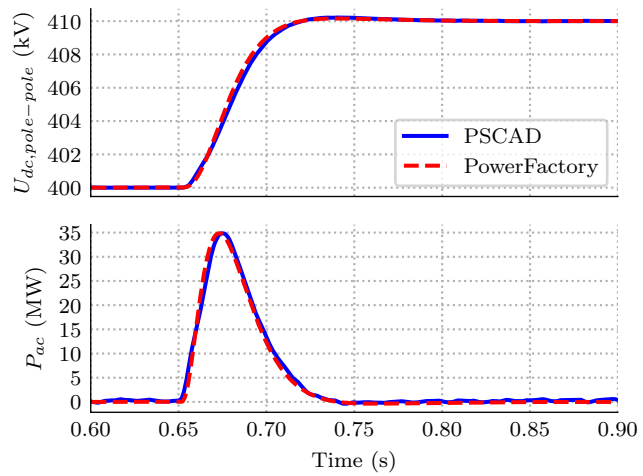


Fig. C.2: DC voltage step response comparison between PSCAD and PowerFactory model when the DLT method is activated.

APPENDIX D. IFC IMPLEMENTATION IN SIMULATION TOOLS

D.1. MODULAR APPROACH

The IFC has been developed by considering a modular design. For simulation purposes, the same consideration holds, i.e. the IFC has been implemented as a Python script, which is then called by each converter in the system that is involved in DC network regulation (operated in *UdcCtrl*). Furthermore, since the proposed method has higher time response as compared to the existing converter control, the same script can be used for both electromagnetic transient (EMT) and transient stability (RMS) simulations.

To simplify the development processes, i.e. one code fits both EMT and RMS programs, this script is then embedded into a dynamic-link library (DLL) file, which is used by PSCAD and PowerFactory when running the dynamic simulation. This approach is depicted in Figure D.1 and was inspired by "common component" concept used in [133].

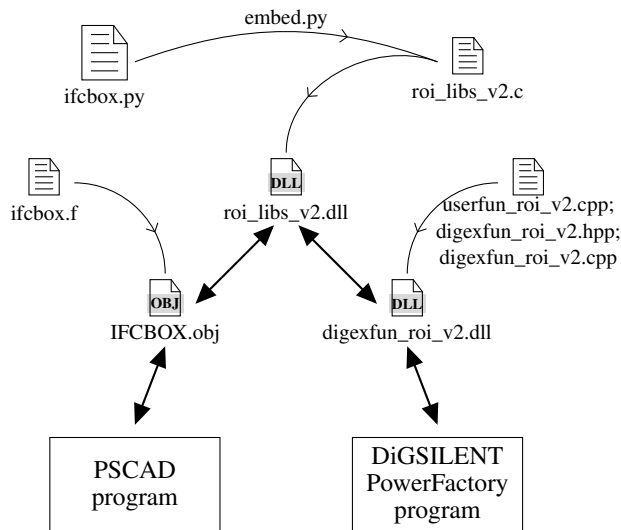


Fig. D.1: The implementation of the IFC in power system simulation software. The curved lines represent source code conversion or compilation process, while the thicker lines represent the interaction between simulation programs with the library.

In Figure D.1, the IFC explained in chapter 4 is implemented as a python code, `ifcbox.py`. The main function of this python code is called `callifcbox()` function. The C Foreign Function Interface for Python (CFFI) package is used for converting this Python into C code, by running `embed.py` code, which results in `roi_libs_v2.c` [134]. This C-code is then compiled using Microsoft C/C++ compiler version 18 to get `roi_libs_v2.dll`. It should be noted that the compiler options need to be adjusted depending on the target engine (a 32- or 64-bit machine).

The interface codes between `roi_libs_v2.dll` and both PSCAD and PowerFactory software are used for passing input/output and allocating storage needed by the IFC (measurement and lead-lag filters states). Fortran language is used for coding the PSCAD interface, while C++ is used for coding PowerFactory interface.

In PSCAD, a user-defined component is used to call the `IFCBOX()` inside the interface code, which is called `roi_libs_v2.dll`. Figure D.2 depicts the representation of IFC unit in PSCAD.

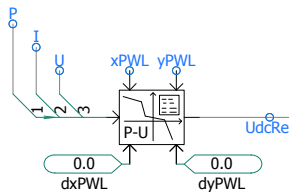


Fig. D.2: The IFC unit representation in PSCAD software.

On the other hand, as depicted in Figure D.1, there are two codes required to build the PowerFactory interface, i.e. `userfun_XXX.cpp` and `digexfun_XXX.cpp`. The user-defined functions are implemented in `userfun_roi_v2.cpp` code, whereas the other two codes are used to load these functions into the PowerFactory engine when it is started. These codes along with the header file for the `digexfun` code are then compiled and the resulting `digexfun_roi_v2.dll` is called by using a DiGSILENT Simulation Language (DSL) component inside PowerFactory. This DSL model is then placed inside a controller frame, i.e. shown in Figure D.3, and used along with the converter control system.

D.2. LEAD-LAG FILTER REPRESENTATION

The IFC structure depicted in Figure 3.16 is realized within the `ifcbox.py`. The historical values from the previous time step are not required by both the DLT method and the droop shift components inside the IFC. However, the phase compensator uses a lead-lag filter $\left(\frac{1+sT_1}{1+sT_2}\right)$, which requires the previous time step values to be stored. The implementation of this filter is based on the trapezoidal rule, i.e. formulated in

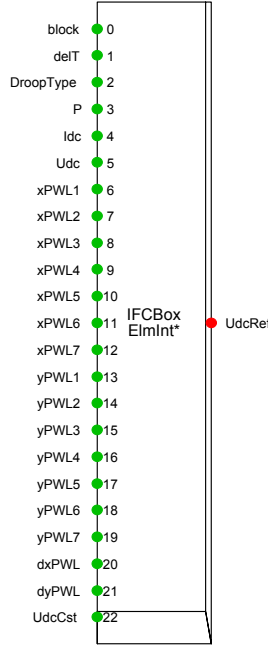


Fig. D.3: The IFC slot representation in PowerFactory software, i.e. represents the input (left) and output (right) signals required and provided by the IFC. The output is then connected with the converter control model's input.

(D.1) [124]:

$$Y(t) = Y(t - \Delta t)e^{-\frac{\Delta t}{T_2}} + X(t) \left(1 - e^{-\frac{\Delta t}{T_2}} \right) + \frac{T_1}{T_2} (X(t) - X(t - \Delta t)) e^{-\frac{\Delta t}{T_2}} \quad (D.1)$$

where $X(t)$ is the actual input signal, $Y(t)$ is the actual output signal, Δt is the simulation time step (in seconds). The time constants of the filter is given as T_1 and T_2 , i.e. the lead and lag time constants (in seconds), respectively. The parameters with $(t - \Delta t)$ represent the stored values from the previous time step.

In order to avoid division by zero in (D.1), i.e. when $T_2 = 0$, the formulation in (D.2) is used instead [124]:

$$Y(t) = X(t) + \frac{T_1}{\Delta t} (X(t) - X(t - \Delta t)) \quad (D.2)$$

Furthermore, as mentioned in Subsection 4.2.6, a lag or low-pass filter is used to condition the inputs of the IFC. This low-pass filter can be achieved using the lead-lag filter formulated in (D.1) by giving $T_1 = 0$. It should be noted that the plotted converter's signals in this thesis have been filtered using this low-pass filter with a time constant of 0.02 s (1-cycle of the AC frequency).

The source code representing (D.1) and (D.2) is given as follows:

```

1  """
2  LeadLagFilt.py
3
4  @author: Roni Irnawan (Aalborg University)
5  """
6
7  import numpy as np
8
9  def LeadLagFilt(IN, DELT, T1, T2, Y_OLD, IN_OLD):
10     """
11     Lead-lag filter implementation. This function is based on the
12     equation given in PSCAD user's manual.
13     IN is the input signal.
14     DELT is the simulation time step.
15     T1 and T2 are the lead and lag time constants, respectively.
16     Y_OLD and IN_OLD are the saved states from the previous time step.
17
18     @author: Roni Irnawan (Aalborg University)
19     """
20
21     # Refer to PSCAD's help
22     if (T2>0.0):
23         OUT = Y_OLD * np.exp(-DELT/T2) + IN * (1-np.exp(-DELT/T2)) +
24             (T1/T2) * (IN-IN_OLD) * np.exp(-DELT/T2)
25     else:
26         OUT = IN + (T1/DELT) * (IN-IN_OLD)
27
28     Y_OLD = OUT
29     IN_OLD = IN
30
31     return OUT, Y_OLD, IN_OLD

```

APPENDIX E. THE SIMPLIFIED TEST SYSTEMS

The behavior of the MTDC system following a disturbance will depend on the configuration of the system and the control modes being applied in each converter within the system [25]. Furthermore, each non-islanded converter in the MTDC system is expected to operate autonomously, i.e. there is no direct communication between each of these converters. Each of the non-islanded converters within the MTDC system will follow their predefined characteristic, which is given by the coordinated MTDC control. This means that the behavior of the MTDC system is a projection of each individual converter within the system.

Therefore, to study the use of the new DC grid control layer explained in Chapter 4, simplified test systems, which only involve one converter, are considered. This way, the converter can be isolated from other non-linearities originated from either other converters or the DC network. Hence, the converter is operated with an ideal systems. The simplified test systems used in Chapter 4 can be divided into the following sections. It should be noted that for this section, the simulation is performed in PSCAD software with a simulation time step of $50 \mu\text{s}$.

E.1. DC VOLTAGE CONTROL TEST

For the purpose of testing the *UdcCtrl* of the converter, an open-end-DC converter is used, i.e. depicted in Figure E.1. The converter rating used is an 800 MW and ± 200 kV symmetric-monopole converter connected to an AC Thévenin equivalent source with short-circuit capacity (SCC) of 30 GVA. The converter parameters are given in Section A.1.

The *UdcCtrl* is used to control the DC voltage measured at the DC terminal. In principle, the DC voltage is controlled by changing the current flow through the converter to charge or discharge the converter capacitor (explained in Subsection 4.3.1). Therefore, the gains of the *UdcCtrl* depend on this capacitor value [135]. By using the test system depicted in Figure E.1, a step input in the DC voltage reference can measure the time behavior of the *UdcCtrl*. The DC-side is open, which means that the DC current is always zero. Hence, the DC step response only reflects the behavior of the *UdcCtrl*, i.e. the impact from the DC system (DC cables and other converters) is neglected.

In reality, this configuration represents the condition when the converter is operated

in STATCOM mode, i.e. no active power transfer through the converter. Another realization of this configuration is during the start-up of the MTDC system, where the converter in Figure E.1 is the first converter to be deblocked in the system.

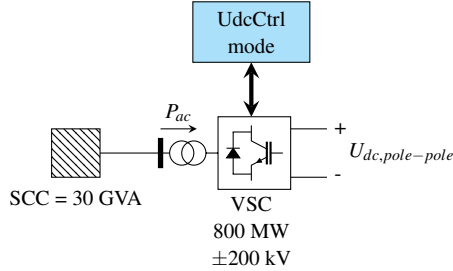


Fig. E.1: The test system for testing the *UdcCtrl* mode. The converter data is given in Section A.1.

In PSCAD, the test system needs 0.6 s to start-up. After this, the DC voltage of the converter is increased from ± 200 kV to ± 205 kV at 0.65 s. The behavior of the DC voltage, which reflects the gains used by the *UdcCtrl* mode, is depicted in Figure E.2. Furthermore, the active power spike represents the amount of energy used to charge the converter capacitor in order to achieve the new DC voltage level.

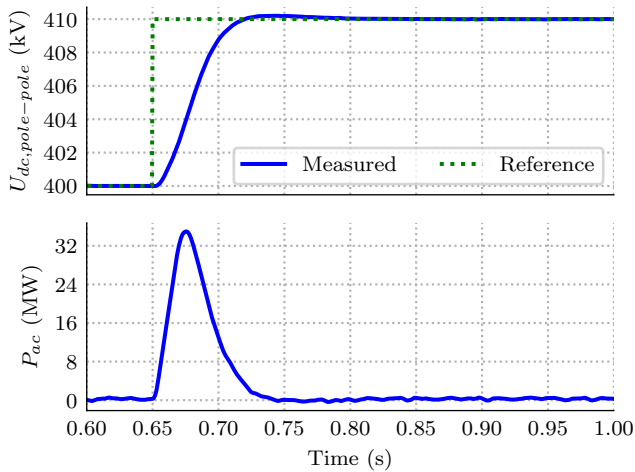


Fig. E.2: DC voltage step response results using the simplified test system depicted in Figure E.1.

E.1.1. INFLUENCE OF ADDITIONAL DC CAPACITANCES

Since the *UdcCtrl* is usually tuned by considering the converter capacitance, adding more capacitances into the DC-side of the converter (e.g.: connection of DC cables

and deblocking additional converters) might influence the behavior of the *UdcCtrl*, i.e. explained in Subsection 4.3.1.

In order to show this behavior, the 4-terminal HVDC system depicted in Figure E.3 is considered. All the converters in this MTDC system have the same rating as the converter depicted in Figure E.1.

It is assumed that Figure E.1 represents the condition when this MTDC system is started by only deblocking VSC2 (configuration 1), which is in *UdcCtrl* mode. The next step is to connect the DC cables and the rest of the converters of the MTDC system with VSC2 (configuration 2). During this condition, VSC1, VSC3, and VSC4 are still blocked. Configuration 3, 4, and 5 are the condition when VSC1, VSC3, and VSC4 are deblocked one after another. Furthermore, the non-islanded converters (VSC3 and VSC4) are operated in *PacCtrl* mode with 0 MW reference. This is because the aim is to measure the behavior of *UdcCtrl* in VSC2,

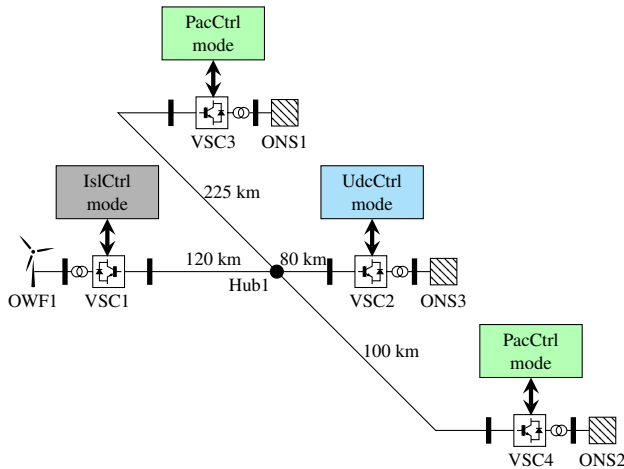


Fig. E.3: The 4-terminal HVDC test system.

For every configuration, the DC voltage reference of VSC2 is increased from ± 200 kV to ± 205 kV. However, each of these configurations take different duration in order to reach steady-state. Therefore, the DC voltage reference step is performed at 0.05 s after each configuration reaches steady-state. The simulation results are depicted in Figure E.4. It should be noted that the time scale for each configuration has been shifted to zero such that they can be overlaid together.

As can be seen in Figure E.4, the higher the DC capacitance (by adding the DC cables and deblocking the converters), the response of the *UdcCtrl* becomes slower. However, the connection of the DC cables and the blocked converters (configuration 2) give a lower impact in the DC voltage step response of VSC2 as compared to the

Appendix E. The simplified test systems

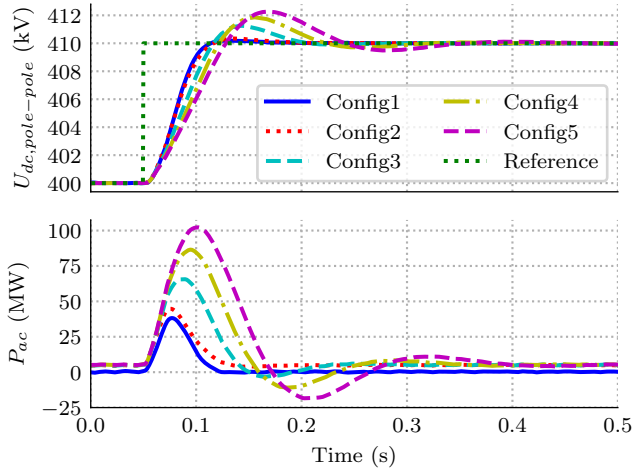


Fig. E.4: DC voltage step response results using the simplified test system depicted in Figure E.1.

deblocking of the converter. This is because the total length of the DC cables are 525 km, which results in approximately $114.7 \mu\text{F}$ of DC cables capacitance, while the equivalent converter capacitance in Figure E.4 equals to $300 \mu\text{F}$.

A simplified test system can then be formed by adding DC capacitors in a single converter system, i.e. depicted in Figure E.5. The capacitance value of these capacitors equal to the total DC capacitance of the different MTDC system configurations. Furthermore, since the capacitance of the converter is more dominant than the DC cables, the capacitors in Figure E.5 reflect the total equivalent converter capacitance for each deblocked additional converters, e.g. 0.3, 0.6, and 0.9 mF for configuration 3, 4, and 5 of the 4-terminal HVDC system depicted in Figure E.3, respectively. The DC voltage step behavior of the simplified test system as compared to the detailed representation of the 4-terminal HVDC system for configuration 1, 3, 4, and 5 are depicted in Figure E.6.

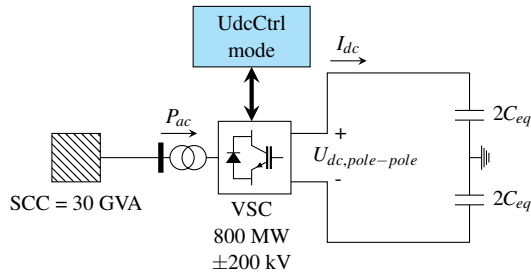


Fig. E.5: The test system for testing the *UdcCtrl* mode.

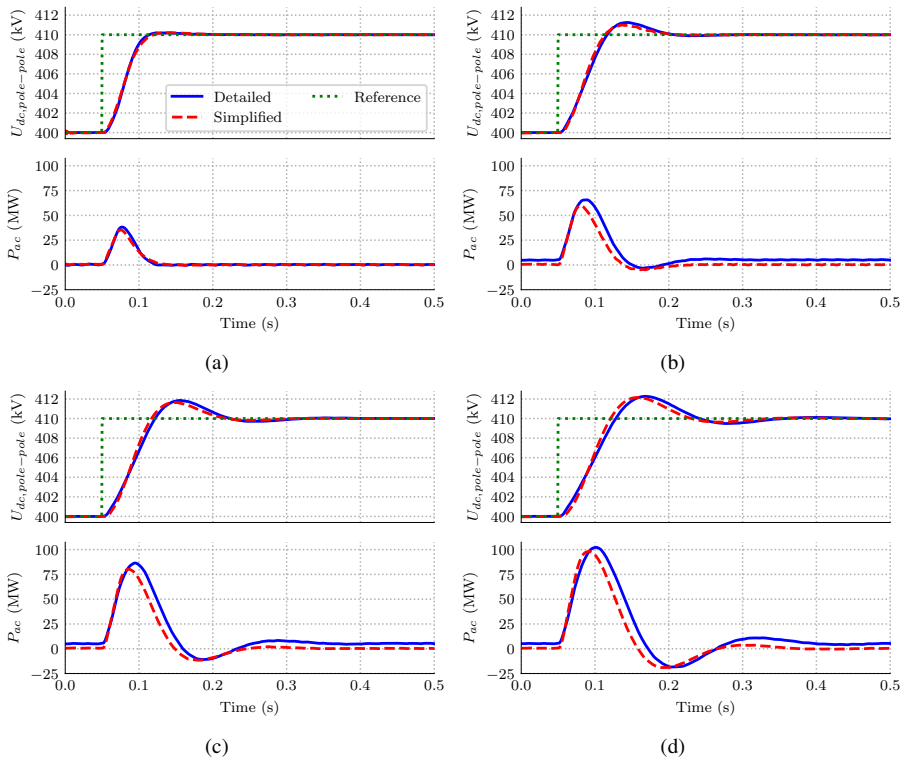


Fig. E.6: Comparison between the DC voltage step response performed using the detailed 4-terminal HVDC (blue) and simplified (red) test system for: (a) configuration 1, (b) configuration 3, (c) configuration 4, and (d) configuration 5. The DC voltage and active power power are measured at VSC2's terminal for the detailed test system.

As can be seen in Figure E.6, the simplified test system depicted in Figure E.5 can be used to represent the $UdcCtrl$ behavior for different MTDC configurations. The rise time, settling time, and overshoot magnitude of the DC voltage waveforms are the same for both using the simplified and detailed test system. However, active power waveform is not really match (especially in Figure E.6(b)–Figure E.6(d)) because the system losses is not considered in the simplified test system.

E.2. ACTIVE POWER CONTROL TEST

In order to test the $PacCtrl$ behavior, the single converter test system is connected with a DC voltage source, i.e. depicted in Figure E.7. This DC voltage source act as the slack bus of the DC system. This means that the requested power from the converter can be supplied by the DC voltage source. Hence, the converter is used to connect the

infinite DC bus with the 30 GVA AC system (can be categorized as a very strong AC system [24]).

The *PacCtrl* generates the active current reference (d -axis current, explained in Subsection 3.2.2) for the current controller. Since the DC terminal of the converter is connected with a constant DC voltage source, the energy storage effect in the converter capacitance can be neglected. Hence, the AC–DC active power transfer is not used for charging or discharging the converter capacitance. This means that the simplified test system depicted in Figure E.7 can be used to show how fast the current reference for the inner control is generated by the *PacCtrl*.

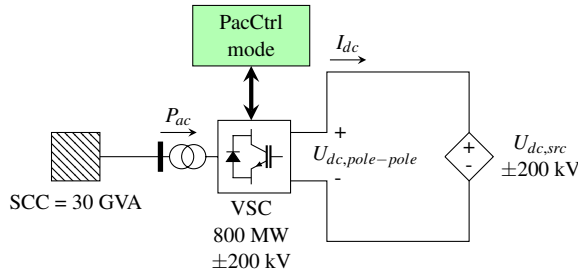


Fig. E.7: The test system for P_{ac} step response test.

In order to show the behavior of *PacCtrl* response, a 300 MW active power step-up is performed using the test system depicted in Figure E.7. As a comparison, the same active power step is performed in VSC4 of the 4-terminal HVDC system depicted in Figure E.3. The results are depicted in Figure E.8.

As can be seen in Figure E.8, the behavior of the *PacCtrl* control are the same regardless to which system this converter is connected. This means that the simplified test system depicted in Figure E.7 can be used to test the behavior of the *PacCtrl*. However, with the MTDC system, the DC voltage has a new steady-state value after the step, due to the changes in the load flow pattern within the system. The DC voltage overshoot is due to the response of the *UdcCtrl* used in VSC2.

E.3. DC VOLTAGE DROOP CONTROL TEST

The intentional use of the previous simplified test systems is to measure a step response of only the *UdcCtrl* or *PacCtrl* modes, while *DroopCtrl* mode could not be tested using these test systems. This is because in order for the *DroopCtrl* mode to work, the deviation in both active power and DC voltage are needed.

In order to demonstrate this condition, the 4-terminal HVDC system with the control mode setting and the steady-state power flow condition as depicted in Figure E.9 is

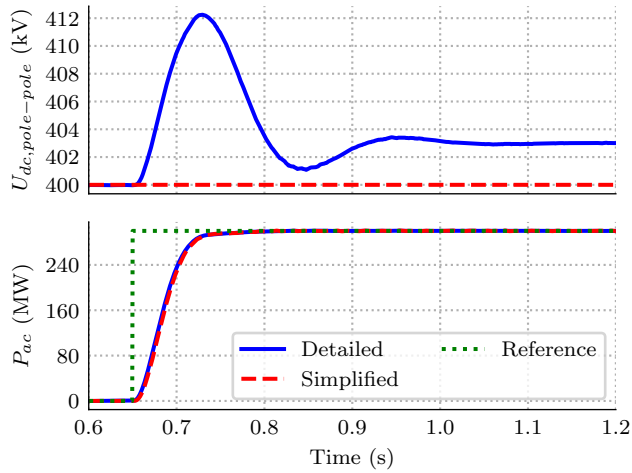


Fig. E.8: Comparison of active power step response performed using the 4-terminal HVDC system (blue) and the simplified test system depicted in Figure E.1 (red). The DC voltage and active power power are measured at VSC4's terminal for the detailed test system.

considered. The droop control in VSC3 has the droop constant of 0.005 kV/MW with the DC voltage and active power origins of 397.96 kV and 0 MW, respectively. While VSC4 in Figure E.9 is the converter of interest, i.e. the same converter as in Figure E.11, with the droop settings of 0.1 kV/MW, 400 kV, and 0 MW. It should be noted that the *DroopCtrl* used in Figure E.9 is implemented as an extension of the *UdcCtrl*, i.e. explained in Subsection 4.2.1.

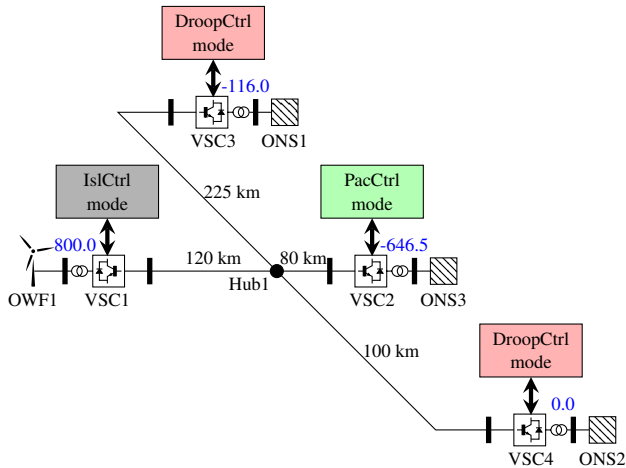


Fig. E.9: The 4-terminal HVDC test system.

When the active power origin for VSC4 is changed to 300 MW, the power flow pattern in the MTDC system is changed. Figure E.10 depicts the behavior of this *DroopCtrl* step. In order to simplify the test system, series resistors are connected between the converter and the DC voltage source in Figure E.7, i.e. depicted in Figure E.11. The resistors in Figure E.11 are calculated using (2.1) and (2.2) such that the converter has the same steady-state operating point. The *DroopCtrl* step using the simplified test system is also depicted in Figure E.10.

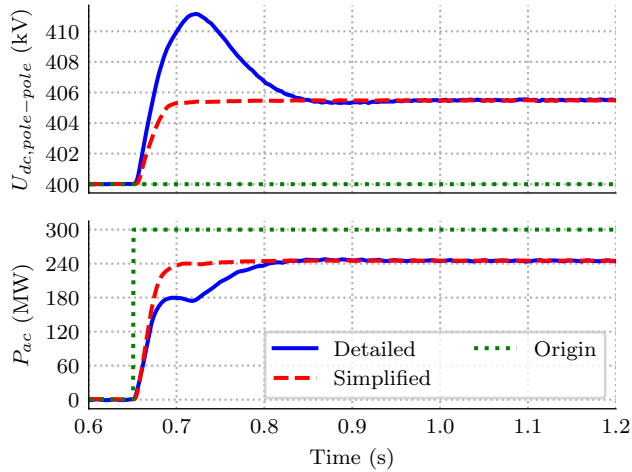


Fig. E.10: Comparison of DC voltage droop step response performed using the 4-terminal HVDC system (blue) and the simplified test system depicted in Figure E.11 (red). The DC voltage and active power power are measured at VSC4’s terminal for the detailed test system.

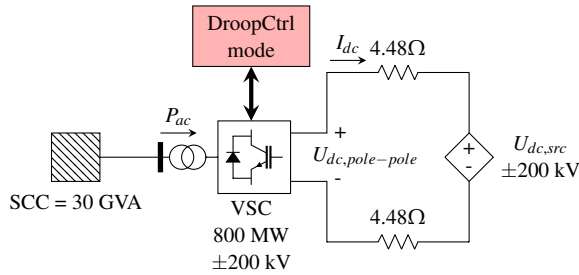


Fig. E.11: The test system for DC voltage droop step response test.

As can be seen from the results in Figure E.10, the time response of the one with the simplified test system is faster. This is because the DC capacitance effect is neglected in the simplified test system. As shown in Figure E.5, the *UdcCtrl* mode becomes slower when more converters are deblocked. This produces the DC voltage overshoot in Figure E.5.

APPENDIX F. THE POWER-BASED DC VOLTAGE DROOP CONTROL

As an alternative of the U_{dc} -based DC voltage droop control method, explained in Subsection 4.2.1, the *DroopCtrl* can be implemented as the extension of the existing *PacCtrl*. This way, the active power reference for the existing *PacCtrl* is manipulated by measuring the deviation in DC voltage such that the converter stays along the droop curve following a disturbance.

Figure F.1 illustrates the generation of the new active power reference ($P_{ac,ref}$), when the operating point of the converter (*meas*) is off the droop lines. For a droop curve with the slope angle of θ'' , the coordinates of the new reference point (point *B*) can be determined using (F.1), i.e. the x -axis coordinate is derived from (3.2).

$$\begin{aligned} x_B &= P_{ac,0} - \Delta U_{dc} \tan\left(\frac{\pi}{2} - \theta\right), 0 < \theta < \frac{\pi}{2} \\ y_B &= U_{dc,meas} \end{aligned} \quad (F.1)$$

where ΔU_{dc} is the deviation in DC voltage ($U_{dc,meas} - U_{dc,0}$).

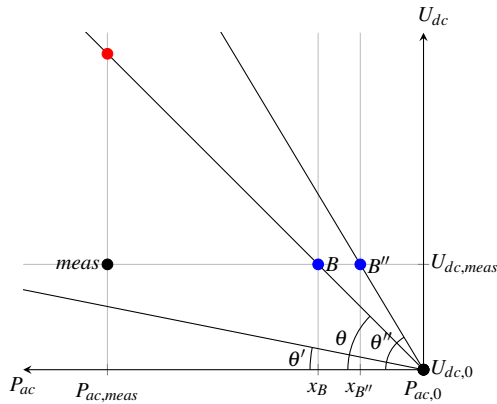


Fig. F.1: Illustration of the P_{ac} -based *DroopCtrl* method in P_{ac} - U_{dc} plane. The blue dots represent the new reference points.

When a higher droop constant is considered, i.e. the droop slope equals to θ'' in Figure F.1, the new reference for the existing *PacCtrl* is denoted as point *B''*. The coordinated of this point can be calculated using (F.1) by using the angle θ'' . Since $\theta < \theta''$, the deviation in the active power reference or origin, $P_{ac,0}$, is lower for θ'' although ΔU_{dc} is the same. Hence, point *B''* is closer to $P_{ac,0}$.

On the other hand, when a lower droop constant value is used, i.e. the droop slope equals to θ' in Figure F.1, the new active power reference for the existing *PacCtrl* lies outside the drawing plane, i.e. to the left of point *B*. This is because the value of $\tan(\frac{\pi}{2} - \theta')$ in (F.1) makes a higher active power reference deviation from the origin for the same ΔU_{dc} value.

This means that as the droop constant is reduced, the existing *PacCtrl* is expected to allow higher deviation from its origin, $P_{ac,0}$. This is similar to the U_{dc} -based droop control approach explained in Subsection 4.2.1. A droop curve step is also performed using the test system depicted in Figure F.2 to assess the performance of the P_{ac} -based droop control approach. The only difference between this test system with the one depicted in Figure 4.2 is the converter control mode. The simulation results when the active power origin is changed from 0 to 300 MW are shown in Figure F.3.

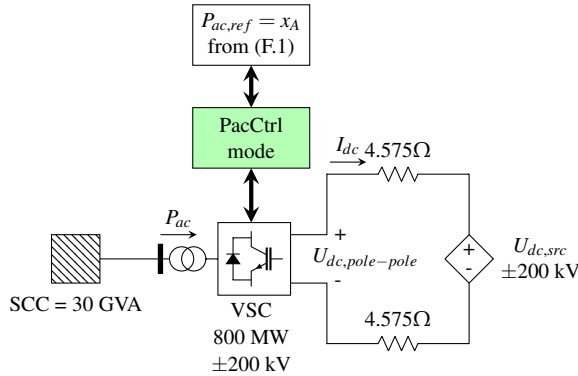


Fig. F.2: The test system for droop step response test.

The results are similar to the U_{dc} -based approach, except that the oscillations occur for the U_{dc} -based *DroopCtrl* method when the value of k_{droop} is reduced. The reason for the oscillations, e.g. shown in Figure F.3(a)–Figure F.3(c), is because the conventional *DroopCtrl* is not able to recognize the position of the operating point from the droop curve. As shown in Figure F.4, the new active power reference is higher as compared to the measured one when the operating point is on the left of the droop curve. As soon as the operating point passes the droop curve, the new active power reference is lower than the measured one. For a very low k_{droop} , e.g. 0.0025 kV/MW, the system becomes unstable because the new active power is oscillating between two points on the left and right sides of the droop curve.

Therefore, the P_{ac} -based *DroopCtrl* method could not be used to represent the *UdcCtrl* mode, i.e. a straight horizontal droop slope as depicted in Figure 3.5. Furthermore, there are some regions between the droop curve and the x -axis of the P_{ac} – U_{dc} plane in which this mode could not be operated.

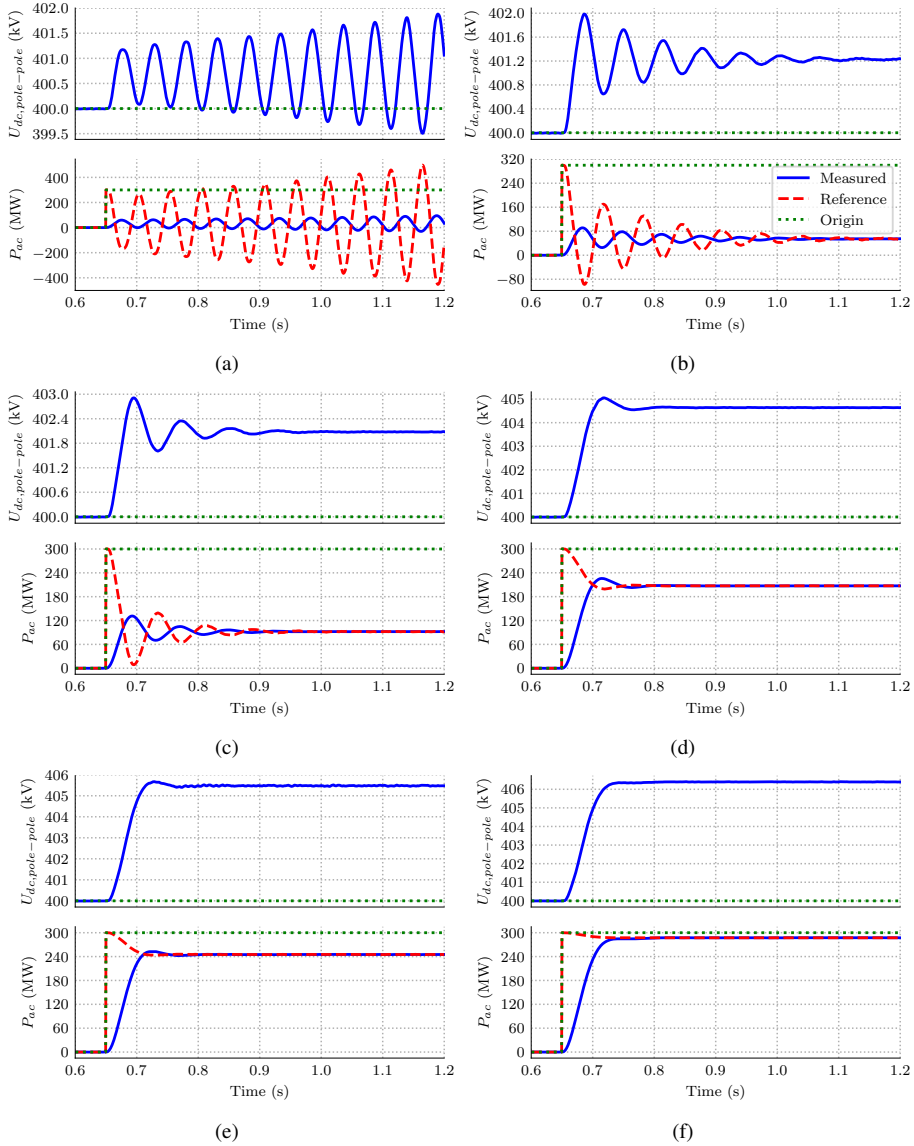


Fig. F.3: The conventional P_{ac} -based *DroopCtrl* step test results for the droop constant of : (a) 0.0025, (b) 0.005, (c) 0.01 kV/MW, (d) 0.05, (e) 0.1 and (f) 0.5 kV/MW. The blue and red waveforms represent the measured and referred values, respectively. The origin of the DC voltage and active power are represented by the green waveforms.

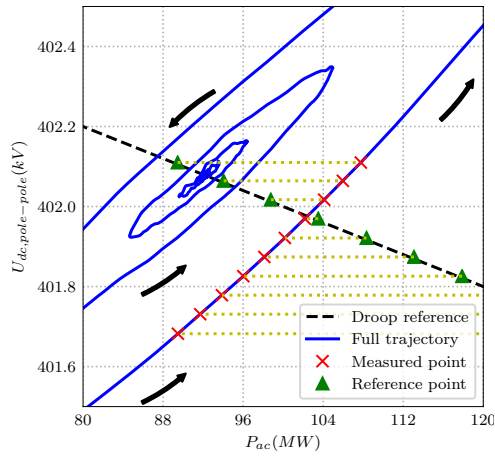


Fig. F.4: The results in Figure F.3(c) plotted in $P_{ac}-U_{dc}$ plane. The arrows indicate the direction of the trajectory. Ten points denoted with \triangle and \times represent the measured and referred DC voltage value at 0.675 until 0.6795 s, respectively. However, some of the active power references are outside the drawing plane and the yellow dotted lines connect the measured and referred active power values for the same time stamp.

APPENDIX G. ADDITIONAL RESULTS FOR THE 4-TERMINAL HVDC SYSTEM

In this chapter, the additional simulation results for the 4-terminal HVDC system depicted in Figure 5.1) are shown. These additional cases are:

1. DC system charging. As mentioned in Subsection 5.2.2, during the charging process of the DC system, the converter control is not yet active. Figure G.1 and Figure G.2 confirm that the simulation results with and without the IFC (conventional converter controls) are the same.
2. OWF ramp up event. The active power production of the OWF is ramped up until 300 MW. The simulation results are depicted in Figure G.3 and Figure G.4.
3. POD control integration with pilot *DroopCtrl* method. The same simulation case as in Subsection 5.2.8, except tha the IFC is used to implement the pilot *DroopCtrl* method. The settings for the IFC for each non-islanded converters are described in Subsection 5.2.7. Figure G.5–Figure G.7 depict the simulation results.

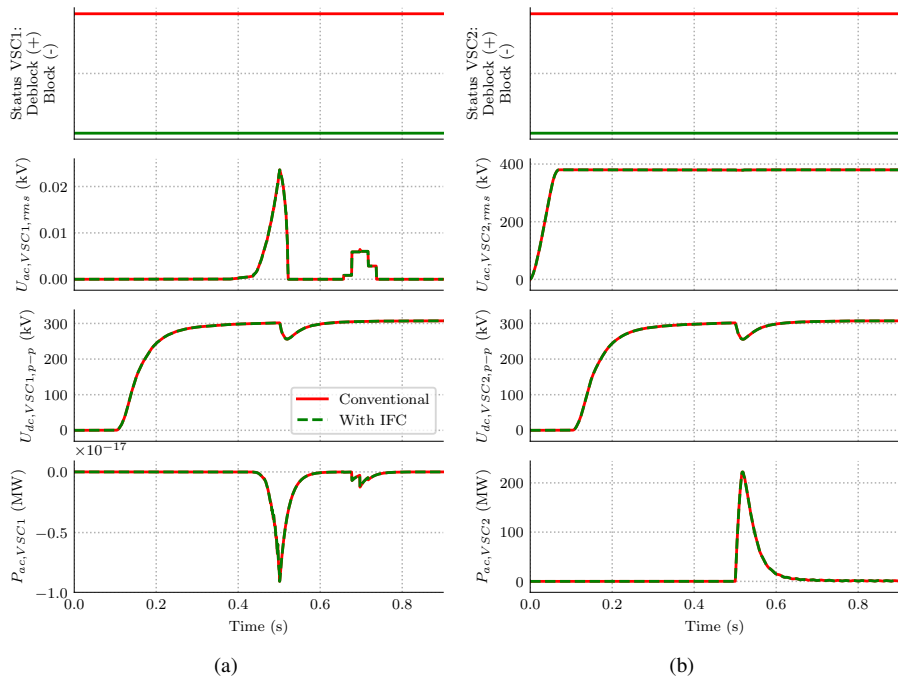


Fig. G.1: Simulation results of (a) VSC1 and (b) VSC2 during the first second when the MTDC system is started. *Conventional* refers to the condition when the conventional controls is activated, while *with IFC* represents the condition when the IFC is activated along with *UdcCtrl* mode in each of the non-islanded converter.

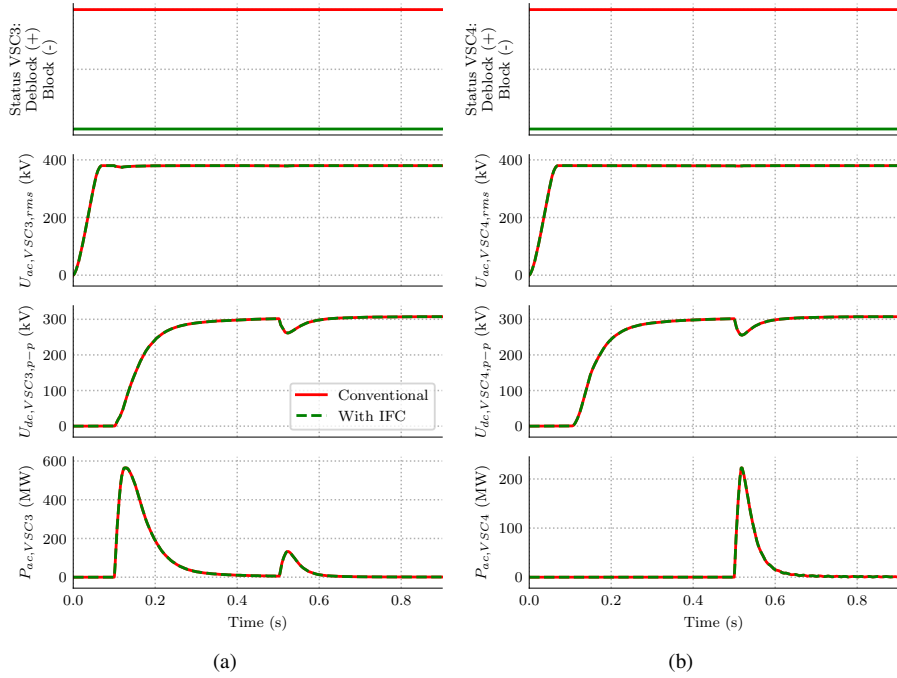


Fig. G.2: Simulation results of (a) VSC3 and (b) VSC4 during the first second when the MTDC system is started.

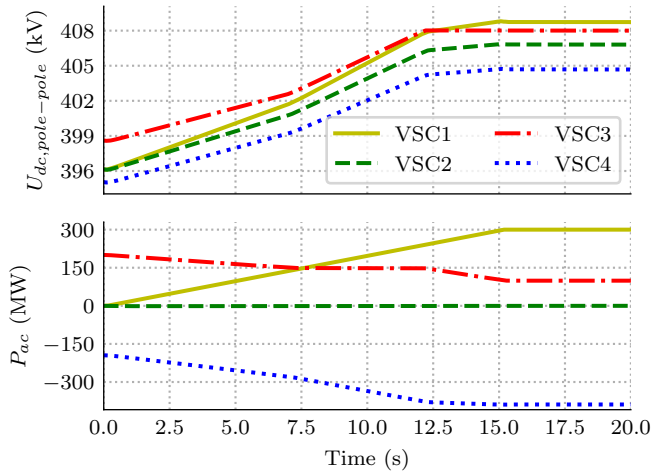


Fig. G.3: Simulation results when the OWF is ramped up until 300 MW with advanced converter control in VSC2, VSC3, and VSC4. The animated plots for these results are shown in Figure I.2.

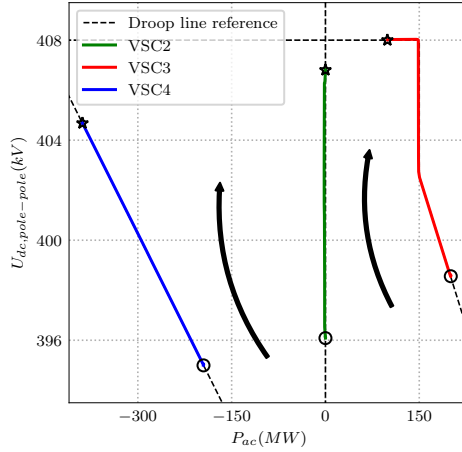


Fig. G.4: Figure G.3 results for VSC2, VSC3, and VSC4 plotted in P_{ac} - U_{dc} plane. The dashed black lines represent the droop line references, while the arrows point the movement direction. The points marked with \circ and \star represent measured values at 0.0 s and 20.0 s respectively. The animated plots for these results are shown in Figure I.3.

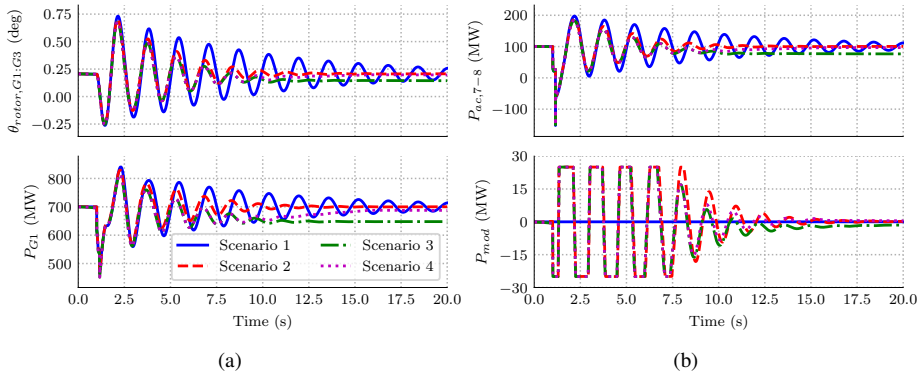


Fig. G.5: AC-side simulation results when the POD control is integrated using the pilot *DroopCtrl* method. (a) Measured rotor angle of G1 relative to G3 ($\theta_{rotor,(G1-G3)}$), the active power output of G1 (P_{G1}) and (b) AC tie-line power flow ($P_{ac,7-8}$). The blue, red, green, and magenta lines represent the results for Scenario 1, Scenario 2, Scenario 3, and Scenario 4, respectively.

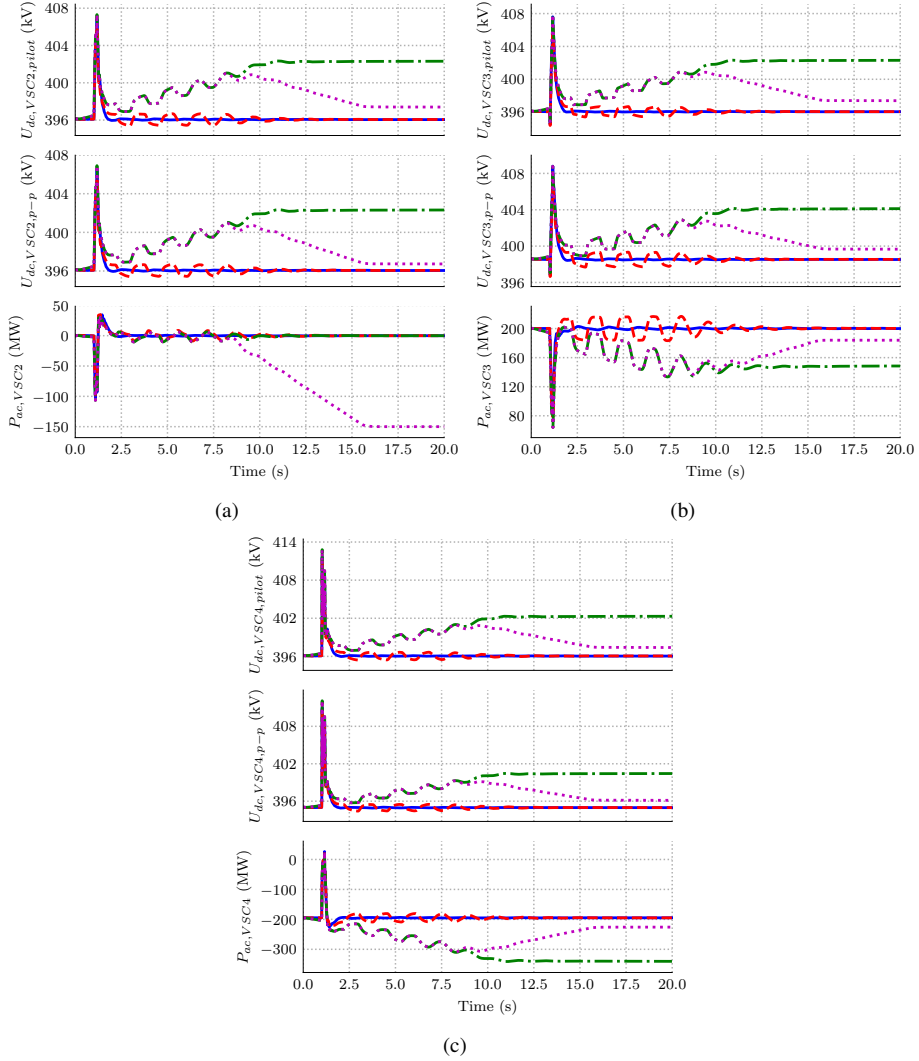


Fig. G.6: DC-side simulation results when the POD control is integrated using the pilot *DroopCtrl* method. (a), (b), and (c) Estimated DC Hub voltage, pole-pole DC voltage, and active power measured at the terminal of VSC2, VSC3, and VSC4.

Appendix G. Additional results for the 4-terminal HVDC system

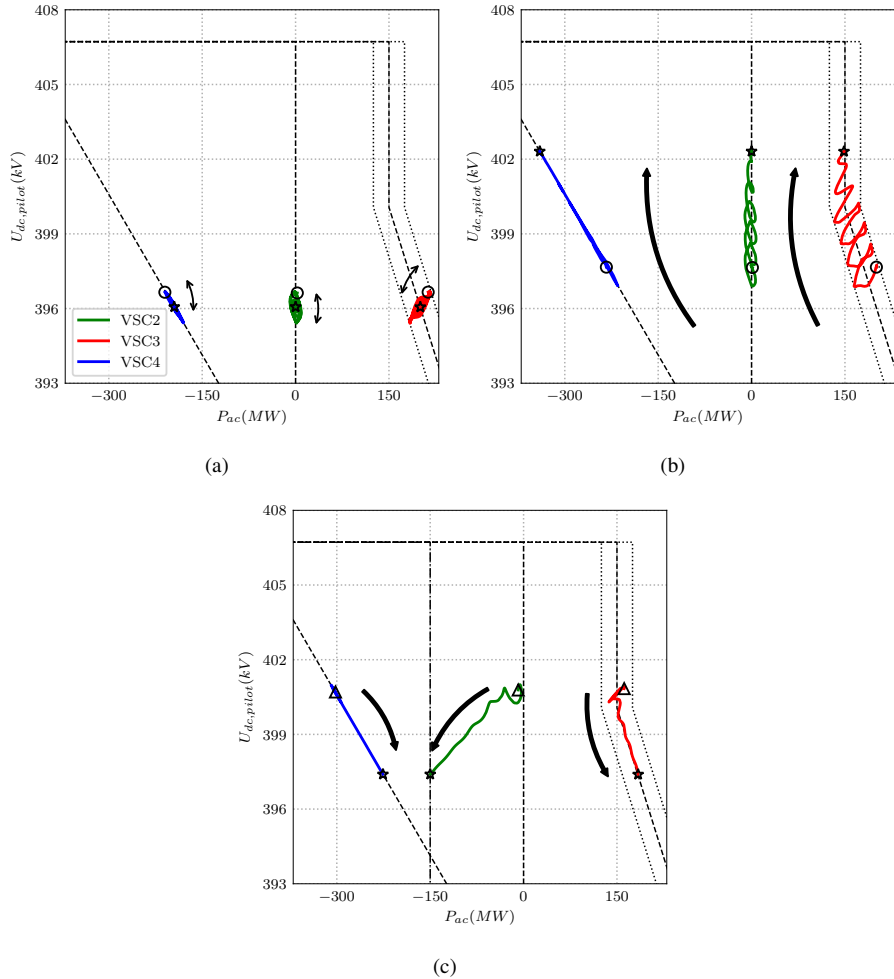


Fig. G.7: The droop plane plots of VSC2, VSC3, and VSC4 when the POD control is integrated using the pilot *DroopCtrl* method for: (a) Scenario 2, (b) Scenario 3, and (c) Scenario 4. The bold black lines represent the droop line characteristics. The dotted lines in VSC3 represent the maximum and minimum changes of the droop line, while the dash-dot line in (c) represents the droop line at the end of VSC2 ramp. The arrows point the movement direction. The points marked with \circ , \star , and Δ represent measured values at 2.0 s, 8.0 s, and 20 s respectively. The animated plots for these results are shown in Figure I.10–Figure I.14.

APPENDIX H. ADDITIONAL RESULTS FOR THE 9-TERMINAL HVDC SYSTEM

In this chapter, the additional simulation results for the 9-terminal HVDC system (Zone 2 and Zone 3 of the DCS3 system depicted in Figure 5.22) are shown. The simulations were performed with and without the IFC in all the non-islanded converters within the MTDC system. Without the IFC, the conventional controls are used, i.e. the conventional *PacCtrl* and U_{dc} -based *DroopCtrl* methods.

The following simulation cases are considered:

1. The startup process of the system. The same process for the 4-terminal HVDC system has been discussed in Subsection 5.2.2. However in this case, Cb-B1, Cb-B2, and Cm-B3 (*DroopCtrl* stations) are directly given the droop reference, i.e. specified in Table 5.4, instead of starting from *PacCtrl* with 0 MW reference as in Subsection 5.2.2. Furthermore, for the *PacCtrl* stations, the power reference is ramped up to its reference right after the converter is deblocked with a ramp speed of 500 MW/s. The simulation results for this case are shown in Figure H.2 (for converters in Zone 2) and Figure H.3 (for converters in Zone 3).
2. The droop reference step for Cb-B2. The droop line step is performed at 6.1 s, i.e. 0.1 s after the MTDC system reaches steady-state (after startup process). For the conventional *DroopCtrl* method this step can be achieved by changing the active power origin of the droop line for Cb-B2 specified in Table 5.4 to 0 MW. As explained in Section 5.3, Cb-B2 is a bipolar converter, which is consisted of two symmetric monopole converters. Therefore, there are 2 IFCs inside Cb-B2, i.e. one for each pole. Figure H.1 depicts the droop reference given to each of these IFCs. The droop reference step is performed by shifting the droop reference to the right, i.e. the green curve in Figure H.1. The simulation results are shown in Figure H.4 (for converters in Zone 2) and Figure H.5 (for converters in Zone 3). The trajectories for Cb-B1 and Cb-B2 (the *DroopCtrl* stations in Zone 2) are depicted in Figure H.6.
3. Emergency power order. This case is similar to the one performed in Subsection 5.3.1, i.e. the active power reference in Cb-D1 is reduced rapidly to 0 MW with the ramp speed of 1000 MW/s. The comparisons between the conventional and the IFC approaches are shown in Figure H.7 (for converters in Zone 2) and Figure H.8 (for converters in Zone 3).

Appendix H. Additional results for the 9-terminal HVDC system

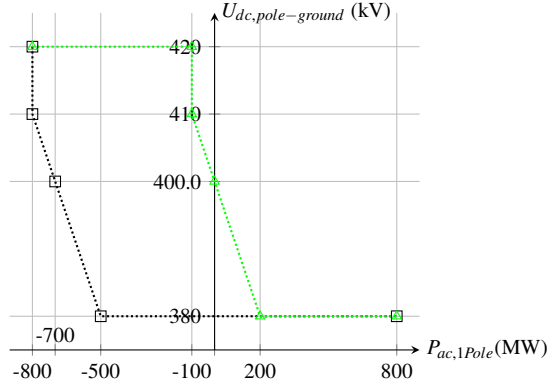


Fig. H.1: The droop line reference for the IFC installed in each pole of the Cb-B2 station. A 700 MW droop step is performed at 6 s, i.e. shifting the droop line from the black to the green one.

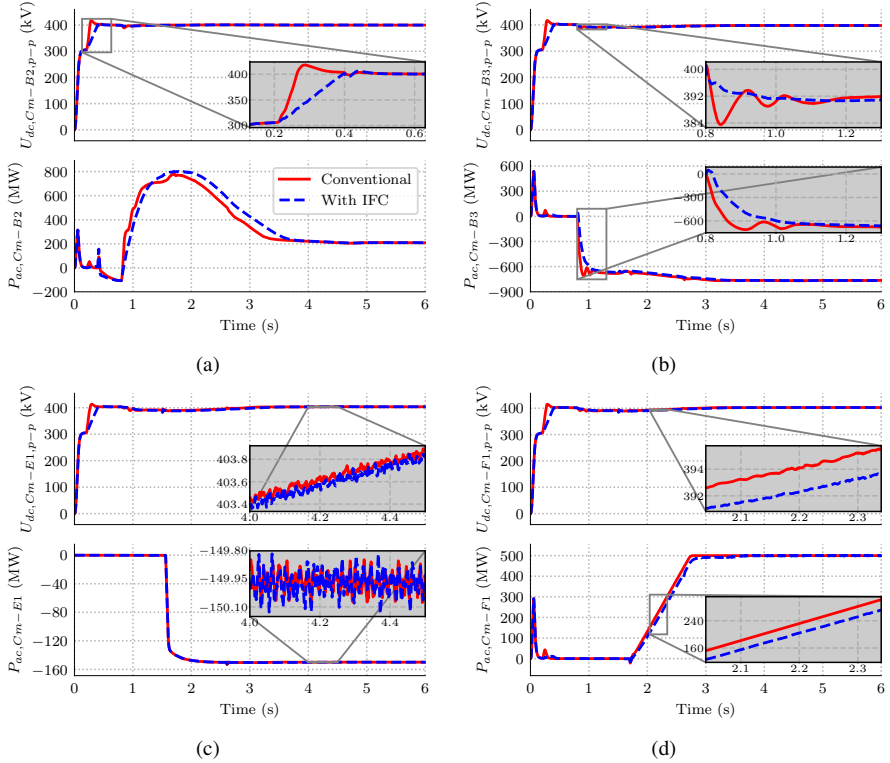


Fig. H.2: The condition in Zone 2 during the startup process of the 9-terminal HVDC system. The pole-ground DC voltage (top) and active power (bottom) measured at the terminal of: (a) Cm-B2, (b) Cm-B3, (c) Cm-E1, and (d) Cm-F1. The red waveforms represent the results with the conventional control system, while the blue ones represent the results with the IFC applied in all the non-islanded converters.

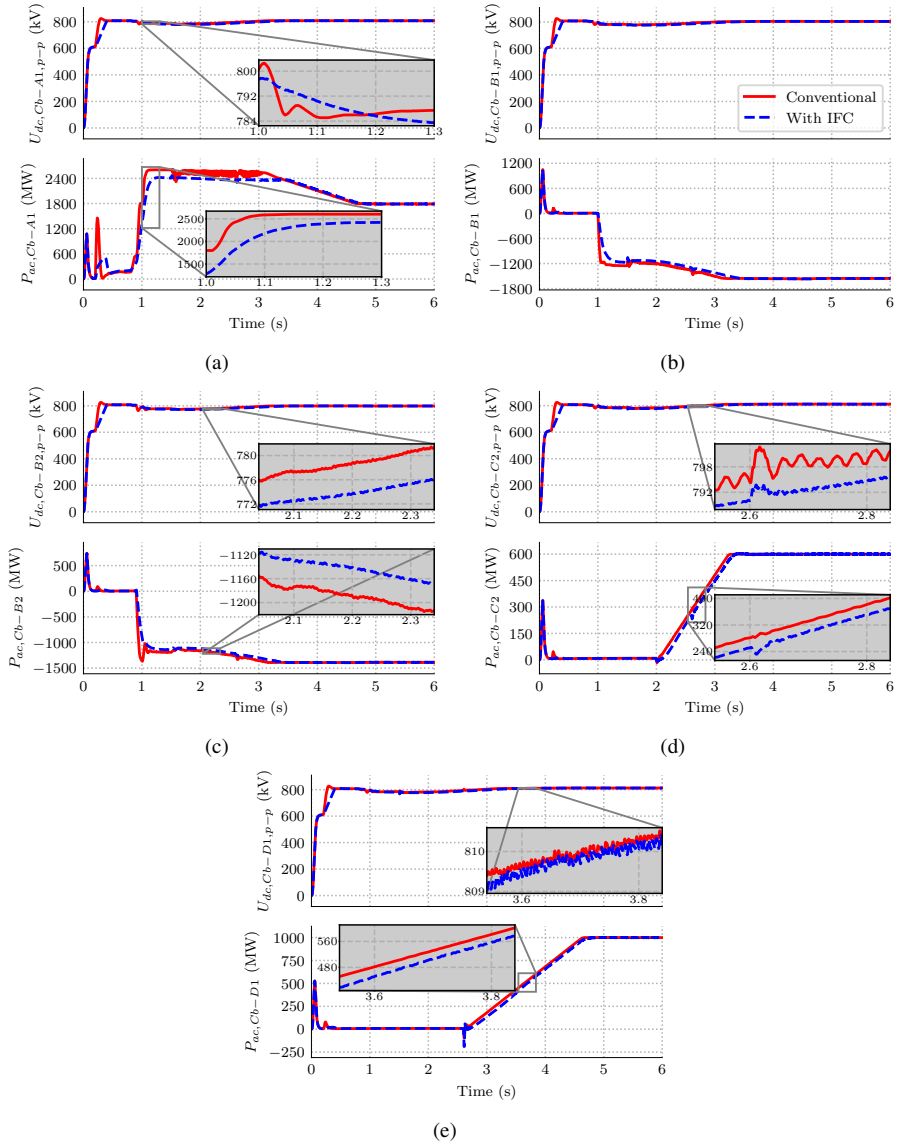


Fig. H.3: The condition in Zone 3 during the startup process of the 9-terminal HVDC system. The pole-pole DC voltage (top) and active power (bottom) measured at the terminal of: (a) Cb-A1, (b) Cb-B1, (c) Cb-B2, (d) Cb-C2, and (e) Cb-D1. The red waveforms represent the results with the conventional control system, while the blue ones represent the results with the IFC applied in all the non-islanded converters. The existing $UdcCtrl$ does not enforce with the active power limiter, therefore in (a) the active power reaches 2560 MW (red waveform) and might lead to oscillations due to the limiter inside the current controls.

Appendix H. Additional results for the 9-terminal HVDC system

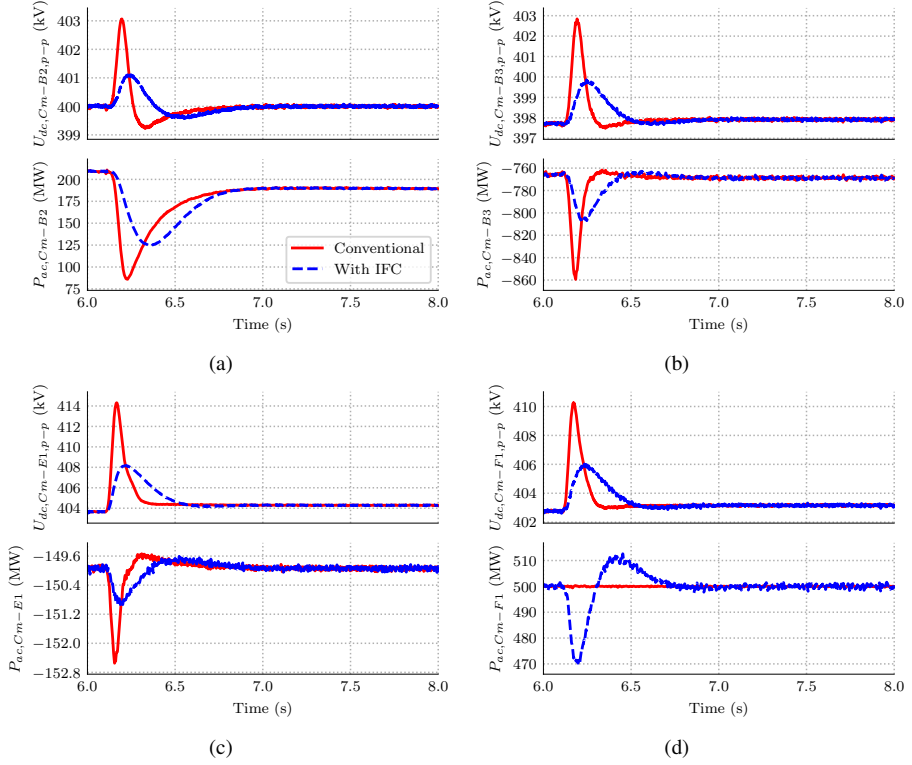


Fig. H.4: The condition in Zone 2 during the droop reference step at 6.1 s applied for Cb-B2. The pole-pole DC voltage (top) and active power (bottom) measured at the terminal of: (a) Cm-B2, (b) Cm-B3, (c) Cm-E1, and (d) Cm-F1. The red waveforms represent the results with the conventional control system, while the blue ones represent the results with the IFC applied in all the non-islanded converters.

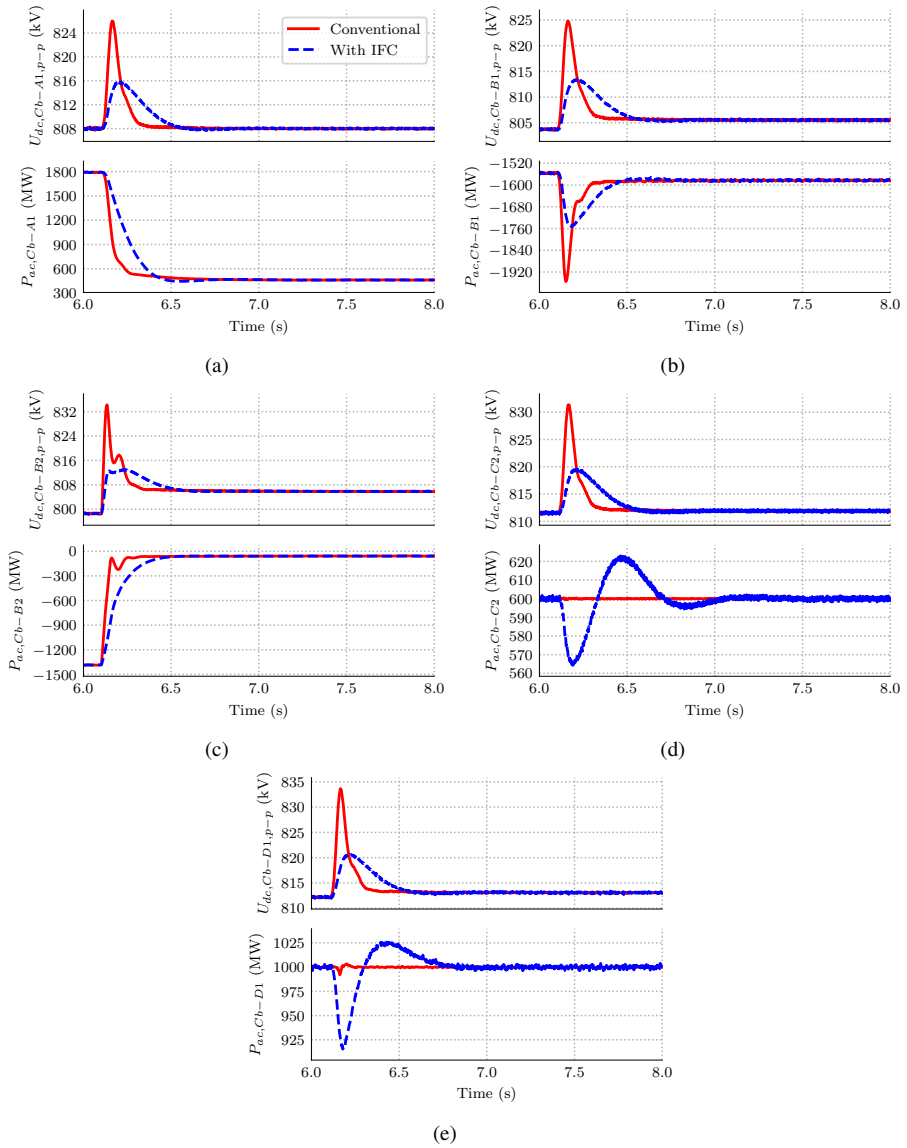


Fig. H.5: The condition in Zone 3 during the droop reference step at 6.1 s applied for Cb-B2. The pole-pole DC voltage (top) and active power (bottom) measured at the terminal of: (a) Cb-A1, (b) Cb-B1, (c) Cb-B2, (d) Cb-C2, and (e) Cb-D1. The red waveforms represent the results with the conventional control system, while the blue ones represent the results with the IFC applied in all the non-islanded converters.

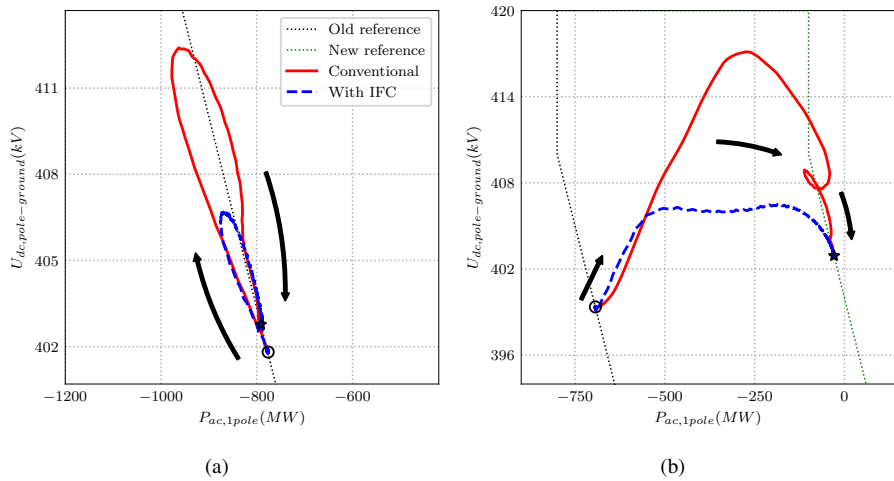


Fig. H.6: The trajectories of the conditions for the positive pole of: (a) Cb-B1 and (b) Cb-B2. The points marked with \circ and \star represent the steady-state conditions before and after the droop step, respectively. The droop step is performed in Cb-B2, i.e. shifting the droop line from the black dotted line to the green one. The arrows point the movement direction.

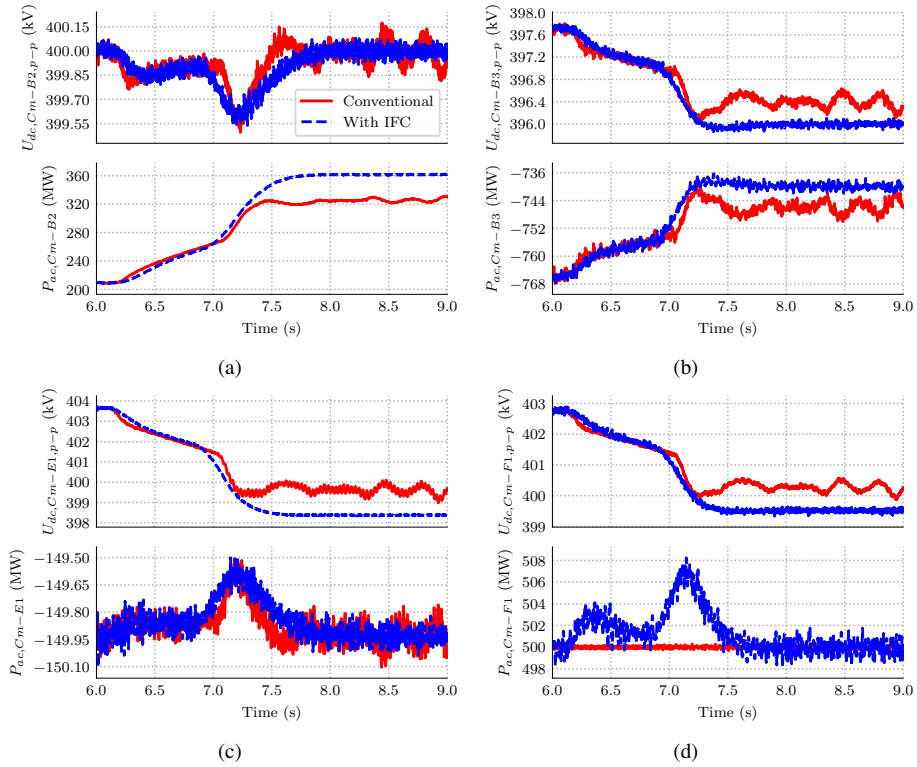


Fig. H.7: The condition in Zone 2 during the emergency power order in Cb-D1. The pole-pole DC voltage (top) and active power (bottom) measured at the terminal of: (a) Cm-B2, (b) Cm-B3, (c) Cm-E1, and (d) Cm-F1. The red waveforms represent the results with the conventional control system, while the blue ones represent the results with the IFC applied in all the non-islanded converters.

Appendix H. Additional results for the 9-terminal HVDC system

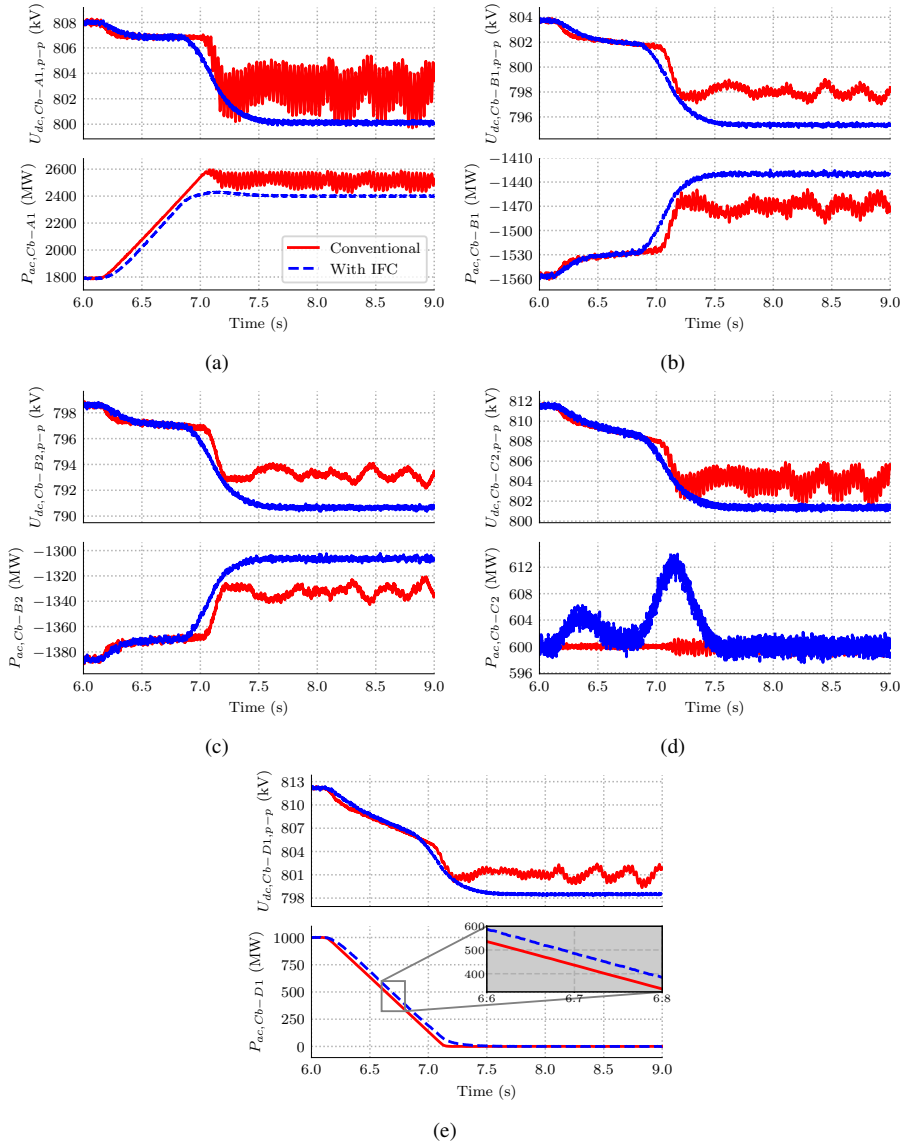


Fig. H.8: The condition in Zone 3 during the emergency power order in Cb-D1. The pole-pole DC voltage (top) and active power (bottom) measured at the terminal of: (a) Cb-A1, (b) Cb-B1, (c) Cb-B2, (d) Cb-C2, and (e) Cb-D1. The red waveforms represent the results with the conventional control system, while the blue ones represent the results with the IFC applied in all the non-islanded converters. The existing $UdcCtrl$ does not enforce with the active power limiter, therefore in (a) the active power reaches 2560 MW (red waveform) and might lead to oscillations due to the limiter inside the current controls.

APPENDIX I. ANIMATED PLOTS

The following animated plots for Section 5.2 are only available in the digital version of this thesis. Adobe PDF reader might be required to play these animated plots.

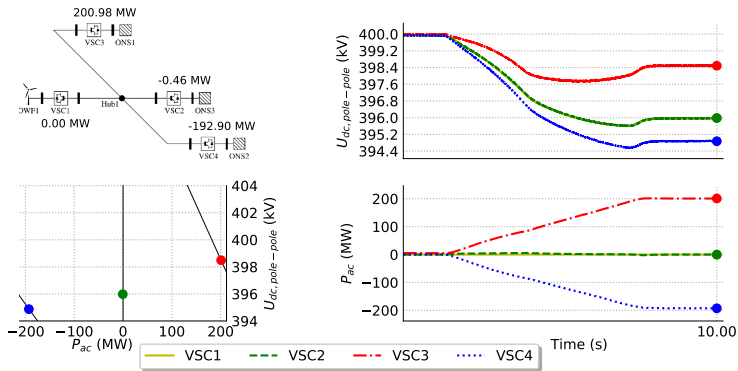


Fig. I.1: Animated plots for simulation results when the control mode of VSC3 and VSC4 are changed to the *DroopCtrl* mode (Figure 5.6 and Figure 5.7). The black lines in the $P_{ac}-U_{dc}$ plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

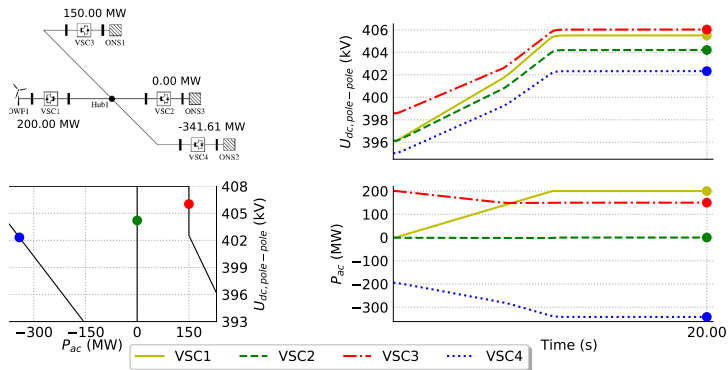


Fig. I.2: Animated plots for simulation results when the OWF is ramped up with the advanced converter control in VSC3 (Figure 5.10 and Figure 5.11). The black lines in the $P_{ac}-U_{dc}$ plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

Appendix I. Animated plots

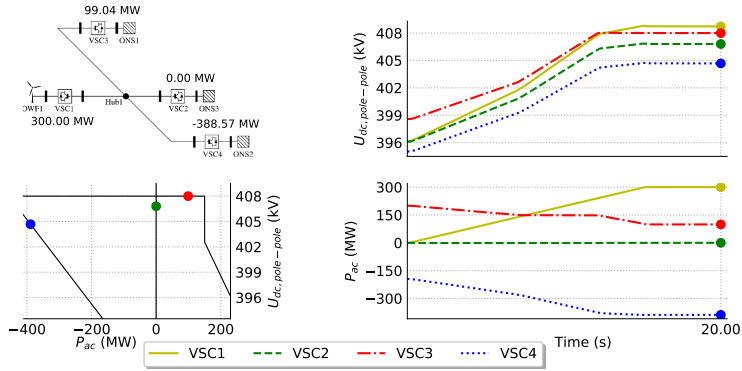


Fig. I.3: Animated plots for simulation results when the OWF is ramped up until 300 MW with the advanced converter control in VSC3 (Figure G.3 and Figure G.4). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

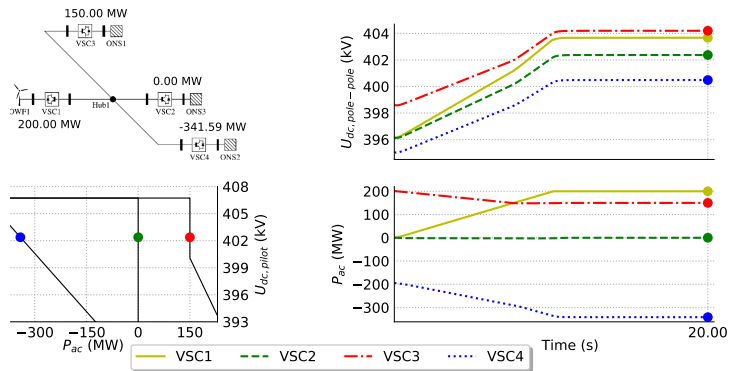


Fig. I.4: Animated plots for simulation results when the OWF is ramped up with the pilot *DroopCtrl* method realized in VSC2, VSC3, and VSC4 (Figure 5.16). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

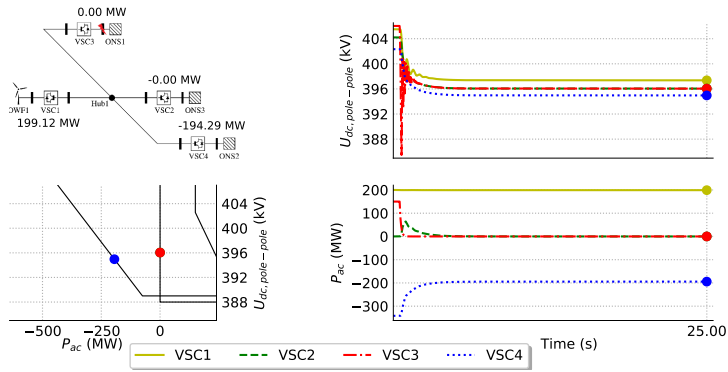


Fig. I.5: Animated plots for simulation results when a permanent AC fault occurs at the terminal of VSC3 after the OWF is ramped up until 200 MW with the advanced converter control in VSC3 (Figure 5.12(a) and Figure 5.13(a)). The black lines in the $P_{ac}-U_{dc}$ plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

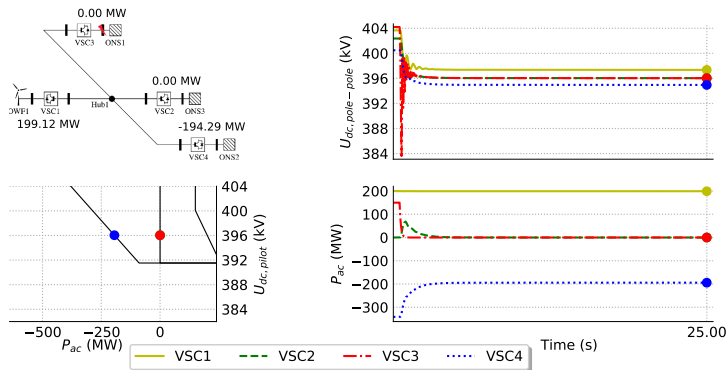


Fig. I.6: Animated plots for simulation results when a permanent AC fault occurs at the terminal of VSC3 after the OWF is ramped up until 200 MW with the pilot *DroopCtrl* method realized in VSC2, VSC3, and VSC4 (Figure 5.17(a) and Figure 5.17(c)). The black lines in the $P_{ac}-U_{dc}$ plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

Appendix I. Animated plots

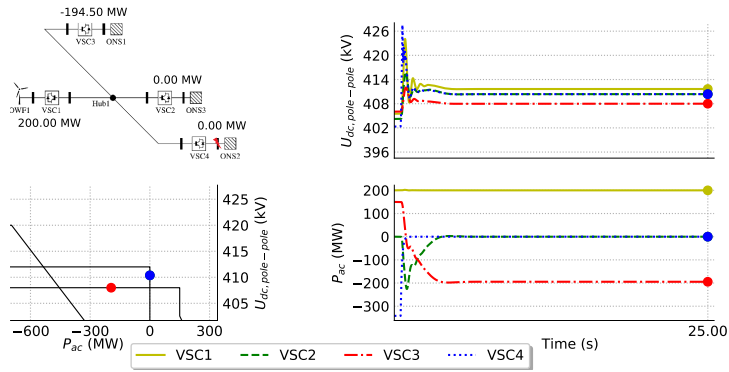


Fig. I.7: Animated plots for simulation results when a permanent AC fault occurs at the terminal of VSC4 after the OWF is ramped up until 200 MW with the advanced converter control in VSC3 (Figure 5.12(b) and Figure 5.13(b)). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

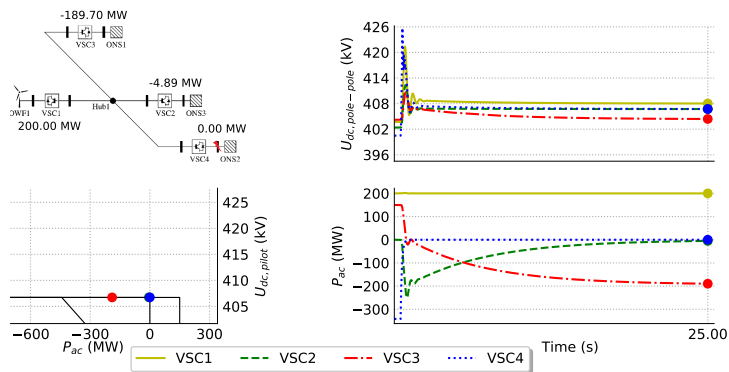


Fig. I.8: Animated plots for simulation results when a permanent AC fault occurs at the terminal of VSC3 after the OWF is ramped up until 200 MW with the pilot *DroopCtrl* method realized in VSC2, VSC3, and VSC4 (Figure 5.17(b) and Figure 5.17(d)). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

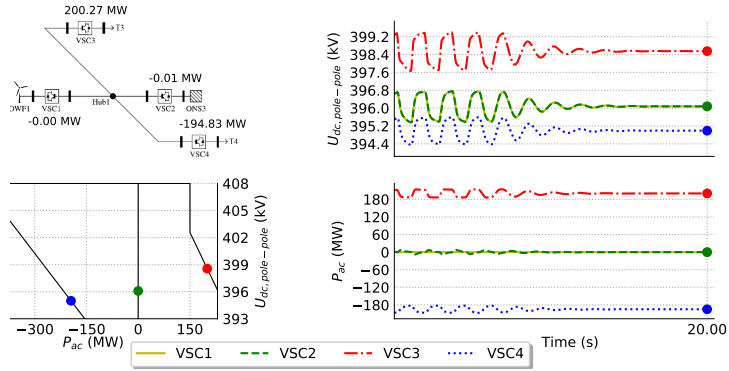


Fig. I.9: Animated plots for simulation results of test system with POD control and without ramp up in the OWF (Figure 5.20 and Figure 5.21(a)). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

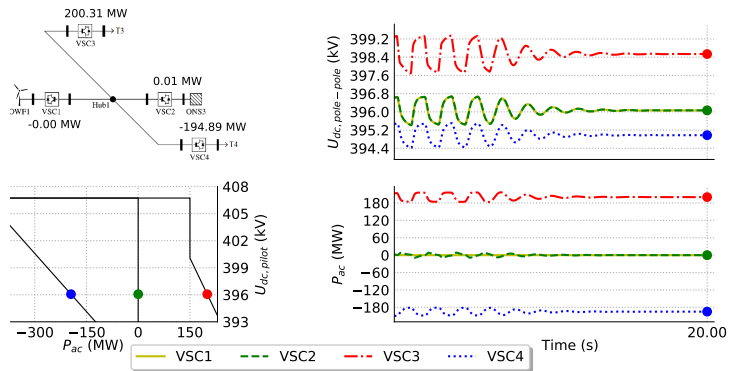


Fig. I.10: Animated plots for simulation results of test system with POD control and without ramp up in the OWF (Figure G.6 and Figure G.7). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

Appendix I. Animated plots

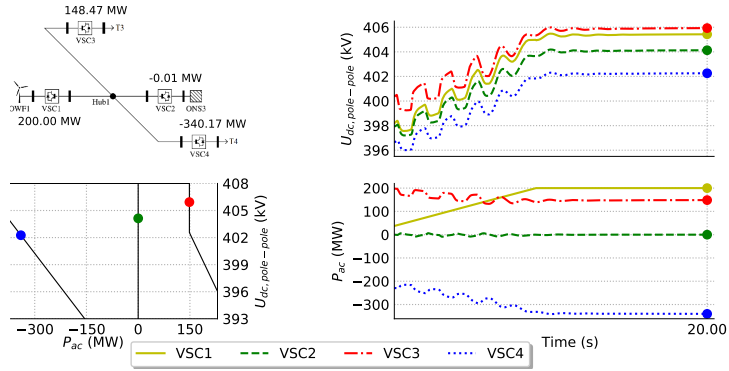


Fig. I.11: Animated plots for simulation results of test system with POD control and ramp up action in the OWF (Figure 5.20 and Figure 5.21(b)). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

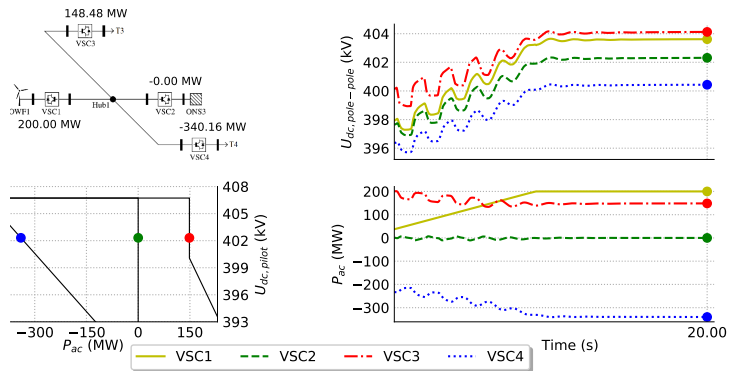


Fig. I.12: Animated plots for simulation results of test system with the pilot *DroopCtrl*, the POD control, and ramp up action in the OWF (Figure G.6 and Figure G.7). The black lines in the P_{ac} - U_{dc} plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

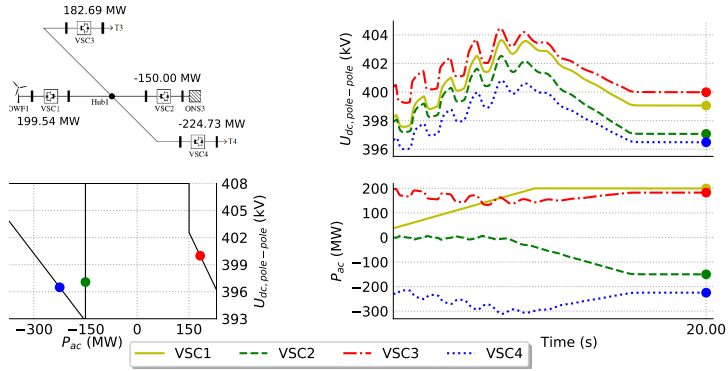


Fig. I.13: Animated plots for simulation results of test system with POD control , ramp up action in the OWF, and ramp down action in VSC3 (Figure 5.20 and Figure 5.21(c)). The black lines in the $P_{ac}-U_{dc}$ plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

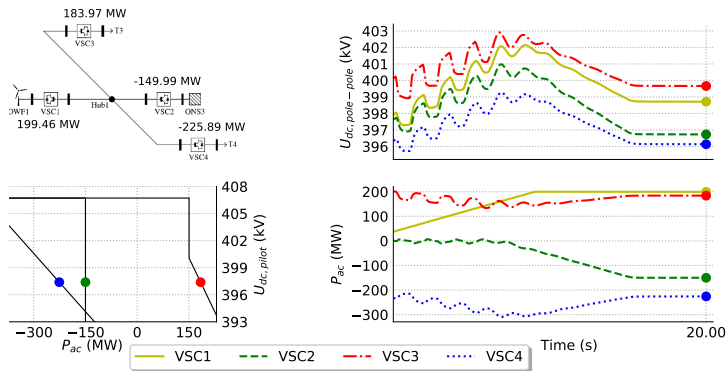


Fig. I.14: Animated plots for simulation results of test system with the pilot *DroopCtrl*, the POD control , ramp up action in the OWF, and ramp down action in VSC3 (Figure G.6 and Figure G.7). The black lines in the $P_{ac}-U_{dc}$ plane represent each droop line reference given to the IFC in VSC2, VSC3, and VSC4.

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