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Reliability of GaN-on-Si high-electron-mobility transistors for power electronics application

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RELIABILITY OF GAN-ON-SI HIGHELECTRON-MOBILITY TRANSISTORS FOR POWER ELECTRONICS APPLICATION

BY
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Sungyoung Song was born in Pusan, Korea, in 1980. He received the B.S and M.S degrees from the Department of Electrical Engineering from Changwon National University, Changwon, Korea, in 2006 and 2008, respectively. In the graduate school, he had studied on power integrated circuits. He participated in the analog-to-digital converter design project as an exchange student at the University of Washington, USA, from Aug. 2016 to Feb. 2017. He had worked as a development engineer of silicon-based semiconductor power devices with Magnachip Semiconductor, Korea, from 2008 to 2014. He is currently pursuing the Ph.D. degree with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His research interests include device technology and reliability for gallium nitride device. He is currently collaborating on the optimization technologies of GaN HEMTs for power applications with Charmers University of Technology, Sweden.

ENGLISH SUMMARY

The power electronic field is experiencing diastrophism with the advent of wide-band-gap devices. As the performance development of silicon metal-oxide-semiconductor-field-effect-transistors (MOSFET) and silicon insulated gate bipolar transistors (IGBT) that have taken over the market for the past four decades has almost saturated, the people have turned to new devices that can overcome their limitations. In principle, it makes sure that the wide-bandgap (WBG) devices have superior performance compared to the silicon counterparts. Nonetheless, there may be some technical barriers to achieving their success in the market, such as the reliability. The reliability of the power devices is very critical because it may directly affect the safety of the power electronic systems. Thus, the reliability of the WBG devices should be deeply investigated to convince the market that silicon devices already occupy.

A Gallium nitride (GaN) power device is a promising candidate to replace silicon MOSFETs at the market below a thousand volts. Several major companies have commercialized discrete GaN devices, and new products using the GaN devices are targeting mainly in new markets; light detection and ranging (LiDAR), Envelope Tracking, and wireless charging. Despite this great interest, the reliability of the commercial power GaN devices is only being verified with the Joint Electron Device Engineering Council (JEDEC) standard based on Si-based devices. The discrete GaN devices are fundamentally different from Si MOSFETs or IGBTs, from the principle the operation to the package technologies. Therefore, it is very urgent to study the reliability of them to prepare for new defects that can occur in the field in the future and to verify the problem in advance. In this PhD project, various researches on the reliability of the GaN devices from a packaged GaN device level to a GaN High-electron-mobility transistors (HEMT) unit structure level are performed.

The main content is divided into three main parts: the first part Chapter 2, the second part of Chapter 3 and 4, and the last part Chapter 5. The first part is including the performance assessment results of current commercial power GaN devices, their theoretical limit and their figure of merit information. The second part is discussing the reliability and failure mechanisms of the cutting-edge commercial GaN device regarding thermal and thermo-mechanical stress. The GaN device to be tested has been selected based on the assessment results in Chapter 2. The apparatus and methodology for an accelerated power cycling test of the GaN device have been presented. The failure analysis of the GaN devices degraded by the power cycling test has been performed with supplement experiments, collected data, the literature and physical examination techniques in Chapter 4. In the last part, the device technologies that could affect the performance and the reliability of a GaN HEMT is discussed, and an experiment plan to find the optimization conditions is proposed.

Main contributions in this project are the first power cycling test with the cutting-edge GaN device and the in-deep consideration of failure mechanisms induced by thermal stress. The power cycling test suitable for the operating features of the advanced GaN devices has been conducted. The new failure phenomenon that has never been reported has been found. The diverse possibilities that could lead to this failure have been checked one by one. Furthermore, potential risk and a solution for this risk have been proposed through this analysis process.

Various experimental results and analysis results carried out in this thesis verify the effectiveness of this project.

DANSK RESUME

Effektelektronik-feltet oplever en rivende udvikling på grund af fremkomsten af "wide-bandgap" komponenter. Silicium transistorene "metal-oxide-semiconductor-field-effect-transistors" (MOSFET) og "insulated gate bipolar transistors" (IGBT), som har domineret transistor-markedet de sidste 4 årtier, er næsten nået grænsen af mulig ydeevne. Dette har fået folk til at søge mod nye komponenter der kan overkomme de gamle transistorers begrænsninger. Teoretisk har "wide-bandgap" (WBG) komponenter overlegen ydeevne i forhold til deres silicium-baseret modstykke. Der kan dog alligevel være tekniske barrierer mod WBG komponenters success på markedet, som for eksempel deres pålidelighed. Pålideligheden af effekt komponenter er meget kritisk da det kan direkte påvirke sikkerheden af et effektelektronisk system. Derfor bør pålideligheden af WBG komponenter undersøges grundigt for at overbevise det marked som silicium allerede sidder på.

En Galiumnitrid (GaN) effekt komponent er en lovende kandidat for at erstatte silicium MOSFET'er under 1000 volt på markedet i dag. Flere store firmaer har kommercialiseret diskrete GaN komponenter og nye produkter der bruger GaN komponenter retter sig hovedsageligt mod nye markeder, såsom "LiDAR" , "Envelope Tracking", og trådløs opladning. Trods den store interesse bliver GaN komponenter kun verificeret med "Joint Electron Device Engineering Council" (JEDEC)-standarden som er baseret på silicum-baseret komponenter, men diskrete GaN komponenter er fundamentalt anderledes end Si MOSFET'er eller IGBT'er, fra deres virkemåde til brugte "packaging" teknologier. Det er derfor meget vigtigt at undersøge pålideligheden af disse komponenter for at forberede sig på nye typer af defekter der can opstå i fremtiden og for at verificere problemerne på forhånd. I dette PhD projekt er forskellige undersøgelser lavet af pålideligheden af GaN komponenter, fra et "packaged" GaN komponent niveau til et GaN "High-electron-mobility-transistor" (HEMT) enheds-struktur niveau.

Hovedmaterialet er opdelt i tre dele: Den første del er kapitel 2, den anden del er kapitel 3 og 4 og den sidste del er kapitel 5. Den første del drejer sig om vurderingen af ydeevnen af GaN effekt komponenter der er tilgængelige kommercielt i dag, samt deres teoretiske grænse og deres "figure of merit" information. Den anden del diskuterer pålideligheden og fejlmekanismerne i den banebrydende kommercielt tilgængelige GaN komponent i forhold til termisk og termomekanisk stress. GaN komponentet der blev testet blev valgt på baggrund af kapitel 2. Apparaterne og methoderne for en accelereret "power cycling" test af GaN komponentet er her præsenteret. Fejlanalysen af GaN komponenterne som er blevet degraderet af "power cycling" testen med supplerende eksperimenter, indsamlet data, literaturliste og fysiske undersøgelsesmetoder kan findes i kapitel 4. I den sidste del diskuteres de komponent-teknologier der kan påvirke ydeevnen og pålideligheden af en GaN eHEMT, og en experiment plan for at finde de optimale betingelser er her foreslået.

De primære bidrag i dette projekt er: Den første "power cycling" test med de banebrydende GaN komponenter og en dybdegående overvejelse af fejlmekanismerne der opstår ved termisk stress. En passende "power cycling" test af funktionerne af de advancerede GaN komponenter er udført, og en ny fejlmekanisme der aldrig har været rapporteret før er blevet fundet. De forskellige grunde der kunne forårsage denne fejlmekanisme er blevet undersøgt én efter én. Der er derudover også blevet vurderet den potentielle risiko denne fejlmekanisme udgør og en mulig løsning dertil gennem en analytisk process.

Mange forskellige eksperimentielle og analytiske resultater fundet igennem denne PhD-afhandling bekræfter værdien af dette projekt.

ACKNOWLEDGEMENTS

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Aalborg Denmark

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CHAPTER 1. INTRODUCTION

This chapter firstly presents the overall background and motivation of this research project. After that, the thesis outline and the list of publications related to this research are described.

1.1. POTENTIAL OF GAN DEVICES IN POWER APPLICATION

1.1.1. PROSPECT OF GAN POWER DEVICES

Wide-band-gap (WBG) semiconductor materials such as Gallium nitride (GaN) and Silicon carbide (SiC) are renowned as alternative candidates against silicon (Si) [1]. Their WBG properties enables a power device to be more compact, faster, and more efficient compared to silicon-based devices. Thanks to the excellence of WBG devices, they are receiving constant attention from the power electronics field. Both GaN and SiC products had already been on the market. Employing WBG devices has been reported mainly in high-end applications such as renewable energy over the recent years [2, 3]. Although GaN devices were universally applied to the three fields of radio frequency (RF), a light emitting diode (LED), and power electronics a decade ago, this thesis is limited to the power electronics field.

The market share of GaN devices at present is tiny in the entire power market, but sustained growth of them is predicted with the possibility of development. Yole Development expects a thirty-two-times increase of GaN device market by 2022 based on 2016 revenue [4]. Fig 2-1 shows the promising outlook of GaN device market. Emerging end-products using GaN transistors inside are now gradually expanding especially in power supply for datacentre and telecom, AC fast charger, automotive LiDAR, Envelope Tracking, and wireless power [5]. There is a promising future for GaN devices in power applications.
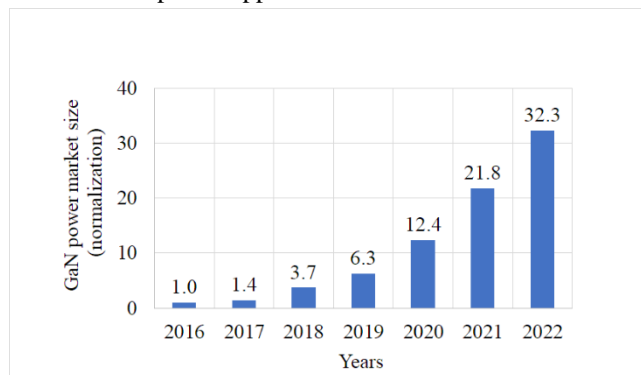
Figure 1- 1 Market size prospect of GaN power devices from 2016 to 2022 [4].
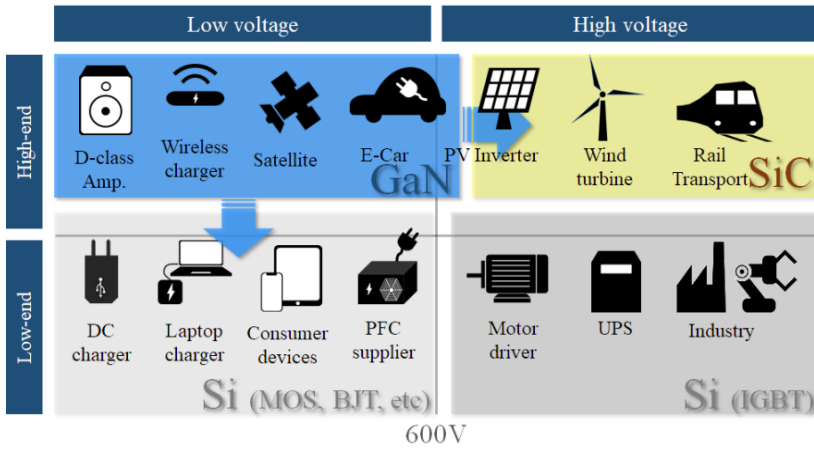
Figure 1- 2 Market segmentation and applications of major power electronic devices [139].

1.1.2. APPLICATION OF POWER GAN DEVICES

GaN power devices is an attractive device in the field of low voltage (LV) power electronics application. They can promise end-users higher efficiency, size and weight reduction, and faster operation frequency. Despite these advantages, commercial GaN devices are expensive compared to the similar voltage-rate Si metal-oxide semiconductor field-effect-transistor (MOSFET). Figure 1-2 exhibits the market segmentation of the significant power devices for each use [1, 3]. Although the GaN devices are in the high-end and under 650 V application range [2, 3], they are expanding their area through ongoing cost savings and technology improvement. Hence, the prospects of GaN power devices are bright for the future.
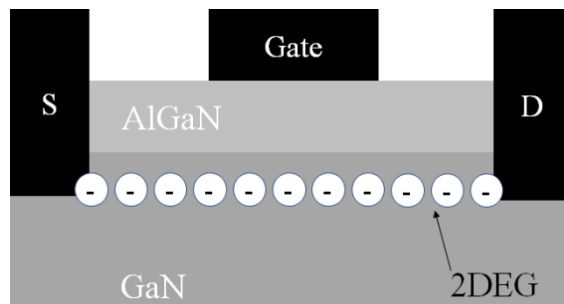
Figure 1- 3 Basic structure of a depletion mode GaN HEMT.

1.1.3. POTENCIAL OF A GAN POWER DEVICE

Most of commercial GaN power devices have a GaN high-electron-mobility-transistor (HEMT) structure. Figure 1-3 shows a basic structure of a depletion-mode GaN HEMT. The GaN HEMTs intrinsically have a two-dimensional electron gas (2DEG) as a current channel. Because the 2DEG is highly conductive, it can contribute to the excellent on-state resistance characteristics of a GaN HEMT.

The properties of a GaN power device can be examined looking at their theoretical limit of the device. The relationship between specific $R_{DS(ON)}$ (R_{SP}) and breakdown voltage (V_{BR}) of a power device is stated as given in Equation (1.1). In this equation based on solid-state physics [6], ε_0 is the permittivity of a vacuum, ε_r is the relative permittivity of the crystal compared to a vacuum, E_{crit} is the critical electric field of material, and μ_n is the electron mobility in given semiconductor.

$$R_{SP} = \frac{4 \cdot V_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot E_{crit}^3 \cdot \mu_n} \quad [m^2 \cdot \Omega] \quad\quad (1.1)$$

The fraction of Equation (1.1) is composed of constants from the physical properties of given material. Si, SiC, and GaN are primary candidates for a power transistor. GaN power devices can be classified into two types: a vertical GaN transistor and a GaN HEMT using a 2DEG. The theoretical limits of both are different because of electron mobility difference between GaN and 2DEG. Table 1-1 displays specific characteristics of each material. In GaN HEMT material, the electron mobility of 2DEG is adopted as μ_n. The electron mobility of GaN material is applied to the theoretical limit of a vertical GaN transistor. The equation can be plotted with the material properties of Si, SiC, vertical GaN, and GaN HEMT as shown in figure 1.4. Theoretical borders of a power device by a given semiconductor material are included

Para meter	Description	Unit	Material properties			
			Si	4H-SiC	GaN	GaN HEMT
ε_0	Vacuum permittivity	F/cm	8.9 E-14			
ε_r	Relative permittivity	-	11.8	9.7	9	9
E_{crit}	Critical electric field	MV/cm	0.3	2.2	3.3	3.3
μ_n	Electron mobility	cm²/V·s	1300	950	900	2215

Table 1- 1 Material properties of Si, 4H-SiC, GaN, and GaN HEMT [6, 7, 140].
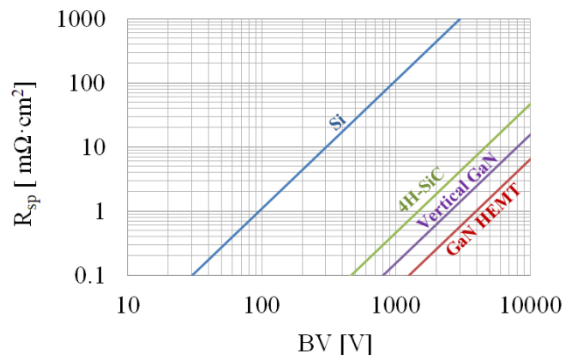
Figure 1- 4 Ideal R_{sp} and V_{BR} capability of Si, 4H-SiC, vertical GaN, and GaN HEMT.

in the chart. In theory, GaN HEMTs can have the best conductivity than Si, SiC, or vertical GaN transistors at the same V_{BR}, thanks to their 2DEG and WBG properties.

1.2. A GAN HEMT IN POWER APPLICATION

A GaN HEMT built on a SiC substrate emerged as a transistor for radio frequency (RF) application in 2004 [6]. There had been various efforts for GaN HEMT to be used as the switching device for power application [12]. Subsequently, we can meet a commercial power GaN HEMT that overcomes technical hurdles on the market. In this section, technologies used in a commercial GaN HEMT are discussed.

1.2.1. A SUBSTRATE

The appearance of a GaN HEMT grown on Si substrate had attracted attention of the power electronics device market [6, 12]. In the early of development, a GaN layer the

Parameters	Unit	Material properties		
		Sapphire	SiC	Si
Thermal conductivity	W/cm·K	0.3	4.9	1.5
Lattice mismatch with GaN	%	16	4	17
Coefficient thermal expansion mismatch with GaN	%	39	3.2	54

Table 1- 2 Material properties of different substrates [10].

basis of a GaN HEMT had been mostly grown on sapphire or SiC. The sapphire substrate has some disadvantages: lower thermal conductivity, the large lattice mismatch with GaN, and significant coefficient of thermal expansion (CTE) mismatch. On the other hand, a SiC substrate shows high thermal conductivity, low lattice mismatch, relatively low CTE mismatch compared with Si or sapphire [8]. Despite these merits, a SiC substrate wafer is more expensive than a Si substrate wafer. In Ref. [9], a SiC wafer cost is fifteen times as much as a Si wafer. Primary properties of each substrate in Table 1-2 describe their advantages and disadvantages [10]. For these reasons, power GaN device suppliers have developed a product with a GaN on Si HEMT.

Price competitiveness of GaN devices is essential to penetrate the power electronics market. Although the Si substrate has lower thermal conductivity, more considerable lattice mismatch with GaN, and larger CTE mismatch compared to the SiC substrate, most commercial power GaN devices are fabricated on a Si wafer most inexpensive of the above three candidates. Besides, wafer suppliers such as EpiGaN has developed an 8-inch GaN-on-Si wafer [11, 12]. Currently, primary power GaN device suppliers such as EPC, Panasonic and GaN systems Corporation are applying a 6-inch wafer to their products [5, 13, 14]. Therefore, if they migrate to an 8-inch GaN-on-Si wafer, the price of GaN devices may drop further.

1.2.2. NORMALY-OFF TECHNOLOGY

Normally-off characteristic of GaN transistors is required in power electronics application. A transistor with the normally-off characteristics is often called an enhancement mode (E-mode) transistor. Various technical challenges have been attempted to achieve a positive threshold voltage: p-doped GaN under gate, p-doped AlGaN under gate, recessed gate, plasma treatment under gate, recessed AlN gate, hybrid MOS-HFET, and cascode structure [15]. These technologies are very significant factors which affect the electrical performance of GaN devices such as on-state resistance and off-leakage current.

Company	V_{th} [V]	Gate technology for normally-off
EPC [15, 16]	1.4	P-doped GaN gate cap
GaN Systems [17, 18]	1.3	P-doped GaN gate cap
Panasonic [19, 20]	1.2	AlGaN recess etch, P-doped GaN gate cap, P-doped GaN near drain
Transphorm [21]	1.8	Cascode
On-Semiconductor [22]	2.1	Cascode

Table 1- 3 Threshold voltages (Vth) and gate technologies for normally-off operation of commercial discrete GaN transistors [15-22].

Commercial GaN devices are using different gate technologies for the normally-off operating. Table 1-3 shows the threshold voltage level and gate technologies of primary suppliers of GaN transistors on the market. EPC and GaN Systems are using p-doped GaN gate cap layer for E-mode operation [7, 8]. Even though Panasonic had employed a simple p-doped GaN cap layer in the beginning, they had introduced a new product named X-GaN with a hybrid drain-gate injection transistor (HD-GIT) technology in 2017 [9]. The architecture is complex and uses three techniques; AlGaN recess etch, p-doped GaN in the gate, and p-doped GaN layer in drain [10]. They improved current collapse issues due to the new technology. The last two companies Transphorm and On Semiconductor incorporate an additional low-voltage Si MOSFET for normally-off operation. Two chips a normally-on GaN die and a normally-off Si MOSFET are connected in a cascode structure [11]. These diverse technologies eventually result in performance difference among products.

1.2.3. PACKAGE TECHNOLOGY

Package technology of a power GaN device has a significant effect on overall performance of the product. It had been confirmed that a GaN device could offer promising switching performance for a power conversion circuit [23, 24]. To maximize this advantage of the GaN device, the performance of the package becomes more critical than others. There are three primary functions required of the power GaN device: small stray inductance, high thermal conductivity, and high reliability. Particularly in the high-speed application, a low parasitic inductance characteristic of the package is emphasized more. Therefore, commercial GaN devices need more enhanced package technology.

Package technologies of commercial GaN devices show exceptional performance compared to conventional packages. Stray inductance and junction-to-case thermal resistance times package area ($R_{\theta JC}$ * A) are crucial figures of merit (FOM) which
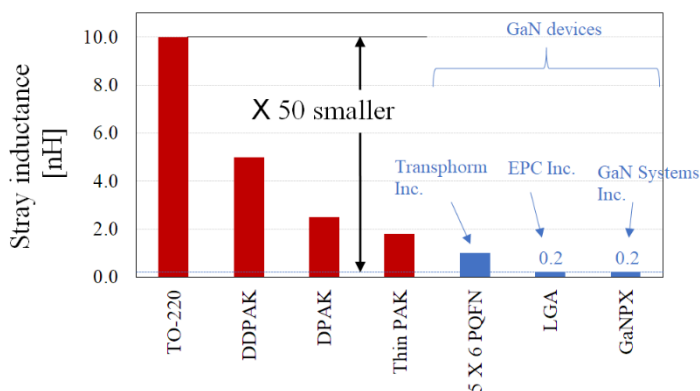
Figure 1- 5 Stray inductances of different package technologies [25-27].
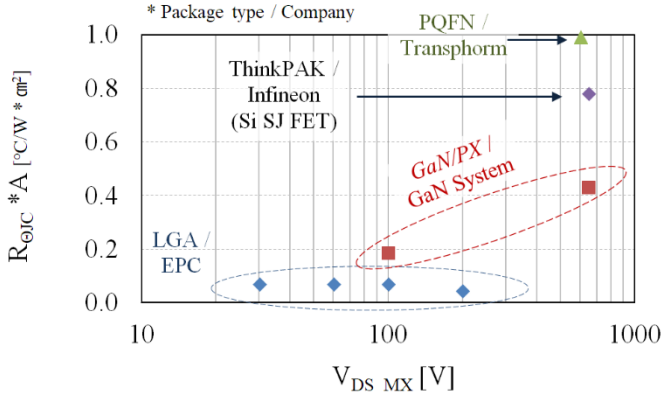
*Figure 1- 6 R$_{\theta JC}$ * A versus maximum drain-to-source voltage of commercial discrete GaN power devices [16,17, 28-33].*

express the performance of specific package technology. A bar graph in Figure 1-5 displays the stray inductances of different package technologies [25-27]. The commercial GaN devices have relatively lower stray inductances than others. The stray inductance of land grid array (LGA) and GaNPX^{TM} from GaN Systems packages is 0.2 nH fifty times smaller than the TO-220. Figure 1-6 illustrates thermal conductivity of each device. To easily understand, the state-of-the-art Si-based Super-junction (SJ) device are added [33]. LGA and GaNPX show less R$_{\theta JC}$ * A than the Si SJ device. At V$_{BR}$ = 650 V, GaNPX has two times better thermal conductivity compared to the Si SJ device. These advanced package technologies are contributing to the performance of the commercial GaN devices.

The GaNPX package, which exhibits excellent performance in the highest operating voltage of commercial power GaN devices, is different from the conventional package technology. Figure 1-7 displays that GaNPX is much geometrically different than a conventional package [25, 32]. GaNPX can achieve nine times thinner thickness due
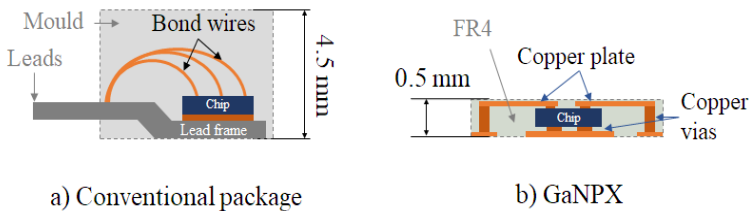
Figure 1- 7 Cross section of a) conventional package technology with bond wires [32] b) GaNPX^{TM} [25].

to the spetial structure using copper vias and plates instead of the bond wires. The compact structure allows the GaN device to possess not only better electrical performance but also better thermal conductivity. Besides, this packaging technology ultimately can be embedded in an FR4 printed circuit board (PCB). For these reasons, the package has received attention from the power device market.

1.3. RELIABILITY OF GAN HEMTS IN POWER APPLICATION

Concerning the possibilities for superior electrical performance, the GaN HEMTs can be a challenging candidate to replace Si-based transistor in specific fields of the power electronics. For successful positioning of GaN HEMTs on the power electronics market, GaN HEMTs must be accompanied by sufficient evaluation results to prove their reliability. Major GaN suppliers recently are currently under the qualification of their products with the Si-based qualification standard Joint Electron Device Engineering Council (JEDEC). However, the reliability of the GaN HEMT products cannot wholly guarantee solely with the existing qualification procedures of Si devices because of the new failure phenomena found only in GaN HEMTs. Therefore, additional qualification standard suitable for GaN HEMTs and new reliability studies focused on GaN HEMTs are needed. In this section, the reliability of GaN devices in power electronics application and the needs for additional reliability studies will be discussed.

1.3.1. RELIABILITY OF POWER DEVICES IN POWER ELECTRONICS

Power devices play a crucial role for the reliability of power electronics systems. The systems consist of various components such as a power device, gate driver IC, inductor, capacitor, resistor, transformer etc. They can affect individually the reliability of the entire systems [35]. There was a survey to inverstigate which device is critical for the reliability of power electronics products [36]. A pie chart in Figure 1-8 shows the failure contribution in power electronics systems from the survey. In
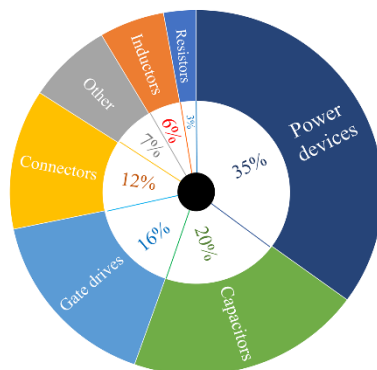
Figure 1- 8 Failure distribution in power electronic systems from the survey [36].

the survery, it is revealed the the power device are the most breakable element in a power electronics product. In this regard, securing the robustness of the power device allows for a more rubust systems.

Thermo-mechanical stress is a significant stressor that can destroy power devices [37]. For this reason, there had been many studies on test methodes, failure mechanisms, and life time modeling of the failure induced by thermo-mechanical stress [38-40]. The failure mechanism from the thermo-mechanical stress can be described with the different coefficient of thermal expansion (CTE) among the material constituting a power device. In the above survey, the half of overall converter operation is subjected to juction temperature swings larger than 80 degree Celcius [36]. The repeated temperature variation during operating provokes the thermo-mechanical stress amongst elements inside a power device. Finally, the power device loses their normal function due to this stress at a certain point in time.

1.3.2. FAILURE MECHANISMS BY A POWER CYCLING TEST

There are representative two test methodologies relevant to verify the robustness of a power device against the repeated thermal-mechanical stress: i) temperature cycling test and ii) power cycling test. The temperature cycling (TC) test is called a passive TC test because they use external temperature swings [41]. It is to examine the reliability of package technologies for ambient temperature changes. In contrast, the PC test is closer to the actual operation of the power devices because the test simulates the temperature changes from heat generated at the internal junction by the power consumption of a power semiconductor chip. The failure phenomenon by the PC test can occur in not only the package area but also the semiconductor chip area [42-46].

There are provoked failure mechanisms that can occur in the PC test [47]: bond wire fatigue, solder fatigue, metallization reconstruction, gate oxide failure, and burnout failure. A device under test for the PC test consists of a power semiconductor device and a heat sink structure. The bond wire fatigue and the solder fatigue are the predominant failure mechanisms in the power devices. Although these two are observed outside a power semiconductor chip, the other three failure modes are related to the power chip. These various failure mechanisms reflect the underlying device technology. To date, studies on the failure mechanism by the PC test have been conducted mainly with Si-based power devices such as IGBT or MOSFET [38-48].

1.3.3. RELIABILITY OF GAN HEMTS

The reliability of commercial power GaN HEMTs can be one of the biggest challenges to occupy the new or current power electronics markets [49]. Some companies are performing their reliability tests for their products based on Joint Electron Device Engineering Council (JEDEC) standard. Table 1-4 exhibits the qualification results of

Test items	EPC	Transphorm	Panasonic	GaN Systems
High temperature reverse bias (HTRB)	Pass	Pass	Pass	Under qualifying
High temperature gate bias (HTGB)	Pass	-	Pass	
High temperature storage life (HTS)	Pass	Pass	Pass	
High temperature high humidity reverse bias (H3TRB)	Pass	-	Pass	
Temperature cycling test (TC)	Pass	Pass	Pass	
Power cycling test (PC)	Pass	Pass	Pass	
Highly accelerated temperature and humidity test (HAST)	-	Pass	-	

Table 1- 4 The qualification results of major products from the manufactures [50-53].

major products from the manufactures: EPC, Transphorm, Panasonic, and GaN Systems [50-53]. Their reliability qualification is work in progress in the first half of

2018 and will be continuously updated. The reliability reports of EPC and Panasonic corporation particularly include the electrostatic discharge (ESD) test results. In case of GaN Systems, they announce that their devices success beyond ten times of JEDEC requirements [53] and do not release in detail reports yet. In spite of these various efforts, one remaining question for this reliability assessment is "Is the existing JEDEC standard sufficient to ensure the reliability of the current power GaN devices ?" [49, 54].

The mainstream standards of significant power devices are providing reliability assessment methods and verification criteria [55-57]. They reflect the enormous knowledge and experiments accumulated over the last few decades. Basic reliability research for the standards is based on finding various failure modes and lifetime models against a couple of stress sources. Actually, the conventional investigation mostly had been implemented with Si-based devices. Due to these standards, many Si-based power device manufacturers have been able to stably supply their products to the market. The qualification standards have been very mature for Si-based power devices.

There is a new movement to develop the specific qualification standard oriented to power GaN devices. Most reliability standards including JEDEC was established by

Si device procedures [55-57] so that the conventional evaluation methodologies need to be extended to be appropriate for power GaN HEMTs. GaN Standards for Power Electronics Conversion Devices Working Group (GaNSPEC DWG) that comprises industry experts is leading this action [58]. Their objectives are to create standards and guidelines for test methods, reliability & qualification procedures, and datasheet parametric for power GaN devices. They are working closely with JC-70.1 the new committee involved in a GaN device in JEDEC [59]. Hence, we will soon see the new JEDEC standard for a power GaN device and products satisfied by the standard on the market.

Besides, new possible failure modes of GaN HEMTs have to be taken into consideration [54]. GaN HEMTs employing 2DEG have a fundamentally different structure from Si MOSFET or IGBT using p and n junctions. Apart from a semiconductor part, package technologies they use also are challenging compared to conventional packages of power devices. LGA and GaNPX are package technologies without a bond-wire that do not apply to other Si-based or SiC-based discrete power devices. There already had been many studies on the failure phenomenon confirmed distinctively in GaN HEMT technology [60-62]. Therefore, the reliability of power GaN HEMTs has to be investigated in various degrees outside of the Si device range.

The market always wants power devices to have better performance than the present. One of the GaN device performances the power electronics market expects for the future may be the higher operation junction temperature over 150 Celcius degrees [63]. All Si-based semiconductor cannot be used over the 150 Celcius degrees due to the intrinsic property of Si material, while GaN HEMT is able to operate over the temperature [64]. If the temperature limitation of power device can increase, it can efficientively reduce the complex thermal management structure that occupies a large area in overall power systems [65]. Electric vehicles (EV) applications are interested in this performance [63]. Nevertheless, raising the operating temperature should cause the severe reliability problems. For these reasons, GaN HMETs also require constant research regarding the reliability with high temperature.

1.4. THESIS OBJECTIVES

1.4.1. RESEARCH QUESTIONS AND OBJECTIVES

The fundamental goal of this thesis is to understand the GaN device technology in power applications. Power GaN devices are standing at the beginning of their long journey, considering the entire history of Si power devices until now. In spite of the enormous interest in the GaN devices from power electronics engineers, their present market share of power applications is not high. But, as the new markets that need GaN devices will progressively emerge and expand, their market prospects are up-and-coming. New various techniques have been applied to GaN HEMTs with a sudden change of the market. These new attempts have not been studied enough to convince

the market. Therefore, these cutting-edge techniques should be deeply investigated for GaN HEMTs to succeed in the power electronics market.

Two big topics to describe the device technology should be electrical performance and reliability of GaN HEMTs in power electronics applications. It is known that the electrical performance of GaN devices can theoretically go beyond SiC as well as Si. We can understand the matured GaN device technology at present with commercial GaN devices. Considering the reliability of power electronics systems, the robustness of the GaN device against thermo-mechanical stress is essential to convince the market. Unfortunately, possible failure mechanisms related to GaN devices against the thermo-mechanical stress have not been sufficiently investigated yet. Besides, for better performance and reliability of GaN HEMTs for the future, various design and structural factors of the devices also should be multiply analyzed here and now. Taking into account the needs for investigating GaN device technologies, the following research questions are raised:

1. Where has been a current location of commercial GaN devices on the way to their theoretical limit?

2. How to evaluate the robustness of a commercial power GaN device with an advanced electrical performance against thermo-mechanical stress?

3. What are failure mechanisms of a commercial power GaN device regarding thermo-mechanical stress? And, is there any possible failure phenomenon that uniquely happens in GaN devices regarding that stress?

4. What are the primary factors of power GaN devices to optimize their electrical performance and reliability?

To answer for the above research questions, studies on the performance, reliability, and optimization of GaN devices are performed.

The primary objectives of this project are

1. To compare the performance of commercial power GaN devices using the FOM.

2. To conduct accelerated power cycling (PC) tests for the selected GaN device and to evaluate the reliability of the tested power GaN device.

3. To analyze the specific failure mechanisms of GaN devices aged by the power cycling test.

4. To find the critical design and structural factors for optimizing performance and reliability of GaN HEMTs.

In this thesis, the performance assessment of the leading commercial power GaN devices is conducted for the first objective. In the result of the assessment, the state-of-the-art commercial GaN device is selected for the PC test, and the accelerated power cycling test with the selected GaN device is carried out for the second objective. The specific failure mechanisms of aged GaN devices is analyzed in detail for third objectives. For the last objective, various design and structural factors that can affect device performance are reviewed based on the literature of conventional GaN HEMTs, and an experiment plan to optimize electrical performance and reliability of a GaN HEMT is proposed.

1.4.2. PROJECT LIMITATIONS AND ASSUMPTIONS

In Chapter 2, seven GaN devices of seven different models on the market have been selected for performance assessment. Electrical characteristics of the power device products in a single model are normally distributed in the specification limits promised by a manufacturer. Some device variation in electrical parameters is to be expected even with the same product. The characteristics measured with one selected devices may not precisely represent the technology of devices due to the distribution. Hence, there can be in a little gap between the measured characteristics and the representative values of each model, but still, key performance characteristics can be compared between devices.

In Chapter 3, the power cycling tests were conducted with only one type and only a restricted number of samples to allow failure mechanism in-depth analysis of the degradation. Stress conditions were accelerated compared to temperature swing in practical operation in the field in PC tests to obtain the results in a reasonable test time. These PC tests had been conducted with the two kinds of temperature swings 100 and 125 Celsius degrees to confirm the failure phenomenon within reasonable test time. A failure phenomenon in the PC test with the relatively lower temperature swing, however, may be different from the failure phenomena observed in the accelerated PC tests. Hence, further PC tests are required with lower temperature swings below 100 degrees Celsius. Besides, during PC tests, electrical characteristics are periodically carried out to diagnose test sample health in a curve tracer machine separated from the PC test circuit. If this measurement result determines a failure, it is difficult to specify the exact number of cycles to the failure because this measurement interval is around thousands of cycles. The studies were focused on failure mechanism analysis.

In Chapter 4, a new failure mechanism, that had not been reported in conventional PC tests with Si-based devices, is observed. Various experiments and analysis were conducted to understand this new failure phenomenon. Although a reasonable failure

mechanism based on the test results and logical analysis was proposed in this thesis, the additional experiment, physical failure analysis using photon emission microscope, and finite element method simulation are currently being investigated, but results are not concluded in this paper.

In Chapter 5, an efficient experiment plan was suggested with statistical analysis and Technology Computer-Aided Design (TCAD) simulation results to optimize electrical performances and reliability of power GaN HEMTs. To finally verify these analysis results, GaN HEMTs that reflect the above experiment plan are being manufactured at Chalmers University of Technology. The evaluation results of the real GaN HEMTs will be discussed and will be published further outside this report.

1.5. OUTLINE OF THE THESIS

The Ph.D. dissertation of six chapters is organized as the follows:

Chapter 1: Introduction

The background and motivation for this research project are demonstrated. The objectives of this project corresponding to the proffered research questions also are presented. Finally, the outline of an entire thesis is explained here.

Chapter 2: Performance assessment of commercial GaN-on-Si discrete power device with a figure of merit

Performances of the selected commercial GaN devices are assessed with two sorts of FOM: $R_{DS(ON)}$ * Area and $R_{DS(ON)}$ * Q_g. For the reliable FOM, electrical parameters of the selected commercial GaN devices are characterized under the same test environment. Each parameter by devices is defined under the consistent concept proposed in this chapter. Decapsulating discrete devices derive active area information of each device needed in the first FOM. The performances of each device are compared each other with the extracted FOM based on the measured values, and the possibility of power GaN devices is discussed with their theoretical limit.

Chapter 3: Power cycling test for a cutting-edge GaN device in power application

Overall test environment and result analysis for the implemented PC tests are demonstrated in detail. For the PC test environment, the fundamental operating principle and the methodology for monitoring the DUT health aged are presented. In the test results, a failure mechanism confirmed at the end of the test is analyzed with the monitored data and addition physical failure analysis.

Chapter 4: Failure mechanism analysis of off-state drain-to-source leakage current failure in PC test

Newly detected failure phenomenon that has not been reported in the PC tests with Si-based power devices has been introduced. A hypothesis is proposed, and additional experiments and physical failure analysis are implemented to evaluate this hypothesis. Also, various failure mechanisms to be able to provoke this failure are reviewed based on the current literature regarding GaN HEMTs for RF and power applications.

Chapter 5: Optimization of high voltage GaN HEMT for power application

Design factors and structure factors of GaN HEMTs that affect the electrical performance are discussed based device information from the literature and TCAD simulation. Importance of each factor is confirmed with statistical analysis methodology. Finally, an logical experiment plan that reflects significant factors extracted from the importance review result is proposed.

Chapter 6: Conclusion and Future work

This chapter presents the summary, main findings and conclusion of this thesis. Topics for the future research are also discussed.

In the end of the thesis, the published papers during the Ph.D. study period are attached.

1.6. LIST OF THE PUBLICATIONS

A. Journal

[J.1] S. Song, S. Munk-Nielsen, and C. Uhrenfeldt. "Failure mechanism analysis of off-state drain-to-source leakage current failure of a commercial 650 V discrete GaN-on-Si HEMT power device by accelerated power cycling test," Microelectronics Reliability, Vol. 76-77, pp. 539-543, Jul. 2017.

B. Conference

[C.1] S. Song, S. Munk-Nielsen, C. Uhrenfeldt, and I. Trintis, "Performance Assessment of Commercial Gallium Nitride-on-Silicon Discrete Power Devices with Figure of Merit," in Proc. of IEEE Industrial Electronics Society (IECON), pp. 1143-1148, Oct. 2016.

[C.2] S. Song, S. Munk-Nielsen, C. Uhrenfeldt, and I. Trintis, "Failure Mechanism Analysis of a Discrete 650 V Enhancement Mode GaN-on-Si Power Device with

Reverse Conduction Accelerated Power Cycling Test," in Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 756-760, Mar. 2017.

[C.3] S. Song, S. Munk-Nielsen, C. Uhrenfeldt, and K. Pedersen, "Power Cycling Test of a 650 V Discrete GaN-on-Si Power Device with a Laminated Packaging Embedding Technology," in Proc. of IEEE Energy Conversion Congress and Expo (ECCE), pp. 2540-2545, Oct. 2017.

CHAPTER 2. PERFORMANCE ASSESSMENT OF COMMERCIAL GAN ON SI DISCRETE POWER DEVICES WITH A FIGURE OF MERIT

Commercialized GaN devices can provide more compact, fast switching, and more efficient power conversion systems for users compared to Si-based devices. Even though their market share is not high, they are drawing much attention from the market. A FOM is used objectively to assess and compare their performance to other devices. The FOM is expressed by electrical characteristics and actual die area of each device. In this chapter, electrical characteristics of each device measured in the same test environment and the active areas derived by decapsulation of packages are introduced. The performances of commercial GaN devices are evaluated with their FOM based on the measured data. Their development possibility is discussed based on their theoretical limit.

2.1. FOM OF GAN POWER TRANSISTORS

The FOM of power switching devices becomes an objective barometer when a designer of a power conversion system selects a power device [66]. There are two types of FOM that typify the performance of power devices: the specific on-state resistance (R_{sp}) and on-state resistance ($R_{DS(ON)}$) multiplied the gate charge (Q_g) [6]. The R_{sp} is expressed as the product of an $R_{DS(ON)}$ and an active area (A) representing the area of the die actually operating in the package. They are ultimately associated with power efficiency of a power conversion system. Hence, the information helps the user to choose a power device.

- 1st FOM: $R_{DS(ON)} \cdot A = R_{sp}$ ← conduction loss capability
- 2nd FOM: $R_{DS(ON)} \cdot Q_g$.   ← conduction and switching loss capability

The FOM of a power device elucidates its quantitative performance, technology competitive, and potential for development. The performance and technology competitive of power GaN devices can be demonstrated compared to a Si-based device in a similar level of the maximum drain voltage. Also, the possibility of the power GaN devices can be discussed with their theoretical limits introduced in Section 1.1.3. Obtaining the exact FOM is very important because of these various meanings. Although $R_{DS(ON)}$ and Q_g values representing their specific models are basically provided in their datasheet, the difference in measurement methods and measurement conditions can produce unwanted errors in the FOM comparison. Therefore, it is

significant to evaluate their electrical characteristics under the equivalent measurement methodology for the more accurate FOM.

2.2. MEASUREMENT METHODOLOGY

It is essential for a designer of power conversion systems to choose the proper device. A power device selected can directly affect the performance of the entire system. Electrical characteristics and FOM of a power GaN device should be valuable information to pick out them. Choosing representative samples and reasonable test environment are essential to obtain a significative result. In this section, the state-of-the-art commercial GaN devices for evaluation and the environment to test them is introduced.

2.2.1. REVIEW OF TEST SAMPLES

Current commercial GaN devices embody full-grown cutting-edge technologies. Power density and parasitic elements of current GaN devices had been substantially improved when compared to the early products. A complete normally-off operation of a commercial power device had been achieved in power application. The normally-off operation is not required of a GaN HEMT in RF applications. The commercial GaN devices can be divided into an enhancement mode group and a cascode group

Company	Name of sample	Information of samples			
		V_{DS_MX} [a]	V_{GS_MX} [b]	I_{ON} [c]	Package
EPC	EP-30	30	5	60	LGA [26]
	EP-60	60	5	60	
	EP-100	100	5	60	
	EP-200	200	5	8.5	
GaN Systems	GS-100	100	7	90	GaNPX [23]
	GS-650	650	7	30	
Transphorm	TR-600	600	8	17	PQFN [67]

V_{DS_MX}[a]: Drain to source maximum operating voltage
V_{GS_MX}[b]: Gate to source maximum operating voltage
I_{ON}[c]: Continuous drain to source current in on-state at 25 ℃

Table 2- 1 Information of test samples based on data sheet [16,17,28-32].

based on the way to implements the normally-off operating. These two groups are clearly distinguished from each other in electrical characteristics. Improvement of their power density capability is currently underway. The power density of commercial GaN devices can be demonstrated by the comparison of their FOM to the state-of-the-art silicon device. The seven GaN power devices, which are reflected in the state-of-the-art technology of a commercial GaN device, have been assessed. They are built in a grown epitaxial GaN layer on a Si substrate wafer in common and utilize different package solutions by a company.

Table 2-1 displays the critical information for each sample as collected from the datasheets offered by the manufacturers. Commercial GaN device products assure a maximum drain-to-source voltage up to 650 V. Product lines of the GaN devices are distributed widely from 15 V to 650 V of maximum operating voltage. There are not many kinds of the products by voltage rating in the market under 200 V. Most GaN manufactures aim to the 600s V-rated applications. In this chapter, representative voltage levels of commercial GaN devices are firstly decided considering main applications, and then the typical devices in the similar voltage level are selected for electrical characteristics. Package solutions employed by each manufacturer are various, which is to maximize the potential of their GaN transistors.

2.2.2. TEST ENVIRONMENT

The test environment can be divided into the three parts: i) test fixture including a GaN component, ii) measurement instrument, and iii) test conditions. Surface mount device (SMD) type package technology is preferred for most commercial discrete GaN components and is to diminish stray inductance from electrical leads in practical applications. The SMD type components cannot be straight connected to the curve tracer or similar other measurement machines. The curve tracer supports standardized slots: drain, source, and gate. Seven sorts of test fixtures are made up to connect the SMD components to the curve tracer. The fixture consists of a specific PCB corresponding to the footprint of each device and terminal legs that enable the fixture to fit the slot of the curve tracer. An individual SMD GaN component is joined to the
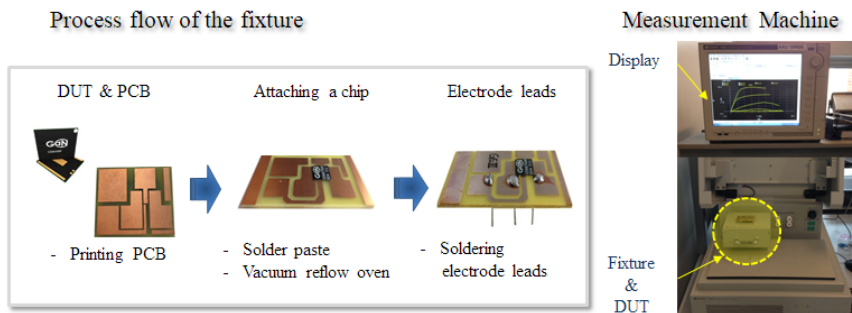
Figure 2- 1 Process flow of the test fixtures and the measurement instrument.
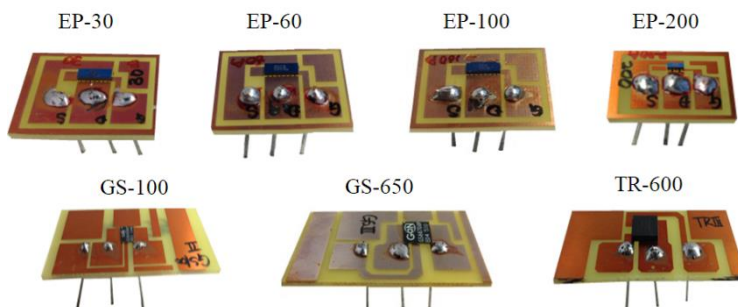
Figure 2- 2 Seven kinds of test fixtures with power GaN devices.

PCB using a SAC305 solder paste and vacuum soldering in a reflow oven. The three leg leads are connected by soldering to a printed copper layer of the PCB. The fixture electrically connects the SMD GaN device to the measurement equipment. Figure 2-1 illustrates an example of the test fixtures, and Figure 2-2 shows the seven test fixtures with power GaN devices.

A curve tracer model B1506 from Keysight Technologies is used to characterize each device electrically [68]. Figure 2-1 also displays the image of the measurement instrument. This instrument enables to measure the following characteristics: the threshold voltages, $R_{DS(ON)}$, off-state leakage currents, capacitances, and Q_g elements. They are vital parameters when assessing the performance of a GaN power device. Especially, $R_{DS(ON)}$ and Q_g are used as the main factors to determine the FOM of the device.

Parameters		Description	Measurement condition
Static	V_{th}	Threshold voltage	$V_{DS} = V_{GS}$, V_{GS} @ $I_{DS} = 0.03 \cdot I_{ON}$
	$R_{DS(ON)}$	On-state resistance	$V_{GS} = *V_{GS\_R(ON)}$, R_{DS} @$I_{DS} = 0.3 \cdot I_{ON}$
	IDSS	Off-state leakage current	$V_{GS} = 0$ V, I_{DS} @$V_{DS} = V_{DS\_MX}$
Dynamic	C_{ISS} C_{OSS} C_{RSS}	Input capacitance Output capacitance Feedback capacitance	$V_{GS} = 0$ V, $V_{DS} = 0.8 \cdot V_{DS\_MX}$
	Q_g	Gate charge	$V_{GS} = 0$ V to $*V_{GS\_R(ON)}$, $V_{DS} = 0.5 \cdot V_{DS\_MX}$

$*V_{GS\_R(ON)}$: The maximum gate driving voltage

Table 2- 2 Test conditions of static and dynamic characteristics.

Electrical test conditions may affect the characteristics of the device. There was a little difference of conditions that decide parameter values in the datasheet of each device [16,17,28-32]. Therefore, they are fine-tuned with a common concept. Table 2-2 shows the electrical test conditions of these characteristics. Definition condition of V_{th} is that the gate-to-source voltage is specified as the gate voltage at $I_{DS} = 0.03$ % · I_{ON} when the gate and drain is the same node. Here, I_{ON} is the continuous current capability of each device in on-state in Table 2-1. The on-state resistance is quantified at the proposed gate voltage on the datasheet and the 30 % of I_{ON}. IDSS is specified by the drain-to-source off-state leakage current at the maximum operating drain voltage in Table 2-1. In the dynamic characteristics, the capacitances are measured at the off-state ($V_{GS} = 0$ V) condition and 80 % of the maximum drain voltage in each datasheet. Q_g is the amount of the gate charge required to increase from zero voltage to the desired driving gate voltage $V_{GS\_R(ON)}$. The initial condition is $V_{GS} = 0$ V and $V_{DS} = 50$ % of V_{DS_MX}, and the total electric charges are calculated while the gate voltage reaches the desired voltage.

2.2.3. ON-STATE RESISTANCE COMPENSATION

The GaN transistor products to be tested in this chapter have a relatively low level of milliohm's resistance, which is seen in the datasheet [16,17,28-32]. The device with a small on-state resistance can be easily influenced by parasitic resistance factors from the test environment. Therefore, compensation of a measured resistance value is required to achieve an accurate result with reasonable way. In this test, the test fixture designed for the measurement of SMD type GaN devices is a major parasitic factor. The fundamental principle of the compensation is to subtract the parasitic resistance from the measured resistance. The below equation (2-1) expresses this compensation principle:

$$R_{DS(ON)\_measurement} - R_{fixture} = R_{DS(ON)} \qquad (2\text{-}1)$$

Five sorts of PCBs are fabricated to evaluate the resistance of each test fixture as shown in Figure 2-3. One universal PCB is used for EP-30, EP-60, and EP-100 because they have the same footprint. The drain and source of a PCB are shorted in these PCBs while holding basic design of the test fixtures. Measured resistance values from the five PCBs are utilized for the compensation of $R_{DS(ON)}$.
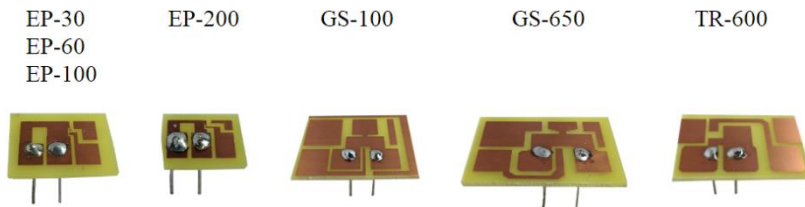
Figure 2- 3 Five PCBs to measure $R_{fixture}$ of each test fixture.

2.3. CHARACTERSTICS OF COMMECITAL GAN POWER DEVICES

2.3.1. STATIC CHARACTERISTICS

The measured static characteristics of each sample are shown in Table 2-3. V_{th} is the minimum gate-to-source voltage to turn a transistor from off-state to on-state. Most of the commercial GaN device except TR-600 have the positive threshold voltage range from 1.28 V to 1.75 V. TR-600 has a little bit higher threshold voltage 2.26 V than other devices because it is the cascode GaN device. The external gate node of this cascode device is connected to the gate of a low-voltage (LV) Si metal-oxide semiconductor field-effect-transistor (MOSFET) inside the device. Consequently, the gate of cascode device behaves much like an LV Si MOSFET [69]. Gate technology for normally-off behavior determines a threshold voltage of GaN devices. It is confirmed that even though four samples from EPC company employ the same gate technology, there is a little more considerable variation among their threshold voltages.

The gate voltage in a measurement of $R_{DS(ON)}$ is very significant because it decides the number of induced charges in the 2DEG channel underneath the gate structure. The gate voltage conditions are based on the datasheet of each device. $R_{DS(ON)}$ data of Table 2-3 is compensated by the measured stray resistances of each test fixture. Entire power loss in a power device consists of conduction loss and switching loss in a power conversion circuit. The on-state resistance $R_{DS(ON)}$ is the primary cause to establish the

Sample	Static characteristics [units]				
	V_{th} [V]	$R_{DS(ON)\_meas.}$ [mΩ]	$R_{fixture\_parastic}$ [mΩ]	$R_{DS(ON)}$ [mΩ]	IDSS [μA]
EP-30	1.52	5.99	5.02	0.97	101.1
EP-60	1.75	6.15		1.13	40.9
EP-100	1.28	6.56		1.54	92.9
EP-200	1.52	37.82	6.19	31.63	6.3
GS-100	1.62	9.03	2.70	6.33	0.5
GS-650	1.50	45.04	2.90	42.14	0.1
TR-600	2.26	153.84	3.24	150.6	2.2

Table 2- 3 Measured static characteristics of tested seven samples in the room temperature.

conduction loss. For this reason, $R_{DS(ON)}$ can be proper criteria for performance evaluation of power devices. $R_{DS(ON)}$ is inversely proportional to the size of the die, IDSS, Q_g and various stray capacitances. Q_g and stray capacitances effect on the switching loss of a power device. Hence, $R_{DS(ON)}$ should be discussed with the dynamic characteristics when a performance of a power device is compared to others.

IDSS means a total flowing current from drain to source, gate, and substrate in the off-state. It is defined in the test conditions: $V_{GS} = 0$ V, $V_{DS} = V_{DS\_MX}$, and the room temperature. It is notable that IDSS of two devices from GaN Systems company is lower than devices of other company. Comparing them within a similar voltage range, IDSS of GS-650 is only 5 % of TR-600, and IDSS of GS-100 is 0.5 % of EP-100. The leakage current of the switching device becomes a source of power loss generated at off-state. Although the power loss at off-state is a small piece of overall power dissipation, these characteristics should be considered by a designer in a precise application asking low standby power consumption [6].

2.3.2. DYNAMIC CHARACTERISTICS

Dynamic characteristics are mainly associated with switching power dissipation in a power conversion system. They can represent the capability for the power systems to switch fast. Stray capacitances of a GaN HEMT are major factors which determine the switching energy loss during a transition from off-state to on-state or vice versa. The capacitances are composed of three elements: gate-to-source (C_{GS}), gate-to-drain (C_{GD}), and drain-to-source (C_{DS}). A datasheet of a power transistor introduces three kinds of capacitances: C_{ISS}, C_{OSS}, and C_{RSS}. C_{ISS} and C_{OSS} are total capacitance seen at the input terminal and output terminal respectively. The below equations show their relationship [70]. Their capacitances are defined in the conditions: $V_{GS} = 0$ V off-state, $V_{DS} = 80$ % $\cdot$ V_{DS_MX}, and 1 MHz frequency.

$$C_{ISS} = C_{GS} + C_{GD} \tag{2-2}$$

$$C_{OSS} = C_{GD} + C_{DS} \tag{2-3}$$

$$C_{RSS} = C_{GD} \tag{2-4}$$

The Q_g and reverse recovery charge (Q_{rr}) are critical parameters which evaluate switching performance of a power device [71-73]. These charge factors are defined by the parasitic capacitances and voltage across both terminals of each capacitor. Q_g is extracted by time integration of current flowing into the gate terminal while a gate voltage is driven from zero to V_{GS_MX} in Table 2-1. The smaller charge characteristics imply a higher operating frequency applying the same driving current from a gate driver.

Table 2-4 displays the measured dynamic characteristics of the individual commercial GaN device. It includes attributes from the datasheet of a state-of-the-art silicon super junction (SJ) MOSFET (FCH077N65F) [74] for performance comparison between

GS-650 and a Si-based power device with similar resistance and current level to GS-650. V_{DS_MX} of the SJ MOSFET is the same as GS-650, and the dynamic characteristics are described following the conditions of Table 2-2. The measurement of GaN devices is carried out by built-in routines of the B1506 curve tracer. It is confirmed by the calibration function of the curve tracer that the parasitic capacitance of each test fixture influences the final measured value.

In the results of the characteristics, the apparent result is that GS-650 has eleven times smaller C_{ISS} than the SJ MOSFET. The difference of Q_g between GS-650 and the SJ MOSFET appears to be like the gap of C_{ISS} because the Q_g is the total integrated charge amount of C_{ISS} from the initial voltage to the desired voltage on the input terminal. GS-650 has nine times smaller Q_g than the SJ MOSFET. Meanwhile, an input terminal of cascode GaN device is connected to LV Si MOSFET. Considering three times bigger $R_{DS(ON)}$ of TR-600, E-mode GaN device GS-650 shows better Q_g performance compared to coscode GaN device (TR-600) in this result.

A Q_{rr} is the reverse recovery charge stored in a body diode of a Si-based MOSFET when the diode turns on. The amount of charge is dissipated when the diode turns off. The source of the power dissipation is minority carriers of each area: P-type body and N-type drain. On the other hands, an E-mode GaN HEMT has no Q_{rr} because there is no minority carrier engaging in conduction. Zero Q_{rr} of the GaN device is a distinct advantage compared to Si-based power devices. However, Q_{rr} of TR-600 a cascode GaN device is not zero due to an intrinsic body diode of a series-connected LV

Sample	$R_{DS(ON)}$ [mΩ]	Dynamic characteristics [units]				
		C_{ISS} [pF]	C_{OSS} [pF]	C_{RSS} [pF]	Q_g [nC]	Q_{rr} [nC]
EP-30	0.97	2418	1437	24.0	21.4	
EP-60	1.13	2200	969	3.9	19.2	
EP-100	1.54	1493	868	4.0	15.1	
EP-200	31.63	260	106	3.2	2.9	-
GS-100	6.33	408	212	30.5	11.0	
GS-650	42.14	289	75	13	14.6	
TR-600	150.6	801	56	8	10.6	54
FCH077N65F	68	4600	96	13	126	900

Table 2- 4 Measured dynamic characteristics of tested seven samples in room temperature with measured static $R_{DS(ON)}$ and characteristics of SJ MOSFET.
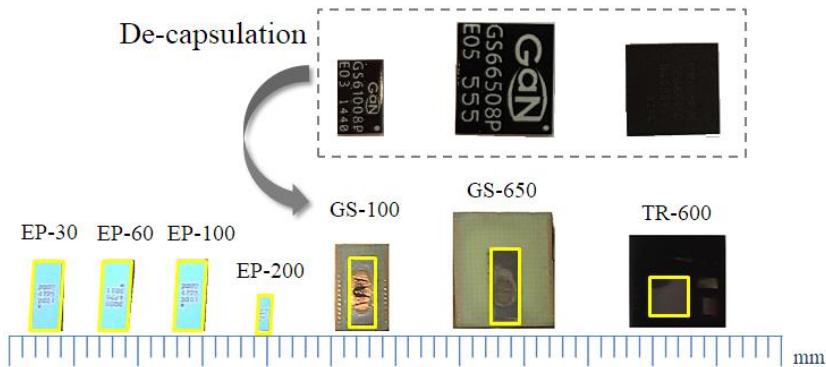
Figure 2- 4 Actual GaN areas of the tested commecial GaN-on-Si device.

MOSFET. Its Q_{rr} can be compared to the SJ Si MOSFET in Table 2-4. This SJ MOSFET has 2.2 times smaller $R_{DS(ON)}$ than TR-600. Nevertheless, the SJ MOSFET has 16.7 times greater Q_{rr} than TR-600. Therefore, the comparisons briefly demonstrate superior dynamic characteristics of a GaN device. Their performance will be discussed with the FOM in detail.

2.3.3. ACTIVE GAN AREA

 In the first FOM in Section 2.1, which represents power density capability of a power device, the area factor means an active area of a power device. There is a difference between the active region and a package size according to package solutions, and this information is not in a datasheet. For an accurate comparison of the FOM, GS-100, GS-650, and TR-600 are mechanically decapsulated using the rotating plate machine with a grinding paper. The four samples of the EPC company employee a land grid array (LGA) package solution. The LGA package is one of the wafer level package technologies, and its active area corresponds to the package size [6]. The active area information of the four samples from EPC Inc. in Table 2-5 is given by each datasheet [16, 28-30]. For the remaining three samples, the exact size is derived using a microscope and an assistant computer program. Figure 2.4 exhibits actual areas of

Unit: cm²	Samples						
	EP-30	EP-60	EP-100	EP-200	GS-100	GS-650	TR-600
Area		0.139		0.019	0.112	0.123	0.104

Table 2- 5 Extracted actual active GaN areas of each devices.

the seven GaN devices used in this chapter. They are marked with a yellow rectangle. Table 2-5 shows the active area of each device.

2.4. FOM OF CUMMERCIAL GAN DEVCIES

A FOM quantitatively expresses the performance of a device or technology. It allows a designer easily to understand how a selected device is better than other devices. There are the two FOM introduced in Section 2.1. They are well-known FOMs to examine the ability of a power transistor. Power density, switching capability, and potential of current commercial GaN devices will be discussed with the FOM calculated by the characteristics shown in the previous sections.

$R_{DS(ON)} \cdot A$ is the FOM which can show the power density of a power device. A smaller FOM means higher power density. This FOM is theoretically proportional to V_{BR} squared in the equation (1.1). The second FOM $R_{DS(ON)} \cdot Q_g$ represents switching ability of a power device. The FOM is the smaller the value, the better the performance. The switching performance of one device can be compared to the FOM of another device having a similar V_{BR}. Moreover, for $R_{DS(ON)} \cdot A$, the possibility of a specific device can be understood with the theoretical limits of each semiconductor material in Figure 2-5. The 2DEG of GaN HEMT becomes an electrical channel in the conduction state. The electron mobility of the 2DEG affects the theoretical limits of a GaN HEMT in the equation (1.1). The electron mobility of 2DEG has different values depending on the device [6, 7, 75]. In Figure 2-5, a value of 1500 $cm^2 / V \cdot s$ [6] is applied as the 2DEG mobility in addition to the 2215 $cm^2 / V \cdot s$ [7] in Table 1-1. These two values are marked as a red area in Figure 2-5. The electron mobility of 900 $cm^2 / V \cdot s$ at GaN in Table 1-1 is lower than 2DEG. For this reason, GaN HEMTs can go beyond the vertical GaN limit of Figure 2-5 for the future.
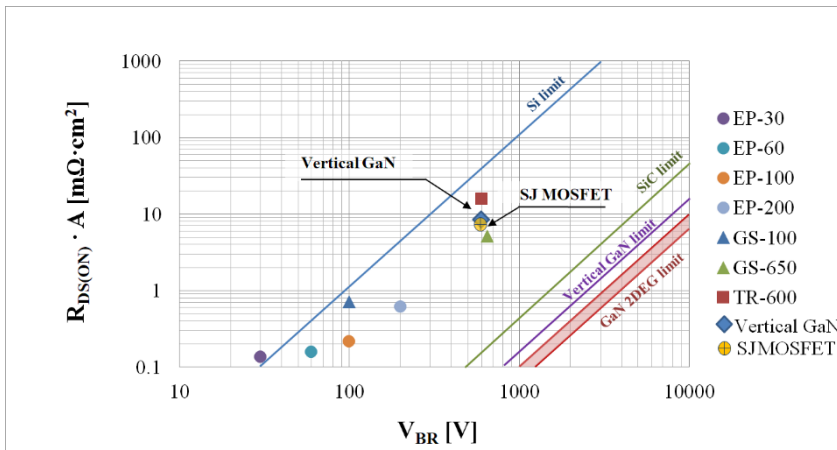
Figure 2- 5 $R_{DS(ON)} \cdot A$ based on measured date versus breakdown voltage for commercial GaN devices.

Figure 2-5 illustrates a correlation between the first FOM the measured $R_{DS(ON)}$ times the confirmed active area and blocking voltage capability of the tested devices. Moreover, it can explain the current point of the commercial GaN HEMT or GaN device technology in a field of a power device. Both axes set as a logarithmic scale easy to understand visually. It shows a definite tendency that $R_{DS(ON)} \cdot A$ of the devices is proportional to blocking voltages of devices in Figure 2-5. These results are consistent with the theoretical background. V_{DS_MX} of each device is substituted for V_{BR} in this analysis.

It is shown in Figure 2-5 that most of the tested commercial GaN devices already have overperformed the Si theoretical limitation. GaN power devices on the plot can be divided into two groups based on V_{DS_MX}: $V_{DS\_MX} \leq 200$ V and 600 V $\leq V_{DS\_MX}$. EPC's have ushered in the market in the first group below 200 V. They have various product lineup in the maximum drain voltage range from 15 V to 200 V. GaN Systems Inc. has a 100 V-rated product GS-100. EP-100 is 3.3 times better than GS-100 in the first FOM comparison. Two GaN products GS-650 and TR-600 are having V_{DS_MX} above 600 V in the graph. In comparison of GS-650 and TR-600, GS-650 an E-mode GaN device shows three times better FOM than a cascode type TR-600. Although the cascode GaN transistor has merit easy to implement the normally-off characteristic, this is disadvantageous regarding $R_{DS(ON)}$ because two devices an LV MOSFET and a D-mode GaN HEMT is connected in series in conduction channel. Thus, it can be seen that different gate technologies can affect the conduction characteristics of the power GaN devices.

Besides, a 600 V-rated vertical GaN device is added to understand the performance difference between a lateral GaN transistor and a vertical GaN transistor. In terms of chip size utilization, the vertical GaN device is more efficient than a lateral-type GaN HEMT when a device designer tries to increase the drain blocking voltage because a drain draft length of the device vertically increases in a thickness direction of a wafer. For this reason, it is advantageous for relatively higher voltage applications. There is one example of vertical GaN transistors in Ref. [76]. The vertical GaN device is far from GaN theoretical limit. GS-650 has the 64 % better FOM compared to the R_{SP} of the vertical GaN device 8.5 m$\Omega \cdot$ cm^2. The device does not reflect the whole vertical GaN transistors. However, A vertical GaN transistor is expected to be more successful in the market above 600 V.

A 600 V-rated SJ MOSFET is also added to understand the performance difference between a cutting-edge Si-based device and GaN HEMTs. The SJ MOSFETs show the excellent performance compared to MOSFET. Die size of the cutting edge SJ MOSFET FCH077N65F introduced in Table 2.4 is not in the datasheet [74], so that the R_{SP} value of the representative SJ MOSFET made from the same manufacturer of FCH077N65F is applied to the graph of Figure 2.5 [138]. The SJ MOSFET also exceed the Si limit of the graph, which is possible because a drain draft length of SJ MOSFET also vertically increases. Compared to the R_{SP} of this SJ MOSFET 7.5 m$\Omega \cdot$ cm^2, GS-650 shows the 45 % better FOM. However, SJ MOSFETs are still widely
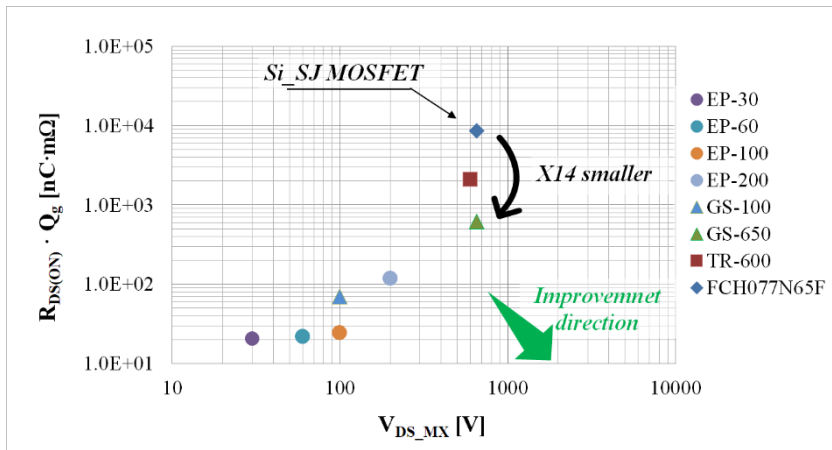
Figure 2- 6 $R_{DS(ON)} \cdot Q_g$ based on measured date versus the maximum drain voltages for commercial GaN devices.

used because they are cheaper to manufacture than GaN HEMTs [9] and can switch faster than IGBTs.

$R_{DS(ON)} \cdot Q_g$ had been introduced as the vital FOM representing the switching ability of a power device in Section 2.1. The smaller the figure, the higher operating frequency can be achieved. Figure 2-6 illustrates that $R_{DS(ON)}$ times Q_g versus V_{DS_MX} of eight kinds of device. FCH077N65F embodies a state-of-the-art Si-based SJ MOSFET. Their fundamental tendency is similar to the results of the first FOM, which is because a charge element indirectly involves an active area factor of a device. The second FOM of EP-100 is 2.9 times smaller than GS-100 in a comparison of 100 V-rated two devices. In the group above 600 V, it is confirmed that there is a somewhat larger chasm of the FOM between a commercial GaN device and the Si MOSFET. GS-650 has fourteen times smaller FOM than the cutting-edge Si MOSFET. Also, a difference between a commercial E-mode GaN and a cascode GaN device is seen on the graph in Figure 2-6. The FOM of GS-650 is three times lower than TR-600. Thus, these results show that switching characteristics of GaN devices basically are better than the cutting-edge Si device, and E-mode GaN has better switching capability than the cascode GaN device.

The current commercial GaN devices show their superior performance in the two kinds of FOM. One of the factors that hindered GaN devices from entering the market a few years ago was the high price. Their cost reduction had processed with some factors such as a wide-diameter GaN-on-Si wafer, mass volume, and yield improvement. Nowadays, the price difference between a commercial GaN transistor and the Si counterpart is not big [54, 77]. The current price 17 euro of GS-650 is twice as expensive as the price 8 euro of FCH077N65F on the online market (MOUSER

Electronics), which shows the gap between them is dramatically narrowing from past years. Moreover, due to diverse technical advances, this gap is expected to narrow further [12]. A GaN device allows a power-conversion system to operate faster. Increasing frequency can dramatically scale down the filter size in the entire system. Therefore, the power system with a GaN device can be greatly minimized [78]. Even though GaN devices had overcome the theoretical limit of Si, their positions stand back far away from their limitation like Si devices did 30 years ago [6]. It means that the power GaN devices are just at the beginning and they have much potential. It can, therefore, be expected that the uses of the commercial GaN devices in the field increase, while their performance will continue to be improved.

2.5. SUMMARY

This chapter has reviewed the electrical characteristics of representative commercial GaN power devices and the performance of them with two kinds of FOM. The seven samples have been selected in various voltage rages below 650 V for the evaluation. To obtain more reliable data, their electrical characteristics have measured in the equivalent test environment and measurement condition. The measurement methodology has been announced in detail. Besides, their actual active areas of each device have confirmed by decapsulating packaged discrete devices to extract the FOM of the GaN devices.

The two kinds of FOM of the GaN devices calculated by the previously measured data here has been proposed to understand their performance and possibility compared to other devices. In the first FOM, it has established that most of the commercial GaN devices evaluated in this chapter have already conquered the theoretical limit of Si devices. The strong development potential of the GaN devices has been described by the long distance from the theoretical limit of a GaN HEMT. In the second FOM, their capability of high-speed operation has been discussed. In the comparison of the 650 V-rated GaN device and the Si counterpart, fourteen times excellent FOM of the GaN device have been seen. Thus, it is confirmed in this investigation that the current commercial GaN devices has not only superior performance but also a good prospect.

CHAPTER 3. POWER CYCLING TEST FOR A CUTTING-EDGE GAN DEVICE IN POWER APPLICATION

GaN HEMT power devices can switch very fast due to their inherent wide-band-gap properties. To fulfill this potential of them, the impact of package technology for a GaN HEMT is very significant. The cutting-edge commercial GaN device is employing the new package technology with a minimal parasitic inductance and an excellent junction-to-case thermal conductive capability. In this chapter, PC test to understand the robustness of the state-of-the-art commercial discrete GaN device against thermo-mechanical stresses has been conducted. A total of six samples have been tested with two temperature swing condicions. After the end of test, failure mechanism of the samples also is analyzed through various means.

3.1. POWER CYCLING TEST FOR A GAN DEVICE

Power switching devices play a leading role in determining the reliability of power electronics systems. A power conversion system uses various components: capacitors, resistors, gate drivers, inductors, power switching devices, etc. There had been an industry-based survey asking which device is the weakest of your power systems. In the result of this, failure of a power switching device occupied the most significant portion at thirty-four percentage [36]. It had been confirmed in the Ref. [79] that the primary stress source of their failures is thermo-mechanical stress. Thus, it is vital to study the reliability of the power devices against this stress for a durable power conversion system.

PC test is the most common thermal-accelerated test to evaluate the reliability of a power switching device. The behaviour of the PC test is close to a real operation because of using power dissipation inside the device for a heat source. A DUT with a heatsink structure consists of various parts made of different materials, and each element is having its intrinsic coefficient temperature expansion (CTE). Thus, thermo-mechanical stress is generated by the CTE mismatch between each component in the PC test. In the PC test, a single cycle divides into heating and cooling periods. These materials expand during the heating period and contract during the cooling period, respectively. The DUT suffers from repeated thermo-mechanical stresses during PC test.

For examing the robustness of power devices in the field, it is imperative to explore failure mechanism by the PC test. There had been various studies on PC tests with Si-based power devices for the last few decades. In these studies, the failure mechanism

and lifetime of the device can be affected by various factors: test strategy, stress condition, package type, etc. Bond wire fatigue, metalization reconstruction, and solder joint fatigue had been reported as main causes of the failure by PC test in Ref. [80-86]. Despite numerous research on PC test, few studies on the reliability of the GaN devices using a LGA package by thermo-mechanical stress found in the literature [141]. A commercial GaN HEMT differs from conventional power semiconductor devices in a couple of ways: target application, operation principle, and package technology. To succeed in the market, a new study on a PC test with a GaN device is necessary. A new study is required for the success of commercial GaN HEMTs on the market [54].

In this chapter, PC test with a commercial GaN HEMT device has been conducted, and failure phenomena by the test have been analyzed. GS-650 from GaN systems Inc. had been selected for the PC test. The device has the highest breakdown voltage of the GaN device market and shows excellent performance index in Chapter 2. Moreover, it employs the enhanced package technology without a bond wire. Although this product has better performance compared to other Si-based power device products, there have been few studies on their reliability. The reliability and failure mechanism by PC test of the cutting edge GaN device will be discussed.

3.2. BIDIRECTION CONDUCTIVE ADVANTAGE OF A GAN HEMT

A power switching device needs a bidirectionally conductive function in most switching power-conversion circuits, which is to protect the switching device from a reverse current flow during freewheeling action. Thus, a capability of reverse conduction as well as the forward conduction character is significant. A Si IGBT, Si MOSFET, and SiC MOSFET are conventional switching devices in the power electronics. A IGBT has a unidirectional current carring capability, so that it needs a exteral diode for the reverse conduction. Si and SiC MOSFETs can provide the reverse conduction with an intrinsic body diode. However, they often utilize additional diodes, such as a fast recovery diode or Schottky diode, to satisfy desired reverse recovery performance in specific applications [87, 88]. This structure of co-packaging two chips results in increaing the cost, the device volume, and the paracitic capacitance between the drain and the source. However, an E-mode GaN HEMT is not only naturally capable of reverse conduction like the Schottky diode without any addtional diode [89, 90] but also does have no reverse recovery charge, which is an additional virtue of the E-mode GaN device.

An E-mode GaN HEMT itself can support good reverse conduction as well as forward characteristics with no reverse recovery charge. The good forward conduction feature of the E-mode GaN HEMT is thanks to a 2DEG layer the main path of a channel between the drain and source. As using the same path in the reverse conduction, the reverse conduction can have the same conductivity to the forward. Besides, there is
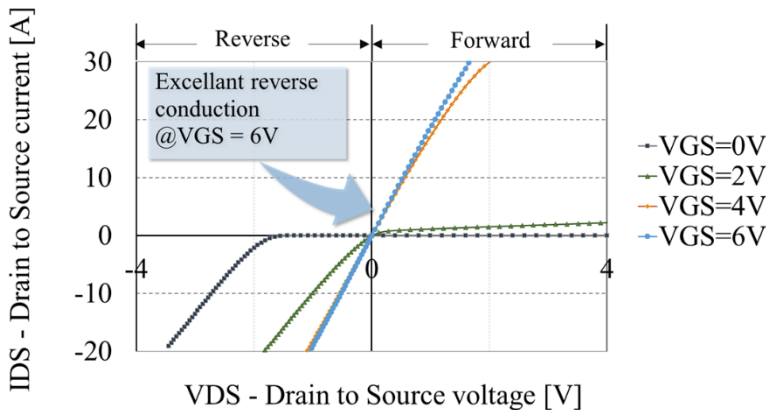
Figure 3- 1 Measured V_{DS} Vs. I_{DS} curve of a commercial E-mode 650 V GaN device.

no reverse recovery charge of E-mode HEMTs that contributes to the switching loss because there are no minority carriers involved in the 2DEG conduction. Figure 3-1 exhibit measured bidirectional conductivity characteristics of a commercial E-mode 650 V-rated GaN device [17]. The GaN device behaves like a reverse diode when the gate-to-source voltage is zero. In this case, the device has a voltage drop similar to its threshold voltage. The voltage drop is two times higher than a built-in voltage of a PN junction diode. It can be eliminated as the device turns on with six volts of gate-to-source voltage (V_{GS}). In $V_{GS} = 6$ V, the reverse conductivity is the same with the forward conductivity without any voltage drop [25], which is shown in the graph of Figure 3-1. This operating strategy can be similarly utilized in a Si or SiC MOSFET. In contrast, in comparison to an IGBT, which should depend on a freewheeling diode in the reverse conduction operating, this solution can improve a reverse conduction loss. The excellent reverse conductive ability without any other component and zero reverse recovery charge are crucial benefits of a power GaN device. This advantage is maximized in a particular application such as a motor driver [6, 91]. The device measured in Figure 3-1 is the same model of devices to PC-test in this chapter.

3.3. POWER CYCLING TEST SETUP

A PC test setup can be divided into four parts: a PC test circuit, a device under test (DUT), online measurement, and offline measurement. The PC test circuit has to control the current following through a DUT to generate wanted temperature swings. Measured data allow diagnosing the failure of a DUT with specific criteria. The monitored data during PC test will be able to be substantial evidence for failure analysis after the test.

	Bottom cooling package	**Top cooling package**
Top side	GaN GS66508P E04 51U	GS66508T E0108N 5 4 Y — Thermal pad
Bottom side	— Thermal pad	
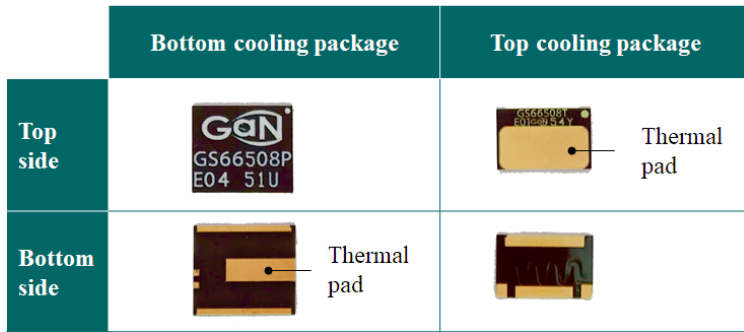
Figure 3- 2 Bottom side cooling and top side cooling packages of a commercial GaN device from GaN Systems Inc.

3.3.1. DEVICE UNDER TEST

A DUT for PC test consists of a discrete power GaN device mounted on a thermal management structure. A 650 V-rated E-mode GaN-on-Si device from GaN systems Inc. is used as a power device for the test. The product supports two types of package: top-side and bottom-side cooling packages. The difference between both of them is exhibited in Figure 3-2. A thermal pad in the figure serves as a significant path for transferring the heat generated in the die to the outside. GS66508P with the bottom side cooling package has been used in this PC test. The device allows measuring top surface temperature of the device on the opposite side with an infrared (IR) camera during PC test because all electrodes and a thermal pad (TPAD) are located on the bottom surface. In case of the top cooling package, measuring temperature in this way is difficult.

The discrete GaN component going to be tested needs not only efficient thermal transfer from the semiconductor chip to a heat sink but also electrical connections to the PC test circuit. An Al PCB can provide both functions. It is composed of a thin Cu layer on the top side, a thin dielectric polymer layer in the middle, and a thick Al layer on the bottom side [92]. The Cu layer is divided into the specific patterns to provide the desired electrical connections. The discrete GaN component and four customized Cu leads are soldered on the Cu patterns of the Al PCB with lead-free SnAgCu solder alloy (SAC305). The leads are compatible with offline measurement instrument as well as the PC test circuit. The DUT is finally completed as the structure of the chip and Al PCB is placed on a big Al heat sink with thermal interface material (TIM). The CTE of Al PCB is higher than Direct Bond Copper (DBC) so that it is not the best choice in terms of thermo-mechanical stress. However, an Al PCB is selected for this experiment in consideration of low price, high thermal conductivity, and ease of manufacture. Figure 3-3 display a cross-section of a DUT 3D model and a real image of the DUT.

Figure 3- 3 A cross-section image of DUT 3D model and real image of the DUT.
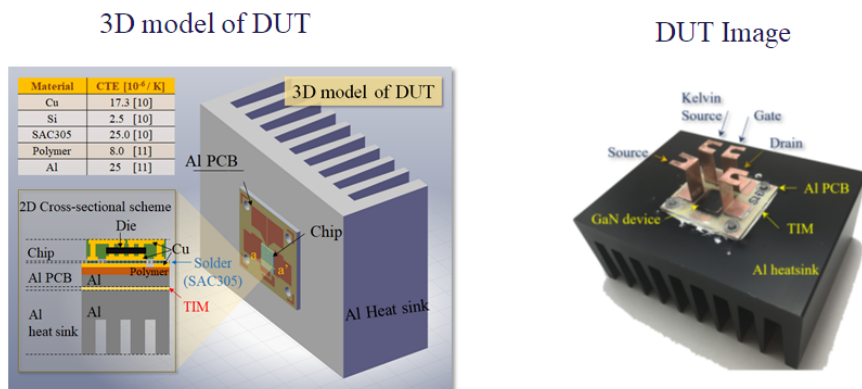
The quality of a solder joint is essential in the PC test because the solder joint fatigue is one of the causes of failures that appear in PC test. For better quality of the solder joint, strict precleaning, solder paste stencil, and vacuum solder processes are employed for the solder joint [93]. The cleaning is to remove a native dioxide copper layer and micro dust between Cu layers and solder. The stencil process is used to ensure a constant amount of solder paste in every sample production. The solder reflow process in the vacuum assures a high-quality solder layer without any void. The void-free quality before the PC test can be confirmed through scanning acoustic microscope (SAM) analysis later in Section 3.5.

Total six samples have been manufactured with the above process for the PC test. The first three samples are PC-tested in reverse conduction, and another three samples are tested in forward conduction. The reverse and forward PC tests are conducted as changing an electrical connection between the DUT and PC test circuit. This method is described in more detail below in the next section.

3.3.2. POWER CYCLING TEST SETUP

A PC test setup can be explained as divided into three parts: the PC circuit, DUT, and online measurement. PC test uses heat generated by power consumption in a power device, which resembles the operation in a real application. Figure 3-4 illustrates a configuration of the PC test setup. DC PC methodology is selected in this PC test [48, 94] where a tested power device does not be directly switched. The PC test circuit applies a specific constant current I_{load} to the power device in pulse form.

In the PC test, the PC circuit controls load current conducted by the power GaN device in the DUT with two Si MOSFETs: MOS_DUT and MOS_BYP. When MOS_DUT
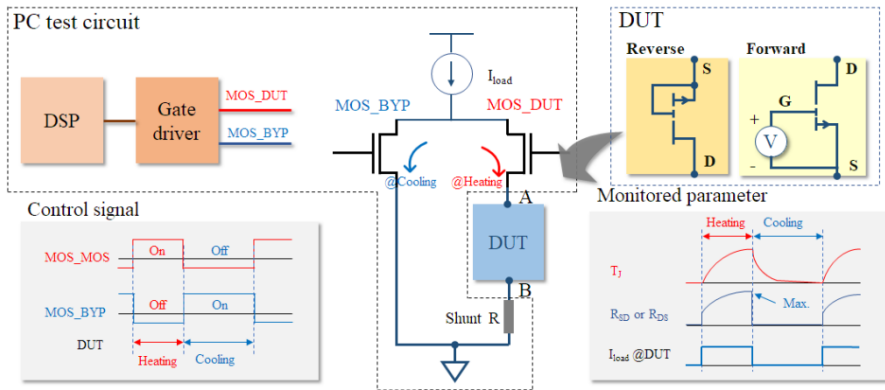
Figure 3- 4 Configuration of PC test setup: A PC test circuit, a DUT, control signal, and monitored parameters.

turns on, power loss in the GaN device produces during the heating period of a single PC. MOS_BYP turns off at this time. At the end of the heating period, the temperature of the power device has reached the maximum value of targeted temperature swing in the PC test. In the cooling period, MOS_DUT cuts off the current injected into the GaN device, and the current bypasses the turned-on MOS_BYP. The heatsink cools the heated device during the cooling period. The control pulse signals are created from digital signal processing (DSP). The two MOSFETs are controlled by the signals amplified by a gate driver. The two MOSFETs should have higher current capability than the tested power GaN device. They are also mounted on a large Al heat sink. Ultimately, this circuit allows the DUT to experience periodic desired temperature swings during the PC test.

In PC test for an E-mode GaN HEMT, the DUT can be electrically connected to the PC circuit in two ways: i) forward conduction and ii) reverse conduction. In the forward conduction PC test, a DUT is kept in on-status with gate-to-source voltage (V_{GS}) = 5 V during the PC test, which is similar to a turned-on condition of a power device in power conversion application. In the reverse conduction PC test, the connection method is changed. In this case, there is no voltage difference between the gate and source electrode. An E-mode GaN HEMT can also conduct in the reverse direction when the gate voltage is higher than the drain voltage by the threshold voltage of the device. Therefore, gate and source electrodes should be connected to the A node in Figure 3-4, and the drain of the GaN HEMT should be connected to the B node in the PC circuit. The connections reflect reverse conduction operation in the device inactivation state. Through these two types of connections, a bidirectional PC test can be implemented on a single PC circuit.
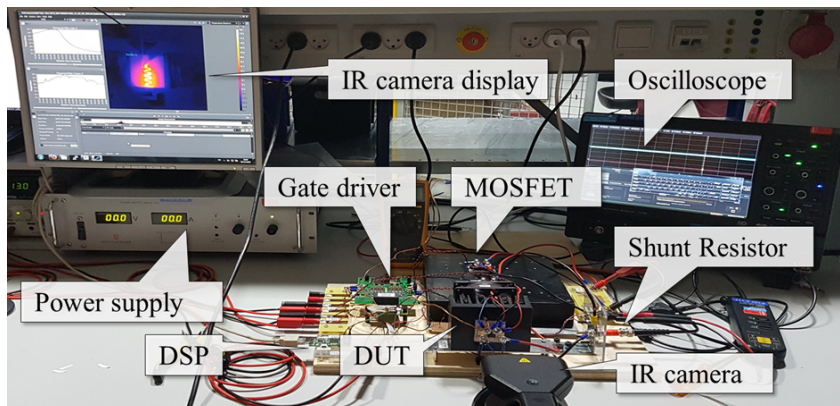
Figure 3- 5 A PC test setup.

This PC test setup can monitor three parameters: load current, a voltage drop between the node A and B in Figure 3-4, and the temperature of a tested GaN device. The load current is supplied in a constant current mode of a power supplier. A shunt resistor is connected in series between the B node and ground potential for collecting the exact current value. The voltage difference between the two ends of the resistor is read through the oscilloscope. Thus, the load current can be calculated with the measured voltage and a known resistance of the shunt resistor. The measured voltage difference between A and B nodes in Figure 3-4 becomes drain-to-source voltage of the GaN device in forwarding conduction PC test and source-to-drain voltage in reverse conduction PC test. The oscilloscope measures this voltage with active differential probes during the PC test. The resistance between A and B nodes is calculated by the measured voltage divided by the measured load current. The resistance increases similarly to the thermal waveform in Figure 3-4 in the heating period because $R_{DS(ON)}$ of the GaN device GS66508p used for this PC test has a temperature coefficient of approximately 0.013 / °C [23]. The maximum resistance (R_{DS_MX} or R_{SD_MX}) of the tested power GaN devices in heating is monitored. The resistance change can become an excellent indicator to detect thermal resistance fatigue. Figure 3-5 shows the PC test setup based on the previous explanation.

Thermo-mechanical stress is a major stress source of the PC test so that it is significant to monitor a temperature of the GaN device. The temperature is scanned on the top-side surface of a GaNPX-packaged GaN device using a high-performance infrared (IR) camera. Temperature measurement environment is explained well in Figure 3-6. Thermographic images from the IR camera is analyzed in the specific program provided by the camera manufacturer. The pictures are recorded at 60 frames per second (fps). T_J is expressed as the average value of temperatures on the line in the thermographic image of Figure 3-6. Although the measured temperature, in general, is lower than the actual junction temperature, results in Ref. [25] shows that the
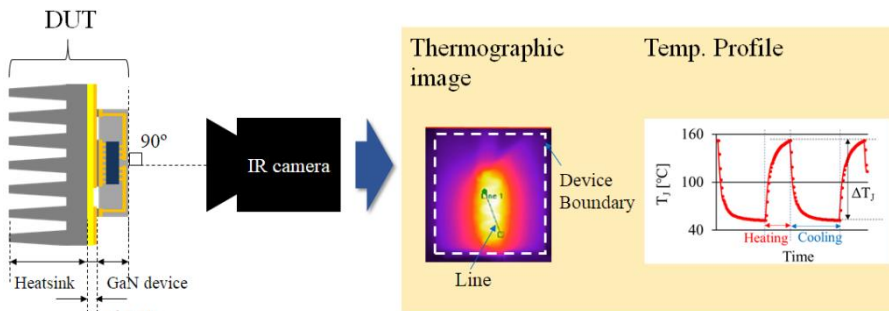
Figure 3- 6 Temperature measurement environment with IR camera, a thermographic image, and temperature profile.

temperature measured in this way is very close to the junction temperature. It might be thanks to a thin-structural feature of GaNpx package. A distance from the top surface of a GaN HEMT chip might top surface of the package might be short considering 0.45 um thickness of the packaged device. Moreover, both surfaces are connected by many micro Cu vias possessing highly thermally conductive. Ref. [25] describes that the junction temperature of a thermal simulation is around 4 % higher than top-side measured temperature with an IR camera in a real experiment. The simulation and experiment were carried out under the same power loss and static condition. The width of the temperature swing that occurs during the PC test is expressed as ΔT_J. It represents directly thermal resistance change of the tested DUT. These two elements mentioned above; R_{DS_MX} or R_{SD_MX} and ΔT_J, are classified as online parameters in this experiment.

3.3.3. PERIODIC DEVICE CHARACTERISTICS IN OFFLINE TO PC TEST

Periodic characteristics of a DUT in the offline is performed in a curve tracer Keysight's B1505A [95] during PC test. V_{th}, $R_{DS(ON)}$, and IDSS are monitored at the room temperature. Table 2-2 in the previous chapter provides measurement descriptions and conditions that define them. For the offline characteristics, the DUT is detached from the PC circuit. Figure 3-7 displays the offline test environment. These parameters are also critical indicators to diagnose defective devices alongside the online parameters. However, if the failure is confirmed by the offline parameters, it is hard to define the correct the number of cycles to failure because they are not real-time monitoring. In this case, the range from the previous measurement point to the failure confirmation point is defined as the failure prediction interval. Nevertheless, the data would be crucial information to understand and analyze failure mechanism.
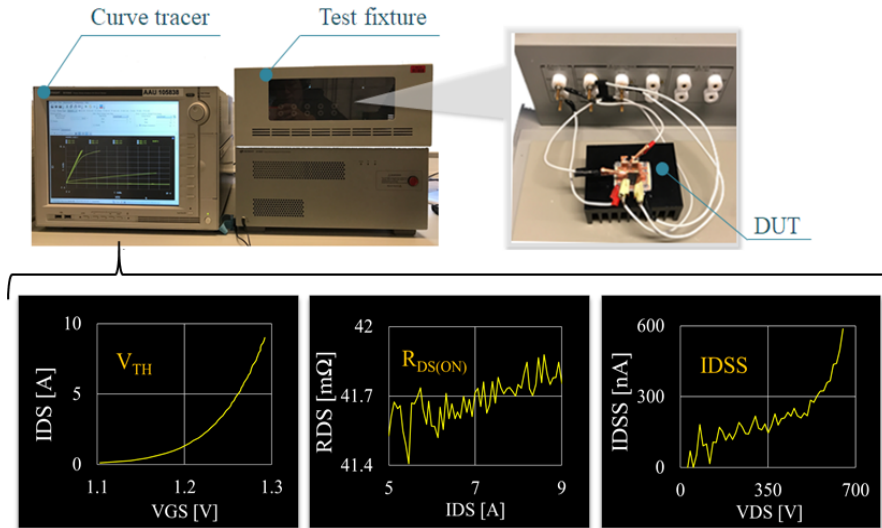
Figure 3- 7 An offline test environment: curve tracer Keysight's B1505A.

3.3.4. FAILURE CRITERIA

Failure criteria of PC test are set with five parameters previously introduced in Table 3-1. The requirements are chosen according to the IEC 60747-9-2007 standard [96]. The initial values of R_{DS_MX} or R_{SD_MX} and ΔT_J in the early stage of the PC test are the basis to determine the degradation of a DUT in the latter stage. And, the values of V_{th}, $R_{DS(ON)}$, and IDSS measured before the PC test are the basis to decide the failure of the tested DUT in the latter stage. If any of them exceed the standard limit during the

Para.	Symbol	Description	Limit
Online	ΔT_J	Temperature swing	Initial + 20 %
	R_{SD_MX} or R_{DS_MX}	Maximum on-state resistance	Initial + 20 %
Offline	V_{th}	Threshold voltage	Initial $\pm$ 20 %
	$R_{DS(ON)}$	On-state resistance	Initial + 20 %
	IDSS	Off-state leakage current	Initial + 100 %

Table 3- 1 The failure criteria of parameters monitored in PC test.

PC test, a DUT is judged to be a failure sample. The limit of each parameter is described in Table 3-1.

3.3.5. OPERATION STRATEGY AND INITIAL STRESS CONDITIONS

It is essential to choose the appropriate strategy for the PC test because the chosen strategy can significantly affect the outcome of the PC test [97]. Ref. [97] presented four kinds of test strategies: ΔT_J, case temperature swing (ΔT_C), power loss, and on/off time = constant. The first three strategies have weaknesses to reflect actual behavior or to identify overall defects of the aged DUT. Whereas, the last strategy 'on/off = constant' indicates the experimental conditions most similar to an actual operation, so that has been chosen for this PC test. Thus, it means that the PC test with this strategy can demonstrate the genuine failure phenomenon that occurs in the field.

In this PC test, the on and off times are fixed at one second and two seconds respectively. The load current to meet the desired temperature maximum (T_{J_MAX}) for one second is set as the initial stress condition. This initional current does not change until the end of the PC test. T_{J_MAX} is targeted around 150 degree Celsius the maximum operating temperature limited by the manufacturer [17]. A DUT heated to 150 degree Celsius is allowed to cool for the next two seconds by heat sink structure. The forward conduction and reverse conduction PC tests have different cooling conditions. While the forward PC test uses an active cooling solution with a fan, the reverse PC test employs a passive cooling solution without a fan. The minimum temperature (T_{J_MIN}) difference between both tests occurs during the cooling period. T_{J_MIN} of the reverse PC test is around 50 degree Celsius while T_{J_MIN} of the forward PC test is close to the room temperature. Eventually, an initial ΔT_J condition of the two types of PC tests is different from each other.

The initial stress conditions of six samples to be examined are summarized in Table 3-2. Three samples with reverse conduction mode have around 100 degree Celsius ΔT_J at the beginning of PC test. In PC test with a REV#2, T_J was not be monitored. In the reverse conduction test group or the forward conduction test group, the initial loading current conditions vary slightly amongst samples. These differences can be originated from electrical resistance characteristics or thermal resistance characteristics of each DUT. The reverse conduction PC tests have around 25 degrees Celsius lower temperature swing than the forwarding conduction PC tests. The different stress condition should affect the number of cycles to failure in individual PC tests.

Sample	Test mode	Temperature swing [°C]			I_{LOAD} [A]
		T_{J_MIN}	T_{J_MAX}	ΔT_J	
REV#1	Reverse conduction	51.1	151.0	99.9	6.66
REV#2		-	-	-	6.53
REV#3		52.3	152.5	100.2	5.53
FWD#1	Forward conduction	23.7	147.9	124.2	17.04
FWD#2		26.2	150.3	124.1	17.16
FWD#3		26.1	146.3	120.2	16.73

Table 3- 2 Initial stress conditions of PC test for six test samples.

3.4. RESULT OF POWER CYCLING TESTS

PC tests of the six samples introduced in Table 3-2 have been conducted to investigate the reliability of the cutting edge GaN power device. Five parameters have been monitored during each PC test. An aged DUT is determined to be defective by the five parameters. At the end of the PC test, failure analysis is performed based on this data. Furthermore, we can discuss the failure phenomenon according to the two different experimental conditions: 1. reverse conduction mode and $\Delta T_J \fallingdotseq 100\ °C$, 2. forward conduction mode and $\Delta T_J \fallingdotseq 125\ °C$.

3.4.1. ONLINE PARAMETER RESULTS OF PC TEST: REVERSE VS. FORWARD CONDUCTION MODE

Figure 3-8 exhibits the online parameters of PC test results under the two different test conditions. For reveiwing the PC test results, REV#1 and FWD#1 have been selected as a representative of each group, respectively. Each graph shows R_{SD_MX} or R_{DS_MX} and ΔT_J simultaneously. The left Y-axis expresses R_{SD_MX} or R_{DS_MX}, and the right Y-axis expresses ΔT_J measured by an IR camera surface measurement. The X-axis represents the number of kilocycles (kcycles).
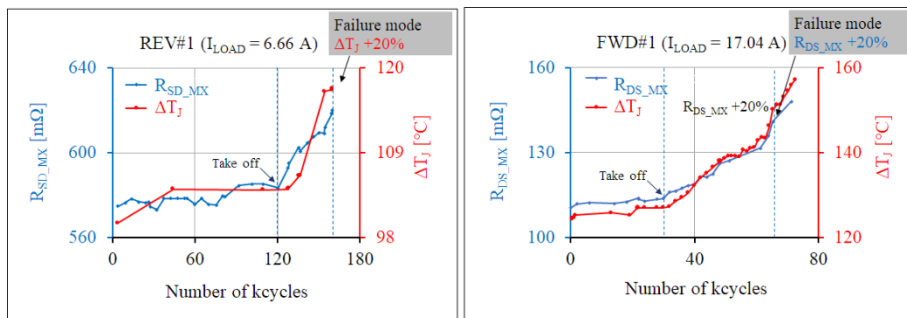
Figure 3- 8 Online parameters of REV#1 Vs. FWD#1 during PC test.

The fundamental trends of the two devices are similar under different test conditions. R_{SD_MX} or R_{DS_MX} and ΔT_J change together because the resistance of a GaN device increases corresponding to the T_J rise [17, 23]. They maintain a constant level until the take-off points in the graphs. After those points, they are gradually increasing to the end of a test. It is observed that the tested six samples have the similar tendency during PC test [93]. Meanwhile, there is a difference in the number of kcycles to failure between $\Delta T_J \fallingdotseq 100$ °C and $\Delta T_J \fallingdotseq 125$ °C conditions. Generally, a larger temperature swing condition results in a shorter lifetime [42].

There can be two causes of the change of online parameters after the take-off point: degradation of electrical resistance or degradation of thermal resistance of the DUT. The different two causes can lead to the same phenomenon, so that we cannot determine which is the primary cause of this degradation with the only online parameters, here. Therefore, the precise failure mechanism will be discussed with offline parameters and additional physical failure analysis (FA) in the later section.

3.4.2. OFFLINE PARAMETER RESULTS OF PC TESTS: REVERSE VS. FORWARD CONDUCTION MODE

Offline parameters should become crucial information to understand failure mechanism by PC test. Three offline parameters V_{th}, $R_{DS(ON)}$, and IDSS have been measured at the room temperature during PC tests. They can sensitively respond to defect of the aged GaN device. The offline measurements had conducted at intervals of around dozens of kcycles. When the failure is detected with these offline parameters, an estimated failure period is defined from the previous measurement point to the failure confirmation point.
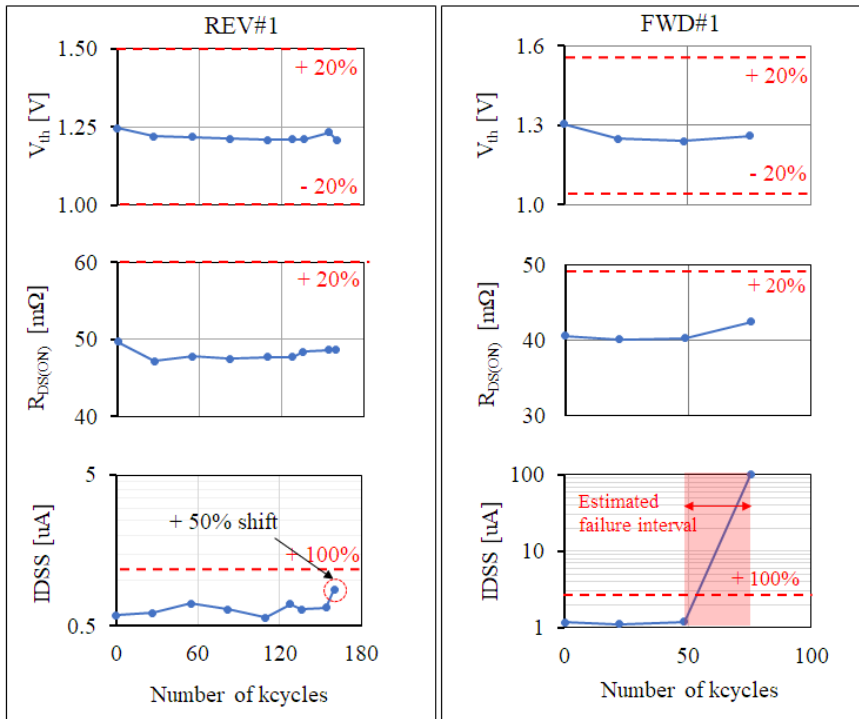
Figure 3- 9 Offline parameters of PC tests of REV#1 Vs. FWD#1.

Figure 3-9 shows the measured offline parameters of REV#1 and FWD#1. There is no observable change in V_{th} of both samples until the end of the PC test. Their $R_{DS(ON)}$ also remains at the same level as an initial measured value at the end of the test. It was, however, observed that online parameters R_{SD_MX} and R_{DS_MX} had definitively shifted after the take-off point. Although these online resistances measured with high-temperature swing had gradually shifted after the take-off point, $R_{DS(ON)}$ measured at the room temperature in the curve tracer has not been changed. It means that there is the only decline of thermal conductivity in the aged DUT without any electrical resistance degadation of the GaN device during the PC tests.

It is indicated that IDSS of the two samples dramatically increases at the end of the test. IDSS of REV#1 does not exceed the failure limit, but it has increased by 50 percent compared to the initial value. There is a remarkable change of IDSS of FWD#1 at the end of the test. The IDSS gets to 0.1 mA the programmed compliance of the curve tracer under the condition V_{DS} = 10 V. It occurs suddenly at the end of the experiment without previous signs. This IDSS failure was found in not only these two but also other samples [93, 98], which shows the correlation between thermo-mechanical stress and this failure.

3.4.3. RESULT SUMMARY

Total six samples have been PC-tested under different two test conditions in Ref. [93, 98]. In the previous two sections, the failure phenomenon had been described in detail with the test results of representative two samples. The experimental results of the remaining four samples also are similar to the previously identified results of REV#1 and FWD#1. The PC test results of all six samples are summarized in Table 3-3.

The numbers of cycles to failure are separated into the two groups according to stress conditions; reverse conduction mode & $\Delta T_J \fallingdotseq$ 100 °C and forward conduction mode & $\Delta T_J \fallingdotseq$ 125 °C. The first group with a less ΔT_J condition has a longer lifetime. In the first group, it is observed that there is the difference between the numbers of cycles to failure of REV#1 and REV#2 and the number of cycles to failure REV#3 under the $\Delta T_J \fallingdotseq$ 100 °C condition. The improved precleaning recipe before soldering was applied to only REV#3 unlike the first two samples (REV#1, REV#2). The improve recipe enhanced with a longer cleaning time, additional cleaning processes, and an ultrasonic cleaner. The difference in these cleaning conditions has an effect on solder bonding quality, which results in the difference of the numbers of cycles to failure. REV#3 shows approximate double longer lifetime compared to REV#1 and REV#2.

Sample	Initial ΔT_J [°C]	No. of cycles to failure	Failure mode	Remark
REV#1 [a]	99.9	160 k	ΔT_J +20%	IDSS +50% @ 160 k
REV#2 [a]	-	74 ~ 106 k	IDSS +100%	
REV#3 [b]	100.2	214 ~ 305 k	IDSS +100%	-
FWD#1 [b]	124.2	49 ~ 73 k	R_{DS_MX} +20% IDSS +100%	-
FWD#2 [b]	124.1	22 k	R_{DS_MX} +20%	IDSS +100% @ 27 k
FWD#3 [b]	120.1	38 k	R_{DS_MX} +20%	-

[a]: Initial precleaning receipe before soldering
[b]: Improved precleaning receipe before soldering

Table 3- 3 Summary from the PC tests results of six samples [93, 98].

In the second group $\Delta T_J \fallingdotseq 100$ ℃, it is shown that the distribution amongst the numbers of cycles to failure of tested devices is large. For all six tests, the wear-out phenomenon of thermal conductivity of samples had been confirmed by the monitored online and offline parameters in common [93, 98]. Failure mechanism of the event will be analyzed in the next section.

It is perceived that IDSS abnormality phenomenon occurs in the five of tested six samples. The dominant failure mode of REV#2, REV#3, and FWD#1 is IDSS failure. Further, Although failure mode of REV#1 is ΔT_J, IDSS has increased by 50 percent at that time. In the case of FWD#2, IDSS failure occurs after R_{DS_MX} exceeding + 20 percent. These results suggest that the IDSS failure is highly correlated with the PC test. The IDSS failure mechanism will be investigated in the next chapter.

3.5. FAILURE ANALYSIS OF AGED DEVICES BY POWER CYCLING

In the result of the previous PC test, it is observed that thermal resistance of the aged DUT is gradually degraded from the take-off point to the end of PC test. The solder joint fatigue is the primary cause of failure in conventional PC tests [99]. The DUT has solder joint between a discrete GaN chip and Al PCB. The state of solder joint before and after PC test can be checked by a scanning acoustic microscope (SAM).

3.5.1. A SCANNING ACOUSTIC MICROSCOPE

SAM is a non-destructive inspection method in physical failure analysis. It can be used to find delamination, cracks, and voids of internal structure. Therefore,
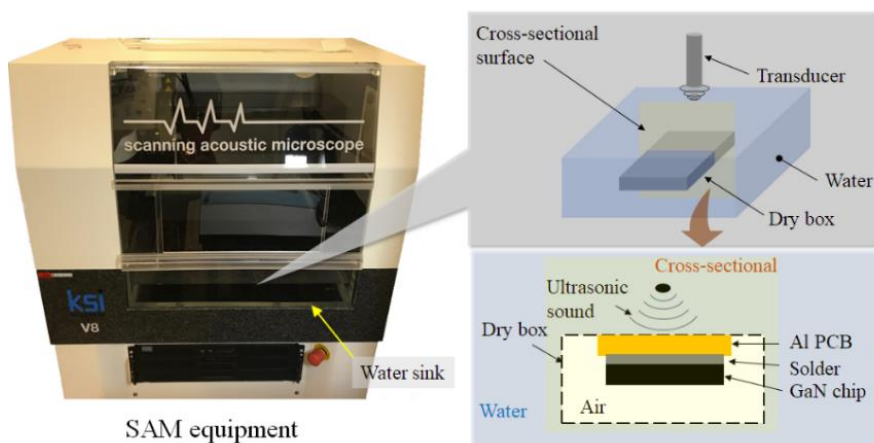
Figure 3- 10 SAM equipment (KSI V-8 from IP Holding) and analysis environment.

comparing the solder joint image before PC test to the aged solder joint after the PC test, the degradation of the solder joint can be confirmed.

Figure 3-10 shows the SAM equipment and analysis environment. Although the method is non-destructively implemented, the sample should be immersed in water. A customized dry box is utilized to eliminate unwanted damage from the water. For scanning the sample is separated from a heat sink. It consists of an Al PCB, solder,
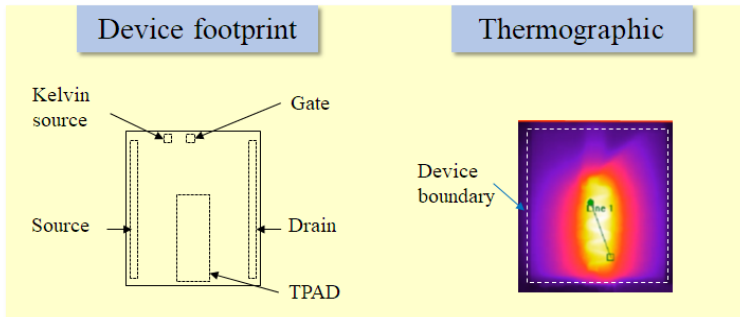
a) Device footprint and the themographic in PC test
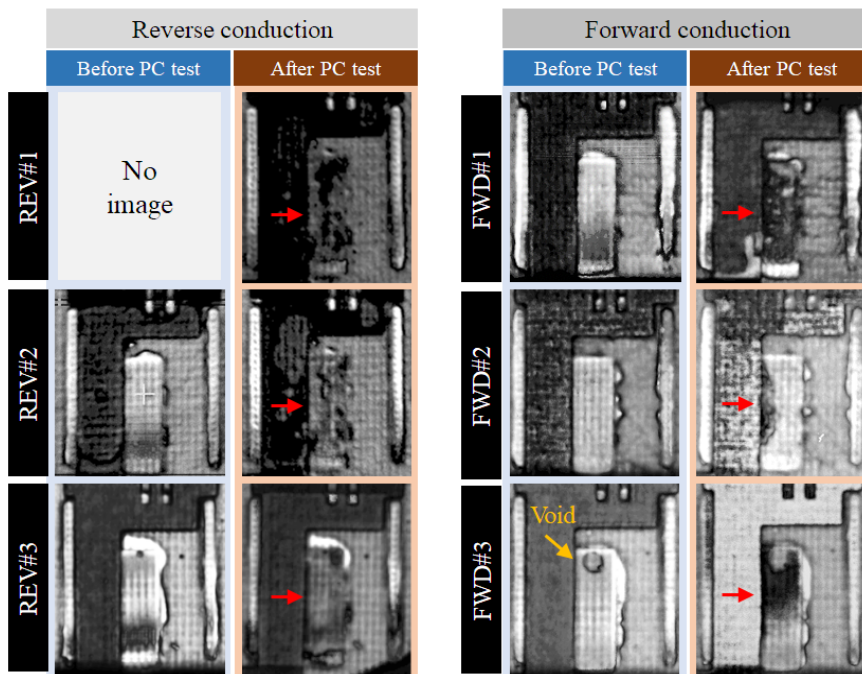
b) SAM images before and after PC test of the tested six samples

Figure 3- 11 a) Device footprint and thermographic in PC test, b) SAM images before and after PC test of the tested six samples.

and a discrete GaN device. The chip is not be contacted with water due to The sample is mounted on the top of the dry box upside down.

3.5.2. FAILURE ANALYSIS WITH SAM

Figure 3-11 displays device footprint, thermographic image from an IR camera, and SAM images of the solder joint before and after PC test. As described above, the heat stress is concentrated in the TPAD region of the discrete GaN component during PC test. In the thermographic and footprint shown in Figure 3-11 a), the heating area overlaps with TPAD. Normal quality of solder layer without any void is shown in the SAM images of REV#2, REV#3, FWD#1, and FWD#2 before PC test. The SAM before PC test of REV#1 is not implemented and FWD#3 has a small void in the image before PC test. In contrast, the solder delamination in the TPAD area is observed in the SAM images after PC test of all samples. Thermo-mechanical stress induced by PC test causes this degradation. Therefore, there has not to be an abnormality in the unstressed other solder layers in electrical interconnections: drain, source, gate, and Kelvin source. In all the images after PC test, normal shapes of solder layers in the areas without thermo-mechanical stress have been confirmed. In conclusion, it is proved that the cause of thermal resistance degradation during PC test is solder delamination in the TPAD.

3.6. SUMMARY

Considering operation characteristics of the cutting edge GaN device, bidirectional PC test is suggested. Total six samples have been PC-tested under different two test conditions. In the results of tests, it is indicated that thermal conductivity is consistently degraded during PC test after a specific point in time, and IDSS failure phenomenon occurs around the end of the test. It has been proven through physical failure analysis that solder delamination created by repeated thermo-mechanical stress during PC test causes the thermal conductivity degradation.

The IDSS failure phenomenon induced by PC test has been newly found. This failure mode is not matched with conventional failure mechanisms originates from PC test. In-depth analysis of this new failure phenomenon, therefore, is required to understand this failure mechanism. The IDSS failure will be discussed in detail with an additional investigation and test in the next chapter.

CHAPTER 4. FAILURE MECHANISM ANALYSIS OF OFF-STATE DRAIN-TO-SOURCE LEAKAGE CURRENT FAILURE IN PC TEST

Unlike conventional failure mechanisms in PC test, the failure phenomenon had been observed in Chapter 3. The primary stress factor in PC test is thermo-mechanical stress. The failure phenomenon should be considered from various perspectives because this failure can be caused by various factors of the aged DUT. In this chapter, different causes provoking the IDSS failure have been stated and reviewed. The reasonable hypothesis of a correlation between solder delamination in TPAD and the IDSS failure will be suggested, and verified by a detailed analysis, supplemental experiments, and SEM analysis. Furthermore, the correlation between this IDSS failure and the stresses generated by PC test will be discussed based on conventional failure mechanisms of GaN HEMTs in the literature.

4.1. IDSS FAILURE MECHANISMS INDUCED BY PC TEST

In Chapter 3, the all online parameters R_{SD_MX} or R_{DS_MX} and ΔT_J increased after PC tests, and it was found that the reason for these increases is the solder fatigue by thermomechanical stress. On the other hand, in offline parameters, the only IDSS failure phenomenon had been found at the end of the PC tests without any change of V_{th} and $R_{DS(ON)}$. These results are identical regardless of the stress conditions or the quality of the solder joint. They are summarized in Figure 4-1 a). The five of the tested six samples had the issue in common. It shows a strong relationship between this failure and PC test. This phenomenon is unlike the phenomenon reported in the PC tests with silicon-based power devices. It is the new failure phenomenon that has not been reported in PC tests. The issue can create severe problems such as short-circuit, which can put the power device itself as well as peripheral elements in danger in the real application [100, 101]. A detailed analysis of the failure mechanism is required to avoid the severe destruction.

This IDSS phenomenon can occur in three locations inside a DUT: the DUT structure excluding a discrete GaN chip, package part excluding a die, and a GaN HEMT die. The DUT is aged by thermal stress over the normal operating temperature and repeated mechanical stress during each cycle. The maximum operating junction temperature of the device limited by the manufacturer is 150 degree Celsius [17]. As seen in Figure 3-8, it is indicated that T_{J_MAX} exceeds 150 degrees Celsius from the take-off point to the end of PC test. This thermal stress can cause electrical

Electric parameter change after PC test
- Online parameter increase : R_{SD_MX} or R_{DS_MX} and ΔT_J
- Offline parameter with no change: $R_{DS(ON)}$ and V_{th}
- Offline parameter increase : IDSS

a) Electric parameter change summary after PC test

Thermal & mechanical stress

DUT
- Solder delamination
- PCB surface contamination

Package
- Dielectric Crack
- Delamination
- Cu via lift-off

Die
- Trap
- Punch through
- Gate edge degradation
- Dielectric layer crack
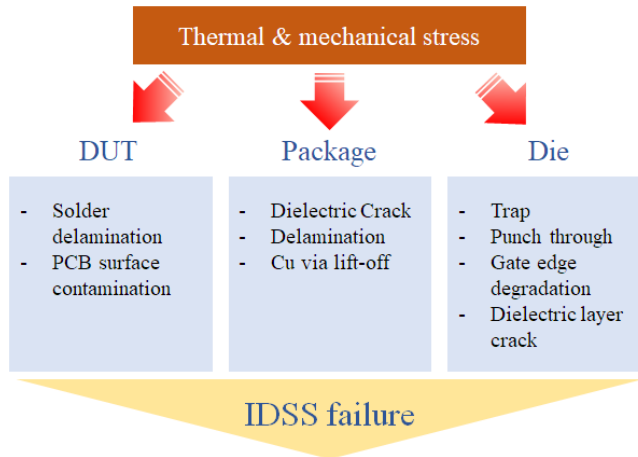
IDSS failure

b) IDSS failure mechanism of a GaN HEMT by thermo-mechanical stress in PC test

Figure 4- 1 a) Electric parameter change summary after PC tests, b) IDSS failure mechanisms of a GaN HEMT by thermo-mechanical stress in PC test.

performance degradation of a GaN HEMT [102-105]. Furthermore, the mechanical stress induced by thermal expansion can also induce various deformation of the aged DUT: lift-off, delamination, and crack. Figure 4-1 b) shows IDSS failure mechanisms that may happen by PC test. Any of the failure mechanisms may cause the IDSS problem.

In this chapter, several possible causes of this IDSS failure in PC test will be analyzed one by one based on the PC test results in Chapter 3, supplemental experiments, and literature. There can be many leakage paths in the previous identified IDSS failure. Therefore, a structured approach to the fundamental cause of this issue is needed. Detailed analysis has been conducted in three areas: DUT excluding the packaged GaN device, package area excluding a GaN HEMT die, and a GaN HEMT die. Notably, a suspected hypothesis that the solder delamination on TPAD results in IDSS failure is presented and tested with targeted analysis methods. In the other areas, possible failure mechanisms have been reviewed with test data and literature information.

4.2. IDSS FAILURE MECHANISM INDUCED BY PC TEST IN A DUT

There is a hypothesis that the complete solder delamination can lead to IDSS failure of a GaN HEMT. Complete solder delamination under the TPAD which cause loss the electrical connection between Si substrate and source potential can have an influence on leakage current in a cut-off state between drain to source, as will be explained in the following. In the SAM images after PC test of Chapter 3, severe damage to solder layer in total TPAD area had been seen. The possible hypothesis supporting this mechanism will be described in detail in this section. Further, it will be verified stage by stage with supplement experiment, electrical measurement, and physical analysis.

4.2.1. HYPOTHESIS: IDSS FAILURE BY SI-SUBSTRATE FLOATING

As instructed by the manufacturer, A Si substrate of a GaN-on-Si HEMT must be connected the source potential to ensure normal behavior [17, 106]. In the discrete GaN component used in Chapter 3, this Si substrate is externally connected to the TPAD via Cu vias and electrically isolated with other electrodes; gate, drain, and source. Thus, the TPAD should be electrically linked with the source potential via solder and the Cu lead-frame on the Al PCB. The solder supplies the electrical potential of the source to the Si substrate and simultaneously transfers the heat in the device to the Al PCB. If it is completely detached from the Al PCB during PC test, the Si substrate of the GaN HEMT becomes electrically floating. In the PC test results, discernible delamination of the solder layer under TPAD had been indicated in Chapter 3.

In the lateral power device such as a GaN HEMT, the electrical connection of the substrate can affect the leakage current measurement at off-state with a higher drain voltage. It can be explained by the unit structure of a GaN HEMT. GaN HEMTs in
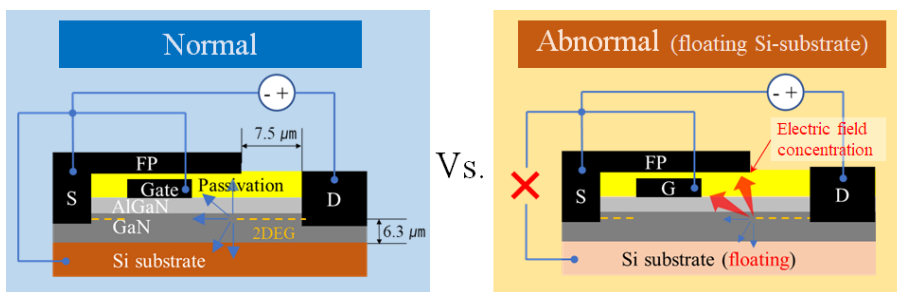
Figure 4- 2 The expected difference of the electric field distributions between the source-connected Si substrate versus the floating Si substrate under a drain-to-source reverse bias condition.

power application have a field plate (FP) located near the gate between the gate and drain to maximize breakdown capability under limited dimension [107]. The FP reduces the concentration of the electric field created by the high bias voltage between the drain and source potential [108]. In GaN-on-Si HEMT structure, Si substrate may play a similar role as the FP. In structural analysis of the same device type as the tested GaN device [109], it is found that the distance between Si substrate and 2DEG channel is very close to 4.3 μm. Considering the distance 7.5 μm between the drain to the edge of the FP in a structure of a GaN HEMT with similar breakdown capability [110], the distance 4.3 μm may be enough to affect the electric field distribution. Figure 4-2 shows the expected difference of the electric field distributions between the source-connected Si substrate versus the floating Si substrate substrate under a drain-to-source reverse bias condition.

The hypothesis is proposed to explain the correlation between the PC test and the IDSS failure. When IDSS failure appears, the harsh solder delamination under TPAD is observed in the SAM analysis. If the defect at the end of PC test is so severe that the electrical connection between TPAD and source potential is cut off, this can be a reasonable cause of the IDSS failure phenomenon. The hypothesis will be verified with additional experiment and failure analysis.

4.2.2. EFFECT OF FLOATING SI SUBSTRATE ON IDSS CHARACTERISTICS

A dedicated experiment has been conducted to prove the impact of the floating Si substrate. A test sample consists of a GaN component of the same model used in the previous PC test and a PCB with TPAD and source separated from each other. After the device is soldered to the PCB, the separate source and TPAD electrodes are short-circuited together by an external wire. In the first step of the experiment, IDSS is ten
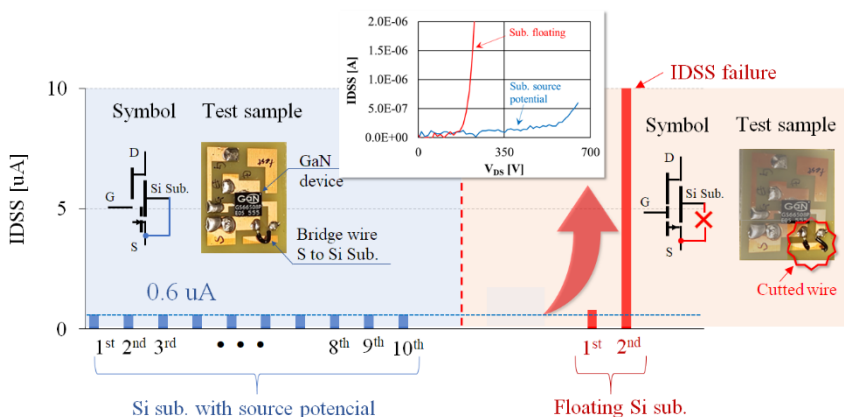
Figure 4- 3 IDSS measurement results at $V_{DS} = 650$ V with source potential Si substrate versus floating Si substrate.

times repeatably measured in the condition of Si substrate connected with the source potential. Subsequently, IDSS will be rechecked under floating Si substrate implemented by cutting the external wire. This experiment is very close to the complete solder delamination environment that may occur in the PC test.

In the experiment result, a significant change of the measured IDSS is detected after the Si substrate lost electrical connection. Figure 4-3 exhibits the IDSS results under source-connected Si substrate and under floating Si substrate, simultaneously. In the first ten measurements, IDSS is in the normal range on a data sheet basis [17]. On the other hand, it is confirmed that the IDSS dramatically increases in the second test after the floating Si substrate. Hence these results support the hypothesis that exhaustive solder delamination brought about by repeated PC can lead to severe IDSS failure. For final verification of the hypothesis, the confirmation of the complete solder delamination, which can cause the floating Si substrate, is required.

4.2.3. THE FLOATING SI SUBSTRATE TESTED USING MEASURED OUTPUT CAPACITANCE

In general, the methods of identifying the failure phenomenon can be classified into non-destructive testing and destructive testing. The non-destructive inspection is always carried out prior to the destructive investigation that produces an irreversible alteration of a sample. The potential loss of the PC-tested DUT can be inferred from monitored electrical characteristics. In this section, a method of identifying the floating Si substrate using the measured output capacitance (C_{OSS}) between before and after PC test will be introduced. It is assumed that the C_{OSS} measurement at a negligible voltage ($V_{DS} = 0.1$ V) gives no additional impact to the failure DUT.
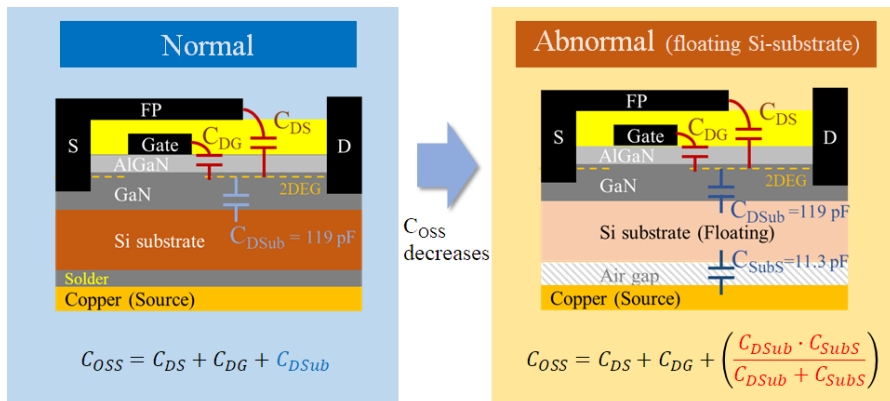
Figure 4- 4 C$_{OSS}$ configuration with source potential on Si substrate versus C$_{OSS}$ configuration with the complete delamination solder under TPAD.

The floating Si substrate can result in a noticeable change in C_{OSS} of the DUT. C_{OSS} is a sum of gate-to-drain capacitance (C_{GD}), drain-to-source capacitance (C_{DS}), and drain-to-substrate capacitance (C_{DSub}). The complete solder delamination decreases C_{DSub}. In the complete delamination, the C_{DSub} in normal condition changes into two capacitors connected in series: C_{DSub} and substrate-to-source capacitance (C_{SubS}). Because of this phenomenon, the capacitance C_{DSub} between the drain and the substrate is reduced in the case of the floating Si substrate. Figure 4-4 displays the composition of the Coss of a GaN HEMT before and after the complete solder delamination. Therefore, the lager the difference between C_{DSub} and C_{SubS}, the more significant the change of the C_{OSS} by the complete solder delamination can be confirmed.

The difference between the C_{OSS} without and with the complete delamination solder can be estimated by measured capacitances, the equations of the Figure 4-4, and assumptions. In Figure 4-4, C_{DSub} of 119 pF is calculated based on the measured capacitance between drain-gate-source terminals and substrate terminal ($C_{SGD-to-Sub}$) and the source-to-gate-to-drain dimension ratio of a unit GaN device; i) $C_{SGD-to-Sub}$ = 142 pF, ii) the dimension ratio (width of source, gate, and drain) = 2.42: 1.38: 19.5 respectively. The $C_{SGD-to-Sub}$ is measured at bias 0.1 V with REV#3 introduced in Chapter 3, and the dimension ratio is confirmed by a cross-sectional image of a unit GaN device from Ref. [9]. In the cross-sectional image of Ref. [9], a 4 μm thick GaN dielectric layer of C_{DSub} between 2DEG to Si substrate also is identified. Assuming area of C_{DSub} and C_{SubS} are the same, and dielectric thickness of both is equal to 4 μm, D_{SubS} capacitance becomes around 11.3 pF 1/9.5 of C_{DSub} depending on the permittivity difference between air (1) and GaN (9.5) [142]. In the first C_{OSS} equation of Figure 4-4, $C_{DS} + C_{DG}$ = 422 pF can be calculated by subtracting C_{DSUB} = 119 pF from the measured C_{OSS} = 541 pF of REV#3. In the second C_{OSS} equation of Figure 4-4, the C_{OSS} of 432 pF with the complete solder delamination with a 4 μm air gap can be calculated with $C_{DS} + C_{DG}$ = 422 pF, C_{DSub} = 119 pF, and C_{SubS} = 11.3 pF. Therefore, it is expected that the difference between the C_{OSS} without and with the complete delamination solder is around 20 % [111].

The consideration of the 20 % difference between the C_{OSS} without and with the complete delamination solder is based on the thickness over 4 μm of the air gap between a TPAD and copper layer. If the air gap thickness is reduced to 0.42 μm, C_{DSub} and C_{SubS} have the same capacitance of 119 pF. In this case, the difference decreases to around 10 %, which should still be observable. The air gap thickness induced by the solder delamination will be discussed with a cross-sectional SEM image in Section 4.2.4.

The C_{OSS} shift after the floating Si substrate can be checked out by using the tested sample in Section 4.2.2. The capacitance measurement has been done twice in total. The measurement condition is V_{GS} = 0 V and V_{DS} = 0.1 V, which to minimize the effect of the DUT from the measurement. Two kinds of Coss in connection and

Sample	C$_{OSS}$ before PC test [pF]	C$_{OSS}$ at the end of PC test [pF]
REV#1	536	531
REV#2	536	544
REV#3	541	-
FWD#1	-	528
FWD#2	-	536
FWD#3	530	526

Table 4- 1 The comparison of measured COSS before PC test and at the end of PC test.

disconnection between the source and Si substrate are 478 pF and 397 pF respectively. The capacitance decreases by 17.0 % after the disconnection, which is in good agreement with the estimation of Ref. [111]. Therefore, it is possible to predict whether or not complete solder delamination has occurred in the aged DUT by comparison between the output capacitance before and after the PC test.

Table 4-1 shows the C$_{OSS}$ measurement results of the PC-tested six devices in the last chapter. The three of DUT which are REV#1, REV#2, and FWD#3 have both before and after values. In their comparison, no significant change in C$_{OSS}$ is observed. For three other samples with missing data, the C$_{OSS}$ value before or after PC test similar to those of the previous three samples. That in turn, therefore, implies that there is no loss of electrical connection due to the complete solder delamination of all the tested DUT at the end of PC test. This analysis result can be reinforced by the additional destructive inspection of the DUT.

4.2.4. CROSS-SECTIONAL ANLYSIS OF THE AGED DUT

A cross-sectional scanning electron microscope (SEM) analysis of the aged DUT visualizes the solder delamination identified in the SAM analysis as a two-dimensional (2D) image. The two samples are prepared with epoxy molding and polishing processes.

Figure 4-5 exhibits cross-sectional SEM images of REV#2 after 106 kcycles and FWD#1 after 73 kcycles, respectively. It is noticeable that complete delamination of the solder layer under TPAD is not confirmed. Apparent degradation is commonly observed in the solder layer underneath TPAD of the two samples. The degradation

a) SAM and Cross-sectional SEM images of REV#2 at the end of PC test

b) SAM and Cross-sectional SEM images of FWD#1 at the end of PC test
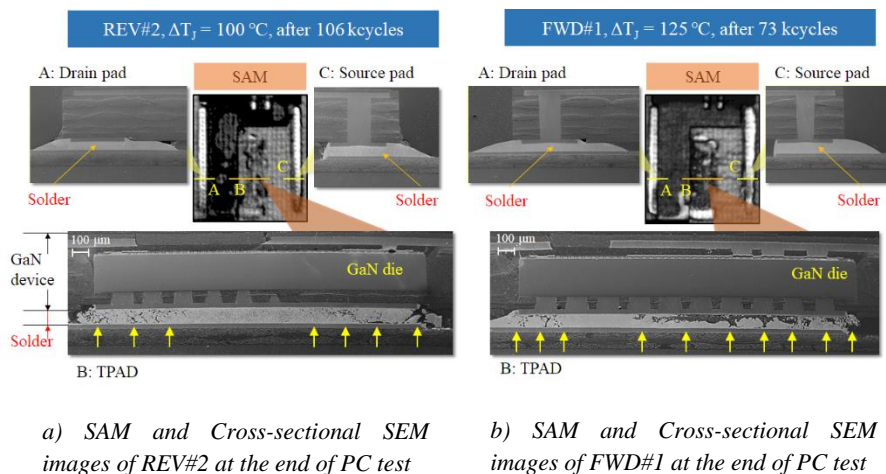
Figure 4- 5 a) SAM and Cross-sectional SEM images of REV#2 and b) FWD#1 at the end of PC test [93, 98].

degree of FWD#1 is worse than REV#2, which is reasonable considering given their different ΔT_J conditions. This structural damage of the solder layer below TPAD severely degrades the thermal conductivity of the DUT during the PC test. In contrast, it is shown that no defects were found in the solder parts not subjected to thermo-mechanical stress under the source and drain pads. These analysis results accurately correspond to the previously SAM results of Section 3.5.2 and the analysis in Section 4.2.3. In the result of the failure analysis, it is proven that the solder delamination cannot be the cause of the IDSS failure induced by PC test.

In Section 4.2.3, the non-destructive method to verify the complete solder delamination under TPAD with the C_{OSS} measured before and after the PC test was introduced. In this method, a thickness of delamination (air gap) of 4 μm or more is assumed to ensure a 20 % difference between these two C_{OSS}. In the SEM image of Figure 4-5 b), the vertical crack width of tens of micrometer is seen in the degraded solder joint under TPAD. Thus, this method can be utilized to verify complete solder delamination under TPAD after PC test.

A surface current of Al PCB can be measured using only Al PCB separated from a discrete device. Firstly, the discrete GaN device of the DUT REV#3 had been detached from Al PCB by desoldering. The surface leakage current measured between drain to source leads is found to be in femtoampere level at $V_{DS} = 650$ V. Thereby, the surface leakage current of the Al PCB cannot be also the cause of this IDSS failure.

4.3. IDSS FAILURE MECHANISM INDUCED BY PC TEST IN A PACKAGE

The package structure except a die suffers from considerable thermo-mechanical stress during PC test. This stress can mainly cause problems in the package such as layer delamination, Cu vias lift-off or Cu vias crack and metallization [80-86]. In the conventional PC tests, bond wire lift-off, wire bond crack, and metallization had been reported as significant failure mechanisms [80]. In their failure analysis, $R_{DS(ON)}$ of the DUT sensitively responds to structural deformation of the various kind of the package. In these PC tests in Chapter 3, no noticeable change in the values of $R_{DS(ON)}$ during the PC test is observed. Moreover, these defective phenomena related to open circuit failure are not also matched to the IDSS failure of short circuit issue.

IDSS failure can happen by an undesirable defect, such as crack, created in a dielectric of the package. A dielectric between source and drain electrodes electrically isolates both terminals to withstand the intense electric field applied at off state. The thermo-mechanical stress can lead to the crack of the dielectric, and the crack becomes a critical path for the leakage current.

IDSS failure by the crack is dominated by the electric field strength which is expressed as the bias voltage divided by the distance. Hence, this IDSS failure readily occurs at higher voltage bias and closer distance. When FWD#1 has 100 uA IDSS at the end of PC test, a drain-to-source bias voltage was around 5 V. The distance between both terminals can be confirmed with simple structure analysis. Figure 4-6 a) shows a
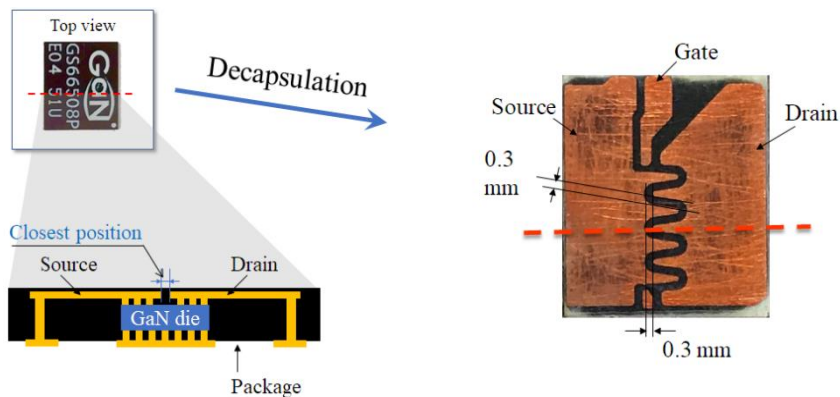
a) a cross-sectional image of the GaN device

b) Top view of Cu plates of a decapsulated GaN device

Figure 4- 6 a) A cross-sectional image of the GaN device, b) top view of Cu plates of a decapsulated GaN device.

cross-sectional image of the tested GaN device. In this picture, the closest position between source and drain in the package is between top Cu plates. Figure 4-6 b) displays the top view of Cu plates after removing the thin layer covering the top of the chip. The distance between both terminals identified by the microscope is around 0.3 mm. Considering a dielectric strength of air 3 kV / mm [112], it is implausible that a package crack causes the IDSS failure. Moreover, Ref. [113] explains that package crack mainly leads to open circuit issues in various failure analysis of semiconductor chips, not IDSS failure. Therefore, the defects in the package mentioned in the above can be carefully excluded from the suspect causes list of the IDSS failure.

4.4. IDSS FAILURE MECHANISM INDUCED BY PC TEST IN A DIE

The tested GaN HEMT semiconductor exposed to thermal stress above the allowed maximum operating temperature and experience repeated thermo-mechanical stress during PC test. Such stresses can sufficiently contribute to the GaN die deterioration by various mechanisms. The GaN HEMT had been studied in diverse failure mechanisms. In this section, failure mechanisms identified in the current literature summarized by the type of stresses and results of each strain. The summary is subsequently compared with the IDSS failure caused by the PC test.

4.4.1. LEAKAGE CURRENT LOCALISATION ANALYSIS

Localization of the IDSS in the GaN HEMT is essential for more accurate failure analysis because the IDSS is defined as the total current flowing between the drain and source potentials with $V_{GS} = 0$ V and $V_{DS} = 650$ V. The total current includes the current elements of three paths: drain-to-source, drain-to-gate, and drain-to-substrate in the semiconductor die. To investigate the leakage path REV#3 after IDSS failure was used for the localization analysis. Its discrete GaN device had been detached from Al PCB by desoldering. Regional current elements are examined using four amperemeters and a probe station with four probes. Figure 4-7 a) illustrates a test circuit schematic for the localization analysis. An identified leakage path can support to explain a particular failure mechanism.

Figure 4-7 b) shows the results analysis of the leakage localization. It is shown that the drain-to-gate (I_{DG}) and drain-to-substrate leakage currents (I_{DSub}) are a small part of the IDSS. On the other hands, the portion of the drain-to-source leakage current (I_{DS}) is predominant in the total IDSS. The primary leakage path of the IDSS phenomenon in PC test, therefore, is between drain and source. This result is going to be utilized as relevant evidence for comparison between the IDSS failure phenomenon induced by PC test and failure mechanisms from conventional studies.

a) Test circuit for leakage localization   b) test results of IDSS localization
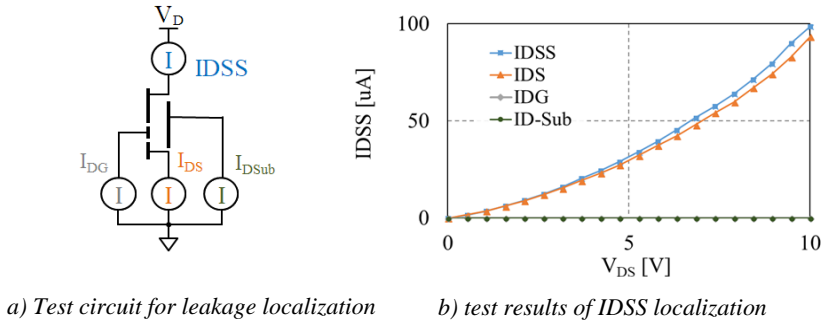
Figure 4- 7 a) Test circuit for leakage localization, b) test results of IDSS localization.

4.4.2. THE IDSS FAILURE IN PC TEST VS. CONVENTIONAL FAILURE MECHANISM

Potential nine failure mechanisms of GaN HEMTs were enumerated in Ref. [114]. In the literature, specific failure phenomenon is triggered by one or more stress factors. Table 4-2 shows the major stresses and results for each failure mechanism. In the PC test, the GaN HEMT is worn out by thermal stress and thermo-mechanical stress. Any reverse voltage bias between drain and source, gate, and substrate electrodes is not applied during PC test since the GaN HEMT did not actively switch. By comparing the results of the PC test to the conventional failure mechanisms of GaN HEMTs, this IDSS failure mechanism can be discussed logically.

As shown in Figure 4-1, the most prominent feature of the failure phenomenon in the PC test was that only the drain-to-source leakage current increased without changing offline parameters $R_{DS(ON)}$, V_{th}, and C_{OSS}. In Table 4-2, there are failure mechanisms related to the thermal stress of the case number (No.) from 1 to 6. They must accompany an alteration of $R_{DS(ON)}$ or V_{th}. Whereas, noticeable degradation of $R_{DS(ON)}$ was not seen in the PC-tested DUT. Thermo-mechanical stresses cause the failure phenomenon in the case No. 7. Here, traps generated in a GaN layer reduce the conductivity performance of 2DEG of a GaN HEMT. Thus, this failure should entail degradation of $R_{DS(ON)}$ as well as a change in V_{th}. The other two cases No. 8 and No. 9 are not considered owing to their stress types unrelated to PC test. Therefore, in summary, the observations for failures PC test induces does not match the reported mechanisms in literature.

Repeated thermo-mechanical stress in PC test can still result in physical damage to dielectric layers: AlGaN, GaN, and passivation. Considering GaN HEMT structure

No. of cases	Failure mechanism	Major stress	Symptoms of parameters			
			$R_{DS(ON)}$	V_{th}	I_{DS}	I_{DG}
1	Feed metal degradation	Thermal	●	-	-	-
2	Schottky contact degradation		●	●	-	●
3	Ohmic contact degradation	Thermal, reverse bias	●	-	-	-
4	Passivation delamination	Thermal	●	●	●	-
5	Electron trapping in SiN	Hot-electron, Thermal	●	●	●	-
6	Hot-electron trapping		●	●	●	-
7	Trap generation	Thermo-mechanical	●	●	●	-
8	Gate-edge degradation	High reverse bias	●	●	-	●
9	Punch-through effect	GaN buffer condition	●	●	●	-

●: change & -: no change

Table 4- 2 Failure mechanisms, stress sources, and symptoms of parameters of GaN HEMTs based on the literature [114].

and the analysis results of leakage current localization, multilayer crack of AlGaN and SiN between an FP connected to source and 2DEG connected to drain can describe the IDSS failure mechanism well. This reasonable suspicion requires further physical analysis to find defective positions of the GaN semiconductor.

Unknown failure mechanism induced by the overheating remains a possibility. Additional PC tests with a temperature swing condition not exceeding the maximum operating $T_J = 150$ °C at the end of PC test is needed to confirm the potential scenario.

4.5. SUMMARY

In this chapter, the IDSS failure phenomenon found in Chapter 3 has investigated systematically. We have approached this failure phenomenon induced by PC test in three directions: 1. DUT excluded a discrete GaN chip, 2. package excluded a GaN die, and 3. a GaN die.

A hypothesis of how solder delamination achieved by PC test affects the IDSS failure has been suggested. It has been proven with complement tests and cross-sectional SEM analysis. Although this hypothesis cannot delineate the IDSS failure confirmed in this test, a risk factor that the complete delamination of solder linking between the Si substrate and the source electrode can induce IDSS failure has been identified. For eliminating this potential risk, the precaution is proposed that the Si substrate must be connected to a source electrode inside a package or a die, not solder. Moreover, the non-destructive inspection method to verify complete solder delamination under TPAD after PC test is newly proposed.

Repetitive thermomechanical strain during PC test may initiate crack or delamination in a package. Even though these defects should bring out $R_{DS(ON)}$ shift, there is any no abnormality of a offline parameter $R_{DS(ON)}$ measured at the end of the test. This failure mechanism does not also coincide with the IDSS failure phenomenon found in these tests.

Failure mechanisms in the literature caused by thermal or thermo-mechanical stress in a GaN die have been reviewed. It turns out that the major leakage route of the IDSS failure is between drain to source, not gate or Si substrate through localization analysis results. Based on the analysis results and information collected from PC tests, this IDSS failure by PC test is compared to the conventional failure mechanisms from the literature. However, we cannot find any failure mechanism in the literature matched to this IDSS failure.

In summary, it is found that the cause of the IDSS failure phenomenon induced by thermomechanical stress or thermal stress is in a GaN HEMT die not DUT and package. Moreover, the IDSS failure is a new phenomenon that is not covered in the conventional literature. Two potentialities for overheating or dielectric cracks to trigger the IDSS failure, which were identified from this study, will be discussed with additional PC test with lower temperature swing condition and physical failure analysis of them to find dielectric fatigue inside a die in the future.

CHAPTER 5. OPTIMIZATION OF A HIGH VOLTAGE GAN HEMT FOR POWER APPLICATION

A GaN HEMT debuted as an RF electric device in around 2004 years. Now, several power semiconductor companies have succeeded to commercialize GaN HEMTs for power application. As a GaN HEMT has extended from RF to power application field, they have experienced many technological developments. High voltage (HV) resistant technologies have played a major role in helping GaN HEMTs make inroads into the power electronics market. The breakdown capability of a GaN HEMT is also related to its reliability since various failure phenomena of the GaN HEMTs occur in reverse bias condition.

In this chapter, optimized depletion mode (D-mode) power GaN-on-Si HEMTs is proposed in the aspect of stability against higher reverse bias. The tentative target of the maximum drain-to-source operating voltage (V_{DS_MX}) is 600 volts. Diverse technologies that enhance the performance of breakdown voltage and leakage current of GaN HEMTs have been overviewed based on literature. Moreover, additional design factors that affect this performance has been considered with technology computer-aided design (TCAD) simulation. Finally, an experiment plan that reflects significant factors extracted from the review of the technologies and the simulation result has been proposed.

5.1. TECHNICAL FACTORS FOR A HIGH VOLTAGE GAN HEMT

Breakdown capability and reliability of a GaN HEMT depend on some factors such as structural and design factors. Understanding the influence of each element helps us find conditions able to optimize a GaN HEMT. Selected factors that can act on breakdown capability of a GaN HEMT have been considered with data analysis based on literature and simulation results.

5.1.1. CHARACTERISTICS OF BREAKDOWN CAPABILITY

Leakage current and breakdown voltage characteristics represent the breakdown capability of a power device. Figure 5-1 displays one example of the leakage current versus reverse bias voltage in off-state. Various definitions describe detail features of breakdown capability. The Y-axis of the graph is scaled logarithmically.
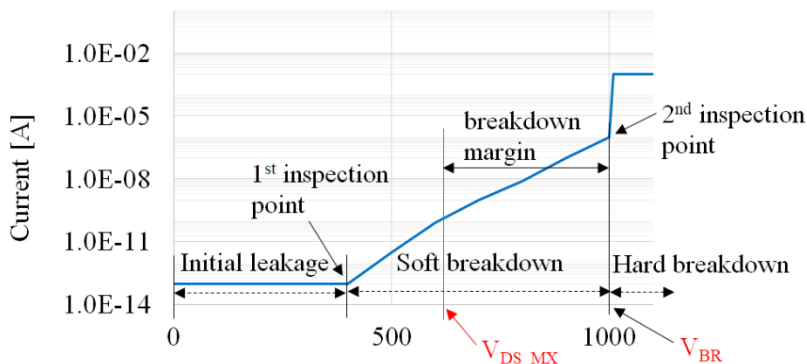
Figure 5- 1 An example of the leakage current versus reverse bias voltage in off-state with primary definitions of leakage current curve.

The graph shows the process in which the power device is destroyed under the reverse bias condition. It is divided be three regions based on two inflection points: initial IDSS, soft-breakdown, and hard-breakdown. An initial leakage region is named before the first inflection point. This region is where the leakage current is least affected by a reverse bias strength. After the first inflection point on the graph, the current curve enters the soft-breakdown region. In this second region, the leakage current logarithmically increases versus reverse bias linear growth, which appears by a specific mechanism such as quantum mechanical tunnelling. Generally, V_{DS_MX} of power switching devices is determined in this region, and the off-state leakage current (IDSS) in the datasheet is defined as total measured current at V_{DS_MX}. The read drain-to-source bias voltage around the second inflection point is called breakdown voltage (V_{BR}). The device irreversibly breaks by the avalanche breakdown mechanism at this point. The current dramatically increases, and the device is destroyed after this point. The section between V_{DS_MX} and V_{BR} becomes a breakdown margin. Higher margin promises safety against reverse bias condition but undermines other performance such as on-state conductivity of the device simultaneously. This area, therefore, must be considered with caution in designing a new device. A GaN HEMT device also has the similar leakage current trend to the graph under reverse bias condition.

5.1.2. FACTORS ABLE TO AFFECT BREAKDOWN CAPABILITY

The previous series of events is induced by locally concentrated electric field strength between drain and source, gate, and Si substrate. Figure 5-2 illustrates primary factors in a GaN HEMT that affect electric field distribution in reverse bias. The electric field strength is expressed in volts per distance. The electric field indicated by blue arrows spreads from drain to source, gate, and a substrate. The factors that affect the electric field can be divided into two groups: design and structural factor groups.
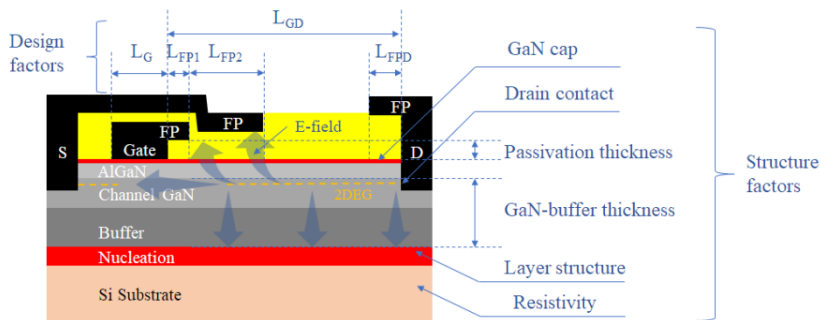
Figure 5- 2 Primary factors in a GaN HEMT that affect electric field distribution in reverse bias.

The influence of design factors on breakdown capability is significant because of the structural features of a lateral device such as a GaN HEMT. A gate-to-drain length (L_{GD}) that decides a total size of GaN HEMT is a fundamental design factor. Widening L_{GD} increases the breakdown capability of the device, whereas reducing the performance of $R_{DS(ON)}$. Thus, a device designer tries to maximize the breakdown capability of the device under a limited L_{GD}. The field plate (FP) structure improves this capability of a GaN device under a limited L_{GD}. There are three types of field plats in the literature [110, 115-117]: gate, source, and drain FPs. The length of each FP has an influence on breakdown capability as well as reliability. These lengths are indicated by L_{FP1}, L_{FP2}, and L_{FPD} on Figure 5-2. An insufficient gate length (L_G) under reverse bias condition can cause a higher leakage current due to a punch-through mechanism between drain and source, while a longer L_G also increases $R_{DS(ON)}$. Thus, these crucial design factors should be considered with current study results and TCAD simulation carefully.

Structural factors also affect leakage current and breakdown capability. Some GaN HEMTs have a thin GaN cap layer. This extra dielectric layer can reduce the leakage current between the gate and drain. Thicknesses of passivation, channel GaN, buffer GaN, and the nucleation layer are related to vertical distance from drain electrode to gate, source, and substrate electrodes. Besides, a relevance between the drain contact methods and V_{BR} had been described in Ref. [118, 119]. In Chapter 4, it was confirmed that the distortion of an electric field between the drain and substrate could lead to an abnormal leakage current issue. A depletion width in a Si substrate under drain-to-substrate HV reverse bias relies on the resistivity of the Si substrate. Hence, the resistance property of Si substrate also can modify electric field distribution. A high resistivity (HR) substrate has a longer depletion width than a low resistance substrate at the same reverse bias.
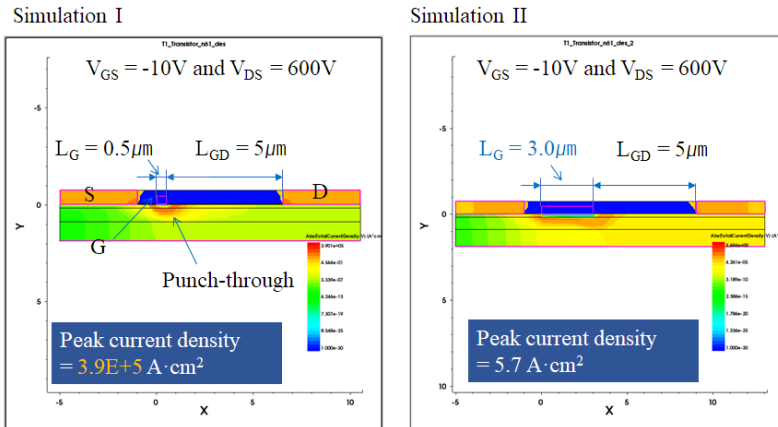
Figure 5- 3 Current density TCAD simulation of GaN HEMTs with L_G = 0.5 μm and L_G = 3 μm.

5.2. DESIGN FACTORS FOR A HIGH VOLTAGE GAN HEMT

To optimize a GaN HEMT for power application, a device designer must scrutinize as much information as possible at the beginning. Nonetheless, reflecting all the proposed factors in an experiment requires a lot of time and money. In the stage of planning an experiment, the elements with an insignificant or significant impact on breakdown capability of the device can be found, and they can replace with the appropriate values confirmed by statistical analysis of current data and TCAD simulations. Hence, design factors able to improve breakdown capability; L_G, L_{GD}, L_{FP1}, L_{FP2}, and L_{FPD}, are reviewed. And the factors (L_{FP1} and L_{FPD}) that require confirmation of interaction for the device optimization have been used as primary experimental variables.

5.2.1. GATE LENGTH

In Simulation I of Figure 5-3, the L_G not long enough to prevent the punch-through phenomenon and increasing IDSS, whereas the distance longer than necessary hurts $R_{DS(ON)}$ and gate capacitance. The length should, therefore, be minimized at a somewhat acceptable level of leakage current considering margin. The appropriate gate length can be considered with TCAD simulation.

A model for the simulation has L_{GD} = 5 μm. Figure 5-3 is different peak current density difference between L_G = 0.5 μm and 3 μm with 2D TCAD simulation. The simulation has been conducted in V_{GS} = -10 V and V_{DS} = 600 V. In results of a simulation with
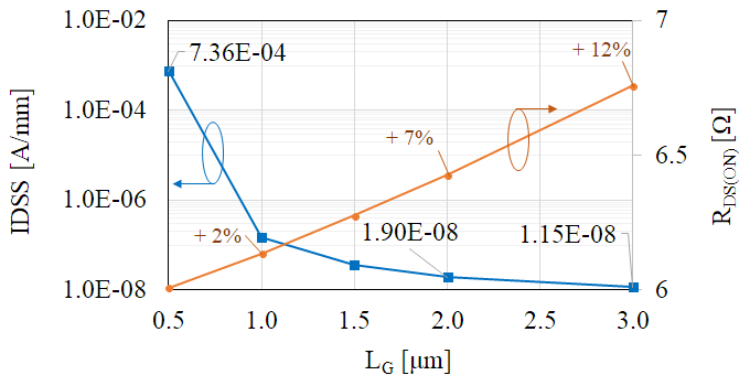
Figure 5- 4 Trends of IDSS and $R_{DS(ON)}$ according to the L_G range from 0.5 μm to 3 μm based on TCAD simulation.

$L_G = 0.5$ μm, the peak current density of 3.9 E+5 A·cm² is 68,400 times bigger than $L_G = 3.0$ μm, which shows a strong correlation between a gate length and the off-state leakage current. More additional simulations, therefore, are needed.

Figure 5-4 displays trends of IDSS and $R_{DS(ON)}$ according to the L_G range from 0.5 μm to 3.0 μm based on TCAD simulation. The primary Y-axis of the graph is scaled logarithmically. The primary and secondary Y-axis represent IDSS and $R_{DS(ON)}$ respectively. IDSS is measured in $V_{GS} = -10$ V and $V_{DS} = 600$ V. $R_{DS(ON)}$ is calculated by V_{DS} measured in $VGS = 2$ V, $I_{DS} = 1$ A, channel width (W_{ch}) = 1 mm. The simulation results show the IDSS decreases sharply after $L_G = 0.5$ μm. There is no notable change after $L_G = 1.5$ μm. As mentioned above, increasing the L_G immediately raise the $R_{DS(ON)}$. In the simulation results, the $R_{DS(ON)}$ at $L_G = 1.5$ μm increases about seven percent from $L_G = 0.5$ μm.

Based on the previous simulation results, an appropriate L_G can be found. It is confirmed that L_G should be at least 1.5 μm to ensure the stable IDSS. It cannot be an absolute standard since many factors such as process variation are excluded in the simulation. It is, therefore, advantageous to have enough margin of the length to get meaningful results in the initial experiment. Also, the $L_G = 2.25$ μm of a commercialized GaN HEMT with $V_{DS\_MX} = 650$ V was checked by a cross-sectional SEM image in Ref. [109]. As considering various results and margin, $L_G = 2.0$ μm has been selected as a gate length in this experiment.

5.2.2. DRAIN TO GATE LENGTH

L_{GD} has the most substantial effect on the GaN semiconductor die size. Other factors such as L_{FP1}, L_{FP2}, and L_{PFD} should be optimized to the maximum within the selected L_{GD}. Hence, this length needs to be long enough to achieve desired HV breakdown
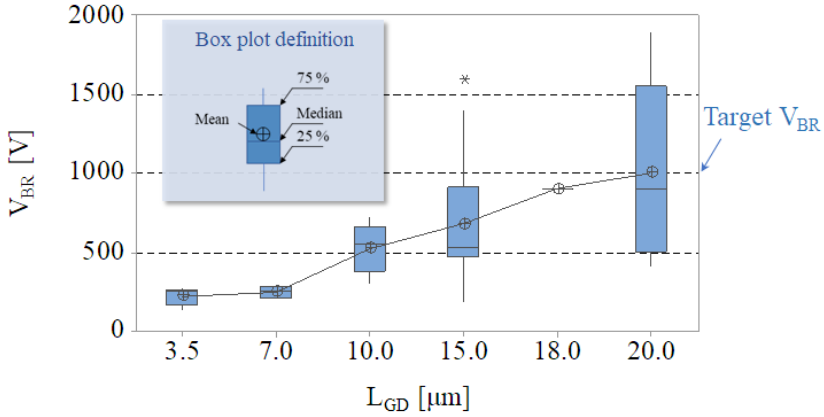
Figure 5- 5 The box plot that illustrates V_{BR} distribution of forty-four GaN HEMTs by L_{GD} groups based on literature (44 cases from 9 papers).

capability. If the breakdown margins the described in Figure 5-1 is around fifty percent of V_{DS_MX} in this experiment, target V_{BR} should be around one thousand volts. The proper L_G value can be found by investigating the relation between L_{DS} and V_{BR} of various GaN devices from the previous literature.

The box graph in Figure 5-5 illustrates V_{BR} distribution of GaN HEMTs by L_{GD} groups. The data used for this analysis is including total of forty-four cases from nine reference papers [110, 115, 117, 120-125]. The most GaN HEMTs in the literature
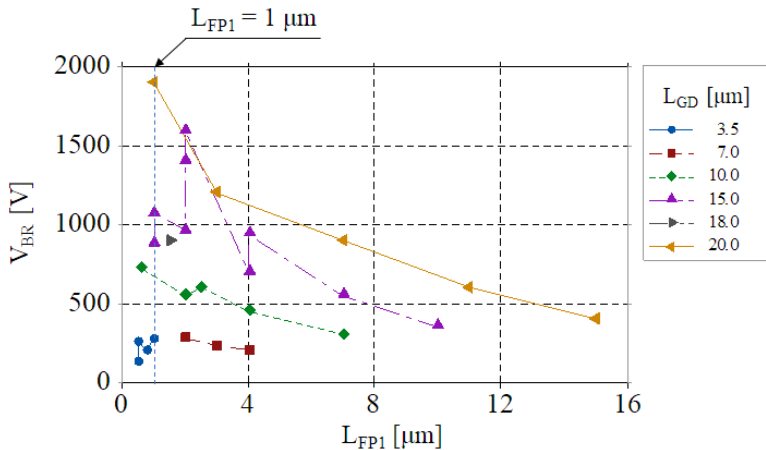
Figure 5- 6 The scatter plot that exhibits a relation between L_{FP1} and V_{BR} by L_{GD} groups based on literature (33 cases from 8 papers).

have a field plate structure between gate and drain. It shows a meaningful trend that, as L_{GD} increases, V_{BR} a GaN HEMT can accomplish is also rising. In the $L_{GD} = 20$ μm group, the mean value of them is around a thousand volts. Considering the temporary target $V_{BR} = 1$ kV, the lateral distance from the gate and drain, therefore, should be around 20 μm for this experiment. In the literature [124], a maximum V_{BR} of 1.9 kV can be achieved in this condition.

5.2.3. FIELD PLATE: L_{FP1}, L_{FP2}, AND L_{FPD}

An FP structure serves to release the electric field concentrated between the gate and the drain. It is a necessary structure to ensure the high breakdown voltage of lateral devices such as GaN HEMTs. There are three kinds of FP in Figure 5-2: L_{FP1}, L_{FP2}, and L_{FPD}. A gate-connected FP (L_{FP1}) extends toward the drain side and releases an electric field focused at the gate edge. A source-connected FP (L_{FP2}) extends from the L_{FP1} edge toward the drain side. It not only undermines an electric field concentrated at L_{FP1} edge but also affects an electric field distribution from L_{FP1} edge to drain. A drain-connected FP spreads out electric field concentration around the drain side. These should be optimized within the previously limited $L_{GD} = 20$ μm.

Figure 5-6 exhibits a relation between L_{FP1} and V_{BR} of various thirty-three GaN HEMTs based on eight papers [110, 115, 117, 120-124]. They are grouped by L_{GD}. In the result of $L_{GD} = 20$ μm, it is confirmed that the GaN HEMT with $L_{FP1} = 1$ μm has the highest $V_{BR} = 1.9$ kV. In contrast, in the group of $L_{GD} = 15$ μm, the GaN HEMT with $L_{FP1} = 2$ μm has the highest V_{BR}. In this case, the GaN HEMT with $L_{FP1} = 1$ μm has a lower V_{BR} than $L_{FP1} = 2$ μm. It, therefore, means that V_{BR} can be optimized at the any particular L_{FP1} length. In the experiment of this chapter, two conditions of $L_{FP1} = 1$ μm and $L_{FP1} = 3$ μm has been selected to obtain the optimized V_{BR}.
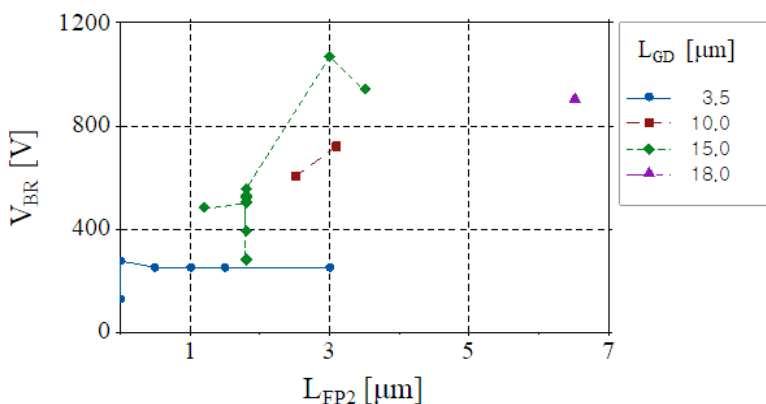
Figure 5- 7 The scatter plot that exhibits a relation between L_{FP2} and V_{BR} by L_{GD} groups based on literature (19 cases from 6 papers).

Figure 5-7 shows V_{BR} of GaN HEMTs grouped by L_{GD} versus L_{FP2}. The numerical data of the graph is extracted from nineteen cases of six papers [110, 115, 120-122, 125,]. How much L_{FP2} affect V_{BR} is challenging to determine with this graph. However, Ref. [122] shows the V_{BR} increase of twelve percent and the improved dynamic $R_{DS(ON)}$ characteristics of the GaN HEMT with $L_{FP1} = 1$, $L_{FP2} = 3$, and $L_{FPD} = 15$ µm comparing to the GaN HEMT without a source-connected FP. In this device, the distance of L_{FP2}
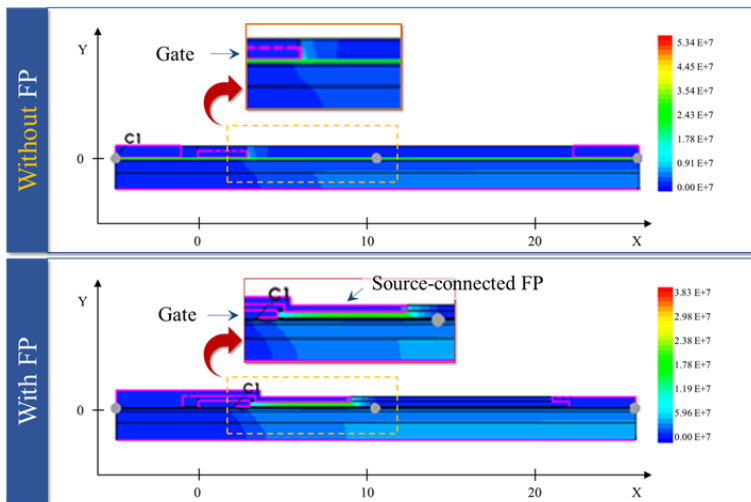
a) TCAD simulation between a GaN HEMT without FP and with FP
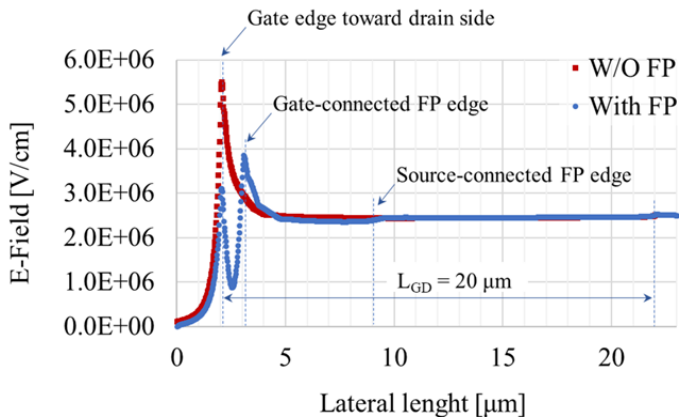
b) The electric field distributions along the 2DEG between a GaN HEMT without FP and with FP

Figure 5- 8 a) TCAD simulation b) the electric field distributions along the 2DEG beween a GaN HEMT without FP and with FP.

edge to the drain is 11 μm. It is evident that the effect on V_{BR} of the source-connected FP length is not important, but being this FP has a positive effect of V_{BR} and a dynamic $R_{DS(ON)}$ [122]. Hence, as referring to this geometry information, L_{FP2} of the GaN HEMT with $L_{GD} = 20$ μm and $L_{FP1} = 1$ μm for this experiment is selected as 6 μm.

In the research of Ref. [117], the additional drain-connected FP had improved V_{BR} to maximum 1.6 kV in a GaN HEMT with $L_G = 2$ μm, $L_{FP1} = 2$ μm, and $L_{GD} = 15$ μm. L_{FPD} had varied from 1 μm to 8 μm. This result resembles the trend of L_{FP1}. The GaN HEMT has the highest $V_{BR} = 1.6$ kV at $L_{FPD} = 1$ μm, and V_{BR} decreases as the L_{FPD} increases. In the experiment of this chapter, $L_{FPD} = 1$ μm has been selected to obtain the highest V_{BR}. The drain contact solution mentioned in the third paragraph of Section 5.2.1 can also affect an electric field distribution on the drain side. Conditions able to prove the interaction effect of these two factors will reflect on the final experiment plan.

TCAD simulation can describe the electric field dispersion effect by the proposed field plates. This simulation has been carried out in zero volts of the gate, source, and substrate and $V_{DS} = 600$ V. Figure 5-8 displays the TCAD simulation results and the electric field strength along the 2DEG between a GaN HEMT with FP and without FP. In the simulation result with FP in Figure 5-8 a), it can be confirmed that the concentration of electric field is dispersed into two points: the gate edge and the gate-connected FP edge. On the other hand, the TCAD simulation result of the GaN HEMT without FP shows that the electric field is focused only at the gate edge. The electric field distributions along the 2DEG between with FP structure and without FP structure are compared in Figure 5-8 b). Adding the FP structure reduces the peak electric field near the gate edge in the without FP condition around forty-three percent. These reviews from literature and the simulation results illustrate the advantages of FP structure.

5.3. STRUCTURAL FACTORS FOR A HIGH VOLTAGE GAN HEMT

The structural factors introduced in Figure 5-2 can mainly affect the distribution of vertical electric fields. These factors are decided by a thickness of each layer, process conditions, and defects of various layers that make up a GaN HEMT. In this section, we discussed the structural factors that can affect the breakdown performance of the GaN device based on data analysis from literature and TCAD simulation. The structural factors with significant impacts confirmed by the previous consideration will be investigated with the statistics factor analysis and an experiment using two GaN-on-Si wafers with different structures. The two wafers are named as the Wafer A and Wafer B, respectively.
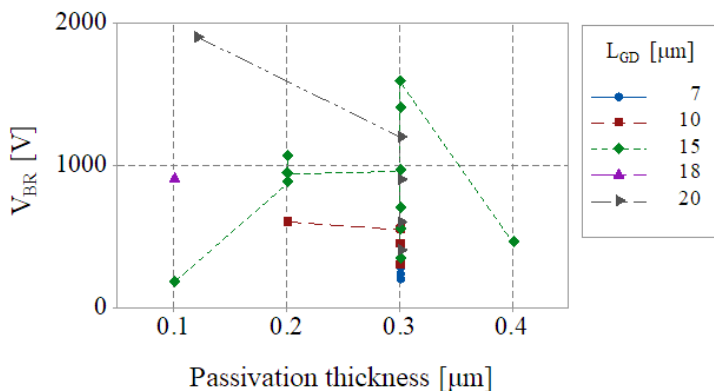
Figure 5- 9 The scatter plot that exhibits a relation between a passivation thickness and V_{BR} by L_{GD} groups based on literature (26 cases from 7 papers).

5.3.1. THE FIRST PASSIVATION THICKNESS

The first passivation thickness determines a vertical distance from a top surface of a GaN cap to the gate-connected FP in the structure of a GaN HEMT, which can be found in Figure 5-2. This passivation layer consists of silicon nitride Si_3N_4. Data found in literature can confirm the influence of a passivation thickness on V_{BR}. Figure 5-9 shows a relation between passivation thicknesses and V_{BR}. The numerical data comes from twenty-six cases of seven papers [110, 117, 120, 122-125]. They are grouped by L_{GD} because the L_{GD} directly affects V_{BR}. There is no clear correlation between each other in the graph. The two wafers described above will be equally fabricated using RF GaN HEMT process of the Chalmers University of Technology so that the Si_3N_4 thickness of them to be employed in this experiment is 70 nm.
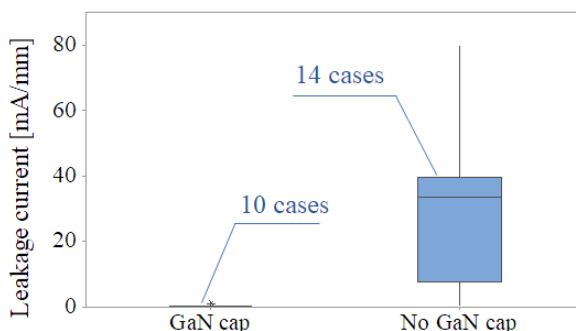
Figure 5- 10 The box plot that exhibits the leakage current distributions between with and without a thin GaN cap layer (24 cases from 9 papers).

5.3.2. GAN CAP ON AN ALGAN BARRIER

A thin GaN cap layer grown on the top surface of AlGaN is widely used to reduce the leakage current [8, 126]. This thin cap layer not only decreases reverse leakage current through Schottky contact of the gate but also protects AlGaN layer against processes after the thin GaN cap deposition. The difference in the leakage current per unit channel width between with and without GaN cap is displayed in Figure 5-10. The box plots are grounded on twenty-four cases from nine papers [110, 117, 120-125, 127]. The group with the GaN cap layer shows lower and less distributed leakage current level. On the other hand, the group with no GaN cap not only has a large dispersion of the leakage current but also has a higher mean value of them compared to the GaN cap group. This difference shows that the thin GaN cap layer can obviously improve the leakage current. Hence, the two wafers used for this experiment have a thin GaN layer in common two obtain better leakage current characteristics.

5.3.3. ENTIRE THICKNESS OF CHANNEL GAN AND BUFFER

The entire thickness given by the channel GaN and the buffer layer between an AlGaN and a Si substrate in Figure 5-2 can affect the electric field distribution under reverse bias condition. When the thickness is not sufficient to withstand an HV reverse bias, the GaN HEMT can encounter the large leakage current or an early avalanche breakdown. Figure 5-11 is drawn based on thirty-four cases from ten papers [110, 117, 122, 123 127-132]. The graph shows a relation between the entire thickness and V_{BR} of GaN HEMTs. A strong correlation between both is not seen. Thus, this vertical thickness does not seem to have a significant effect on V_{BR} in this analysis.
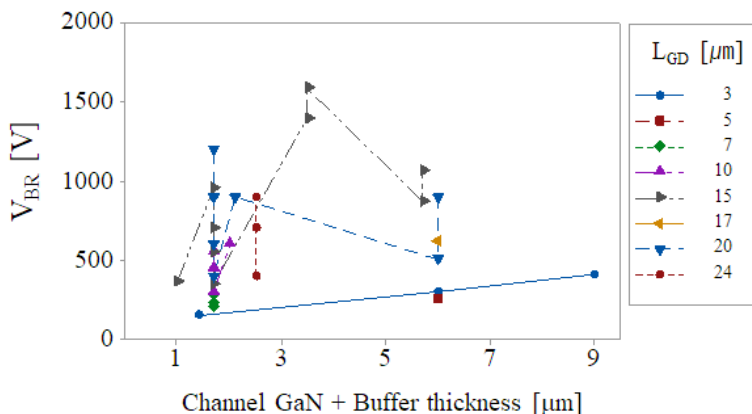
Figure 5- 11 The scatter plot that exhibits a relation between a channel GaN + buffer thickness and V_{BR} by L_{GD} groups based on literature (34 cases from 10 papers).

There is, nevertheless, a study that a buffer thickness comprising multiple pairs of GaN/AlN (20/5 nm) between a nucleation layer and a channel GaN layer can enhance V_{BR} of a GaN HEMT [129]. It is shown in the research that increasing this buffer thickness significantly reduces the dislocation density of the channel GaN layer. The thick buffer layer can ultimately achieve higher V_{BR} and smaller leakage current performance. Two different wafers used in this experiment have different buffer structures. A 1.9-µm Fe-doped GaN layer is grown on a nucleation layer as the buffer layer and channel GaN layer in the Wafer A. The buffer layer and channel GaN layer of Wafer B consist of a 3-µm AlN buffer and a 1.5-µm undoped GaN layer, respectively. In this experiment, the impact of the thickness of a channel GaN layer and a buffer layer on breakdown capability will be able to be verified.

5.3.4. SI SUBSTRATE RESISTVITY

GaN-on-Si HEMTs choose a Si substrate that fits their application. An low resistivity (LR) Si substrate is usually used for power application. An HR Si substrate is mainly employed for RF application to achieve higher RF performance. Some research of RF GaN HEMT on an LR Si substrate had shown a lower RF performance due to the RF signal coupling to the lossy Si substrate than that accomplished with HR Si substrate. The coupling phenomenon depends on frequency and parasitic capacitors connected to the substrate [133, 134]. Although this parasitic capacitances increase in power application with an LR Si substrate, the performance degradation due to the coupling can be negligible because the operating frequency is markedly lower than RF application. Furthermore, LP Si substrate wafer is relatively cheap compared to the HR Si substrate wafer [133]. For these reasons, power application prefers an LR Si substrate wafer.

Si substrate resistivity of a GaN-on-Si HEMT can affect on an electric field distribution at a higher reverse bias condition. As the drain-to-substrate bias increases, depletion region of the Si substrate is extended from the adjacent nucleation layer. A depletion width of an LR Si substrate is shorter than an HR Si substrate under the same reverse bias condition. The two types of Si substrates have different electric field distributions. If the vertical electric field between the drain to the substrate is weakened by a widen depletion width, the electric field strength concentrated to the gate or the gate-connected FP edge can be enhanced. Hence, the resistivity of the Si substrate also should be considered for optimization of an HV GaN HEMT.

The electric field concentration impact due to the vertically slack electric field intensity can cause the leakage current increase or V_{BR} issue. A mechanism of this phenomenon resembles IDSS increase problem induced by the electrically floating substrate in Chapter 4. Figure 5-12 describes TCAD simulation results between a standard condition and electric field distorted by the floating substrate. The model for the simulation has $L_G = 3$ µm, $L_{FP1} = 1$ µm, and $L_{GD} = 5$ µm. The reverse bias between the drain to other electrodes is 600 V. It is difficult to know the Si substrate potential
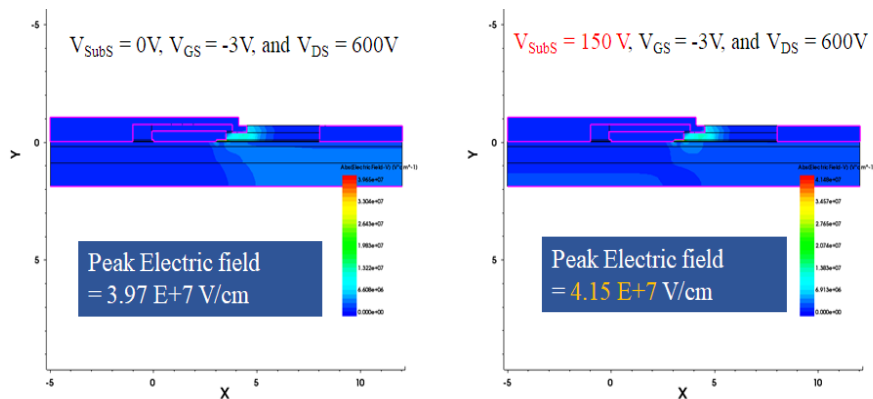
Figure 5- 12 Comparison of TCAD simulation between V_{SubS} = 0V and V_{SubS} = 150 V.

when it is floating so that we assume V_{SubS} = 150 V in the simulation. In the vertically loosen electric field condition, the peak electric field is 4.4 % higher compared to the standard condition. The concentrated electric field can trigger IDSS increase or avalanche breakdown. The Si substrate resistivity of the two wafers used in this experiment is different. Wafer A uses an HR Si substrate for RF application, and the Wafer B employes an LR Si substrate (< 0.02 Ω·cm). The influence of the Si substrate can, therefore, be proven through the final experimental results.

5.3.5. DRAIN CONTACT: OHMIC OR SCHOTTKY CONTACT

There are studies on higher breakdown capability of GaN on Si HEMTs with Schottky drain contact compared to the ohmic drain contact stand condition [127, 135]. Ref. [127] shows that, by changing the drain contact method from the ohmic to the Schottky contact, V_{BR} had been increased by about 78 % from 505 V to 900 V, and $R_{DS(ON)}$ had been also increased by around 47 %. Even though the increase of the on-state resistance is taken into account, the improvement of the breakdown capability is worth noticing. The GaN HEMT with drain Schottky contact and L_{GD} = 20 μm had achieved V_{BR} = 900 V without any FP structure in Ref. [127]. We can, hence, expect the increased breakdown capability of the device with the drain Schottky contact and FP structures. In this experiment, the drain Schottky option will be utilized in this experiment as major experimental variables.

5.4. EXPERIMENT PLAN FOR FACTOR ANALYSIS OF BREAKDOWN CAPABILITY

For a GaN HEMT to achieve optimized breakdown capability, various factors have been reviewed based on literature and TCAD simulations. The appropriate values to meet the device target of a few design factors have been selected in the process. Further, the structural factors influencing the optimization of V_{BR} has been applied to the experiment by using two types of GaN-on-Si wafers with different structures. Except for the previously confirmed factors, there are additional three factors not only that can significantly affect breakdown capability but also of which interactions between each other have not been verified. In this section, the structural elements of the two wafers used for this experiment have been summarized, and an efficient design method of an experiment bottomed on statistics has been proposed.

5.4.1. EXPERIMENT PLAN FOR STRUCTURAL FACTORS ANALYSIS

The four structural factors of the channel GaN, buffer, AlGaN barrier, and resistivity of a Si substrate have been separated into two types by wafer partitioning. Figure 5-13 illustrates a schematic cross-section of the two wafers. Because technologies of Wafer A aim for RF application, a HR Si substrate is employed. By contrast, Wafer B uses an LR Si wafer. Besides, their buffers also show a completely different structure. Wafer A employs a Fe-doped GaN as a buffer layer, while Wafer B uses a thick AlN layer. Thanks to the clear-cut structural difference between both wafers, the effect of structural elements can, therefore, be well verified in the final experiment.

	3 nm GaN cap
	20 nm $Al_{0.2}GaN_{0.8}$
2-3 nm GaN cap	1.5 μm Undoped Channel GaN
11 nm $Al_{0.3}GaN_{0.7}$	
0.2 μm Fe-doped Channel GaN	
1.7 μm Fe-doped GaN	3 μm AlN buffer
Nucleation	Nucleation
HR Si substrate	LR Si substrate ($\rho < 0.02$ Ω·cm)
a) Wafer A	*b) Wafer B*
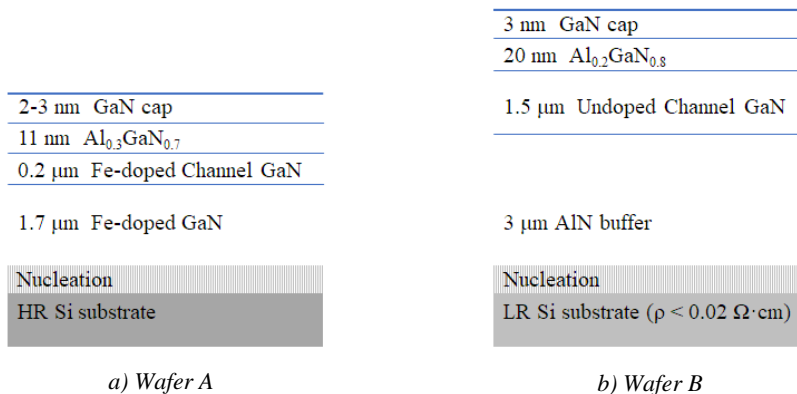
Figure 5- 13 Schematic cross section of a) Wafer A and b) Wafer B.

5.4.2. THE DESIGN OF EXPERIMENTS FOR FACTORS ANALYSIS

Three compelling factors had been proposed in the previous sections: L_{FP1}, L_{FPD}, and drain contact solution. Although the independent influence of these three factors has been confirmed in literature and the analysis of Section 5.2 and 5.3, it is necessary to analyze the effect on breakdown performance when they are applied together. Design of Experiment (DoE) is very efficient means to identify the best conditions for an influence of multiple factors [136]. This tool covers the entire range from the experimental design to the analysis of the final results. It is based on statistical knowledge. The DoE module in Minitab statistical software was used for this experiment.

As mentioned above, these three factors will be tested with two levels. In total eight experiments should be conducted for a full-factorial design of three factors and two levels. The best way to obtain outcome is the full-factorial experiment. Appling a statistical experimental model provided by the Minitab software, the number of these experiments can also be reduced based on the probabilistic analysis. The three-factors two-levels DoE of the Plackett-Burman design is used for this experiment. The number of experiments is reduced from eight to four by half. Figure 5-14 displays a difference between the full-factorial design and the Plackett-Burman design [136, 137]. Indeed, it is difficult to completely analyze interactions among them in the compressed model. However, through this model, we can analyze the sensitivity of each factor and find optimized condition of the critical factors against breakdown performance.

Test	L_{FP1}	L_{FPD}	Drain contact
1	-1	-1	-1
2	1	1	1
3	-1	-1	1
4	1	1	-1
5	1	-1	1
6	-1	1	-1
7	1	-1	-1
8	-1	1	1

Test	L_{FP1}	L_{FPD}	Drain contact
1	-1	1	-1
2	1	1	1
3	1	-1	-1
4	-1	-1	1

a) Full factorial design　　　　　　*b) Plackett-Burman design*

Figure 5- 14 a) Full factorial design versus b) Plackett-Burman design of three factors two levels.

No. of Devices	Wafer	L_{FP1} [μm]	L_{FPD} [μm]	Drain contact
1	Wafer A (HR Si substrate, Fe-doped GaN, and GaN cap)	1	1	Schottky
2		3	1	Ohmic
3		3	0	Schottky
4		1	0	Ohmic
5	Wafer B (LR Si substrate, AlN buffer, undoped GaN, and GaN cap)	1	1	Schottky
6		3	1	Ohmic
7		3	0	Schottky
8		1	0	Ohmic

Table 5- 1 Crucial information of eight kinds of devices to be produced for the experiment.

5.4.3. DEVICE INFORMATION TO BE FABRICATED AND FUTURE TEST PLAN

The four kinds of devices are manufactured per wafer based on the DoE model, and two wafers (Wafer A and Wafer B) with different structure are used for this experiment. Hence, eight kinds of devices can be secured after manufacturing. The detailed conditions of the eight samples to be produced are shown in Table 5-1. The fabricated semiconductor chips will be packaged through the following process: die sawing, die attaching, wire bonding, and Si-gel encapsulating. These completed samples will be subjected to characterization. After characteristics, full-scale factor analysis will be carried out with applied condition and experiment results in the Minitab tool. Furthermore, the best device selected in the experiment will be evaluated for reliability as well as a basic electrical performance by carrying out reliability tests such as high-temperature reverse bias, high-temperature gate bias, and accelerated power cycling test.

5.5. SUMMARY

In this chapter, all factors to able to affect electrical capability of a GaN-on-Si HEMT aiming for 600 V power application have been examined with statistical analysis based on the literature and TCAD simulation results. The three critical factors, L_{FP1}, L_{FPD}, and drain contact solution, had been chosen by logical statements. Reasonable values of remaining design factors except for these three factors were determined by the device simulation result and statistical analysis. The few structural elements were applied to the experiment plan as using two types of GaN-on-Si wafers with different structures. Methodology DoE to efficiently design experimentation was applied to this experiment. The DoE was used to investigate the sensitivity of the three factors against

the breakdown performance and to identify the best condition for the maximum breakdown capability. These samples are currently in production. When the sample production is completed, the reliability evaluation, as well as characteristics of the devices, are finally performed, and the results will be discussed.

CHAPTER 6. CONCLUSIONS AND FUTURE WORK

The purpose of this chapter is to summarize the results, which have been achieved throughout this Ph.D. project and to emphasize the main contributions presented. Finally, topics for the furture work are also discussed.

6.1. SUMMARY OF THESIS

This research project has carried out studies on performance and reliability of GaN HEMTs for power application from the packaged component level to the unit device level. The failure phenomenon and failure mechanisms of the GaN devices to be expected in the power electronics application have been deeply studied. Moreover, significant technical factors to optimize electrical accomplishment of the GaN HEMTs have been discussed.

For the designer to understand the performance of GaN HEMTs, two kinds of FOM has been utilized. The FOM is calculated with electrical characteristics of each device measured in the similar test environment and measurement conditions and their actual active areas of each device confirmed by decapsulating discrete devices. In the results of the first FOM ($R_{DS(ON)} * A$), it is confirmed that most of the commercial GaN devices exceed the theoretical limit of Si-based devices. Besides, the promising development potential of them has been described with the far distance from the ceiling of a GaN HEMT. In the second FOM, their capability of high-speed operation has been discussed. In the comparison of the 650 V-rated GaN device and the cutting-edge Si device, fourteen times superior FOM of the GaN device have been explained. It is, thus, confirmed in this investigation that the current commercial GaN devices have not only superior performance but also a good prospect.

Bidirectional PC test setup, which is the critical method to investigate the reliability of power components against thermo-mechanical stress, has been suggested as considering operation characteristics of the GaN HEMT. Six PC tests have been conducted with different two conditions. In the results, it is indicated that thermal conductivity of DUT has been consistently worn-out during PC test after a specific number of cycles. It has been proven through physical failure analysis that solder delamination between a discrete device and an Al PCB created by repeated thermo-mechanical stress during PC test causes this degradation.

Considering operation characteristics of the cutting edge GaN device, a bidirectional PC test setup is suggested. In total six samples have been PC-tested under different two test conditions. In the results of tests, it is indicated that thermal conductivity is consistently degraded during PC test after a specific point in time, and IDSS failure

phenomenon occurs around the end of the test. It has been proven through experimental physical failure analysis that solder delamination created by repeated thermo-mechanical stress during PC test causes the thermal conductivity degradation. Besides, the IDSS failure phenomenon induced by the PC test a new failure has been seen. This failure is not relevant to conventional failure mechanisms originates from PC test. In-depth analysis of this new failure phenomenon, therefore, is required to understand this failure mechanism.

The IDSS failure phenomenon found during the PC test was investigated systematically. Firstly, a hypothesis of how solder delamination achieved by PC test affects the IDSS failure has been suggested. It has been confirmed with supplement tests and cross-sectional SEM analysis that the solder delamination cannot be the cause of this IDSS failure. A risk factor, however, that the complete delamination of solder linking between the Si substrate and the source electrode can induce IDSS failure has been identified. For eliminating this potential risk, the precaution is proposed that the Si substrate must be connected to a source electrode inside a package or a die, not solder. Secondly, even though repetitive thermo-mechanical stress during PC test may initiate crack or delamination inside a package, this failure mechanism cannot be a cause of the IDSS failure due to the normality of $R_{DS(ON)}$ at the end of PC test. Finally, failure mechanisms of the GaN HEMT in the literature caused by thermal or thermo-mechanical stress have been investigated with IDSS localization analysis results and information collected from the PC tests. In the results, it is confirmed that this failure is a new phenomenon that is not covered in the literature. It has been proposed that potentialities to trigger the IDSS failure by overheating and dielectric cracks will be discussed with additional tests in the future.

Design and structure factors having an influence on the electrical capability and reliability of a GaN-on-Si HEMT are reviewed with statistical analysis based on data from the literature and TCAD simulation results. The three critical factors, which are gate-connected FP, drain-connected FP, and drain Schottky contact, have been chosen for the device optimization experiment. Appropriate values of other design factors, the gate length, gate-to-drain distance, and source-connected FP length, are excluded. These three factors have been decided according to the TCAD simulation results, statistical analysis, and logical consideration. Two conditions of the structural elements, the buffer structure, and Si substrate resistivity, have been reflected in the experiment by building up the devices on the two types of GaN-on-Si wafers. For the afore-mentioned three critical design factors, the methodology DoE based on the statistical knowledge has been applied from design to final analysis of this experiment. These samples are currently in production, and the electrical characteristics and the reliability of the manufactured devices will be investigated after finishing fabrication works.

6.2. CONTRIBUTIONS

The main contributions of this project from the author's point of view are highlighted in the following;

1. **Performance assessment with the FOM of commercial GaN HEMT devices**

   ➤ Reliable electrical characteristics measured under the same test environment of primary commercial GaN devices are provided. This data enables a discuss of how a particular technique of GaN HEMTs affects electrical characteristics. Moreover, by comparing specific electrical properties with another Si-base power device, it is possible to understand the technical difference between the Si-based power devices and GaN HEMTs.

   ➤ To calculate the first FOM ($R_{DS(ON)}$*A), the active area information of commercial GaN devices has been extracted by decapsulating each discrete device. These values can be utilized to understand the capability of power GaN devices.

   ➤ The performance of commercial power GaN devices, which exceeds the theoretical limit of Si-based power MOSFET, has been confirmed by the first FOM ($R_{DS(ON)}$ * A) data of them based on the data measured under the same test environment. It is objectively proven by comparison of this FOM and the theoretical limit of GaN HEMTs that power GaN devices have the promising potential.

   ➤ The second FOM ($R_{DS(ON)}$*Q_g) of major commercial power GaN devices, reflecting the switching capability of the power device, has been provided. From this information, it is explained that the 650 V-rated GaN device has fourteen times better performance FOM compared to the cutting-edge Si device.

2. **Development of apparatus and methodologies for accelerated PC test with an advanced power GaN device**

   ➤ An E-Mode GaN HEMT can conduct in bi-direction without an additional freewheeling diode. Considering this operating feature, bi-directional PC test environment has been proposed.

   ➤ A cutting-edge discrete GaN device applies an advanced package technology with no bond wire to maximize their switching performance. The cutting-edge GaN device has been PC-tested for the first time, and various discussions on their reliability have been made.

➢ The electrical characteristics (V_{th}, $R_{DS(ON)}$, and IDSS) of the DUT worn-out by PC has been monitored periodically in the curve tracer. This vital data to understand the failure mechanism of GaN devices degraded by thermo-mechanical stress is provided.

3. Failure analysis of cutting-edge power GaN devices aged by thermo-mechanical stress during PC test

➢ Thermal conductivity degradation of the DUT during PC test has been observed. It is confirmed by non-destructive inspection (SAM analysis) that the cause of this failure is the solder delamination between a discrete GaN chip and an Al PCB by thermo-mechanical stress.

➢ An IDSS failure phenomenon that has not been reported in previous PC tests with Si-based and SiC-based power devices has been found at the end of PC test.

➢ A hypothesis of the IDSS failure able to be induced by complete solder delamination has been suggested. Although this hypothesis had been verified by supplement tests and cross-sectional SAM analysis, it was eventually proven that this hypothesis cannot explain this failure. The failure mechanism according to the hypothesis, however, may be a latent risk factor for the future. The solution to avoid the potential risk, hence, has been proposed.

➢ The IDSS failure phenomenon able to be induced by thermal or thermo-mechanical stress has been analyzed based on collected data during PC test and the literature. The new analysis results narrow the various possibilities that can be a cause of IDSS failure. Finally, two possibilities, a new failure phenomenon by overheating and dielectric crack in a GaN HEMT die, remain.

4. Methodology to optimize the performance of a GaN power device

➢ Various design and structure factors that can affect the performance of the GaN HEMTs have been reviewed extensively. These factors have been analyzed one by one using statistical analysis and TCAD simulation results. Critical factors that can significantly improve device performance and reliability have been proposed objectively through the analysis results.

➢ A DoE methodology based on statistical knowledge to optimize the performance of GaN HEMTs has been suggested with the previously confirmed critical factors. The methodology can ensure a reasonable result analysis as well as an efficient experiment plan.

6.3. FUTURE WORK

Some other interesting and relevant topics are identified in the process of the project. The significant research subjects that can be considered for the further studies are listed as follows.

1. **Dynamic on-state resistance characteristics for commercial GaN devices**

GaN HEMTs fundamentally have a chronic charge trapping issue. This phenomenon contributes to various failures and degradations of the GaN HEMTs. A dynamic on-state resistance ($R_{DS(ON)\_Dyn}$) is reflecting this phenomenon. An on-state resistance measured within a few microseconds after turn-on of a GaN HEMT has a higher value compared to a static resistance $R_{DS(ON)}$, and the resistance is defined as $R_{DS(ON)\_Dyn}$ at this point. For datasheets of almost GaN HEMT products, this information is missing. This characteristic becomes more critical as the frequency becomes faster. Besides, the many designers want GaN devices to be used for high-frequency power electronic applications. This feature requires a more research, such as measurement methodology and trap generation mechanisms, in the power electronic applications.

2. **Finite element method (FEM) simulation with the laminated embedded package technology**

An advanced GaN device tested in Chapter 3 and 4 is using the laminated embedded package technology to minimize stray inductance in a package. This package does not have bond wires. This structure allows an IR camera to read a temperature very similar to the real junction temperature, which was verified by the only static FEM simulation and IR camera measurement. However, supplement stress analysis is needed to understand a failure mechanism led by thermo-mechanical stress genuinely. The new temperature and stress FEM simulations in dynamic operation are required. They can be useful knowledge to investigate the reliability and performance of power GaN devices. Currently, 3D physical model of a GaNPX package have been secured through reverse engineering analysis, and FEM simulation for thermal stress analysis is in progress. We have not yet reached conclusions regarding this simulation so that this result will be covered in other publication.

3. **Failure mechanism investigation of PC test with different thermo-mechanical stress conditions**

In the literature regarding the PC tests with an IGBT, different failure mechanisms had been found by temperature swing conditions in PC test. The stress conditions of these tests in this thesis had been accelerated compared to the typical operation in the field. Although lower temperature swing condition needs longer test time, the failure mechanism of the PC test with the lower temperature swing is close to the real

operation. Therefore, additional PC tests with lower temperature swing conditions and failure analysis can be performed for the reliability study of GaN HEMTs.

4. Reliability assessment of GaN devices with other package types

Currently, commercial GaN devices are using many kinds of package technologies to fulfil the performance of their products. Failure mechanisms of PC tests may be diverse by the package types of GaN devices. Hence, PC tests with a GaN device using a specific package technology can be an interesting topic.

5. Lifetime estimation and reliability assessment

The lifetime of a GaN device in power electronic applications under the give mission profile can be estimated with a lifetime model built by PC test results. The lifetime model of GaN devices can be developed with PC tests results with different temperature swing conditions under the same mean temperature.

6. Failure diagnosis and prediction of a GaN HEMT device during operation

A power electronics technology is widely used in various applications; transportation, consumer device, and automotive application. A power device such as a GaN HEMT is a critical part of power electronics systems. If unexpected faults of the power device in operation happen, these failures may cause severe problems. For this reason, fault diagnosis is one of the emerging research subjects. The fault diagnosis methodology for GaN devices can be developed by utilizing the characteristics information monitored during PC tests. The technology can not only inspect the faulty devices but also predict the danger of power electronics systems in advance.

7. Extra failure analysis of IDSS failure induced by PC test

The possibility of overheating or internal dielectric breakdown is raised as a cause of the IDSS failure phenomenon newly found in the PC test in Chapter 4. To completely understand the failure mechanism, additional PC tests are required with the temperature swing condition that does not exceed the maximum operating temperature (150 Celsius degrees) allowed in the datasheet at the end of the test. If the similar IDSS failure is seen in the additional test results, physical failure analysis could be carried out to inspect dielectric crack inside the GaN HEMT die. At present, PC test with $\Delta T_J = 100\ °C$ condition from 24 °C to 124 °C has been completed and an additional physical analysis with photon emission microscope (EMMI) is underway

with the failure sample. We have not yet reached conclusions regarding this experiment so that this result will be covered in other publication.

8. **Performance and reliability assessment of optimized GaN HEMTs based on the DoE mentioned in Chapter 5.**

The DoE methodology to optimize the performance of a power GaN HEMT has been introduced in Chapter 5. Currently, these samples reflecting this DoE are in production. The completely manufactured GaN HEMTs can be characterized and the best conditions of critical factors can be predicted. The reliability investigation of the devices, as well as the performance assessment, also can be performed.

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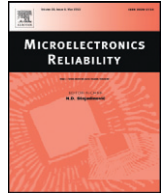
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Failure mechanism analysis of off-state drain-to-source leakage current failure of a commercial 650 V discrete GaN-on-Si HEMT power device by accelerated power cycling test

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ABSTRACT

A gallium nitride on silicon substrate (GaN-on-Si) high-electron-mobility transistor (HEMT) power device is commercially available. The package-level reliability of a GaN-based power device is necessary to respond market demands. Power cycling (PC) tests are a useful method to investigate the reliability of a packaged power component closer to a real application. An off-state drain-to-source leakage current failure (IDSS) of a 650 V discrete GaN-on-Si power device under PC test was reported in a previous study. In this paper, to investigate failure mechanism from the last study experiments to verify the root cause are conducted. Scanning acoustic microscope (SAM) images of failure samples exhibit the solder delamination between the discrete chip and the lead frame. The reasonable hypothesis of a correlation between the delamination and IDSS failure is suggested and is tested with a detailed analysis and supplemental experiments. In the process of analyzing the above hypothesis, the new risk of IDSS failure caused by losing electrical connection of silicon substrate rises. The solution for the risk also is proposed. It is discussed that the IDSS failure phenomenon is related to thermal stress induced during PC test. The tests and the analysis indicate that the failure is a thermal stress induced IDSS leakage, not matched previously reported mechanisms.

1. Introduction

A GaN-on-Si HEMT power device can ensure not only better electrical performance but also cost-efficiency as a key component in the power electronic applications. End-user markets expect the same level of reliability as existing silicon-based devices [1]. The reliability evaluation of a power component is generally classified into three groups; a semiconductor device, package, and ESD [2–4]. Most studies on the reliability of GaN-based power devices to date have focused primarily on the device [5]. Research on the other two areas is necessary for product-level balanced reliability.

In a previous study mainly focused on PC test in reverse conduction, it was reported that prolonged PC led to an increase in IDSS with commercial 650 V GaN-on-Si devices [6]. The same IDSS failure for the same type device has also been reported in PC test with forward conduction [7]. The previous studies had only reported failure mechanism for degradation of thermal dissipating structure, but there is no description of IDSS failure related to PC test in [6,7]. This phenomenon is unlike the existing reports the PC tests results of silicon-based power devices [8,9]. The leakage current issue can cause severe problems such as

short-circuit, which can put the power device itself as well as peripheral elements in danger in the real application [10]. Therefore, a failure mechanism analysis for this phenomenon is important for preventing this serious damage.

In this paper, the failure mechanism of an IDSS increase under PC test [6,7] with a commercial GaN-on-Si power device is analyzed. Based on the results, a suspected hypothesis of failure is presented and tested with targeted analysis methods.

2. Experiment description and results

2.1. Device under test description

A power cycling test employs heat induced by power losses in the GaN-on-Si semiconductor die as a repetitive stress source. The heat ultimately leads to thermo-mechanical stress from the differences of coefficient of thermal expansion (CTE) of each layer comprising the device under test (DUT). The CTE mismatch accelerates degradation of the DUT. The DUT is comprised of a discrete GaN power component, solder joint, an aluminium printed circuit board (Al PCB), thermal interface metrical and Al heat sink as in practical applications. The Al PCB provides higher thermal conductivity 3 W/m-K [11] then FR4-based PCB.

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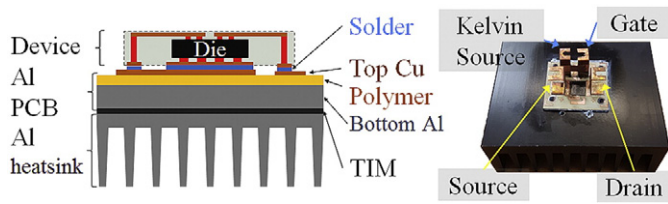 *E-mail address:* sso@et.aau.dk (S. Song).

Fig. 1. Layer section view and an image of a DUT.

This PCB can be used below 180 °C. Fig. 1 displays a cross-sectional structure [6] and an actual image of the DUT.

The solder joint is one of the critical factors for a DUT in general power cycling tests [9]. The electrical connection of the discrete GaN device under study here is divided into four parts; gate, source, drain, and thermal pad (TPAD). The TPAD connected to the Si-substrate is electrically isolated from the other three terminals internally the discrete component. It serves to transfer the heat generated in the junction out of the package. Fig.2 a) displays the electrical connections and Fig.2 b) shows the electrical pads of the discrete component to be tested. According to the instructions from the manufacturer [12], the TPAD should be electrically linked with the source potential via the lead-frames on the Al PCB.

2.2. The PC test experiment details

The stress condition employed in this power cycling test is $\triangle T_j = 125$ °C and the power dissipation time = 1 s. The temperature swing from 25 °C to 150 °C for the power dissipation period. 150 °C is the maximum junction temperature recommended by a manufacturer [13]. Cooling time is 2 s. The control strategy and principle employed in the power cycling are described in detail in [6,7]. The junction temperature of the DUT (T_j) under operation is indicated by measuring the top side of a package with a high-performance infrared (IR) camera.

In line with the previously used method in [6], five criteria-parameters are monitored during the PC test, which indicates abnormality of the DUT. R_{DS_MX} represents the maximum value of the resistance calculated by the current and the V_{DS} measured during one PC. R_{DS_MX} is measured at the end of the current injection, which is also at the highest temperature. R_{DS_ON} is measured in a curve tracer in offline test set-up with 9 mA and current pulse 200 us. $\triangle T_j$ and R_{DS_MX} are monitored every few hours in real time during PC, and curve tracer evaluation is done in between cycling periods.

2.3. The result of PC test

Fig.3 illustrates measured temperature with IR camera and electrical characteristics data of three DUTs Fwd.#1, Fwd.#2, and Fwd.#3 during PC test [7]. $\triangle T_j$ and R_{DS_MX} of them remain almost constant up to a large number of cycles, and they are gradually increasing after around 15 or 30 kcycles. Generally, R_{DS_MX} changes corresponding to the temperature rise [13]. It is measured that the variation ratio of R_{DS_ON} with temperature is 0.84 mΩ / °C from an additional test with the same device, which is in reasonable agreement with the calculated change in
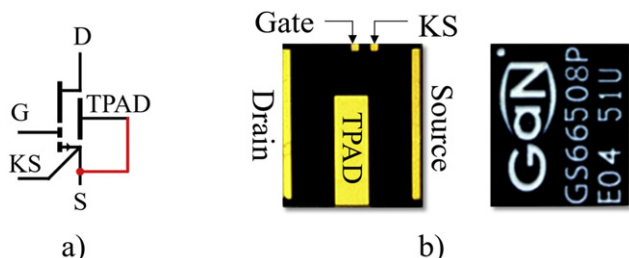
R_{DS_MX} versus $\triangle T_j$ in Fig. 3 [7]. In contrast, there is no significant change of offline-measured R_{DS_ON} in room temperature. It means that the degradation of thermal resistance progresses without any decline of electrical characteristics. After the R_{DS_MX} exceeds the initial value with +20%, IDSS failure is also indicated in two tested samples. This phenomenon will be discussed in the next section.

It was observed that the root cause of thermal conductivity decrease was the solder layer fatigue in the last study [6,7]. The solder layer damage was investigated in a KSI V_8 scanning acoustic microscope (SAM) from IP Holding. Fig.4 shows the SAM images of each DUT before and after PC test. There is discernible delamination of solder layer under TPAD area of the discrete GaN device. On the other hand, there are no signs of abnormality in the solder layer under the electrical connection; source, kelvin source, gate, and drain. The solder fatigue results are similar to the previous researches on PC test of a power device or module [6,7,9]. It is confirmed that two of the three samples above tested [7] and three samples of [6] have IDSS failure phenomenon at the end of power cycling test. This represents a trend between IDSS failure and PC test.

3. IDSS failure mechanism induced by complete solder delamination

As mentioned above, a delamination of the solder under TPAD in a discrete chip had been indicated at the failure of PC test. The solder layer electronically connects the source potential to the Si-substrate inside a GaN die via the TPAD and simultaneously transfers the heat from active region to the Al PCB. Thus, the degradation may lead to two different cases that can stress the device; electrical field stress and/or thermal abnormality. It is reported in the literature [5,14,15] that especially field stress can degrade GaN HEMT. The maximum drain-to-source voltage strength of DUT during PC is under 5 V, which is not high enough to represent an electrical stress due to loss of source connection, but the DUT receives thermal stress repeatedly during PC. In the curve tracer performed in offline PC test, the device is not under thermal stress, but higher electrical field stress is applied between drain and source under the IDSS test condition. In this case the loss of source connection, as indicated by SAM, may lead to device failure.

The hypothesis, in this case, is that failure is induced by a sequence of events. The IDSS failure is induced by entire delamination of solder layer under TPAD. The TPAD is electrically connected to Si-substrate in the GaN-on-Si device. In the discrete device, the TPAD is not connected to any of the electrodes (source, gate, or drain). For this reason, the manufacturer requires the user to externally connect the TPAD to source potential via the PCB to ensure correct performance of the device. It is strictly forbidden for TPAD to connect to drain or gate or to keep electrical floating in [12]. The TPADs of all the DUTs were connected to the source via Al PCB before the PC tests. If a complete delamination occurs in the TPAD region during PC, this means that the silicon substrate inside the device is electrically disconnected from source. As mentioned above this can lead to electrical breakdown of the device.

4. Si-substrate (TPAD) connection impact

In the lateral high voltage (HV) power device such as GaN HEMT, the Si-substrate electrical connection can affect the leakage current measured at higher drain voltage condition. Generally, a HV GaN HEMT device has a field plate between gate and drain to maximize breakdown capability under limited dimension [16]. The field plate reduces the peak electric field strength caused by the drain high potential. In GaN-on-Si HEMT structure, Si substrate may play a similar role as the field plate. In a structure analysis of the tested device type, the distance between Si substrate and 2DEG channel is very close to 4.3 μm [17]. Considering the distance 7.5 μm from drain to the end of an edge in a structure of a device having similar breakdown capability [18] the influence of the Si-substrate on the electrical field is expected to be
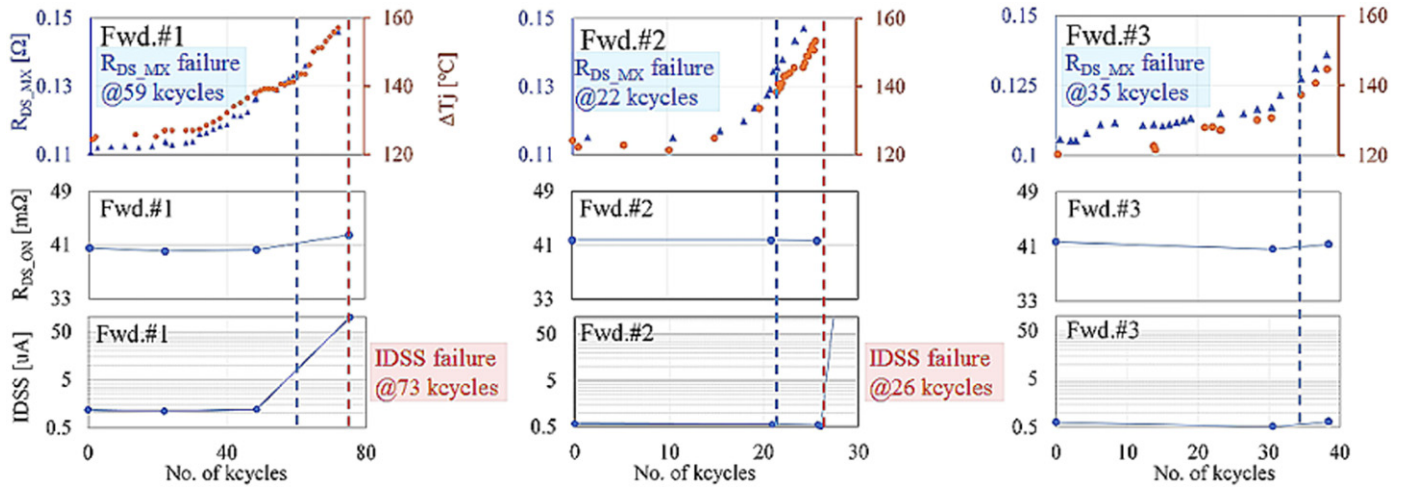

Fig. 2. a) Electrical connection of TPAD and b) Electrical pad information.

Fig. 3. Measured $\triangle T_j$ and R_{DS_MX} during PC test & R_{DS_ON} and IDSS versus the number of kcycles.
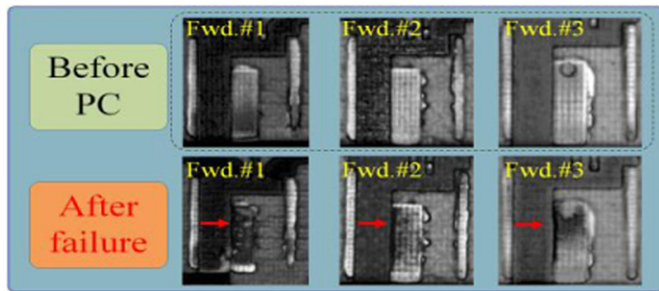

Fig. 4. SAM image of DUTs before and after PC test.

large. Fig. 5 shows supposed electric field concentration to field plate edge and the dimension of gate-to-drain and thickness of GaN layer.

In order to verify this a dedicated experiment was carried out to prove the Si-substrate floating effect. A test sample with separated source and TPAD (Si-substrate) is built up on a PCB. In the first step, IDSS is 10-times measured in the connection of source and Si-substrate with an external wire and the same leakage current level is obtained each time showing the reproducibility of the test. Subsequently, the TPAD is manually disconnected and the IDSS measurement is repeated. The wire-cutting progressed under ESD safety precaution. The leakage current increases 16 times in floating Si-substrate condition compared to the connection condition. Fig. 6 exhibits the IDSS of 10 times repeated measures under the source connection of TPAD and increased IDSS after electrical floating of TPAD. The two tested samples were destroyed around 500 V during these IDSS measurements. Therefore, the test result supports the hypothesis that the higher electrical field biased during the leakage current measurement can destroy the device with disconnected TPAD in a lower voltage range than the allowed the maximum drain voltage (650 V) in the off state.
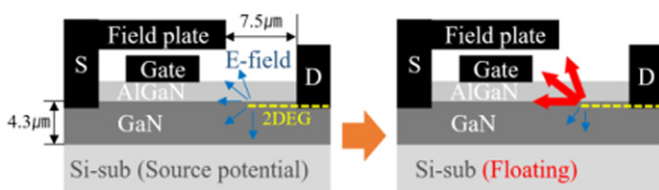
The proposed hypothesis requires a complete electrical disconnection by delamination on the entire TPAD region. Even though the GaN component does not provide a separate connection way to measure the electrical isolation of the TPAD relative to the Si substrate, the connection can be verified by investigating changes in output capacitance (C_{OSS}) of each DUT. The C_{OSS} is a sum of gate-to-drain capacitance (C_{DG}), drain-to-source capacitance (C_{DS}), and drain-to-substrate capacitance (C_{DSub}) (see Fig. 7). If there is a complete delamination in the solder layer, obviously, there should be a decrease in C_{DSub}. This decrease will in turn affect C_{OSS} before and after PC test. To quantify the effect various calculated and measured capacitances ware evaluated.

Fig. 7 illustrates the physical origin of each of these capacitances and estimated C_{Dsub} with and without source potential of Si-substrate. If complete delamination of the solder layer occurs after PC test, C_{DSub} should be converted to a series-connected two capacitors C_{DSub} and a capacitor substrate-to-source (C_{SubS}) with an air gap (assumed air gap thickness of 4um). The permittivity of GaN and air are around 8.9 and 1 respectively. Assuming area and thickness of dielectric material are the same between both capacitors, C_{SubS} should be around 1/9 of C_{DSub}. Based on the above calculations a reduction of around 20% C_{OSS} is expected in case of electrical disconnection due to delamination.

In order to show the effect of the TPAD connection on the Coss the above-tested sample with separated source and TPAD was used. C_{OSS} in connection and disconnection between the source and Si-substrate are 478 pF and 397 pF respectively measured under 0.1-V bias. The capacitance is decreased by around 17.0%, which is in good agreement with the estimated values based on the geometry. Thus, the potential electrical disconnection due to thermal pad degradation can be investigated by measuring the capacitance of the stressed devices.

To provide an overview of the potential electrical disconnection of the power-cycled DUTs the results of C_{OSS} values measured before PC
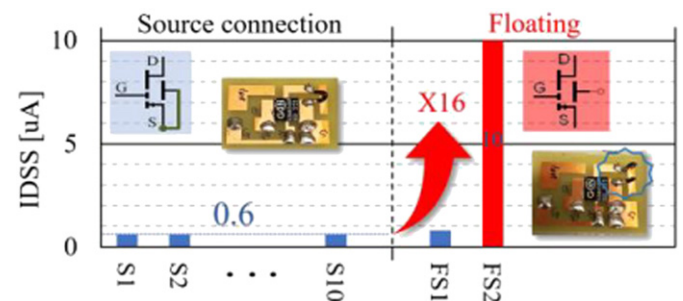

Fig. 5. Effect of floating Si-substrate on electrical field distribution and dimension information.

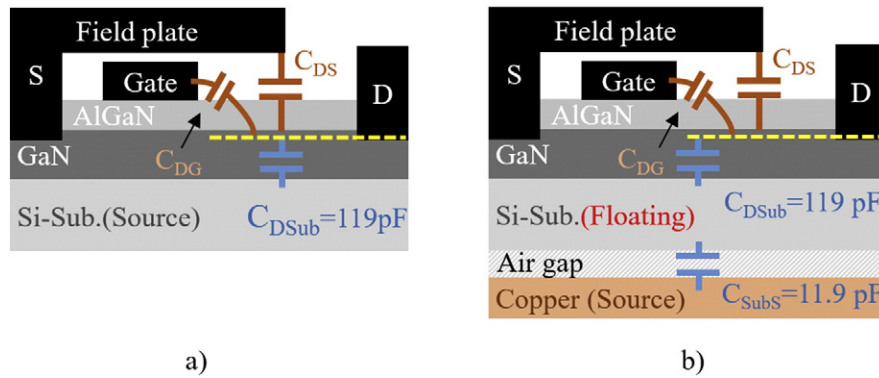**Fig. 6.** An experiment to prove Si-Substrate floating effect.

Fig. 7. Composition of C_{OSS} a) with source potential on Si-substrate b) with complete solder delamination.

test as well as after failure detection are summarized in Table 1. In addition to the presented samples from forward conduction power cycling [7] it also includes three samples tested with reverse conduction mode from [6]. In all samples, no significant change in Coss is seen after failure. Thus, it is confirmed that the observed delamination does not lead to electrical disconnection between source and Si-substrate in the solder layer after IDSS failure. This in turn implies that the observed IDSS is not likely due to field-stress related breakdown during the IDSS leakage measurement. Since, as mentioned previously, the device is only support a minor VDS of 5 V during the PC there is no external source of electrical stress. Thus, the combined observations and analysis indicate that the IDSS failure must be caused by a different effect.

During the PC test the tested DUTs are exposed for long time by accelerated thermal stress. In the applied PC tests, the maximum operating temperature allowed for the device was set up from the beginning. As the thermal contact starts to degrade due to degradation the DUTs are exposed with exceeding maximum operating voltage (150 °C) every cycle. The temperature increases close to failure. The thermal stress can have a negative impact on GaN HEMT power devices [5]: thermally-induced delamination of passivation [19] and pits in AlGaN layer under high-power-tested condition [15].

5. Leakage localisation analysis

To understand the IDSS failure mechanism in the GaN HMET structure in more detail it is interesting to analyze the leakage localisation. The measured IDSS of DUT in a curve tracer is defined as the current between source and drain with $V_{GS} = 0$ V and $V_{DS} = 650$ V. The current can flow through four paths; from drain to source on the Al PCB surface and from drain to source, from drain to gate, and from drain to substrate (TPAD) in the discrete device. The sum of these four leakage currents should be the total IDSS measured between drain and source in the DUT. To identify the main leakage path of the IDSS, firstly the discrete chip is detached from one sample (Rev.#3 from DUT [6]) after IDSS failure using desoldering.

Firstly, the leakage current between drain and source leads was measured on the Al PCB after removal of the discrete device. The leakage current on the Al PCB surface is found to be in femtoampere level at 650 V, thereby showing that the IDSS failure is not caused by an Al PCB leakage path.

Table 1
Measured C_{OSS} before PC test and after IDSS failure.

Sample	C_{OSS} [pF] before PC	C_{OSS} [pF] after IDSS failure
Rev.#1	536	531
Rev.#2	536	544
Rev.#3	541	–
Fwd.#1	–	528
Fwd.#2	–	536
Fwd.#3	530	526

Secondly, the three leakage paths in the discrete device detached from the Rev.#3 DUT; drain-to-source, drain-to-gate, and drain-to-substrate, was investigated using four amperemeters. A probe station is used to electrically contact to four electrodes; gate, source, drain, and substrate. The circuit to measure each leakage component was conducted outside the device. Fig.8 shows this test environment and the result of measurement. The two components; drain-to-gate and drain-to-substrate leakage currents, are a small part of the total IDSS. On the other hands, the source-to-drain leakage current component dominates the total IDSS. This shows that the major leakage path of the IDSS failure is between source and drain.

6. Discussion

Potential failure mechanisms for GaN HEMT device were presented in Ref. [20] where a list of nine failure candidates were listed. They are largely divided into three categories according to the root cause of the failure; hot-electrons induced, GaN-material-related, and thermally-activated failure mechanism.

Firstly, the hot-electrons induced two failure mechanisms are based on electron trapping in the SiN passivation, the AlGaN, or the GaN layer [20]. It should lead to an increase in on-state resistance. However, since there is no significant change of the resistance at failure of devices tested here, this mechanism cannot explain the IDSS failure. Secondly, there are the GaN-material-related three failure mechanisms; gate-edge degradation [15], trap generation due to the electro-thermo-mechanical failure [14], and punch-through effect [21]. It was demonstrated in [14] that the gate-edge degradation and trap generation due to the electro-thermo-mechanical failure can lead to rising gate-to-drain leakage current after stress. However, from the above leakage localisation test done on the device tested here, there was no degradation of the drain-to-gate leakage current, so this mechanism is also disregarded. The punch-through effect can be in GaN layer underneath gated channel
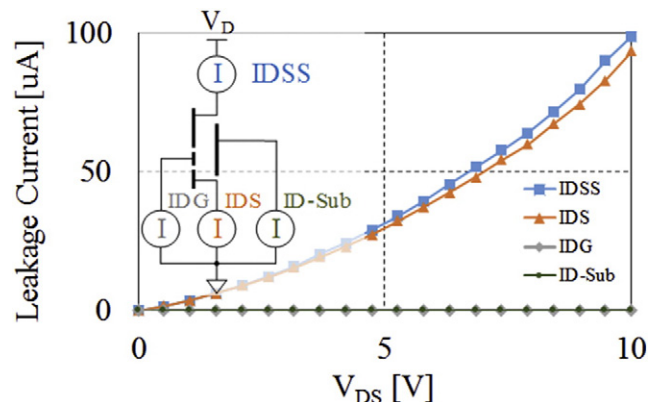

Fig. 8. Analysis of leakage localization after IDSS failure.

region. The effect should be accompanied by degradation of source-to-drain leakage current as well as changes in threshold voltage, and on-state resistance. Since the no significant variation in either threshold voltage and on-state resistance was observed here this detailed mechanism does not seem a plausible cause either. Thus, these three mechanisms also cannot describe the IDSS failure phenomenon in PC test.

Finally, there are four types of thermally-activated mechanisms; feed metal interconnect degradation, ohmic contacts degradation, gate metal degradation, and delamination of passivation. The first three mechanisms are more inherent to the metallization scheme. Since they should lead to a degradation of on-state resistance, the three mechanisms do not apply to this IDSS failure. The delamination of passivation can be induced by continues thermal-mechanical stress. In this test, T_{jmax} had risen to over 180 °C at IDSS failure with ΔT_j 160 °C due to the TPAD delamination. This thermal condition poses a very aggressive stress condition compared to operation in a real application. It was reported in Ref. [22] that the delaminate of passivation can lead to a degradation of breakdown voltage, threshold voltage, and on-state current. As mentioned above in this PC test, the only of these parameters that showed degradation was the IDSS without any changes of threshold voltage, on-resistance, or capacitance. Thus, in summary the observations for the power cycling induced failures does not match the reported mechanisms. In the structure of the GaN HEMT, physical damage of AlGaN and dielectric layers between the field plate connected to source and 2DEG connected to drain may lead to the IDSS failure observed in this test. The physical damage of a GaN HEMT device under high-temperature operation stress had been revealed by [23]. Most failure related reports on GaN HEMT are based on RF application using lower voltage range. Therefore, further researches are required to identify the IDSS failure mechanism for the newer higher voltage ranges at the device physics level.

Although it was shown that the proposed mechanism (entire solder delamination) is not the root cause for the observed IDSS failure, the result still shows a possible severe risk in a real application. The problem can be eliminated by adding a source connection of Si-substrate internally in the package or connecting a source potential to Si-substrate in a die.

7. Conclusion

Hypotheses of how solder delamination by PC test affects the IDSS failure were investigated systematically through experiments, analysis and literature review. In the process of investigation, a IDSS failure risk factor that can be induced from complete delamination of solder layer connecting source to Si-substrate is identified and a solution to remedy this is suggested. From the IDSS leakage localisation analysis, it was revealed that the main leakage current path is drain-to-source, not drain-to-gate or drain-to-substrate. Finally, it is suggested that the IDSS failure phenomenon is related to the higher thermal stress generated during PC test.

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Performance assessment of commercial gallium nitride-on-silicon discrete power devices with figure of merit

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Performance Assessment of Commercial Gallium Nitride-on-Silicon Discrete Power Devices with Figure of Merit

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Abstract— **There have been various technical developments of commercial gallium nitride on silicon power devices over the last couple of years since the initial appearance. Efforts have been made to increase threshold voltage and power density, while reducing stray impedance to improve the efficiency of the power conversion systems. In this paper, seven types of gallium nitride-on-silicon discrete power devices on the market are electrically analyzed and compared in the same test environment. To objectively understand the performance of power semiconductor devices, the figure of merit is derived from the measurements to enable a quantitative comparison. The results demonstrate that the power density of the current commercially available gallium nitride power components already goes beyond the theoretical limitation of the silicon material. Moreover, switching capability of commercial gallium nitride-on-silicon devices are found to be fourteen-times-better than that of a state-of-the-art silicon device from the same category.**

Keywords— *wide band gap; GaN-on-Si; commercial GaN-on-Si discrete devices; gallium nitride; electric characteristics; figure of Merit; FOM; power density; switching capability; performance assessment*

I. INTRODUCTION

Wide band gap (WBG) semiconductor materials such as gallium nitride (GaN) and silicon carbide (SiC) are well known alternative to silicon, thanks to a number of superior [1]. Their wide band gap property allows a power device to be more compact, faster, and more efficient than silicon-based devices. Due to the superiority of WBG devices, there has been continued interest in them from the power electronics market. Both GaN and SiC products have already been released on the market. There have been reports of high-end applications with WBG devices such as renewable energy over the recent years [2, 3]. GaN devices are applied to three main fields; radio frequency (RF), light emitting diode (LED), and power electronics, but this discussion will be limited to the power electronics.

Although the GaN devices at present only make up a small part of the entire power devices market, there is a promising outlook which suggests the possibility of development in view of the market and the technology [2]. Firstly, Fig.1 illustrates the current market segmentation of the major power devices for each application [2, 3]. The current WBG market share is
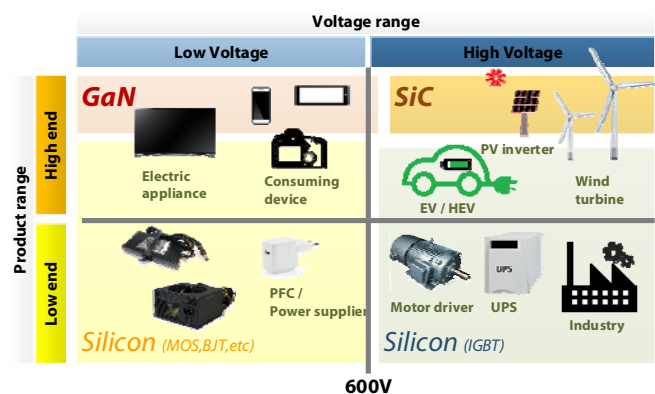

Fig. 1. Market segmentation and applications of major power electronic devices [2,3].

limited to the high-end applications because of the higher prices of WBG devices. However, in the coming years, it is expected that there will be a dramatic expansion of the high-end market as the center of electric vehicles (EV) / hybrid electric vehicles (HEV) and renewable energy applications [3, 4]. The demands of the high-end applications are increasing in the low-voltage range under 600s volt level.

Various efforts are being dedicated to the parts of device and manufacturing as well. The power electronics industry in the medium voltage range has great expectations from the GaN devices. Even though the maximum operating voltage of the commercial GaN devices is 650 V, the technical challenge of pursuing higher voltage applications is going on now. Moreover, a cost reduction may be attained by manufacturing at a higher production capacity by the technology growth of high quality GaN on a 200mm diameter silicon (Si) wafer in the near future [5, 6]. Actually almost all commercial GaN power devices are being manufactured on a Si wafer under 150mm diameter for a competitive price and have a lateral structure. Since the main progress seem to be in the lateral structures the vertical GaN power device using the relatively expensive bulk GaN wafer is not addressed in this paper [7].

Commercial GaN power devices can deliver higher efficiency and lower cost and weight at the system level by operating with high frequency. The benefits of GaN are mainly related to various electrical parameters such as the good on-

resistance, the parasitic capacitances, and the charge factor. The Lateral GaN high electron mobility transistor (HEMT) power devices have substantially smaller parasitic impedance value compared with the silicon power devices in the similar current and voltage range. It means that the GaN power devices can switch with higher speed than the silicon devices. Therefore, the power conversion systems with GaN devices can ultimately achieve less filter size by increasing operating frequency. Thus measurements of such parameters are key when comparing the performance of components on the market. A well-known figure of merit (FOM) in the field of the power device is $R_{DS(on)} \cdot A$ (area) and $R_{DS(on)} \cdot Q_g$, which are used to assess the capacity of each commercial device.

In this paper the performance of commercial state-of-the-art GaN-on-Si power devices is assessed based on measurements and FOMs derived from the measurements. Considering seven types of commercial GaN-on-Si discrete power devices available on the market ware selected as test samples from the three companies EPC, Transphorm, and GaN Systems having bigger market share. To obtain the FOM all the samples ware electrically characterized under the same measurement condition and the semiconductor are was measured by optical microscope. Based on the derived FOMs all the tested devices are compared and their performance evaluated.

II. MEASUREMENT METHODOLOGY

Electrical characteristics of a power device are basic information for a designer to select an appropriate power device. A power device is the crucial component that determines the efficiency of a power conversion system built with a specific converter topology. Representative sample choice and reliable test environment are very important for valuable assessment result. The state-of-the-art GaN-on-Si discrete power devices on the market are chosen for the test based on their power performance and the curve tracer specialized in the analysis of a power device is used for electrical characteristics. The all measurement is progressing at the room temperature 25 Celsius.

A. Test Sample

Current commercial GaN-on-Si power discrete devices contain advanced technologies. Compared with the initial products, they have improved power density and low inductive designs that in turn enable faster operating frequency. Especially the drawback of "normally-on" operation observed in the early versions has already been solved in the current products. The GaN-on-Si discrete power devices on the market may be divided into the enhancement mode (normally-off) type and a cascode type. The power density capability is also being improved by the technical development including developments in thermal management. The superior abilities can be precisely demonstrated by the electric characteristics of the GaN devices and the comparison of their FOMs to the state-of-the-art silicon devices. The seven sorts of GaN-on-Si investigated in this assessment reflect the stat-of-the-art technology of commercial GaN-on-Si discrete power devices.

TABLE I.   INFORMATION OF TEST SAMPLES DATA SHEET [8-14]

Name of Sample	Information of samples				
	Company	$V_{DS\_MAX}{}^{a}$ *[V]*	$I_{ON}{}^{b}$ *[A]*	$V_{GS\_R(ON)}{}^{c}$ *[V]*	*Package solution*
EP-30	EPC	30	60	5	LGA [15]
EP-60		60	60	5	
EP-100		100	60	5	
EP-200		200	8.5	5	
GS-100	GaN Systems	100	90	7	GaNPX [17]
GS-650		650	30	7	
TR-600	Transphorm	600	17	8	PQFN [16]

a. V_{DS_MAX} : Drain to source maximum operating voltage from data sheets

b. I_{ON} : Continuous Drain to source current in on-state at 25 ℃ from data sheets

c. $V_{GS\_R(ON)}$: Gate to source maximum operating voltage from data sheets

Table I shows the basic information for each sample as obtained from the datasheets provided by the manufacturer. The commercial GaN-on-Si discrete power device guarantees a maximum drain to source voltage of 650 volt. Commercial GaN-on-Si discrete devices have wider product lines from 15V to 650V. Firstly, representative voltage ranges of GaN-on-Si power devices are defined considering major applications, and seven commercial GaN-on-Si devices having the best performance in the same voltage range are chosen. In terms of a package technology, various advanced solutions are employed for all test samples to enable the use at their full potential.

B. Test environment

The test environment is divided into three parts; measurement instrument, test fixture including device under test (DUT), and test condition. Firstly, the curve tracer model B1506 from Keysight Technologies is used for electric characteristics of each device. In general, a GaN-on-Si discrete power device is packed in a surface mount device (SMD) to minimalize stray inductances in the application. However, SMD components it is not straight to connect SMD devices to curve tracers and similar instruments. To connect SMD devices to the measurement instrument, seven test fixtures ware designed using special print circuit boards (PCB) for surface mount and terminal legs that enable the DUT and test fixture to fit into standardized slots in the curve tracer. Each GaN chip is attached on the test fixture PCB using solder paste and vacuum soldering in a reflow oven. The DUT is connected on the curve tracer via the test fixture PCB with terminal legs. Since the EPC-30, EPC-40, and EPC-60 have the same footprint the test fixtures are identical for these components.

Fig.2 illustrates an example of the test fixtures and the measurement instrument. This enables the measurement of the following characteristics; threshold voltage, on-resistance, off-leakage current, parasitic capacitances, and gate charge, which are key parameters when assessing the performance of the devices.
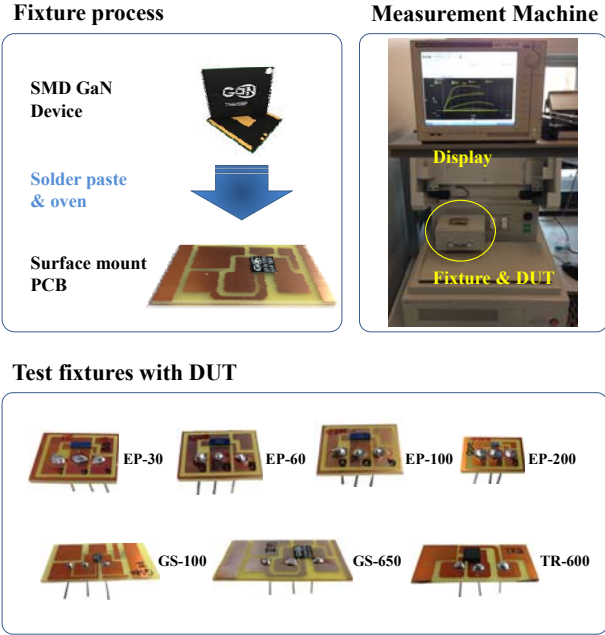
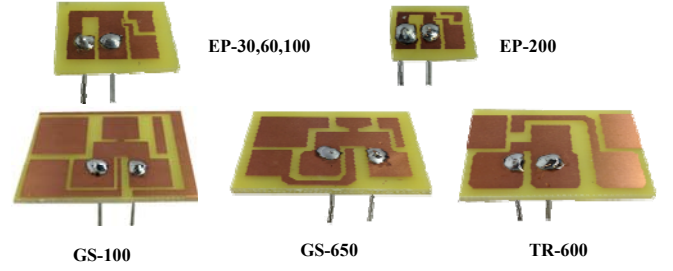Fig. 2. Fixture process, test fixtures, and measurement machine.

Fig. 3. PCBs for measuring parasitic resistances of the test fixtures.

C. On-resistance compensation

Since GaN-on-Si power devices have a smaller on-resistance than conventional power devices are easily affected by parasitic resistance from the test setup or the test fixtures used here. Therefore, a compensation of a measured resistance value is needed to be able to get an accurate result. The basic principle is that if the parasitic resistance ($R_{fixture\_para}$) of the fixture is known, the more correct $R_{DS(ON)}$ can be obtained as follows:

$$R_{DS(ON)\_fixture\_DUT} - R_{fixture\_para} = R_{DS(ON)} \tag{1}$$

Five PCB boards are designed to evaluate the parasitic of each of the types of fixtures shown in Fig. 3. The drain to source of a PCB is shorted by design change that still maintains the footprints of device test fixtures.

III. CHARACTERISTICS AND FIGURE OF MERIT

A. Electrical characteristics

1) Static characteristics

Table III gives the measured static characteristics of each test sample. The threshold voltage is voltage biased gate-to-source at transition from off-state to on-state. Basically, almost any commercial GaN devices have a positive voltage range from 1.28 V to 1.75 V. The cascode GaN transistor (TR-600) has a little bit higher threshold voltage than others because it follows a low-voltage (LV) silicon metal-oxide semiconductor field-effect-transistor (MOSFET) in series with a depletion GaN device [18]. The threshold voltages are decided by gate technologies, which realize normally off. Although four samples from EPC share the same gate technology, a little larger variation is confirmed. The on-resistance signifies the resistance factor between the drain and source in the on-state. Normally it is measured at the fully enhanced gate voltage because of sensitivity to gate voltages. These conditions follow datasheet of each device. $R_{DS(ON)}$ data of Table III is compensated with the procedure previously described. The on-resistance is a major performance factor reflecting the on-state power loss. For this reason, it is good criteria of performance assessment. It exactly trades off with the other parameters such as the size of die, leakage current, and various stray capacitances. The measured on-resistance will be utilized with dynamic characteristics in the figure of merit section to discuss devices performance for power conversion applications.

Table II shows the electrical test conditions of these characteristics. The test conditions are based on the each datasheet provided from manufactures [8-14]. The test methodologies are consistent between the manufactures. The conditions to define parameter values are fine-turned with a common concept by each parameter. They are similar to this definition conditions on the datasheets. The V_{th} condition is that when the gate and drain is the same node, the gate-to-source voltage is specified as the gate voltage at I_{DS}=0.03 %·Ion. The on-resistance is extracted at the proposed gate voltage on datasheet and the 30 % of the continuous drain current in on-state. I_{DSS} is defined by the drain-to-source off-state leakage current at the maximum operating drain voltage. In the dynamic characteristics, the capacitance is measured in the off-state (V_{GS}=0V) and 80 % of drain voltage maximum voltage from data sheet. Q_g is the amount of the gate charge required to increase from zero volt to the desired driving gate voltage. The initial condition is $V_{GS} = 0$ V and $V_{DS} = 50$ % of V_{DS_max}.

TABLE II. TEST CONDITIONS OF STATIC AND DYNAMIC CHARACTERISTICS

Parameters		Description	Condition
Static	V_{th}	Threshold voltage	V_{DS}=V_{GS}, V_{GS}@I_D=0.03%·I_{on}
	$R_{DS(ON)}$	On-resistance	V_{GS}= $V_{GS\_R(ON)}$, R_{DS}@I_D=30%·I_{on}
	I_{DSS}	Leakage current	V_{GS}=0 V, I_{DS}@V_{DS}=V_{DS_max}
Dynamic	C_{ISS}, C_{OSS}, C_{RSS}	Capacitance	V_{GS}=0 V, V_{DS}=80%·V_{DS_max}
	Q_g	Gate charge	V_{GS}=0 to $V_{GS\_R(ON)}$, V_{DS}=50%·V_{DS_max}

TABLE III.   MEASURED STATIC CHARACTERISTICS IN ROOM TEMPARETURE

Name of Sample	Parameter [units]			
	V_{th} [V]	$R_{DS(ON)}$ [mΩ],Tj=25℃	$R_{fixture\_parasitic}$ [mΩ]	I_{DSS} [uA]
EP-30	1.52	0.97	5.02	101.1
EP-60	1.75	1.13	5.02	40.9
EP-100	1.28	1.54	5.02	92.9
EP-200	1.52	31.63	6.19	6.3
GS-100	1.62	6.33	2.70	0.5
GS-650	1.50	42.14	2.90	0.1
TR-600	2.26	150.6	3.24	2.2

Name of Sample	$R_{DS(on)}$ [mΩ]	Parameter [unit]				
		C_{ISS} [pF]	C_{OSS} [pF]	C_{RSS} [pF]	Q_g [nC]	Q_{RR} [nC]
EP-30	0.97	2418	1437	24.0	21.4	
EP-60	1.13	2200	969	3.9	19.2	
EP-100	1.54	1493	868	4.0	15.1	
EP-200	31.63	260	106	3.2	2.9	-
GS-100	6.33	408	212	30.5	11.0	
GS-650	42.14	289	75	13	14.6	
TR-600	150.6	801	56	8	10.6	54
FCH077N65F	68	4600	96	13	126	900

I_{DSS} means the entire drain-to-source leakage current under off-state. It is measured at the maximum operating drain voltage (V_{DS_MAX}) of each device and room temperature. The difference in between the devices of GaN systems and other companies (EPC and Transphorm) is obvious. I_{DSS} of GS-650 and GS-100 are only 5% of TR-600 and 0.5% of EP-100 respectively. The better leakage current performance of the devices from GaN systems is confirmed. This current can be a significant source of power loss in certain power applications [19]. Therefore, it should be considered when designing a power conversion circuit.

2) Dynamic characteristics

The switching energy loss of power conversion systems is induced when a change from the on to off-state or off to on-state happens [14]. It is affected by the three parasitic capacitances (C_{GS}, C_{GD}, and C_{DS}) of the DUT; gate-to source, gate-to-drain, and drain to source capacitances. In this test, the total capacitances are expressed by measured values at input and output terminals. Equation (2) explains the relationship between parasitic capacitance and capacitance in each terminal. These parasitic capacitances determine the charge (Q) that is required to get to the desired voltage at each terminal. Consequently, a smaller charge and capacitance enable a faster switching operation under the same driving condition.

$$C_{ISS}=C_{GS}+C_{GD}$$
$$C_{OSS}=C_{GD}+C_{DS} \quad\quad (2)$$
$$C_{RSS}=C_{GD}$$

These parasitic capacitances can be measured built-in routines of the B1506 curve tracer. It is verified that parasitic capacitances of the test fixtures had no impact on the measured values. The previously measured static on-resistances are added on the table IV for better understanding. C_{ISS}, C_{OSS}, and C_{RSS} are measured in 1MHz frequency, V_{GS}=0V (off state), and 80% V_{DS_MAX}. The gate charge (Q_g) is calculated by time integration of current flowing into gate terminal when a gate voltage is driven from zero to fully enhanced gate voltage. An initial drain voltage is 50% V_{DS_MAX}, and the fully enhanced gate voltage are $V_{GS\_R(ON)}$ in table I.

Table IV exhibits the measured the dynamic characteristics of the commercial GaN-on-Si devices. Data for from a datasheet for a state-of-the-art silicon super-junction (SJ) MOSFET (FCH077N65F) from Fairchild is added as a reference power device with a similar on-resistance to GS-650 [21]. It has the same maximum drain voltage level 650V and the similar on-resistance to the GS-650 sample. The dynamic characteristics of the silicon device are based on datasheet and are defined by the conditions in Table II [21]. The all results of GaN-on-Si devices except the Q_{RR} of TR-600 are measured in this test.

The tested commercial GaN-on-Si devices show a much better dynamic characteristic compared to the state-of-the-art silicon device. C_{ISS} and C_{OSS} are observed at the capacitances of input terminal and output terminal respectively. Firstly, the noticeable result is that C_{ISS} of GS-650 is eleven times smaller than the state-of-the-art silicon SJ MOSFET. The difference appears to be similar with Q_g parameter because Q_g is determined by C_{ISS}. Q_g is the amount of charges at the gate (input terminal) required to increase from zero to the target gate voltage. The smaller charge implies a faster switching operation in the same driving current of the gate driver. The Q_g of GS-650 is nine times smaller than FCH077N65F. It is key information for a designer to define operating frequency of a power conversion system.

There is the one more marked advantage of a GaN power device. Q_{RR} is the reverse recovery charge stored in the body diode of a silicon power device when the diode is in ON state. It is also the dissipated charge when the diode turns OFF and the opposite device in a bridge turns ON. This element does not exist or is insignificant in the GaN-on-Si power device because they do not have a body diode [7]. However, the cascode GaN devices have Q_{RR} from the low-voltage silicon device which is a small disadvantage.

Briefly, the commercial GaN power devices have the better dynamic characteristics compared to the state-of-the-art silicon power device. Considering the history of the silicon devices, the GaN-on-Si power devices at the early stage obviously have huge potential for improvement.

B. Figure of merit

FOM represents the quantitative performance of a particular device or technology. It makes understanding much easier why a GaN power device is excellent and where they should improve. For the discussion of the performance of the tested commercial GaN-on-Si discrete devices, two FOMs are applied; $R_{DS(on)}\cdot$Area (A) and $R_{DS(on)}\cdot Q_g$. All data is based on the measured values in this paper.

The FOM $R_{DS(on)}\cdot A$ represents the power density capability of the devices. $R_{DS(on)}$ is the on-state resistance measured before. The area factor means the physical area of devices. For the precise assessment, the active area of an actual GaN-on-Si die decapsulated is applied to the FOM. In case of commercial devices packaged, generally there is difference between the active area and the chip area according to package solutions. Fig. 4 shows the active GaN areas of the commercial GaN-on-Si devices in this test. The rotating plate machine with a grind paper is used to decapsulate the packaged devices and the die sizes are extracted from an optical microscope. In particular, the chip sizes of the LGA package type are based on each data sheet since the LGA chip size is the same as an active area [19]. The active areas are marked with the yellow line in Fig.4. The extracted area of each device is in the Table V.

The theoretical limit lines are calculated by the interaction formula proposed on various literatures with physical parameters of each material in room-temperature 25 degree Celsius [19, 20]. Equation (3) shows the theoretical relation between $R_{DS(on)}\cdot A$ and breakdown voltage [19].

$$R_{DS(ON)} \times A = \frac{4 \cdot V_{BR}^{2}}{\varepsilon_0 \cdot \varepsilon_r \cdot E_c^{3} \cdot \mu_n} \qquad (3)$$

Fig. 5 illustrates correlation between the measured on-resistance with fully enhanced gate voltage and room-temperature condition times the active area and breakdown voltage. It explains the current position of the GaN device or technology in field of a power device. $R_{DS(ON)}\cdot A$ is exactly proportional with the square breakdown voltage and smaller value means the higher density. The maximum drain operating voltages of each GaN-on-Si discrete device are applied as the breakdown voltages on this analysis. Even though the commercial GaN-on-Si devices already had overcome silicon limitation, the points stand back far away from their theoretical limit like silicon did 30 years ago [19]. The GS-650 to use the only one enhancement GaN device has better performance than the cascade type TR-600 consisted of two chips a LV Si MOSFET and a depletion GaN device.
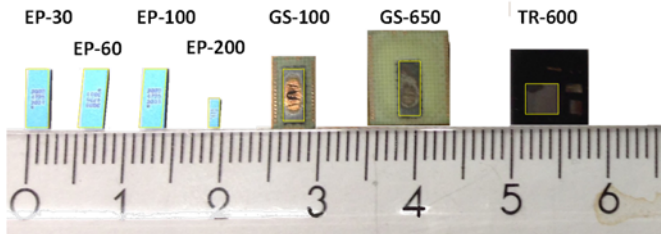
Fig. 4   Actual GaN areas of the tested commecial GaN-on-Si devices.

TABLE V.   THE EXTRACTED AREAS OF ACTIVE GaN AREA

Unit: cm²	Samples						
	EP-30	EP-60	EP-100	EP-200	GS-100	GS-650	TR-600
Area	0.139	0.139	0.139	0.019	0.112	0.123	0.104

$R_{DS(ON)}\cdot Q_g$ is introduced as the significant FOM including the switch ability of the devices. The smaller figure, the higher frequency can be achieved. Fig. 6 displays that the measured on-resistance times Q_g under fully enhanced gate voltage and room-temperature versus breakdown voltage. The fundamental tendency is similar with $R_{DS(ON)}\cdot A$ since the charge element indirectly involves the area. The most remarkable aspect here is the difference between GS-650 and the state-of-the-art silicon device. In this result, GS-650 is 14 times better than the silicon counterpart. Different performance between GaN device manufactures is indicated. $R_{DS(ON)}\cdot Q_g$ of GS-650 is 3 times smaller than cascode TR-600 and EP-100 is 3 times better than GS-100.

The superiority of the commercial GaN-on-Si discrete power devices is demonstrated with two FOMs. In comparison of theoretical limitation base on semiconductor material properties and evaluated data in this test, the current technology of the commercial GaN-on-Si discrete devices has already overcome the wall of silicon. The brighter prospect of a GaN power device is confirmed considering their theoretical barrier. In the second FOM, although there are not diverse devices in each breakdown voltage level, the obvious difference of performance between manufacturing companies in 100V and 600s V.
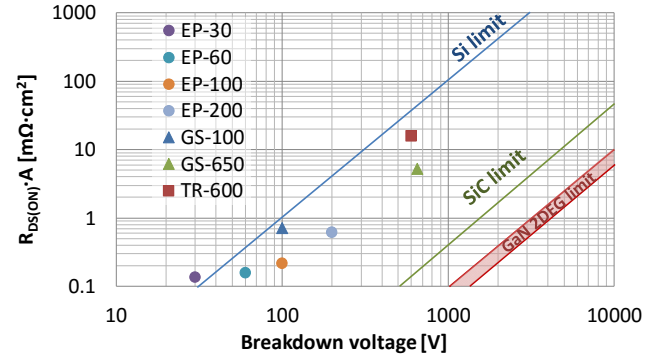
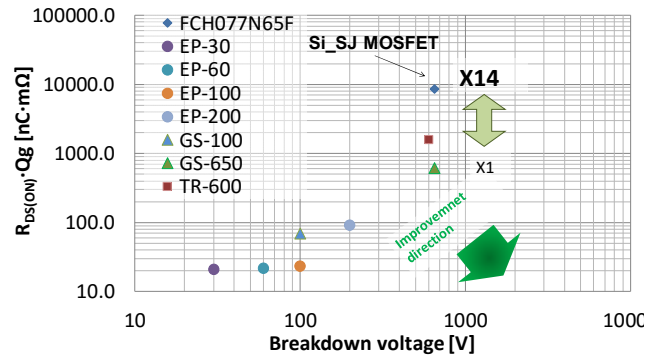Fig. 5. $R_{DS(ON)}\cdot A$ based on measured data versus breakdown voltage for commercial GaN devices.

Fig. 6. $R_{DS(ON)}\cdot Q_g$ based on measured data versus breakdown voltage for commercial GaN devices.

IV. Conclusion

The commercial GaN-on-Si power device provides the higher efficiency and less cost and weight for the power conversion system than a silicon device by increasing operating frequency. The advantages are discussed with electrical characteristics and FOMs of each device. In this work, excellent performances of the seven kinds of the novel GaN-on-Si discrete power devices on the market have been assessed with the figure of merit. For higher accuracy of figure of merit, all electrical characteristics have progressed under the same test methodology. Especially, the compensation solution for measured $R_{DS(ON)}$ is proposed as using the PCBs shorted drain to source. The active areas are extracted by decapsulating the packaged commercial devices. Electrical characteristics and FOMs are based on the measured data in this test. In the first FOM $R_{DS(on)} \cdot A$, the power density capability of the present commercial GaN-on-Si discrete power devices have already conquered the theoretical limit of a silicon device. Moreover, the great potential of them is discussed with the theoretical limit of GaN material. $R_{DS(on)} \cdot Q_g$ of the GaN-on-Si device rated 650 V is 14 times superior to the stat-of-the-art silicon device in the same criteria. Compared to the silicon counterpart, the better conducting and switching performance of the commercial GaN-on-Si devices have confirmed objectively.

Acknowledgment

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Failure Mechanism Analysis of a Discrete 650V Enhancement Mode GaN-on-Si Power Device with Reverse Conduction Accelerated Power Cycling Test

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Failure Mechanism Analysis of a Discrete 650V Enhancement Mode GaN-on-Si Power Device with Reverse Conduction Accelerated Power Cycling Test

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Abstract—A commercial discrete enhancement mode gallium nitride power component employing advanced package technology without conventional bond wire possesses the ability for bidirectional conduction. The gallium nitride power components can provide not only higher forward conductivity but also superior reverse conductivity. For the most part recent critical debates about the reverse conductivity of a GaN device have tended to center around their performance. However, the reliability of the device under reverse operation should be assessed in order for the advantages to be fully utilized in real applications. We present the results of reverse conduction power cycling test of a discrete 650-volt gallium nitride power device with novel package technology at temperature swings of 100 K. The result shows degradation of thermal conductivity and raising leakage current drain to source as reaching the number of cycles to failure. In physical failure analysis, delamination of a solder joint between a chip and a copper layer of an aluminum print circuit board is observed with a scanning acoustic microscope.

Keywords—wide band gap; gallium nitride; HEMT; reliability; power cycling test; solder delamination; leakage current

I. Introduction

An enhancement mode (e-mode) GaN power device can bidirectionally operate without other components such as a fast recovery diode (FRD). It can provide excellent reverse conduction [1]. When the e-mode GaN components are used for bidirectional mode, the reliability of reverse operation as well as forward operation should be clarified. In the coming years, a dramatic expansion of a market as the center of electrical vehicles is expected [2, 3]. They demand higher levels of reliability. Automotive standard AEC-Q101 requires for the power component to endure 15,000 cycles at temperature variation more than 100 ℃ [4, 5].

GaN power devices available on market are mainly adopting a discrete package type. Advanced discrete package technologies have been introduced considering the circumstances such as volume, output power, operating frequency, cost, and thermal management. Improvement needs of a package technology are increasing as electrical performance of GaN devices advances [6].
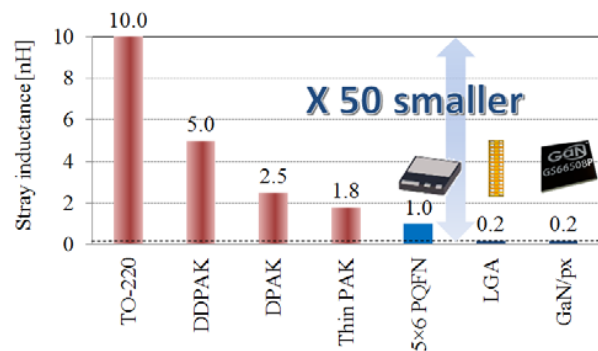

Fig. 1.   Stray inductance performance of different package technologies [1, 7, 8].
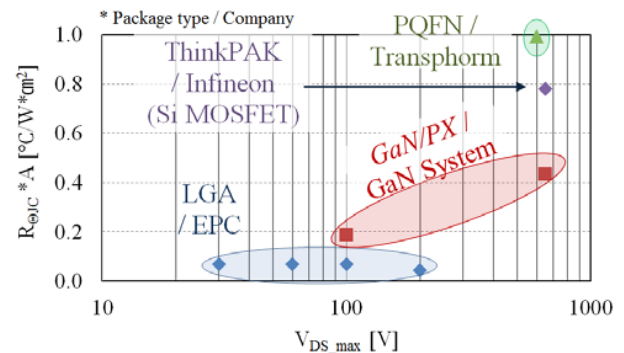

Fig. 2. $R_{\Theta JC}$ * Area of commercial discrete GaN power devices based on datasheet [9-16].

The package technologies of commercial GaN devices have exceptional performances compared to conventional packages. Basically a stray inductance and $R_{\Theta JC}$ (thermal resistance junction-to-case) * A (Package area) are very important figures which can express their own performance of each package technology. Fig. 1 and Fig. 2 show the stray inductances of different package technology [1, 7, 8] and $R_{\Theta JC}$ (thermal resistance junction-to-case) * A (Package area) of commercial discrete GaN power devices respectively [9-16]. 650 V is the

allowed maximum voltage level drain to source of current commercial GaN power devices. GaN Systems inc. provides a 650 V GaN device which is supplied in a custom package technology GaN/PX with very lower stray inductance and superior thermal conductivity. The GaN/PX uses a laminated package embedding technology using micro copper via technology instead of conventional bond wire [17, 18] for high performance operation. In spite of the performance evaluation of GaN/PX package, discussion on its reliability has been insufficient.

In this study, failure mechanism and the number of cycles to failure is debated with reverse directional conduction power cycling test using a 650 V advanced commercial e-mode GaN power device. The device under test (DUT) consists of the discrete GaN device, solder joint, an aluminum printed circuit board, and a heat sink. Failure mechanism of reverse conduction power cycling test can be described with collected data during the test and physical analysis results. The analysis can deliver an accurate method for more reliable application with discrete e-mode GaN devices.

II.   POWER CYCLING TEST SET UP

A. Reverse conduction characteristics

Discrete e-mode GaN power devices can bidirectionally work without an additional device such as a fast recovery diode (FRD). Power conversion systems request reverse conduction operation, which is to protect the switching device from reverse current flow generated by an inductor. An extra FRD is mostly co-packaged with Si IGBT's, or Si, or SiC MOSFET [19, 20]. In contrast, an e-mode GaN power device is natively capable of reverse conduction like a FRD [1, 21].

Fig. 3 exhibits the bidirectional conductivity of a GaN power device. It is based on measured data from a sample which will be power-cycling-tested. An e-mode GaN device operates like a reverse diode with at $V_{GS} = 0$ V. It means that e-mode GaN power devices do not need FRD anymore for the reverse conduction. Moreover, if the device is activated by $V_{GS} = 6$ V, reverse conductivity can achieve the same conductivity with forward conductivity [1]. It should be a strong advantage in the specific application such as motor drive [22]. Therefore, to exploit this promising feature it is necessary to establish the reliability of the GaN device package under reverse conduction. To this end we apply a power cycling test.
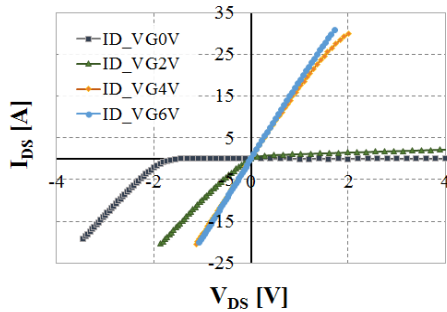

Fig. 3.   Measured drain-to-source voltage Vs. drain-to-source current of a 650 V discrete GaN power device @ T = 25 ℃.
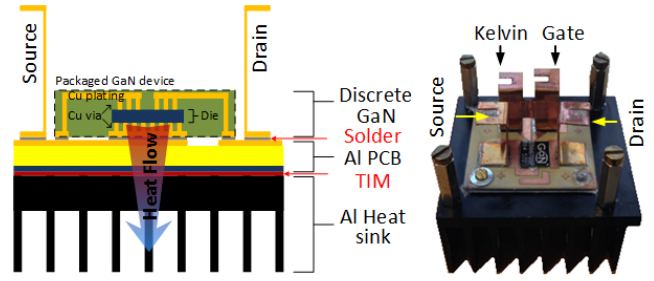

Fig. 4.   Layer section view of DUT and a picture of DUT.

B. Device under test

The device under test for the power cycling consists of GaN System Inc.'s discrete GaN device mounted on a thermal management structure. In general, discrete type power devices are not electrically isolated [2]. An aluminum (Al) PCB can provide electrical isolation as well as excellent thermal conductivity. The discrete GaN device is attached on the Al PCB by soldering using a Sn-Ag-Cu lead-free solder alloy (SAC305). A cross section of the DUT module and an actual image are shown in fig. 4 [1, 18].

To ensure a high quality of the solder layer, the solder paste was applied using stencil printing and the assembly was soldered in a vacuum vapour phase reflow system. A vacuum solder process can give void-free and high quality solder layer. The Al PCB with a discrete GaN component is mounted on an Al heat sink with thermal greases as the thermal interface material.

Although three samples used for this test are build up based on the above process, more advanced pre-cleaning process before daubing solder paste on PCB is applied to the only 3rd sample. The first two samples are wiped with Isopropyl alcohol (IPA) for the pre-cleaning, while a pre-cleaning recipe of the last sample is improved into twice acetone and once IPA cleaning processes with an ultrasonic cleaner. It is observed that the pre-cleaning process does directly affect the lifetime of DUT during the power cycling test through this experiment.

C. Power cycling test principle and Set up

In the power cycling test, the thermal energy generated by the power losses of the DUT is utilized to generate the thermal stress. Fig. 5 shows the strategy of this power cycling test.
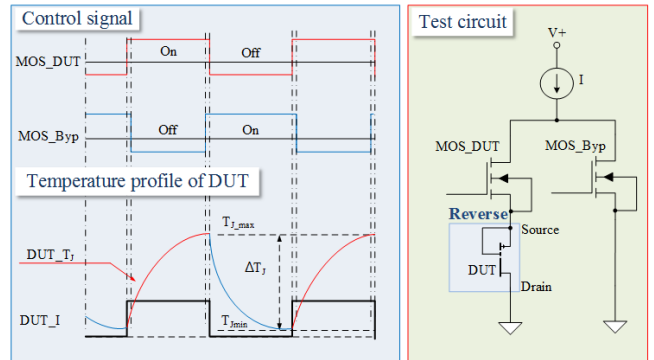

Fig. 5.   Control signals of MOSFET, Temperature profile of DUT, and test principle for reverse mode power cycling test.
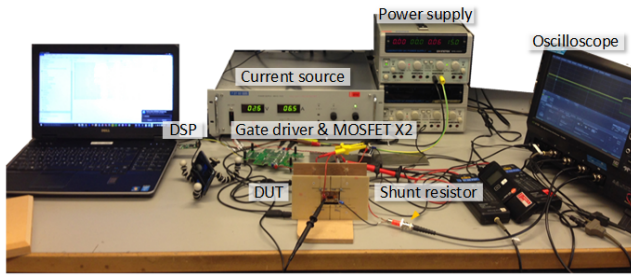
Fig. 6.   Power cycling test setup.

As an operation principle it was chosen to control the load current of the DUT with two MOSFETs. When a MOS_DUT is in the on-state the current is injected into the DUT. When the MOS_DUT is turned-off the current is commutated to the MOS_Byp. Gate-to-source voltage of DUT is zero voltage because Gate node is tied up source node. It reflects reverse conduction operation in device non-activation state.

Fig. 6 illustrates power cycling test set up. The control signals are generated from a digital signal processing (DSP) unit. The gate signals are level-shifted to range from + 15 V to – 10 V to be able to control two power MOSFETs. The MOSFETs are also mounted on heat sinks. A power supply is used as the main current source. The source-to-drain voltage and current of the DUT are monitored and saved at periodic intervals with an oscilloscope. A shunt resistor is connected to the DUT in series to monitor the precise current of the DUT. The current is calculated using voltage drop across the resistor.

To measure the temperature with an infrared (IR) camera the DUT is vertically fixed on table. In general, the measured temperature with IR camera might differ from the true junction temperature, but based on [1] it was shown the measured temperature was very close to the junction temperature from simulation result. The consensus between measured temperature of IR camera and a deadly accurate heating plate was confirmed from 25℃ to 100 ℃.

There are a few more strategies ΔT_J, ΔT_C, power loss, and on / off time = constant in power cycling test. In this test, the strategies on / off time = constant is chosen because of the best way to reflect real applications [23]. The stress conditions to meet the target temperature swing ΔT_J=100 were established via initial testing to be t_{on} = 1 s, t_{off} = 2 s, and I = 6.5 A. Fig. 7 shows measured temperature profile in the test set up.
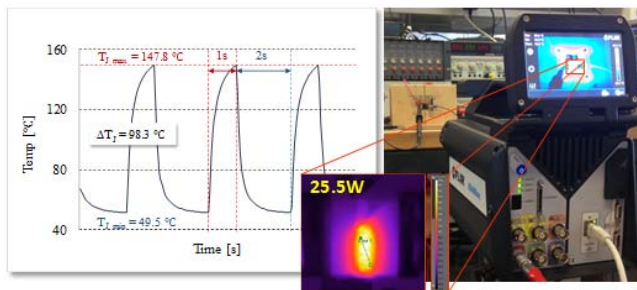

Fig. 7.   Measured temperature profile of DUT and the environment of junction temperature measurement.

The set failure criteria of the power cycling test are displayed in TABLE. I. The criteria were chosen according to the IEC 60747-9-2007 standard [24]. V_{th}, I_{DSS}, and R_{DS} are electrically characterized with a curve trace machine without the connection of power cycling test set up. ΔT_J and R_{SD_MX} are measured in real time under power cycling test. The maximum values of R_{SD} within one cycle are recorded because it was observed that these values grow proportionally to the measured temperature.

TABLE I.   IDENTIFICATION OF FAULT LEG AND FAULTY GROUP

Parameter	Description	Power cycling	Machine	Limit
V_{th}	Threshold voltage	Off-line	Curve trace	± 20%
I_{DSS}	Off leakage current			+ 100%
$R_{DS(on)}$	On resistance			+ 20%
T_{j_MX}	Maximum junction temp.	On-line	Infrared camera & Oscilloscope	+ 20%
R_{SD_MX}	Maximum on-state resistance under PC			+ 20%

III.   RESULT AND FAILURE MECHANISM OF REVERSE CONDUCTION POWER CYCLING TEST

Fig. 8 illustrates measured ΔT_J, ΔR_{SD_MX} and electrical characteristics of three DUT Rev.#1, Rev.#2, and Rev.#3 during reverse conduction power cycling test. For the first two sample Rev.#1 and Rev.#2 I = 6.5 A and t_{on} / t_{off} = 1 / 2 s conditions are applied to the two DUT equally. The same current condition is used because the temperature cannot be measured in Rev.#2. For Rev.#3 the stress condition I = 5.6 A satisfying ΔT_j = 100 ℃ is adopted at the beginning of test.

In the result of Rev.#1, the first graph shows monitored ΔT_J and ΔR_{SD_MX} during power cycling test. They are gradually increasing after 120 kcycles, and then ΔT_j has gone out of initial values + 20 % after 160 kcycles. It is observed that R_{DS_MX} rises proportionally in measured curve as T_{j_MAX} increases. In contrast, there is no change of on resistance R_{DS} measured with a curve tracer at room temperature. It is indicted that only thermal resistance of DUT varies without degradation of electrical interconnection as the number of cycles proceeds.

Rev.#2 shows similar results to Rev.#1. Taking off of R_{SD_MX} is indicated after 78 kcycles during power cycling test without change of R_{DS}. It has earlier failure cycles than Rev.#1. The temperature is not measured in Rev.#2. Despite this, we can expect the higher initial T_{j_MAX} of Rev.#2 then T_{j_MAX} = 147.8℃ Rev.#1 due to higher initial power losses of Rev.#2. The harsher initial thermal stress of Rev.#2 is expected compared to Rev.#1.

Rev.#3 has the longest lifetime. As mentioned in section II-B, the advanced pre-cleaning condition before spreading solder paste is adopted to this sample. Decrease of thermal conductivity starts from 226 kcycles. Failure mode is out of IDSS (leakage current). It is the same with failure mode of Rev.#2. Except for this, V_{th} and R_{DS} are within the normal range in failure criteria. The results of reverse conduction power cycling test are summarized in TABLE II.
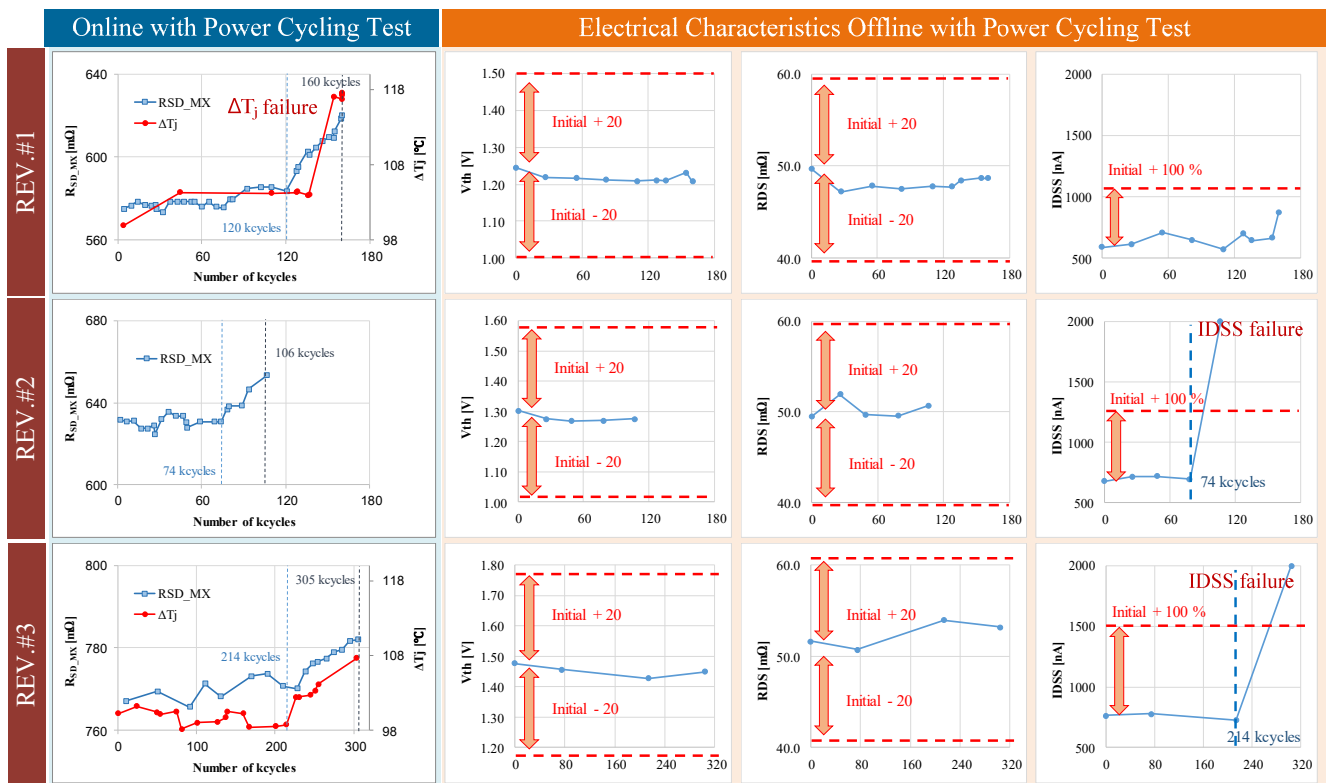
Fig. 8. Measured ΔT_j and ΔR_{SD_MX} during power cycling test & Electrical characteristics versus the number of cycles.

TABLE II. POWER CYCLING TEST RESULTS OF SAMPLES

Sample	Power loss @Initial	Number of cycles to failure	Failure judgement
Rev. #1	25.5 W	160k	$\Delta T > 20\%$ of initial value
Rev. #2	27.1 W	74k ~ 106k	IDSS > +100% of initial value
Rev. #3	23.5W	214k ~ 305k	IDSS > +100% of initial value

IV. DISCUSSION

As the number of cycles increases, degradation of thermal conductivity of all DUTs is confirmed during power cycling test. Although online-measured reverse resistance and junction temperature increase, there is no significant change in the offline-measured on-resistance (R_{DS}) and threshold voltage with curve-tracer at room temperature within failure criteria. For Rev.#1, the end-of-life is reached after 160 kcycles when junction temperature approaches 178°C. In this case, degeneration of thermal conductivity is a direct cause of failure. In results of other two samples, the wearing out thermal conductivity appears after 74 kcycles and 214 kcycles respectively. Although the thermal path consists of diverse layers from a GaN-on-Si semiconductor die to an Al heat sink, the failure is primarily attributed to solder fatigue [25]. The solder joint fatigue between the discrete GaN device and the test fixture can be inspected in a KSI V_8 scanning acoustic microscope (SAM) from IP Holding. Fig.9 shows the SAM

analysis of the three DUTs before and after power cycling test. In the previous IR camera image, heating area in power cycling test overlaps with thermal pad. The SAM image before the power cycling test shows normal quality of solder layer without any void as mentioned in section II.B. Rev.#1 had been not scanned before the power cycling test. On the other hand, solder joint delamination in the thermal pad area is indicated in images after the power cycling test. Normal solder shapes in electrical interconnections; drain, source, gate, and Kelvin, are shown in after SAM image.
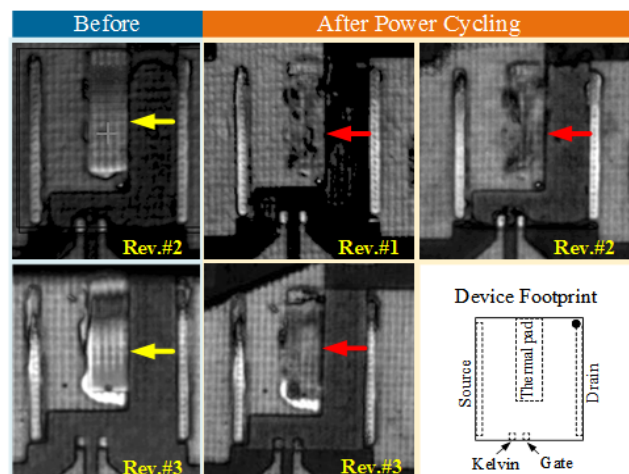

Fig. 9. SAM images before and after power cycling test and a device footprint.

The pre-cleaning process before daubing solder paste is intimately linked with lifetime of a DUT. Rev.#3 with the enhanced pre-cleaning recipe has at least 54 kcycles longer lifetime compared to Rev.#1. Cleaner surface can provide better contact quality when soldering. The quality of this solder joint can be represented with a similar experiment. In [26], the number of cycles to failure of Sn-Ag solder compound in the IGBT module is 25 kcycles under the test condition, $t_{on} = 2$ s, $\Delta T_{j\_max} = 125$ °C, and $\Delta T_j = 100$ °C. Thus, it can be described that 214 kcycles of Rev.#3 is reasonable.

Failures of Rev.#2 and Rev.#3 are perceived with IDSS measurement. Increasing IDSS of Rev.#1 is detected at the failure as well. IDSS is to measure current drain to source with turn-off status. The thermal pad must be electrically connected with a source pad based on [27] because this GaN device substrate is isolated from gate, source, and drain electrodes in the package. When the device is reverse biased source potential of silicon substrate can release concentration of electrical field from drain. If the thermal pad is electrically disconnected from source by the delamination of solder layer, IDSS failure scenario by change of electric field distribution from drain can be expected. To be perfectly explained, however, additional data from further experiment and analysis should be need.

V. CONCLUSION AND FUTURE WORK

A power cycling test environment of reverse conduction mode for a discrete 650 V GaN power device has been introduced. Three samples have been tested with power cycling condition at $\Delta T_J = 100$ °C and t_{on} / $t_{off} = 1$ s / 2 s. Failure progresses are observed with monitoring junction temperature and diverse electrical characteristics. In the result, it is observed that thermal conductivity is gradually degraded at the failure and leakage current drain to source (IDSS) increases as the number of cycles is getting close to each failure. In result of physical failure analysis, it is confirmed that the solder fatigue between the discrete device and the test fixture leads to a decline of thermal conductivity. The delamination of solder layer due to high temperature swings is indicated with SAM analysis. The exact mechanism of IDSS current increase should be verified with further collected data from extra testes and analysis.

The suggested reverse conduction mode power cycling test in this paper can be applied to forward conduction operation on the same concept. Therefore, future research should be directed at determining failure mechanism of forward conduction mode power cycling and comparing that to reverse conduction mode.

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Power Cycling Test of a 650 V Discrete GaN-on-Si Power Device with a Laminated Packaging Embedding Technology

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Abstract— **A GaN-on-Si power device is a strong candidate to replace power components based on silicon in high-end market for low-voltage applications, thanks to its electrical characteristics. To maximize opportunities of the GaN device in field applications, a package technology plays an important role in a discrete GaN power device. A few specialized package technologies having very lower stray inductance and higher thermal conductivity have been proposed for discrete GaN-on-Si power devices. Despite their superior performance, there has been little discussion of their reliability. The paper presents a power cycling test of a discrete GaN power device employing a laminated embedded packaging technology subjected to 125 degrees Celsius junction temperature swing. Failure modes are described with collected electrical characteristics and measured temperature data under the test. In conclusion, physical degradation of a solder layer between a tested discrete chip and an aluminum print circuit board is represented by a scanning acoustic microscope and a scanning electron microscope. A drain-to-source leakage current increase after the failure is reported in resemblance with previous studies.**

Keywords—Gallium nitride; GaN-on-Si; power cycling; reliability; failure mechanism; laminated packaging embedding technology; solder delamination

I. INTRODUCTION

Gallium nitride (GaN) power devices offer promising performance of power electronic systems with enhanced switching efficiency [1]. For maximizing this advantage, sufficient electrical and thermal characteristics of the package technology are required for commercial GaN power devices. For most applications, a low stray inductance and a small thermal resistance of the package are desired. Diverse package approaches are applied to commercial grade GaN-on-Si power products. In terms of performance, GaN Systems's GaN/PX package technology shows a very low 0.2 nH parasitic inductance [2, 3] and a higher thermal transfer capability [3, 4] compared to other packages and thus this is the device studied here.
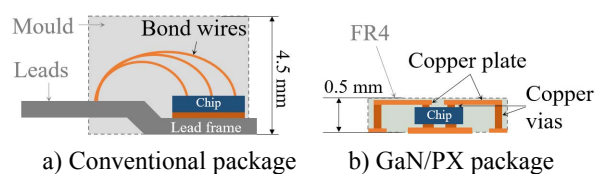

Fig. 1 Cross section of a) conventional package technology with a bond wire [7] b) a laminated packaging embedding technology (GaN/PX) [2].

The GaN/PX technology is based on a laminated package embedding technology [4, 5]. Their low parasitic inductance is due to short electrical interconnections. Micro copper vias are used for interconnects instead of a conventional bond wire process [4, 6]. Fig. 1 displays geometrical differences between a package with bond wire [7] and a laminated embedding package [2]. The laminated package is 10 times thinner than the bond wire type. The laminated embedding package technology normally possesses not only good electrical performance but also better reliability due to a homogeneous mechanical environment of the semiconductor dies [2, 4, 5]. The performance of the GaN/PX technology is often emphasized, but the reliability has not been sufficiently investigated. To this end power cycling (PC) is a valuable tool for studying the reliability characteristics of the GaN/PX technology [8, 9]. A PC test of a power GaN device can be carried out both directions: forward and reverse conductions. In a previous study [8], the reverse conduction PC test was studied with the same type devices. Experiments in this paper are extended to include the forward conduction PC test.

In this study, a PC test which facilitates observation of the change of junction temperature and on-resistance of the tested device in real time is conducted. The device under test (DUT) is composed of a commercial discrete GaN power device and a structure able to dissipate heat from the GaN-on-Si die. The number of cycles to failure of DUT has been established by the monitored junction temperature and the electrical data. Based on

the collected data of DUT during the PC test and physical analysis results, failure modes induced by PC test with high-temperature swing (125 ℃) is described.

II. POWER CYCLING TEST SET UP

A. Device under test

The DUT structure was designed to provide not only electrical connection to the main PC test set-up but also thermal dissipation for the tested discrete GaN device. It consists of four copper leads, a discrete GaN device, an Al PCB [10], and an Al heatsink. The discrete GaN device and the four leads are connected to the top side copper of the Al PCB by soldering with SnAgCu lead-free solder alloy (SAC305). Al PCB can offer electrical isolation as well as higher thermal conductivity 3 W/m-K [10] than a FR-4 based PCB. It is composed of a thin thermally conductive dielectric layer in middle, thin copper layer for electrical circuit bonded to the top side, and thick aluminum bonded to bottom side. Al PCB is usually used for power applications which demand thermal management because of easy of a manufacturing process, good thermal conductivity, and low cost. It is not the best solution in terms of thermal mechanical stress because of higher coefficient of thermal expansion (CTE) of Al PCB. Compared to Al PCB [10], a direct bonded copper (DBC) substrate has very low CTE, which can ensure the more durable reliability of a PC test. However, DBCs are comparatively expensive and for many application purposes the Al PCB is a good representation. An Al PCB is chosen for this test considering the numerous factors. A thin thermal interface material (TIM) is inserted between the Al PCB and the heatsink to enhance the thermal coupling. Assembly processes such as soldering and cleaning are described in detail in [8]. Fig. 2 displays various components that compose the DUT in an actual image.

B. Power cycling test

In a PC test, the thermal source induced by power losses in a power component is used for thermal bias to DUT. It ultimately generates mechanical stress caused by a mismatch of coefficients of thermal expansions (CTE) of each material in the DUT. The thermo-mechanical stress caused by repeated heating and cooling during PC test leads to degradation of the DUT.
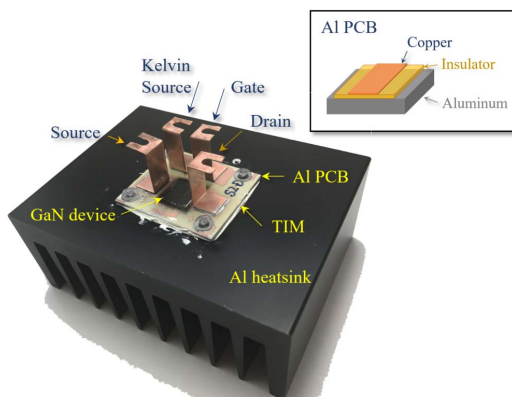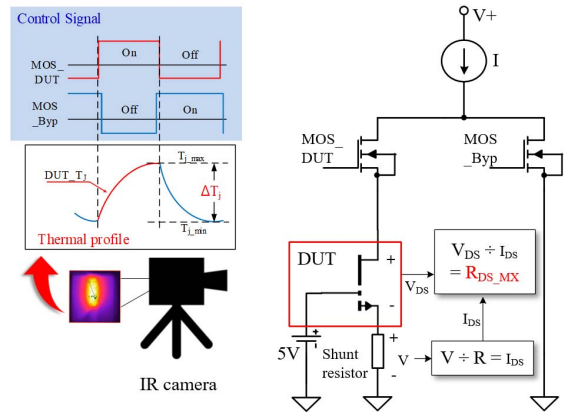

Fig. 2 A picture of DUT and composition of Al PCB.

Fig. 3 Control signal of MOSFET, ΔT_j and R_{DS_MX} measured in an online PC test, and principle of a PC test

Fig. 3 describes the principle of the PC test and how ΔT_j and R_{DS_MX} are monitored during the PC test. DUT is kept in on-status during the test with + 5 V gate-to-source. The injected current into the DUT is controlled by switching operation of two MOSFETs. When the MOS_DUT is turned-on the current is injected into the DUT. When the MOS_DUT is turned-off the current detours to the MOS_Byp. In this PC test, on/off time of the MOS_DUT is set to 1 / 2 second (s). The operation strategy of the PC test here is on/off time = constant since this resembles real application [11]. Constant loading current is generated by a power supply. At the start of the PC test, the main current is set to 17.2 amperes (A) satisfying T_{j_max} = 150 ℃ for 1 s. 150 ℃ is the maximum junction temperature (T_{j_max}) limited by the manufacture [3]. During the cooling time 2 s, the junction temperature drops to around 25 ℃ the room temperature. The heatsink is fan-cooled differently to the last test [8] (ΔT_j = 100 ℃) without fan. As a result, a high-temperature swing (ΔT_j = 125 ℃) is attained by the above set up.

During the PC test, two parameters (ΔT_j and R_{DS_MX}) are monitored from DUT in real time. Fig.3 shows how they are measured. The junction temperature of DUT is estimated with an infrared (IR) camera. In general, there might be differences between the measured temperature and the true junction temperature. From a comparison between simulation result and IR camera measured temperature in [2] tested with the GaN/PX packaged device, it was shown that the measured temperature was very near to the junction from the simulation. The results
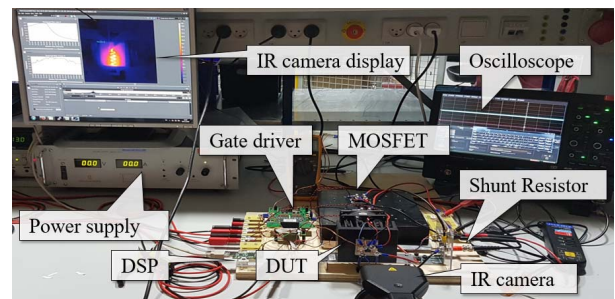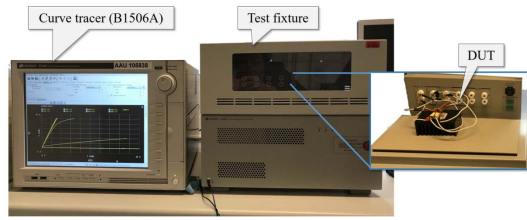

Fig.4 Power cycling test set-up.

Fig. 5 An offline test environment for DUT.

of T_j were evaluated under constant temperature condition from 25 ℃ to 120 ℃, which is slightly differ from the conditions here, but the IR measured temperature still serves as a very useful indicator for the maximum ΔT_j during each swing. R_{DS_MX} is the maximum value of the drain-to-source resistance of the DUT calculated by the flowing current and the drain-to-source voltage measured during PC test. The current is extracted by a voltage drop across the shunt resistor connected in series to the source of the DUT and resistance value. Fig. 4 exhibits the PC test environment. The control signals for switching the two MOSFETS are produced by a digital signal processing (DSP) unit.

In an offline test done in between PCs, three parameters (V_{th}, R_{DS_ON}, and IDSS) are measured in a curve tracer at room temperature. The measurement is conducted daily or half-daily. V_{th}, R_{DS_ON}, and IDSS represent the threshold voltage, on-state resistance, and off-state leakage current of the DUT respectively. Fig.5 displays the offline test environment for DUT.

The above five criteria-parameters are monitored during the PC test, which indicates abnormality of a tested DUT. Failure criteria, which decide that the DUT reaches to failure, are:

- V_{th} is out of the initial value $+ / - 20\%$
- ΔT_j, R_{DS_MX}, and R_{DS_ON} exceed the initial value $+ 20 \%$
- IDSS exceeds the initial value $+ 100 \%$.

It is based on the IEC60747-9-2007 standard [12]. The detail conditions to measure the five parameters are described in [8].

III. RESULT OF POWER CYCLING TEST

Fig.6 illustrates the five parameters monitored during each PC test of three samples; FWD.#1, FWD.#2, and FWD.#3. The first row of Fig.6 shows simultaneously ΔT_j and R_{DS_MX} measured in the online PC test. Their trends, as the number of cycles progresses, is similar in all the three samples. ΔT_j and R_{DS_MX} of them remain almost constant up to a large number of cycles, and then are gradually increasing after 15 or 30 kcycles. Their failures occur between 22 and 59 kcycles with exceeding R_{DS_MX} + 20 %. Generally, on-state resistance changes corresponding to the temperature rise [3]. Therefore, it is natural that R_{DS_MX} increases as ΔT_j rise. The trend can be discussed with R_{DS_ON} measured at the room temperature in detail in the next section.

The last three rows in Fig. 6 display V_{th}, R_{DS_ON}, and IDSS electrically characterized in an offline test at the room temperature. Their notable change implies abnormality of a discrete GaN device in DUT. At the failure of all three samples, there is no change of V_{th}, R_{DS_ON}, and IDSS. In contrast, it is confirmed that R_{DS_MX} exceeds their initial values + 20 % at the failure. This is in line with previous observation done for reverse conduction and the increase in R_{DS_MX} is ascribed to an increase in thermal impedance since no changes are observed in R_{DS_ON} measured in the curve tracer.
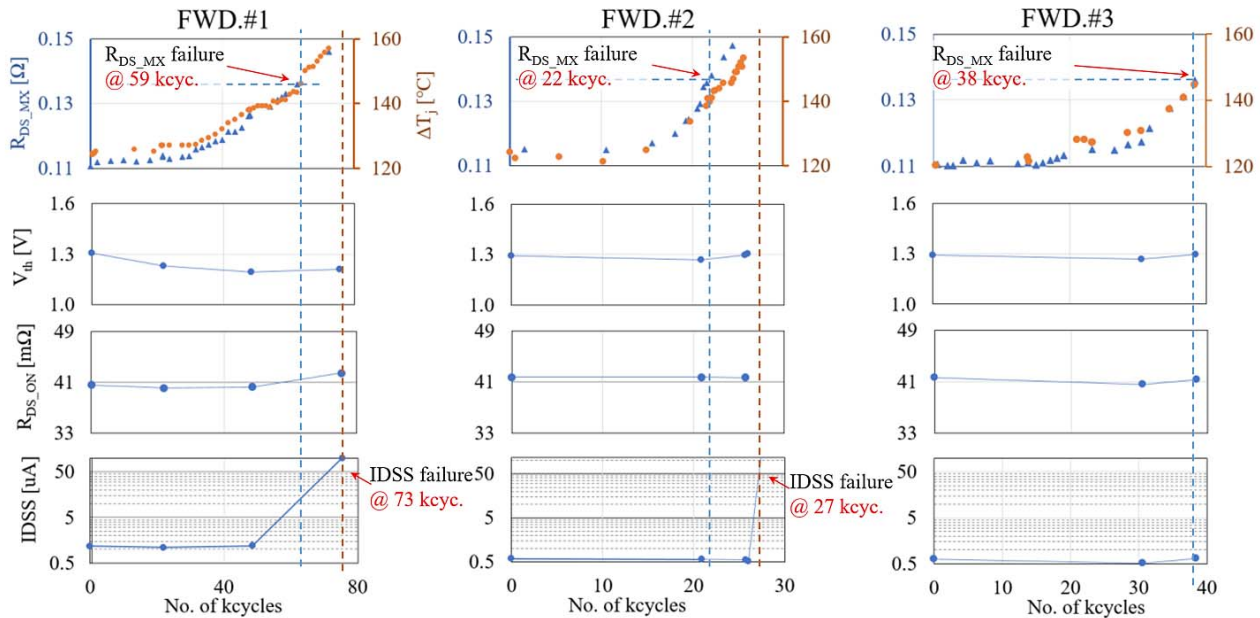

Fig. 6 The results of Mearsured ΔT_j and R_{DS_MX} in online PC test & V_{th}, R_{DS_ON}, and IDSS in offline test.

a) A Scanning point in a cross-section view of device & Foot print and IR image

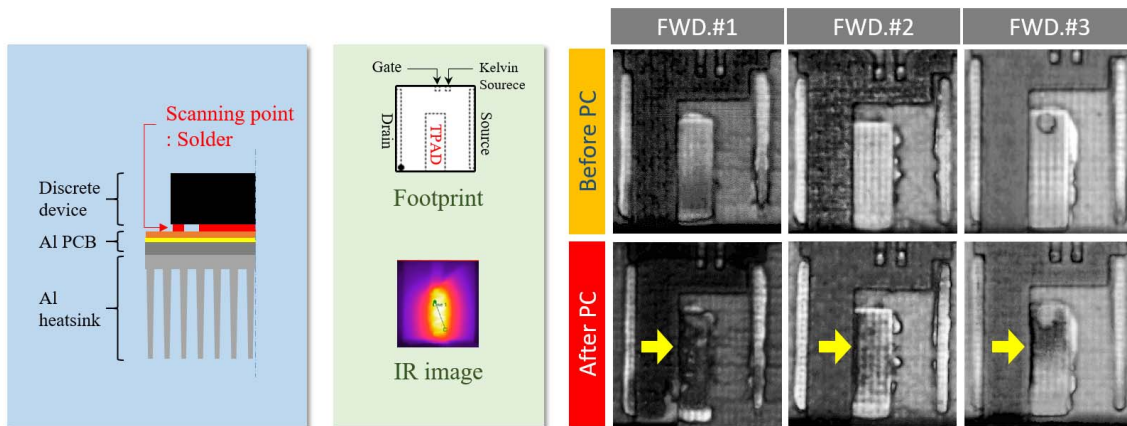b) SAM images before and after PC test of FWD.#1, #2, and #3

Fig. 7 a) A scanning point in a cross-section view of DUT, b) SAM images before and after PC test of FWD.#1, #2, and #3.

The off-state leakage current (IDSS) failure is observed in FWD.#1 and FWD.#2 after failure. In contrast, their V_{th} and R_{DS_ON} are maintained within normal limits at the IDSS failure. At the IDSS failure, ΔT_j and T_{j_max} have increased to 160 ℃ and 185 ℃ respectively. This thermal stress is very aggressive because a manufacture allows operating temperature of the GaN device up to 150 ℃ [3]. It will be discussed with the previous study in section V.

IV. FAILURE ANALYSIS

It was expected that the degradation of thermal conductivity of the DUT tested is induced by thermo-mechanical stress during PC test with high-temperature swing. Even though a heat release path is composed of various layers from a junction to an Al heat sink, the failure of thermal stress is primarily attributed to solder fatigue [8, 13]. The solder joint of the DUT is placed in between the Al PCB and copper pads of the packaged discrete GaN device. The CTE of copper, Al PCB and SAC305 are 17 [14], 25 [10] and 21.6 [15] ppm / ℃ respectively. The CTE mismatch leads to a severe mechanical stress of solder joint under thermal cycling.

The physical abnormality of the solder layer after cycling is investigated in a KSI V_8 scanning acoustic microscope (SAM) from IP Holding. Fig.7 b) exhibits images of the three tested samples taken by the SAM before and after the PC test. Normally, SAM analysis is done by soaking a sample in liquid. However, to avoid artifacts of water in the device characteristics the SAM picture before PC is taken with a customized dry box.

The heating generated by power consumption is focused on the thermal pad (TPAD) area, but not the whole area of the package. Fig.7 a) shows that the heating part in the IR camera image overlaps with TPAD. A normal quality of solder layer without any void is confirmed in SAM images before a PC test FWD.#1 and FWD.#2. FWD.#3 had a small void in solder layer under TPAD before a PC test. It may negatively affect thermal conductivity of a DUT. However, no significant degradation of the thermal conductivity of FWD.#3 was observed in this test.
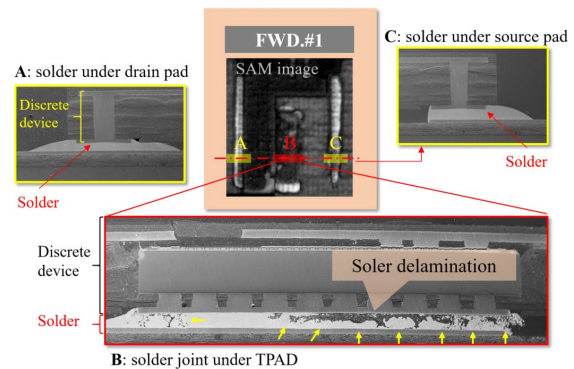

Fig.8 SEM cross-section analysis of FWD.#1 after 73 kcycles.

The abnormality of the solder layer after failure is proved with a comparison between images before and after PC test in Fig.7.

Degradation of solder layer under TPAD area is shown after PC tests. In contrast, there are no signs of abnormality in the solder layer under the four electrical connections. The solder delamination occurs only in the TPAD area where thermos-mechanical stress is concentrated. The results are similar to the previous research [8] for reverse conduction. The state of the damaged solder layer can be inspected locally in more detail with cross-sectional SEM analysis.

Fig. 8 exhibits cross-sectional SEM images of FWD.#1 after 73 kcycles. The sample is prepared with epoxy molding and polishing processes. Severe degradation is observed in a solder layer underneath TPAD. It is not continuous across TPAD in the cross section. They are marked with yellow arrows in Fig.8. The structural degradation directly affects degradation of thermal conductivity during a PC test. On the other hand, it is indicated that there is no abnormality in the solder layers not subjected to thermal-mechanical stress under the source and drain pads. These analysis results accurately correspond to the previous SAM results.

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V. Discussion

As observed above PC capability and failure mechanism due to PC test at ΔT_j = 125 ℃ were investigated with the GaN device employing the laminated packaging embedded technology (GaN/PX). Although the numbers of kcycles to failure are distributed from 22 to 59 kcycles, their failure causes concluded in one failure mechanism. It is confirmed that the solder layer delamination leads to degradation of the thermal conductivity with measured electrical parameters and physical analysis with SAM and SEM of FWD.#1. The quality of the solder joint can be compared with investigation results of solder degradation generated by PC reported in [16]. The number of cycles to failure of Sn-Ag solder compound in the IGBT module is 25 kcycles under the test conditions; t_{on} = 2 s, T_{j_max} = 125 ℃, and ΔT_j = 100 ℃. Thus, allowing for the harsher thermal stress condition of the PC test here; T_{j_max} = 150 ℃, and ΔT_j = 125 ℃, it can be estimated that the numbers of kcycles to failure from the 22 to 59 kcycles of the three samples tested here are reasonable. Although they were manufactured in the same condition, it is indicated that there is a difference in the quality of solder layer among them. The quality of a solder layer in DUT is influenced by the solder layer itself as well as surface conditions in contact with the solder layer; a surface of the copper pad in a discrete device and top copper in an Al PCB. In FWD.#3, it is confirmed that there is a void in solder layer under TPAD which may either be a few artifacts. To ensure a similar quality of solder layer between DUTs, it is important to maintain a strict process control in further tests.

At the failure, it is observed that the discrete GaN devices maintain normal condition with electrical characteristics in the offline test and at the room temperature. It means the GaN device can stand longer PC than 59 kcycles in this test here. This does not, however, represent general reliability since this requires additional statistics analysis with more samples to establish their reliability. Robustness of the GaN device also can be discussed with results of a similar PC test. There was a previous study on a PC test with commercial power module using bond wire technology [11]. The test conditions of this previous test; T_{j_max} = 150 ℃, ΔT_j = 125 ℃, on/off time = constant, and on/off time = 2 / 2 s, are similar with this PC test here. The number of cycles to the failure of the sample was 25 kcycles applying here failure criteria, and the main failure mechanism was the bond wire failure. For exact comparison of the robustness between GaN/PX and the conventional package technology, the geometric information such as area, thickness, and CTE of each layer should be considered. It is expected that GaN/PX can sustain more than 59 kcycles under the above-tested conditions (ΔT_j = 125 ℃). It is revealed that the solder layer fatigue leads to degradation of DUT in these tests. As applying more reliable solutions such as Ag sinter having better thermal conductivity and higher melting point [17], higher reliability of a power system using the GaN power device may be achieved.

Compared to the previous study on the reverse conduction PC test [8] with the test conditions; T_{j_max} = 150 ℃, ΔT_j = 100 ℃, on / off time = constant, and on / off time = 1 / 2 s, the number of kcycles to the failure of the samples tested here are shorter due to the increase in ΔT_j from 100 ℃ to 125 ℃. Nevertheless,

the same failure mechanism based on a solder delamination and IDSS increase phenomenon induced by PC test are indicated in both studies. This demonstrates that although the conditions vary, the nature of failure mechanism is similar, for reverse as well as forward conductions modes. The temperature swing conditions of the two tests were ΔT_j = 100 ℃ and 125 ℃ respectively. In Ref. [9, 18] it was reported that failure mechanism may differ depending on a magnitude of the temperature swinging. Thus, a PC test with smaller temperature swing would be interesting to investigate further. The dramatic IDSS increase is observed without any abnormality of V_{th} and R_{DS_ON}. The degradation of electrical connection (copper vias) in the package may affect R_{DS_ON} increase or V_{th} shift. Thus, the root of this IDSS failure is likely in the GaN die. Further studies on the correlation between PC test and the IDSS failure are needed.

VI. Conclusion

Failure modes of a discrete GaN power device employing a laminated packaging embedding technology have been investigated under a PC test with high-temperature swing (ΔT_j = 125 ℃). It is shown with measured data and physical analysis, SAM and SEM, that the common cause of failure in three DUTs is a solder delamination due to repeated thermal-mechanical stresses during the PC test. Compared to a reverse conduction PC test, it is confirmed that there is no significant difference in the failure mode of PC tests between reverse and forward conduction. IDSS increase phenomenon after failure is observed in both the experiments present and previous results. The correlation between IDSS failure and a PC test should be addressed in further tests.

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