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On the Practical Design of a Two-terminal Active Capacitor

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***Abstract*—A two-terminal active capacitor concept is proposed recently based on an active power electronic circuit with a voltage control method and self-power scheme. It retains the convenience of use as a passive capacitor with two power terminals only without any additional required connections, and has the potential to either increased power density or reduced design cost depending on the applications. Based on the previously proof-of-concept study, this paper addresses the design constraints, impedance modeling, and start-up solutions of two-terminal active capacitors. A design method for functionality, efficiency, lifetime and cost constraints application is applied to size the active components and passive elements. A voltage feed-forward control scheme is implemented to improve its dynamic response. Two start-up solutions are proposed to overcome the issues brought by the self-power scheme. A case study of an active capacitor for the DC link of a single-phase full-bridge rectifier is presented to demonstrate the theoretical analyses.**

***Index Terms*—Capacitors, Power converter, Active circuits, Reliability**

I. Introduction

The applications of power electronics consume unprecedented quantities of capacitors for harmonic filtering, power balancing, and/or short-term energy storage. In a single-phase voltage-source rectifier or inverter system, the capacitive DC link needs to filter low-frequency current components while limiting the voltage variation within a specific range. In a three-phase system, possible unbalances appearing in line voltages and/or loads introduce low-frequency harmonics in the DC link [1]. Therefore, a bulky capacitor bank is required for the capacitive DC links in most single-phase and three-phase applications. Moreover, large capacitor banks are also necessary for the AC filters in MW-level high-power inverter applications [2]. Electrolytic capacitors, film capacitors, and ceramic capacitors have been applied for one or more of those applications by considering their respective electrical characteristics, cost, volumetric efficiency, and reliability performance. Capacitor technology advancements have introduced to the market high-performance products, such as high-density, long-lifetime, low Equivalent Series Resistance (ESR), or high-temperature series. However, capacitors are still one of the highest failure components in power electronic systems, and the design constraints in cost and/or power density compromised with electrical and reliability performance still impose a great challenge even with the state-of-the-art capacitor technologies [3].

Power electronics researchers have explored an alternative path to overcome the challenge by introducing capacitor banks with auxiliary active circuits [4–11], especially for capacitive DC-link applications. The benchmarking of different methods for a single-phase application is presented in [12] in terms of overall component cost in order to fulfill a specific lifetime target. The study identifies that the most cost-effective solutions are based on series-connected auxiliary circuits [8–11]. By applying the auxiliary circuit topology in [8], a voltage control method, and a self-power supply scheme, a two-terminal active capacitor concept has been recently proposed in [11]. Two-terminal active capacitors retain the same convenience of use as passive capacitors with two power terminals only, without any additional required connections of control signals and power supplies. Therefore, the active capacitors could be rated by voltage, ripple current, equivalent capacitance, ESR, Equivalent Series Inductance (ESL) and operational temperature range. Power electronic converters implemented with the active capacitors could achieve either increased power density or reduced design cost for a given reliability specification, as discussed in [11].

Several practical design issues need to be addressed to carry on the two-terminal active capacitor concept proposed in [11]. Firstly, the design constraints, including the functionality, efficiency, cost and reliability aspect considerations, are still open questions. Secondly, the dynamic response of the active capacitors and its associated impedance characteristics with

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respect to that of passive capacitors need to be demonstrated. Thirdly, special attentions are needed for the start-up of the active capacitors due to its self-power schemes and relatively low component ratings. Inspirations from other applications dealing with the above three aspects of issues provide a basis for this research. The design constraints of the active capacitive DC links for a high power density single-phase inverter application is well discussed in [10], which could be applicable for the two-terminal active capacitor design as well. Therefore, the focus of the following discussions is on cost-constraint applications, which is relevant to most industry sectors. The practical challenge for this type of applications is to design the active capacitors to fulfill the functionality, efficiency and lifetime target with minimum cost. Such component sizing procedure is presented in [13] based on the reliability-oriented design method [14] [15] and power electronic component cost models discussed in [16–18]. For dynamic response and impedance characteristic analyses, the large-signal modeling and small-signal modeling are widely applied tools [19]. Voltage feed-forward control is one of the solutions to improve dynamic response and voltage stabilization [20, 21], which is also worthwhile to being explored for the two-terminal active capacitors. Different start-up circuits [22–24] or start-up algorithms [25] [26] are applied in practical designs to limit the inrush current of power electronic converters. Nevertheless, these start-up methods cannot be directly applied for the two-terminal active capacitors due to 1) the active capacitors do not have an internal power source for its gate drivers and controllers during the start-up and 2) its components have relatively low voltage ratings with limited over-voltage capability.

This paper aims to propose associated methods to overcome the above three aspects of practical design challenges of the two-terminal active capacitors for cost-constraint applications. Besides the analysis of design constraints, the study on dynamic response and impedance characteristics modeling, and start-up solutions is also applicable for high power density applications. Even though partial of the results to be discussed in this paper have already been presented in previous conference publications [27] [28], it is worthwhile to having a more comprehensive discussions on all the three important aspects by one case study. Moreover, new results are added including 1) Theoretical analysis and mathematical model for the impedance characteristics of the active capacitor are presented in this paper; 2) Investigation of start-up issue and corresponding solutions, including component sizing and start-up circuit. The structure of this paper is as follows: Section II briefly introduces the two-terminal active capacitor concept; Section III discusses the design constraints and component sizing procedure of the active capacitors in terms of electrical performance, cost, and reliability; Section IV presents the impedance characteristic modeling of the active capacitors with and without feed-forward control scheme; Section V gives the start-up procedure analysis and proposes two start-up solutions for the active capacitors; Section VI demonstrates a case study of a two-terminal active capacitors for a single-phase capacitive DC link application, with experimental verifications on the steady-state performance, dynamic response, and start-up procedure.

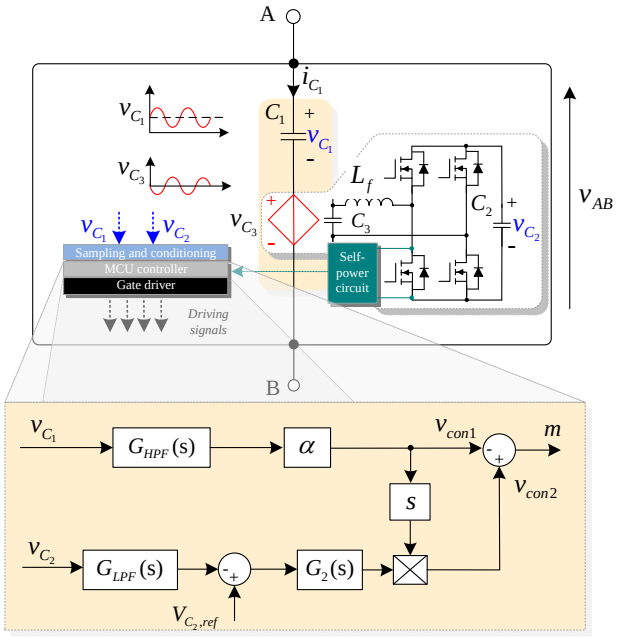

Fig. 1. The system diagram of the active capacitor concept presented in [11].

II. Two-terminal Active Capacitor Concept

Fig. 1 shows the system diagram of a two-terminal active capacitor. A full-bridge converter is connected in series with a capacitor C_1. It handles only the ripple voltage and ripple current of C_1, implying a low *VA* rating. Thus, it is possible to achieve a cost-effective capacitive DC-link solution, as to be discussed in section III. Moreover, because of the low rating auxiliary circuit characteristic, specified start-up considerations are needed to guarantee that the electrical stresses of the auxiliary circuit are under rating.

The control objective of the active capacitor is to shape the impedance seen from AB terminals to be that of an equivalent passive capacitor of interest based on internal signals. Therefore, from the control aspect, it enables fully independent operation of the active capacitor without any feedback signals from external circuits. The control method shown in Fig. 1 is to modulate the voltage v_{C_3} to be out of phase with the ripple components in v_{C_1} and same amplitude. $G_{\mathrm{HPF}}(s)$, $G_{\mathrm{LPF}}(s)$ and $G_2(s)$ are the transfer function of the high pass filter (HPF), low pass filter (LPF) and the PI controller, respectively. $V_{C_2,\mathrm{ref}}$ is the voltage reference of C_2 and α is the scaling factor of the ripple component of v_{C_1}, respectively. In order to compare the terminal characteristics with the passive capacitor, the impedance characteristics of the active capacitors are derived in Section IV.

III. Component Sizing of the Active Capacitor for Cost-constraint Applications

The component sizing of the active capacitor is presented in this section by considering the operating principle, lifetime, and cost. The analytical equations derived in Section III to Section V are generic ones and the presented numerical

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TABLE I
SPECIFICATION OF THE SINGLE-PHASE SYSTEM WITH AN ACTIVE CAPACITOR.

Parameters	Description	Value
P	Power rating	750 W
R_{Load}	Load resistance	53 Ω
v_{AC}	Grid voltage RMS	110 V
f_{a}	Fundamental frequency	60 Hz
n	Order of harmonic considered	2
V_{AB}	Average terminal voltage v_{AB}	200 V
L_{g}	Inductance of grid side inductor	0.75 mH
α_{v}	DC-link voltage ripple ratio	5 %
f_{sw}	Switching frequency	20 kHz
$V_{\mathrm{C_2,ref}}$	Voltage reference of $v_{\mathrm{C_2}}$	60 V
C_1	Capacitance of C_1	110 μF/ 250 V
C_2	Capacitance of C_2	470 μF/ 100 V
C_3	Capacitance of C_3	3 μF/ 63 V
L_{f}	Inductance of L_{f}	100 μH/ 3 A
R_1	ESR of the passive capacitor	405 $m\Omega$
R_2	ESR of C_1	4 $m\Omega$

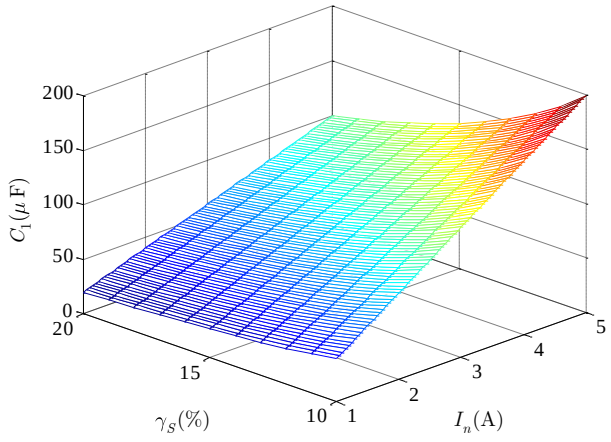

Fig. 2. The relation between C_1, I_{n} and ratio of apparent power (for the case study shown in Table I).

results in figures are based on a specific design case with specifications shown in Table I.

A. Basic Criteria for Component Sizing

1) Criteria to Size C_1: C_1 impacts the apparent power handled by the auxiliary circuit and the efficiency.

- Constraint I- Apparent power limit of the auxiliary circuit
  In steady-state operation, the current flowing through the active capacitor $i_{\mathrm{C_1}}(t)$ is given by

$$i_{\mathrm{C_1}}(t) = \sum I_{\mathrm{n}} \cos(n\omega t + \delta_{\mathrm{n}}) \tag{1}$$

  where ω is the fundamental frequency and n is the order of harmonics. For simplicity, only n th-order harmonic is considered in following analysis. Superposition principle can be applied if two or more harmonic components are considered. I_{n} is the amplitude of the ripple current, and δ_{n} is the phase shift of the ripple current. The steady-state voltage of C_1 is

$$v_{\mathrm{C_1}}(t) = V_{\mathrm{AB}} + \frac{1}{2}\Delta V_{\mathrm{C_1}} \sin(n\omega t + \delta_{\mathrm{n}}) \tag{2}$$

  where $\Delta V_{\mathrm{C_1}} = \frac{2I_{\mathrm{n}}}{n\omega C_1}$ is the peak to peak voltage of C_1 and V_{AB} is the average voltage across the terminal A and B. The control target of $v_{\mathrm{C_3}}(t)$ is the inverse voltage of ripple component in $v_{\mathrm{C_1}}(t)$, therefore

$$v_{\mathrm{C_3}}(t) = -\frac{1}{2}\Delta V_{\mathrm{C_1}} \sin(n\omega t + \delta_{\mathrm{n}}) = -\frac{I_{\mathrm{n}}}{n\omega C_1} \sin(n\omega t + \delta_{\mathrm{n}}) \tag{3}$$

  From (3), it can be seen that C_1 is inversely proportional to the amplitude of $v_{\mathrm{C_3}}(t)$ which determines the voltage stress of the auxiliary circuit. The RMS (Root Mean Square) voltage and current of the auxiliary circuit are $\frac{\Delta V_{\mathrm{C_1}}}{2\sqrt{2}}$ and $\frac{\mathrm{I_n}}{\sqrt{2}}$, while the processed apparent power ratio of the auxiliary circuit S_{aux} to the main system S_{main} can be derived as

$$\frac{S_{\mathrm{aux}}}{S_{\mathrm{main}}} = \frac{\frac{\Delta V_{\mathrm{C_1}}}{2\sqrt{2}} \times \frac{\mathrm{I_n}}{\sqrt{2}}}{S_{\mathrm{main}}} = \frac{\Delta V_{\mathrm{C_1}} I_{\mathrm{n}}}{4S_{\mathrm{main}}} \tag{4}$$

  For the specified single-phase design system with specification shown in Table I, the terminal RMS voltage and current of the active capacitor are V_{AB} and I_{n}, and the while the processed apparent power ratio is

$$\gamma_{\mathrm{S}} = \frac{S_{\mathrm{aux}}}{S_{\mathrm{main}}} = \frac{\Delta V_{\mathrm{C_1}}}{4V_{\mathrm{AB}}} \tag{5}$$

  γ_{S} it implies the apparent power the auxiliary circuit in the active capacitor processed, which affects both the efficiency and cost of the active capacitor. Taking $\Delta V_{\mathrm{C_1}} = \frac{2I_{\mathrm{n}}}{n\omega C_1}$ into above equation, the value of C_1 should satisfy

$$C_1 \geq \frac{I_{\mathrm{n}}}{2n\omega\gamma_{\mathrm{S}} V_{\mathrm{AB}}} \tag{6}$$

  The relation between C_1, the ratio of apparent power and the ripple current is shown in Fig. 2.
- Constraint II: System efficiency limit

  Efficiency is one of the design constraints for active capacitor, which depends on the implementation. As shown in Fig. 3, if it is assumed that the efficiency of the main circuit (with conventional passive DC-link capacitor) and auxiliary circuit of the active capacitor can be designed as η_1 and η_2, respectively, and the ESR of the conventional DC-link capacitor and the capacitor C_1 in the active capacitor are R_1 and R_2, respectively, the total power loss of the system can be

$$\begin{aligned} P_{\mathrm{loss-total}} &= S_{\mathrm{main}}(1-\eta_1) - \frac{I_{\mathrm{n}}^2 R_1}{2} + S_{\mathrm{aux}}(1-\eta_2) + \frac{I_{\mathrm{n}}^2 R_2}{2} \\ &= S_{\mathrm{main}}(1-\eta_1) + \frac{\Delta V_{\mathrm{C_1}}}{4V_{\mathrm{AB}}} S_{\mathrm{main}}(1-\eta_2) - \frac{I_{\mathrm{n}}^2(R_1-R_2)}{2} \end{aligned} \tag{7}$$

  Thus, the efficiency of the system with active capacitor is

$$\eta' = 1 - \frac{P_{\mathrm{loss-total}}}{S_{\mathrm{main}}} = \eta_1 - \frac{\Delta V_{\mathrm{C_1}}}{4V_{\mathrm{AB}}}(1-\eta_2) + \frac{I_{\mathrm{n}}(R_1-R_2)}{2V_{\mathrm{AB}}} \tag{8}$$

  The efficiency drop introduced by the active capacitor can be described by $\Delta\eta$ which is the difference between the efficiency of the system with conventional DC-link

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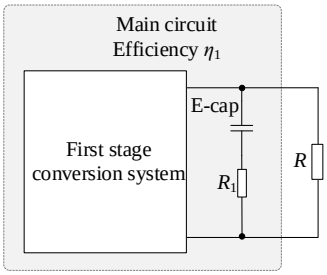
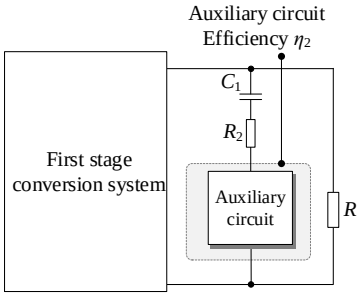


(a) System with DC-link E-cap .



(b) System with DC-link active capacitor.

Fig. 3. Diagram of the system with DC-link E-cap and DC-link active capacitor.

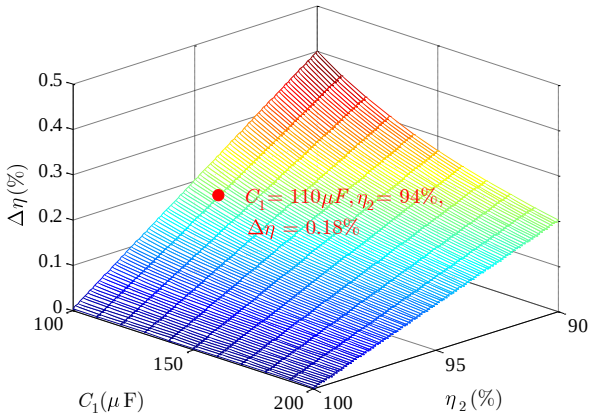


Fig. 4. The relation between efficiency drop $\Delta\eta$ and other design parameters.

E-cap η_1 and the efficiency of the system with an active capacitor η'.

$$\Delta\eta = \eta_1 - \eta' = \frac{\Delta V_{\mathrm{C}_1}}{4V_{\mathrm{AB}}}(1-\eta_2) - \frac{I_{\mathrm{n}}(R_1-R_2)}{2V_{\mathrm{AB}}} = \frac{I_{\mathrm{n}}}{2V_{\mathrm{AB}}}\left(\frac{1-\eta_2}{2n\omega C_1} - R_1 + R_2\right) \tag{9}$$

With a maximum allowable efficiency drop $\Delta\eta_{\max}$ is defined, the value of C_1 should satisfy

$$C_1 \geq \frac{I_{\mathrm{n}} - I_{\mathrm{n}}\eta_2}{4n\omega V_{\mathrm{AB}}\Delta\eta_{\max} - 2nR_2I_{\mathrm{n}}\omega + 2nR_1I_{\mathrm{n}}\omega} \tag{10}$$

The relationship between C_1, η_2 and $\Delta\eta$ is shown in Fig. 4, where $R_1 = 405$ mΩ and $R_2 = 10$ mΩ are measured by the impedance analyzer Agilent E4980A. If η_2 is 94 %, the efficiency drop is 0.18 %. The capacitance of C_1 also affects the efficiency drop of the system. With larger C_1, the efficiency drop is smaller because of power handled by the auxiliary circuit is reduced.

2) Criteria to Size C_2: C_2 is the DC-link capacitor of the auxiliary circuit in the active capacitor. The capacitance of C_2 has impact on the operation of the auxiliary circuit. Two constraints are need to be considered to size C_2:

- Constraint I: Voltage controllability
  Based on the control scheme shown in Fig. 1, the relation between $v_{\mathrm{C}_3}(t)$ and $v_{\mathrm{C}_2}(t)$ is expressed as

$$v_{\mathrm{C}_3}(t) = m(t)v_{\mathrm{C}_2}(t) \tag{11}$$

  where $m(t)$ is the modulation signal, it depends on two control signals: 1) $v_{\mathrm{con1}}(t)$- the extracted ripple component of $v_{\mathrm{C}_1}(t)$ used to control the converter to generate the desired $v_{\mathrm{C}_3}(t)$; 2) $v_{\mathrm{con2}}(t)$ is used to stabilize $v_{\mathrm{C}_2}(t)$. Moreover, the phase of v_{con2} and i_{C_1} is synchronized (i.e., a 90° phase shift with v_{con1}), in order to absorb active power from external circuits through terminals A and B shown in Fig. 1 to compensate the power loss of the auxiliary circuit. Therefore,

$$m(t) = \frac{v_{\mathrm{con1}}(t) + v_{\mathrm{con2}}(t)}{V_{\mathrm{tric}}} \tag{12}$$

  where $v_{\mathrm{con1}}(t) = -\frac{1}{2}\alpha\Delta V_{\mathrm{C}_1}\sin(n\omega t + \delta_{\mathrm{n}})$. V_{tric} is the amplitude of the triangular carrier wave. The current of C_2 can be obtained from

$$i_{\mathrm{C}_2}(t) = m(t)[i_{\mathrm{C}_1}(t) - i_{\mathrm{C}_3}(t)] \tag{13}$$

  By ignoring the power loss of the auxiliary circuit, based on (3), (11), and (12), the voltage ripple across C_2 is derived as

$$v_{\mathrm{C}_2,\mathrm{ripple}}(t) = \frac{1}{C_2}\int i_{\mathrm{C}_2}(t)dt = \frac{\alpha(C_1+C_3)I_{\mathrm{n}}^2[1+\cos(2n\omega+2\delta_{\mathrm{n}})]}{4n^2\omega^2C_1^2C_2V_{\mathrm{tric}}} \tag{14}$$

  The peak to peak voltage is

$$\Delta V_{\mathrm{C}_2} = \frac{\alpha(C_1+C_3)I_{\mathrm{n}}^2}{2n^2\omega^2C_1^2C_2V_{\mathrm{tric}}} \tag{15}$$

  With the modulation index no more than 1, in order to control the auxiliary circuit,

$$v_{\mathrm{C}_2}(t) \geq v_{\mathrm{C}_3}(t) \tag{16}$$

  For the sake of simplification, the minimum value of $v_{\mathrm{C}_2}(t)$ is considered becomes

$$V_{\mathrm{C}_2} - \frac{1}{2}\Delta V_{\mathrm{C}_2} \geq v_{\mathrm{C}_3}(t) \tag{17}$$

  Therefore, the value of C_2 should satisfy

$$C_2 \geq \frac{\alpha I_{\mathrm{n}}^2(C_1+C_3)}{4n\omega C_1V_{\mathrm{tric}}(n\omega C_1V_{\mathrm{C}_2} - I_{\mathrm{n}})} \tag{18}$$

- Constraint II- Voltage ripple limitation of v_{AB}
  The sizing of C_2 should also consider the voltage ripple limitation of v_{AB} defined in Fig. 1. Voltage variations of C_2 introduce ripple to v_{C_3} and therefore the voltage

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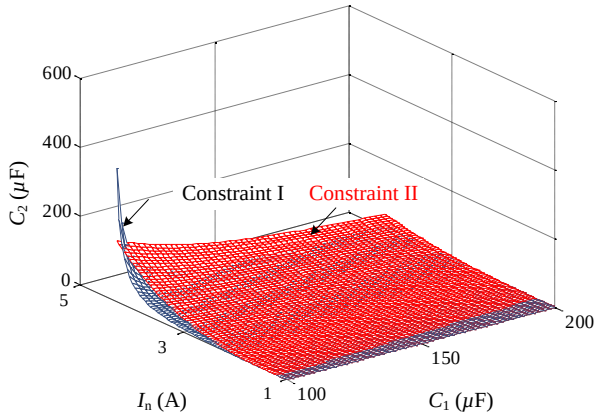

Fig. 5. Component sizing constraints of C_2.

across the terminals A and B. The relationship is described as

$$v_{C_3}(t) = m(t)v_{C_2}(t) = \frac{v_{con1}(t)}{V_{tric}}V_{C_2} + \frac{v_{con2}(t)}{V_{tric}}V_{C_2} + \frac{v_{con1}(t) + v_{con2}(t)}{V_{tric}}v_{C_2,ripple}(t) \quad (19)$$

The first part of (19) is the expected component of $v_{C_3}(t)$, the second part is used for compensating the power loss, and the third part is additional voltage ripples introduced by $v_{con2}(t)$ and $v_{C_2,ripple}(t)$. By ignoring the power loss effect of the auxiliary circuit, the third part of voltage ripple appears also at the two terminals A and B, which should be limited to its voltage specification of v_{AB} as

$$v_{C_3,ripple}(t) = v_{C_2,ripple}(t)\frac{v_{con1}(t)}{V_{tric}} \quad (20)$$
$$= \frac{\alpha^2 \Delta I_n^3 (C_1 + C_3)\cos^2(n\omega t + \delta)\sin(n\omega t + \delta)}{4n^3\omega^3 C_1^3 C_2 V_{tric}^2} \le \alpha_v V_{AB}$$

where α_v is the voltage ripple ratio defined in the system specification. Thus, C_2 should satisfy

$$C_2 \ge \max\left\{\frac{\alpha^2 I_n^3 (C_1 + C_3)\cos^2(n\omega t + \delta)\sin(n\omega t + \delta)}{4n^3\omega^3 C_1^3 V_{tric}^2 \alpha_v V_{AB}}\right\} = \frac{\alpha^2 I_n^3 (C_1 + C_3)}{6\sqrt{3}n^3\omega^3 C_1^3 V_{tric}^2 \alpha_v V_{AB}} \quad (21)$$

Fig. 5 shows the two constraint surfaces to size C_2. The minimum value of C_2 also depends on C_1 and I_n.

B. Component Sizing for the Active Capacitor for Multiple Constraints

For different applications, the design criteria of active capacitor are different from case to case. The design criteria covers the aspects of functionality, efficiency, lifetime, and cost. The weighted importance of each of them would depend on applications. In order to achieve the systems' requirement, a design procedure for active capacitor with multiple design constraints are presented, as shown in Fig. 6. In the present study, the design scenario is to minimize the design cost with specific requirements on the functionality (e.g., capacitor terminal voltage ripple limit, controllability), efficiency, and lifetime.

The input of the design procedure are the mission profile and the design constraints for specified application. Mission profile includes the operating conditions of the active capacitor, such as the ambient temperature and the loading conditions. The design constraints cover aspects of functionality, efficiency, lifetime, and cost. For different mission profile and design constraint, the component sizing results are different. The first step of the design procedure is the component sizing for functionality, due to it is the first priority. C_1, C_2, filters and switches with corresponding rated electrical stress can be obtained according to the sizing criteria discussed in section A. By searching the available devices in the market, the devices which can fulfill the required parameters can be selected. The second step is to evaluate the performance of these components in terms of power loss, cost and lifetime. For the capacitors, the ripple current and ambient temperature are the contributors to the internal thermal stress. Especially, the increase of the capacitor power loss causes a higher hot-spot temperature. Lifetime prediction for the capacitor is based on the hot-spot temperature and the voltage stress. For the power semiconductor, the power losses consists of conduction loss the switching loss, which will induce thermal stresses. Then the lifetime of the power semiconductors can be obtained by using the lifetime model [29]. For the sake of simplicity, the wear out failure of the switches within the targeted lifetime period is assumed much lower than that of the capacitors if its maximum junction temperature is below 100 degree [13]. Since it is assumed that the magnetic components usually has less degradation compared to active switches and capacitors, the lifetime aspect analysis of magnetic components is not considered in this paper. The sizing of the inductor is based on achieving the same ripple current ratio. After the summation of component performance, if there is anyone aspect can not reach the design target, another series components with different parameters will be selected to evaluate the performance.

By changing the parameters of the circuit and the components within the basic criteria discussed in Section III. A, an active capacitor which can achieve multiple design constraints can be selected. Details regarding to the lifetime estimation procedure and cost models can be found in [13].

IV. Impedance Characteristics of the Active Capacitor

A. Modeling of the Active Capacitor

In order to simplify the analysis, the power converter is assumed to be lossless and the ESRs of the passive components are neglected. The large signal model of the active capacitor is shown in (22) by ignoring the high frequency LC filter for switching harmonics.

$$\begin{cases} C_2\frac{dv_{C_2}(t)}{dt} = C_1\frac{dv_{C_1}(t)}{dt}m(t) \\ v_{C_2}(t)m(t) = v_{C_3}(t) \end{cases} \quad (22)$$

By using the averaged ac modeling technique in [30] and neglecting the second-order AC quantities and processing only

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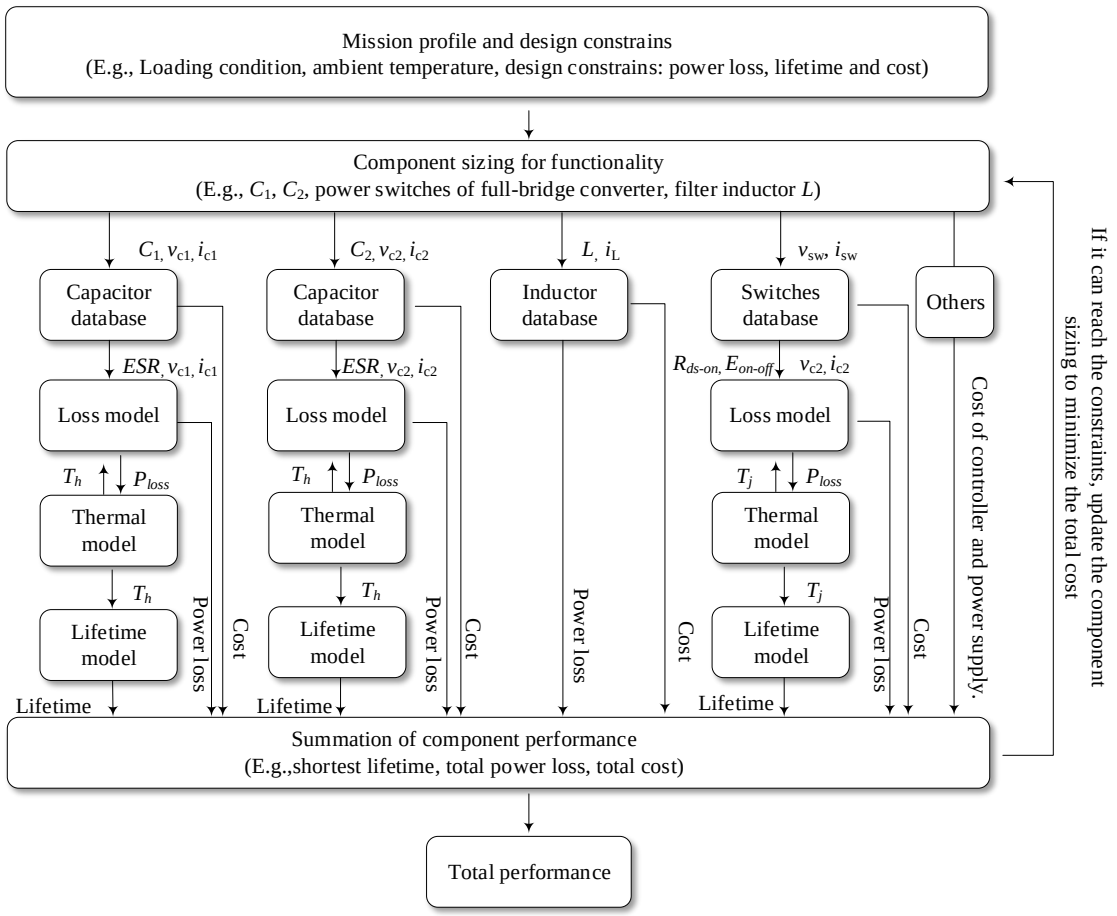

Fig. 6. Flowchart of component sizing procedure considering the reliability and the cost of the active capacitor.

with the AC equations, the RMS (Root Mean Square) based small signal modeling of the system can be seen as below.

$$\begin{cases} C_2\tilde{v}_{\mathrm{C}_2}(s)s = C_1\tilde{v}_{\mathrm{C}_1}(s)Ms \\ \tilde{v}_{\mathrm{C}_2}(s)M + \tilde{m}(s)V_{\mathrm{C}_2} - \tilde{v}_{\mathrm{C}_3}(s) = 0 \end{cases} \tag{23}$$

where $\tilde{v}_{\mathrm{C}_1}(s)$, $\tilde{v}_{\mathrm{C}_2}(s)$, $\tilde{v}_{\mathrm{C}_3}(s)$, and $\tilde{m}(s)$ are the AC perturbations. M is the modulation index. Based on the control structure presented in Fig. 1, it can be seen that the modulation signal contains two parts: 1) v_{con1} is the extracted ripple component of v_{C_1} used to modulate the converter to generate the desired v_{C_3}. $\tilde{v}_{\mathrm{C}_1}$ signal flows through the high pass filter (HPF) to extract the ripple component. The ripple is scaled by alpha and reverses as the reference of $\tilde{v}_{\mathrm{C}_3}$. 2) v_{con2} is used to stabilize v_{C_2}. $\tilde{v}_{\mathrm{C}_2}$ signal flows through the low pass filter (LPF) to extract the DC component. Controller $G_2(s)$ is used to stabilize the voltage of C_2.

$$\tilde{m}(s) = \frac{-\alpha G_{\mathrm{HPF}}(s)\tilde{v}_{\mathrm{C}_1}(s) + G_2(s)G_{\mathrm{LPF}}(s)\tilde{v}_{\mathrm{C}_2}(s)}{V_{\mathrm{tric}}} \tag{24}$$

The transfer function from $\tilde{v}_{\mathrm{C}_1}(s)$ to $\tilde{v}_{\mathrm{C}_3}(s)$ can be derived as,

$$\begin{aligned} G_{\mathrm{r}}(s) = \frac{\tilde{v}_{\mathrm{C}_3}(s)}{\tilde{v}_{\mathrm{C}_1}(s)} &= \frac{MC_1V_{\mathrm{C}_2}G_2(s)G_{\mathrm{LPF}}(s) + M^2C_1V_{\mathrm{tric}}}{C_2V_{\mathrm{tric}}} \\ &\quad - \frac{\alpha C_2V_{\mathrm{C}_2}G_{\mathrm{HPF}}(s)}{C_2V_{\mathrm{tric}}} \end{aligned} \tag{25}$$

The impedance of the active capacitor is obtained as below and is plotted in Fig. 7.

$$\begin{aligned} Z_{\mathrm{ACap}}(s) = \frac{\tilde{v}_{\mathrm{C}_3}(s) + \tilde{v}_{\mathrm{C}_1}(s)}{\tilde{i}_{\mathrm{C}_1}(s)} &= \frac{1 + G_{\mathrm{r}}(s)}{C_1 s} \\ = \frac{MC_1V_{\mathrm{C}_2}G_2(s)G_{\mathrm{LPF}}(s) + M^2C_1V_{\mathrm{tric}}}{C_1C_2V_{\mathrm{tric}}s} &\\ - \frac{\alpha C_2V_{\mathrm{C}_2}G_{\mathrm{HPF}}(s) + C_2V_{\mathrm{tric}}}{C_1C_2V_{\mathrm{tric}}s} & \end{aligned} \tag{26}$$

From Fig. 7, it can be seen that the impedance curves of the active capacitor with different high pass filters are different, depending on the bandwidth of the high pass filters. At a certain low-frequency bandwidth, the impedance characteristics is same with C_1. In the middle-frequency bandwidth, the high pass filter starts to work. The active capacitor has an equivalent negative resistance component at this certain frequency range, which is due to the impact of the introduced high pass filter $G_{\mathrm{HPF}}(s)$ shown in Fig. 1. It implies that the auxiliary circuit release power and the capacitor C_2 is discharged if low-frequency disturbances appear (e.g., below 100 Hz when the cut off frequency of $G_{\mathrm{HPF}}(s)$ is 10 Hz. At the frequency higher than middle bandwidth, such as $\geq$ 100 Hz, the high pass filter operates to extract all the harmonics, while the active capacitor has the same characteristics with

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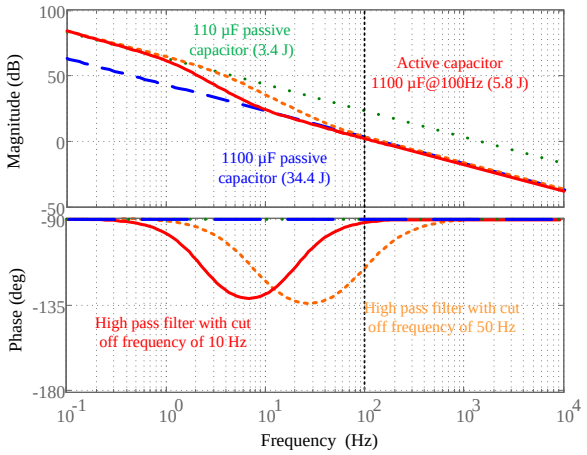


Fig. 7. Impedance comparison between the passive capacitor and active capacitor ignoring the LC filter. The green dot line is the impedance curve of a 110 μF passive capacitor with 3.4 J total energy storage; blue dash line is the impedance curve of a 1100 μF passive capacitor wtih 34.3 J total energy storage and red solid line is the impedance curve of the active capacitor with 5.8 J total energy storage. The red and orange curves are the impedance curve of the active capacitor with 10 Hz and 50 Hz high pass filters.

the 1100 μF passive capacitor. With a proper selection of the cut off frequency (e.g., 10 Hz), the phase angle is the same as an ideal capacitor when the frequency is 100 Hz or above if ignore the power loss, which are the frequency range of interest for the DC-link current during stead-state operation. The impedance differences between low frequency and high frequency bandwidth results in over voltage during the load change condition, because the capacitor charging current contains both DC and AC components during load changing. The large signal modeling of the active capacitor regarding to the DC and AC disturbances are shown in Fig. 8. Fig. 8 (a) shows the simplified model of the active capacitor with only ripple compensation loop v_{con1}. R_{Load} is the load of the system.

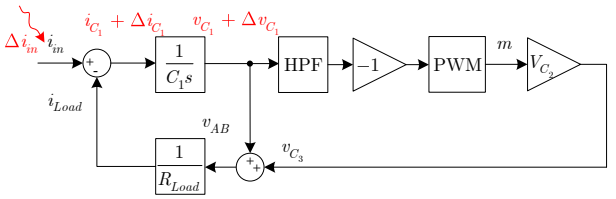
1) AC disturbance

Fig. 8 (b) shows the AC disturbance $\Delta i_{\mathrm{C_1,AC}}$ perturbs at the input of the active capacitor and transfers to $\Delta v_{\mathrm{C_1,AC}}$. Because $\Delta v_{\mathrm{C_1,AC}}$ is an AC signal, it can flow through the HPF to extract the ripple component as the reference signal of $v_{\mathrm{C_3}}$. Thus, the disturbance can propagate all the blocks in the equivalent model with red line. Because of differential compensation between $\Delta v_{\mathrm{C_1,AC}}$ and $\Delta v_{\mathrm{C_3,AC}}$, there is no disturbance at the AB terminal voltage v_{AB}.

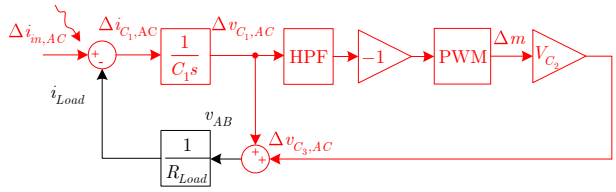
2) DC disturbance

In Fig. 8 (c), the DC disturbance $\Delta i_{\mathrm{C_1,DC}}$ perturbs at the input and introduce DC voltage on $\Delta v_{\mathrm{C_1,DC}}$. Different from the AC disturbance, the DC disturbance $\Delta v_{\mathrm{C_1,DC}}$ can not be filtered by the HPF, therefore the $\Delta v_{\mathrm{C_3,DC}}$ can not compensate the voltage overshoot or voltage droop of $\Delta v_{\mathrm{C_1,DC}}$. The $\Delta v_{\mathrm{C_1,DC}}$ disturbance has impact on v_{AB} directly.

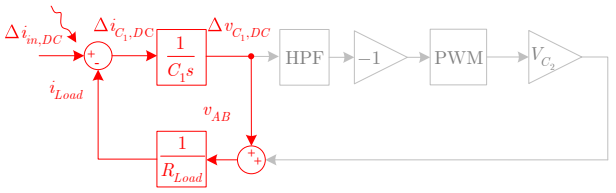
From above analysis, it can be seen that the over-voltage during the load change is introduced by the DC disturbance. In order to eliminate the effect introduced by the $\Delta v_{\mathrm{C_1,DC}}$, the negative $\Delta v_{\mathrm{C_1,DC}}$ is fed at the load disturbance point. The voltage feed-forward control scheme is obtained as shown in



(a) Simplified equivalent model of the active capacitor.

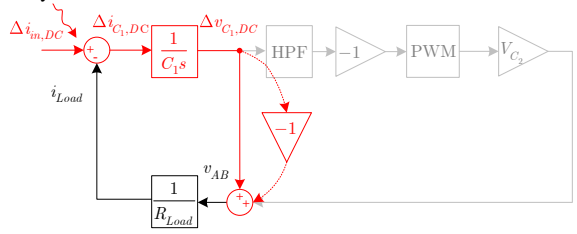


(b) Flowing path of the AC disturbance.

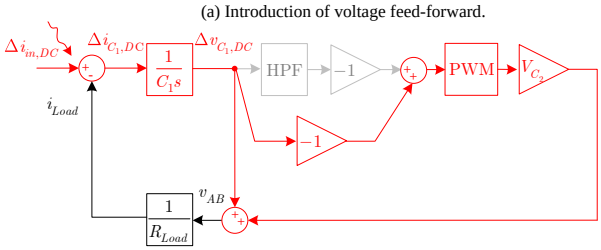


(c) Flowing path of the DC disturbance.

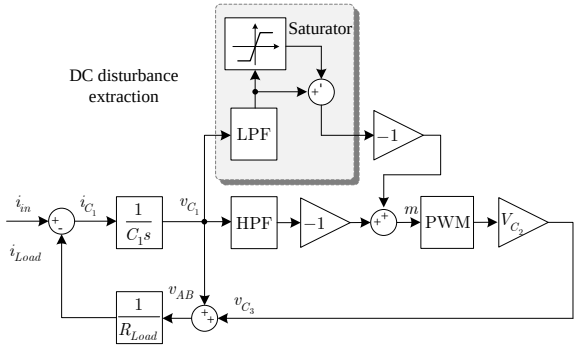
Fig. 8. Equivalent model of the active capacitor for disturbance analysis.



(a) Introduction of voltage feed-forward.



(b) Equivalent transformation of voltage feed-forward.



(c) Volatge feed-forward structure.

Fig. 9. Derivation of the voltage feed-forward compensation scheme for overshoot reduction.

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Figs. 9 (a) and (b). The negative signal is added to the modulation signal for disturbance mitigation. The LPF or notch filter is used to extract the DC component of v_{C_1}, and a saturator is used to obtain the DC disturbance. With this configuration, the controller of the system is nonlinear including two modes. Mode I: Within the bandwidth of the saturator, the feed-forward control is disabled. Only the conventional controller is in operation. Mode II: overtop the bandwidth of the saturator and within modulation capability, the feed-forward control is enabled to reduce the over voltage.

B. Equivalent Model of the Active Capacitor

1) Capacitance: Based on the (26), the equivalent capacitance is obtained as

$$C_{\rm eq}(s) = \frac{C_1 C_2 V_{\rm tric}}{MC_1 G_2(s) G_{\rm LPF}(s) V_{C_2} + M^2 C_1 V_{\rm tric}} \overline{-\alpha C_2 G_{\rm HPF}(s) V_{C_2} + C_2 V_{\rm tric}} \tag{27}$$

It can be noted that the equivalent capacitance is frequency-dependent.

2) ESR: The ESR of the active capacitor is derived from the total power loss of the active capacitor contributed by the auxiliary circuit and C_1. Based on (7), the power loss of the active capacitor is derived as

$$P_{\rm loss-Acap} = \frac{I_{\rm n}^2}{2nC_1\omega}(1-\eta_2) + \frac{I_{\rm n}^2 R_2}{2} \tag{28}$$

The equivalent ESR of the active capacitor can be obtained as follows

$$ESR = \frac{P_{\rm loss-Acap}}{I_{\rm n}^2/2} = \frac{(1-\eta_2)}{nC_1\omega} + R_2 \tag{29}$$

3) ESL: ESL of the active capacitor contains two parts: one is L_{C_1}, which is the ESL of C_1, and the other one is the parasitic inductance of the auxiliary circuit, $L_{\rm aux}$, depending on the physical layout design of the active capacitor.

$$ESL = L_{C_1} + L_{\rm aux} \tag{30}$$

Assuming the efficiency of the active capacitor is 94 % and $L_{\rm aux}$ is 30 nH, the equivalent model shown in Fig. 10.

In the bandwidth from 100 Hz to 1 kHz of interest, the impedance curves can match with 1100 μF capacitor with a significantly lower energy storage. The phase angle of the active capacitor at 100 Hz is higher than -90deg . It implies that the active capacitor has a positive resistance component and absorb power from the external circuit through terminals A and B at higher frequency level (e.g., 100 Hz or above). This mechanism makes it possible to regulate the voltage of capacitor C_2 even under low-frequency disturbances, with the aid of the feedback control loop of v_{C_2} shown in Fig. 1.

V. Start-up Solutions for the Active Capacitor

This section discusses the start-up process of the active capacitor with a conventional scheme and two proposed solutions to overcome the associated challenge.

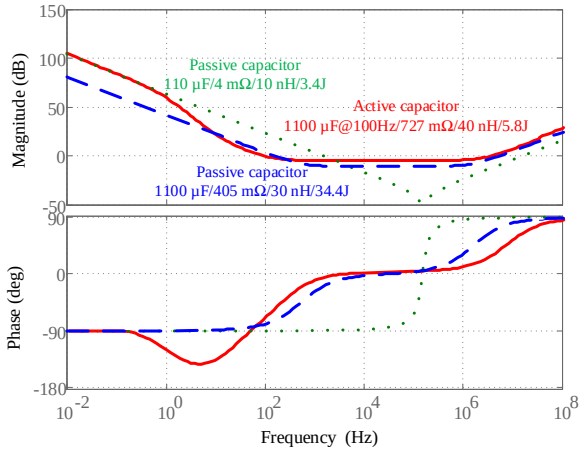

Fig. 10. Bode diagram of the passive capacitor and equivalent bode diagram of an active capacitor.

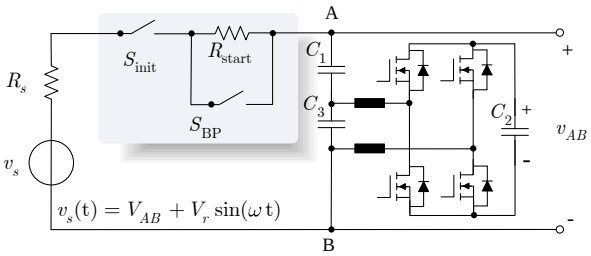

Fig. 11. The circuit diagram of an active capacitor with conventional start-up solution.

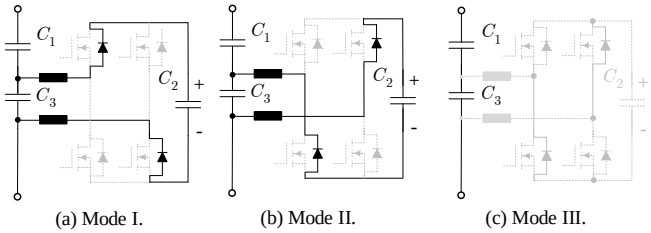

Fig. 12. Three modes of the active capacitor during the start-up procedure.

A. Start-up Process Analysis with a Conventional Scheme

Fig. 11 shows a typical start-up circuit widely applied in power electronic circuits [25]. $v_{\rm s}$ and $R_{\rm s}$ are the equivalent voltage source and resistor. $S_{\rm init}$, $S_{\rm BP}$ and $R_{\rm start}$ are the components of the conventional start-up circuit. If the active capacitor is used in a power electronic system already including such a start-up circuit, the equivalent operation modes of the start-up process are shown in Fig. 12. It assumes that the initial capacitor voltage is 0 V. The three operation modes are described as follows.

Mode I: If the voltage of C_3 is higher than voltage of C_2, C_2 will be charged as shown in Fig. 12 (a). It happens at the beginning several fundamental cycles. The circuit is equivalent to C_2 connected in parallel with C_3 and then connected in series with C_1. The voltage of C_1 and C_3 can be obtained as

$$\begin{cases} v_{C_1}(t) = (V_{\rm AB} + V_{\rm r}\sin n\omega t)\frac{C_2+C_3}{C_1+C_2+C_3} \\ v_{C_3}(t) = (V_{\rm AB} + V_{\rm r}\sin n\omega t)\frac{C_1}{C_1+C_2+C_3} \end{cases} \tag{31}$$

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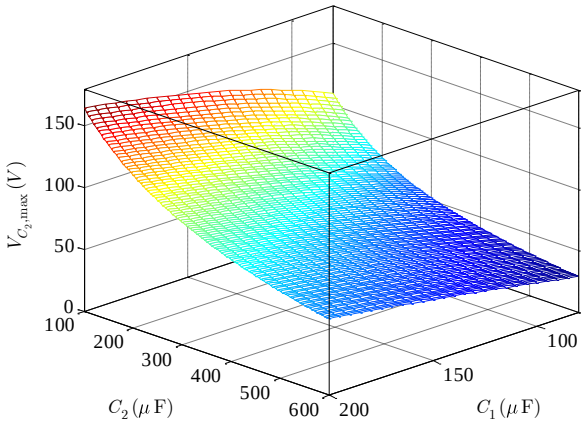


Fig. 13. The relationship between $V_{\mathrm{C_2,max}}$, C_1 and C_2 for the conventional start-up solution I shown in Fig. 11.

Thus, the maximum voltage of C_3 becomes

$$V_{\mathrm{C_3,max}} = (V_{\mathrm{AB}} + V_{\mathrm{r}})\frac{C_1}{C_1 + C_2 + C_3} \tag{32}$$

From the analyses of the three operation modes, it can be seen that the voltage stress of C_3 is effected by the parameters of C_1, C_2 and C_3 in mode I.

Mode II: If the negative voltage of C_3 is higher than the voltage of C_2, C_2 will also be charged as shown Fig. 12 (b) mode II. During the start-up procedure, the DC charging current will introduce DC voltages in C_1, C_2 and C_3. Thus, the negative voltage of C_3 is never higher than the voltage of C_2. Mode II will not happen during the start-up process.

Mode III: The other mode is when the voltage of C_3 is lower than that of C_2, the current will only flow through C_1 and C_3. There will have large ripple voltage on C_3, which is lower than the voltage of C_2, otherwise mode III will transfer to mode I. Thus, in this case, the maximum voltage of C_2 is same with that in mode I, while the maximum voltage of C_3 is lower than that of C_2.

From above three modes analysis, the maximum voltage of C_2, which is same with the maximum voltage of C_3 is

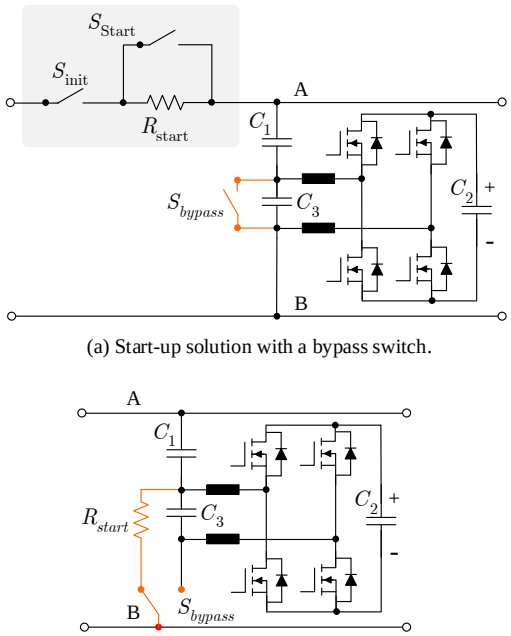
$$V_{\mathrm{C_3,max}} = (V_{\mathrm{AB}} + V_{\mathrm{r}})\frac{C_1}{C_1 + C_2 + C_3} \tag{33}$$

With the conventional start-up solution, the inrush charging current can be limited into the specification of the system. However, C_2 and C_3 may experience over-voltage, depending on the voltage of the source and the parameters of the capacitors.

B. Proposed Start-up Solutions

According to the analysis in Part A, the key issue is how to limit the maximum voltage of C_2 to avoid over-voltage of the components used in the active capacitor. Two start-up solutions to tackle the issue are proposed below.

1) Solution I - Re-sizing of C_2: The constraints for sizing C_2 shown in Fig. 5 do not take the start-up process into account. According to (33), the increase of C_2 is beneficial to the reduction of the maximum voltage of C_2, therefore, the



(a) Start-up solution with a bypass switch.

(b) Integrated version of the solution shown in (a).

Fig. 14. Start-up solution through a bypass switch to charge the C_1 at the beginning.

voltage stresses on the power switches in the auxiliary circuit of the active capacitor. With the conventional start-up circuit shown in Fig. 11, an additional design constraint among the values of C_1, C_2, and maximum voltage of C_2 is obtained as shown in Fig. 13. For a given limit of $V_{\mathrm{C_2,max}}$ and C_1, a minimum value of C_2 can be found to avoid over-voltage during start-up process. The drawback of this solution is that a higher value of C_2 is required compared to that based on the constraints shown in Fig. 5.

2) Solution II - Bypass switch: Fig. 14 (a) proposes a solution based on a bypass switch connected in parallel with C_3 without the need of over-sizing C_2. At the beginning of the start-up, the bypass switch S_{bypass} is turned on. The auxiliary circuit of the active capacitor is bypassed and only the C_1 is charged. Until the voltage of C_1 reaches its steady-sate, the bypass switch is turned off. The capacitors C_2 and C_3 start to be charged.

The charging current and the voltage of C_3 are both sinusoidal, implying that there is no DC voltage in $v_{\mathrm{C_3}}$. The voltage across C_2 finally reaches to the maximum voltage of C_3, that is

$$V_{\mathrm{C_2,max}} = V_{\mathrm{r}}\frac{C_1}{C_1 + C_2 + C_3} \tag{34}$$

Fig. 14 (b) shows an alternative version of Fig. 14 (a) by combing the conventional start-up circuit and the bypass switch function into the active capacitor. The operation principle is similar as the solution shown in Fig. 14 (a). The advantage of this integrated version is that the implemented active capacitor has self-start-up protection circuit which is independent of the external circuit design.

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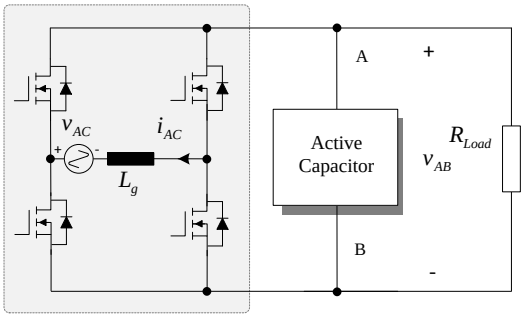


Fig. 15. The circuit topology of the single-phase rectifier with an active capacitor.

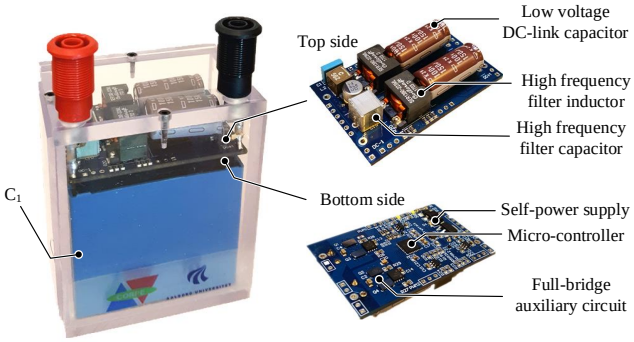


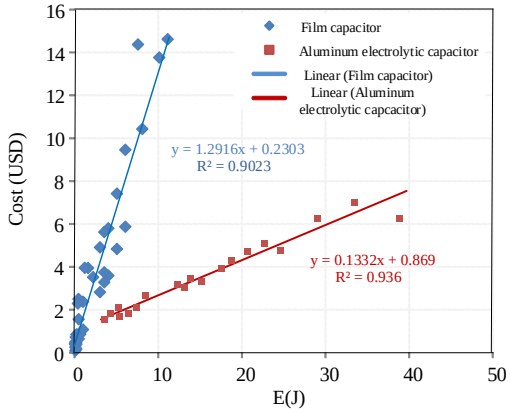
Fig. 16. Two-terminal active capacitor prototype for DC-link application.

VI. A Case Study for a Capacitive DC Link Application and Experimental Verifications

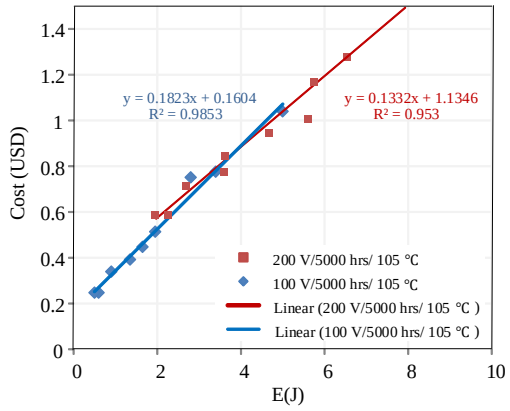
This section presents a case study of a two-terminal active capacitor for a capacitive DC link of a 750 W single-phase rectifier, as shown in Fig. 15. The specifications of the rectifier is shown in Table I. A two-terminal active capacitor prototype for DC-link application is built up as shown in Fig. 16. The testing procedure is that run the single-phase rectifier firstly, while the DC-link active capacitor will be initialized automatically with two start-up solutions. Then the steady-state and dynamic performance of the active capacitor can be provided by changing the load resistance. Following the same testing procedure, the performance of passive capacitor can also be obtained to make a comparable study.

A. Sizing of Key Components for the Cost-constraint Application

The key components of the two-terminal active capacitors are the capacitors C_1 and C_2, the four switching devices, the filter inductor L_{f}, in additional to a small filter capacitor C_3, the gate drivers and a micro-controller with relatively low computation capability. In principle, C_1 and C_2 can be implemented by electrolytic capacitors, film capacitors or ceramic capacitors. However, in most practical applications, aluminum electrolytic capacitors may not be suitable for C_1 due to its limited ripple current capability. For high power density applications, ceramic capacitors are preferable to C_1 and C_2 since its high volumetric efficiency as the design demonstrated in [10], at the expense of a relatively high cost. As the presented case study focuses on a cost-constraint application, film



(a) Curve-fitted cost models of 250 V film capacitors and electrolytic capacitors.



(b) Curve-fitted cost models of 100 V and 200 V electrolytic capacitors.

Fig. 17. Capacitor cost model used for sizing C_1 and C_2 [31].

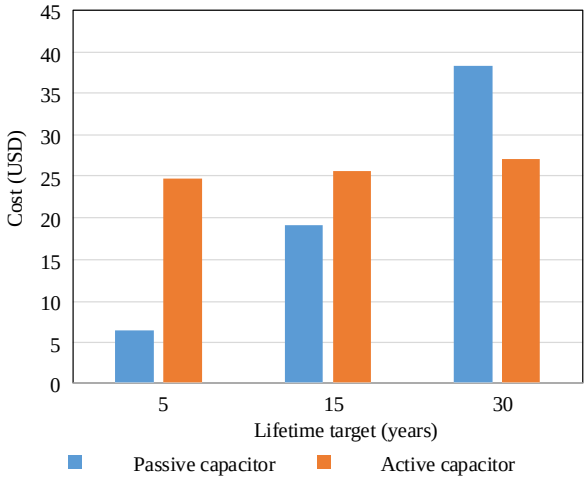


Fig. 19. Cost comparison between the active capacitor and the passive electrolytic capacitor.

capacitors and aluminum electrolytic capacitors are considered for C_1 and C_2, respectively. It should be noted that even moderate aluminum electrolytic capacitors could achieve as long as 15 years of lifetime by thermal and electrical aspects of derating [32]. Therefore, film capacitors are not necessarily favorable for C_2 to meet a specific lifetime target from the cost

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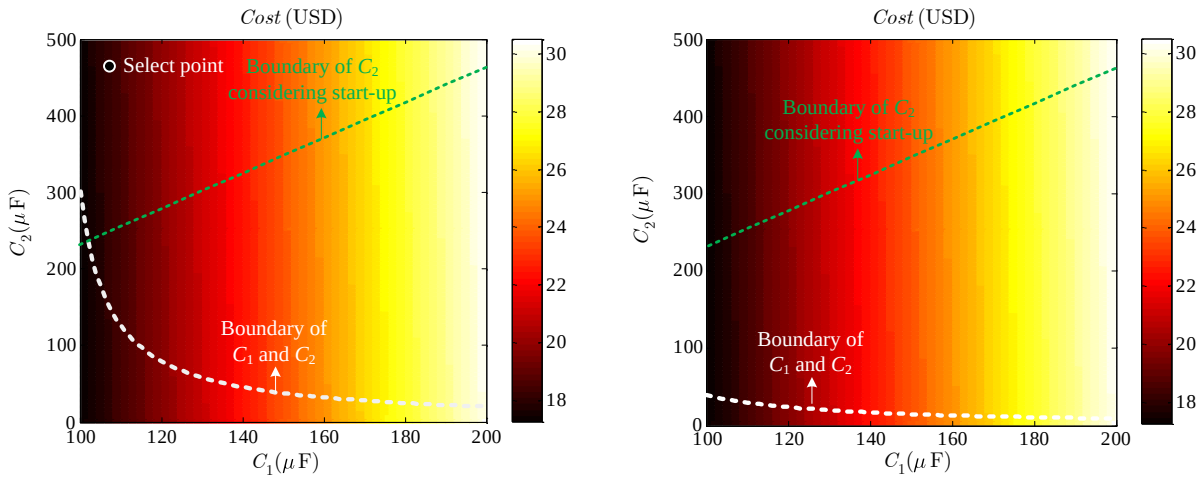

(a) Design space of C_1 and C_2 with a mapping of total component cost ($V_{C2,\ max}$ = 66 V, by considering 100 V switching devices with 50% voltage margin)

(b) Design space of C_1 and C_2 with a mapping of total component cost ($V_{C2,\ max}$ = 100 V, by considering 150 V switching devices with 50% voltage margin)

Fig. 18. The relationship between the capacitance of C_1, C_2 and the total cost of the active capacitor.

TABLE II
COST OF THE AUXILIARY CIRCUIT FOR THE ACTIVE CAPACITOR [31].

Component	Detail information	5 years cost	15 years cost	30 year cost
Passive capacitor	1200 / 250 V, ELXS251VSN122MA40S	6.4	19.2	38.4
C_1	60 μF / 250 V*2, C4ATDBW5600A30J	16.4	16.4	16.4
C_2	470 μF / 100 V, UVR2A471MHD	0.5	1.5	3
MOSFETs	100 V, IRLR3410TRLPBF*4	2	2	2
Micro controller	Microchip dsPIC30F2011	2.6	2.6	2.6
Amplifiers IC	TLV2362IDR*2	0.6	0.6	0.6
Power supply	UA78M*2	0.6	0.6	0.6
PCB		1	1	1
Others		1	1	1

point of view. In order to establish the relationship between the component costs and the design constraints discussed in Section III, the component cost modeling method presented in [13] is applied to analyze the total component cost. Particularly, the cost models of film capacitors and aluminum electrolytic capacitors are shown in Fig. 17, which is based on the price information from Digikey [31] with an order quantity of 1,000 pcs. In the design of the two-terminal active capacitor, start-up solution I (Re-sizing of C_2) is incorporated, so that the cost comparison does not include the start-up circuit. By taking into account also the cost models of other key components as discussed in [33], the design spaces of C_1 and C_2 with 100 V and 150 V switching devices (50 % voltage margin) are shown in Fig. 17 (a) and (b), respectively.

It should be pointed out that the cost mapping shown in Fig. 18 are based on limited component price information and without considerations into the manufacturing cost and installation cost, etc. The numerical results serve as a comparative study for preliminary selection of design solutions. More comprehensive cost information is needed for a more accurate analysis.

From Fig. 18 (a), it can be seen that the cost of the active capacitor is mainly determined by C_1. The dashed line is the design constraint of C_1 and C_2, in consistent with that shown in Fig. 5. Each design point above the dash line may result in a different lifetime as well. The reliability-oriented sizing procedures for the capacitors and switching devices follow the ones discussed in [13]. For a 15 years of lifetime target with reliability of 0.9 (e.g., 15 years of B10 lifetime), the selected design point is $C_1 = 110\mu F$, $C_2 = 470\mu F$, 100 V MOSFETs, as shown in Table I as well. The corresponding total component cost is minimum of 18 USD. With 150 V MOSFETs, the minimum component cost becomes 19 USD according to Fig. 18 (b).

For comparisons between the active capacitor with passive capacitor, the auxiliary component shown in Table II (e.g., controller, amplifiers ICs, PCB ect.) should be taken into account for fairly to compare with the passive capacitors [17] [18]. The cost benchmarking between the passive capacitor and the active capacitor are shown in Fig. 19. The total system cost with active capacitor introduces 36.8 % increment than that with the passive capacitor for B10 lifetime 15 years lifetime target, and 28.9 % reduction than the passive capacitor for B10 lifetime 30 years lifetime target.

B. Steady-state Performance of the Active Capacitor

An experimental setup is built up to verify the active capacitor with C_1 =110 μF, where the selected design point shown in Fig. 18 (a). In the controller, due to the DC-link ripple harmonics is 120 Hz, the cut-off frequency of the HPF is 10 Hz in design. LPF with 20 Hz cut-off frequency is to acquire DC component of v_{C_2} to maintain a stable DC-link

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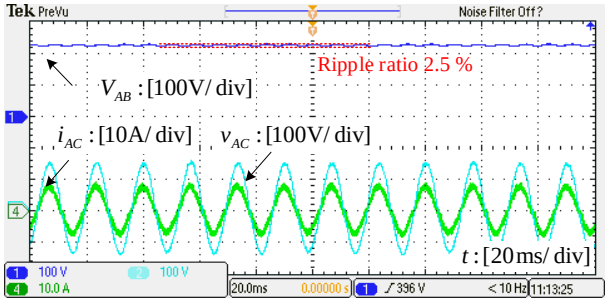
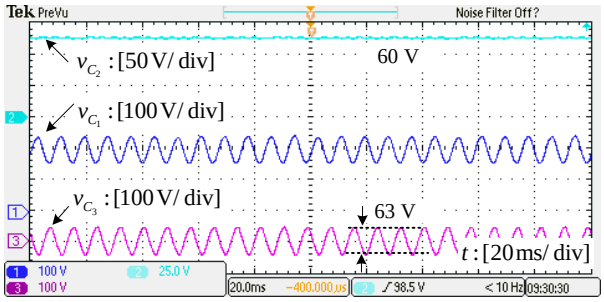
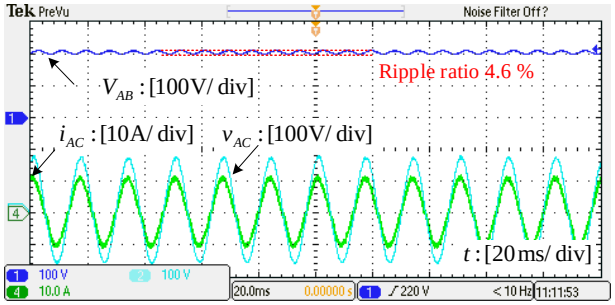


(a) Waveforms of the DC-link voltage, and the rectifier input voltage and input current with 50 % load.

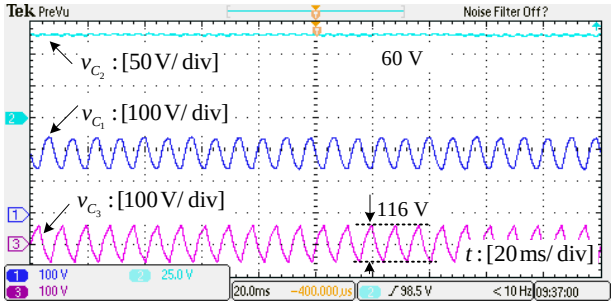


(b) Voltage waveforms of the C_1, C_2, and C_3 inside the active capacitor.

Fig. 20. Steady-state waveforms of the 750 W rectifier with 100 % load.



(a) Waveforms of the DC-link voltage, and the rectifier input voltage and input current with 100 % load.



(b) Voltage waveforms of the C_1, C_2, and C_3 inside the active capacitor.

Fig. 21. Steady-state waveforms of the 750 W rectifier with 50 % load.

voltage for the full-bridge converter. The PI controller $G_2(s)$ is in the feedback control loop for stabilizing the voltage of C_2, where the K_p and K_i are tuned as 0.01 and 0.1, respectively. Fig. 20 shows the experimental waveforms of the rectifier and the key components inside the active capacitor under full-load condition. Both AC voltage and current operate with unit power factor, while the voltage ripple of the DC link is 4.6 %, which fulfills the design specification. The average voltage of v_{C_2} is controlled to be constant and v_{C_3} follows

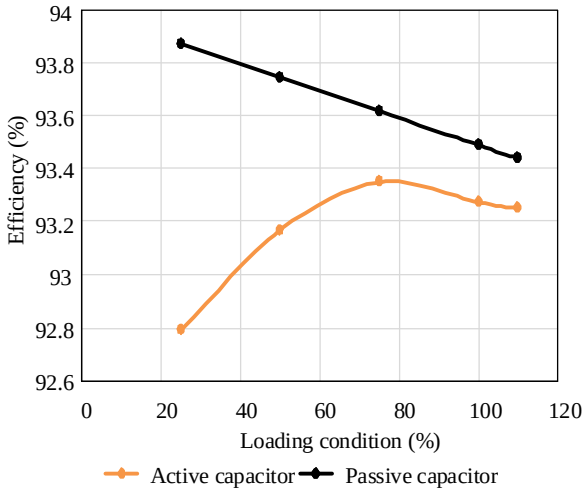


Fig. 22. Efficiency curves of the single-phase systems with active and passive capacitor.

the voltage ripple of v_{C_1}. The voltage of C_2 is controlled at 60 V with a ripple of 3.6 V, which is higher than $v_{\mathrm{C}_3}(t)$. It can be noted that the voltage ripple of C_1 is approximately out of phase with v_{C_3}. The slight phase shift is due to the mechanism to absorb an insignificant amount of active power to compensate the power loss of the active capacitor. The experimental results with 50 % load is shown in Fig. 21. Fig. 22 shows the efficiency of the single-phase system with active capacitor and the passive capacitor. With higher power rating, the efficiency of the system with passive DC-link capacitor is reduced, while the efficiency of the system with the active capacitor is increased. At rated load, the efficiency of the auxiliary circuit is 94 %, while the efficiency drop of the whole system introduced by the active capacitor is 0.2 %, which is compatible with the analysis in theory.

C. Dynamic Response of the Active Capacitor

The load step-down from 100 % to 50 % is considered as a case study to show the dynamic response of the active capacitor with and without the voltage feed-forward control scheme. Fig. 23 (a) shows the comparative results of the rectifier with a passive capacitor of 1100 μF (i.e., total rated energy storage of 34.4 J). The DC-link voltage ripples before and after the load change are 5 % and 3 %, respectively, with an overshoot of 216 V. Fig. 23 (b) shows the experimental waveforms of the rectifier with the active capacitor with the feed-forward voltage control. The voltage ripple of the DC link is limited within 5 % with 16.8 % of total rated energy storage compared to the passive solution, with a slightly higher overshoot of 221 V. The experimental results of the active capacitor with the feed-forward compensation are shown in Figs. 23 (d) and (e). The overshoot is reduced to 217 V.

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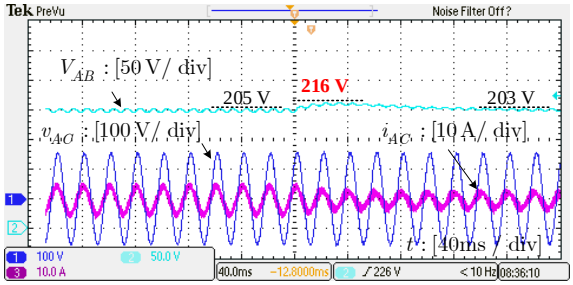
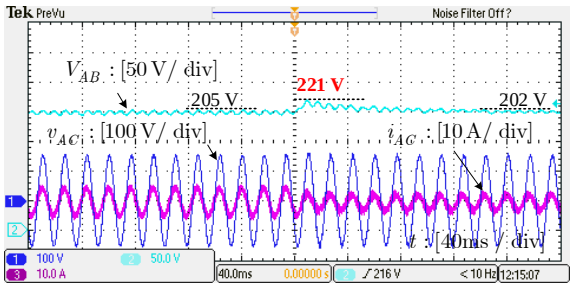
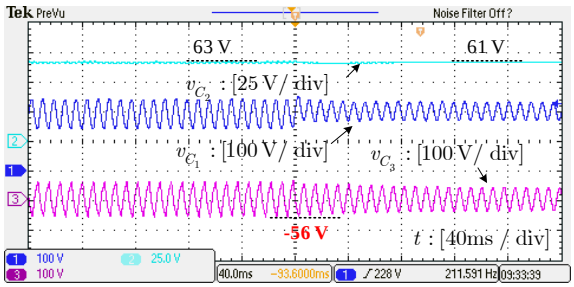


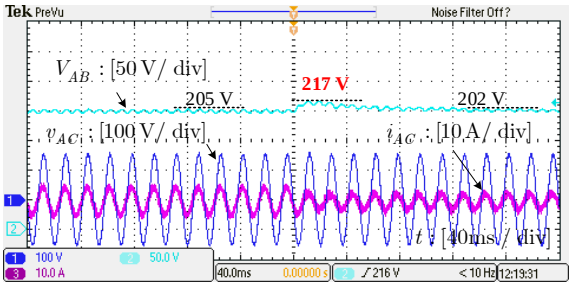
(a) Dynamic response of a capacitive DC link with a 1,100 uF electrolytic capacitor (34.4 J total rated energy storage)



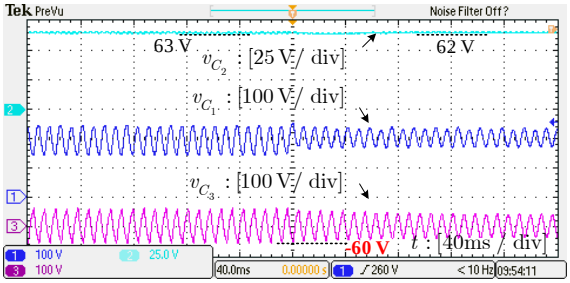
(b) Dynamic response of a capacitive DC link with the active capacitor (5.8 J total rated energy storage) without the voltage feed-forward control.



(c) Dynamic response of voltages of C_1, C_2, and C_3 inside the active capacitor (5.8 J total rated energy storage) without the voltage feed-forward control.

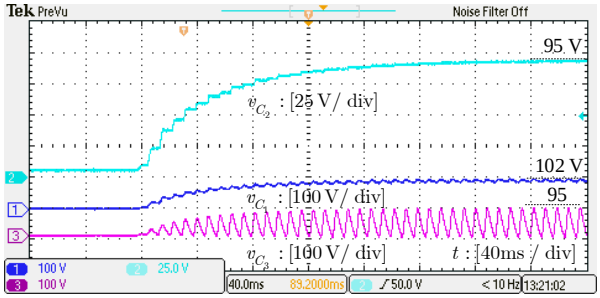


(d) Dynamic response of a capacitive DC link with the active capacitor (5.8 J total rated energy storage) with the voltage feed-forward control.

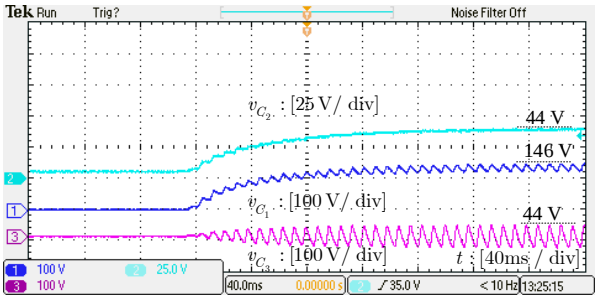


(e) Dynamic response of voltages of C_1, C_2, and C_3 inside the active capacitor (5.8 J total rated energy storage) with the voltage feed-forward control.

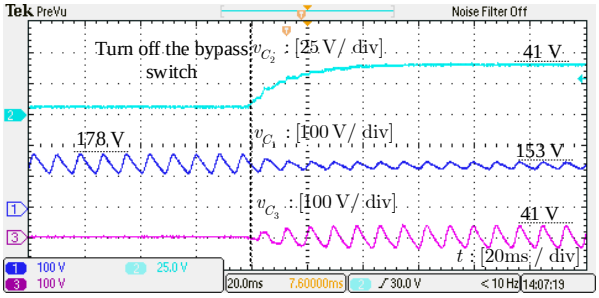
Fig. 23. Experimental waveforms on the dynamic response of a capacitive DC link with a passive capacitor, an active capacitor with and without voltage feed-forward control (with a load change from 100 % to 50 % in a 750 W single-phase rectifier)



(a) Capacitor waveforms of the active capacitor with conventional start-up solution.



(b) Capacitor waveforms of the active capacitor with component sizing solution.



(c) Capacitor waveforms of the active capacitor with bypass switch solution.

Fig. 24. Experimental waveforms of the voltage stresses of C_1, C_2, and C_3 with different start-up solutions.

D. Start-up of the active capacitor

Following the basic operation criteria discussed in Section III, if C_1=110 μF, the minimum C_2 is 150 μF. Fig. 24 (a) shows the key waveforms of the active capacitor with $C_2 = 150\mu F$. The voltage stresses on C_2 and C_3 are 95 V, which exceed the limit of 60 V. By increasing C_2 to 470 μF, the maximum voltage stresses of C_2 and C_3 are reduced to 44 V, which is within the design specification, as shown in Fig. 24 (b). Fig. 24 (c) presents the experimental results with a bypass switch shown in Fig. 14 (b). In this implementation, bypass switch is a relay with two switching states. When the DC voltage has been built in C_1, the switch turns off to initialize the active capacitor. At the beginning, the bypass switch is in on-state. C_1 withstands all the DC-link voltage. There is no current flowing through the auxiliary circuit. When the bypass switch is turned off, the AC current charges C_2 and C_3 through the diode bridge. Therefore, no DC component appears in v_{C_3}. The maximum voltages of C_2 and C_3 are limited to 41 V, which is within the design specification.

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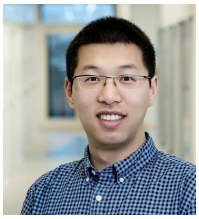
VII. Conclusions

This paper investigates the component sizing, impedance characteristics, and start-up solutions of a two-terminal active capacitor for cost-constraint and reliability-specific applications. In the case study of a 750 W single-phase rectifier with a DC link voltage of 200 V, the active capacitor achieves comparable steady-state performance and dynamic response as a 1,100 uF passive capacitor, with 16.9 % total rated energy storage only. The overall cost of the active capacitor is 136 % as the passive capacitor to fulfill a reliability target of 0.9 at 15 years of service. When comes to a more demanding reliability performance, the active capacitor has the potential to reducing the overall design cost (i.e., estimated 28.9 % cost reduction for a reliability target of 0.9 at 30 years of service). Experimental results also demonstrate the effectiveness of the proposed two start-up solutions to avoid over-stress of the key components in the active capacitor.

The case study reveals that two-terminal active capacitors become attractive for applications with a relatively high reliability requirement. There are application scenarios that passive capacitor based solutions show superior performance in terms of design cost. It should be noted that the presented case study is limited to its cope for cost-constraint applications and based on the state-of-the-art reliability modeling and cost modeling approaches. The conclusions draw from the study are not inclusive to all the application scenarios. With different DC-link voltage levels and DC-link voltage ripple specifications, the application scenarios which the active capacitors show better cost-effectiveness can be obtained by following the analysis method proposed in this study.



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