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ABSTRACT This paper mainly focuses on the analysis, DC-transformer modeling, comparison, and experimental investigation of a non-inverting and non-isolated Nx multilevel boost converter (Nx MBC) for low to high DC applications. Recently, numerous isolated and non-isolated DC-DC converter configurations have been addressed for low to high DC voltage conversion purposes, which is vital for several applications (e.g., renewable energy, medical equipment, hybrid vehicles, fuel cells, DC-links, multilevel inverters, and drive applications), by utilizing and modifying the structure of reactive elements (switched capacitors and switched inductor circuitry). Among all the switched reactive structures, voltage multiplier circuitry provides a feasible solution for low to high DC voltage conversion due to its flexible and modular structure, voltage clamping capability, reduced rating of components, and ease of modification. Non-inverting and non-isolated Nx MBC combine the features and structures of conventional boost converters and voltage multiplier circuitry. DC-transformer modeling of Nx MBC is discussed for the continuous current mode (CCM) and discontinuous current mode (DCM), which helps to analyze the characteristics of the converter in a more practical way and helps to study the effect of semiconductor components, internal resistances, and load on the voltage conversion ratio of the converter. The mode of operation of Nx MBC in the CCM and DCM is also discussed with the boundary condition. The derived analysis is verified by simulations and experimental investigations, and the obtained results of 3x MBC always show good agreement with each other and the theoretical analysis.

INDEX TERMS Boost converter, DC to DC, DC-transformer modeling, CCM, DCM, multilevel, non-inverting, non-isolated, voltage multiplier.

NOMENCLATURE

$\rfloor_{on}$, $\rfloor_{off}$	Defines ON and OFF state
Δ, dX	Small change, Small change in X
$\uparrow$, $\downarrow$	Charging and discharging of the capacitor
χ	Dimensionless parameter (a measure of the tendency of the converter to operate in DCM)
ξ	Voltage Reduction Factor
α	Drop factor measure in ohms
$\Delta i_L(t), \Delta v_c(t)$	A ripple of inductor current and the capacitor voltage
$\chi_{critical}(k)$	Defines CCM and DCM boundary,
$C_{critical}, L_{critical}$	Critical Capacitance and Inductance
C_{ij}, L, D_{ij}	Capacitor, Inductor and Diode (subscript ij defines the number of capacitor and diode)
C_{ON}, C_{OFF}, C_Z	Equivalent capacitance in ON state, OFF state and DCM

f_s, T_S, k	Switching frequency, Time period, duty cycle
$i_C(t), I_C$	Capacitor current, Average capacitor current
$i_{in}(t), I_{in}$	Input current, Average input current
$i_L(t), I_L$	Inductor current, Average Inductor current
$i_s(t), I_S$	Switch current, Average switch current.
N, N_X	Number of levels of the converter, N times
R, S	Load resistance in ohm, Control switch
$R_{d,on}$	ON state resistance of the Diode
R_{in}	Internal resistance of input voltage source
R_l	Internal resistance of inductor
$R_{S,on}$	ON state resistance of the MOSFET
T_{on}, T_{off}	ON and OFF Time of MOSFET
Vs or V_{DS}	Drain to source voltage of MOSFET
$V_{d,on}$	Thermal voltage of Diode
V_{in}	Input voltage (Average value)
$v_o(t), V_o$	Output voltage and average output voltage
$v_{1x}(t), v_{2x}(t)..$	Output voltage for N=1, 2, ..
$V_{1x}(t), V_{2x}(t)..$	Average Output voltage for N = 1, 2 . . .
$x(t)$	A voltage drop occurs while charging and discharging of the inductor.

I. INTRODUCTION

Recently, DC-DC multistage converter configurations have been well established and are a key technology for home to industrial and low to high voltage conversion applications, e.g., photovoltaic (PV) and fuel cell (FC) applications, DC-link, Multilevel Inverter (MLI), medical equipment, automobiles, large offshore wind farms, and HVDC [1]–[4]. Currently, among all renewable energies, PV energy is gaining more attention because it is a clean, cheap, unlimited source and because of the depletion of fossil fuels. To utilize renewable energy sources for real-time applications, DC-DC boost converters with high conversion ratios are compulsory, particularly for PV and FC applications, because the output voltage is generally in the range of 12-48 V, differing for the power capability of the panels and the cell [5]–[8]. Conventional DC-DC converters are not advisable to incorporate with low voltage energy sources to achieve high voltage because, with a larger duty cycle, the parasitic components limit the voltage conversion ratio. Moreover, high voltage and current stress appear on the devices, along with low reliability, reverse recovery problems of diodes, electromagnetic interference (EMI) and low voltage conversion efficiency [9], [10]. Numerous DC-DC converter configurations have been proposed in the literature due to the continuous requirement of DC-DC converter configurations with high reliability and efficiency, small-sizes, and light in weight for voltage boost conversion applications [11]–[13]. Cascade versions of conventional boost converters are an antiquated

key solution to generate high voltage from the low voltage source. The main drawbacks of the cascaded converter are complex control algorithms and circuitry with the requirement of several inductors, controlled switches with different ratings and driver modules, etc. [14], [15]. Later, the structure of the cascaded converter is modified, and Quadratic Boost Converter (QBC) circuitry is designed by using only two conventional stages and a single switch [16], [17]. However, the entire output voltage appears across the control switch, which increases the voltage rating, stress, and cost of the switch. Moreover, QBC also required two inductors and a high current capable control switch since the total input current is passed through the switch.

Many isolated DC-DC converters, such as forward converters, flyback converters, bridge converters, and push-pull converters, have been proposed with several arrangements of the transformer and coupled inductor to achieve a high voltage conversion ratio [18], [19]. In isolated DC-DC converter configurations, a high voltage is achieved by increasing the number of turns of the transformer and the coupling factor of the coupled inductor. A flyback converter is commonly employed to attain a high conversion ratio by selecting the proper transformer with a suitable number of turns [20], [21]. In the flyback converter, the transformer leakage inductor causes high voltage spikes and induces energy losses. Nevertheless, the addition of a high-frequency transformer and coupled inductor increases the price of the converter, produces high power losses due to the leakage inductance of the transformer, and makes the circuit bulky. Somehow, active clamping and snubber circuitry is employed in an isolated converter to reduce the aforementioned problems, but this circuitry increases the complexity of the control, size, and price [20], [21]. In the last few years, to achieve a high conversion ratio, many boost converters based on tapped and coupled inductors have been addressed with low voltage stress across the switch and without using a high duty cycle [22]–[25]. Conversely, as the coupled or tapped inductor turn ratio increased to obtain a high voltage conversion ratio, the ripple in the input current increased. Hence, a high-quality input filter is employed in the isolated coupled inductor converter. To decrease the ripple of input current, cross-coupled inductor winding methodology and the interleaved converter was presented as the solution [25], [26].

Due to the advantages of non-isolated configurations,e.g., simple structure, light-weight design and small size, many non-isolated converter configurations using switched capacitor circuitry (voltage doubler, quadruple, voltage multiplier, Dickson charge pump, etc.) and switched inductors (voltage lift, re-lift, self-lift, etc.) have been articulated for low to high voltage conversion applications [26]–[28]. A review of non-isolated converter configurations is discussed in [11] and [15]. By means of these methods, the voltage conversion ratio is augmented appropriately for the applications; nevertheless, the existing drawback is the rating of semiconductor switches, complex control circuitry and a large number of components. In [26] and [29], to achieve a high voltage

conversion ratio with high efficiency, a minimal number of control switches, and wide-range operation, a parallel and series connected non-isolated converter configuration was proposed for renewable energy applications. However, high current and voltage stress, high voltage ripple, and complex switching, as well as the large size, cost and absence of sufficient performance, are the main drawbacks of this technique. To reduce the number of inductors, switched capacitor methodology is presented in [30]–[32], and the large voltage conversion ratio is attained only by the arrangement of the control switches and capacitors. However, the requirement of complex control circuitry due to several switches, a large current ripple, and a large number of capacitors are the main drawbacks of designing this converter with a high voltage conversion ratio. Moreover, switching loss is due to the hard switching of several control switches, which is the main drawback of this technique. Further, in [34], a converter was proposed by modifying the arrangement of the diode and the capacitor, with advantages such as minimum voltage stress and easy control. Due to flexible arrangement of the capacitor and switches, these converters are gaining more attention and increasing the interest in the achievement of new DC-DC converter configurations that can perform efficient low DC to high DC voltage conversion operations with a wide range.

To reduce the number of control switches, a new converter chain called the multilevel converter was proposed in [35] and [36], which combine the feature of the conventional DC-DC converter and the CW voltage multiplier. The benefits are that this configuration provides a viable solution for switched capacitor converters to attain a high voltage conversion ratio without using a large duty cycle (T_{on}/T_S) and a transformer. The input current is continuous, and it's a superior case of the switched capacitor, where all the control switches of the switched capacitor circuitry are replaced by diodes.

Originally, non-inverting and non-isolated Nx MBC is proposed in [35] and is believed to have several advantages, such as a single switch, minimum effective series resistance (ESR), continuous input current, a high voltage conversion ratio, a modular structure, transformer-less configurations, and a self-balanced structure [35]–[36]. In addition, the input side inductor plays a vital role in improving the voltage boosting factor of the converter. Controlling Nx MBC is similar to the traditional boost converter since the single switch and conventional PWM circuitry is required to control the voltage of all the capacitors, and each voltage multiplier stage only adds the voltage by a constant factor, which is equal to the voltage conversion ratio of the traditional boost converter. The power circuit of non-inverting and non-isolated Nx MBC is depicted in Fig. 1(a). It is noted that 2N-1 number of diodes, 2N-1 number of capacitors, a single MOSFET with the appropriate gate driver and a single inductor are required to design the power circuit of Nx MBC. Ideally, Nx MBC provides a voltage conversion ratio N times higher than that of the traditional boost converter. In [35], the mode of operation of Nx MBC along with the application, and the advantages of
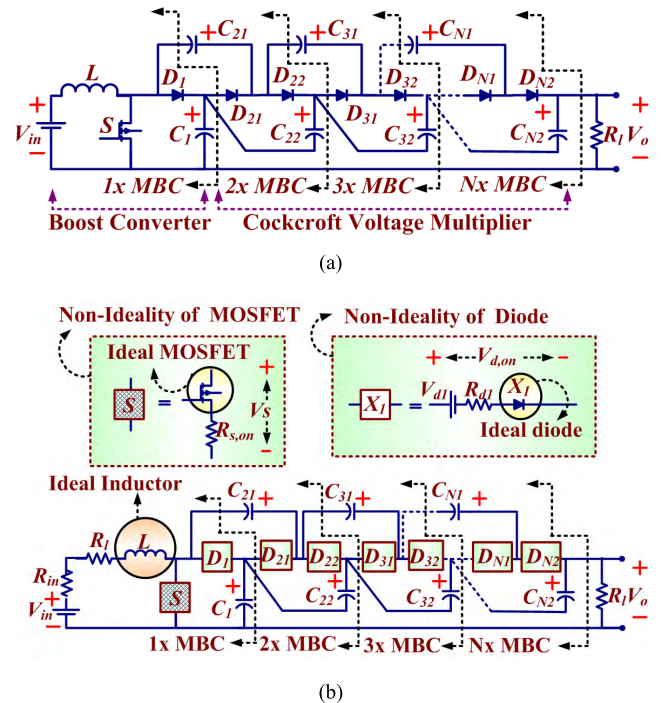

FIGURE 1. Power circuit of multilevel boost converter (a) Nx Multilevel Boost Converter configuration (Boost converter+ Cockcroft voltage multiplier), (b) Nx MBC configuration with non-idealities of inductor, diodes, switch and input supply. Note: 1x MBC, 2x MBC, 3x MBC, Nx MBC defines the power circuitry required to design one level, two level, three level MBC and N level MBC.

feeding voltage to the DC-link of the multilevel inverter by Nx MBC are discussed in detail. In [37]–[40], steady-state and AC equivalent circuits are discussed for other topologies, which are suitable for the low to high DC voltage conversion applications. In [41], several stabilization techniques as compensation have been reviewed for DC microgrid and DC-DC converter applications to overcome the issue of instability due to constant power load which shows negative incremental impedance. These stabilization techniques include, non-linear sliding surface, virtual resistance based technique (By impedance matching approach), sliding mode control (SMC), circular switching surface technique, damping technique, and an input filter feed forward stabilization technique etc. Further, in general, these stabilization techniques are classified in the three categories; 1) feeder side compensation (to make circuit robust against constant power load), 2) using additional intermediate circuit compensation (to enhance system stability), and 3) load side compensation (effect of constant power load is nullified). The Nx MBC structure is more suitable to feed MLI because of the stack of capacitors at the output side. Therefore, for voltage balancing and to maintain a constant voltage across each capacitor at the output side of Nx MBC (to feed MLI), source side compensation is more suitable to overcome the issue of the constant power instability. Several source side compensation techniques e.g. damping technique, Lyapunov stability theory, constant voltage source mode provides a possible solution to reduce constant power instability.
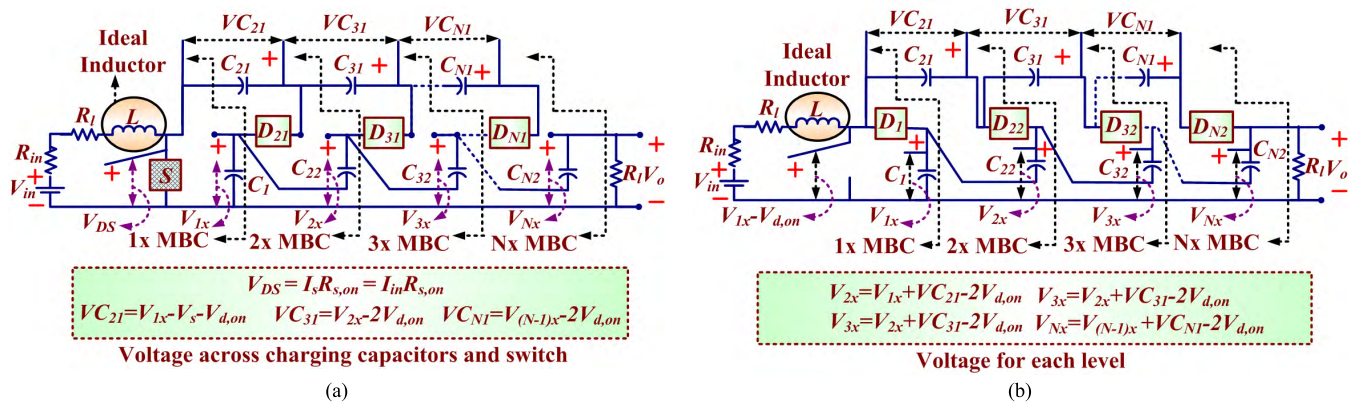
FIGURE 2. Equivalent circuitry of Nx MBC and equations (a) When MOSFET is turned ON, and (b) When MOSFET is turned OFF.

In light of the advantages of Nx MBC configurations, this article provides modeling, a detailed analysis, a reactive and semiconductor component design, and a comparison with the experimental investigation in CCM, as well as in DCM, for low to high DC applications. DC transformer modeling is presented by considering the internal resistance of the inductor and the source, and effect of the diodes at the same time, which is critical to the approach mentioned in [35]. In this paper, the boundary of CCM and DCM is presented with the relationship between the number of stages and the duty cycle, which is a new contribution in this field. Moreover, through simulations and experiments, the regulation of the converter for CCM and DCM at various duty cycles is investigated and verified.

The article is organized as follows: In the beginning, detailed nomenclature is provided to make the article clear and readable. Section-I discussed the introduction, art, and drawbacks of existing DC-DC converters, which have high voltage capabilities, along with the motivation and necessity of MBC. In section-II, the DC transformer modeling of Nx MBC in CCM and DCM is discussed, which provides another future direction for analysing the converter and its internal parasitic component effects on the voltage conversion ratio. Section-II also addresses the design of Nx MBC, and a comparison of Nx MBC is provided with several recently proposed converters. In section-III, a simulation and experimental investigation of Nx MBC for three levels with CCM and DCM are presented. Finally, the conclusion is provided in section-IV. Further, the acknowledgement section is provided. In the last section, selected references are provided to support the presented work.

II. DC TRANSFORMER MODELING OF Nx MBC
In this section, the Nx MBC configuration is modeled using a DC-Transformer, which allows for ease in the analysis and in the computation of the voltage conversion ratio, incorporating the effects of load, duty cycle, and internal resistance of the inductor, switch, and diodes at the same time. Generally, depending on the switching rate of the control

switch, the PWM switching frequency ($f_s = 1/T_s$) of the DC-DC converter lies in the range of 1 kHz to 1 MHz. Let us consider T_{ON} as the ON time during switching of the control switch. The Nx MBC configuration is a combination of a single boost stage and the voltage multiplier. Therefore, to model the Nx MBC configuration as a DC-Transformer, first, the circuit is analyzed by considering only the single stage and then modified for N stages based on the functioning of the voltage multiplier. In Nx MBC, multiplier circuitry is only used to transfer the energy of one capacitor to another capacitor (also called voltage clamping). Let us consider Nx MBC configuration with non-idealities, as shown in Fig. 1(b).

To analyze the Nx MBC circuit, assume the non-idealities (power loss) of the power source is modeled by the resistance in the series (R_{in}). Generally, the inductors of Nx MBC or any converter have power losses in two categories: copper loss and core loss. Resistor R_l is considered in series with the inductor to describe the copper losses of the inductor. Core loss occurs because of magnetic core eddy currents and hysteresis, which is minimal and neglected for the simplicity of derivation. The forward voltage drop due to the semiconductor device (MOSFET and Diode) is another most important cause of power loss (also called conduction loss). In Fig. 1(b), the forward voltage drop of MOSFET is modeled with resistance ($R_{s,on}$) and realistic accuracy. For the good accuracy, the diode X_1 (arbitrary diode name) is modeled by the ON state resistance (R_{d1}) series with the voltage source (V_{d1}). When MOSFET receives the high gate pulse, diode D_1 is turned OFF, and the inductor current increases with a constant slope because of the connected input supply voltage. Capacitor C_1 provides the energy to load (R).

A. CONTINUOUS CONDUCTION MODE (CCM) DC-TRANSFORMER MODELING OF Nx MBC
The equivalent circuit and equations of Nx MBC when MOSFET is turned ON and OFF are shown in Fig. 2(a) and Fig. 2(b) respectively. Initially, consider only 1x MBC for the analysis and the load connected across the capacitor C_1. When MOSFET is turned ON, the voltage across inductor L

is known by (1) and (3).

$$\left.\begin{array}{l} \underline{v_L(t)}\Big|_{on} = L\dfrac{di_L(t)}{dt}\Big|_{on} = V_{in} - \underline{x(t)}\Big|_{on} \\[2mm] \underline{x(t)}\Big|_{on} = \underline{i_{in}(t)}\Big|_{on} R_{in} + \underline{i_L(t)}\Big|_{on} R_l + \underline{i_s(t)}\Big|_{on} R_{s,on} \end{array}\right\} \quad (1)$$

where $\Big|_{on}$ defines the ON state of the MOSFET and $\underline{x(t)}\Big|_{on}$ is the drop that occurs in the ON state due to the internal resistance of the inductor, source, and switch. In general, $\underline{i_y(t)}\Big|_{on}$ is equal to $I_y + \underline{i_{y,ripple}(t)}\Big|_{on}$ where I_y is the DC component present in current $i_y(t)$, and $\underline{i_{y,ripple}(t)}\Big|_{on}$ is the ripple content in $i_y(t)$ when the switch is in ON state. It is observed that:

$$\underline{i_{in}(t)}\Big|_{on} = \underline{i_L(t)}\Big|_{on} \approx \underline{i_s(t)}\Big|_{on} \quad (2)$$

By putting equation (2) in (1), equation (3) is derived as:

$$\left.\begin{array}{l} \underline{v_L(t)}\Big|_{on} = L\dfrac{di_L(t)}{dt}\Big|_{on} = V_{in} - \underline{x(t)}\Big|_{on} \\[2mm] \underline{x(t)}\Big|_{on} = \underline{i_{in}(t)}\Big|_{on} (R_{in} + R_l + R_{s,on}) \end{array}\right\} \quad (3)$$

The current through capacitor C_1 is known by:

$$\underline{i_{c1}(t)}\Big|_{on} = C_1 \dfrac{dv_{C1}(t)}{dt}\Big|_{on} = \dfrac{-v_o(t)\big|_{on}}{R} \Bigg\} \quad (4)$$

In general, $\underline{v_y(t)}\Big|_{on}$ is equal to $V_y + \underline{v_{y,ripple}(t)}\Big|_{on}$ where V_y is ripple appears as DC component in voltage $v_y(t)$ and $\underline{v_{y,ripple}(t)}\Big|_{on}$ is the ripple content in $v_y(t)$ when switch is in ON state. For 1xMBC, $\underline{v_o(t)}\Big|_{on} = \underline{v_{1x}(t)}\Big|_{on}$.

When MOSFET is turned OFF, the voltage across inductor L_1 is known by (5) and (6).

$$\left.\begin{array}{l} \underline{v_L(t)}\Big|_{off} = L\dfrac{di_L(t)}{dt}\Big|_{off} = V_{in} - \underline{x(t)}\Big|_{off} - \underline{v_o(t)}\Big|_{off} \\[2mm] \underline{x(t)}\Big|_{off} = \left\{\begin{array}{l} \underline{i_{in}(t)}\Big|_{off} R_{in} + \underline{i_L(t)}\Big|_{off} R_l \\ + \underline{i_d(t)}\Big|_{off} R_{d1,on} + V_{d1,on} \end{array}\right\} \end{array}\right\} \quad (5)$$

where $\Big|_{off}$ defines the OFF state of the MOSFET and $\underline{x(t)}\Big|_{off}$ is the drop that occurs due to the internal resistance of the inductor, the source and the diode in the OFF state. For 1x MBC, $\underline{v_o(t)}\Big|_{off} = \underline{v_{1x}(t)}\Big|_{off}$.

It is observed that:

$$\underline{i_{in}(t)}\Big|_{off} = \underline{i_L(t)}\Big|_{off} \approx \underline{i_{d1}(t)}\Big|_{off} \quad (6)$$

By putting equation (6) in (5):

$$\left.\begin{array}{l} \underline{v_L(t)}\Big|_{off} = L\dfrac{di_L(t)}{dt}\Big|_{off} = V_{in} - \underline{x(t)}\Big|_{off} - \underline{v_o(t)}\Big|_{off} \\[2mm] \underline{x(t)}\Big|_{off} = \left\{\underline{i_{in}(t)}\Big|_{off} (R_{in} + R_l + R_{d1,on}) + V_{d1,on}\right\} \end{array}\right\} \quad (7)$$

The current through capacitor C_1 is known by:

$$\underline{i_{c1}(t)}\Big|_{off} = C_1 \dfrac{dv_{C1}(t)}{dt}\Big|_{off} = \underline{i_{in}(t)}\Big|_{off} + \dfrac{-v_o(t)\big|_{off}}{R} \Bigg\} \quad (8)$$

Using a linear ripple or a small ripple approximation, equations (9)–(12) are obtained.

$$\left.\begin{array}{l} \underline{v_L(t)}\Big|_{on} \approx V_{in} - \underline{x(t)}\Big|_{on} \\[2mm] \underline{x(t)}\Big|_{on} \approx I(R_{in} + R_l + R_{s,on}) \end{array}\right\} \quad (9)$$

$$\left.\begin{array}{l} \underline{v_L(t)}\Big|_{off} \approx V_{in} - \underline{x(t)}\Big|_{off} - \underline{V_o(t)}\Big|_{off} \\[2mm] \underline{x(t)}\Big|_{off} \approx \left\{I(R_{in} + R_l + R_{d1,on}) + V_{d1,on}\right\} \end{array}\right\} \quad (10)$$

$$\underline{i_{c1}(t)}\Big|_{on} \approx \dfrac{-V_o\big|_{on}}{R} \Bigg\} \quad (11)$$

$$\underline{i_{c1}(t)}\Big|_{off} \approx I + \dfrac{-V_o\big|_{off}}{R} \Bigg\} \quad (12)$$

The Inductor Volt-Second Balanced (IVSB) methodology is applied, and the following equations are obtained:

$$\langle v_L(t)\rangle = \dfrac{1}{Ts}\int_0^{Ts} v_L(t)dt = \dfrac{1}{Ts}\left[\begin{array}{c} \int_0^{Ton} \underline{v_L(t)}\Big|_{on} dt \\ + \int_0^{Toff} \underline{v_L(t)}\Big|_{off} dt \end{array}\right] = 0 \quad (13)$$

$$\langle v_L(t)\rangle = \dfrac{T_{on}}{T_s}[V_{in} - \underline{x(t)}\Big|_{on}] + \dfrac{T_{off}}{T_s}\left[\begin{array}{c} V_{in} - \underline{x(t)}\Big|_{off} \\ - \underline{Vo(t)}\Big|_{off} \end{array}\right] \quad (14)$$

$$V_{in} - I\left[\begin{array}{c} R_{in} + R_l + \dfrac{Ton}{Ts}(R_{s,on}) \\ + \dfrac{Toff}{Ts}(R_{d1,on} + \dfrac{V_{d1,on}}{I}) \end{array}\right] - \dfrac{Toff}{Ts}\underline{Vo(t)}\Big|_{off} = 0 \quad (15)$$

To obtain the voltage conversion ratio, it is compulsory to eliminate I from equation (15). Hence, the applied Capacitor Charge Balance (CCB) methodology and the following equation are obtained:

$$\langle ic(t)\rangle = \dfrac{1}{Ts}\int_0^{Ts} ic(t)dt = \dfrac{1}{Ts}\left[\begin{array}{c} \int_0^{Ton} \underline{ic(t)}\Big|_{on} dt \\ + \int_0^{Toff} \underline{ic(t)}\Big|_{off} dt \end{array}\right] = 0 \quad (16)$$

$$\langle ic(t)\rangle = \dfrac{Ton}{Ts}\left(\dfrac{-V_o\big|_{on}}{R}\right) + \dfrac{Toff}{Ts}\left(I + \dfrac{-V_o\big|_{off}}{R}\right) = 0 \quad (17)$$

It is assumed that capacitor C_1 is large enough to reduce the voltage ripple at its load. Hence, $\dfrac{-V_o\big|_{on}}{R} = \dfrac{-V_o\big|_{off}}{R} = \dfrac{-V_o}{R}$, and the solution for equations (15) and (17) yields:

$$\dfrac{V_o}{V_{in}} = \dfrac{V_{1x}}{V_{in}} = \left[\dfrac{\dfrac{Ts}{Toff}\left[1 - \dfrac{Toff}{T}\dfrac{V_{d1,on}}{V_{in}}\right]R}{R + \left(\dfrac{Ts}{Toff}\right)^2\left(\begin{array}{c} R_{in} + R_l \\ + \left(\dfrac{Ton}{Ts}\right)R_{s,on}\end{array}\right) + \left(\dfrac{Ts}{Toff}\right)R_{d1,on}}\right] \quad (18)$$
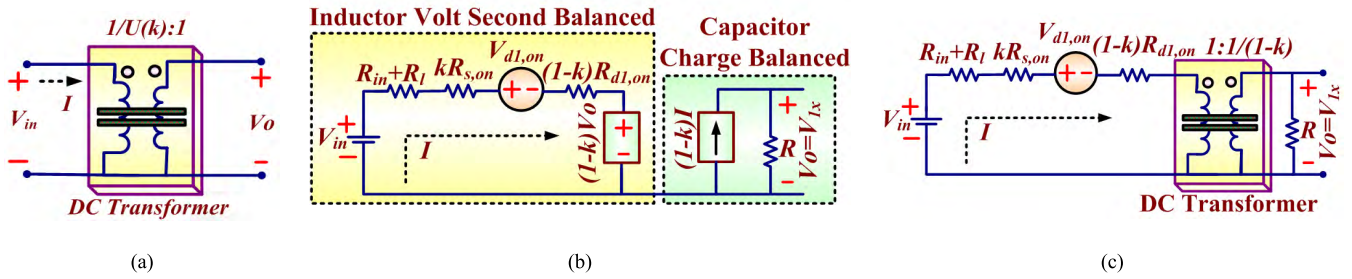
FIGURE 3. Equivalent circuitry and DC transformer modelling of DC-DC converter (a) Generalized two port DC transformer model, where U(k) is function of duty cycle (*k*), (b) Equivalent circuit for 1x MBC, where Inductor Volt Second Balanced (IVSB) methodology is used to design input port and capacitor charge Balanced (CCB) methodology is used to design output port, and (c) DC transformer model of 1x MBC, obtained by combined the input and output port by transformer. Note: In Transformer, solid lines are connected between primary and secondary which indicated transformer is allow to pass DC voltage current.
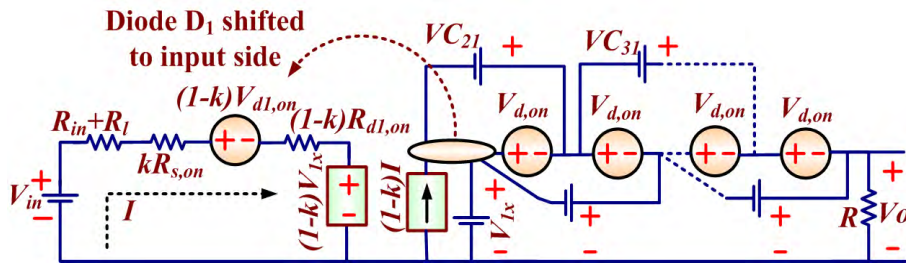

FIGURE 4. Equivalent circuitry of Nx MBC obtained by shifting diode D_1 to input side.
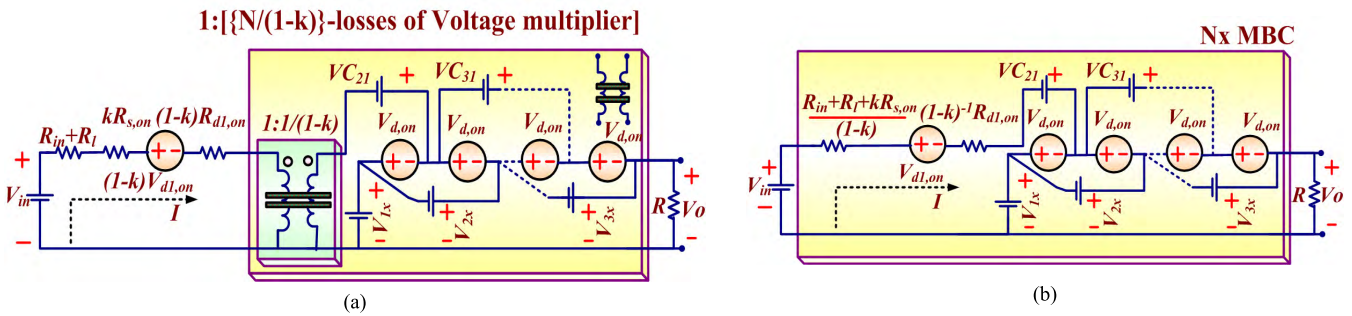

FIGURE 5. DC transformer modelling of Multilevel Boost Converter (a) Nx MBC, and (b) Nx MBC with all elements shifted to secondary side.

Now, let us consider Nx MBC configurations (Fig. 1(b)), where all the diode voltage drops are assumed to be the same and equal to $V_{d,on}$, and the voltage across the capacitors is known by (19) and (20), where ↑ denotes the charging of capacitor and ↓ denotes the discharging of capacitors.

$$
\left.\begin{array}{l}
V_{2x}\uparrow = V_{1x}\uparrow + V_{C21}\downarrow - 2V_{d,on} \\
V_{3x}\uparrow = V_{2x}\uparrow + V_{C31}\downarrow - 2V_{d,on} \\
V_{Nx}\uparrow = V_{(N-1)x}\uparrow + V_{CN1}\downarrow - 2V_{d,on}
\end{array}\right\} \ off\ state \quad (19)
$$

$$
\left.\begin{array}{l}
V_{C21}\uparrow = V_{1x}\downarrow - Vs - V_{d,on} \\
V_{C31}\uparrow = V_{2x}\downarrow - 2V_{d,on} \\
V_{CN1}\uparrow = V_{(N-1)x}\downarrow - 2V_{d,on}
\end{array}\right\} \ On\ state \quad (20)
$$

Using (19) and (20), the voltage across load *R* is given by (21) and (22), as shown at the bottom of the next page:

The generalized two port DC transformer model of an ideal single-stage DC-DC converter is shown in Fig. 3, where U(k)

is a function of T_{on}/T_S or *k* (duty cycle) and 1/U(k) is the converter voltage conversion ratio. 1/U(k) is the number of primary side winding, and single winding is considered at the secondary side (therefore, the turns ratio is 1/U(k):1). First, the DC transformer model is designed for 1x MBC, with the assumption that the capacitors are large enough to minimize voltage ripples. The equation of IVSB (15) and CCB (17) are used to construct the equivalent circuit for 1x MBC, and the equivalent circuit is shown in Fig. 3(b). In Fig. 3(c), the model is modified by employing the DC-Transformer at the place of dependent voltage and a current source, which gives ease to the analysis of the 1x MBC.

Similarly, equivalent circuitry is obtcained for Nx MBC by applying KVL on the voltage multiplier circuitry, and the results are shown in Fig. 4. In Fig. 5(a), the model is modified with the DC-Transformer, which also allows the
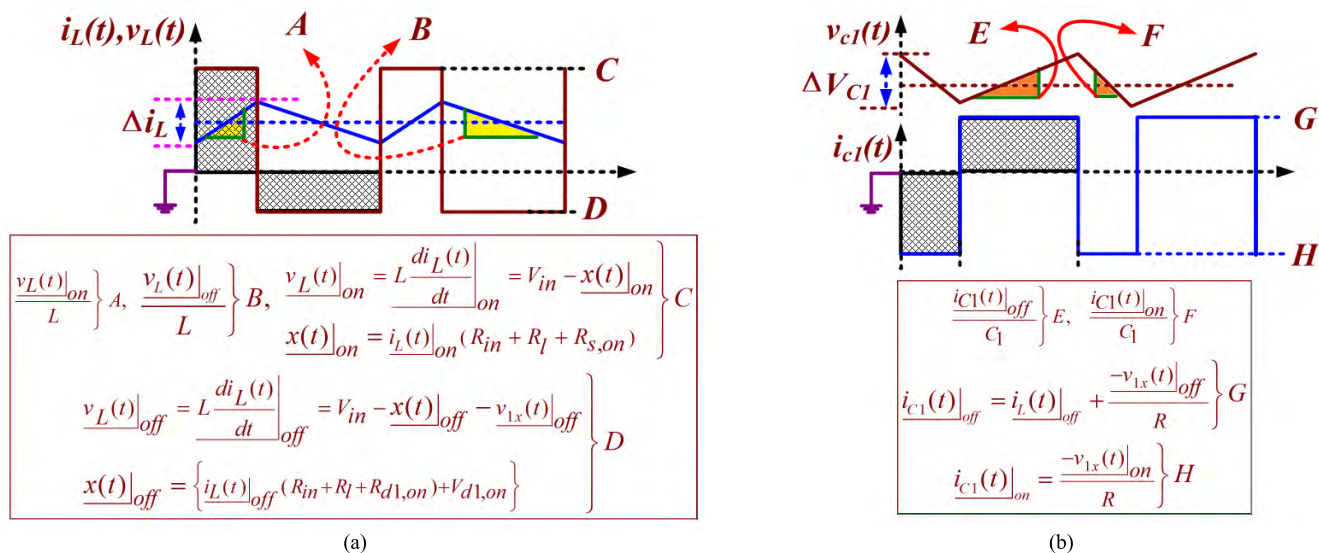
FIGURE 6. Characteristics waveform and its equation in CCM (a) Inductor current and voltage, (A: slope of inductor current in ON state, B: slope of inductor current in OFF state, C: voltage across inductor in ON state, D: voltage across inductor in OFF State), and (b) Capacitor C_1 current and voltage (E: slope of capacitor voltage in ON state, F: slope of capacitor voltage in ON state, G: current through capacitor C_1 in ON state, H: current through capacitor C_1 in OFF State).

relationship between input and output ports parameters to be easily obtained. The same equation (21) is derived by the DC transformer model of Nx MBC. Finally, all the primary side elements are transferred to the secondary side, and equivalent circuitry for Nx MBC is obtained and shown in Fig. 5(b). The characteristics of the current and the voltage waveform of the inductor and capacitor C_1 for 1x MBC is shown in Fig. 6, with a mathematical slope calculation. The relationship of the voltage conversion ratio, T_{on}/T_s and N is graphically shown in Fig. 7. Moreover, it is observed that a higher voltage conversion ratio can be obtained by adding more number of levels. A similar investigation has been done for negative voltage multilevel converter in [42]. However, as higher number of levels is added and the duty cycle is increased beyond 0.8, the voltage conversion ratio becomes non-linear due to internal resistance as shown in Fig. 7 and the quasi-operating region is reduced. It is also noteworthy that for a very high number of levels, the voltage conversion ratio plot becomes non-linear above 0.8. Thus, to operate

Nx MBC the best operating point is near 0.5 to 0.7 duty ratio.

B. DISCONTINUOUS CONDUCTION MODE (DCM) OF Nx MBC

The converter generally functioned in DCM mode when a large inductor current ripple (enough to reach zero) and the voltage ripple of the capacitors was present. The stipulations for DCM and CCM are:

$$\text{DCM} \left\{ I_L < \Delta \left. i_L(t) \right|_{on} \text{ or } \Delta \left. i_L(t) \right|_{off} \right. \tag{23}$$

$$\text{CCM} \left\{ I_L > \Delta \left. i_L(t) \right|_{on} \text{ or } \Delta \left. i_L(t) \right|_{off} \right. \tag{24}$$

For simplicity, assume that all the components are ideal and that all the capacitors are equal in rating. Thus, the output voltage is obtained by:

$$V_o = V_{Nx} = NV_{1x} = \frac{NT}{T_{off}} V_{in} \Bigg\} \tag{25}$$

$$V_o = V_{Nx} = NV_{1x} - Vs - 4(N - 1.25)V_{d,on}$$
$$= \left[\frac{\frac{T_s}{T_{off}} \left[1 - \frac{T_{off} V_{d1,on}}{V_{in} T} \right] RV_{in} - \left(\begin{array}{c} Vs \\ +4(N-1.25)V_{d,on} \end{array} \right) \alpha}{\alpha} \right] \Bigg\} \tag{21}$$

$$\textit{1x Level Voltage reduction factor}, \xi = \left(1 - \frac{V_{d,on}}{V_{in}} \right) \left(\frac{V_{in} R}{\alpha} \right) \Bigg\}$$

$$\alpha = R + \left(\frac{Ts}{T_{off}} \right)^2 \left(\begin{array}{c} R_{in} + R_l \\ + \left(\frac{Ton}{Ts} \right) R_{s,on} \end{array} \right) + \left(\frac{TR_{d1,on}}{T_{off}} \right) \Bigg\} \tag{22}$$
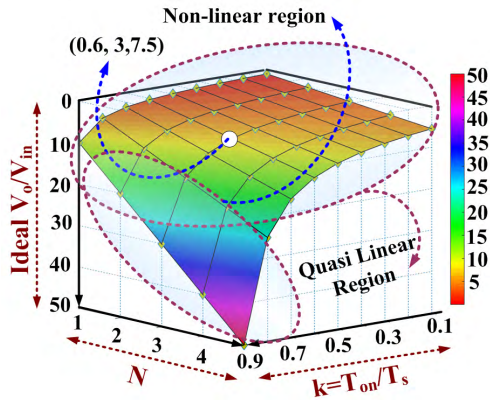
FIGURE 7. Relationship of the voltage conversion ratio, T_{on}/T_s and N for Nx MBC.

FIGURE 8. Boundary of CCM and DCM for various levels (1 to 5).

In the OFF state, it is observed that the DC component of the input current is equal to the load current.

$$(1-k)I_L = \frac{Vo}{R} \Rightarrow I_L = \frac{NT_s^2 V_{in}}{T_{off}^2 R} \Biggr\} \quad (26)$$

For DCM mode,

$$I_L = \frac{NT_s^2 V_{in}}{T_{off}^2 R} < \frac{V_{in}T_{on}}{L}$$
$$\frac{L}{R} < \frac{T_{off}^2 T_{on}}{NT_s^2} \, or \, \frac{L}{TsR} < \frac{k(1-k)^2}{N} \Biggr\} \quad (27)$$
$$\chi < \chi_{critical}(k); \, where, \, \chi = \frac{L}{TsR}$$

The dependency of $\chi_{critical}(k)$ with k is shown in Fig. 8, and it is observed that the value of $\chi_{critical}(k)$ decreases as the number of levels increases, and the maximum value of $\chi_{critical}(k)$ is *4/27N* for the Nth level. As a result, the converter operates in DCM mode when $\chi < 4/27N$ at $k = 33.33\%$.

The characteristic waveform of the inductor and the capacitor of Nx MBC for DCM are shown in Fig. 9(a)-(b), respectively. Let us assume that the inductor current reaches zero at Z, the equivalent circuitry for the ON, OFF and DCM states is shown in Fig. 10(a)-(c), respectively, and the equivalent capacitance (C_{ON}, C_{OFF}, and C_Z) is calculated as:

$$C_{ON}^{-1} = \begin{pmatrix} (C_1+C_{21})^{-1} \\ +(C_{22}+C_{31})^{-1} \\ +(C_{(N-1)1}+C_{N1})^{-1} \end{pmatrix} \Rightarrow C_{ON} = \frac{C}{2N-2} \Biggr\} \quad (28)$$

$$C_{OFF}^{-1} = \begin{pmatrix} (C_{22}+C_{21})^{-1} \\ +(C_{32}+C_{31})^{-1} \\ +....(C_{N1}+C_{N2})^{-1} \end{pmatrix} \Rightarrow C_{OFF} = \frac{C}{2N-2} \Biggr\} \quad (29)$$

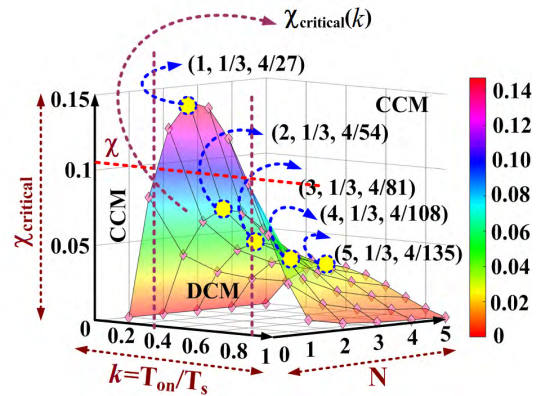$$C_Z^{-1} = C_{22}^{-1} + ...C_{N2}^{-1} \Rightarrow C_Z = \frac{C}{N-1} \Biggr\} \quad (30)$$

When MOSFET is turned ON ($0 < t < kT_s$), the inductor voltage and capacitor current are given by:

$$v_L(t)\Big|_{on} = L\frac{di_L(t)}{dt}\Big|_{on} \Rightarrow v_L(t) = V_{in}$$
$$i_c(t)\Big|_{on} \approx \frac{-V_o\big|_{on}}{R} \Rightarrow i_c(t) = \frac{-V_o}{R} \Biggr\} \quad (31)$$

When MOSFET is turned OFF ($kT_s < t < Z$), the inductor voltage and capacitor current are given by:

$$v_L(t)\Big|_{off} = V_{in} - \frac{v_o(t)\big|_{off}}{N} \Rightarrow v_L(t) = V_{in} - \frac{V_o}{N}$$
$$i_c(t)\Big|_{off} \approx I + \frac{-V_o\big|_{on}}{R} \Rightarrow i_c(t) \approx I + \frac{-V_o}{R} \Biggr\} \quad (32)$$

When the inductor current is zero, the converter operates in DCM mode ($Z < t < T_s$), and:

$$v_L(t)\Big|_{DCM} = 0 \Rightarrow v_L(t) = 0$$
$$i_c(t)\Big|_{DCM} = \frac{-V_o\big|_{DCM}}{R} \Rightarrow i_c(t) \approx \frac{-V_o}{R} \Biggr\} \quad (33)$$

By using IVSB and CCB methodology, the following equations are derived:

$$\langle v_L(t)\rangle = 0 \Rightarrow \begin{pmatrix} kV_{in} + (Z-k)\left(V_{in} - \frac{V_o}{N}\right) \\ +(1-Z)0 \end{pmatrix} = 0$$
$$\therefore V_o = \frac{NZV_{in}}{Z-k} \Rightarrow Z = \frac{kV_o}{V_o - NV_{in}} \Biggr\} \quad (34)$$

To calculate the voltage conversion ratio, consider an imaginary diode D, as shown in Fig. 10(b). It is observed that diode D is forward biased only when $kT_s < t < Z$, and, in this period, the current through the inductor and the diode is the same, which is also equal to the DC components of the load current.

$$I_{L \, max} = \frac{V_{in}kT_s}{L}, \, Z-k = \frac{kNV_{in}}{Vo - V_{in}} \Biggr\} \quad (35)$$

$$\langle I_D\rangle = \frac{1}{2}\frac{V_{in}kT_s}{L}(Z-k) = \frac{Vo}{R} \Biggr\} \quad (36)$$
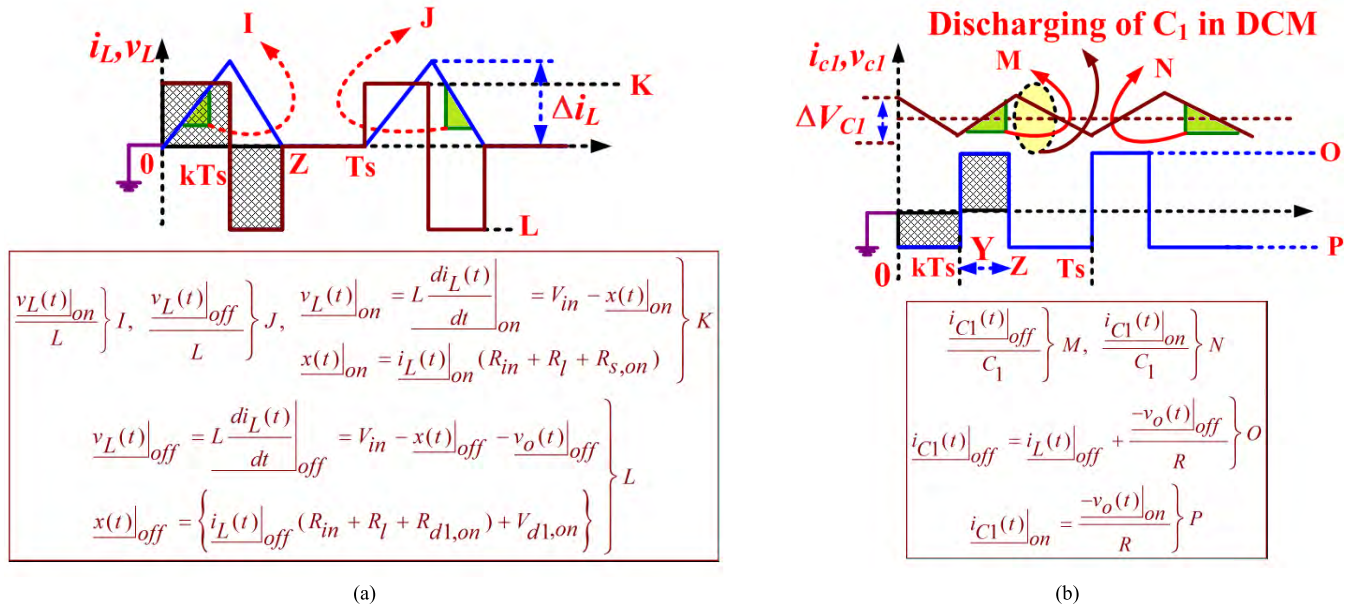
FIGURE 9. Characteristics waveform and its equation in DCM (a) Inductor current and voltage, (I: slope of inductor current in ON state, J: slope of inductor current in OFF state, K: voltage across inductor in ON state, L: voltage across inductor in OFF State), and (b) Capacitor C_1 current and voltage (M: slope of capacitor voltage in ON state, N: slope of capacitor voltage in ON state, O: current through capacitor C_1 in ON state, P: current through capacitor C_1 in OFF State).
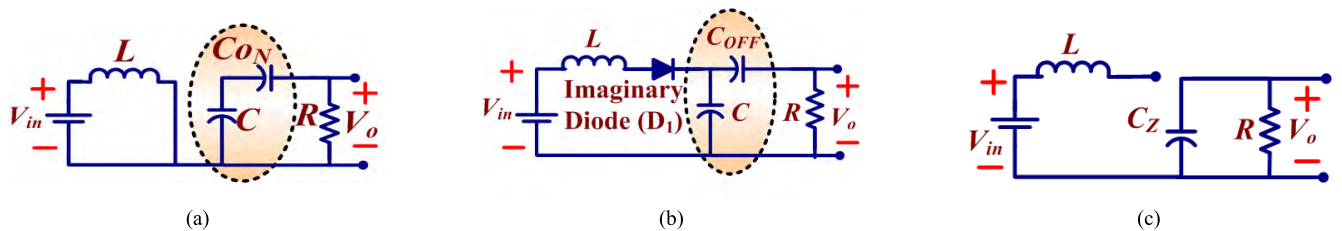

FIGURE 10. Equivalent circuit of Nx MBC in DCM (a) When switch is turned ON (b) When switch is turned OFF, and (c) When switch is turned OFF and inductor current reached to Zero.

Using (35) and (36), the following quadratic equation is obtained:

$$V_o^2 - V_o V_{in} - \frac{NV_{in}^2 k^2}{2\chi} = 0 \Bigg\} \qquad (37)$$

The solution of (37) yields two roots, but the output of the boost converter is positive. Hence, the positive root is selected, and the following equation is obtained, where $\chi = L/RT_s$.

$$\frac{V_o}{V_{in}} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2Nk^2}{\chi}}\right) \qquad (38)$$

Equation (38) provides the voltage conversion ratio of Nx MBC. It is observed that the output voltage turns into load dependence, which provides an increase in the converter output impedance.

C. COMPARISON OF Nx MBC WITH THE EXISTING CONVERTER

Recently, based on the arrangement of reactive elements and semiconductor devices, numerous converters are proposed for low to high voltage conversion ratio applications. For comparison purposes, many converter configurations are reviewed, and the best configurations are selected, which are derived from the conventional boost converter [11], [13], [17]. In Fig. 11 and Fig. 12, Nx MBC is compared with other existing converter configurations in terms of the voltage conversion ratio and V_S/V_o, respectively. First, it is determined that the Nx MBC generates a higher voltage conversion ratio with minimum V_S/V_o. It is also determined that for Nx MBC, V_S/V_o is constant at all duty cycles and the ratio decreases as the number of levels increases. Second, it is also shown that quasi-linear or operating region is reduced as the number of levels and duty cycle is increased; because voltage conversion ratio becomes non-linear due to inductor series resistance at a higher duty cycle (above 0.8) and levels.

TABLE 1. Comparison of the DC-DC converters in terms of the number of components and the behavior of the current.

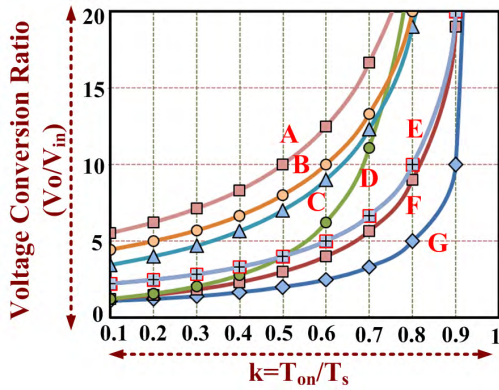| Converter Type	Number of inductors	Number of capacitors	Number of control switches	Number of diodes	Behavior of Input current
Conventional Boost	1	1	1	1	Continuous
Switched Inductor (SI) DC-DC Boost	2	1	1	4	Continuous
Traditional Three Level DC-DC Boost	1	2	2	2	Continuous
Quadratic Three Level DC-DC Boost	2	2	2	2	Continuous
Single switch DC-DC Quadratic Boost	2	2	1	3	Continuous
DC-DC Converter using bootstrap capacitors and boost Inductors	2	3	3	4	Continuous
Switched Capacitor Based DC-DC Boost	2	2	1	2	Continuous
2x MBC	1	3	1	3	Continuous
3x MBC	1	5	1	5	Continuous
Nx MBC	1	2N-1	1	2N-1	Continuous

FIGURE 11. Comparison of Nx MBC with the recently proposed converter. Note: A: 5x MBC, B: 4x MBC, C: 3x MBC and DC-DC Converter using bootstrap capacitors and boost Inductors, D: 2x MBC and traditional three level DC-DC boost converter, E: Quadratic three level DC-DC boost converter and single switch DC-DC Quadratic Boost Converter (QBC), F: Switched Inductor (SI) DC-DC boost converter, Switched Capacitor Based DC-DC boost converter and G: conventional boost converter.
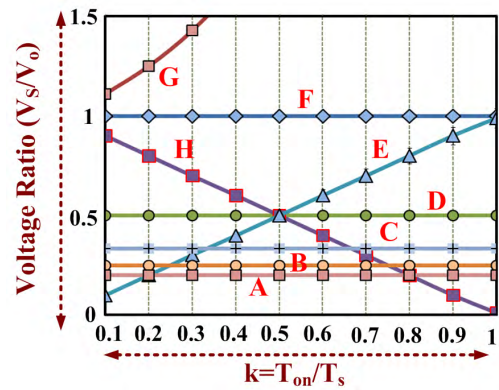

FIGURE 12. Comparison of Nx MBC with the recently proposed converter in terms of switch voltage stress. Note: A: 5x MBC, B:4x MBC, C: 3x MBC, D: 2x MBC and traditional three level DC-DC boost converter, E: Quadratic three level DC-DC boost converter (First Switch), F: Single switch DC-DC Quadratic Boost Converter (QBC), DC-DC converter using bootstrap capacitors and boost Inductors, Switched Inductor (SI) DC-DC boost converter and conventional boost converter G: Switched Capacitor based DC-DC boost converter and H: Quadratic three level DC-DC boost converter (second switch)

In Table 1, the Nx MBC converter is compared with existing converters in terms of a number of switches, inductors, capacitor, diodes and the behaviour of the input current.

D. RATING OF INDUCTOR, CAPACITORS, DIODES, AND MOSFET

The inductor value is selected by using the slope of the inductor current waveform, such that the assumed ripple in the inductor current (Δi_L) is obtained. The critical inductance is given by:

$$L_{critical} = \frac{V_{in} - x(t)\big|_{on}}{\Delta i_L} T_{on} = k \frac{V_{in} - x(t)\big|_{on}}{f_s \Delta i_L}$$
$$= \left(\frac{V_{in} - i_{in}(t)\big|_{on} (R_{in} + R_l + R_{s,on})}{\Delta i_L} T_{on} \right) \quad (39)$$

It is noted that if the effect of the diode is ignored during the charging and discharging of the capacitor, then the voltage across each capacitor is nearly the same. Due to the advantage of the voltage multiplier, it is possible to select all the capacitors with an equal rating. The capacitor's value is selected by using the slope of the capacitor voltage waveform; such that the assumed ripple in capacitor voltage is
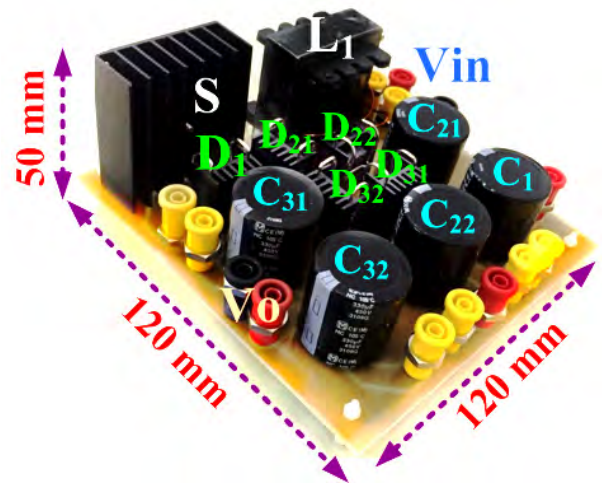

FIGURE 13. Hardware prototype of 3x MBC (Tested at power 100 W).

obtained. The voltage rating of each capacitor must be higher than (*1/N*) times the output voltage. The current rating of the inductor must be higher than the input current of the
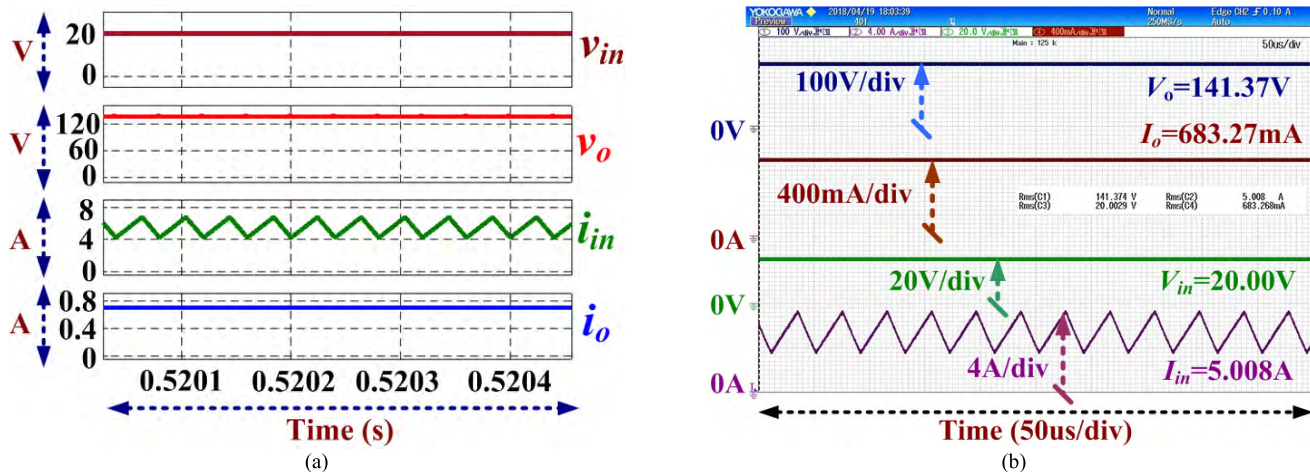
FIGURE 14. Output voltage, input voltage, output current and input current at duty cycle 60% (a) Simulation results [V_{in} = 20 V, V_o = 141.9 V, I_o = 0.69 A, I_{in} = 5.03 A] and (b) Experimental results [V_{in} = 20 V, V_o = 141.37 V, I_o = 683.27 mA, I_{in} = 5.008 A].

converter.

$$C_{critical} = \frac{V_{1x}}{R \Delta v_C} T_{on} = k \frac{V_o}{NRf_s \Delta v_C} \Bigg\} \quad (40)$$

$$i_L(t) > i_{in}(t), V_C > \frac{V_o}{N} = \frac{T_S}{T_S - T_{on}} \Bigg\} \quad (41)$$

It is also noted that if we consider that all the capacitors are charged equally, then the voltage across each diode is the same and equal to ($1/N$) times the output voltage. Thus, the voltage rating of the diode must be higher than ($1/N$) times the output voltage, and the current rating of the diode must be higher than the input current since the input current is flowing through the diode when MOSFET is turned OFF.

$$i_D(t) > i_{in}(t), V_D > \frac{V_o}{N} = \frac{T_S}{T_S - T_{on}} \Bigg\} \quad (42)$$

The drain to the source voltage of MOSFET is equal to ($1/N$) times V_o. During the ON state condition, the entire input current plus the capacitor clamping current flow through the MOSFET. Thus, for MOSFET, the voltage rating must be higher than V_o/N, and the current rating is higher than the input current plus clamping current.

$$\left. \begin{array}{l} i_S(t) > i_{in}(t) + C\text{apacitor clamping current} \\ i_S(t) \gg i_{in}(t), V_{DS} > \dfrac{V_o}{N} = \dfrac{T_S}{T_S - T_{on}} \end{array} \right\} \quad (43)$$

III. NUMERICAL SIMULATION, EXPERIMENTAL RESULTS, AND DISCUSSION

In this section, the numerical simulation and experimental results of 3x MBC in CCM, as well as in DCM, are discussed in detail. To analyze the Nx MBC, simulation and hardware prototype of 3X MBC is implemented and tested with 100 W power, 20 V input supply, 140 V output voltage, and 25 kHz switching frequency. The critical value of the reactive components and the semiconductor devices are calculated based on the equation discussed in section II, and the larger values are selected. A single ferrite core inductor (300 μH, 10A) and

five electrolyte capacitors (330 μF, 450 V) are used to design the 3x MBC and voltage, as well as the current regulation that is investigated at various duty cycles. FPGA Virtex-5 XC5VLX50T^{TM} is used to generate the control PWM for the single N-channel MOSFET (C2M01601200), and five diodes (STTH6012W) are used with a flat-back heat sink to control the power flow in the 3-level voltage multiplier circuit. The hardware prototype of 3x MBC is shown in Fig. 13, with dimensions of (l = 12 cm, b = 12 cm and h = 5 cm). The prototype is tested several times at various duty cycles and always observes consistent results in CCM and DCM.

A. INVESTIGATION OF 3x MBC IN CCM

To investigate the 3x MBC in CCM, the converter is operated at various duty cycles. Fig. 14(a) shows the simulation waveform of the output voltage and current (V_o, I_o), and the input voltage and current (V_{in}, I_{in}) at 60% duty cycle. First, it is determined that V_o = 141.9 V and I_o = 0.69 A is obtained from 20 V input supply with input current 5.03 A. Second, it is determined that the input current increases and decreases when the switch is turned ON and OFF, respectively, and a 2.97 A ripple is observed in the input current. The experimentally obtained waveform of the output voltage, current (V_o, I_o) and the input voltage, current (V_{in}, I_{in}) at 60% duty cycle, is shown in Fig. 14(b). The observed values are V_o = 141.37 V, I_o = 683.27 mA, V_{in} = 20 V, and I_{in} = 5.008 A, which are closely matched with the obtained simulation values.

Fig. 15(a) shows the simulation obtained waveform of level 3, level 2, inductor current (I_L) and the voltage across switch (V_S) at 60% duty cycle. First, it is determined that the inductor is charged and discharged with an average current of 5.028A when the switch is ON and OFF, respectively. The voltage at level 2 is 96.14 V and at level 3 is 141.9 V, The voltage across the switch in the OFF state is $V_{DS}(t)\big|_{off}$ or $V_S(t)\big|_{off}$ = 49.3 V, which is also approximately equal to the level 1 voltage. The experimentally
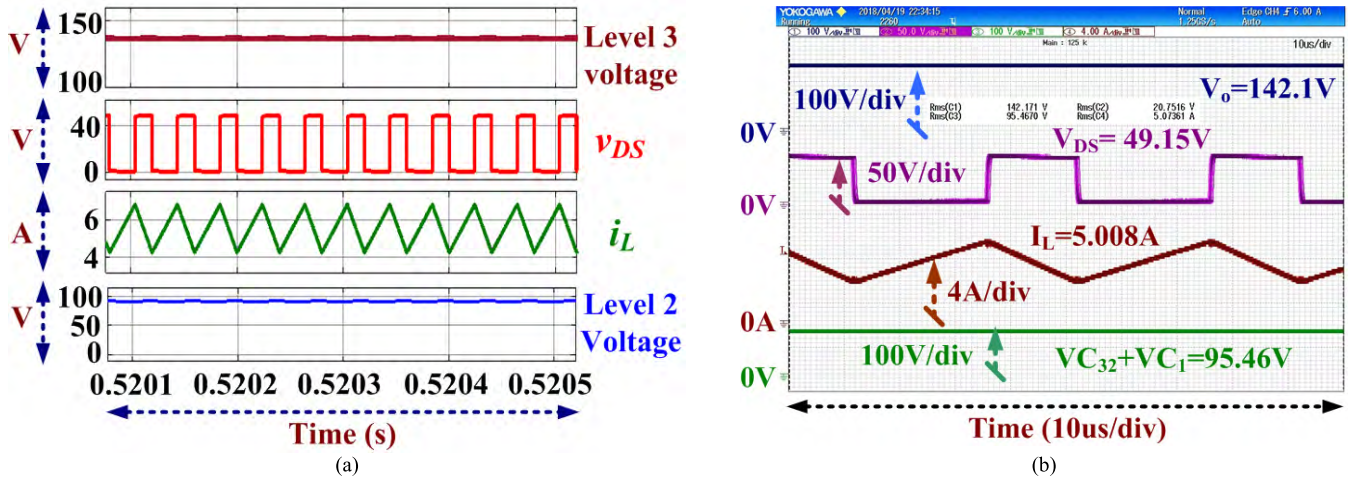
FIGURE 15. Voltage at level 3 and 2, inductor voltage, inductor current at duty cycle 60% (a) Simulation results [Level 3 voltage = V_O = 141.9 V, Level 2 voltage = $VC_{32} + VC_1$ = 96.14 V, V_{DS} = 49.3 V in OFF state, I_L = 5.028 A], and (b) Experimental results [V_o = 142.1 V, $VC_{32} + VC_1$ = 95.46 V, V_{DS} = 49.15 V in OFF state, I_L = 5.0008 A].
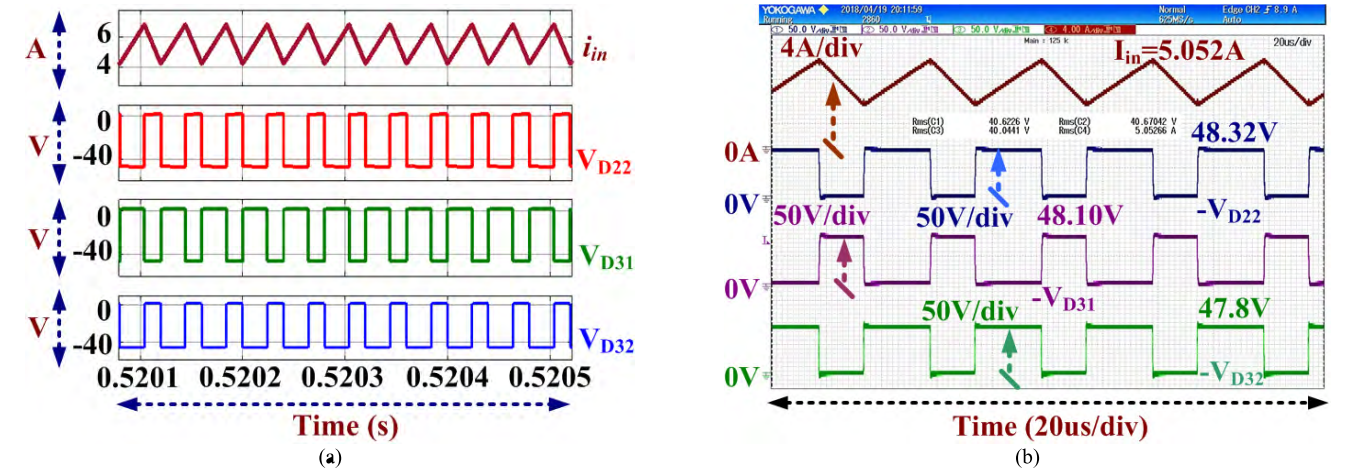

FIGURE 16. Inductor current, Diodes D_{22}, D_{31}, and D_{32} voltage at duty cycle 60% (a) Simulation results [$VD_{22} = -48.67$ V, $VD_{31} = -48.62$ V, $VD_{32} = -48.34$ V, and I_L = 5.0008 A], and (b) Experimental results [$VD_{22} = -48.32$ V, $VD_{31} = -47.10$ V, $VD_{32} = -47.8$ V, and I_L = 5.0008 A].

obtained waveforms of level 3, level 2, inductor current (I_L) and the voltage across switch (V_S) at 60% duty cycle is shown in Fig. 15(b). The voltage at level 2 is 95.46 V and at level 3 is 142.1 V, and the voltage across the switch in the OFF state is $V_S(t)\big|_{off} = 49.15$ V.

The simulation obtained waveform of the voltage across diodes D_{22}, D_{31}, and D_{32} with the inductor current (I_L) at 60% duty cycle is shown in Fig. 16(a). First, it is observed that diodes D_{22} and D_{32} are forward biased when the switch is OFF to provide a path to discharge the inductor, whereas D_{31} is forward biased when the switch is ON. Second, the Peak Inverse Voltage (PIV) of diodes D_{22}, D_{31}, and D_{32} are -48.67 V, -48.62 V and -48.34 V, respectively.

Fig. 16(b) shows the experimentally obtained waveform of the voltage stress of diodes D_{22}, D_{31}, and D_{32} with the inductor current (I_L) at 60% duty cycle. The experimentally observed Peak Inverse Voltage (PIV) of diodes D_{22}, D_{31},

and D_{32} is -48.32 V, -48.10 V and -47.8 V, respectively (Note: voltage are observed with reversed probe polarity)

To investigate the regulation of 3x MBC, the converter is regulated from a 60% to 40% duty cycle, and Fig. 17(a) shows the simulation obtained waveform of the output voltage (V_o), inductor voltage (V_L) and current (I_L) with zoom. First, it is determined that the values of V_o, V_L, and I_L decrease as the duty cycle decreases, which is expected in the boost converter. The obtained values at the 60% duty cycle are V_o = 141.7 V, $V_L(t)\big|_{on} = 20$ V, $V_L(t)\big|_{off} = -29.1$ V and I_L = 5.03 A.

The obtained values at the 40% duty cycle are V_o = 94.4 V, $V_L(t)\big|_{on} = 20$ V, $V_L(t)\big|_{off} = -13.7$ V and I_L = 2.07 A. The experimentally obtained waveforms of output voltage (V_o), inductor voltage (V_L) and current (I_L) with zoom are shown in Fig. 17(b). The observed values at the 60% duty cycle are V_o = 141.41 V, $V_L(t)\big|_{on} = 20$ V, $V_L(t)\big|_{off} = -28.9$ V and I_L = 5.067A. The obtained values at the 40%
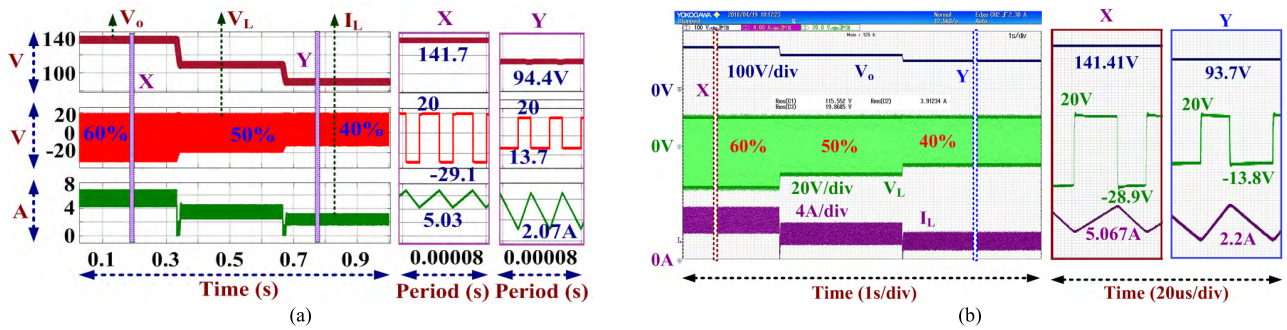
FIGURE 17. Regulation of output voltage, inductor voltage, inductor current from duty cycle 60% to 40% (a) Simulation results, and (b) Experimental results.
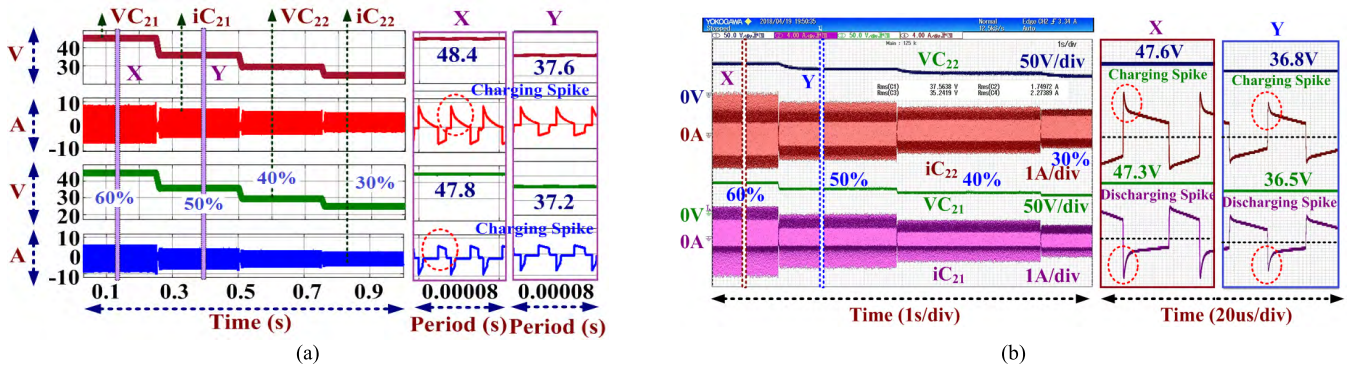

FIGURE 18. Voltage and current regulation of capacitor C_{21} and C_{22} from duty cycle 60% to 30% (a) Simulation results, and (b) Experimental results.

duty cycle are $V_o = 93.7$ V, $V_L(t)\big|_{on} = 20$ V, $V_L(t)\big|_{off} = -13.8$ V and $I_L = 2.2$ A.

To investigate the voltage and current regulation in capacitors, the converter is regulated from a 60% to 30% duty cycle, and Fig. 18(a) shows the simulation obtained waveforms of capacitor C_{21} voltage (V_{C21}), current (I_{C21}) and capacitor C_{22} voltage (V_{C22}), current (I_{C22}) with zoom for 60% and 40%. First, it is observed that the capacitor voltage and current decrease as the duty cycle decreases. At the 60% duty cycle, the observed capacitor voltage values are $V_{C21} = 48.4$ V and $V_{C22} = 47.8$ V, and at the 50% duty cycle, the observed capacitor voltage values are $V_{C21} = 37.6$ V and $V_{C22} = 37.2$ V. Fig. 18(b) shows the experimentally obtained waveforms of capacitor C_{21} voltage (V_{C21}), current (I_{C21}) and capacitor C_{22} voltage (V_{C22}), current (I_{C22}) with zoom for 60% and 50%. At the 60% duty cycle, the experimentally observed capacitor voltage values are $V_{C21} = 47.6$ V and $V_{C22} = 47.3$ V, and, at 50% duty cycle, the observed capacitor voltage values are $V_{C21} = 36.8$ V and $V_{C22} = 36.5$ V. In both cases, simulation and experimentally, it is observed that capacitor C_{21} is charged and discharged when the switch is ON and OFF, respectively, whereas capacitor C_{22} is charged and discharged when the switch is turned OFF and ON, respectively. High charging current spikes (shown in Fig. 18(b)) are observed in capacitors C_{21} and C_{22} current when the switch is turned ON and OFF, respectively.

To investigate the voltage and current regulation in capacitor C_{32}, the converter is regulated from a 60% to 30% duty cycle. Fig. 19(a) shows the simulation obtained waveforms of capacitor C_{32} voltage (V_{C32}) and current (I_{C32}), along with input current (I_{in}) and output voltage (V_o), with zoom for 60% and 30%. First, it is observed that the capacitor C_{32} voltage and current decrease as the duty cycle decreases. At 60% and 30% duty cycles, the observed capacitor voltages are $V_{C21} = 47.7$ V and $V_{C21} = 27.9$ V, which is approximately 1/3rd of the total output voltage (1/3rd of 142.4 at 60% and 83.4 V at 30%). At 60% and 30% duty cycles, 5.06 A and 910 mA input currents are observed, respectively. Fig. 19(b) shows the experimentally obtained waveforms of capacitor C_{32} voltage (V_{C32}) and current (I_{C32}), along with input current (I_{in}) and output voltage (V_o), with zoom for 60% and 30%. The experimentally observed capacitor voltage V_{C21} at 60% and 30% is 47.31 V (approx. 1/3 of 141.2 V) and 27.48 V (approx. 1/3 of 82.2 V), respectively. Experimentally, 5.03 A and 840 mA input currents are observed at 60% and 30% respectively. In both cases, simulation and experimentally, charging and discharging of the current spike is also observed when the switch is turned OFF.

In all cases of CCM, the experimentally observed results are closely matched with the simulation results, which validate the design and the performance of Nx MBC in CCM.
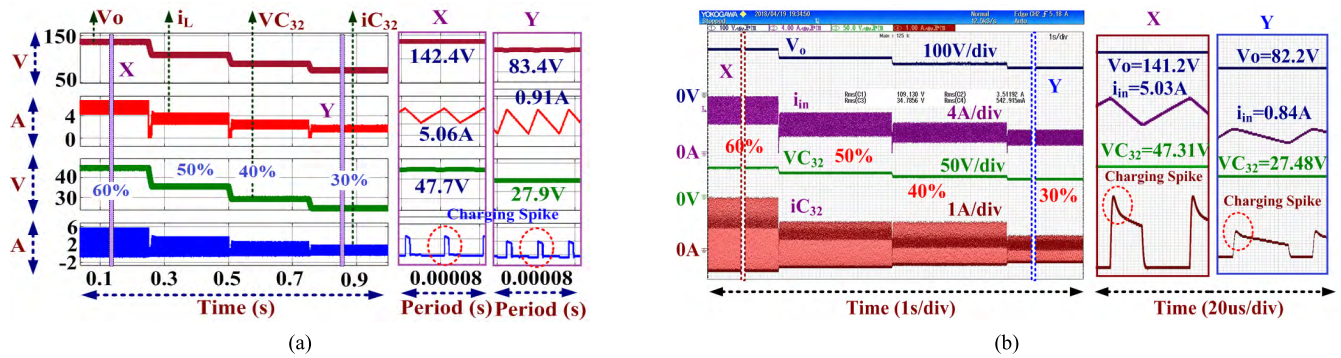
FIGURE 19. Voltage and current regulation of capacitor C_{32}, output voltage and input current from duty cycle 60% to 30%. (a) Simulation results, and (b) Experimental results.
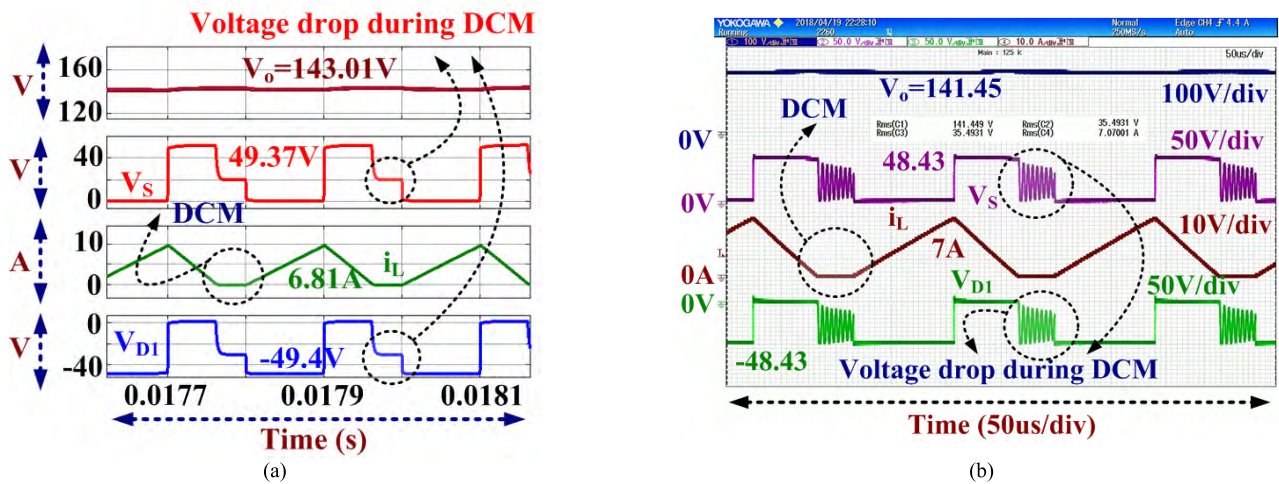

FIGURE 20. DCM output voltage, voltage across switch, inductor current, voltage across diode D_1 at duty cycle 50%. (a) Simulation results, and (b) Experimental results.

B. INVESTIGATION OF 3x MBC IN DCM MODE

To investigate the 3x MBC in DCM, the converter is operated at 60% and 50% duty cycles, with a lower frequency of 5 kHz. Fig. 20(a) shows the simulation obtained waveforms of the output voltage (V_o), the voltage across switch (V_s), inductor current (I_L) and the voltage across the diode (V_{D1}) at 50% duty cycle. At 50% duty cycle, first, it is observed that the output voltage is 143.01 V, the maximum voltage across the switch is 49.37, and the PIV of diode D1 is -49.4 V. Second, it is observed that there is an equal voltage drop in the switch and diode voltage when the inductor current reaches zero. At 50% duty cycle, the observed value of the inductor current is 6.81 A. The experimentally obtained waveforms of the output voltage (V_o), voltage across switch (V_s), inductor current (I_L) and voltage across the diode (V_{D1}) at 50% duty cycle is shown in Fig. 20(b). Experimentally observed values are 141.45 V for the output voltage, -48.43 V for the voltage across the diode, 7 A for the inductor current, and 47.43 V for the voltage across the switch. The voltage across the switch and diode decreases and voltage ringing are observed when the inductor current reaches zero. From the simulation and

experimental results, it is clearly observed that the inductor current starts from zero and reaches a maximum value when the switch is turned ON. When the switch is turned OFF, the inductor discharges and its current starts decreasing and finally reaches zero during the OFF state, which confirms the DCM operation.

The 3x MBC is operated at 60% in DCM to investigate the regulation in the output voltage. Fig. 21(a) shows the simulation obtained waveforms of the output voltage (V_o), the voltage across switch (V_S), inductor current (I_L) and the voltage at the second level. At 60% duty cycle, first, it is observed that the output voltage is 162.3 V, the maximum voltage across the switch is 60.32 V, the voltage at the second level is 109.47 V, and the inductor current is 8.9 A. Second, the voltage across the switch decreases when the inductor current is zero. Experimentally obtained waveforms of the output voltage (V_o), voltage across switch (V_S), inductor current (I_L) and the voltage at the second level are shown in Fig. 21(b). The experimentally obtained values are 160.95 V for the output voltage, 59.71 V for the maximum voltage across the switch, 108.95 V for the voltage at the second level,
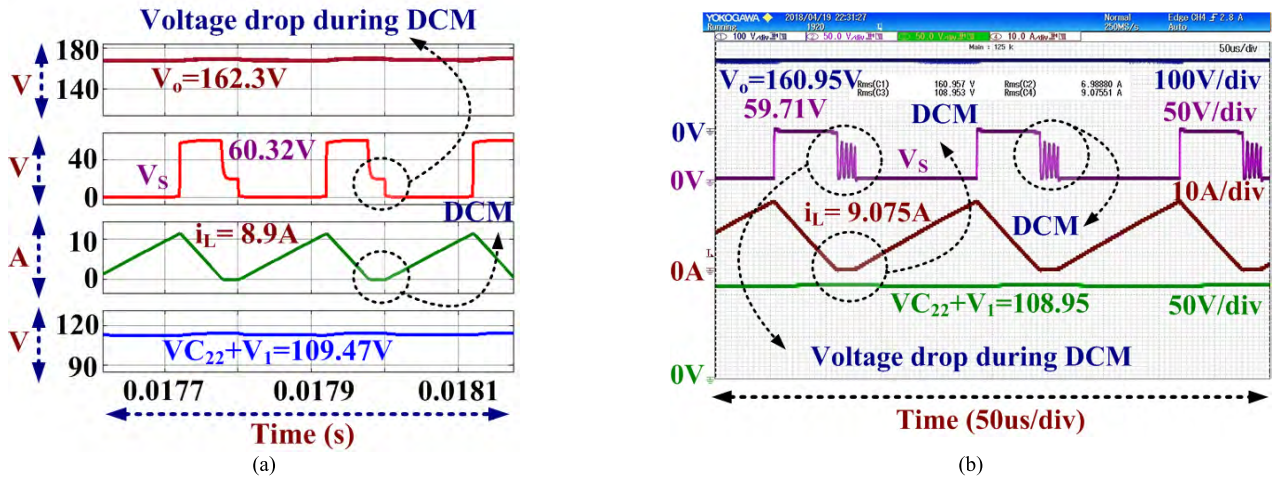
FIGURE 21. DCM output voltage, voltage across switch, inductor current, voltage at level 2 at duty cycle 60%. (a) Simulation results, and (b) Experimental results.
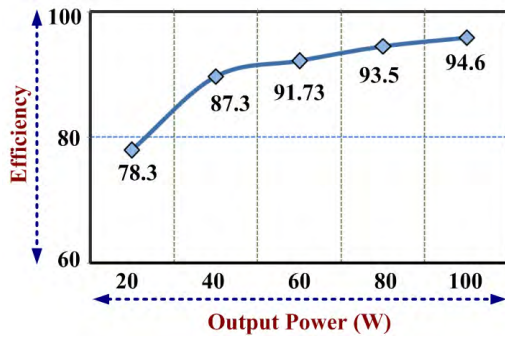

FIGURE 22. Plot of efficiency versus power.

and 9.075 A for the inductor current. The voltage across the switch decreases and voltage ringing are observed when the inductor current is zero. In all cases of DCM, the experimentally observed results are closely matched with the simulation results, which validate the design and the performance of Nx MBC in DCM.

C. EFFICIENCY

The efficiency is plotted versus power and is shown in Fig. 22. It is noted that 94.6% efficiency is observed at power 100 W. The efficiency decreases when the power of the converter decreases and an average of 89.9% efficiency is observed.

IV. CONCLUSION

The paper has presented the DC modeling of the non-isolated and non-inverting Nx MBC, considering internal resistance and semiconductor losses, which has provided ease in analysing the Nx MBC and other multilevel converters for the future direction of low to high voltage conversion. Continuous input current, single switch, single inductor, stack of the capacitors at the output side, self-balanced structure, low voltage rating reactive components and semiconductors, and transformer-less structure have been the main advantages

of the Nx MBC. Detailed analysis of Nx MBC in CCM and DCM has been provided, and the boundary of CCM and DCM has also been discussed. The voltage conversion ratio in CCM and DCM has been derived with considering the losses of the input voltage, inductor and semiconductor devices. It has been noteworthy that the CCM and DCM boundary of the converter is dependent on the load, inductor, a number of stages, switching period, and duty cycle. The voltage conversion ratio has been nonlinear at a higher number of levels and duty cycle (above 0.8). Hence, there has been a reduction in the operating region when the converter has been designed for a higher number of levels and high duty cycle. To show the benefit of Nx MBC, a comparison has been provided with a recently proposed converter in terms of the voltage conversion, voltage across the switch and number of components. The selection of reactive components and semiconductor devices has been discussed in detail, and the prototype has been designed and implemented for three levels and tested at power 100 W. Nevertheless, the circuitry of Nx MBC can be easily extended to obtain a high conversion ratio by adding a repeating structure of diodes and capacitors on the output side of the converter. To verify the performance of 3x MBC, simulation and experimental investigations have been discussed in detail for CCM and DCM. The performance of the converter has been tested by regulating the converter at the various duty cycles and an efficiency of 94.6% has been observed at 100 W for the three levels MBC. The simulation and experimental results have shown good conformity with the mathematical analysis. Based on the investigation, it is noteworthy that the Nx MBC has provided a solution to achieve higher voltage conversion ratio and highly suitable to feed multilevel inverters due to its functionality and stack of capacitor structure at the output side.

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