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Baker, Nick; Iannuzzo, Francesco; Li, Helong

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Impact of Kelvin-Source Resistors on Current Sharing and Failure Detection in Multichip Power Modules

Nick Baker, Francesco Iannuzzo
Aalborg University
Aalborg, Denmark
nba@et.aau.dk, fia@et.aau.dk

Helong Li
Dynex Semiconductor
Lincoln, United Kingdom
Helong.Li@dynexsemi.com

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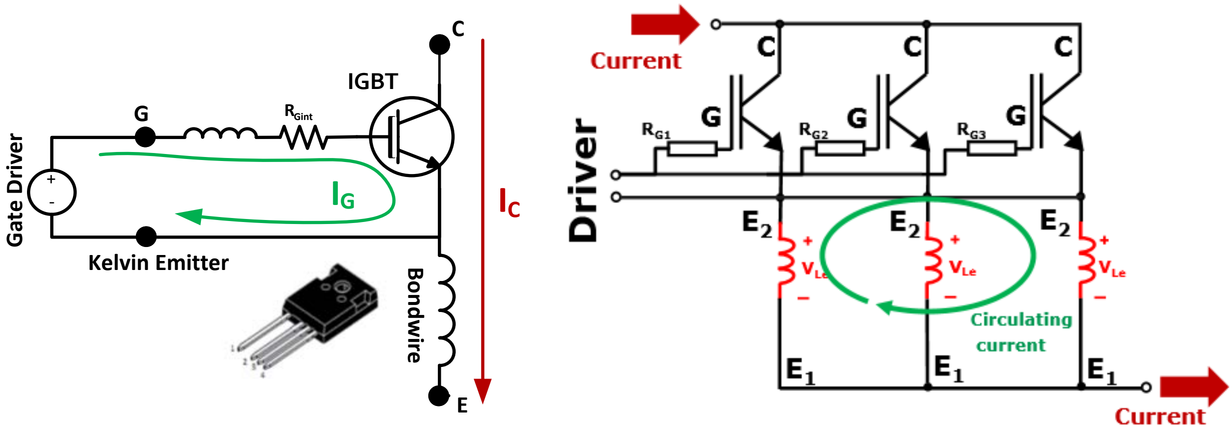
Abstract

The use of a kelvin-source (sometimes referred to as an auxiliary-source) terminal is becoming common in fast switching semiconductors such as Silicon Carbide MOSFETs. The kelvin-source terminal decouples the path of the load current from the path of the control current, leading to improved switching characteristics. However, in multiple paralleled chips, kelvin-source connections sometimes lead to load current imbalances among the bondwires of each paralleled chip. A simple method to prevent this is to introduce kelvin-source resistors. This paper investigates the sizing of kelvin-source resistors and their subsequent impact on current balancing. This investigation has primarily been conducted in the context of using the kelvin-source resistor as a failure detection sensor. We find that a kelvin-source resistor of 0.5Ω to 1Ω is adequate for current balancing purposes, however for dual purpose use as a failure sensor, a value of 2Ω or more may be recommended.

Introduction

Faster switching semiconductors mean that the parasitic elements of power semiconductor packaging impact semiconductor performance to a greater degree. As a result, the use of a fourth terminal known as a kelvin-source (or kelvin-emitter in IGBTs) connection to provide the reference potential for the gate control voltage is becoming more common [1, 2]. For example, TO-247-4 packages are now widespread for both Silicon and Silicon Carbide devices. This connection separates the path of the gate current from the path of the load current, as shown in Fig. 1a. This leads to increased switching speed and increased efficiency since the induced voltage over the bondwires during turn-on and turn-off no longer attenuates the effective gate voltage [3].



(a) (b)

Figure 1: (a) Power semiconductor schematic with kelvin-source connection. (b) Schematic with paralleled semiconductors circulating current path through kelvin-source/emitters [3].

In power semiconductor modules with multiple chips in parallel, a kelvin-source connection for each semiconductor chip does not completely decouple the gate current from the load current path. In fact, a low impedance path exists through the kelvin-source and power-source bondwires where circulating currents can occur, as shown in Fig. 1b. Even a minor difference in the induced voltage across the source inductance can generate extremely high circulating currents during transient conditions. This can happen for instance if the paralleled chips have mismatched switching properties [3]. Additionally, current imbalances occur during normal steady-state conditions, where load current from one chip can flow through its kelvin-source bondwire and subsequently through the power-source bondwires on another chip [2].

To reduce the magnitude of these current imbalances, one simple solution is to place a kelvin-source resistor (R_{KS}) in the kelvin-source path [2-4] for each chip, which becomes part of the overall gate resistance. Fig. 2 displays a circuit diagram of two semiconductors in parallel, each with an R_{KS}. In this case, the total gate resistance becomes the sum of the external gate resistor, the internal gate resistor, and R_{KS}. Our activities in this paper are focused on Silicon Carbide MOSFETs, since the kelvin-source topic is pertinent to wide band-gap devices due to their fast switching nature [2, 5, 6]. As an example, Fig. 3a and Fig. 3b show photos of a multichip Silicon Carbide MOSFET power module both with and without kelvin-source resistors respectively. However, in general the work in this paper should be transferable to IGBTs if a kelvin-emitter connection is used.

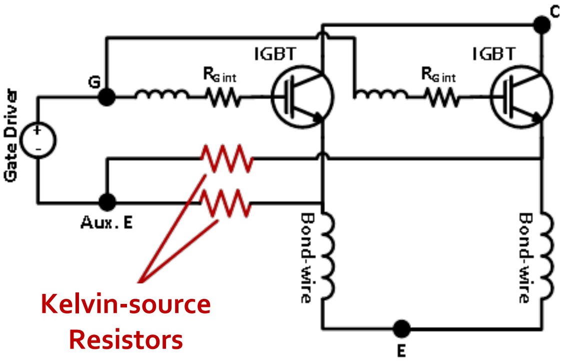
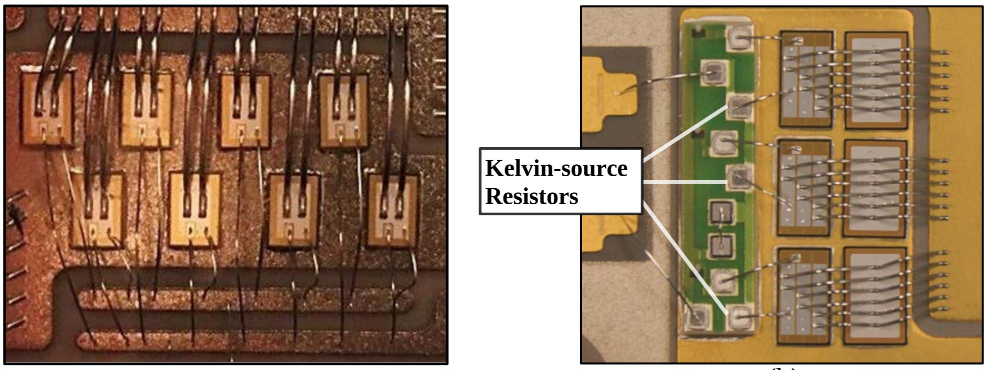


Figure 2: Schematic with paralleled semiconductors and kelvin-source resistors



(a) (b)

Figure 3: (a) Layout of SiC module without kelvin-source resistors (b) Layout of SiC module with kelvin-source resistors [3].

Despite the phenomenon of current imbalances caused by paralleled kelvin-source connections being mentioned in several publications [2-4], there is little public literature regarding the impact of the resistor sizing. Furthermore, we have recently proposed and presented a proof-of-concept for the use of kelvin-source resistors as a failure prevention and failure detection sensor [7].

Therefore, in this paper, we perform simulations on six paralleled SiC MOSFETs in order to investigate the impact of kelvin-source resistor sizing for both current sharing and reliability purposes.

Simulation

Current Balancing

Fig. 4 shows the schematic of an LTSpice electrical simulation for 6 SiC MOSFETs in parallel. We have included several module packaging parasitics, including the inductance and resistance of the power-source bondwires and the kelvin-source bondwires. The MOSFET models are for C3M0120100 dies which are rated for approximately 15A, and were acquired directly from WolfSpeed. The values for inductance and resistance of the bondwire interconnections were approximated using ANSYS Q3D. In Fig. 4, the kelvin-source connections are modelled as inductors that have a series resistance parasitic component, which can be edited to form the kelvin-source resistance.

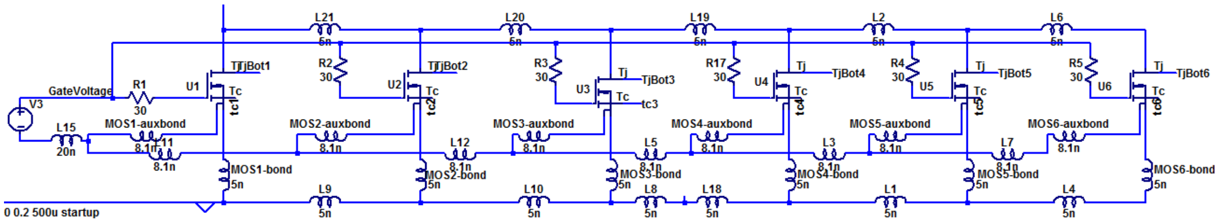


Figure 4: LTSpice simulation schematic of 6-chip SiC MOSFET module

Fig. 5 displays the simulation results for the current through each MOSFET's drain, power-source and kelvin-source bondwires when a current of 80A is injected. Two different levels of kelvin-source resistance are shown. The first value is 1mΩ, representing no kelvin-source resistor added. The second value is 6Ω, which is added to each individual kelvin-source path. This value was chosen arbitrarily so that the overall additional gate resistance amounted to 1Ω.

Fig. 5 displays a clear imbalance of current in the power-source bondwires of each MOSFET when no kelvin-source resistor is present. The drain currents of each MOSFET appear to be evenly distributed within a 200mA span around 13.5A. However, the current distribution in the source side bondwires shows a decisive imbalance. The power-source bondwires of MOSFET 1 carry the greatest load, with a peak current of over double that of MOSFET 6. After 80µs, the power bondwires in MOSFET 1 carry a 25% higher current than MOSFET 6 with 15.5a to 11.8A respectively.

The cause of this imbalance is the fact that load current is able to flow through the kelvin-source bondwires. The kelvin-source bondwires of MOSFETs 4, 5 and 6 (the MOSFETs furthest from the ground terminal) display negative currents of several amps, while the kelvin-source bondwires of MOSFETs 1, 2 and 3 (those closest to the ground terminal) display positive currents of several amps. This indicates that a proportion of the current flowing through MOSFETs 4, 5 and 6 is redirected through the bondwires of MOSFET 1, 2 and 3, before flowing to ground. The direction of this current flow could be altered by changing the positioning of the ground terminal (i.e. moving it closer to MOSFET 6, or to the midpoint between MOSFET 3 and 4); nevertheless, the principle causing the current imbalance remains the same.

The bondwire current imbalance described above can have several impacts on the reliability of the module. The bondwires of MOSFET 1 experience significantly higher current density and higher current per bond-foot than those on the other MOSFETs in the module. This can lead to higher thermo-mechanical stress and a higher susceptibility to wear-out failure. On the other hand, the kelvin-source bondwires are typically sized to carry only the current required for charging and discharging of the gate (an average current in the mA range typically), and therefore may only be in the region of 50µm to 100µm in diameter. This for example can be seen from Fig. 3, where it is visually clear that the kelvin-source wire bond is a single wire that is significantly thinner than those designated for carrying the load current.

If the kelvin-source bondwire is forced to carry current several orders of magnitude higher than the average gate current, there is a new risk that the kelvin-source bond becomes the source failure. In fact, in this simulation, it is MOSFET 1 that stress on both its power bondwires and kelvin-source bondwires – so will likely be the chip most susceptible to failures in both bondwires.

It can be seen from Fig. 5 however, that introducing the 6Ω kelvin-source resistors rectify the current imbalance, with kelvin-source bondwires of all MOSFETs now conducting current in the region of mA amplitude. As highlighted previously, we chose the value of 6Ω for the kelvin-source resistance arbitrarily. Therefore, we ran the simulation with a sweep of the kelvin-source resistances from 1mΩ to 10Ω. The results of this are shown in Fig. 6, where we plot the maximum and steady-state current through the kelvin source bondwire vs. kelvin-source resistor for most stressed MOSFET 1. Fig. 6 displays both a linear and log scale. It can be seen from this plot that it only requires a very small kelvin-source resistance to reduce the current through the kelvin-source bondwire from several amps to a few mA. Just 100mΩ is enough to reduce the steady-state current to the milliamp range, while increasing the kelvin-source resistance beyond 1Ω appears to have no additional benefit.

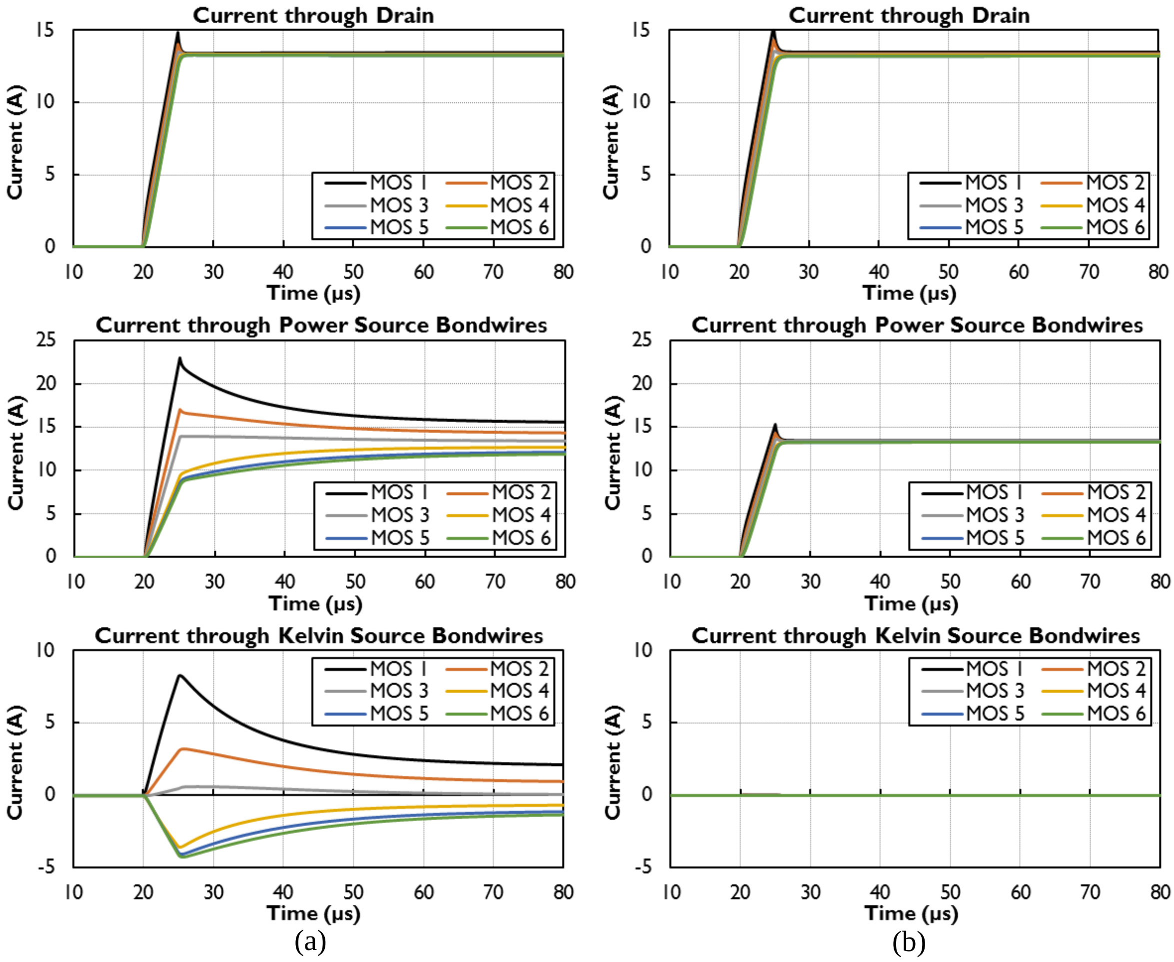
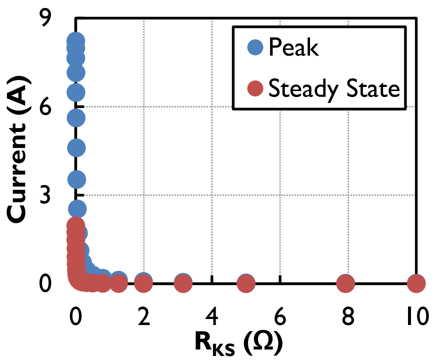
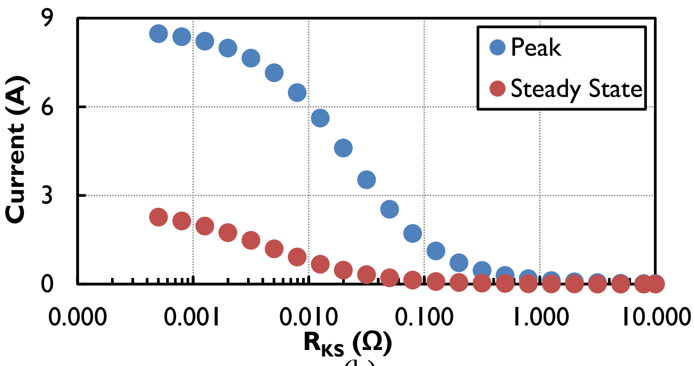


Figure 5: LTSpice simulation results for current flowing through each MOSFETs drain, power-source bondwires, and kelvin-source bondwires. (a) With no added kelvin-source resistor. (b) With 6Ω kelvin-source resistors.



(a)



(b)

Figure 6: LTSpice simulation results peak and steady-state current flowing through MOSFET 1 kelvin-source bondwire, with sweep of kelvin-source resistance from 1mΩ to 10Ω. (a) Linear scale (b) Log scale.

Failure Detection Sensor

In [7] we describe a method to use the kelvin-source resistor as a reliable failure detection sensor for power modules with multiple chips in parallel. This failure detection method can prevent module explosion and detect and respond to a failure in under one switching cycle. The method will briefly be described in the following paragraphs.

The principle can be described as follows. In a module with paralleled semiconductor chips, at some point in the modules life, one chip will experience the entirety of its power bondwires lifting off. In a normal module without a kelvin-source terminal, this would leave an open circuit on the source side of one of the chips, leading to a floating gate and subsequent explosion of the module. However, with a kelvin-source terminal and resistor included, there remains a pathway, albeit of high impedance, for a small amount of load current to continue to pass through the chip and for gate control to be maintained. The blue dotted arrow in Fig. 7 shows the available pathway despite the chip having ruptured bondwires.

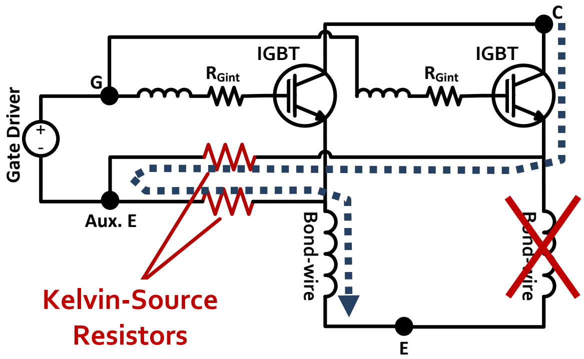


Figure 7: Current flow (blue arrow) in paralleled chips with a kelvin-source terminal when one chip suffers complete bond-wire rupture [7].

This small amount of current flowing through the kelvin-source resistor induces a voltage across the resistor which can be detected by monitoring the voltage across the kelvin-source and power-source terminal. The voltage is monitored with a comparator to subsequently implement a fault control strategy before the remaining paralleled chips fail due to thermal overload from carrying excess current.

One of the advantages of this failure detection method is the warning signal provided when the module is in a failed condition is an order of magnitude greater than prior state-of-the-art [7]. Nevertheless, the size of the warning signal is logically dictated by the size of the kelvin-source resistor. In [7] however, we arbitrarily chose 6Ω as the kelvin-source resistor. Fig. 8 displays the LTSpice simulation schematic used to assess the impact of kelvin-source resistor sizing on this failure detection concept. We removed the power bondwire from MOSFET 1, highlighted by the red circle, and again performed a sweep of the kelvin-source resistors from 1mΩ to 10Ω.

Fig. 8 displays the results of sweep with the MOSFETs conducting 80A. It displays both the warning signal generated, as well as the current flowing through the kelvin-source of MOSFET 1. Here it is possible to note that small values of kelvin-source resistance do not attenuate the current significantly, unlike in Fig. 6. For example, at 100mΩ the current through the kelvin-source is still 8A. It is not until the value of the kelvin-source resistance reaches 3Ω that the current is reduced to below 500mA. This is an important point for the failure detection method, since a pertinent feature is that the presence of the resistor should not only provide a warning signal, but also prevent the kelvin-source bondwire from failing which leads to loss of gate control and subsequent explosion. Too high current can lead to the bondwire melting, as displayed in the photograph in Fig. 10. However, we have also observed rapid failures of the kelvin-source bondwire without experiencing a visible self-heating phenomenon. Therefore, it is important to keep the current conducted through the kelvin-source bondwire to a minimum when in this condition. Another option is to increase the wire gauge of the kelvin-source bondwire so that is it capable of safely handling the current with 1Ω.

With regards to generating a warning signal, values greater than 2Ω also appear to be preferable. This provides a signal in the region of 450mV – an order of magnitude higher than that of healthy state. As a result, it would appear that sizing the kelvin-source resistor to greater than 2Ω would be a favourable if the failure prevention possibilities are to be taken into consideration.

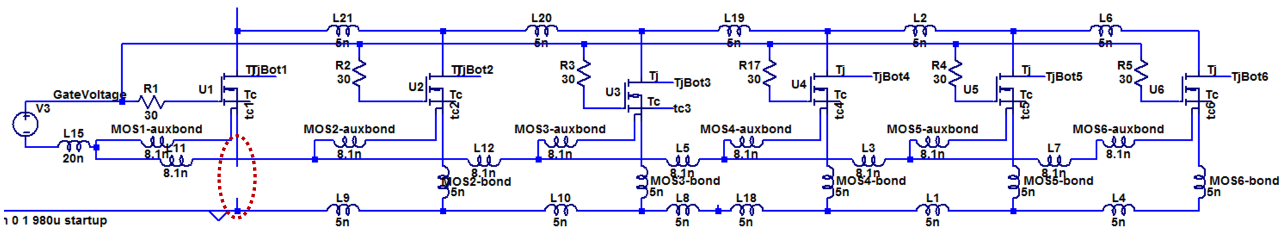


Figure 8: LTSpice simulation schematic of 6-chip SiC MOSFET module with MOSFET 1 having power bondwires removed.

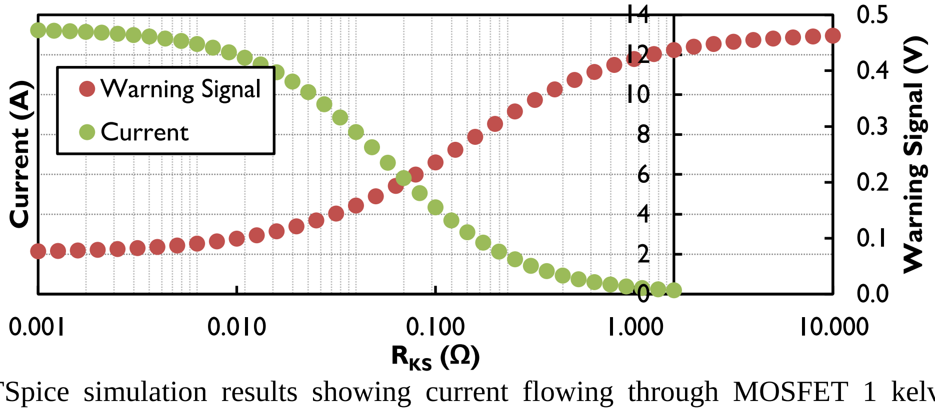


Figure 8: LTSpice simulation results showing current flowing through MOSFET 1 kelvin-source bondwire, and warning signal voltage from kelvin-source to power-source vs. kelvin-source resistance. MOSFET 1 has had power-source bondwires removed.

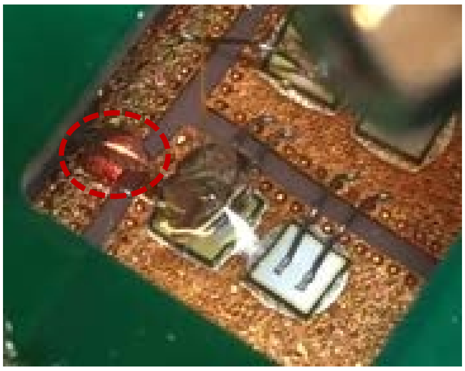


Figure 10: Kelvin-source bondwire of a SiC MOSFET overheating due to conduction of high current.

Conclusion

In this paper we investigate the impact of kelvin-source resistor sizing for improving current sharing and for failure detection purposes. We perform this investigation using a simulation of six paralleled Silicon Carbide MOSFETs. We find that kelvin-source resistors of 0.5Ω to 1Ω are adequate for current balancing purposes, however for using the resistor as a failure sensor, a value of 2Ω or more may be recommended in order to ensure that the kelvin-source bondwire does not fail due to over current, and also to generate a sufficient warning signal from the resistor.

A limitation of the presented simulation is that although the SiC MOSFET models included self-heating for die junction temperature, the bond-wire interconnections do not have a relationship to temperature or with temperature coupling to the die. Therefore, we have not made any assumptions regarding bondwire temperature due to current density, which would alter the bondwire resistance and the subsequent current distribution. Nevertheless, we feel that the simulation gives a reasonable approximation of the improvement the inclusion of kelvin-source resistors can make with regards to current sharing inside multichip power modules, as well as an indication on their sizing if they are also to be used as a failure sensor.

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