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A Family of High Step-Up Coupled-Inductor Impedance-Source Inverters with Reduced Switching Spikes

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***Abstract*—By using coupled inductors, impedance-source inverters can greatly increase their voltage step-up abilities at the expense of high voltage spikes at their dc-links due to leakage inductances. These voltage spikes can then cause damages and greater power losses. Therefore, to better clamp their dc-link voltages, various absorbing circuits have been proposed in this letter for forming a unique family of impedance-source inverters with even higher gains. The abilities of these inverters in clamping their dc-link voltages have been verified by experimental results presented at the end of the letter.**

***Index Terms*—coupled inductor, Impedance-source inverter, leakage inductance, voltage spikes, Y-source inverter.**

I. Introduction

Over the past one and half decades, various impedance- or Z-source inverters (ZSIs) [1] have been proposed for voltage-boosting by including a unique shoot-through (ST) state in the power circuit. Most of them have aimed to achieve a high step-up gain without excessively lowering the inverter modulation ratio. For instances, in [2], diode-capacitor unit have been introduced to the most elementary ZSI, while in [3], a cascaded quasi-ZSI (QZSI) has been proposed. But, in both ZSIs, their number of components may increase significantly, depending on the extent of improvement targeted.

They may therefore not be as competitive as the high frequency transformer isolated ZSI (HFFI-QZSI) proposed in [4], where an isolated transformer has been used for gain boosting. The tradeoff is an extra switch, which may complicate the gate-driving and protection. To avoid that switch, while still relying on magnetics for voltage-boosting, coupled-inductor impedance-source inverters (CISIs) may be better choices [5]-[11]. Nevertheless, they are commonly burdened by high voltage spikes at their dc-links, caused by the interruption of leakage currents of coupled inductors.

Some absorbing circuits for lowering these voltage spikes, and then absorbing the interrupted leakage energies, are thus necessary. In [5], the absorbing circuits proposed are an active snubber and a passive clamp, which can respectively be used with the T-source inverter. The active snubber includes an extra switch, while the passive clamp carries a large circulation current. They are thus not optimal solutions. Two other clamping circuits have been proposed in [12] and [13], but an impedance-source inverter protected by either of them will suffer small voltage spikes on the dc-link from the ST to the non-ST (NST) states unintentionally. Yet another recycling circuit has been proposed in [14], which although can generate a high gain and eliminate the dc-link spikes, but can only be used with a traditional coupled-inductor converter.

There are hence many existing challenges yet to be resolved, which this letter has attempted by proposing a family of twelve high step-up CISIs. Basic idea of the proposed inverters is to appropriately add novel absorbing circuits to the traditional CISIs. The absorbing circuits can then recycle leakage energies timely during state transitions, which upon ensured, greatly reduce transient voltage spikes at dc-links of the inverters. Besides, compared with the traditional CISIs, the proposed inverters generate higher gains, even though they share the same ST and NST operating principles. Their similar operating principles have also rendered a full presentation of all mathematical derivations for the twelve inverters as unnecessarily duplicative. Therefore, only mathematical derivation for the diode-assisted Y-source inverter has been presented, but for better gain comparison, final expressions for the twelve inverters have been summarized as a table to be discussed later.

II. Topologies

A family of twelve CISIs with effective absorbing circuits are provided in Fig. 1, where their respective absorbing circuits have been drawn in red. The remaining components in black are existing CISIs proposed in the literature, but they are not practically ideal because of high voltage spikes. Additionally, in each topology, L_{couple} represents its coupled inductor, which can be the Y-type [8], T-type [5], Δ-type [9], LCCT-type [15]

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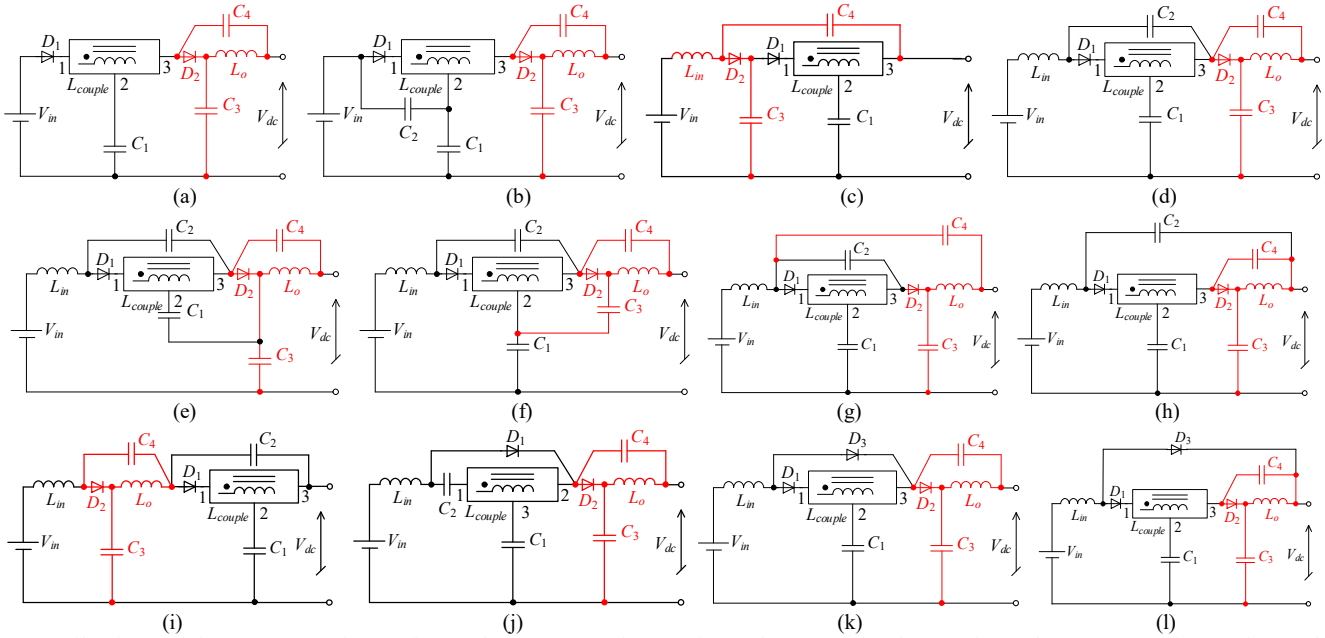

Fig. 1. Family of proposed CISIs. (a) Topology 1, (b) Topology 2, (c) Topology 3, (d) Topology 4, (e) Topology 5, (f) Topology 6, (g) Topology 7, (h) Topology 8, (i) Topology 9, (j) Topology 10, (k) Topology 11, (l) Topology 12.

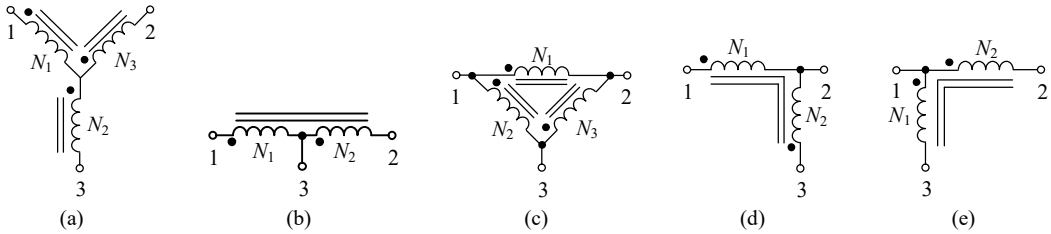

Fig. 2. Different L_{Couple} configurations. (a) Y-type, (b) T-type (c) Δ-type (d) LCCT-type (e) Γ-type.

or Γ-type [7], as shown in Fig. 2. The resulting twelve topologies can then be categorized into four types, named respectively as the T-source, quasi-Z-source, LCCT, and diode-assisted (DA) types, according to their applications and structures. Irrespective of that, certain general features can be observed from the twelve topologies.

For instance, topology 1 uses minimum components, which may eventually lead to a reduction of volume and cost. However, it carries a discontinuous input current, and may hence not be suitable for photovoltaic systems. Topology 2 can smooth its input current, but only if its ratio of C_2 to C_1 matches strictly with its magnetic turns ratio. This strict requirement is however not applicable to topology 3, since it has an inductor in series with its input source. Nevertheless, the above three topologies can be commonly categorized as the T-source type, since their existing coupled inductors in black effectively form T-shaped structures.

The same inductive smoothing of input current has also been ensured by topology 4, which in addition, generates the highest boost among the twelve topologies. Topologies 5 to 9 have, in fact, been modified from topology 4 to introduce different current and voltage stresses. For example, by connecting the negative terminal of C_3 to the positive terminal of C_1 in topology 4, topology 6 is formed with a decreased voltage stress across C_3. Topologies 4 to 9 can therefore be grouped together under quasi-Z-source type, since their existing circuits in black resemble the quasi-Z-source inverter found in [16].

As for topology 10, it can better prevent saturation of its coupled inductor, because of two capacitors connected in series with windings of L_{couple} in Fig. 1(j). A third capacitor at terminal 2 of L_{couple} is however absent, but according to circuit laws, no dc current will still flow through that terminal. The concept here is thus similar to the existing LCCT-type CISI, whose two windings are also in series with two capacitors. Thus, topology 10 is categorized under the LCCT type. Topologies 11 and 12 are considered as the DA type, since they use more diodes than capacitors for voltage boosting. The DA-type CISIs will therefore have more prominently different gain expressions than the other high step-up CISIs, as demonstrated next.

III. Operational Principles

Fig. 3 shows the diode-assisted Y-source inverter (DA-YSI), derived from topology 11 in Fig. 1. For conciseness, its inverter bridge and load have also been replaced by a switch *SW* and a current source in parallel, while its coupled inductor has been modeled by a leakage inductance and three ideal windings. Fig. 4 shows its operational modes, while Fig. 5 shows the key waveforms accompanying these modes. Both figures are now described, as follows.

ST [t_0, t_1]: Switch *SW*, diodes D_1 and D_3 conduct, while diode D_2 is reverse-biases, leading to Fig. 4(a). The coupled inductor is thus clamped by C_1 and C_4. Moreover, a large voltage v_{LK}

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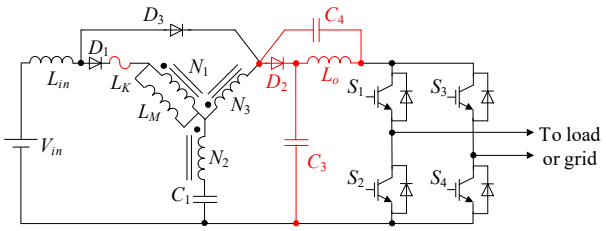

Fig. 3. DA-YSI with clamped dc-link voltage.

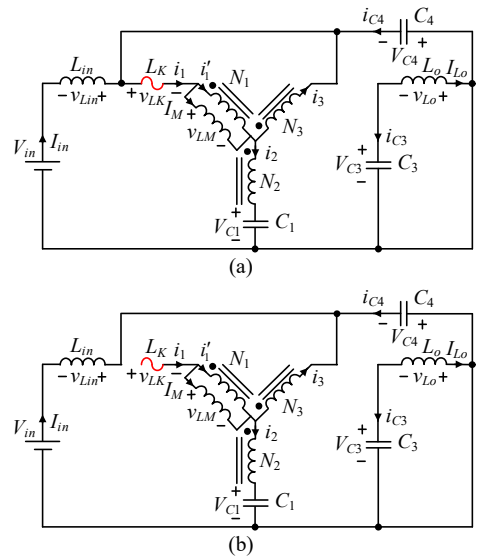

Fig. 4. Equivalent circuits of DA-YSI when in (a) ST state [t_0, t_1], (b) ST state [t_1, t_2], (c) NST state [t_2, t_3], and (d) NST state [t_3, t_0].

appears across the leakage L_K to force its current down rapidly. During that time, source V_{in} also charges L_{in}, which when considered with other observations, yields the following voltages across L_M, L_{in} and L_o.

$$v_{LM} = (V_{C1} + V_{C4})\frac{N_1}{N_3 - N_2} \tag{1}$$

$$v_{Lo} = -V_{C3} \tag{2}$$

$$v_{Lin} = -(V_{in} + V_{C4}) \tag{3}$$

$$v_{LK} = -K(V_{C1} + V_{C4}),\ K = \frac{N_1 + N_3}{N_3 - N_2} \tag{4}$$

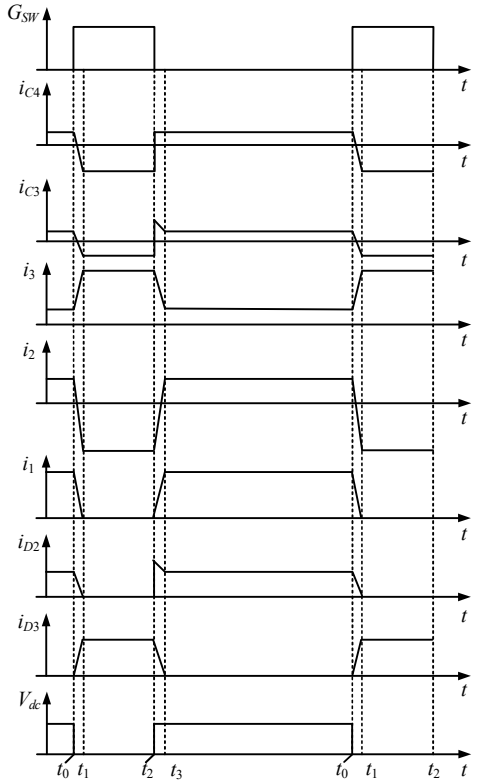

Fig. 5. Key waveforms of DA-YSI.

where d is the ST duty ratio, and K is the winding factor.

ST [t_1, t_2]: Current through leakage L_K reaches zero, causing the diode D_1 to reverse-bias in Fig. 4(b) without affecting the states of the other devices. The voltages across L_M, L_{in} and L_o are thus the same as those during [t_0, t_1], but v_{LK} across L_K is now zero.

NST [t_2, t_3]: Switch SW turns OFF with all diodes remaining in conduction, as shown in Fig. 4(c). Conduction of D_3 is particularly necessary, in order to carry most current through L_{in}, as leakage current through L_K increases gradually from zero. The increase in leakage current is, in turn, brought by a large leakage voltage v_{LK}, which together with other observations, yields the following voltage expressions.

$$v_{LM} = (V_{C1} - V_{C3})\frac{N_1}{N_3 - N_2} \tag{5}$$

$$v_{Lo} = V_{C4} \tag{6}$$

$$v_{Lin} = V_{C3} - V_{in} \tag{7}$$

$$v_{LK} = K(V_{C3} - V_{C1}) \tag{8}$$

Moreover, since the conduction of D_3 ends when leakage current rises to current I_{in} through L_{in}, the duration $\Delta dT = t_3 - t_2$ can be calculated from:

$$I_{in} = \frac{P}{V_{in}} = \frac{1}{L_K}\int_{dT}^{(d+\Delta d)T} v_{LK}\,dt \tag{9}$$

where T is the switching period, and $d = (t_2 - t_0)/T$ is the earlier defined ST duty ratio.

NST [t_3, t_0]: This corresponds to Fig. 4(d), which is the state entered, after diode D_3 begins to block, while the other two diodes remain in conduction. Voltages across L_M and L_o thus remain unchanged from those during [t_2, t_3], while voltage

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TABLE I
SUMMARY OF GAINS FOR DIFFERENT CISIS IN FIG. 1

Figure Number	Gain $B = V_{dc}/V_{in}$	category
Topology 1 (Fig. 1(a))	$1/[1-(1+K)d]$	T-source type
Topology 2 (Fig. 1(b))	$1/[1-(1+K)d]$	
Topology 3 (Fig. 1(c))	$1/[1-(1+K)d]$	
Topology 4 (Fig. 1(d))	$1/(1-(2+K)d)$	Quasi-Z-source type
Topology 5 (Fig. 1(e))	$1/[1-(2+K)d]$	
Topology 6 (Fig. 1(f))	$1/[1-(2+K)d]$	
Topology 7 (Fig. 1(g))	$1/[1-(2+K)d]$	
Topology 8 (Fig. 1(h))	$1/[1-(2+K)d]$	
Topology 9 (Fig. 1(i))	$1/[1-(2+K)d]$	
Topology 10 (Fig. 1(j))	$1/(1-Kd)$	LCCT type
Topology 11 (Fig. 1(k))	$1/[1-(2+K)d+Kd^2]$	DA-CISIs type
Topology 12 (Fig. 1(l))	$1/(1-d)\ [1-(1+K)d]$	

TABLE II
TURNS RATIOS OF DIFFERENT COUPLED INDUCTOR CONFIGURATIONS

Coupled Inductor	Turns ratio K
Y-type	$(N_1+N_3)/(N_3-N_2)$
T-type	$(N_1+N_2)/N_2$
Δ-type	$(N_2+N_3)/N_3$ $(N_2=N_1-N_3)$
LCCT-type	N_1/N_2
Γ-type	$N_2/(N_2-N_1)$

across L_{in} changes to:

$$v_{Lin} = \alpha\left[K(V_{C1}-V_{C3})+V_{C3}-V_{in}\right] \tag{10}$$

where $\alpha = L_{in}/(L_{in}+L_K)$ is the series voltage division factor between L_{in} and L_K.

When the equations in the four states now are defined, volt-second balance respectively applies to L_M, L_o and L_{in} and gives:

$$\begin{aligned}&\int_{t_0}^{t_2} v_{Lx}dt+\int_{t_2}^{t_3} v_{Lx}dt+\int_{t_3}^{t_0} v_{Lx}dt\\&=\int_0^{dT} v_{Lx}dt+\int_{dT}^{(d+\Delta d)T} v_{Lx}dt+\int_{(d+\Delta d)T}^{T} v_{Lx}dt=0\end{aligned} \tag{11}$$

where $L_x = L_M$, L_o or L_{in}. Further assuming that L_K is small, and hence $\alpha \approx 1$ and $\Delta dT \approx 0$, concise expressions for the capacitor voltages and voltage gain B of the DA-YSI can be derived as:

$$V_{C1} = \frac{(1-2d)V_{in}}{1-(2+K)d+Kd^2} \tag{12}$$

$$V_{C3} = \frac{(1-d)V_{in}}{1-(2+K)d+Kd^2} \tag{13}$$

$$V_{C4} = \frac{dV_{in}}{1-(2+K)d+Kd^2} \tag{14}$$

$$B = \frac{V_{dc}}{V_{in}} = \frac{1}{1-(2+K)d+Kd^2} \tag{15}$$

In contrast, the gain of the traditional YSI has earlier been derived as $B = 1/(1-Kd)$ in [9], which for the same d, is smaller than that of the DA-YSI. Alternatively, to generate the same gain, the DA-YSI will demand a smaller d, which must now vary within the following narrower range.

$$0 < d < \frac{2+K-\sqrt{4+K^2}}{2K} \tag{16}$$

Even more importantly, its dc-link voltage has successfully been clamped by C_3 and C_4 during the NST states. Voltage spikes across its dc-link have hence been effectively lowered throughout the full switching period. The lowering of spikes can also be ensured by other topologies in Fig. 1, which for comprehensiveness, have their gains derived and listed in Table I. Different winding factor K expressions for those coupled inductors shown in Fig. 2 have also been summarized in Table II for an easier reference.

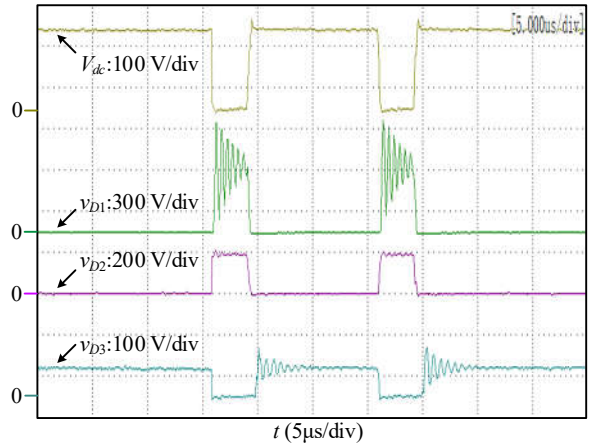

Fig. 6. Experimental waveforms of V_{dc}, v_{D1}, v_{D2} and v_{D3}.of DA-YSI.

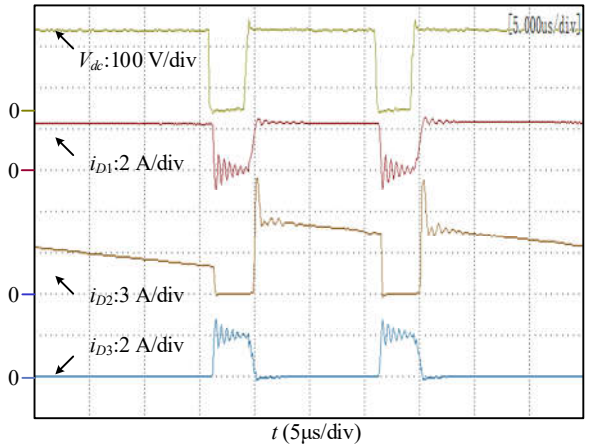

Fig. 7. Experimental waveforms of V_{dc}, i_{D1}, i_{D2} and i_{D3} of DA-YSI.

IV. EXPERIMENTAL RESULTS

Experiments have been performed with a 200 W DA-YSI, whose coupled inductor with winding turns of 40:40:80 ($K = 3$) has been "loosely" wound on a C055863A2 core. The inductances of N_1, N_2 and N_3 are L_1 = 0.3669mH, L_2 = 1.4215mH, L_3 = 0.3661mH. The leakage inductances of N_1, N_2 and N_3 are L_{K1} = 2.29μH, L_{K2} = 1.83μH, L_{K3} = 7.77μH. This is to deliberately enlarge leakage influences for more effective testing of the inverter, whose input voltage and switching frequency have been set to 80 V and 10 kHz, respectively. The expected dc-link and output ac peak voltages are then 200 V and 160 V, respectively, if d = 0.13 and modulation index M =

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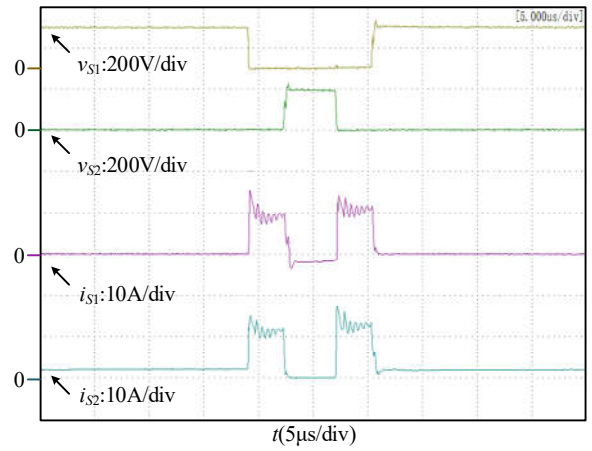

Fig. 8. Experimental waveforms of v_{S1}, v_{S2}, i_{S1} and i_{S2} of DA-YSI.

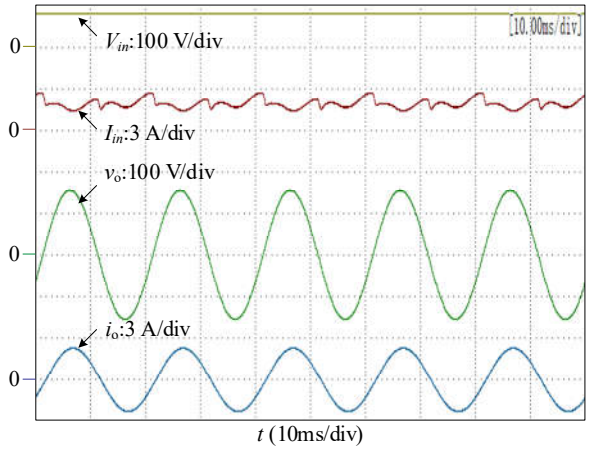

Fig. 9. Experimental waveforms of V_{in}, I_{in}, v_o and i_o of DA-YSI.

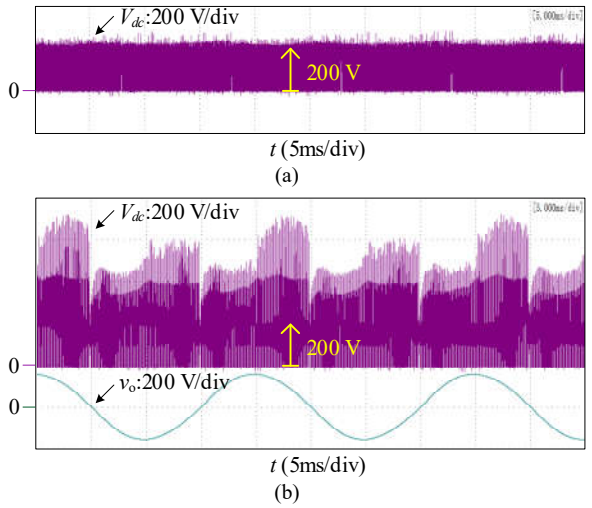

Fig. 10. Experimental waveforms of (a) V_{dc} of DA-YSI, and(b) V_{dc} and v_o of YSI.

0.8. These expectations that the overvoltage spikes disappear have been verified by results presented from Fig. 6 to Fig. 10. Starting with Fig. 6 and Fig. 7, the illustrated dc-link voltage and diode variables are obviously not burdened by unwanted high voltage spikes, except for transient ringing triggered by semiconductor switching.

Voltages and currents of the phase-leg formed by switches S_1 and S_2 are next shown in Fig. 8, where it can be seen that the

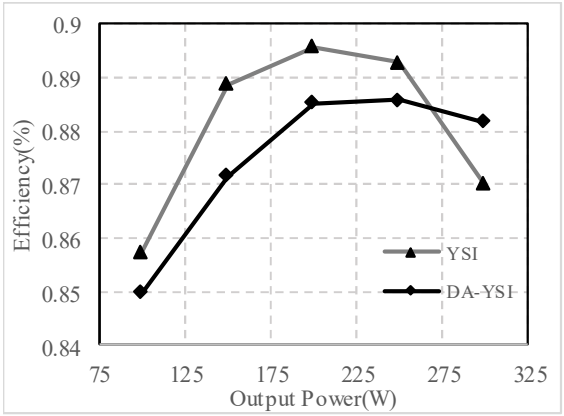

Fig. 11. Efficiency comparison of the YSI and DA-YSI.

same positive ST current i_{st} flows through both switches when their voltages are both zero. On the other hand, when in a NST state, only one switch current is non-zero, and will flow through the corresponding anti-parallel diode if its value is negative. Fig. 9 then shows the input dc voltage V_{in}, input dc current I_{in}, output ac voltage v_o and output ac current i_o, from which the peak ac voltage has been read to be 155 V. It is thus only 5 V less than its theoretically computed value, which is mostly attributed to the effects of the leakage inductance and the equivalent series resistance (ESR).

The YSI is also tested on the same board for comparison. The duty ratio and modulation index are 0.2 and 0.8 for YSI, respectively, and the circuit parameters are the same with DA-YSI. Thus, the theoretical dc-link voltage is 200 V and output ac peak voltages are 160 V. Fig. 10 shows the V_{dc} of DA-YSI and YSI. It can clearly be seen that the dc-link voltage spikes have been limited to small values in the DA-YSI, while the voltage spikes of the YSI is more than two times above the theoretical value of dc-link voltage. Measured efficiencies of both inverters are next shown in Fig. 11, where the trend noted is efficiency of the DA-YSI is slightly lower than that of the YSI from around 100W to 265W. Above that range, efficiency of the DA-YSI becomes higher, as the amount of leakage energy efficiently recycled becomes more prominent.

V. Conclusion

This letter presents a new family of CISIs, which in addition to inheriting all advantages offered by a coupled inductor, generate even higher gains with a specified shoot-through duty ratio. Additionally and more importantly, by including a diode, an inductor and two capacitors to form an absorbing circuit, all proposed CISIs do not generate dangerously high dc-link voltage spikes, and are hence less prone to damages. This intended feature, together with the inverter voltage gain, has thoroughly been analyzed with a DA-YSI, which indeed, are in agreement with obtained experimental results.

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