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Reduced Switch-Count Structure for Symmetric Multilevel Inverters with a Novel Switched-DC-Source Sub-Module

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Abstract: These days, Symmetric multilevel inverters (SMLIs) have become as one of the efficient solutions to improve the output power quality of many renewable-energy based applications. To achieve better output power spectrum in the conventional types of SMLIs, as the number of output voltage levels increases, the number of required power switches and the overall cost will be enhanced. The aim of this study is to present a new cost effective SMLIs configuration, which can generate greater number of output voltage levels with a least of switching devices. The proposed structure contains a novel switched-dc-source (SDCS) sub-module that can produce three positive output voltage levels with a contribution of four equal dc voltage sources, two unidirectional, and one bi-directional power switches. Accordingly, to create a uniform staircase output voltage with multiple levels, the proposed SDCS sub-module is integrated into a new design. Therefore, a new family of reduced switch-count (RSC)-SMLIs is derived, which is capable of generating at least 13- and 15-level output voltages using only ten power switches and nine gate drivers. Furthermore, when employing several of the proposed SDCS sub-modules in series, a new generalized RSC-SMLI topology is obtained. Comparisons with prior-art SMLIs structures are done, which also highlights the beneficial potential of the proposed topology. To demonstrate the superior performance of the proposed topology, several simulation and experimental results have been provided.

1. Introduction

In high power -medium -voltage power electronic applications, high-performance DC-AC power converters (inverters) are always demanded. Generally, the inverters should possess a good output power quality (low harmonics), low cost, and high efficiency. Among the voltage source DC-AC inverters, the advent of multilevel inverters (MLIs) can properly address many shortcomings of the conventional inverters, especially the power quality in energy management of flexible AC micro grids [1], [2].

Theoretically, MLIs can generate a staircase output voltage, which resembles the shape much close to a sinusoidal wave [3]. Therefore, a low total harmonic distortion (THD) is one of the most important benefits of such converters that can eventuate to reduce the size of the output filter and its power losses [1]. As a result, a reduction in the total cost is expected. Apart from this merit, MLIs are also able to remarkably diminish the voltage stresses of the power switches at the OFF-state condition. Therefore, in medium-voltage applications, a wide range of power switches can be used [3], [4].

Diode-clamping, flying capacitor and cascaded H-bridge (CHB) structures are assigned as the three major families of MLIs. Each one has its own specific benefits and also drawbacks [5]-[8]. Basically, as the number of output voltage levels increases, the count of power switches becomes higher. In this regard, the use of a great deal of power switches increases the total conduction and switching losses, and it can also jeopardy the reliability of the entire system [3]-[5]. More importantly, the cost increases at the same time.

Among the conventional MLIs, the CHB-based structures require the least number of power switches. Additionally they have a modular architecture that enables the flexible extension capability of the inverters to reach any desired number of output voltage levels [9]-[10]. Herein, isolated dc voltage sources of the CHB-MLIs can be either symmetric or asymmetric. It is clear that providing the non-equal and relatively large values of the dc sources in the asymmetric version is more costly. Moreover, their accessibility usually becomes much difficult than the symmetric types. The OFF-state voltage across the power switches of the asymmetric topologies is much higher than the symmetric ones [11]-[12]. Those disadvantages further limit the applications of asymmetric MLI systems.

Therefore, the symmetric multilevel inverters (SMLIs) become preferable for many industrial-based applications, e.g., electric vehicles and photovoltaic (PV) systems. However, it is not an efficient solution to using the conventional CHB-MLIs to achieve the larger number of output voltage levels, since a great deal of power devices will be required. For instance, to generate a nine-level output voltage, 16 power switches are required in the conventional CHB-based SMLI system [3].

To address this issue, many attempts have been made in the literature to introduce new reduced switch-count (RSC)-SMLIs [13]-[23]. Some of the most prior-art schemes of the RSC SMLIs are shown in Fig. 1.

As shown in Fig. 1(a), by using switched dc source (SDCS) sub-modules, a modular SMLI design was proposed in [13] which can properly reduce the total number of ON state power switches. Here, by integrating six or seven non-isolated dc voltage sources in the same circuit design, 13 levels or 15 levels of the output voltage can be respectively obtained, while 12 power switches are required.

Connecting several ladder bi-directional switches (LBS) to the conventional H-bridge cell is an effective attempt to reduce the switch count, as shown in Fig. 1(b). The use of H-bridge cell to make the negative steps of the output voltage is also conceptualized in [15]-[16], where new efficient RSC-SMLI topologies were investigated. Notably, all the power switches used in the H-bridge cells have to bear the highest peak inverse voltage (PIV). This can make some practical limitations for the RSC-SMLI topologies in high-voltage applications. A u-cell version of the SMLI was thus recommended in [18] (see Fig. 1(c)). It offers a modular design without H-bridge cells for turning the output polarity. Here, a cross-switched technique like what was using in [17] has been utilized, which can properly divide the total standing voltage (TSV) among the switches. Moreover, at each level of the output voltage, half number of the total power switches should be ON.

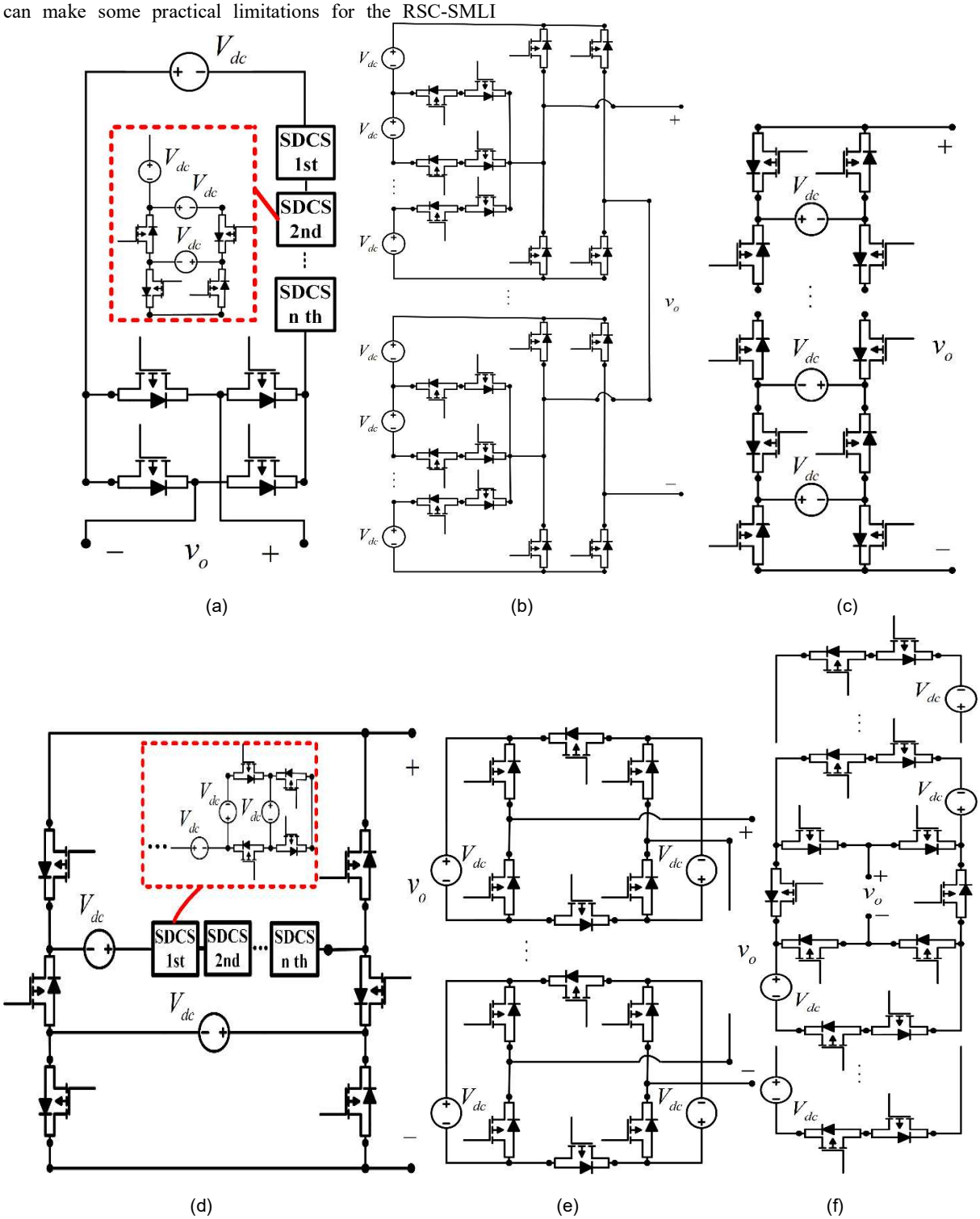


Fig. 1. *Different RSC-SMLIs topologies proposed in (a) [13], (b) [14], (c) [18], (d) [19], (e) [20], and (f) [21]*

TABLE 1. A Summary Description of Different RSC-SMLIs Shown in Fig.1

Ref	Topology Description	Example Case Study
Fig. 1. (a) [13]	• Use of Unidirectional Power Switches • Modularity × Higher TSV	15-Level Output Voltage • No. Unidirectional Switch Count: 12 • Maximum No. ON State Switches: 6 • Overall TSV in Per Unit: 5.71 • No. Gate drivers:12
Fig. 1 (b) [14]	• Modularity • Lower No. ON State Switches × Higher TSV × Use of Bi-directional and Unidirectional Power Switches	15-Level Output Voltage • No. Unidirectional Switch Count: 4 • No. Bi-directional Switch Count: 6 • Maximum No. ON State Switches: 4 • Overall TSV in Per Unit: 8 • No. Gate drivers: 10
Fig. 1 (c) [18]	• Modularity • Use of Unidirectional Power Switches • Lower TSV × Higher No. Power Switches and Gate Drivers	15-Level Output Voltage • No. Unidirectional Switch Count: 16 • Maximum No. ON State Switches: 8 • Overall TSV in Per Unit: 4 • No. Gate drivers: 16
Fig. 1 (d) [19]	• Modularity • Use of Unidirectional Power Switches × Higher TSV	11-Level Output Voltage • No. Unidirectional Count: 10 • Maximum No. ON State Switches: 5 • Overall TSV in Per Unit: 6 • No. Gate drivers: 10
Fig. 1 (e) [20]	• Modularity • Lower TSV • Use of Unidirectional Power Switches × Higher No. of Power switches and Gate Drivers	13-Level Output Voltage • No. Unidirectional Count: 18 • Maximum No. ON State Switches: 9 • Overall TSV in Per Unit: 4 • No. Gate drivers: 18
Fig. 1 (f) [21]	• Modularity • Lower No. Power switches and Gate Drivers × Use of Bi-directional and Unidirectional Power Switches × Intermediate value of TSV	`15-Level Output Voltage • No. Unidirectional Count: 6 • No. Bi-directional Switch Count: 5 • Maximum No. ON State Switches: 7 • Overall TSV in Per Unit: 4 • No. Gate drivers: 11

With this concept, SDCS sub-modules can be inserted into the u-cell topology, as it was developed in [19] (see Fig. 1(d)). Additionally, a series connection of improved H-bridge cells reported in [20] is another innovative approach to reduce the required components of SMLIs. The topology is shown in Fig. 1(e). In this regard, by employing the LBS technique, those topologies can be generalized to make an optimum SMLI structure with the lowest switch-count [21], as demonstrated in Fig. 1 (f). Similar concepts have also been proposed in [22] and [23].

In order to better reflect the potentiality of different abovementioned RSC-SMLI structures, a summary of topology description has also been conducted in Table 1.

Considering the above, this study continues the former breakthrough by presenting a new low-cost RSC configuration for SMLIs. The proposed structure follows the SDCS concept with a novel sub-module, which will be introduced in section II. The proposed SDCS sub-module is able to create three positive voltage levels with a step of $2V_{dc}$ and includes four equal dc voltage sources, two unidirectional, and one bi-directional power switches. Following, to portray a basic circuit design for the proposed RSC-SMLI, the SDCS sub-module is incorporated into a new circuit configuration, which can involve two or three additional dc voltage sources alongside six unidirectional power switches. Therefore, without the conventional H-bridge cell, an output voltage of 13 levels and 15 levels with the same number of required power switches can be obtained. Afterwards, in order to define a generalized architecture, several proposed SDCS sub-modules are connected in series, and then they are put into the proposed basic design. The proposed generalized RSC-SMLI possesses a modular feature. A comparative study along with several experimental results is presented in section VII to verify the performance of the proposed SMLI.

2. Proposed SDCS Sub-module

Fig. 2 (a) shows the proposed SDCS sub-module configuration. Herein, four dc voltage sources with the contribution of three switching devices are arranged in such a way that three different voltage steps can be obtained at the output. In this case, S_{u1} and S_{u2} are unidirectional, while

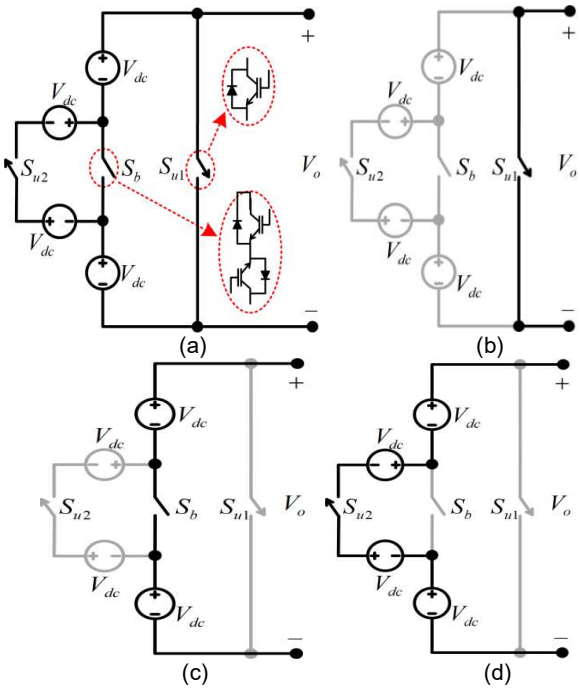


Fig. 2. *Proposed SDCS sub-module*
(a) main configuration, (b) at the first output voltage level, (c) at the second output voltage level, and (d) at the third output voltage level.

S_b operates as a bi-directional power switch. Clearly seen in Fig. 2(a), the back-to-back connection of two unidirectional power switches is adopted to represent a bi-directional power switch, which requires one gate driver. Thus, the proposed SDCS sub-module needs three gate drivers and four unidirectional power switches.

The current flowing paths of the three different output steps have also been depicted in Fig. 2(b)-(d). As it can be observed, only one power switch should be ON at each instant to create the possible state of the output voltage. In addition, it is clear that the PIV of S_{u1} and S_{u2} in the proposed SDCS sub-module is $4V_{dc}$, whereas the bi-directional power switch (S_b) should bear $2V_{dc}$ at the OFF-state. Therefore, the TSV of the overall circuit configuration will be $10V_{dc}$. It should be noted that the main objective of the proposed SDCS scheme is to optimally using the minimum count of active power switches that are switched among various isolated dc voltage sources. Therefore, this technique can properly control a considerable number of dc sources with a few number of required power switches.

It is worth nothing that since all the involved dc sources have the same magnitude in the proposed SDCS sub-module, they can easily be provided through single-input multi-output DC-DC converters [24],[25]. In respect to these techniques and regarding the polarity of the dc sources in the proposed SDCS sub-module, instead of applying four non-isolated dc sources, two isolated dc sources connected to two different single input two output DC-DC converters shown in Fig. 3 can be used in order to reduce the number of multiple required dc voltage sources. Here, the presented converter in Fig. 3 is suitable for the un-regulated dc sources

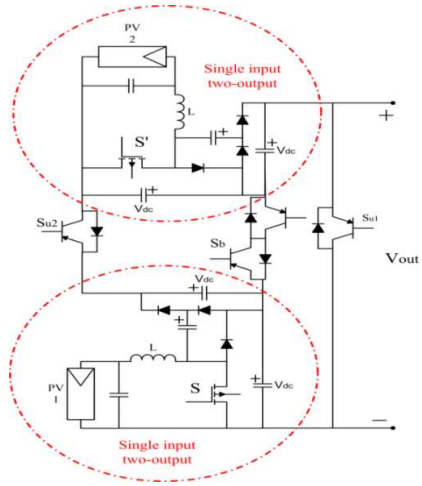


Fig. 3. Proposed SDCS sub-module when two single-input two-output are used as the dc sources

like PV panels. Details of working operation for this type of single-input two-output DC-DC converter used in the proposed SDCS are beyond the scope of this paper and it can be found in [25]. Here, the internal power switch of each DC-DC converter (S and S' in Fig. 3) can also be integrated in the maximum power point tracking (MPPT) operation for each PV panel. In this case, although several passive elements like power diodes, inductors and capacitors are incorporated into the proposed SDCS sub-module, the total number of required dc sources can be halved which can significantly decline the overall cost. It should also be noted that the ability of reduction in number of dc sources with the proposed schemes is only valid for those basic units whose their dc sources can be connected in series like what arranged for the proposed SDCS sub-module. It is clear that for the CHB-based SMLIs requiring isolated dc sources, this technology cannot be workable and instead their isolated dc sources have to be provided through the single input multi output line frequency transformer associated with the respective rectifiers. Therefore, the proposed scheme can be a suitable and practical choice for medium-voltage renewable energy (RE)-based applications, which demand less isolated dc sources.

3. Basic Design of The Proposed RSC-SMLI

In order to make a staircase output voltage with positive and negative polarities, a new RSC circuit topology of the SMLIs constructed on the basis of the proposed SDCS sub-module is presented in this section. As shown in Fig. 4(a) and (b), the basic design of the proposed RSC-SMLI can be made by integrating six unidirectional power switches and two or three same dc voltage sources with the same value in addition to the proposed SDCS sub-module. Observations in Fig. 4 indicates that the number of required switching devices is the same in both types of the proposed basic RSC-SMLI. However, they can generate an output voltage of 13 levels and 15 levels using only nine isolated gate drivers and 10 power switches. Therefore, compared to the conventional CHB-SMLI, the proposed RSC-SMLIs achieve 59.4% and 65% reductions in terms of required main power switches, when generating a 13-level and 15-level voltage, respectively. In addition, they can alternatively result a 62.5% and 67.8% reductions in the

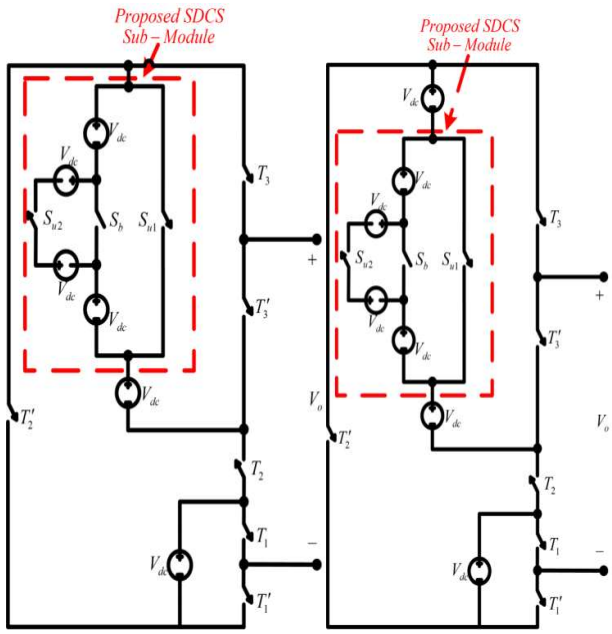


Fig. 4. *Proposed RSC-SMLI with (a) the 13-level basic design and (b) the 15-level basic design.*

number of required gate drivers in contrast to the conventional CHB-SMLI.

The ON-states of the proposed RSC-SMLI to generate the output voltage of 13 levels and 15 levels are listed in Table 2. As it is shown, by considering two ordinary IGBTs for a single bi-directional power switch, the maximum number of ON-state switches becomes five. Seen from this aspect, 58.3% and 64.3% reductions in the maximum number of ON-state current path switches can be obtained, when comparing with the conventional CHB-based SMLIs to generate the 13-level and 15-level voltage, respectively. Therefore, the total voltage drop across on the power switches of the proposed scheme can be acceptable, which can considerably diminish the overall conduction power losses.

Since the number of power switches has a remarkable reduction in both the proposed basic RSC-SMLI designs, different PIV ratings for the involved power switches can be obtained, similar to the cases of other RSC-SMLIs structures. In respect to Fig. 4(a) and (b), T_2 and T_2' withstand the maximum PIV with a value of $6\,V_{dc}$ and $7\,V_{dc}$ in the proposed 13-level and 15-level output voltage conditions, respectively. In this case, the number of ON- and OFF-switching for these power devices is only one per each cycle. Therefore, T_2 and T_2' can be switched at the line (fundamental) frequency, while the switching frequency of other involved power switches depends on the applied modulation strategies. From the PIV point of view, T_1 and T_1' are always bearing V_{dc} as the PIV, whereas the power switches of T_3 and T_3' offer $5\,V_{dc}$ and $6\,V_{dc}$ PIV for the proposed 13-and 15-level basic RSC-SMLI designs, respectively.

4. Proposed Generalized RSC-SMLI

Having the extended ability to create a higher number of output voltage levels is a common feature for the developed cases of RSC-SMLI structures. Considering this ability, a modular SMLI can be derived, which can improve the reliability of the overall system. Therefore, based on the basic designs for the proposed RSC-SMLI, two different versions of a generalized topology named as SMLI-G1 and SMLI-G2 can be obtained, as shown in Fig. 5 (a) and (b).

As it can be seen in Fig. 5, both of the proposed generalized SMLI, have n series-connected SDCS sub-module. In this case, by properly switching, as described in Section II, three positive output voltages (i.e., zero, $2\,V_{dc}$, and $4\,V_{dc}$) for each of the proposed SDCS modules can be produced. Since SMLI-G1 and SMLI-G2 adopt the same number of circuit components, the number of required insulated gate bi-polar transistors (IGBTs) and gate drivers can be expressed as:

$$N_{IGBTs} = 4n + 6 \qquad (1)$$

$$N_{Drivers} = 3n + 6 \qquad (2)$$

Because the only difference between the circuit architectures of SMLI-G1 and SMLI-G2 is the number of involved dc voltage sources, different output voltage levels can be generated. In this case, the number of required isolated dc voltage sources for both schemes is

$$N_{dc-G1} = 4n + 2 \qquad (3)$$

$$N_{dc-G2} = 4n + 3 \qquad (4)$$

TABLE 2 ON-Switching States for the Basic Structures of the Proposed RSC-SMLI.

No. States	On Switches	Output Voltage	
		13-level	15-level
1	T_1', T_2, S_{u2}, T_3	$6\,V_{dc}$	$7\,V_{dc}$
2	T_1, T_2, S_{u2}, T_3	$5\,V_{dc}$	$6\,V_{dc}$
3	T_1', T_2, S_b, T_3	$4\,V_{dc}$	$5\,V_{dc}$
4	T_1, T_2, S_b, T_3	$3\,V_{dc}$	$4\,V_{dc}$
5	T_1', T_2, S_{u1}, T_3	$2\,V_{dc}$	$3\,V_{dc}$
6	T_1, T_2, S_{u1}, T_3	V_{dc}	$2\,V_{dc}$
7	T_1', T_2, T_3'	V_{dc}	V_{dc}
8	T_1, T_2, T_3' T_1', T_2', T_3	0	0
9	T_1, T_2', T_3	$-V_{dc}$	$-V_{dc}$
10	T_1', T_2', S_{u1}, T_3'	$-V_{dc}$	$-2\,V_{dc}$
11	T_1, T_2', S_{u1}, T_3'	$-2\,V_{dc}$	$-3\,V_{dc}$
12	T_1', T_2', S_b, T_3'	$-3\,V_{dc}$	$-4\,V_{dc}$
13	T_1, T_2', S_b, T_3'	$-4\,V_{dc}$	$-5\,V_{dc}$
14	T_1', T_2', S_{u2}, T_3'	$-5\,V_{dc}$	$-6\,V_{dc}$
15	T_1, T_2', S_{u2}, T_3'	$-6\,V_{dc}$	$-7\,V_{dc}$

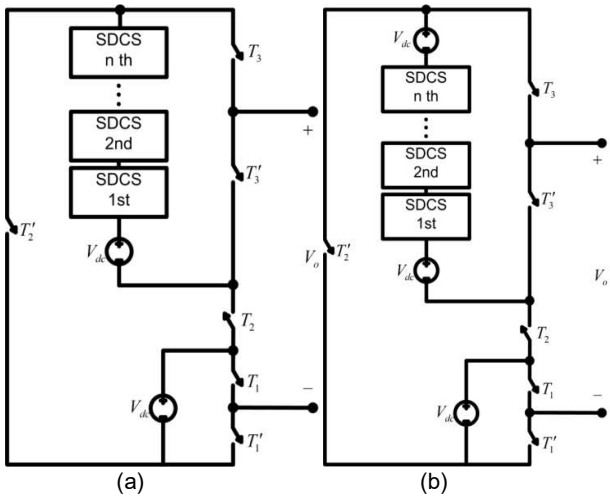


Fig. 5. *Proposed generalized structures (a) SMLI-G1 and (b) SMLI-G2.*

Similar to the basic designs of the proposed SMLI, the maximum number of ON-state power switches at each instant ($N_{ON,max}$) is the same for both structures. Thus, we have

$$N_{ON,max} = 2n + 3 \quad (5)$$

The possible number of output voltage levels for the proposed SMLI-G1 and SMLI-G2 can respectively be written as

$$N_{Level-G1} = 8n + 5 \quad (6)$$

$$N_{Level-G2} = 8n + 7 \quad (7)$$

On the contrary, in both cases, the PIV of T_1 and T_1' offers the same V_{dc}. However, the PIV of the middle pair switches (T_2 and T_2') for the proposed schemes in SMLI-G1 and SMLI-G2 are obtained as given in (8) and (9), respectively, while the PIV of pair switches (T_3 and T_3') for SMLI-G1 and SMLI-G2 is equal to (10) and (11), respectively.

$$PIV_{(T_2,T_2')-G1} = (4n + 2)\,V_{dc} \quad (8)$$

$$PIV_{(T_2,T_2')-G2} = (4n + 3)\,V_{dc} \quad (9)$$

$$PIV_{(T_3,T_3')-G1} = (4n + 1)\,V_{dc} \quad (10)$$

$$PIV_{(T_3,T_3')-G2} = (4n + 2)\,V_{dc} \quad (11)$$

Therefore, with (8)-(11), the TSV of the proposed SMLI-G1 and SMLI-G2 can be obtained as

$$TSV_{G1} = (24n + 8)\,V_{dc} \quad (12)$$

$$TSV_{G2} = (24n + 12)\,V_{dc} \quad (13)$$

5. Overall Cost Evaluation

The number of the required dc voltage sources is the same for each specific output voltage level in all the RSC-SMLI topologies, so the overall cost of each new circuit design of such converters can be assessed by considering the number of the required IGBTs and the gate drivers. In high-power-medium-voltage applications, the PIV of each involved power switch is also another important factor in the overall cost evaluations [26]. Typically, the minimum value of the PIV rating begins from 600 V in the IGBT modules [26], as shown in Table 3. Herein, it is clear that the price of IGBTs with different ranges of PIVs is different. Regarding different number of required power switches and gate drivers used for the recommended RSC-SMLIs in [13]-[23], a comprehensive survey from the overall cost view point is done in this section. Here, the main focus in the overall cost evaluation is based on some recently proposed topologies that are using the similar concept with multiple isolated dc voltage sources. Other multilevel based structures like multicell or neutral point clamp topologies are not using multiple dc voltage sources and their output voltage always is limited by a certain number of levels. Also, although they are using fewer number of dc sources, their additional requirements like charge balancing control procedures and use of many passive elements make some other challenges like extra cost, less reliability and non-modularity problems. Therefore, since the type of proposed topology is on the basis of multiple isolated dc sources SMLIs, some similar recently proposed structures have been chosen for comparison. Herein, to have a fair comparison, different IGBTs prices made by POWEREX industrial company with the nominal current of 100 A and 300 A has been enlisted in Table 3 based on the USD and as a role example [26]. All these types of IGBT modules are quite suitable for the inverter applications.

According to Table 3 and for two specific output voltages (13 and 23 levels) that can be generated by all the compared topologies, a cost comparison is done as summarized in Table 4. Two maximum amplitudes of the output voltage and nominal currents have been considered. Therefore, to reach a specific value of the maximum output voltage amplitude, the same number of the isolated dc voltage sources is used for each specific output voltage level among different SMLIs topologies. The number of the involved power switches should be compatible with their respective PIV ratings. In these cases, to estimate the overall cost of the required gate drivers, the VLA 500-01 hybrid IC IGBT deriver (40.72 USD) recommended by POWEREX has been considered.

TABLE 3 Prices of IGBTs with Different Ratings from POWEREX Co.

No	IGBTs Type	Ratings	Cost (USD) per 1/2 Module
1	CM 100DU-12F	600V-100A	42.26
2	CM100DY-24A	1200V-100A	45.21
3	CM100 DU-34KA	1700V-100A	75.35
4	CM300DU-12NFH	600V-300A	74.4
5	CM300DU-24NFH	1200V-300A	119.64
6	CM300DY-34A	1700V-300A	147.28

As clearly shown in Table 4, the proposed 13-level RSC-SMLI (Fig. 4(a)) with the nominal current being 100 A needs the lowest value of the total cost (IGBTs cost and drivers cost) among all the compared structures. In this case, to generate a 13-level output voltage with the peak being 1500 V, each involved dc source for all the mentioned topologies should be set at 250 V. Therefore, for the proposed 13-level RSC-SMLI, T_1 and T_1' in addition to the bi-directional power switch in the proposed SDCS sub-module, two back-to-back unidirectional power switches should bear the voltage of 250 V. Hence, four IGBTs with the PIV of 600 V are selected.

Also, S_{u1} and S_{u2} in the proposed SDCS sub-module are withstanding 1000 V. In return, two 1200-V IGBTs should be used thereby. Moreover, the pair switches of (T_3, T_3') and (T_2, T_2') offer 1250 V and 1500 V. Therefore, for these switches, IGBTs with the maximum PIV being 1700 V are used.

The reduction in the overall cost by the proposed RSC-SMLI can be further enhanced in the higher number of output voltage levels and in the higher range of nominal currents, as it can be observed in Table 4. Hereby, by employing two SDCS sub-modules in Fig. 4(b), only 14 IGBTs and 12 gate drivers are needed to produce a 23-level 1650 V output voltage. In this case, the nominal current of the power switches has been supposed to be 300 A. Therefore, as indicated in Table 4, the overall cost of the switching devices of the proposed structure is very low compared to the prior-art solutions. It should be noted that in Table 4 the cost of the required power diodes used in [15] and [23] has been ignored. However, the presented RSC-SMLI in [15] with such incorporated power diodes cannot pass the reverse inductive load current during the generation of each output voltage level, while the proposed RSC-SMLIs are suitable for any kinds of loading conditions.

6. Loss Analysis

Overall power losses of the proposed RSC-SMLI structure can be assessed by taking the switching and conduction losses into account. In the switching loss of such converters, the number of turn-on (N_{On}) and turn-off of the power switches (N_{OFF}) besides the rate of switching voltage (V_{sw}) at each instant of the output voltage are important. With a linear approximation between the passing current and the switching voltage across of a typical power switch, the dissipated energy during each turn-on and turn-off of the jth involved power switch can be obtained as [15], [22]

$$E_{On,j} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} \left[\left(\frac{V_{Sw,j}}{t_{on}} t \right) \left(-\frac{I_j'}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{SW,j} I_j' t_{on} \tag{14}$$

$$E_{OFF,j} = \int_0^{t_{Off}} v(t)i(t)dt = \int_0^{t_{off}} \left[\left(\frac{V_{Sw,j}}{t_{off}} t \right) \left(-\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt = \frac{1}{6} V_{Sw,j} I_j t_{off} \tag{15}$$

In which, t_{on} and t_{off} denote the delay time for turning ON and OFF of each power switch, I_j' and I_j are the current of each power switch before turning ON and after turning OFF, respectively. Since the load current usually passes from each typical power switch, these values will be equal with each other at each instant. Here, by considering λ as the supposed output voltage level at each instant and under the typical resistive loading condition (R_L), we can write:

$$|I_j| = |I_j'| = \left(\frac{\lambda V_{dc}}{R_L} \right) \qquad \lambda = 1, \ldots, \frac{N_{level} - 1}{2} \tag{16}$$

Therefore, the average value of the switching losses for each level of the output voltage and for each of the involved power switches is calculated by

$$P_{sw,j} = \frac{1}{6T} \left[t_{on} \left(\sum_{k=1}^{N_{on}} V_{sw,kj} \times |I_j'| \right) + t_{off} \left(\sum_{k=1}^{N_{off}} V_{sw,kj} \times |I_j| \right) \right] \tag{17}$$

Considering (16)-(17) and under the purely resistive loading condition for the proposed 13-level inverter, the total switching losses in relation within a full cycle of the output waveforms (T) can be obtained as

$$P_{sw,T} = \frac{67}{3T} \times \frac{V_{dc}^2}{R_L} (t_{on} + t_{off}) \tag{18}$$

TABLE 4 Overall Cost Evaluations of Different RSC-SMLIs Topologies.

	IGBTs 1700 V		IGBTs 1200 V		IGBTs 600 V		Drivers counts		IGBTs cost (USD)		Drivers cost (USD)		Total cost (USD)	
SMLIs	13L	23L	13L	23L	13L	23L	13L	23L	13L	23L	13L	23L	13L	23L
CHB	0	0	0	0	24	44	24	44	862.08	3273.6	977.28	1791.68	1839.36	5065.28
[17],[18]	0	0	0	0	14	24	14	24	502.88	1785.6	570.08	977.28	1072.96	2762.88
[14]	4	4	0	4	10	16	9	14	669.62	2258.1	366.48	570.08	1036.1	2828.18
[15]	4	4	2	0	6	11	12	15	611.36	1407.54	488.64	610.8	1100	2018.34
[16]	4	4	2	0	10	17	14	21	755.04	1853.94	570.08	855.12	1325.12	2709.06
[13],[19]	4	4	0	0	8	18	12	22	592.78	1928.34	488.64	895.84	1081.42	2824.18
[20],[23]	0	0	0	0	18	36	18	36	646.56	2678.4	732.96	1465.92	1379.52	4144.32
[21]	2	2	4	4	12	22	12	17	764.59	2409.93	488.64	692.24	1253.23	3102.17
[22]	2	2	4	4	8	18	10	15	620.91	2112.33	407.2	610.8	1028.11	2723.13
Proposed	**4**	**4**	**2**	**0**	**4**	**10**	**9**	**12**	**539.52**	**1333.14**	**366.48**	**488.64**	**906**	**1821.78**

Regarding the same calculations, the following equations for the total value of switching loss of the conventional 13-level CHB based SMLI can be expressed as:

$$P_{sw,T,CHB} = \frac{49}{3T} \times \frac{V_{dc}^{2}}{R_L}\left(t_{on} + t_{off}\right) \quad (19)$$

By comparing the relations mentioned in (18) and (19), one can be realized is that the total switching loss of the proposed 13-level RSC-SMLI is about 36% higher than its counterpart based on the conventional 13-level CHB-SMLI. Herein, this incremental trend for the total value of switching loss is usual since the total number of required power switches have been declined significantly by the proposed topology. By taking a look at Table 4, it can also be found that such reductions could contribute to about 50% decreases in the overall cost value in contrast to the CHB-SMLIs. Moreover, at the fundamental switching frequency, this mentioned difference of switching loss is not remarkable owing to the fact that a significant portion of total power loss belongs to the conduction losses.

On the other hand, the total conduction losses of the proposed RSC-SMLI pertains to the sum of conduction losses of the ON-state IGBTs ($P_{C,IGBT}$) and their anti-parallel diodes ($P_{C,D}$). By considering $R_{On,IGBT}$ and $R_{On,D}$ as the ON-state resistance of each IGBT and power diode and also taking $V_{On,IGBT}$ and $V_{On,D}$ as the ON-state voltage drop of each IGBT and power diode into account, the average $P_{C,IGBT}$ and $P_{C,D}$ within a full cycle of the output waveforms can be calculated by

$$P_{C,IGBT} = N_{C,ON}\left[\frac{2}{T}\int_{0}^{T/2}(V_{On,IGBT}I_L + R_{On,IGBT}I_L^{\beta+1})\,dt\right] \quad (20)$$

$$P_{C,D} = N_{C,ON}\left[\frac{2}{T}\int_{0}^{T/2}(V_{On,D}I_L + R_{On,D}I_L^{\beta+1})\,dt\right] \quad (21)$$

where $N_{C,ON}$ is the number of ON-state components (IGBTs or diodes) that are involved into the load current (I_L) path during the generation of each output voltage level, and β is a constant coefficient related to the characteristic of each IGBT/diode module. From (20) and (21), it is clear that with an assumption of the same IGBT modules for different topologies, the coefficient of $N_{C,ON}$ will be an important factor for evaluating the general performance of each RSC-SMLI structure in terms of conduction losses. In order to show the suitable condition of the proposed RSC-SMLI structure compared to others, the counts of $N_{C,ON}$ in each level of the output voltage and for different 13-level RSC-SMLI topologies have been listed in Table 5.

As it can be seen in Table 5, during the generation of the 4th and 5th levels of the positive and negative output voltage levels, the maximum number of ON-state components for the proposed 13-level RSC-SMLI is five, while within the two first levels of the output voltage, only three power switches should be ON. Here, although the presented structure in [14] requires four ON-state power switches in the middle output voltage levels, its overall switching cost is much higher than the proposed 13-level RSC-SMLI.

TABLE 5 A comparison of $N_{C,ON}$ for different 13-level RSC-SMLIs structures.

	Different output voltage levels						
SMLIs	0	$\pm V_{dc}$	$\pm 2V_{dc}$	$\pm 3V_{dc}$	$\pm 4V_{dc}$	$\pm 5V_{dc}$	$\pm 6V_{dc}$
CHB	12	12	12	12	12	12	12
[17], [18]	7	7	7	7	7	7	7
[14]	2	4	4	4	4	4	2
[15]	2	5	5	6	6	6	7
[16]	2	5	7	7	7	9	9
[13], [19]	2	6	6	6	6	6	6
[20]	9	9	9	9	9	9	9
[21]	3	5	5	5	7	7	7
[22]	3	5	5	3	5	5	3
[23]	12	11	10	9	8	7	6
Proposed	3	3	4	5	5	4	4

In order to further compare the overall conduction losses of the proposed 13-level RSC-SMLI in contrast to its CHB-based counterpart, a system with 1500 V 13-level output voltage and 100 A nominal current is considered as a role example. Regarding the PIV rating analysis of switches in the previous section and based on Table 3, the proposed topology requires four 600 V IGBTs, two 1200 V IGBTs and four 1700 V IGBTs modules. Considering the resistive loading condition and neglecting the non-linear terms of (20) and (21), the instant value of conduction loss for each of IGBT modules will be equal to $(R_{On,IGBT} + R_{On,D}) \times I_j^{\,2}$. Therefore, taking $N_{C,ON}$ given in Table 5 at each level of the output voltage contributes to the total value of average conduction loss per a full cycle of the output voltage as:

$$P_{Con,T} = \frac{2V_{dc}^{2}}{TR_L^{2}}\sum_{j=1}^{6}(j^2 K_j \Delta t_j) \quad (22)$$

Where, $K_j\,(i = 1,...,6)$ can be obtained as (23)-(25) and are the equivalent parasitic resistance put into the load current path based on the number of ON-state current path switches.

$$K_1 = R_{On,IGBT600} + R_{On,D600} + 2(R_{On,IGBT,1700} + R_{On,D1700}) \quad (23)$$

$$K_j = R_{On,IGBT600} + R_{On,D600} + 3(R_{On,IGBT1700} + R_{On,D,1700}) \quad (j = 2,5,6) \quad (24)$$

$$K_3 = K_4 = R_{On,IGBT600} + R_{On,D600} + R_{On,IGBT1700} + R_{On,D1700} + 2(R_{On,IGBT1200} + R_{On,D1200}) \quad (25)$$

Also, the term of $\Delta t_j (j = 1,...,6)$ in (22) is related to the time interval of different output voltage levels.

By considering the same calculations and regarding 12 ON-state power switches at each instant of the conventional 13-level CHB, its total average value of conduction power loss can be written as:

$$P_{Con,T,CHB} = \frac{24(R_{On,IGBT600} + R_{On,D600})V_{dc}^{2}}{TR_L^{2}}\sum_{j=1}^{6}(j^2\,\Delta t_j) \quad (26)$$

Hence, by taking Table 3 into account and regarding the data sheet of different IGBT modules at 100 A nominal

TABLE 6. A Comparative Summary of Power Loss Distribution for the Proposed 13-level Inverter and CHB-SMLIs

	Proposed 13-level SMLI			CHB 13-level SMLI		
$P_{out}[w]$	$P_{Con,T}[w]$	$P_{sw,T}[w]$	$P_{loss,T}[w]$	$P_{Con,T,CHB}[w]$	$P_{sw,T,CHB}[w]$	$P_{loss,T,CHB}[w]$
100	0.14	0.11	0.25	0.79	0.08	0.88
500	1.54	0.55	2.09	8.75	0.4	9.15
1000	13.8	1.1	14.9	78.8	`0.8`	79.6

current and 25° ambient temperature [26], the internal parasitic ON-state resistance ($R_{On,IGBT}$) of IGBT modules 600 V-CM 100DU-12F, 1200 V- CM100DY-24A, and 1700 V-CM100 DU-34KA are respectively 0.35Ω, 0.186Ω, and 0.14Ω. Also, the internal parasitic ON-state resistance of IGBT's antiparallel diode ($R_{On,D}$) for the mentioned switches are respectively, 0.7Ω, 0.34Ω and 0.24Ω.

Hence, it is clear that when the voltage rating of switches enhances, the internal ON-state resistance will be reduced. This feature is the main advantage of the proposed topology in contrast to the CHB-SMLI since only four 600 V IGBT modules has been used at the 1500 V 13-level output voltage, while this count is 12 in the CHB-SMLI and its effect is apparently obvious in (22) and (26). In the following, to exactly calculate the overall conduction loss of the proposed 13-level RSC-SMLI and 13-level CHB-based SMLI, the time intervals of different output voltage levels should be considered that are $\Delta t_1 = 0.52\,mS$, $\Delta t_2 = 0.53\,mS$, $\Delta t_3 = 0.57\,mS$, $\Delta t_4 = 0.7\,mS$, $\Delta t_5 = 0.91\,mS$ and $\Delta t_6 = 1.34\,mS$ at the 50 Hz output frequency. All of these values have been extracted from the simulation results. Therefore, by replacing such values along with the internal parasitic resistance of different IGBT modules in (22) and (26), we can write:

$$P_{Con,T} = \frac{0.4V_{dc}^2}{TR_L^2} \quad (27)$$

$$P_{Con,T,CHB} = \frac{2.27V_{dc}^2}{TR_L^2} \quad (28)$$

Regarding (27) and (28), it can be realized that a significant reduction in the count of total power switches of the proposed RSC-SMLI could lead to more than 85% reductions in the total average value of conduction loss in compare to the 13-level CHB-based SMLI. In order to better compare the overall percentage of switching and conduction losses in the proposed 13-level SMLI and its CHB-based counterpart, Table 6 can be taken into account. Here, three different operating points for 13-level 1500 V output voltage have been considered and as it can be seen, a significant portion of total power loss belongs to the conduction loss. Therefore, such considerable reduction in the total conduction loss is a great achievement of the proposed topology since not only could its overall cost be minimized but also its overall efficiency at the rated power is significantly improved.

7. Simulation and Experimental Results

In order to validate the general performance of the proposed RSC-SMLI structure, several simulation and experimental tests are performed. Here, the output waveforms of the proposed 13-level (Fig. 4(a)) and 15-level (Fig. 4(b)) RSC- SMLIs will be assessed. The results are presented in two subsections. In the first sub-section, some experimental results for the stand-alone operation of the proposed topologies will be shown, whereas in the second case study, the close-loop performance of the proposed topologies under the dynamic changes in the type of loads and modulation index are illustrated by the aim of PSCAD/EMTDC software.

7.1. First case study (Experimental results)

Regarding the symmetric configuration of the proposed circuits, the magnitudes of all the involved dc voltage sources are supposed to be 50 V. Therefore, based on the calculated PIV ratings of ten involved power switches, 600 V IGBT modules of CM600DU-12F are selected for the experimental setup. In addition, the fundamental switching frequency (50 Hz) has been chosen. The switching pulses are obtained from Table 2 and they have been saved in the PIC 18F452 microchip as a look-up table. Regarding this specification, Fig. 6 (a) and (b) show the 13-level output voltage at the no-load and purely resistive loading conditions besides at the purely inductive loading condition. As it can be observed, all the output voltage levels with the maximum amplitude being 300 V can be obtained, while under the loading condition, the obtained load current waveform has the maximum peak value of 2 A.

In addition, the output waveforms of the proposed 15-level RSC-SMLI under the inductive and resistive loading conditions have been illustrated in Fig. 7(a) and (b), respectively. As it can be observed, all the supposed output voltage levels with the maximum amplitude of 375 V can be generated, while the maximum values of the load current in both type of loading conditions are 2 A.

Furthermore, in the case of the proposed 15-level RSC-SMLI, the PIVs of all the involved power switches are demonstrated in Fig. 8. As it has been previously mentioned, the maximum PIV belongs to the two interconnected power switches (T_2 and T_2') with a value of 375 V. In addition, it is clear that except for the power switch S_b, all the power switches offer a PIV with a unidirectional polarity, while the power switch S_b in the proposed SDCS offers a bi-directional polarity with the maximum amplitude of 100 V. The low switching frequency of T_2 and T_2' over a full cycle of the output voltage waveform is another feature that can remarkably reduce the overall switching losses with the fundamental switching strategy (50 Hz).

7.2. Second case study (Simulation results)

To show the robustness of the proposed topology under different types of load and modulation indexes, some simulation results based on the proposed 15-level RSC-SMLI are presented in this subsection. In order to evaluate the performance of the output voltage and the load current

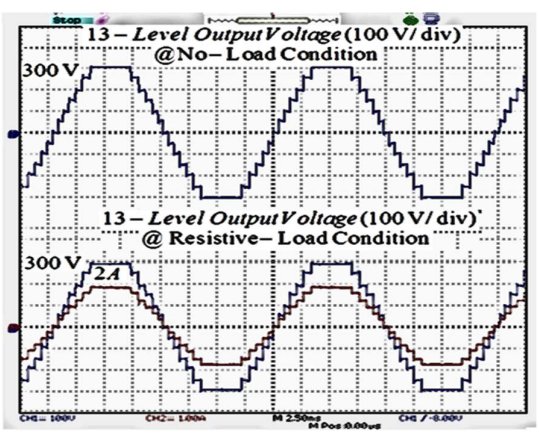
under different ranges of modulation indexes, an open loop control system based on the sinusoidal pulse width modulation (SPWM) technique is used. Details of this diagram are shown in Fig. 9 (a), while the modulation index for the proposed 15-level RSC-SMLI can be formulated by:

$$M = \frac{V_{ref}}{7V_c} \qquad (29)$$

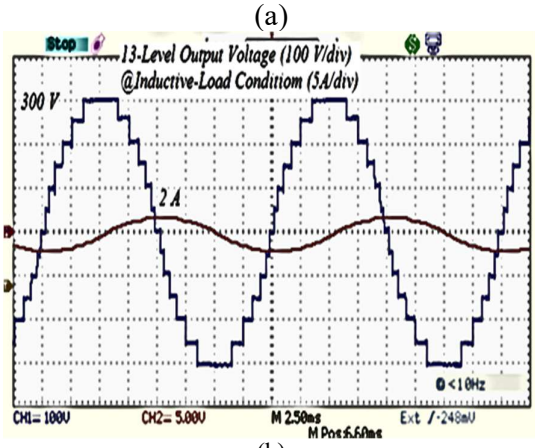
Where, V_{ref} and V_c are the amplitude of reference and each of carrier waveforms. Here, seven triangular high frequency carrier waveforms are used that should be compared by an absolute function of the reference sinusoidal wave. Hence, in order to distinguish each half cycle of the reference waveform resembling the shape of desired output voltage, a commander coefficient is used as CM [27]:

$$CM = \frac{1+\mathrm{sgn}(V_{ref})}{2} \qquad (30)$$

Therefore, if the switching frequency is to be chosen at 10 KHz and the type of load is to be assumed as R-L load with a value of 10 ohm and 0.3mH, the output voltage and load current can be seen in Fig. 9(b). In this case, the dc voltage value of all the dc-sources is assumed to be 65 V. As it is clear, by changing the value of modulation index, the number of output voltage levels will be varied but the load current maintains its quality and is quite compatible with any changes on the range of modulation index.

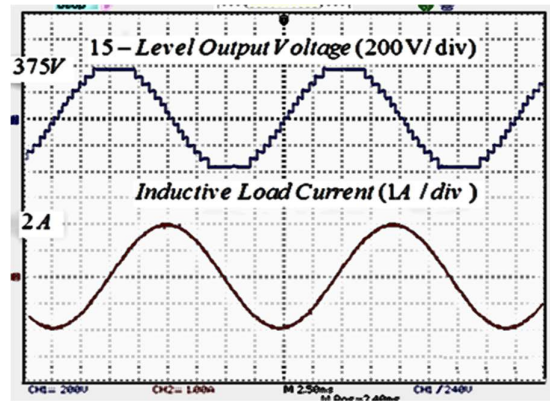


(a)

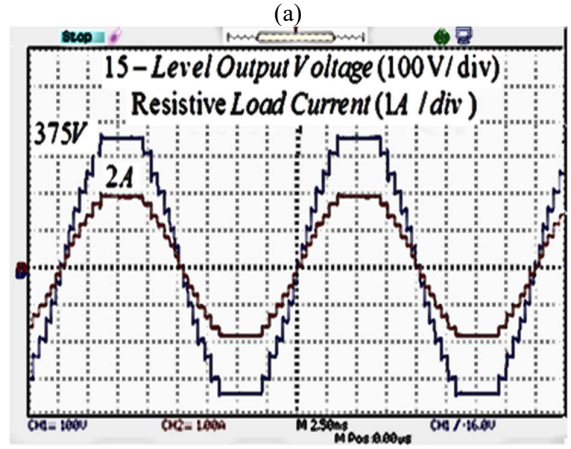


(b)

Fig. 6. *Output waveforms of the proposed 13-level RSC-SMLI structure. (a) at the no-load and under 2 A resistive load (b) under 2 A inductive load*



(a)



(b)

Fig. 7. *Output waveforms of the proposed 15-level RSC-SMLI (a) at purely inductive loading condition and (b) at purely resistive loading condition.*

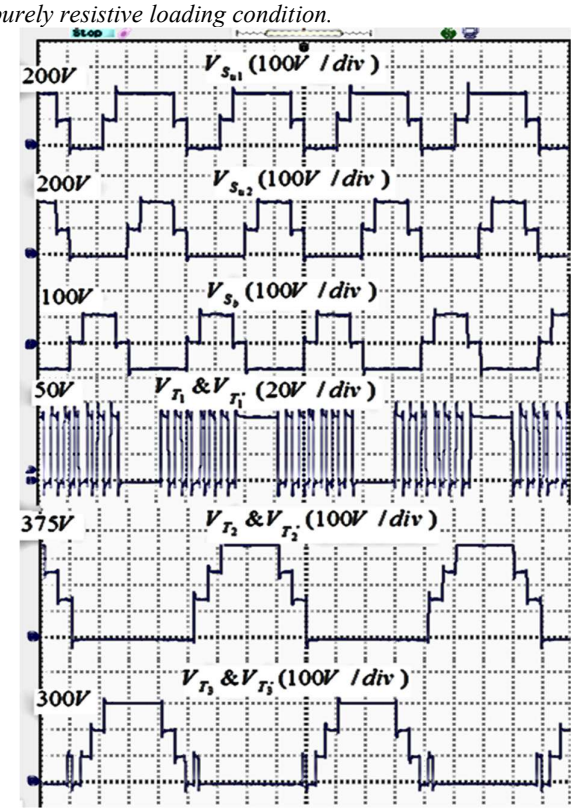


Fig. 8. *Observed PIV rating of different involved power switches in the proposed 15-level RSC-SMLI structure*

In the following, the proposed 15-level RSC-SMLI through a single inductor as a filter is directly connected to the ac grid. In this case, a close loop control strategy as shown in Fig. 10 (a) is used in order to inject an ac current into the grid and trigger the gate of power switches. As depicted in Fig. 10(a), a phase lock loop (PLL) block is required to detect the phase of grid's voltage. Also, the importance of L filter is as for providing a slight phase difference between the inverter output voltage and the grid voltage's phase to inject the inverter power into the grid. Owing to use of 15-level SMLI inverter in grid connected application, a small size of first-order L filter can properly alleviate the concern of integrating the second-order LCL low pass filters. So, additional measures in suppressing the possible resonant between the grid side inductance and the filter side capacitor can also be avoided [28].

Regarding Fig. 10 (a), the desired reference waveform used in the SPWM technique is made by comparing the actual current demanded by the grid ($I_g^* \sin(\theta+\theta^*)$) with the inverter output current (i_g). Then this difference is sent to a proportional-resonant (PR) controller to proper adjust the level of reference waveform for modulation process. In this case, the transfer function of the PR controller in the Laplace domain is:

$$G_{PR}(S) = K_P + \frac{2K_i\omega_c S}{S^2 + 2\omega_c S + \omega_c^2} \quad (31)$$

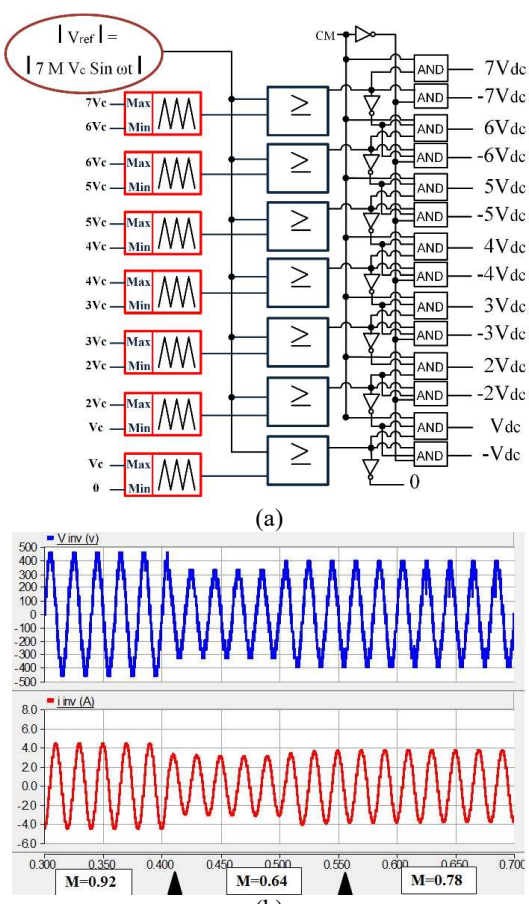


Fig. 9. Impact of modulation index on the output performance of the proposed 15-level RSC-SMLI (a) Overall SPWM procedure (b) output voltage and current waveform

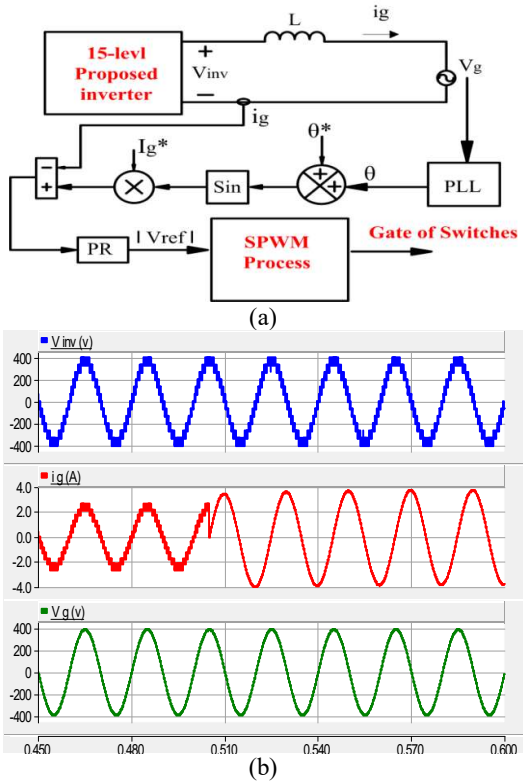


Fig. 10. Grid-connected application of the proposed 15-level RSC-SMLI (a) control procedure (b) inverter output voltage, grid current and grid voltage waveforms.

The reason of choosing the PR controller instead of the conventional proportional-integral (PI) controllers is for its ability to properly cancel any steady state error during the dynamic changes in the value of injected output current [1], [29].

Regarding the above mentioned control scheme and by selecting all the dc sources value on 65 V which is quite suitable for obtaining the desired maximum output voltage compatible with the local 50 Hz/220 V rms grid, the 15-level inverter voltage along with the grid current and its voltage waveform are demonstrated in Fig. 10(b). Hereby, the parameters of PR controller are set as $K_p = 2$, $K_i = 300$ and the cut of frequency(ω_c) is set as $2\pi \times 5000 rad/s$, whereas the value of output inductor is about 5mH. The details of providing such parameters for the PR controller are beyond the scope of this paper and can be found in [28]. As it can be seen, 15-level output voltage could be precisely generated during the injection of power into the grid. Also, as shown in this figure, through changing the angle of θ^* in the controller block, the inverter is capable of injecting the reactive power with a lagging power factor of 0.84. Here, appropriate dynamic performance of the proposed topology can be confirmed and the range of output power for unity power factor is about 400 W, while with the reactive power exchange, the amount of active and reactive powers are respectively 478 W and 92 VAR.

8. Conclusion

A new low-cost RSC-SMLI configuration has been presented in this paper. The proposed structure employs a

novel SDCS sub-module that can control the dc-link voltage of four isolated dc voltage sources with three power switches. By a series connection of the proposed SDCSs integrated into a new circuit configuration, a considerable number of output voltage levels with a reduced number of required power switches can be obtained. The overall cost evaluations of the proposed topology have been also conducted in this paper. The power loss analysis was developed which proves that the proposed structure has an acceptable condition in reduction of the maximum number of involved power switches in the load current path as well as conduction losses. Finally, simulation and experimental results were provided in this paper, which verified the overall performance of the proposed RSC-SMLI topology.

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