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Dragievi, Tomislav

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Dynamic Stabilization of DC Microgrids with Predictive Control of Point of Load Converters

Tomislav Dragičević, *Senior Member, IEEE*

***Abstract*—This paper investigates the possibility of deploying a finite control set model predictive control (FCS-MPC) algorithm for dynamic stabilization of a dc microgrid that supplies tightly regulated point-of-load (POL) converters. Within their control bandwidth, such converters behave as constant power loads (CPLs), where the microgrid sees them as impedances with a negative incremental resistance. Due to this characteristic, POL converters have a destabilizing impact which may cause large voltage oscillations or even a blackout of the whole microgrid. This paper proposes an active damping method realized by introducing a stabilization term in the cost function of the FCS-MPC algorithm that is used for regulation of the POL converter. This approach, on one hand, stabilizes a dc microgrid without implementing any additional active or passive components, thus providing higher energy efficiency and better cost-effectiveness than methods which rely on such components. On the other hand, when compared to other approaches that focus on dc link stabilization via POL converter control, the proposed method has a significantly lower influence on the load voltage regulation performance. These findings are confirmed through comprehensive analytical investigation that shows how the proposed stabilization term affects the input impedance of the POL converter and the load voltage tracking performance. This is followed by experimental validation, where an FCS-MPC regulated UPS inverter was used as a particular CPL example.**

***Index Terms*—Finite control set model predictive control (FCS-MPC), constant power load (CPL), dc microgrid (MG), stability, impedance analysis.**

I. Introduction

CONTINUED development of power electronics technology has over the past several decades led to a situation where a large part of electrical power today is processed by power electronic converters. They are widely used in renewable energy generation, electrical power transmission and transportation, while the share of consumer electronics is starting to dominate the total distribution grid loading [1]–[3].

Most of the electric power today is produced and distributed in the alternating-current (ac) form. However, a common characteristic of the vast majority of power converters used in practical applications is that electricity appears in a direct-current (dc) form at a certain stage of their power conversion chains [4]. Therefore, in power electronic intensive systems that may comprise many converters, the number of back and forth ac-dc and dc-ac conversions can be significantly reduced if converters use a common dc interface. In this way, not only the efficiency and reliability of such systems can be improved, but also the integration of renewable and energy storage systems can be simplified since many of these technologies are inherently dc [5]. An additional benefit of dc systems is that they are fairly simple to control as there are no synchronization issues, reactive power flows and phase unbalances [6]. All these benefits have recently led to a tremendous surge of interest in dc distribution systems and microgrids [7].

The majority of end-users in dc microgrids are electronic loads that employ point-of-load (POL) converters for power conditioning and voltage regulation. Due to their active regulation capability, such loads are able to extract steady power even under varying voltage at the microgrid side, and are thus commonly referred to as constant power loads (CPLs) [8]. An interesting characteristic of a CPL is that its incremental input impedance is negative. Thus, it tends to destabilize the system to which it is connected.

This challenge has been known for a long time, and was commonly analyzed using an impedance based approach, which points out that the minor loop gain, i.e. the ratio between the source and load impedances Z_{out} and Z_{in}, plays a key role in determining the system's stability [9]–[12]. Therefore, by properly shaping either one or both of them, good and stable performance can be ensured. In general, there are three possible approaches to do this; passive or active damping of Z_{out}, and active damping of Z_{in}. Damping of Z_{out} requires either an installation of additional passive components [13], [14], or availability of actively controlled power electronic converters at the source side [15]–[19]. However, additional passive components increase the size of the system and cause losses, while numerous industrial applications of dc microgrids tend to use passive front-end converters [7]. In such applications, addition of active converters solely for stabilization purposes is usually too costly to be justifiable.

On the other hand, only control effort is needed to shape Z_{in} and the aforementioned negative effects are avoided. However, when a POL converter is regulated by cascaded linear control loops and a pulse width modulator (PWM), modification of Z_{in} can only be done by reducing the loop gain of the control system, which inevitably degrades the load regulation performance [20]–[22]. An approach that can to some extent reduce this problem was reported in [23]–[25], where authors proposed to deploy the stabilization feedback signal directly to the PWM. In this way, the stabilization signal has less effect on other control loops, thus allowing somewhat better trade-off between dc-link stability and load dynamic performance. However, if these loops are avoided, the converter can easily enter over-modulation or even get tripped since the current limiting functionality is lost. What

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T. Dragičević is with the Department of Energy Technology, Aalborg University, 9220 Aalborg East, Denmark (e-mail: tdr@aau.dk).

is more, the converter's bandwidth is in both cases limited by the controller's sampling rate that has a locked ratio to the switching frequency. In particular, sampling frequency can be either the same or double than the switching frequency (e.g. see Section 2.2.3. in [26]).

Inspired by the shortcomings of the state-of-the-art dc microgrid stabilization methods summarized above, this paper takes a fundamentally different approach. Firstly, it proposes to use finite control set model predictive control (FCS-MPC) for the regulation of the POL converter. In clear contrast to cascaded linear control loops and PWM, this method directly manipulates the converter's switches. More specifically, a model of the converter is used to predict its future behavior for all possible voltage vectors, where the one that minimizes a certain cost function (CF) is applied to the converter at every sampling step [27]. This means that the switching is now not restricted to a predetermined switching pattern of the PWM, but is flexibly adjusted to the operating conditions. Therefore, the sampling rate can be significantly higher than the average switching frequency, which allows much better transient response and a similar steady-state performance compared to linear control methods [28]. Furthermore, FCS-MPC is characterized by extreme robustness to parameter variations. For instance, robustness to more than $100\ \%$ control parameter mismatch was showed in [28] for the POL converter, which is a significant gain over linear control methods where control parameters need to be carefully tuned to ensure stability (see e.g. [29]). Finally, due to its CF based control, FCS-MPC allows simple controllability of nonlinear systems, as well as seamless integration of multiple control objectives and constraints [30]. For all these reasons, FCS-MPC has in recent years been applied to a wide range of power electronic applications [31]–[35].

In this paper, a new CF for control of the POL converter with embedded dc link stabilization term is proposed. Such a CF ensures a stable dc microgrid, but also does not compromise the good load regulation performance nor the safe operation of the converter. As it will be shown, this approach automatically shapes Z_{in} with respect to designed CF and according to the system's operating conditions in order to fulfill the performance objectives. To this end, when there are oscillations in the dc link, the stabilization term shapes Z_{in} to ensure the designated damping. On the other hand, when the dc link is stabilized, the stabilization term has a minor influence on the value of the CF and the ac voltage tracking term plays a dominant role. Indeed, this capability of FCS-MPC to flexibly balance the two conflicting control objectives leads to significantly improved performance compared to the state-of-the-art POL converter control methods.

The paper is organized as follows. In Section II, a generic structure of a dc microgrid is described and it is shown how such a structure can be represented by an impedance model consisting of Z_{out} and Z_{in}. Then, some common stability criteria that restricts the relation between these impedances are discussed. Several conventional stabilization approaches that are able to meet the respective criteria are presented in Section III, where their advantages and drawbacks are also critically assessed. This discussion leads to a motivation for using the FCS-MPC in the POL converter control system. Basic FCS-MPC principles and the proposed stabilization approach are introduced in Section IV. Design guidelines for the weighting factor of the stabilization term, as well as a detailed analytical investigation of its influence on the performance of the system are presented in Section V. Section VI provides the experimental verification using an UPS inverter that acts as a CPL, while conclusions of the paper are given in Section VII.

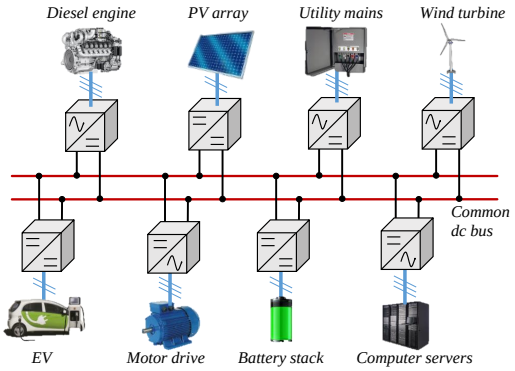


Fig. 1. A typical dc microgrid architecture.

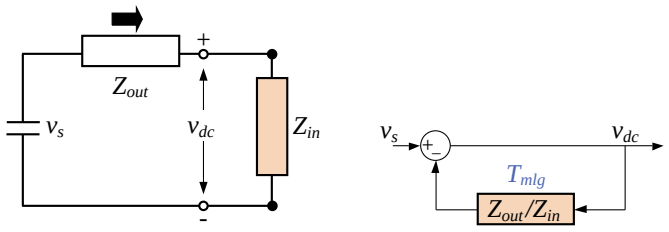
II. System Description

A broad class of modern grid-connected and autonomous power distribution systems can be categorized as dc microgrids. Some examples include electric vehicles (EVs) and EV charging stations, smart dc homes, future shipboard and aircraft power systems, data centers, and others [7]. Fig. 1 shows a generic dc microgrid that illustrates the basic structure, valid for all of these systems. It consists of one or more power sources, a common dc bus, and a variety of possible loads.

Sources, which are given in the section of the figure above the common dc bus, can be active or passive. On the other hand, the majority of end-users in the section below are electronic loads that employ point-of-load (POL) converters for power conditioning and voltage regulation. Such loads are often referred to as CPLs since their consumed power, within the bandwidth of the POL converter controller, is independent from voltage variations in the dc microgrid. Constant power behavior implies that the current drawn by the POL converter will change in the direction opposite of the dc bus voltage, i.e. rising voltage will result in a falling current and vice versa. This leads to a phenomenon where the input impedance of such a converter behaves as an incremental negative resistor, which has a destabilizing effect on the system [8]. It is thus worthwhile to investigate this effect in order to understand the necessary conditions for stable operation of dc microgrids.

A. Impedance Model of a DC Microgrid

For the sake of understanding the stability of a dc microgrid, one possibility is to construct the equivalent Thevenin circuit of the system given in Fig. 1. In order to do this, the microgrid can be split into two parts – a power supply part which



(a) Equivalent Thevenin circuit. (b) Equivalent block diagram.

Fig. 2. Equivalent Thevenin circuit and a block diagram of a dc microgrid with aggregated output impedance of the source side, Z_{out} and aggregated input impedance of the load side, Z_{in}.

corresponds to the section of the figure above the common dc bus, and a load part that corresponds to the section below. As elaborated in [36], the overall power supply part can then be represented by a single voltage source v_s and an output impedance Z_{out}, whereas the effects of all loads can be aggregated within a single input impedance Z_{in}. A block diagram of the Thevenin's representation of the microgrid is given in Fig. 2. The dynamics of such a system can be described by the ratio Z_{out}/Z_{in}, which is commonly referred to as the minor loop gain T_{mlg} [9]–[12]. The following relation is valid:

$$v_{dc} = v_s \cdot \frac{Z_{in}}{Z_{in} + Z_{out}} = v_s \cdot \frac{1}{1 + \underbrace{Z_{out}/Z_{in}}_{T_{mlg}}}. \qquad (1)$$

It can be immediately appreciated from (1) that T_{mlg} plays a major role in stability. The following subsection describes some criteria that T_{mlg} needs to fulfill to ensure the stability and good dynamic response of the system.

B. Stability Criteria

Under the assumption that both Z_{out} and Z_{in} are linear, the necessary condition for stability of (1) is that all the poles of $1/(1 + T_{mlg})$ are located in the left-half plane. This is equivalent to saying that T_{mlg} satisfies the Nyquist stability criterion. It should be noted that the latter stability criteria formulation is more frequently used since it is more intuitive and is also applicable to nonlinear systems under certain assumptions. Namely, if a certain sinusoidal perturbation signal that is applied to a nonlinear element always excites a sinusoid at the same frequency in the output, then such an element can be represented by its linear "equivalent" frequency response, which is also commonly called a describing function (DF) (see chapter 5 in [37]). As a result, standard frequency domain techniques can be used to assess the stability and stability margins of the systems which comprise a nonlinear element that can be represented by DF (e.g. as in chapter 18 of [38]). Indeed, the DF method will turn out to be an essential tool for characterizing the effects of nonlinear Z_{in} on stability of the system in Section V-A of this paper. For this purpose, the DF of Z_{in} will be measured using the standard methodology discussed in e.g. [39].

It is important to notice that it is usually not enough only to ensure the stability of the system, but also to have sufficient stability margins. Numerous criteria have been proposed in the literature that impose certain constraints on the magnitude and phase of T_{mlg} in the frequency domain. These constraints are defined by a so-called forbidden region for the polar plot of T_{mlg}. If T_{mlg} is designed to meet any of these criteria, the overall system is guaranteed to have stability margins associated with the given forbidden region. A more detailed discussion about these criteria can be found in the literature (e.g in [6] and [36]).

The following section discusses a number of approaches with which the fulfillment of stability criteria can be achieved. Advantages and drawbacks of those methods are discussed, resulting in the motivation to develop a new improved stabilization strategy, which is described in detail in Section IV.

III. Conventional Stabilization Approaches

It has been shown in the previous section that the mismatch of impedances around a common bus is the root cause of instability in dc microgrids. This situation can be avoided by properly shaping these impedances to ensure that their ratio, i.e. T_{mlg}, satisfies the Nyquist stability criterion as a necessary condition. As discussed before, T_{mlg} could also be designed to comply with some of the more strict criteria defined in [6], [36] that can impose mandatory stability margins of the system. In any case, there are three general ways of achieving this, as described below.

A. Passive Damping of Z_{out}

Passive damping is based either on increasing the capacitance of the dc bus or on connecting additional resistor banks in series and parallel with the capacitors and inductors. The aim is to reduce the resonance peak of Z_{out} and avoid its interaction with Z_{in}.

Increase of the dc link capacitance usually requires the usage of electrolytic capacitors that, although cheaper, also have a large volume and weight, and are inferior to small film capacitors in terms of reliability and efficiency [40]. Therefore, it is often advantageous to use film capacitors in industrial applications that have stringent reliability requirements or limitations in permissible footprint. On the other hand, the addition of damping resistors is a very robust and effective solution to achieve stabilization, but it introduces losses in the system and hence reduces its energy efficiency [13], [14].

B. Active Damping of Z_{out}

Another possibility to shape Z_{out} is by actively controlling the active-front end interface or power conditioning modules, if they are available. These components are normally dc-dc or ac-dc power electronic converters that have only a minor negative impact on the total efficiency and can effectively reduce the resonance peak of Z_{out}. A proportional control of active front-end was proposed in [16], [17], and a control of power-conditioning module in [18]. Another research approach is to actively regulate the voltage of a dc microgrid with droop control strategy implemented in one or more active-front ends [15], [19]. Compared to simple voltage regulators, droop

control provides additional damping effect and it also allows power sharing between multiple converters at the same time. It should be noted that droop has been first proposed to allow adaptive voltage positioning functionality in microprocessor power supplies [41]. This research has shown that with the proper control design, droop regulation can completely flatten the resonance peak in Z_{out} and thus mitigate the instability effects associated with CPLs.

C. Active Damping of Z_{in}

The active-front end interface is not available in numerous industrial applications of dc microgrids, in which only unidirectional power flow is required. Examples are data centers, electric vehicle charging stations and industrial multi-motor drives [7]. In such applications, it is usually also not justifiable to install costly power conditioning modules only for stabilization purposes because they add to the total number of active components in the system and thereby reduce the economic prospects and reliability of the whole system. Therefore, a very common scenario in practical applications is that the power supply is a passive front-end rectifier with an LC filter [9]–[12], [17], [42], [43].

An example of a passive front-end configuration is shown in Fig. 3, where a two-level VSC feeding a stand-alone ac load is supplied from a passive front-end interface. Here, Z_{out} can be calculated as follows:

$$Z_{out} = \frac{R_{dc} + sL_{dc}}{s^2 L_{dc} C_{dc} + sC_{dc} R_{dc} + 1}, \tag{2}$$

where L_{dc} is the filter inductor, C_{dc} is the filter capacitor, and R_{dc} is a resistance in series with the inductor. It can be seen that such a configuration is the most unfavorable from the stability point of view since Z_{out} is the undamped impedance of the LC filter.

To stabilize this system without adding any additional components, active control of the POL converter that shapes Z_{in} can be adopted. One possibility to do that is by introducing a stabilization feedback in the POL converter's cascaded linear control structure. However, this approach has two drawbacks. Firstly, stabilization is not even possible if the resonance frequency of Z_{out} is higher than the bandwidth of the loop where the stabilization signal is applied, which is a realistic scenario when a small dc link capacitor is used. On the other hand, even if the bandwidth is sufficient, stabilization of the dc link can only be achieved by degrading the load regulation dynamics [20]–[22]. The implementation of the stabilization signals directly to the PWM has been proposed to reduce this problem [23]–[25]. Yet, since the stabilization signal is now fed after the current control and limiting loop, the POL converter could easily enter over-modulation or even get tripped under some transient conditions.

Finally, all of the Z_{in} shaping strategies described above are designed for the specific parameters of the system (i.e. the resonant frequency of Z_{out} is assumed to be known), so the applicability to other system parameters and configurations is not clear. In addition, the bandwidth of the POL converter is in all these cases limited by the control sampling rate that has a locked ratio to the switching frequency. Therefore, the flexibility to balance different control objectives is restricted as well, as evident from the trade-off between dc link dynamics and load regulation performance that is a major drawback of state-of-the art techniques.

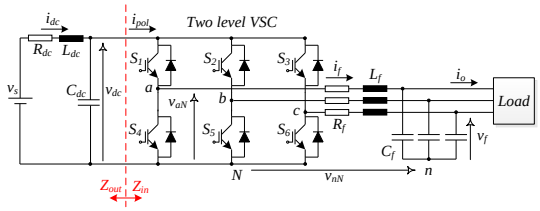


Fig. 3. A constant power load (CPL) case study: Two-level VSC fed from a dc link bus and supplying an ac load.

IV. Proposed FCS-MPC Based Stabilization Approach

Motivated by the drawbacks of the state-of-the-art stabilization approaches discussed in previous section and summarized in Table I, a new methodology is introduced here as an alternative solution for regulating the POL converter. This method should allow stable control of the dc link with negligible effect on the load regulation performance, while simultaneously operating the converter within the safe limits. Control of the POL converter based on FCS-MPC methodology that leads to this is proposed in the following.

A. FCS-MPC Operating Principle

Derivation of the converter model and design of the CF are the two key steps required to realize the FCS-MPC controller. Following the same approach as in [28], the VSC is modeled in a stationary α-β reference frame. In that sense, all the generic three-phase variables x_a, x_b and x_c, are transformed into a corresponding α-β frame by applying an amplitude-invariant Clarke transformation $\mathbf{T}$:

$$\bar{x} = x_\alpha + jx_\beta = \mathbf{T}\,[x_a \;\; x_b \;\; x_c]' \tag{3}$$

where

$$\mathbf{T} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix}. \tag{4}$$

The topology of the two level VSC, which is used in this paper to emulate the CPL, is presented in Fig. 3. The three gating signals S_a, S_b and S_c determine the voltage vector of the converter.

Since there are three legs and each leg can be in two states, the overall converter can be in one out of $2^3 = 8$ voltage vectors. The potential of the middle point of any inverter leg with respect to the point N can be obtained by multiplying v_{dc} with the associated gating signal, as $v_{aN} = S_a \cdot v_{dc}$, $v_{bN} = S_b \cdot v_{dc}$ and $v_{cN} = S_c \cdot v_{dc}$. Only a part of these voltages reach the output LC filter. To be more precise, there exists a common mode voltage drop v_{nN} that results in reduced voltage across

TABLE I
COMPARISON BETWEEN DIFFERENT STABILIZATION METHODS

	Cost-effectiveness	Energy efficiency	Load performance
Passive damping of Z_{out} [13], [14]	Additional passive components are needed	Reduced	Not affected
Active damping of Z_{out} [15]–[19], [41]	Active-front end or additional active components are needed	Slightly reduced	Not affected
Active damping of Z_{in} by stabilization signals applied in the control loops [20]–[22]	No additional active or passive components are needed	Not affected	If stabilization is possible, load dynamics are inevitably reduced
Active damping of Z_{in} by stabilization signals applied directly to PWM [23]–[25]	No additional active or passive components are needed	Not affected	Dynamics are somewhat improved compared to approach above, but the POL converter can enter over-modulation or get tripped
Proposed FCS-MPC based active damping of Z_{in}	No additional active or passive components are needed	Not affected	Excellent dynamics and safe load operation

TABLE II
COMPLEX VOLTAGE VECTORS USED IN TWO-LEVEL THREE-PHASE VSC

S_a	S_b	S_c	Voltage vector $\bar{v}_i$
0	0	0	$\bar{v}_0 = 0$
1	0	0	$\bar{v}_1 = \frac{2}{3}v_{dc}$
1	1	0	$\bar{v}_2 = \frac{1}{3}v_{dc} + j\frac{\sqrt{3}}{3}v_{dc}$
0	1	0	$\bar{v}_3 = -\frac{1}{3}v_{dc} + j\frac{\sqrt{3}}{3}v_{dc}$
0	1	1	$\bar{v}_4 = -\frac{2}{3}v_{dc}$
0	0	1	$\bar{v}_5 = -\frac{1}{3}v_{dc} - j\frac{\sqrt{3}}{3}v_{dc}$
1	0	1	$\bar{v}_6 = \frac{1}{3}v_{dc} - j\frac{\sqrt{3}}{3}v_{dc}$
1	1	1	$\bar{v}_7 = 0$

the filter. This voltage can be obtained by taking into account the voltage balance in the system:

$$v_{nN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3}. \tag{5}$$

The voltages across the filter are then given as $v_{an} = v_{aN} - v_{nN}$, $v_{bn} = v_{bN} - v_{nN}$ and $v_{cn} = v_{cN} - v_{nN}$. Finally, the Clarke transformation, given in (3)-(4), is applied to the filter voltages for all possible gating signal combinations, to obtain their expressions in the stationary α-β frame.

These voltage vectors, represented as $\bar{v}_i$, are summarized in Table II. As mentioned before, they represent the 8 possible voltage vectors that can be applied to the LC filter, which is composed of inductance L_f with a series resistance R_f, and a capacitance C_f. The differential equations that describe the dynamics of the inductor current $\bar{i}_f$ and capacitor voltage $\bar{v}_f$ are as follows:

$$\begin{aligned} L_f \frac{d\bar{i}_f}{dt} &= \bar{v}_i - \bar{v}_f - R_f \bar{i}_f \\ C_f \frac{d\bar{v}_f}{dt} &= \bar{i}_f - \bar{i}_o \end{aligned} \tag{6}$$

where $\bar{i}_o$ is the output current.

For convenience, (6) can be expressed in the state-space form as:

$$\frac{d}{dt}\begin{bmatrix} \bar{i}_f \\ \bar{v}_f \end{bmatrix} = \mathbf{A}\begin{bmatrix} \bar{i}_f \\ \bar{v}_f \end{bmatrix} + \mathbf{B}\begin{bmatrix} \bar{v}_i \\ \bar{i}_o \end{bmatrix} \tag{7}$$

where

$$\mathbf{A} = \begin{bmatrix} -\frac{R_f}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix} \tag{8}$$

and

$$\mathbf{B} = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & -\frac{1}{C_f} \end{bmatrix}. \tag{9}$$

Apart from relations that describe the load filter side, dynamics are also present on the dc side, as shown in the Fig. 3. Namely, the inductance L_{dc} in series with the resistance R_{dc} is connected between the stiff voltage source v_s, and the dc filter capacitance C_{dc}. In this paper, only a differential equation describing v_{dc} is used for modeling of the dc link dynamics, and the current i_{dc}, which flows through the inductor, is treated as an external disturbance:

$$C_{dc}\frac{dv_{dc}}{dt} = i_{dc} - i_{pol}. \tag{10}$$

The main reason for validity of representing the dc current as a disturbance is a rather high value of dc inductor, as well as the continuous nature of the dc source voltage and the dc link voltage, which all make the change of dc inductor current negligible during the sampling step of 25 μs. To this end, this current can be assumed constant between the two inter-sampling periods. In (10), i_{pol} is the current flowing into the UPS inverter. It can be synthesized from the filter currents and the gating signals, as:

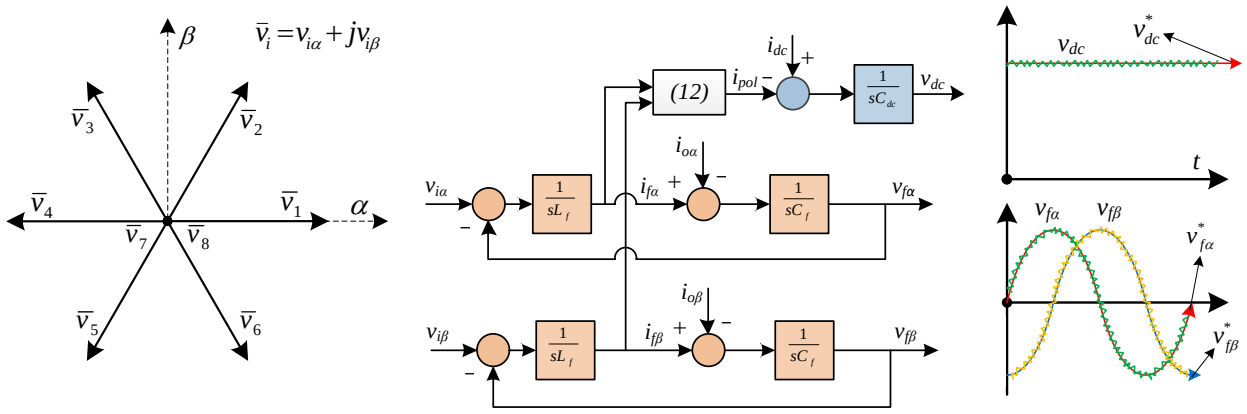
$$i_{pol} = S_a i_{fa} + S_b i_{fb} + S_c i_{fc}. \tag{11}$$

For consistency, (11) can also be represented using complex variables, as follows:

$$i_{pol} = \begin{bmatrix} S_a & S_b & S_c \end{bmatrix} \mathbf{T}^{-1} \begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix}. \tag{12}$$

The equations above completely define the continuous state-space model of a two-level three-phase VSC with dynamics on both the ac and dc sides. The zero-order hold (ZOH) discretization method is used to obtain $\mathbf{A_d}$ and $\mathbf{B_d}$ from (8) and (9). This method ensures that the discrete-time model coincides with the continuous model at the sampling instants and is thus suitable for digital control implementation. The discrete model on the ac side is as follows [28]:

$$\begin{bmatrix} \bar{i}_f(k+1) \\ \bar{v}_f(k+1) \end{bmatrix} = \mathbf{A_d}\begin{bmatrix} \bar{i}_f(k) \\ \bar{v}_f(k) \end{bmatrix} + \mathbf{B_d}\begin{bmatrix} \bar{v}_i(k) \\ \bar{i}_o(k) \end{bmatrix} \tag{13}$$



(a) Possible voltage vectors of a two-level VSC that correspond to Table II.

(b) Model of the dc link and inverter filter LC stages using α and β reference frames.

(c) State variables of interest, namely the dc link voltage v_{dc}, and ac filter capacitor voltage $\bar{v}_f$.

Fig. 4. The operating principle of the FCS-MPC regulated two-level three-phase VSC with an LC filter that simultaneously controls ac and dc bus voltages.

On the other hand, the following approximation is used on the dc side to estimate how much the dc link capacitor is charged/discharged during each sample period:

$$v_{dc}(k+1) = v_{dc}(k) + \frac{1}{C_{dc}}\left(i_{dc} - \frac{i_{pol,i} + i_{pol,p}}{2}\right) T_s. \quad (14)$$

where $i_{pol,i}$ and $i_{pol,f}$ are the initial and final currents flowing into the UPS inverter during the following time step, respectively, and T_s is the sampling time. It should be noted that both of these currents depend on the future voltage vector (the one to be chosen), and hence need to be computed for all possible states. When compared to equation (9) from [31], where only the predicted current was taken into account, by doing the averaging operation, (14) allows a better estimation of the energy taken out of the dc link during each sampling time and consequently a more accurate prediction of the capacitor voltage.

Equations (13) and (14) are used to predict $\bar{i}_f$, $\bar{v}_f$ and v_{dc} at the end of the next sampling instant. These predictions are then fed to a CF, which determines the optimal actuation. Fig. 4 summarizes the overall representation of the POL converter model, as well as the variables of interest to be controlled, i.e. the load voltage and the dc link voltage. It is important to notice that FCS-MPC methodology described above provides excellent robustness to parameter variations, as empirically proved in Sections VI and VII of [28]. Among other parameters, variation of L_f in the control algortihm with more than 200% has been shown not to compromise the stability of the system. On the other hand, the common ac inductor variations of 10 to 20% have essentially a negligible influence on the performance of the system. Following subsection proposes a CF that is able to effectively regulate both ac and dc voltages at the same time.

B. Stabilization via Cost Function

Evaluation of the CF is the final step of the FCS-MPC algorithm which determines the actuation to be applied at the next sampling instant. The objective is to select the gating signals S_a, S_b and S_c in such a way that the state variables of interest track their references with minimal error. Each combination of gating signals corresponds to a particular input voltage vector $\bar{v}_i = v_{i\alpha} + jv_{i\beta}$, as indicated in Table II. The conventional CF used for ac voltage regulation on the LC filter is given as follows [44]:

$$g_{con} = \left(v_{f\alpha}^* - v_{f\alpha}\right)^2 + \left(v_{f\beta}^* - v_{f\beta}\right)^2. \quad (15)$$

TABLE III
PARAMETERS OF THE TEST SYSTEM USED IN SIMULATIONS AND EXPERIMENTS

Supply side voltage	v_s = 300 V
LC-filter on the ac side	L_f = 2.4 mH, C_f = 25 μF
LC-filter on the dc side	L_{dc} = 5 mH, C_{dc} = 30 μF
Linear loads	R_l= 33 Ω
Sampling time	T_s = 25 μs
Turnaround time	$T_t \approx 15$ μsec
Load reference voltage	v_{ref} = 207.85 V ph-ph, f_{ref} = 50 Hz
Derivative factor	λ_{der} = 0.5

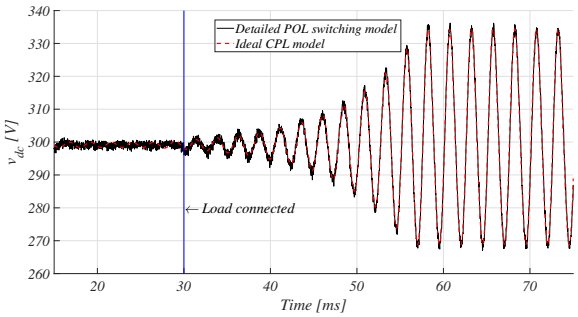


Fig. 5. Comparison between the detailed model of the FCS-MPC regulated VSC and an ideal CPL ($i = P_l/v_{dc}$).

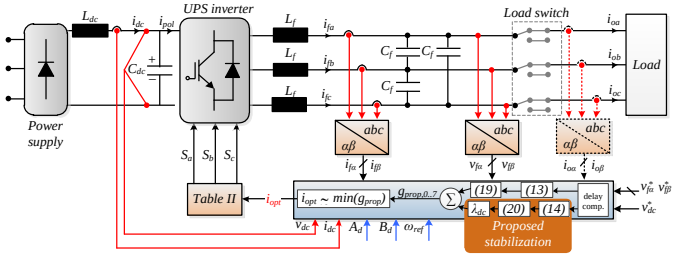


Fig. 6. Complete implementation of proposed stabilization approach.

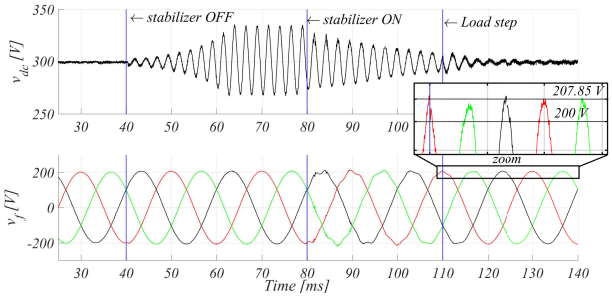


Fig. 7. Response of v_{dc} and v_f for $\lambda_{dc} = 0.1$.

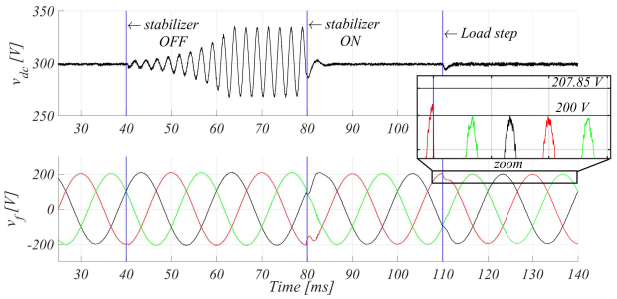


Fig. 8. Response of v_{dc} and v_f for $\lambda_{dc} = 1$.

In [28], it was shown that the steady-state performance can be significantly improved by incorporating a term that tracks the derivative of the voltage reference, as follows:

$$g_{der} = \left(C_f \omega_{ref} v^*_{f\beta} - i_{f\alpha} + i_{o\alpha}\right)^2 + \left(C_f \omega_{ref} v^*_{f\alpha} + i_{f\beta} - i_{o\beta}\right)^2 \tag{16}$$

where $\omega_{ref} = 2\pi f_{ref}$ is the angular frequency of the load reference voltage. The respective term can be added to the basic CF and balanced with a weighting factor λ_{der}. Moreover, to achieve safe and efficient operation of the converter, the current limiting term h_{lim}, and switching penalization term sw, are also introduced:

$$h_{lim} = \begin{cases} 0, & \text{if } |\bar{i}_f| \leq i_{max} \\ \infty, & \text{if } |\bar{i}_f| > i_{max} \end{cases} \tag{17}$$

$$sw = |S_a(i+1) - S_a(i)| + |S_b(i+1) - S_b(i)| + |S_c(i+1) - S_c(i)|. \tag{18}$$

Finally, all the terms are integrated into a complete cost function for the ac side voltage tracking [28].

$$g_{ac} = g_{con} + \lambda_{der} g_{der} + h_{lim} + \lambda_{sw} sw^2. \tag{19}$$

While (19) achieves excellent voltage regulation performance on the ac side when a stiff dc link is used, it also enforces the converter to behave as a CPL. As discussed before, this may result in unstable performance of the system if there is a resonance in the output impedance of the power supply. To investigate this possibility, a simulation of a system shown in Fig. 3 is performed using the parameters given in Table III. Indeed, as shown in Fig. 5, the system becomes unstable after connecting the load. This is not surprising since the output impedance of the power supply, that can be computed using (2), surpasses the input impedance of the POL converter within its bandwidth, which is calculated as $Z_{in} = -v_s^2/P_l$. Here, P_l is the power of the load given as $P_l = 3v_{ref}^2/2R_l$[1].

It is interesting to notice that if the full switching model of the POL converter is replaced by Z_{in} given above, there is essentially no difference in the dynamic response, as shown by comparing the red dashed and black lines in Fig. 5. This indicates that the bandwidth of the POL converter is much higher than the resonance frequency of Z_{out}, which will also be confirmed by measurements provided in the following section. It can also be seen that dc link oscillations are sustained, rather than building up. This phenomenon, known as the limit-cycle in nonlinear control theory, can occur in systems that have saturation in the loop [37]. Here, the saturation is introduced by unidirectional power supply that does not allow the feedback power and therefore limits the current flowing through the dc inductor to only positive values. For this reason, the dc current and voltage oscillations are restricted to a constant magnitude. This phenomenon is well-known and has also been reported in earlier publications that deal with stabilization of dc microgrids [17].

A simple solution to the instability problem is proposed here. In particular, (14) is firstly used to predict the propagation of a dc voltage for every possible actuation. Then, the term which penalizes the actuations that lead to deviations of the dc link voltage from its steady value is introduced as follows:

$$g_{dc} = \left(v^*_{dc} - v_{dc}\right)^2. \tag{20}$$

Finally, (20) is multiplied with a weighting factor λ_{dc} and added to (19) in order to form a complete CF:

$$g_{prop} = g_{con} + \lambda_{der} g_{der} + h_{lim} + \lambda_{sw} sw^2 + \lambda_{dc} g_{dc}. \tag{21}$$

Fig. 6 presents the overall control approach in the system. All the inputs to the FCS-MPC algorithm are shown. They include the references, measurements, as well as fixed inputs embedded into the code prior to execution. Also, the execution order is indicated by direction of the arrows. Namely, the algorithm first performs a delay compensation using the method from [45]. Then it predicts $\bar{i}_f$, $\bar{v}_f$ and v_{dc} using (13) and (14), and evaluates all predictions with the CF stated in (21). Lastly, the voltage vector for which the CF has the minimal value, is applied to the converter.

[1]Shape of Z_{in} in a wide frequency range is shown in Fig. 11 (a) that is given in the next section.

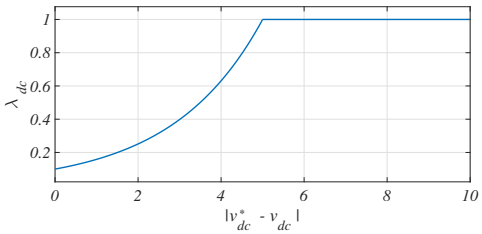


Fig. 9. Function of λ_{dc} in relation to dc-link voltage tracking error.

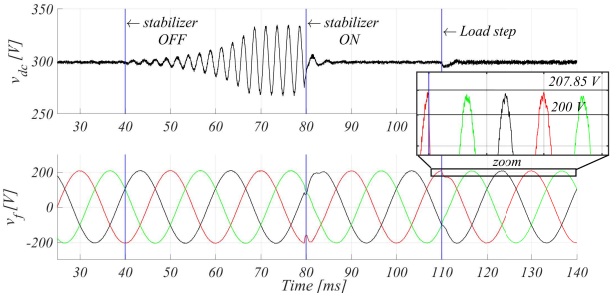


Fig. 10. Response of v_{dc} and v_f for λ_{dc} set according to (22).

The capability of the proposed controller to stabilize the system is tested for two arbitrary settings of λ_{dc}, namely $\lambda_{dc} = 0.1$ and $\lambda_{dc} = 1$. The results for $\lambda_{dc} = 0.1$ are shown in Fig. 7, while Fig. 8 shows them for $\lambda_{dc} = 1$. It can be seen that the performance is not good when λ_{dc} is set too low. In particular, the dc link exhibits high ringing that is also replicated to the ac side response. On the other hand, when λ_{dc} is set too high, as in Fig. 8, stabilization occurs much faster, but the fundamental voltage amplitude on the ac side significantly drops. Some design guidelines for adaptive λ_{dc} settings that allow good trade-off between these performance metrics are suggested next.

C. Adaptive Cost Function Design

As it has been shown in the previous section, a good load performance is achieved with a low setting of λ_{dc}, while higher λ_{dc} gain ensures better dc link dynamic response. To this end, an adaptive calculation of λ_{dc} is proposed here in order to capture the best features of the two. In particular, the following function is chosen:

$$\lambda_{dc} = 0.1 \cdot exp(|v^*_{dc} - v_{dc}| \cdot \frac{ln(10)}{5}). \qquad (22)$$

where 0.1 is the value of λ_{dc} when there is no dc voltage error. On the other hand, when there is a dc link voltage error, λ_{dc} is adapted according to (22), eventually reaching the value of 1 when the voltage error becomes $5\ V$. This is achieved by the factor $ln(10)/5 = 0.4605$ in the exponential term, where factor 10 implies that λ_{dc} setting at error $5\ V$ is ten times higher than setting at zero voltage error. In addition, λ_{dc} is limited to the value of 1 for errors higher than $5\ V$ to avoid unnecessary degradation of the load voltage during transients. Fig. 9 shows λ_{dc} as a function of deviation of dc-link voltage from the reference, while Fig. 10 shows the simulation result that confirms that the objective is achieved. Namely, dc-link is quickly stabilized after the step change in load, while the voltage at the load side has excellent dynamic response and negligible steady state amplitude deviation from the reference.

Following section provides a theoretical background that justifies proposed adaptive law by investigating its effects on Z_{in}, as well as on dynamic and static performance of the load voltage.

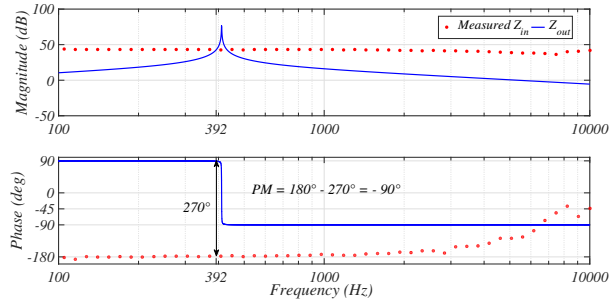
V. Design and Theoretical Analysis of the Proposed Stabilization Method

The effect of proposed CF (21) on the dc link stability and the ac side voltage tracking performance is analyzed in this section. Proper selection of the weighting coefficients plays an instrumental role in achieving good performance. Detailed analysis about design of λ_{der} was done in [28]. This term is used to improve the steady-state performance of the load voltage and has a negligible impact on dynamics of the system. On the other hand, the focus here is on addressing the influence of λ_{dc}, which gives weight to the proposed stabilization term.

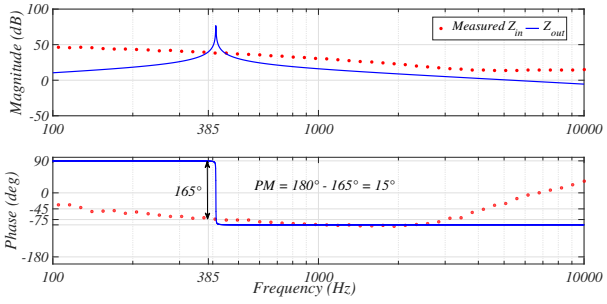
A. DC-Link Stability

An FCS-MPC regulated POL converter is essentially a high-bandwidth power processing system that can rapidly adjust the voltage at the ac load side. Since the ac load voltage determines the instantaneous power consumption of the POL converter, by modifying it in accordance with the dc-link voltage oscillations defined by the proposed stabilization term in the cost function (CF), the system can be effectively stabilized. To this end, the CF prefers to apply the switch configurations that increase the POL power consumption if the dc-link voltage is above its reference and vice versa. The net effects are both the amplification and the phase shifting of i_{pol} at the dc link oscillation frequency compared to the case when there is no stabilization term. Both effects become stronger by increasing the value of λ_{dc}, as it will become apparent next.

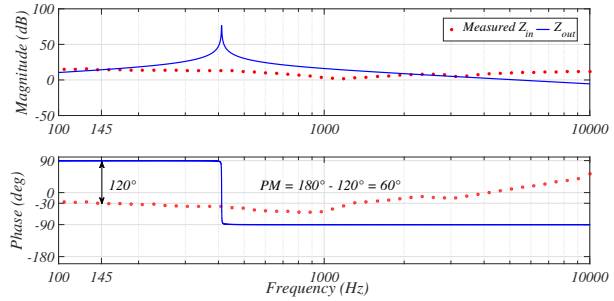
To study the effects of proposed stabilization, measurements of Z_{in} from the full order nonlinear simulation model have been performed, as commonly done by other researchers as well (see e.g. [46]). As discussed in Section II-B, measurement of frequency responses is a standard approach to study the dynamic behavior of complex nonlinearities for which such response is difficult to analytically calculate (e.g. see section 5.1.5. in [37]). Central to this approach is the concept of DF, where measured Z_{in} is used to approximate (or describe) the nonlinearity, which is in our case FCS-MPC regulated POL converter. Once Z_{in} measurement are obtained, the concepts of phase and gain margins can be used to assess the stability margins of the nonlinear system (e.g. as explained in section 18.1.4 of [38]). A well-known configuration for Z_{in} measurement has been used to perform the measurements [39]. In particular, an ac voltage source was inserted between the ideal dc source and the POL converter. The frequency of the ac voltage source was then varied between $100\ Hz$ and $10\ kHz$ in 48 logarithmically spaced discrete steps, while its amplitude was kept constant at $10\ V$. Therefore, for each setting of λ_{dc}, 48 simulations have been carried out. Finally,



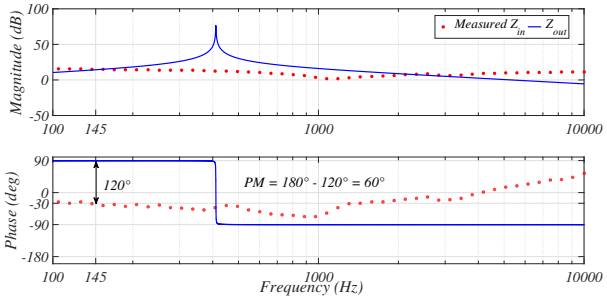
(a) Z_{in} without the stabilization term.



(b) Z_{in} with $\lambda_{dc} = 0.1$.



(c) Z_{in} with $\lambda_{dc} = 1$.



(d) Z_{in} with λ_{dc} according to (22).

Fig. 11. Influence of λ_{dc} on input impedance of the POL converter.

for every frequency value, both the amplitude and phase of Z_{in} have been calculated.

After determining empirically Z_{in} at 48 specific frequency points, the corresponding minor loop gain T_{mlg} can be directly derived by dividing Z_{out} (calculated analytically from (2)), with Z_{in} at each frequency point. The stability of the system can then be assessed by checking if T_{mlg} fulfills the Nyquist stability criterion, as explained in Section II-B. A straightforward option to do that would be to draw the polar plot of T_{mlg}. However, since Z_{out} has limited fidelity if calculated only at specific points, Z_{in} and Z_{out} are shown separately, as seen in Fig. 11 for four different settings of λ_{dc}. Moreover, an impedance plot provides more information about the relationship between the two impedances than the loop gain plot, while also allowing to inspect the phase margin of the system. In the respective system, the phase margin directly determines whether the Nyquist stability criterion is fulfilled or not. Positive phase margin ensures that the -1 point is not encircled and vice-versa. It should be noted that the impedance and admittance plots have also been frequently used in other prominent references to verify the Nyquist stability criterion (e.g. see [9] and [23]).

To this end, it can be clearly seen from Fig. 11 how the stabilization term affects the stability margins of the system. In particular, when $\lambda_{dc} = 0$, Z_{in} of the POL converter has a pure negative impedance up to frequencies around 1 kHz, as shown in Fig. 11 (a). Since the resonance frequency of Z_{out} is much lower than that (around 400 Hz), the system exhibits a negative phase margin and is unstable, as also confirmed by the simulation results. On the other hand, when $\lambda_{dc} = 0.1$, both the magnitude and phase of Z_{in} are shaped in a way to make to the system stable, as shown in Fig. 11 (b). However, the phase margin in this case is only around 15°, which implies that prolonged oscillations should be expected. This is again confirmed by the simulation result from Fig. 7. When $\lambda_{dc} = 1$, Fig. 11 (c) shows that Z_{in} is shaped in a way that drastically increases the phase margin (to around 60°), so the dc bus is stabilized much faster than in the previous case. However, such a high λ_{dc} setting results in reduced amplitude of fundamental voltage on the ac side, as also indicated in Fig. 8. The latter problem can be solved by setting λ_{dc} in adaptive fashion. In this case, Z_{in} has essentially the same phase margin as when $\lambda_{dc} = 1$, as shown in Fig. 11 (d). However, there is almost no amplitude deviation on the ac side with adaptive λ_{dc}, which is thus clearly the best setting overall.

It is important to notice that, as with most other nonlinear elements, the frequency response of Z_{in} is amplitude dependent. The reason why Z_{in} measurements have been taken here for fixed perturbation voltage of 10 V is that it turned out that higher amplitude provided higher stability margins. On the other hand, lower amplitude caused negligible differences in the margins, and it also turned out difficult to measure due to a low signal to noise ratio. Therefore, the amplitude where lowest stability margins could have been reliably measured has been used. Indeed, this approach is also recommended in standard control textbooks (see section 18.1.4 in [38]). Following two sections investigate the effect of λ_{dc} on load performance.

B. Load Dynamic Performance

Besides clarifying the influence of the stabilization term and λ_{dc} setting on the dc link stability, it is of equal importance to

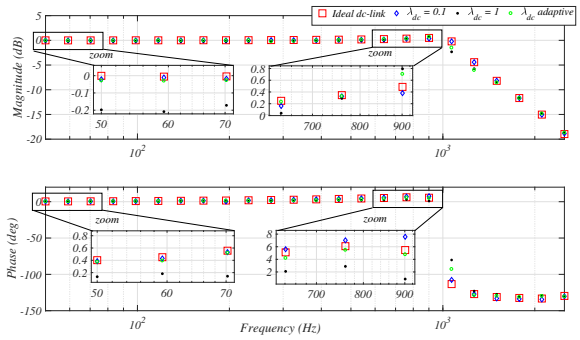


Fig. 12. Frequency response of the load voltage reference tracking performance.

investigate its effects on the load dynamic performance. For this purpose, again a frequency sweep has been performed. However, in this case the frequency of voltage reference has been varied from 50 Hz to 2.5 kHz in 24 logarithmically spaced discrete steps, while its amplitude was kept constant at 120 V. Therefore, for each setting of λ_{dc}, 24 simulations have been carried out. For every frequency value, both the amplitude and phase of the load voltage has been measured and its relationship to reference voltage has been calculated. The benchmark case is the one where the dc link is stiff. Since there is no resonance in Z_{out}, the stabilization term is not needed and the POL converter can freely operate as an ideal CPL, which allows the best possible dynamic performance. For other three cases, the same structure as in Fig. 3 was used and the frequency response was captured for each of the remaining three λ_{dc} settings, after the dc link was fully stabilized.

Fig. 12 shows the results of these measurements. It can be seen that for $\lambda_{dc} = 0.1$, there is only a negligible difference in load regulation performance compared to the benchmark, both in terms of amplitude and phase tracking. However, as seen in the previous section, this setting provides very low phase margin in the dc link and is hence not suitable. On the other hand, $\lambda_{dc} = 1$, although providing fast stabilization of the dc bus, also deteriorates the load voltage steady state performance. In particular, there is a noticeable drop in voltage tracking at lower frequencies that can be seen in the zoomed part of the plot. Finally, when λ_{dc} is set adaptively, there is virtually no effect on the amplitude tracking at lower frequencies, while only a small difference can be observed near the crossover frequency. This indicates only small influence of adaptive setting on dynamic voltage tracking performance and virtually unaffected steady-state performance. The latter one is further investigated in the following.

C. Load Steady-State Performance

The final step is to provide a quantitative measure of the steady-state performance. For this reason, a parameter sweep has been performed. In particular, λ_u has been swept from 0 to 10 in a step of 0.01 in order to capture the behavior of the system under different average switching frequencies. These sweeps have been done for four different values of λ_{dc}, i.e. 0.1, 0.2, 0.5 and 1. In comparison, simulations have also been carried out for the ideal dc link where λ_{dc} was set to 0. Therefore, 5000 simulations have been carried out in total on a 24 core, 2.4 GHz processor, where sampling time of each simulation was chosen as 1 μsec. The PC carried out all simulations in approximately 15 minutes.

The results are shown in Fig. 13, where it can be seen that the amplitude drop of the fundamental harmonic becomes larger at higher λ_{dc}, while it also shows a tendency to drop with a lower switching frequency (higher λ_u). Therefore, it is advisable to set the stabilization coefficient as low as possible while ensuring stability. As seen before, these two objectives can be balanced by adaptive λ_{dc}. Finally, it should be noted that the total harmonic distortion (THD) of the load voltage has been captured from simulations. However, λ_{dc} has not proved to have a noticeable influence on it. For that reason, THD has not been shown here. Next section provides the experimental verification of the proposed method.

VI. Experimental Results

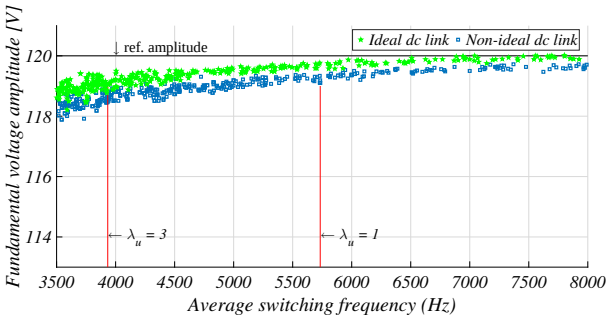
The FCS-MPC based dc microgrid stabilization strategy was verified experimentally, where an 18 kW-rated test system, as shown in Fig. 14, was built for that purpose. The power stage comprises a Delta Elektronika SM 600-10 dc power supply, a Semikron two-level three-phase VSC, an LC filter on the dc side, a three phase LC filter on the ac side, and a linear load. The experimental system corresponds to the structure given in Fig. 3. It should be noted that the Semikron VSC by default comprises electrolytic dc link capacitors. For the purpose of this test, these capacitors have been disconnected, and replaced by a film capacitor following the guidelines from the converter manufacturer.

A. Implementation of the Algorithm

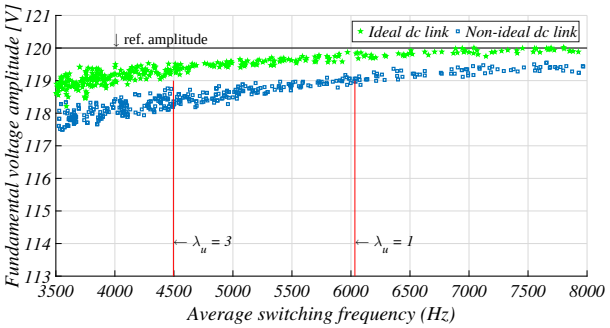
The control algorithm was implemented in the dSpace MicroLabBox with DS1202 PowerPC DualCore 2 GHz processor board and DS1302 I/O board. The achieved turn-around time was around 15 μsec. It should be noted that the majority of that time came from the A/D conversions, while the algorithm itself took only around 2 μsec. In particular, the dSPACE A/D converter samples at a rate of 1 MSPS. Therefore, the time required for sampling of one channel is approximately 1 μsec. As indicated in 6, the FCS-MPC controller measures 11 variables (9 on the ac side, and 2 on the dc side). Therefore, the total sampling time is around 1 μsec. On the other hand, the exemplary industrial micro controller TMS320F28377 samples at a rate of 3.5 $MSPS$ and it would thus do the A/D conversion in less than a third of that time, while the algorithm execution time would not differ much. Since the algorithm has synchronized sampling and switching procedures, the computational delay of exactly T_s needed to be compensated. As mentioned before, the method proposed in [45] was used for that purpose. The overall parameters of the test setup can be found in Table III.

B. Tests

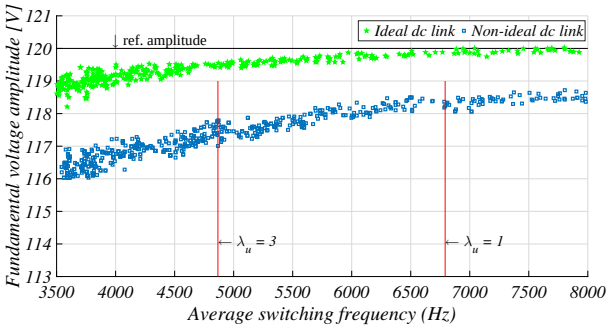
Two sets of tests have been carried out to validate the effectiveness of the proposed strategy for each of the three



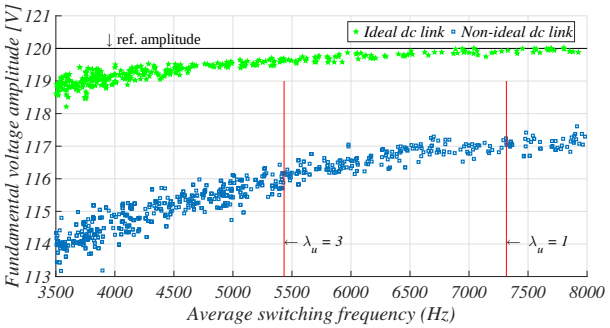
(a) Fundamental amplitude vs. average switching frequency for $\lambda_{dc} = 0.1$.



(b) Fundamental amplitude vs. average switching frequency for $\lambda_{dc} = 0.2$.



(c) Fundamental amplitude vs. average switching frequency for $\lambda_{dc} = 0.5$.



(d) Fundamental amplitude vs. average switching frequency for $\lambda_{dc} = 1$.

Fig. 13. Influence of weight settings λ_{dc} and λ_u from (21) on the average switching frequency and the amplitude of fundamental portion of the voltage.

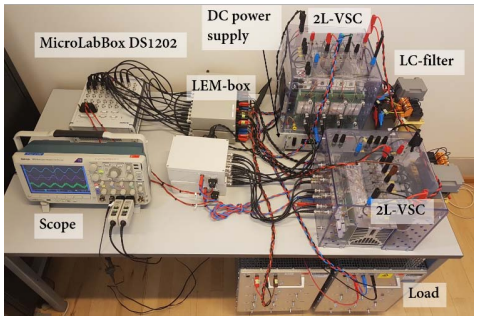


Fig. 14. Photo of the experimental setup used for model predictive control.

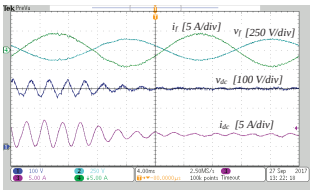
representative λ_{dc} settings, i.e. $\lambda_{dc} = 0.1$, $\lambda_{dc} = 1$, and adaptive λ_{dc} set in accordance with (19).

For the first test, the VSC has been first loaded with a resistive load of 33 Ω and the stabilization term deactivated. Behaving as an ideal CPL in the frequency range of the resonance of the dc side LC filter, the VSC has expectedly caused unstable oscillations of the dc link voltage. Fig. 15 (a) shows the moment of activating the stabilization term for $\lambda_{dc} = 0.1$. As predicted by analytical analysis and simulation results, this setting is able to stabilize the dc link, but phase margin is low and significant ringing can be observed. On the other hand, a higher weight setting $\lambda_{dc} = 1$ results in a faster stabilization, but also deteriorates the voltage tracking performance on the ac side, as seen in Fig. 15 (c). Finally, the adaptive setting provides good performance in both metrics, as it can be seen from Fig. 15 (e).

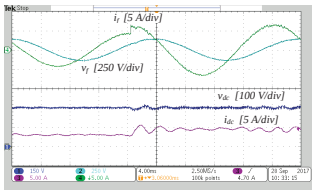
The second test verifies the performance of the system under dynamic changes of the load on the ac side. In particular, Fig. 15 (b) shows the moment of sudden connection of another 33 Ω load in parallel with the first one for $\lambda_{dc} = 0.1$. In accordance with the earlier analysis, a significant ringing can be seen on the dc side. On the other hand, for $\lambda_{dc} = 1$, very good dynamic performance on the dc link can be observed, but there is a drop in the steady-state voltage drop on the ac side. Finally, with adaptive setting, shown in Fig. 15 (f), both performance metrics are excellent, as expected.

C. Comparison of Results to those Achieved in the State-of-the-Art

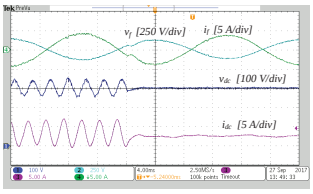
It is important to notice that proposed strategy allows significantly better performance than state-of-the-art POL converter based stabilization methods. One of the recent references in the field, e.g. [22], can be used to prove the point. In particular, the sampling/switching frequency of the POL converter is 20 kHz in [22], while the dc link filter is in the worst case L_{dc} = 6 mH and C_{dc} = 60 μF. In clear contrast, the switching frequency in this paper is less than 8 kHz while L_{dc} = 5 mH and C_{dc} = 30 μF. Therefore, not only does [22] make a study on a POL converter with higher possible bandwidth, but also on Z_{out} with a much lower resonance peak. Nonetheless, the control strategy in this paper significantly outperforms the one in [22], as it can be immediately appreciated by comparing Fig. 13 (c) from [22] with Fig. 15 (f) in this paper. Namely, after the step load change here, the system reaches steady state almost immediately and without ringing, while in [22], it takes more than 40 ms to reach the steady state and ringing is significant.



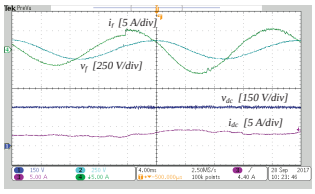
(a) Stabilization of the dc link with $\lambda_{dc} = 0.1$.



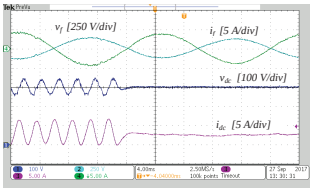
(b) Step load change with $\lambda_{dc} = 0.1$.



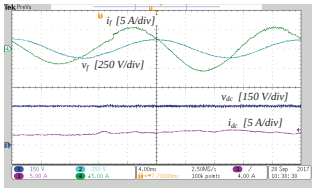
(c) Stabilization of the dc link with $\lambda_{dc} = 1$.



(d) Step load change with $\lambda_{dc} = 1$.



(e) Stabilization of the dc link with λ_{dc} according to (22).



(f) Step load change with λ_{dc} according to (22).

Fig. 15. Experimental validation of proposed control strategy.

D. Generalization Aspects

The stabilization approach proposed in this paper is applicable in a more general dc microgrid setting where, instead of the passive front-end, one or several active sources could regulate the system with or without the droop characteristics.

As discussed in [13] (see equation 9.3 in section 9.2) for voltage feedback control and in [41] for voltage feedback with droop control, the resonance peak of Z_{out} will in both cases generally be significantly reduced compared to open loop Z_{out}. Therefore, the instability will less likely occur in the first place. Nevertheless, the proposed stabilization could still be useful. For instance, if stability margin of the system is not sufficient even with active front end control (e.g. under heavy CPL conditions or with improper design of active front-end controller), proposed method can provide additional damping and improve the performance. On the other hand, it could also serve as a back up stabilization option in autonomous dc microgrids, which cannot always guarantee the availability of actively-regulated sources [19].

The practical applicability of proposed method in systems where standard voltage feedback control in the active front-end is used is straightforward because the active-front end and POL converter can have the same reference for dc link voltage. On the other hand, to be able to use it together with droop-regulated sources, the proposed term has to be somewhat modified. Namely, droop regulated sources adapt the dc link voltage according to the load in order to ensure proper current sharing between themselves [19]. Therefore, a high-pass or band-pass filtered voltage measurement should be deployed in order to capture only the oscillating phenomenon, while v_{dc}^* should be set to 0 instead of the value of v_s.

VII. Conclusion

This paper has proposed a simple and intuitive method that can solve the unstable dynamic interactions between a CPL and a dc microgrid. In particular, a two-level FCS-MPC regulated UPS inverter that feeds a linear three-phase load is chosen as a demonstrative CPL example. By using a standard CF dominated by the ac voltage reference tracking term, the inverter achieves a stiff-voltage regulation on the ac side, which makes it behave as an ideal CPL in the frequency range of interest. By comparing the negative incremental input impedance of the CPL and the output impedance of the LC filter installed in a series with dc power supply, it is shown that the instability phenomenon can be accurately predicted. As a remedy to the instability phenomenon, an additional term is introduced into the standard CF used in the UPS inverter. It is based on monitoring the dc link capacitor voltage, predicting its future propagation, and finally penalizing the switching configurations that lead to unstable oscillations. Since FCS-MPC controller operates with a sampling time of 25 μs while average switching frequency is below 8 kHz, the algorithm has a lot of flexibility to balance the ac and dc voltage tracking objectives. This results in a significantly better trade-off between a stable dc link voltage and a load regulation performance compared to the existing approaches. The benefits of this strategy are verified both theoretically and experimentally.

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Tomislav Dragičević (S'09-M'13-SM'17) received the M.E.E. and the industrial Ph.D. degree from the Faculty of Electrical Engineering, Zagreb, Croatia, in 2009 and 2013, respectively. From 2013 until 2016 he has been a Postdoctoral research associate at Aalborg University, Denmark. From March 2016 he is an Associate Professor at Aalborg University, Denmark. His principal field of interest is overall system design of autonomous and grid connected DC and AC microgrids, and application of advanced modeling and control concepts to power electronic systems. He has authored and co-authored more than 110 technical papers in his domain of interest and is currently editing a book in the field. He serves as an Associate Editor in the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and in the Journal of Power Electronics.