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Failure Analysis of a Degraded 1.2 kV SiC MOSFET after Short Circuit at High Temperature

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***Abstract*—This paper presents the experimental results obtained from investigating the impact of short-circuit in SiC MOSFETs at high temperatures. The results indicate that a gate degradation mechanism occurs under a single-stress short circuit event at nominal voltage and junction temperature of 150°C. The failure mechanism is the gate breakdown, which can be early detected by monitoring the voltage drop of the gate-voltage waveform. The reduction of the gate voltage indicates that a leakage current flows through the gate, leading to a permanent damage of the device but preserving its voltage blocking capability. This hypothesis has been validated through semiconductor failure analysis by comparing the structure of a fresh and a degraded SiC MOSFET. A Focused Ion Beam cut is performed showing cracks between the poly-silicon gate and aluminium source. Furthermore alterations/particles near the source contact have been found for the degraded device.**

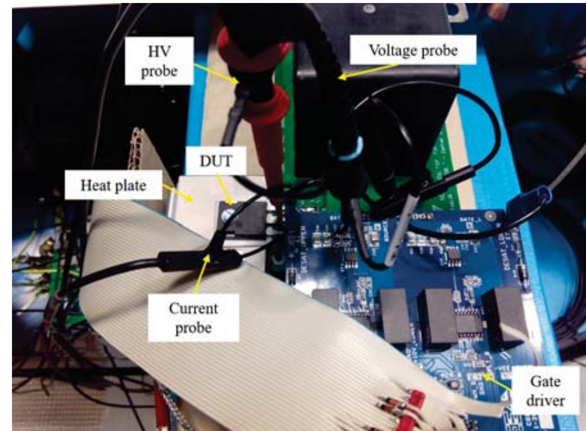

Fig. 1. The Non-Destructive Test bench showing the DUT, heat plate, gate driver and measurement equipment.

I. Introduction

Silicon Carbide (SiC) MOSFETs are widely assumed to have superior performance in respect to silicon IGBTs in medium-to-high power applications. However, this assumption needs to be further investigated, especially for applications requiring short-circuit proof devices operating at high ambient temperatures, such in the case of motor drives applications. Many efforts have been devoted to the short-circuit robustness testing of SiC MOSFETs under non-destructive operations; while some of them investigated the ageing of the device with a Repetitive Short Circuit testing approach [1]–[3], others identified degradation mechanisms with a stressful single-event short circuit test [4]–[6].

The most common failure mode reported in the literature, after the device is exposed to a short circuit, is the gate-oxide breakdown [7], whose indicator is the on-state gate-source voltage reduction due to the increase in gate leakage current. This failure mode has been attributed to the high temperature and high electric field withstood across the thin gate oxide. The small oxide thickness is used in SiC MOSFETs with the purpose of minimizing the channel resistance [8], therefore, robust short-circuit SiC MOSFETs can be fabricated, but on the other hand, the performance under normal operation will be compromised with high conduction losses and this is not acceptable from the end user perspective.

Furthermore, there are several challenges that the SiC/SiO_2 interface needs to deal with if compared with traditional Si/SiO_2 interfaces: (1) the large bandgap of SiC enhances tunneling currents through the gate oxide; this means that for the same oxide field, the gate leakage current is higher for SiC/SiO_2 interfaces [9], (2) the high blocking capability achieved with SiC devices brings the necessity of limiting the field in the gate oxide by implanting deep p-regions below the gate oxide and limiting the negative gate voltage in blocking mode, and (3) the high defect density of SiC leads to extrinsic defects in the gate oxide (i.e., substrate defects, particle inclusion, process variations, etc.) [10]. To confirm the above theories, physical inspection of damaged SiC MOSFETs has been performed recently, showing cracks in the field oxide between the gate poly-silicon and the source contact [3], and showing melted aluminium [11]. Nevertheless, no damage has been observed in the thin gate oxide as discussed in [12]. The weakness of the gate oxide has also been observed through power cycling tests as reported in [13] and [14], where a positive shift of the threshold voltage has been detected.

Another failure mode typically observed after a short circuit event is a thermal runaway failure. Two indicators have been pointed out; a large turn-off tail current [4] and an uncontrolled increase of the drain current at the end of the short-circuit pulse [5]. The uneven current and temperature distribution inside the chip has been proposed as the root cause, which in turns triggers thermal instabilities leading to leakage current increase. Another theory is that the parasitic npn bipolar transistor may become active due to large amount of holes injected in the p-body region [7].

In this paper, failure analysis on 1.2-kV planar SiC MOSFETs after a single short-circuit test at junction temperature of

150°C is performed. The degraded SiC MOSFET is compared with a new one in order to investigate the root cause of the failure mechanism leading to the gate leakage current increase phenomenon. The tested SiC MOSFET shows a permanent gate-oxide degradation from the electrical waveforms; this hypothesis is later confirmed with the physical inspection of the device. The vertical cut proves that a crack exists between the poly-silicon gate and the source terminal, more specifically in the field oxide region.

II. Short-Circuit Tests

A. Setup description

A 2.4-kV/10-kA Non-Destructive Tester is applied to perform safe short circuit tests, whose main features are summarized in the following. The tester structure includes the following parts: a high-voltage power supply V_{DC} which charges up a capacitor bank C_{DC}, whose energy is used to perform the tests; a series protection that switches off, breaking the circuit right after the tests in order to prevent explosions of the DUT in the case of failure and thus allowing post-failure analysis [4]. A commercial moulded discrete 1.2-kV/90-A SiC planar MOSFET has been experimentally investigated. During the tests, the gate driver provides the gate control signal of V_{GS} = -5 V/ 20 V and the gate resistance is set to R_g = 10 Ω.

The drain current is measured with an ultra-mini rogowski coil, whose drain peak current is 6 kA (CWT30). The drain voltage is measured with a passive high-voltage probe from Lecroy with maximum voltage of 1.2kV (PPE 1.2kV) and the gate voltage waveform is measured with a passive probe from Tektronix (TP0200). Furthermore, a temperature controller is used to regulate the temperature of the heat plate. Fig. 1 shows the details of the experimental setup, where the Device Under Test (DUT) is placed in the test position.

B. Short-circuit waveforms

The waveforms of a typical short circuit test can be observed in Fig. 2, where the drain voltage, drain current and gate voltage are shown. The tests have been performed under a high temperature of T_j = 150°C and bias voltage of 600 V. The drain voltage exhibits negative and positive peaks related to the current variation through the circuit stray inductance. The drain current peak is 380 A and then decreases according to the junction temperature increase, which is a well-known phenomenon related to the positive thermal coefficient of MOSFETs. Furthermore, it is worth to note that two abnormal phenomena take place, which can be recognized as two different failure indicators: (1) the occurrence of a large tail current at turn-off, which is not typical of unipolar devices and it does not occur under normal conditions, and (2) the significant reduction of the on-state gate-source voltage V_{GS}, indicating that a large leakage current is flowing through the gate. The latter failure indicator is only observed when the device is tested with a short-circuit pulse duration of 4 μs. After the last test, the SiC MOSFET shows a permanent damage because the device cannot recover its initial state, but the device is still functional. From these results, one can give a

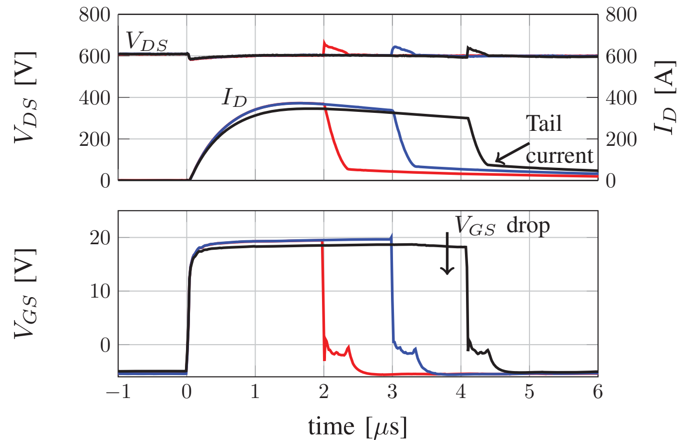

Fig. 2. Short-circuit tests with increasing time of a 1.2-kV/90-A SiC MOSFET: V_{DC} = 600 V T_j = 150°C.

first conclusion that a conductive path between the gate and the source has been formed. The assumption that a new resistive path has been originated will be validated through the physical inspection of the device in the following section.

III. Semiconductor Failure Analysis

A. Analysis of the degraded SiC MOSFET

In this section, the electrical behaviour will be correlated with the physical failure analysis of the 1.2-kV/ 90-A SiC MOSFET. To do so, a thermal analysis followed by a Focused Ion Beam (FIB) cut have been performed on the degraded SiC MOSFET in order to find possible damages on the gate oxide. First, the package material has been removed by high-temperature etching, and then, an Indium Gallium Arsenide (InGaAs) infra-red camera has been used to find possible hot spots. The principle is to apply a voltage on the drain terminal, for example up to 150 V, and connect the gate and the source terminals to ground. If the SiC MOSFET has a defect, a leakage current will appear from drain to source or drain to gate, which it can be detected with a very sensitive infrared camera. The infra-red camera can penetrate to the device with a certain depth, so it is possible to observe the chip surface and the structure underneath. The results can be observed in Fig. 3, where two hot spots can be identified. The hot-spot analysed in this paper is the one localized in the active region, which is highlighted in in Fig 3.

A Focused Ion Beam (FIB) at the hot spot location is used to obtain the vertical cross-section of the SiC MOSFET structure, whose image is revealed in Fig. 4. The image shows the physical structure corresponding to three cells, where one of the cells appears to be cracked on the field-oxide region. This cell in particular is further magnified in Fig. 5, where the crack between the poly-silicon gate and the aluminum source is clearly observed. On the other hand, the thin gate-oxide layer appears to be intact, concluding that the field oxide is the weakest part when the device is stressed under short circuit. These results are in agreement with the literature, since cracks

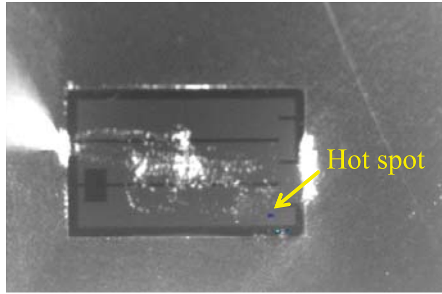

Fig. 3. InGaAs infra-red image of the degraded SiC MOSFET.

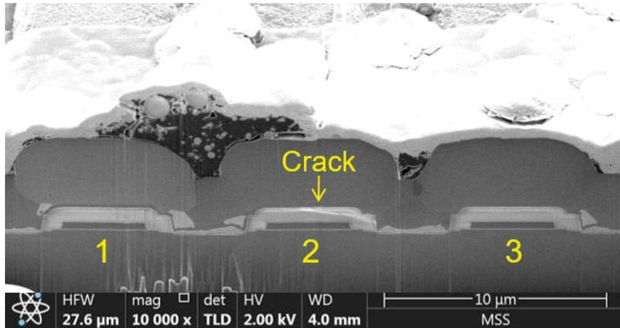

Fig. 4. Focused Ion Beam (FIB) cross-section of three cells at the hot spot location, where one of the cells presents a crack.

have also been observed in the field oxide region in [15]. A more in-depth analysis has been performed on adjacent cells, showing that not only one cell but several ones have cracks on the field oxide region.

Furthermore, the salicide which is the technology that is used to form the electrical contact between the semiconductor substrate and the source terminal appears severely degraded, as pointed out in Fig. 5. This region is further magnified in Fig. 6, where it can be observed that solid particles accumulate in the alluminum source region between the salicide and the gate oxide. So far, the origin of these particles is not clear and it is not possible to provide the relevant information about the failure mechanism due to the short circuit stress. To better understand whether these particles may come from a process defect or could have originated after the applied short circuit stress, a cross-section of a new 1.2-kV/90-A SiC MOSFET will be presented in the next section.

B. Analysis of the new SiC MOSFET

A physical investigation of a new SiC MOSFET device is presented in this section, with the aim of comparing the cell differences between a new and a degraded SiC MOSFET. To ensure an effective and comparable microstructural analysis, the package material of the new device has been removed by high-temperature etching similar as before, then, an Indium Gallium Arsenide (InGaAs) infra-red camera has been used showing no hot spots. The next step was to perform a cut in an arbitrary region of the active area and visually inspect the vertical cross-section of the new SiC MOSFET cell.

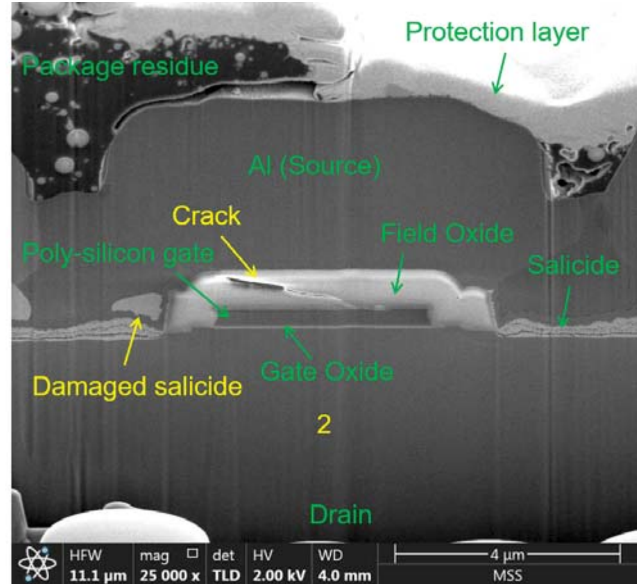

Fig. 5. Magnified Focused Ion Beam (FIB) cross-section of the damaged cell.

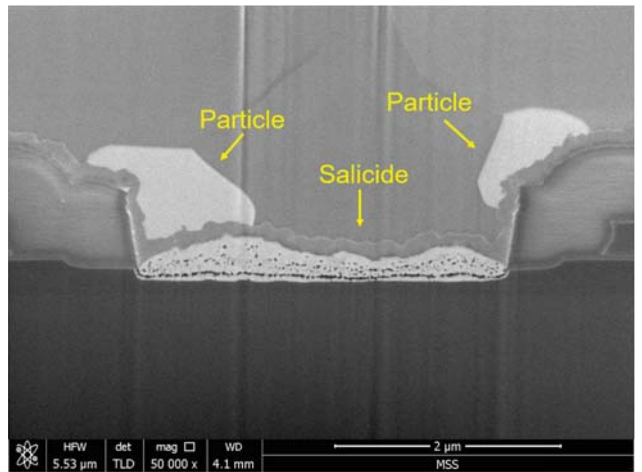

Fig. 6. Magnified Focused Ion Beam (FIB) of the salicide region of the degraded SiC MOSFET.

The results can be observed in Fig. 7, where the vertical structure of three cells is presented. It is interesting to compare Figs. 4 and 7, showing that a number of differences can be observed between the new and the degraded device. First, the cracks found in the degraded device between the poly-silicon gate and the aluminium source are not detected in the new device, as it is observed in Fig. 8. Second, the particles seen in the degraded SiC MOSFET near the salicide are not visible for the new device. This indicates that they could have originated as a consequence of the short-circuit stress and not from defects originating from the device process. A more detailed inspection of this region can be observed in Fig. 9. It can be confirmed that the particles cannot be observed and it is also worth to note that the granular structure is significantly altered when compared with the new device. Finally, the shape of the interface between the upper Aluminium layer and

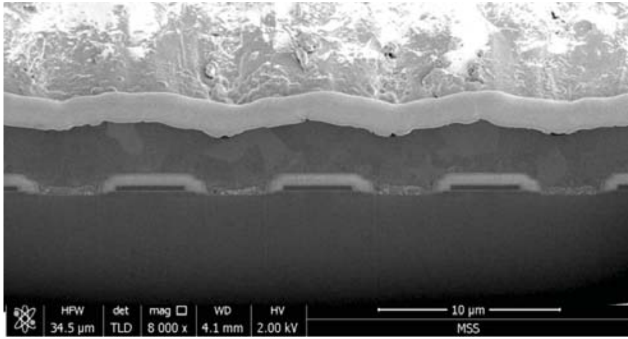

Fig. 7. Focused Ion Beam (FIB) vertical cross-section of a new SiC MOSFET showing three cells.

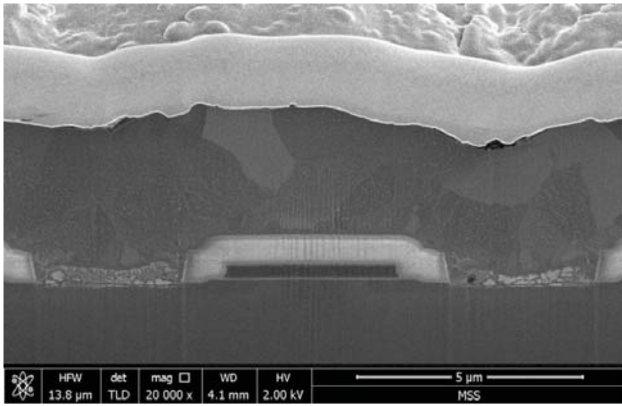

Fig. 8. Zoomed view of the FIB cross-section of a new SiC MOSFET.

the passivation layer shows a significant degradation between the non-degraded cell and the degraded one, since this layer appears to be deformed. From these results, it can be inferred that the temperature reached during short circuit provokes the deformation of the cells that could lead to the formation of cracks in the upper oxide region. These deformations may stress the gate structure and induce the observed cracks between the poly-silicon gate and the aluminium source, which forms a resistive path and as a consequence a gate leakage current appears causing the catastrophic failure of the device.

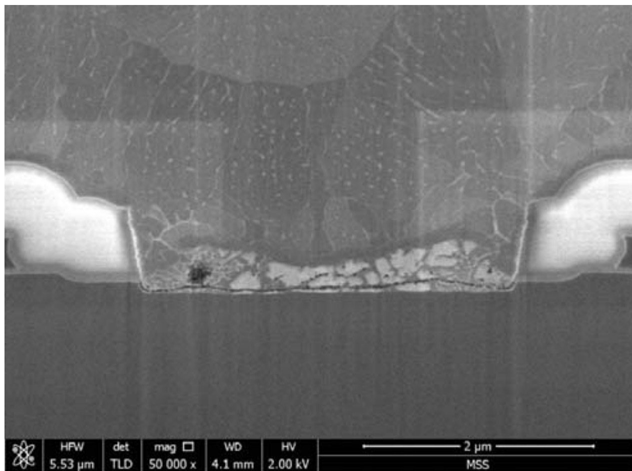

Fig. 9. Magnified Focused Ion Beam (FIB) of the salicide region of a new SiC MOSFET.

IV. Conclusions

In this work, short circuit tests have been performed on discrete 1.2-kV/90-A planar SiC MOSFETs, showing the failure mechanism is related to the gate-oxide breakdown. The electrical analysis points out that a gradual degradation occurs at high junction temperature and nominal bias voltage, causing irreversible damages and provoking a significant gate leakage current increase. The assumption of the gate oxide weakness is validated by means of a physical failure analysis between a degraded and a new device, where a SEM analysis in combination with a FIB cut shows the existence of a crack in the field oxide for the degraded device. The observed gate leakage current after the short circuit stress can be correlated with the formation of the crack, which creates a path between the poly-silicon gate and the source terminal. Though, many prior researches have pointed out that the gate-oxide is the weakest part, the micro-structural analysis did not show any cracks in the gate-oxide. Furthermore, a severe alteration in the salicide has been found for the first time. It is worth to note that the interface between the upper Aluminum layer and the passivation layer shows a significant degradation when compared with the non-degraded cell. This phenomenon may result in the formation of the observed particles accumulated in the aluminium source region near the salicide, since such particles cannot be found in the new device.

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