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Model Predictive Control Approach for Distributed Hierarchical Control of VSC-based Microgrids

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Keywords

≪Distributed hierarchical control≫, ≪finite control set (FCS)≫, ≪model predictive control (MPC)≫, ≪voltage source converter (VSC).≫

Abstract

This paper embeds a high bandwidth distributed hierarchical control structure for a power electronic based ac microgrid. Conventionally, hierarchical linear control loops are applied to control the grid frequency and voltage. However, they suffer slow dynamic response and high sensitivity to parameter variations. In this paper, high bandwidth control approach realized with a finite control set model predictive control (FCS-MPC) scheme to control multiple voltage source converters (VSCs). Furthermore, droop control and virtual impedance are employed to share active and reactive power. At the upper level distributed secondary control can be programmed with much higher bandwidth compare to linearized cascaded control structures. Simulation and experimental results indicate that voltage and frequency have been regulated order of magnitude faster than state of the art.

Introduction

With the high penetration of intermittent distributed energy resources (DERs) and flexible loads, the control structure of microgirds (MGs) play a prominent role in reliable and optimal MG operation. The general trend for MGs operation is to become more flexible and distributed. Thus, power electronic equipments and specially voltage source converters (VSCs) as an interface between DERs and ac common bus will be the backbone of the power grids in the next decades. Compared to the conventional grids which are mainly dominated by high inertia synchronous generators, MGs comprise DERs with inherent low inertia. Thus, in the islanded MG an individual load can have a significant influence on power balance. Hence, a high bandwidth voltage and frequency control structure and appropriate load sharing are prerequisites for efficient and stable operation of MGs [1, 2]. In order to achieve accurate power sharing among DERs as well as voltage and frequency stability, a hierarchical control structure has been introduced in literature [3, 4, 5, 6].

The major objective of the primary control level (PCL) is autonomous control of DERs, which mainly comprises inner voltage/current control loops, droop control function and virtual impedance loop [7, 8]. In order to regulate frequency and voltage deviations caused by the operation of PCL, a secondary control level (SCL) is utilized [9, 10]. The infrastructure of conventional SCL consists of a central computing unit, slow frequency and voltage regulation control loops, and a low bandwidth communication network for sharing control signals among DERs [11, 12, 13]. Due to a single point of failure, central SCL decreases the reliability of MG. Thus, distributed SCLs have been introduced [14, 15, 16, 17].

Nonetheless, aforementioned distributed SCL approaches are based on the linearized cascading control loops. Since these structures have inherent low-pass filter behavior, the SCL is slow and sensitive

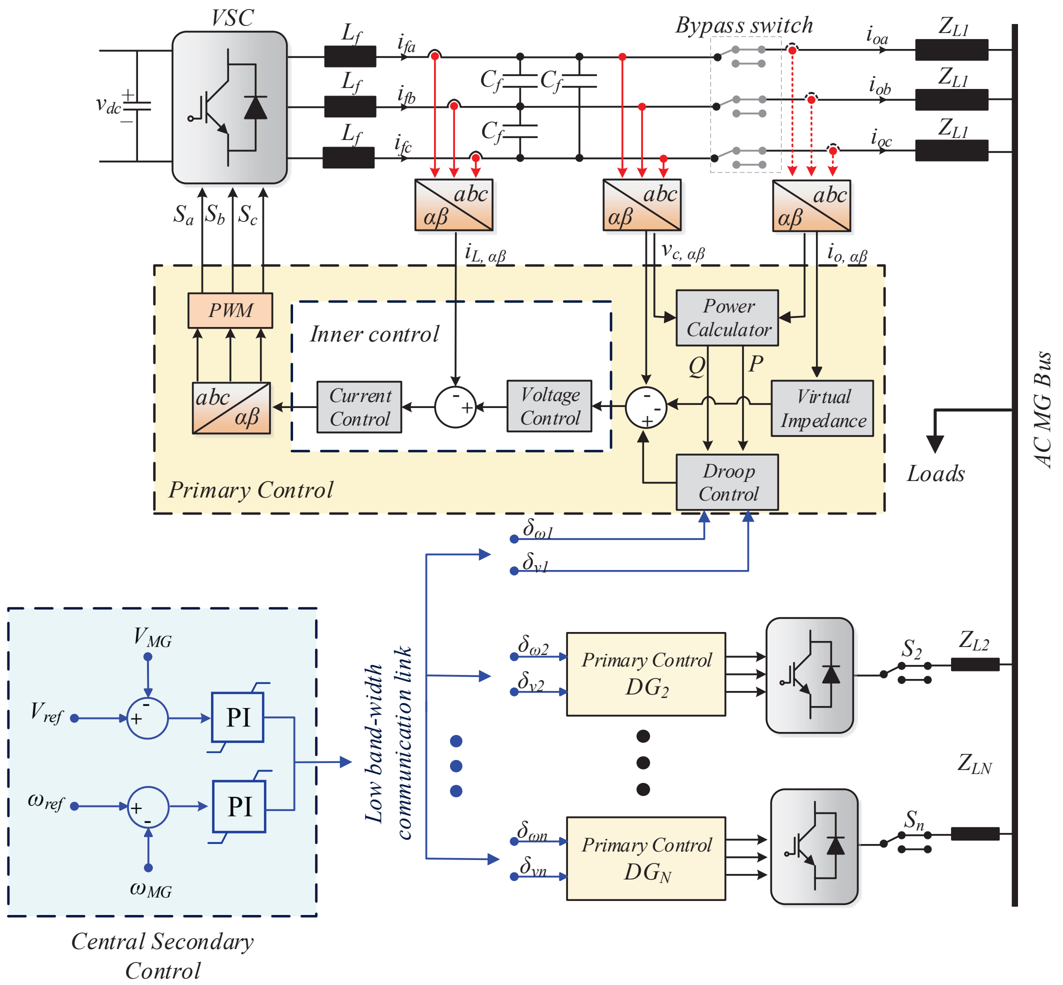

Fig. 1: Conventional primary and secondary control structures.

to parameter variations. Practically, slow response in MG with inherent low inertia will lead to voltage/frequency instability. Therefore, enhancing the response time is an excellent solution for compensating steady state errors rapidly.

In this paper, an alternative finite control set model predictive control (FCS-MPC) structure is proposed to address the aforementioned deficiencies. By applying modern microprocessors and raw data processing, all the inner control loops are replaced with a single FCS-MPC loop. This approach not only decreases the MG response time but compensate also the frequency and voltage deviations promptly. Practically, the proposed control scheme regulates voltage and frequency in distributed fashion, much faster than state of the art.

Conventional Control Structure

The foundation of a conventional control structure is illustrated in Fig. 1. As it can be seen, voltage and current control loops are applied as the inner controllers [18]. Furthermore, a droop characteristic methodology is implemented to share the power among the VSCs accurately. If VSCs are considered as an ac source with an amplitude of V_i and power angle of δ_i, then the power exchange (active/reactive) between the VSC and ac bus can be formulated as follows:

$$V_{MG}I_i^* = \frac{V_{MG}V_i\measuredangle(\theta_i-\delta_i)}{Z_L} - \frac{V_{MG}^2\measuredangle\theta}{Z_L}. \tag{1}$$

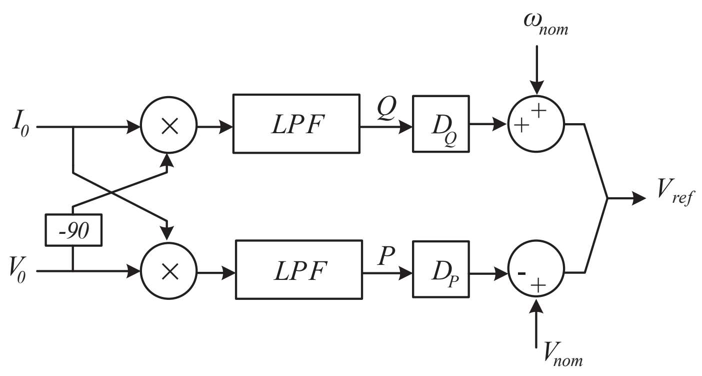

Fig. 2: Droop control structure.

Where $V_{MG}\measuredangle 0$ refers to MG common bus voltage and connection impedance is $Z_{L_i}\measuredangle\theta_i$. Therefore, the active and reactive power exchange can be achieved from (2) and (3) respectively by:

$$P = \frac{V_{MG}V_i}{Z_{L_i}}\cos(\theta-\delta_i) - \frac{V_{MG}^2}{Z_{L_i}}cos(\theta), \tag{2}$$

$$Q = \frac{V_{MG}V_i}{Z_{L_i}}\sin(\theta-\delta_i) - \frac{V_{MG}^2}{Z_{L_i}}sin(\theta_i). \tag{3}$$

The droop control characteristic has different forms according to the type of line and output impedance. Although the virtual impedance can be implement as a inductive or resistive impedance, it is better to utilize a more resistive. Since the value of such virtual impedance does not depend on nonlinear load and frequency changes[19]. Thus, in such a system active and reactive power exchange can be controlled based on the $Q-\omega$ and $P-V$ droop control characteristics. Consequently, (2) and (3) can be simplified to:

$$\begin{cases}\omega_{ref} = \omega_{nom} + D_Q Q \\ V_{ref} = V_{nom} - D_P P\end{cases}, \tag{4}$$

where, ω_{nom} and V_{nom} are nominal frequency and voltage amplitude of VSC at the no load, whereas, ω_{ref} and V_{ref} refer to the reference frequency and voltage amplitude correspondingly.

In the conventional SCL, the voltage of each VSC and frequency of MG is compared with the reference value and then, proper signals are sent to VSCs in order to compensate for voltage and frequency deviations. In contrast to PCL, a low bandwidth communication link is used in SCL to transfer the required data (frequency and voltage) among DGs. The control signals can be achieved from (5) and (6).

$$\Delta\omega_{sec} = k_{P_\omega}(\omega_{ref}-\omega_{MG}) + k_{I_\omega}\int(\omega_{ref}-\omega_{MG})dt, \tag{5}$$

$$\Delta v_{sec} = k_{P_v}(V_{ref}-V_{MG}) + k_{I_v}\int(V_{ref}-V_{MG})dt, \tag{6}$$

where, k_{P_ω} and k_{I_ω} are the constants of PI for voltage controller and k_{P_v} and k_{I_v} refer to PI coefficients of the frequency controller respectively. The proper signals to compensate for voltage and frequency (Δv_{sec} and $\Delta\omega_{sec}$) are sent to droop controllers of each VSCs to regulate steady state error.

When the conventional cascaded linear control structure is applied, the calculated power in the inner loop should be processed before the application to (5) and (6) through low-pass filters with bandwidth lower than internal loops. This inherent filtering not only limits the allowed SCL bandwidth, but it also leads to the slow response time intensely, especially during load transients.

Proposed Control based on the Robust Finite Control Set MPC

In the distributed manner, the PCL and SCL are utilized together as a local controller. Furthermore, a communication link at the upper level shares the required measurements among SCL of each DER. By applying FCS-MPC, inner control loops are avoided. Therefore, voltage and frequency regulation are performed at the upper bandwidth limit which is defined by the physical parameters of MG. Furthermore, a number of control objectives and constraints can be explicitly included in a simple and intuitive way, while the response speed of the system to external disturbances is not limited by the low pass filtering behavior characteristic to conventional linear cascaded control loops.

Operating principle of FCS-MPC

The MPC approach mainly relies on prediction and how the control signals affect on the system. FCS-MPC takes advantage of discrete nature of the power converter and known model of its output filter to explicitly find the converter switch configuration which minimizes a certain cost function at every sampling time instant. Consequently, predicted signals that minimize the cost function will be implemented. This cost function typically reflects one or more imposed control objectives and the process will be repeated for the next sampling time. In order to increase accuracy of the proposed technique, a comprehensive model of VSCs and feasible control signals have to be scrutinized. Two level converter comprises three phase legs (a, b and c). Each leg consists of upper and lower switch which are controlled by external gating signals. Voltages v_a, v_b, v_c and currents i_a, i_b, i_c in paralleled three phase VSCs are modeled in $\alpha-\beta$ orthogonal reference frame by applying Clarke transformation $\bar{T}$:

$$\begin{cases} \bar{v} = v_\alpha + jv_\beta = \bar{T}[v_a \quad v_b \quad v_c]' \\ \bar{i} = i_\alpha + ji_\beta = \bar{T}[i_a \quad i_b \quad i_c]' \end{cases}, \tag{7}$$

where,

$$\bar{T} = \frac{1}{3}[1 \quad e^{j\frac{2}{3}\pi} \quad e^{j\frac{4}{3}\pi}]. \tag{8}$$

In order to model the switching configuration of a two-level three phase VSC, three gating signals S_a, S_b and S_c are defined as a binary variables of 0 and 1 as follow:

$$S_x = \begin{cases} 1, & \text{if } \mathrm{S_{1x}} \text{ is on and } \mathrm{S_{2x}} \text{ is off} \\ 0, & \text{if } \mathrm{S_{1x}} \text{ is off and } \mathrm{S_{2x}} \text{ is on}, x \in a,b,c \end{cases} \tag{9}$$

Consequently, all feasible switching states will be eight (2^3) configurations. By using Clark transformation, the corresponding voltage vector v will be achieved in a new reference frame of the $\alpha-\beta$ frame. The major objective of the FCS-MPC approach is to accurately select the voltage input vector v, hence, the output voltage v_f follows the reference trajectory v_f^* successively with a minimum error. Thus, the cost function for the prediction horizon of N time steps can be formulated as follows:

$$CF : \sum_{i=k}^{k+N-1} (\|\overline{v}_e(i)\|^2 + h_{lim}(i) + \lambda.sw^2(i)), \tag{10}$$

where $\overline{v}_e(i)$ is the Euclidean distance error for predicted tracking N time steps, $h_{lim}(i)$ imposes the current constraint, and the last term shows the switching effort (sw) with a weighting factor (λ) which reduce the switching frequency and total harmonic distortion (THD). In order to decrease high THD, an apt regulator should follow the voltage reference and its derivative simultaneously [20, 21]. Therefore, another term is added to the cost function to minimize voltage derivative error as well. Therefore, the cost function can be modified as follows:

$$CF : \|\overline{v}_e(i)\|^2 + h_{lim}(i) + \lambda_w sw^2(i)) + G_d, \tag{11}$$

$$\overline{v}_e(i) = \overline{v}_f^*(i) - \overline{v}_e(i), \tag{12}$$

$$h_{lim}(i) = \begin{cases} 1, & \text{if } |i_f(i)| \leq i_{max} \\ \infty, & \text{if } |i_f(i)| > i_{max} \end{cases}, \tag{13}$$

$$sw(i) = \sum |u(i) - u(i-1)|, \tag{14}$$

$$G_d = \left(\frac{d\overline{v}_f^*(t)}{dt} - \frac{d\overline{v}_f(t)}{dt} \right) = (C_f \omega_{ref} v_{f\beta}^* - i_{f\alpha} + i_{o\alpha})^2 + (C_f \omega_{ref} v_{f\alpha}^* - i_{f\beta} + i_{o\beta})^2, \tag{15}$$

where G_d demonstrated the derivative error. Worth to note that the reference voltage is determined in the upper level through droop control and virtual impedance.

Distributed secondary control of MG frequency and voltage

In distributed SCL, each DG collects all measured data from other VSCs via a communication link at the upper control level. Then, transferred data are averaged, and SCL send a proper signal to the PCL to change the references. Frequency compensatory signal can be achieved from (16):

$$\delta_{\omega_{DG_k}} = k_{p_\omega}(\omega_{ref} - \overline{\omega}_{DG_k}) + k_{i_\omega} \int (\omega_{ref} - \overline{\omega}_{DG_k}) dt, \tag{16}$$

$$\overline{\omega}_{DG_k} = \frac{\sum_{i=1}^{N} \omega_{DG_i}}{N}, \tag{17}$$

while $\overline{\omega}_{DG_k}$ and ω_{ref} are the averages of frequency for all DGs and set point frequency of MG respectively. Obviously, $\delta_{\omega_{DG_k}}$ is a regulating signal sent from the local SCL to PCL in every sampling time, and N is the number of DGs.

A similar signal should be sent from the SCL to compensate for the voltage deviations caused by the PCL.

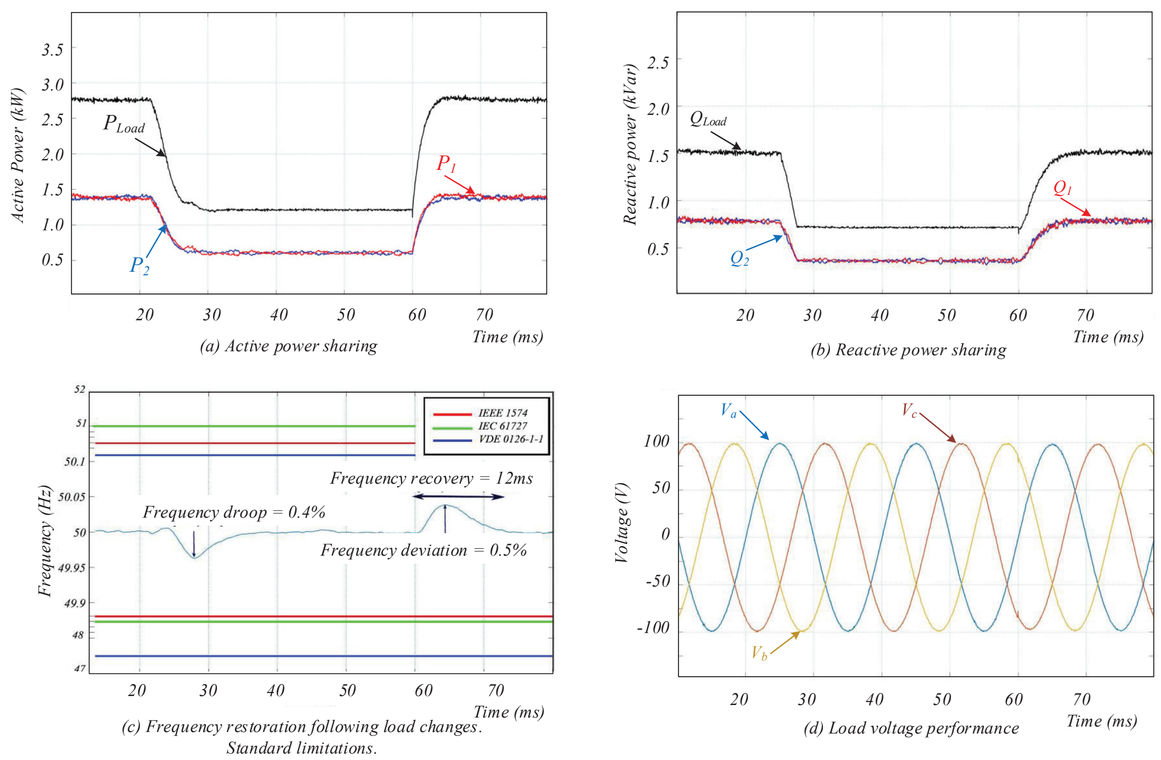

Fig. 3: Simulation validation of the proposed approach: (a) Active power sharing. (b) Reactive power sharing. (c) Frequency restoration. (d) Load voltage performance.

$$\delta_{V_{DG_k}} = k_{pV}(V_{ref} - \overline{V}_{DG_k}) + k_{iV}\int(V_{ref} - \overline{V}_{DG_k})dt, \tag{18}$$

$$\overline{V}_{DG_k} = \frac{\sum_{i=1}^{N} V_{DG_i}}{N}, \tag{19}$$

where $\overline{V}_{DG_k}$ refers to the average of voltages broad casted from each VSC in every sampling time. The proposed signals are applied to the $P-V$ and $Q-\omega$ primary droop control (see Fig. 1).

Simulation and Experimental Results

In order to evaluate the effectiveness of the proposed control structure, an islanded case study MG consists of two DGs is considered. The nominal simulation parameters are summarized in the Table I. It is worth to note that the parameters are selected similar with the literature to have a comprehensive comparison (e.g [17]). Two load changes have been carried out at $t = 20$ ms and $t = 60$ ms.

The major approaches are demonstrated in Fig. 3, which shows fast and accurate power sharing (Fig. 3(a) and (b)). Moreover, frequency regulation with a high performance margin with IEC 62040 and IEEE 1574 standards is shown in Fig. 3 (c). The three phase load voltages are given in Fig. 3 (d). Note that frequency restoration and power sharing in [17] Fig. 14 and 15 are in order of several seconds. Simulation results illustrate the two VSCs share the power accurately during the transient period with super fast dynamic response compared to the literature approaches.

The performance of the proposed approach is also evaluated practically by applying two Semikron 18 kW-VSCs with Schaffner LC filter. A DC power supply (Delta Elektronika SM600-10) is utilized as a

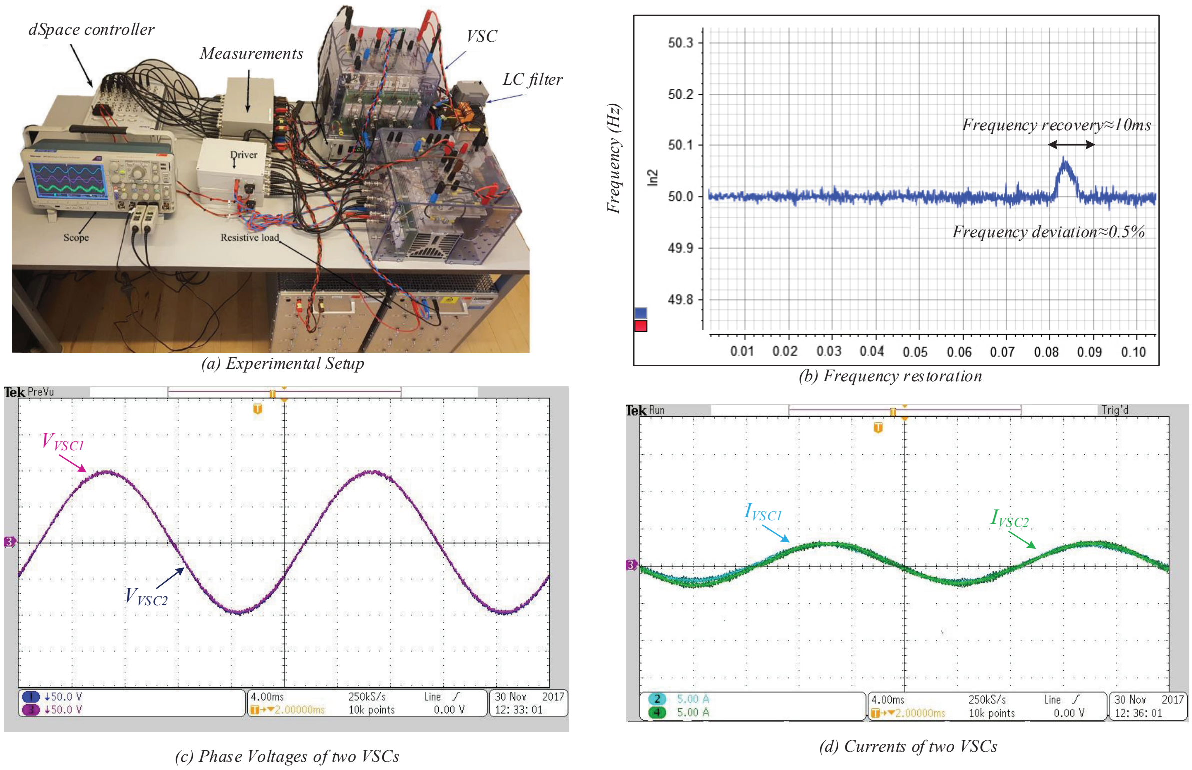

Fig. 4: Simulation and experimental validation of the proposed approach: (a) Photo of experimental setup; (b) Frequency restoration; (c) Voltage amplitude of two VSCs; (d) Measured phase output currents of two VSCs.

main source and the converters are controlled with a real time 1202 dSPACE platform. The experimental setup is demonstrated in Fig. 4(a), the sampling time for the proposed FCS-MPC algorithm is T_s = 25 μs, v_{dc} = 300 V, and *LCL*-filter with L_f = 2.4 mH, C_f = 13.5 μF and L_{oi} = 1.8 mH is utilized. In order to validate the effectiveness of the proposed strategy, a step load change is carried out. Fig. 4(b) shows Measured frequency restoration following a load step (from the dSPACE). Fig. 4(c) and (d) show measured phase voltages and output currents of the two VSCs respectively. As it can be seen from Fig. 4 performance of the system durring transient period and steady state is acceptable.

Conclusion

In this paper, a predictive control structure for VSC-based MG is suggested. This approach enables distributed SCLs to compensate voltage and frequency deviations with high bandwidth and super fast response rates compared to the conventional linearized cascaded control strategy suggested in the lit-

Table I: PARAMETERS OF THE TEST SYSTEM.

Parameter	Symbol	Value
DC Voltage	V_{dc}	300 V
Nominal voltage amplitude	V_{nom}	100 V
Nominal frequency	f_{nom}	50 Hz
LC filter	$L_f,\ C_f$	$L_f = 2.4\ mH,\ C_f = 13.5\ \mu F$
Sampling time	T_s	25 μs
Droop coefficients	$D_p,\ D_q$	$D_p = 0.005\ V/W,\ D_q = 0.002\ rad/sVar$
Line impedance	$R_l,\ L_l$	$R_l = 0.1\ \Omega,\ L_l = 2.4\ mH$
Virtual resistance	R_v	2 Ω

erature. Furthermore, this approach enhances the system performance with a large margin according to three standards. In particular, a FCS-MPC approach is utilized at the inner loop. Practically, two three-phase VSCs with *LC* filters supply a load with rapid changes. Simulation and experimental results show fast and accurate power sharing as well as acceptable voltage and frequency regulation. Since SCL bandwidth is limited by the dynamic response of the inner primary control loops, by utilizing proposed approach, SCL allows to regulate frequency and voltage with much higher bandwidth.

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