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A Fixed-Length Transfer Delay-based Adaptive Frequency Locked Loop for Single-Phase Systems

Zhiyong Dai, Zhen Zhang, Yongheng Yang, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, Yigeng Huangfu, *Senior Member, IEEE*, Juxiang Zhang

***Abstract*— This letter presents an adaptive frequency locked loop with fixed-length transfer delay units for single-phase systems. By analyzing the relationship between the grid voltage and its transfer delay signals, a linear regression model of the grid voltage is established. Accordingly, a transfer delay-based adaptive frequency locked loop (TD-AFLL) is proposed. A mathematic proof indicates that the proposed TD-AFLL can reject both phase offset errors and double-frequency oscillatory errors. Thus, the grid voltage parameters can be estimated accurately, even when the frequency drifts away from its nominal value. Moreover, fast dynamics of the TD-AFLL are achieved due to the transfer delay structure. Experiments verify the effectiveness of the proposed method.**

***Index Terms*— Frequency locked loop (FLL), fixed-length transfer delay, single-phase systems, grid synchronization, frequency variations.**

I. Introduction

In the past decades, single-phase inverters for vehicle-to-grid/ grid-to-vehicle devices and small-scale photovoltaic systems have been extensively developed. In grid-connected applications, the grid current has to be synchronized with the grid voltage. The grid synchronization typically estimates the frequency, amplitude, and phase angle of the grid voltage [1]. To achieve so, many methods are proposed in the literature. Among those, phase locked loops (PLLs) are one of the favorites [2]-[6]. For instance, the transfer delay-based PLL (TD-PLL), inverse-park transformation-based PLL (IPT-PLL), generalized integrator-based PLL (GI-PLL), and enhanced PLL (EPLL) are a few PLL-synchronization representatives.

Additionally, the TD-PLL creates fictitious orthogonal signal using a simple transfer delay block, and thus it has low computational burden and fast dynamics. However, it suffers from phase offset errors and double-frequency oscillatory errors, when the grid frequency drifts away from its nominal (it is practical in grid-connected applications) [6]. To tackle this issue, an improved method called the non-frequency-dependent TD-PLL (NTD-PLL) has been proposed [7], [8], which adds another transfer delay block as a new feedback path to reject the phase offset error. However, the double-frequency error impact remains, and thus the NTD-PLL has steady-state errors when the grid frequency shifts away from its nominal value. In [9], another advanced TD-PLL was introduced to adjust the delay length of the TD block based on the estimated grid frequency, and it improves the steady-state estimation accuracy when the grid frequency drifts. Yet, the time-varying TD block may challenge the stability. Furthermore, in [6], a novel quadrature-signal-generator (QSG), called adaptive transfer delay (ATD), was developed. It effectively suppresses the phase offset and double-frequency oscillatory errors.

It should be noted that frequency locked loops (FLLs) can also be adopted to achieve advanced grid synchronization. For instance, the second-order generalized integrator FLL (SOGI-FLL) is a typical FLL, which achieves the parameter estimation of the grid voltage [10], [11].

However, the TD-PLL methods are still the favorites due to the simplicity, and the TD-FLL grid-synchronization has not yet been reported. In light of this, a transfer delay-based adaptive frequency locked loop (TD-AFLL) is proposed in this letter to fill this gap. Compared with the TD-PLLs, the proposed TD-AFLL applies two fixed-length transfer delay blocks to the grid voltage and establishes the first-order linear regression model with the relationship between the grid voltage and its transfer delay signals. Accordingly, an adaptive identification method is developed to estimate the grid voltage parameters. A strict mathematic proof is provided in this letter, implying that the proposed TD-AFLL can estimate the grid voltage parameters accurately when the grid frequency drifts. Experimental results also demonstrate the superior performance of the proposed TD-AFLL in terms of fast dynamics and high accuracy.

II. Linear Regression Model of the Grid Voltage

In single-phase systems, the grid voltage can be given as

$$v(t) = V\sin\left(\omega t + \phi\right) = V\sin\psi \tag{1}$$

where ω, V, and ψ is the frequency, amplitude, and phase angle of the grid voltage, respectively. Discretizing the grid voltage with the sample time T_s yields

$$v(k) = V\sin\left(\omega k T_s + \phi\right),\quad k = 0,1,2,... \tag{2}$$

Similar to the prior-art TD-PLLs, two transfer delay units are applied to the discretized grid voltage $v(k)$. They can be expressed as

$$v_1\left(k\right) = v\left(k - \frac{T_0}{4T_s}\right) = V\sin\left(\omega k T_s - \frac{\omega T_0}{4} + \phi\right) \tag{3}$$

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Z. Dai and J. Zhang are with the School of Mechanical and Electrical Engineering, Xidian University, Xi'an 710071, China (e-mail: zydai@xidian.edu.cn; jxzhang@mail.xidian.edu.cn).

Z. Zhang and Y. Huangfu are with School of Automation, Northwestern Polytechnical University, Xi'an 710129, China (e-mail: zhangzhen_nwpu@163.com; yigeng@nwpu.edu.cn).

Y. Yang and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, DK-9220 Aalborg, Denmark (e-mail: yoy@et.aau.dk; fbl@et.aau.dk).

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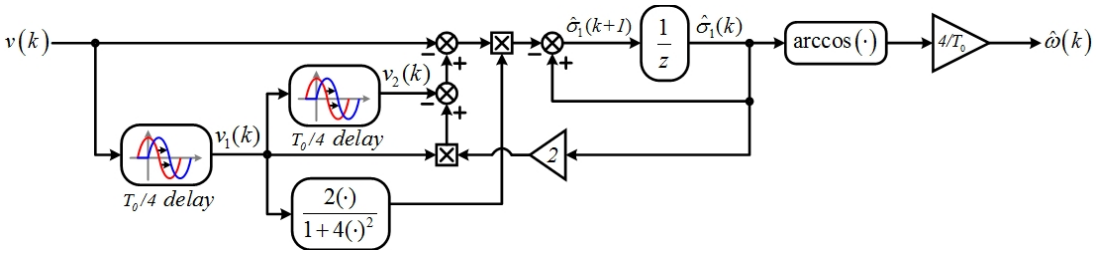

Fig. 1. Structure of the proposed transfer delay-based adaptive frequency locked loop (TD-AFLL).

$$v_2(k)=v\left(k-\frac{T_0}{2T_s}\right)=V\sin\left(\omega kT_s-\frac{\omega T_0}{2}+\phi\right) \tag{4}$$

in which $k = 0, 1, 2, \ldots$ and T_0 is the nominal period of the grid voltage. Eqs. (3) and (4) can be further expressed as

$$v_1(k)=\sigma_1 V\sin(\omega kT_s+\phi)-\sigma_2 V\cos(\omega kT_s+\phi) \tag{5}$$

$$v_2(k)=\sigma_3 V\sin(\omega kT_s+\phi)-\sigma_4 V\cos(\omega kT_s+\phi) \tag{6}$$

where σ_1, σ_2, σ_3, σ_4 are coefficients that can be calculated by

$$\sigma_1=\cos\frac{\omega T_0}{4}\ ,\ \sigma_2=\sin\frac{\omega T_0}{4} \tag{7}$$

$$\sigma_3=\cos\frac{\omega T_0}{2}\ ,\ \sigma_4=\sin\frac{\omega T_0}{2} \tag{8}$$

and furthermore,

$$\sigma_3=2\sigma_1^2-1\,,\quad \sigma_4=2\sigma_1\sigma_2 \tag{9}$$

Since $0<\omega T_0/4<\pi$, the following holds:

$$\sigma_2\neq 0 \tag{10}$$

Substituting (2) into (5) and (6) gives

$$\sigma_2 V\cos(\omega kT_s+\phi)=\sigma_1 v(k)-v_1(k) \tag{11}$$

$$\sigma_4 V\cos(\omega kT_s+\phi)=\sigma_3 v(k)-v_2(k) \tag{12}$$

According to (7)-(12), it can be obtained that

$$v(k)+v_2(k)=2\sigma_1 v_1(k) \tag{13}$$

Eq. (13) is the linear regression model of the grid voltage $v(k)$, which describes the relationship among the grid voltage and its transfer delay signals. Clearly, in (13), $v(k)$ is measurable, $v_1(k)$ and $v_2(k)$ are available through the transfer delay blocks, and σ_1 is the unknown parameter related to the grid frequency ω. Obviously, once σ_1 is estimated accurately, the grid voltage frequency ω can be calculated, i.e., the synchronization is achieved. With σ_1 and ω, the amplitude and phase angle can be obtained (e.g., following (23)-(25)).

III. Proposed TD-AFLL Algorithm

In this section, based on the linear model (13), the TD-AFLL is proposed to estimate the unknown parameter σ_1 and the grid voltage frequency ω, and then the amplitude and phase angle are also obtained accurately. Firstly, the TD-AFLL is designed as

$$\hat{\sigma}_1(k+1)=\hat{\sigma}_1(k)-\frac{2v_1(k)}{1+4v_1^2(k)}\left(2\hat{\sigma}_1(k)v_1(k)-v(k)-v_2(k)\right) \tag{14}$$

$$\hat{\omega}(k)=\frac{4\arccos\left(\hat{\sigma}_1(k)\right)}{T_0} \tag{15}$$

where $\hat{\sigma}_1(k)$ and $\hat{\omega}(k)$ are the estimates of σ_1 and ω, respectively. Subsequently, the structure of the TD-AFLL is shown in Fig. 1. Next, a strict derivation is provided to prove that Eq. (14) and (15) are a frequency locked loop and the TD-AFLL estimates the grid frequency with zero steady-state errors.

First, consider the estimation error as

$$\tilde{\sigma}_1(k)=\hat{\sigma}_1(k)-\sigma_1 \tag{16}$$

Then, according to (13)-(16), it is derived that

$$\begin{aligned}\tilde{\sigma}_1(k+1)&=\hat{\sigma}_1(k+1)-\sigma_1\\&=\hat{\sigma}_1(k)-\sigma_1-\frac{2v_1(k)}{1+4v_1^2(k)}\left(2\hat{\sigma}_1(k)v_1(k)-v(k)-v_2(k)\right)\\&=\tilde{\sigma}_1(k)-\frac{2v_1(k)}{1+4v_1^2(k)}\left(2\hat{\sigma}_1(k)v_1(k)-2\sigma_1 v_1(k)\right)\\&=\tilde{\sigma}_1(k)-\frac{4v_1^2(k)}{1+4v_1^2(k)}\tilde{\sigma}_1(k)\\&=\frac{1}{1+4v_1^2(k)}\tilde{\sigma}_1(k)\end{aligned} \tag{17}$$

Iterating (17) yields

$$\begin{aligned}\tilde{\sigma}_1(k)&=\frac{1}{1+4v_1^2(k-1)}\tilde{\sigma}_1(k-1)\\&=\frac{1}{1+4v_1^2(k-1)}\frac{1}{1+4v_1^2(k-2)}\tilde{\sigma}_1(k-2)=\cdots\\&=\frac{1}{1+4v_1^2(k-1)}\frac{1}{1+4v_1^2(k-2)}\cdots\frac{1}{1+4v_1^2(0)}\tilde{\sigma}_1(0)\end{aligned} \tag{18}$$

where $\tilde{\sigma}_1(0)$ is the initial estimation error and $v_1(0)$ is the initial transfer delay voltage of v_1.

For convenience, it is assumed that there are m non-zeros in $\{v_1(0), v_1(1), \ldots, v_1(k-1)\}$ and these are referred as $v_1(i_1)$, $v_1(i_2)$, …, $v_1(i_m)$. Among the non-zero elements, the minimum is denoted as $v_{1\min}(i)$.

Obviously, when $v_1(j)=0$ with $j\in\{0, 1, \ldots, k-1\}$, $1/(1+4v_1^2(j))=1$. With the above assumption, $\tilde{\sigma}_1(k)$ is rewritten as

$$\tilde{\sigma}_1(k)=\frac{1}{1+4v_1^2(i_1)}\frac{1}{1+4v_1^2(i_2)}\cdots\frac{1}{1+4v_1^2(i_m)}\tilde{\sigma}_1(0) \tag{19}$$

Applying the absolute value operation yields

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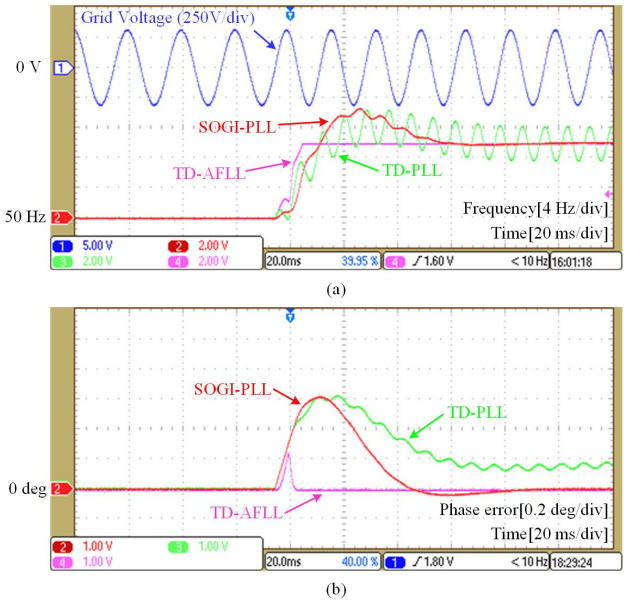

Fig. 2. Experimental results for a 10-Hz frequency jump in the grid voltage (from 50 Hz to 60 Hz). (a) Estimated grid frequency. (b) Estimation error of the phase angle.

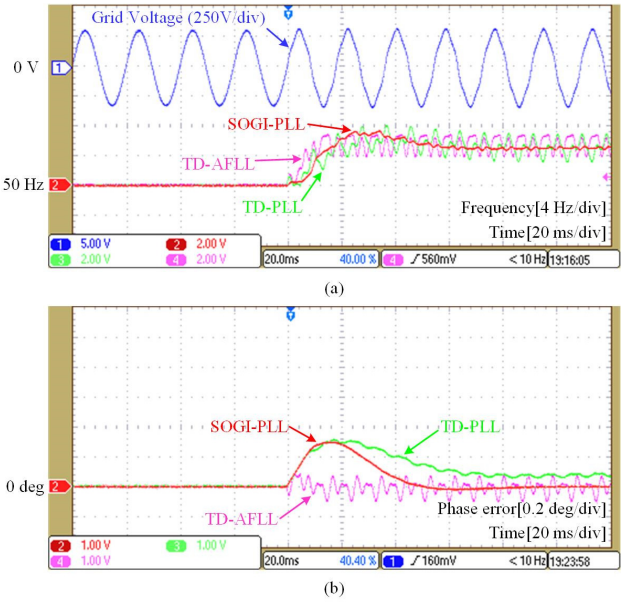

Fig. 3. Experimental results under grid harmonic disturbances (0.05 p.u. for the 5th- and 0.01 p.u. for the 7th- harmonics) and frequency jump (from 50 Hz to 55 Hz). (a) Estimated grid frequency. (b) Estimation error of the phase angle.

$$\left|\tilde{\sigma}_1(k)\right| = \left|\frac{1}{1+4v_1^2(i_1)}\frac{1}{1+4v_1^2(i_2)}\cdots\frac{1}{1+4v_1^2(i_m)}\tilde{\sigma}_1(0)\right| \le \left|\left(\frac{1}{1+4v_{1\min}^2(i)}\right)^m\left|\tilde{\sigma}_1(0)\right|\right| = \left(\frac{1}{1+4v_{1\min}^2(i)}\right)^m\left|\tilde{\sigma}_1(0)\right| \tag{20}$$

Meanwhile, according to the definition of $v_1(k)$ in (3), it is observed that m will be infinite when k is infinite. It can be obtained that

$$\lim_{k\to+\infty}\left|\tilde{\sigma}_1(k)\right| = \lim_{m\to+\infty}\left|\frac{1}{1+4v_1^2(i_1)}\frac{1}{1+4v_1^2(i_2)}\cdots\frac{1}{1+4v_1^2(i_m)}\tilde{\sigma}_1(0)\right| \le \lim_{m\to+\infty}\left(\frac{1}{1+4v_{1\min}^2(i)}\right)^m\left|\tilde{\sigma}_1(0)\right| \tag{21}$$

Since $0<1/\left(1+4v_{1\min}^2(i)\right)<1$, it yields

$$\lim_{k\to+\infty}\left|\tilde{\sigma}_1(k)\right| \le \lim_{m\to+\infty}\left(\frac{1}{1+4v_{1\min}^2(i)}\right)^m\left|\tilde{\sigma}_1(0)\right| = 0 \tag{22}$$

In other words, (14) can estimate the unknown parameter σ_1 with zero steady-state errors. Based on the obtained $\hat{\sigma}_1$ and the definition of σ_1 in (7), (15) also achieves zero steady-state estimation of the frequency. In that way, an adaptive frequency locked loop is established.

Furthermore, according to (11), the orthogonal signal of the grid voltage $v(k)$ is obtained by

$$\hat{v}_\perp(k) = \frac{\hat{\sigma}_1 v(k) - v_1(k)}{\sin\left(\hat{\omega}T_0/4\right)} \tag{23}$$

where $\hat{v}_\perp(k)$ is the estimated orthogonal signal of the grid voltage. The amplitude and phase angle can be obtained as

$$\hat{V}(k) = \sqrt{v^2(k)+\hat{v}_\perp^2(k)} \tag{24}$$

$$\hat{\psi}(k) = \arctan\frac{v(k)}{\hat{v}_\perp(k)} \tag{25}$$

In summary, the frequency, amplitude, and phase angle of the grid voltage can be accurately estimated by the proposed TD-AFLL, following (14), (15) and (23)-(25).

IV. Experimental Results

In this section, the performance of the proposed TD-AFLL has been evaluated by experiments under several abnormal grid conditions. For comparison, the conventional TD-PLL and SOGI-PLL are also implemented and tested. The parameters of SOGI-PLL are chosen as: $k = 1.414$, $k_p = 92$ and $k_i = 4232$. The sampling frequency is fixed at 10 kHz. Various cases are tested, and the algorithms are implemented in a dSPACE system. The grid voltage is generated by a programmable power supply.

Fig. 2 shows the experimental results for a 10-Hz frequency jump in the grid voltage (from 50 Hz to 60 Hz). It can be observed that the proposed TD-AFLL has fast dynamics and small overshoots, compared with the other two PLL's. It takes less than one cycle of the nominal period to reach the steady state with zero steady-state errors and no double-frequency ripples. However, the TD-PLL presents a double-frequency variation, while the SOGI-PLL has relatively slower dynamics and higher overshoots.

Fig. 3 shows the experimental results under grid harmonic disturbances (0.05 p.u. for the 5th- and 0.01 p.u. for the 7th-harmonics are present in the grid voltage) and frequency jump (from 50 Hz to 55 Hz). Observations in Fig. 3 indicate that the proposed TD-AFLL has a fast dynamic response and small overshoot. Compared to the conventional TD-PLL, it removes the phase-offset error in the phase angle estimation. However, in terms of harmonic immunity, the SOGI-PLL is the best among the benchmarked methods. This is because the high

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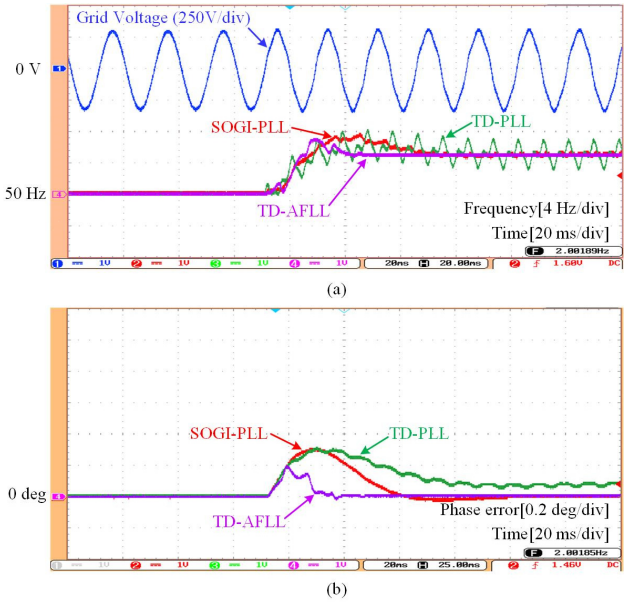

Fig. 4. Experimental results of the proposed TD-AFLL with an observer-based filter under grid harmonic disturbances (0.05 p.u. for the 5th-order and 0.01 p.u. for the 7th-order harmonics) and frequency jump (from 50 Hz to 55 Hz). (a) Estimated grid frequency. (b) Estimation error of the phase angle.

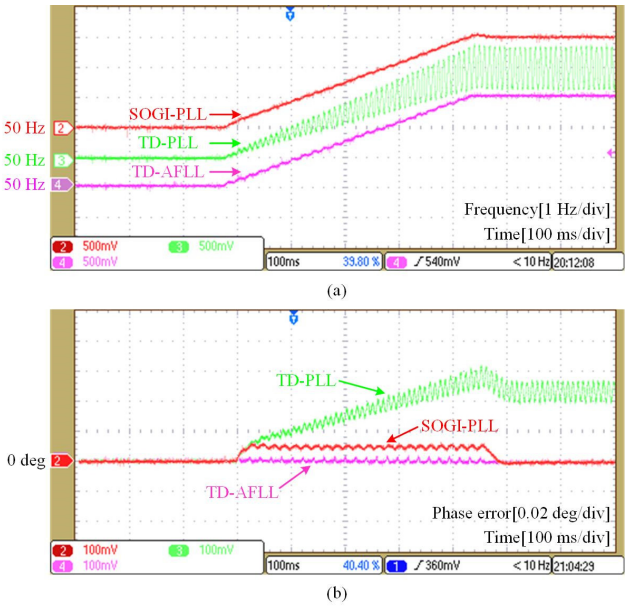

Fig. 5. Experimental results when the grid voltage undergoes a ramp-up change from 50 Hz to 53 Hz. (a) Estimated grid frequency. (b) Estimation error of the phase angle.

filtering characteristics of the SOGI used in this PLL, which also lead to slow dynamics to certain extent.

In order to improve the harmonic rejection capability of the proposed TD-AFLL, additional filters can be adopted. For example, an observer-based filter [12] (detailed in the Appendix) is added before the TD-AFLL and the experimental results are shown in Fig. 4. Here, the grid voltage with harmonics and frequency jump is the same as the case in Fig. 3. It is observed in Fig. 4 that the harmonic rejection capability of the proposed TD-AFLL is improved with the observer-based filter, thus consolidating the estimation of the frequency and

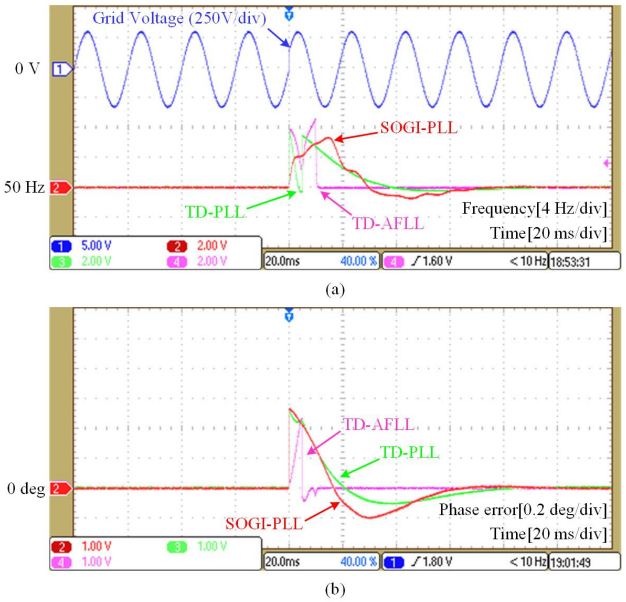

Fig. 6. Experimental results under a π/6-phase angle jump. (a) Estimated grid frequency. (b) Estimation error of the phase angle.

phase angle. Compared with the SOGI-PLL and TD-PLL, the proposed with the filter has the fastest dynamics.

Fig. 5 shows the experimental results when the grid voltage frequency undergoes a ramp-up change from 50 Hz to 53 Hz. This case is designed to demonstrate the performance of the synchronization algorithms under frequency drifts. Nevertheless, it can be seen in Fig. 5 that the proposed TD-AFLL can track the frequency change with zero phase-offset errors during the entire period, and it achieves zero steady-state errors.

Fig. 6 shows the experimental results when a π/6-phase angle jump occurs. It is observed in Fig. 6 that the TD-AFLL can estimate the frequency and phase angle with zero steady-state errors. Compared with the two PLLs, the fastest dynamics by the proposed are further confirmed.

In addition, the execution time of the TD-PLL, SOGI-PLL and TD-AFLL are 0.96 μs, 2.11 μs, and 1.97 μs, respectively. It demonstrates that the conventional TD-PLL has the least computation burden.

V. Conclusion

Different from the common TD-based grid synchronization methods (usually, PLL-based), this letter proposed an adaptive frequency locked loop with fixed-length transfer delay blocks (TD-AFLL) to estimate the grid voltage parameters, including the frequency, amplitude, and phase angle. Additionally, a mathematic model was established to describe the linear relationship between the grid voltage and its transfer delay signals, and then the TD-AFLL was proposed to estimate the grid voltage parameters with zero steady-state errors. Various cases (i.e., frequency jump, harmonics, frequency ramp-up, and phase angle jump) have been tested with the proposed TD-AFLL, which has demonstrated the effectiveness in terms of fast dynamics and relatively high accuracy. Notably, the harmonic immunity of the TD-AFLL is poor, and it can be enhanced by adding filters, as exemplified in this letter.

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APPENDIX

The added observer-based filter is

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + L\left(C\hat{x} - v\right) \\ v_{filter} &= \hat{x}_1 \end{aligned} \tag{A.1}$$

where v is the grid voltage, v_{filter} is the filtered grid voltage that is the input of the TD-AFLL, the state variable $\hat{x}=[\hat{x}_1,\ldots,\hat{x}_6]^T$, the matrixes $C = [1, 0, 1, 0, 1, 0]$, and

$$A = \begin{bmatrix} 0 & \hat{\omega} & 0 & 0 & 0 & 0 \\ -\hat{\omega} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 5\hat{\omega} & 0 & 0 \\ 0 & 0 & -5\hat{\omega} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 7\hat{\omega} \\ 0 & 0 & 0 & 0 & -7\hat{\omega} & 0 \end{bmatrix} \tag{A.2}$$

with $\hat{\omega}$ being the estimated frequency, and the filter parameter $\boldsymbol{L}$ is designed in a way that the poles of the matrix $\boldsymbol{A+LC}$ are set as $-1.8\omega_r \pm 1.8j\omega_r$, $-2\omega_r \pm 2j\omega_r$, and $-2.2\omega_r \pm 2.2j\omega_r$ with $\omega_r = 100\pi$ rad/s.

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