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Design and Analysis of a Transformerless STATCOM based on Hybrid Cascaded Multilevel Converter

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Abstract: This paper presents a new concept of Static Synchronous COMpensator (STATCOM) based on a Hybrid Cascaded Multilevel Converter (HCMC). The HCMC consists of a two- level voltage converter and a wave-shaping circuit formed by cascaded H-bridge Sub-Modules (SM). Firstly, the operation principle and overall control strategy of HCMC are presented. After that, some key parameters including size of capacitors, numbers of sub-modules are in-depth analyzed. And then, a thorough comparison between the proposed HCMC-based STATCOM and conventional cascaded H-bridge based STATCOM is made, which turns out that the proposed HCMC-based STATCOM requires less number, size and stored energy of capacitors and has less power loss. Finally, a 35kV/±50Mvar HCMC-based STATCOM simulation model is constructed in PSCAD/EMTDC software platform. The simulation results validate the feasibility of the proposed HCMC-based STATCOM and the correctness of the analysis.

Keywords: Hybrid Cascaded Multilevel Converter (HCMC), Static Synchronous COMpensator (STATCOM), sizing of capacitor, control strategy

1. INTRODUCTION

Static synchronous compensator (STATCOM) using voltage source converter is a flexible ac transmission system (FACTS) device for generating or absorbing reactive power. With reactive power compensation in power system, voltage regulation and maximum power transmission can be achieved [1] - [13].

Different kinds of STATCOMs have been tested and installed in many electrical networks during

the past few decades [1] - [5]. Many kinds of multilevel converters, such as 1) diode-clamped converter, 2) flying-capacitor converter, 3) cascaded H-bridge converter [7] - [13], modular multilevel converter (MMC) [14] – [17], alternate arm converter (AAC) [18] – [20], can be used as STATCOM. The multilevel structure provides redundancy and scalability. However, it requires a fairly large number of H-bridge sub-modules to reduce the harmonics and each sub-module requires a large DC capacitor.

This paper proposes a novel STATCOM based on hybrid cascaded multilevel converter (HCMC), which is a newly introduced voltage-source converter [21]. As shown in Fig.1, it has two key parts, i.e., the two-level converter and the wave-shaping circuit (WSC) containing cascaded H-bridge sub-modules. The two-level converter is arranged to operate at fundamental frequency with square-wave modulation, which reduces switching loss and simplifies dynamic voltage sharing along the series string of IGBTs [20]. The overall rating of the STATCOM is shared between the two-level converter and the wave-shaping circuit, with the result that fewer sub-modules are needed in the wave-shaping circuit in comparison with the cascaded H-bridge STATCOM. This is particularly beneficial in reducing the required number and rating of DC capacitors, which dominate the size and weight of the converters [21]. To achieve stable operation, the coordination and synchronization between the two-level converter and the wave-shaping circuit are required.

This paper focuses on the principle, control scheme of the proposed STATCOM and the sizing of the DC capacitors. The outline of this paper is organized as follows: The operation principle of the proposed STATCOM will be discussed in Section 2. Section 3 proposes a control scheme for this proposed STATCOM. Section 4 establishes the DC voltage ripple equations and the criterion for sizing the DC capacitors of the two-level converter and the wave-shaping circuit, respectively. Section 5 gives the comparison of the number of IGBTs and the number, size and stored energy of the DC capacitors between the proposed STATCOM and the cascaded H-bridge STATCOM. The feasibility of the HCMC-based STATCOM is verified by simulation results in Section 6. Section 7 concludes the paper.

2. PROPOSED STATCOM AND ITS OPERATION PRINCIPLE

2.1 Main Circuit Configuration

The three-phase main circuit configuration of the proposed STATCOM is illustrated in Fig.1. The WSC composed of the cascaded H-bridge sub-modules is placed on the AC side. Each arm of the two-level converter consists of series-connected IGBTs shown in Fig.1(a). Fig.1(b) illustrates the H-bridge structure, whose output voltage U_{HB} has three states: 1) $+U_c$; 2) $-U_c$; and 3) 0. Here, U_c is

the rated voltage of the capacitor. This means each sub-module has three states in normal operation: 1) positively inserted ($U_{HB} = U_c$); 2) negatively inserted ($U_{HB} = -U_c$); and 3) bypassed ($U_{HB} = 0$).

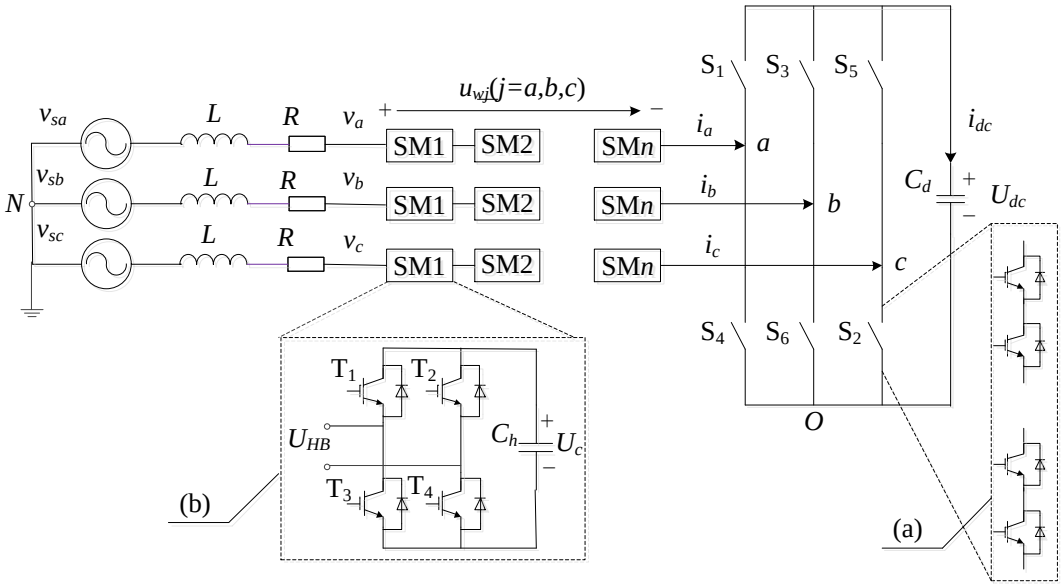


Fig.1. Main circuit configuration of proposed STATCOM. (a) IGBTs connected in series in the two-level converter. (b) H-bridge sub-module structure.

2.2 Operation Principle

The two-level converter is arranged to operate at fundamental frequency (50 Hz) by using square-wave modulation, producing a square wave at its AC terminal. The wave-shaping circuit constructs multilevel output voltage and compensates the difference between the output of the two-level converter and the desired (sinusoidal) voltage. It operates as a series active power filter to attenuate the voltage harmonics produced by the two-level converter. Thus, the output voltage of HCMC is almost purely sinusoidal, making a significant improvement compared to the traditional two-level converter.

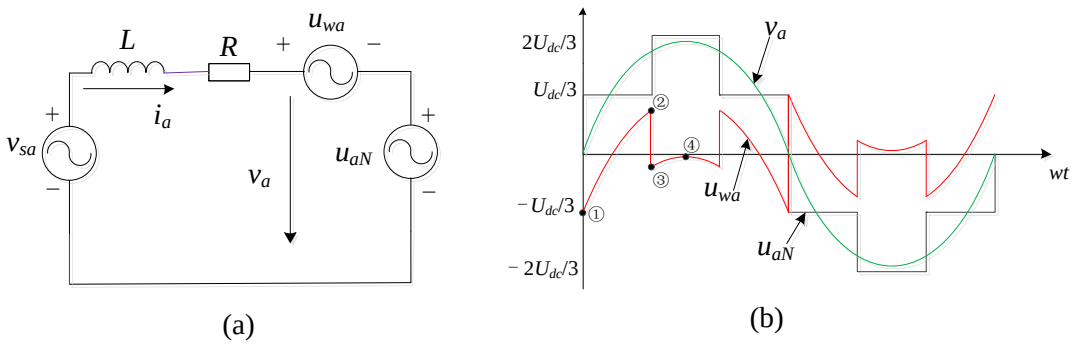


Fig.2. Single phase equivalent circuit and reference voltage waveforms. (a) Single phase equivalent circuit of the system. (b) Reference voltage waveforms

Fig.2 illustrates the basic single-phase equivalent circuit and reference voltage waveforms of the

STATCOM, where v_{sa} is the grid voltage of phase a, u_{aN} is the output voltage of the two-level converter in phase a, and L and R are the total equivalent AC inductance and resistance. From Fig.2 (a), the basic characteristics of the STATCOM can be described as follows:

$$v_{sa}(t) = U_{\mathrm{m}} \sin \omega t \tag{1}$$

$$i_a(t) = I_m \sin(\omega t + \pi/2) = I_m \cos \omega t \tag{2}$$

$$v_a(t) = u_{wa}(t) + u_{aN}(t) \tag{3}$$

$$u_{aN}(t) = M_a U_{dc} \tag{4}$$

$$u_{wa}(t) = \sum_{j=1}^{N} G_j U_{cj} \tag{5}$$

where U_m denotes the phase voltage amplitude, v_a is the output voltage of the STATCOM of phase a, I_m denotes the current amplitude, M_a denotes the switching factor which is determined by the states of the switches in the two-level converter, U_{dc} is the voltage of the DC capacitor of the two-level converter, N is the number of H-bridge sub-modules per phase, U_{cj} (j=1,2,…,N) is the capacitor voltage of the jth H-bridge sub-module, and G_j is the switching function corresponding to the three operation states of the jth H-bridge sub-module ,i.e., positively inserted (G_j=1), negatively inserted (G_j=-1), and bypassed (G_j=0).

2.3 Analysis of U_{dc} and N

When the number of the H-bridge sub-modules per phase N and the rated voltage of the H-bridge capacitors U_c are specified, the output voltage range of the cascaded H-bridge cells is determined as follow:

$$-NU_c \le u_{wa}(t) \le NU_c \tag{6}$$

According to (1), (3) and (4), neglecting the voltage drop on the inductor, u_{wa} can be obtained as

$$u_{wa}(t) = U_{\mathrm{m}} \sin \omega t - M_a U_{dc} \tag{7}$$

Then, substituting (7) into (6), equation (6) results in

$$-NU_c \le U_{\mathrm{m}} \sin \omega t - M_a U_{dc} \le NU_c \tag{8}$$

In (8), U_m is determined by the reactive power Q exchange between the STATCOM and the system. Therefore, if U_{dc} and N satisfy (8), the proposed STATCOM can operate stably. However, this may lead to high voltage of the two-level converter and many H-bridge sub-modules. To achieve low system cost and high performance of the proposed STATCOM, the values of U_{dc} and N need to be coordinated and optimized. In this paper, a method which can minimize the number of the H-bridge

sub-modules is proposed.

Since three phases are identical under symmetrical conditions, phase *a* is taken as an example and the following equations are given.

$$u_{aN} + u_{bN} + u_{cN} = 0 \tag{9}$$

The three-phase switching functions of the two-level converter are given by

$$S_a(\omega t) = \begin{cases} 1 & 0 \le \omega t < \pi \\ 0 & \pi \le \omega t < 2\pi \end{cases} \tag{10-a}$$

$$S_b(\omega t) = \begin{cases} 1 & 2\pi/3 \le \omega t < 5\pi/3 \\ 0 & 5\pi/3 \le \omega t < 8\pi/3 \end{cases} \tag{10-b}$$

$$S_c(\omega t) = \begin{cases} 1 & -2\pi/3 \le \omega t < \pi/3 \\ 0 & \pi/3 \le \omega t < 4\pi/3 \end{cases} \tag{10-c}$$

where $S_a(\omega t)$, $S_b(\omega t)$ and $S_c(\omega t)$ denote the three-phase switching functions of the two-level converter, respectively. Therefore, output voltages of the two-level converter referring to *O* can be calculated by

$$u_{ao}(\omega t) = S_a(\omega t)U_{dc} = \begin{cases} U_{dc} & 0 \le \omega t < \pi \\ 0 & \pi \le \omega t < 2\pi \end{cases} \tag{11-a}$$

$$u_{bo}(\omega t) = S_b(\omega t)U_{dc} = \begin{cases} U_{dc} & 2\pi/3 \le \omega t < 5\pi/3 \\ 0 & 5\pi/3 \le \omega t < 8\pi/3 \end{cases} \tag{11-b}$$

$$u_{co}(\omega t) = S_c(\omega t)U_{dc} = \begin{cases} U_{dc} & -2\pi/3 \le \omega t < \pi/3 \\ 0 & \pi/3 \le \omega t < 4\pi/3 \end{cases} \tag{11-c}$$

Regarding a fundamental cycle ($0 \sim 2\pi$), summing (11-a) to (11-c) gives

$$u_{ao}(\omega t) + u_{bo}(\omega t) + u_{co}(\omega t) = \begin{cases} 2U_{dc} & 0 \le \omega t < \pi/3 \\ U_{dc} & \pi/3 \le \omega t < 2\pi/3 \\ 2U_{dc} & 2\pi/3 \le \omega t < \pi \\ U_{dc} & \pi \le \omega t < 4\pi/3 \\ 2U_{dc} & 4\pi/3 \le \omega t < 5\pi/3 \\ U_{dc} & 5\pi/3 \le \omega t < 2\pi \end{cases} \tag{12}$$

Thus, [(9) – (12)]/3 gives

$$u_{oN}(\omega t) = \begin{cases} -2U_{dc}/3 & 0 \le \omega t < \pi/3 \\ -U_{dc}/3 & \pi/3 \le \omega t < 2\pi/3 \\ -2U_{dc}/3 & 2\pi/3 \le \omega t < \pi \\ -U_{dc}/3 & \pi \le \omega t < 4\pi/3 \\ -2U_{dc}/3 & 4\pi/3 \le \omega t < 5\pi/3 \\ -U_{dc}/3 & 5\pi/3 \le \omega t < 2\pi \end{cases} \tag{13}$$

Then, adding (11-a) to (13) gives

$$u_{aN}(\omega t)=\begin{cases} U_{dc}/3 & 0\le \omega t<\pi/3 \\ 2U_{dc}/3 & \pi/3\le \omega t<2\pi/3 \\ U_{dc}/3 & 2\pi/3\le \omega t<\pi \\ -U_{dc}/3 & \pi\le \omega t<4\pi/3 \\ -2U_{dc}/3 & 4\pi/3\le \omega t<5\pi/3 \\ -U_{dc}/3 & 5\pi/3\le \omega t<2\pi \end{cases} \tag{14}$$

According to (3), the voltage reference of WSC can be calculated by

$$u_{wa}(\omega t)=U_m\sin(\omega t)-u_{aN}(\omega t) \tag{15}$$

To minimize the number of H-bridge in WSC, the maximum value of the voltage generated by WSC $\left|u_{wa\_\max}\right|$ should be minimized. According to Fig.2 (b), the $\left|u_{wa\_\max}\right|$ can only appear at point ①, ②, ③ and ④, whose corresponding phase angle are 0, $\pi/3$, $\pi/3$ and $\pi/2$, respectively. Thus, substituting these angles into (15) and combining (14) give

$$\begin{cases} u_{wa1}=-\dfrac{U_{dc}}{3} \\ u_{wa2}=\dfrac{\sqrt{3}}{2}U_{\mathrm{m}}-\dfrac{U_{dc}}{3} \\ u_{wa3}=\dfrac{\sqrt{3}}{2}U_{\mathrm{m}}-\dfrac{2U_{dc}}{3} \\ u_{wa4}=U_{\mathrm{m}}-\dfrac{2U_{dc}}{3} \end{cases} \tag{16}$$

$$\left|u_{wa\_\max}\right|=\max\left\{\left|u_{wa1}\right|,\left|u_{wa2}\right|,\left|u_{wa3}\right|,\left|u_{wa4}\right|\right\} \tag{17}$$

Given a certain grid PCC, U_m is a constant. Divided by U_m and taken absolute value, (16) turns to

$$\begin{cases} \left|\eta u_{wa1}\right|=\left|\dfrac{u_{wa1}}{U_{\mathrm{m}}}\right|=\left|-\dfrac{1}{3}\dfrac{U_{dc}}{U_{\mathrm{m}}}\right| \\ \left|\eta u_{wa2}\right|=\left|\dfrac{u_{wa2}}{U_{\mathrm{m}}}\right|=\left|\dfrac{\sqrt{3}}{2}-\dfrac{1}{3}\dfrac{U_{dc}}{U_{\mathrm{m}}}\right| \\ \left|\eta u_{wa3}\right|=\left|\dfrac{u_{wa3}}{U_{\mathrm{m}}}\right|=\left|\dfrac{\sqrt{3}}{2}-\dfrac{2}{3}\dfrac{U_{dc}}{U_{\mathrm{m}}}\right| \\ \left|\eta u_{wa4}\right|=\left|\dfrac{u_{wa4}}{U_{\mathrm{m}}}\right|=\left|1-\dfrac{2}{3}\dfrac{U_{dc}}{U_{\mathrm{m}}}\right| \end{cases} \tag{18}$$

where $\left|\eta u_{wa1}\right|$ denotes the absolute value of u_{wa1} to U_m ratio. Thus, the maximum of (18) is expressed by

$$\left|\eta u_{wa\_\max}\right|=\max\left\{\left|\eta u_{wa1}\right|,\left|\eta u_{wa2}\right|,\left|\eta u_{wa3}\right|,\left|\eta u_{wa4}\right|\right\} \tag{19}$$

Four curves of (18) are plotted in Fig.3, which shows that the curve *abcd* is the $\left|\eta u_{wa\_\max}\right|$. Hence, $\left|\eta u_{wa\_\max}\right|$ reaches minimum at point c, where $\left|\eta u_{wa1}\right|=\left|\eta u_{wa2}\right|$. Therefore, based on (16), the

minimum of $|u_{wa\_max}|$ can be calculated as

$$\left|u_{wa\_\max}\right|_{\min} = \frac{\sqrt{3}}{4}U_{\mathrm{m}} \tag{20}$$

when

$$U_{dc} = \frac{3\sqrt{3}}{4}U_{\mathrm{m}} \tag{21}$$

Hence, without considering the redundancy, the minimum value of N is given by

$$N = \frac{\left|u_{wa\_\max}\right|_{\min}}{U_c} = \frac{\sqrt{3}}{4}\frac{U_{\mathrm{m}}}{U_c} \tag{22}$$

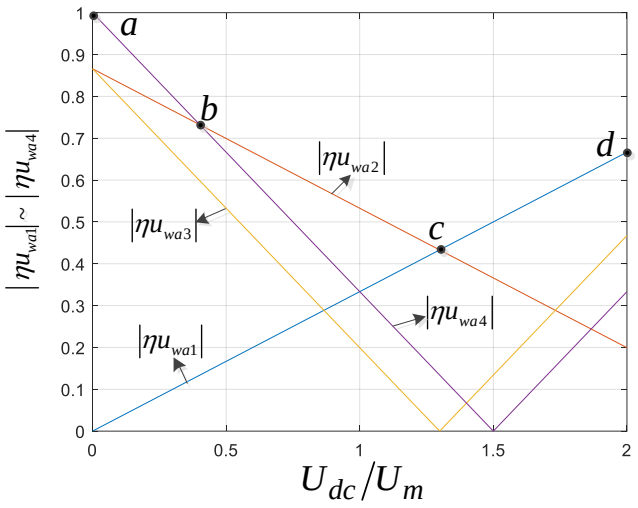


Fig.3 Dependence of $|\eta u_{wa1}|$, $|\eta u_{wa2}|$, $|\eta u_{wa3}|$ and $|\eta u_{wa4}|$ to U_{dc}/U_m

2.4 Analysis of power sharing in WSC and two-level converter

Calculating the Fourier Series of u_{aN} as

$$u_{aN} = \frac{2U_{dc}}{3n\pi}\sum_{n=1}^{\infty}\left[\cos\frac{n\pi}{3} - \cos\frac{2n\pi}{3} + 1 - (-1)^n\right]\sin(n\omega t) \tag{23}$$

Thus, the wave-shaping circuit can be expressed as

$$u_{wa} = U_m\sin(\omega t) - \frac{2U_{dc}}{3n\pi}\sum_{n=1}^{\infty}\left[\cos\frac{n\pi}{3} - \cos\frac{2n\pi}{3} + 1 - (-1)^n\right]\sin(n\omega t) \tag{24}$$

Since harmonic components contribute nothing to the reactive power, only the fundamental frequency component is considered.

$$u_{aN}^1 = \frac{2U_{dc}}{\pi}\sin(\omega t) = \frac{3\sqrt{3}U_m}{2\pi}\sin(\omega t) = 0.827U_m\sin(\omega t) \tag{25}$$

$$u_{wa}^{1} = (1 - \frac{3\sqrt{3}}{2\pi})U_m \sin(\omega t) = 0.173U_m \sin(\omega t) \quad (26)$$

Hence, 82.7% reactive power is handled by the two-level converter, while 17.3% is handled by the wave-shaping circuit.

3. CONTROL SCHEME

To achieve stable operation, the coordination and synchronization between the two-level converter and the wave-shaping circuit are required. Fig.4 shows the overall control scheme of the proposed STATCOM, which is based on decoupling control shown in [22], which contains two parts, i.e., control of the two-level converter and control of the wave-shaping circuit.

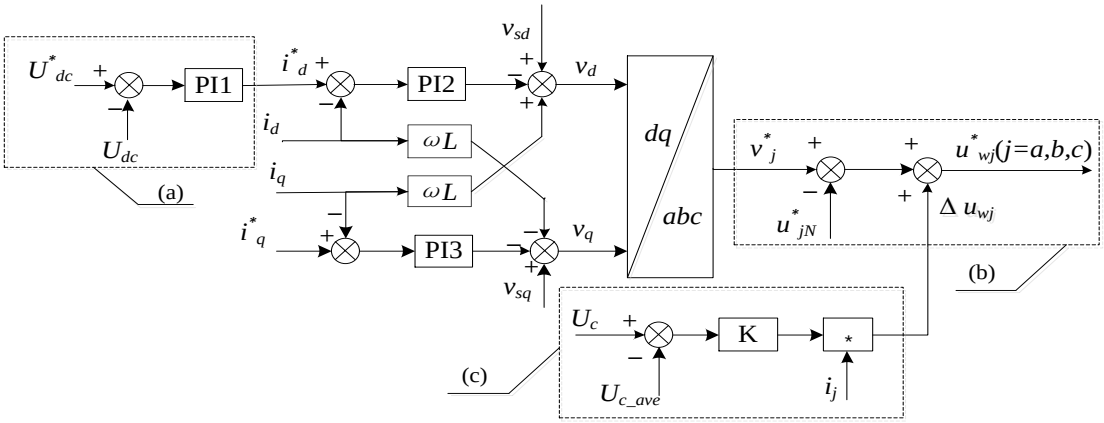


Fig.4. Block diagram of the proposed STATCOM control system

3.1 Control of the Two-Level Converter

To achieve low switching frequency and low loss, square-wave modulation is adopted, which makes the two-level converter switch at fundamental frequency (50 Hz). The switch states of the two-level converter are closely related to the three-phase reference output voltages v^*_j (j= a, b, c), which are obtained by decoupling control illustrated in Fig.4. As shown in Fig.5, U_{S1} and U_{S4} are the switching functions of the switches S_1 and S_4 respectively. When the reference output voltage v^*_a>0, the switch S_1 turns on, while the switch S_4 turns off. When the reference output voltage v^*_a<0, the switch S_1 turns off, while the switch S_4 turns on. The switches in phase b and c are similar according to v^*_b and v^*_c respectively.

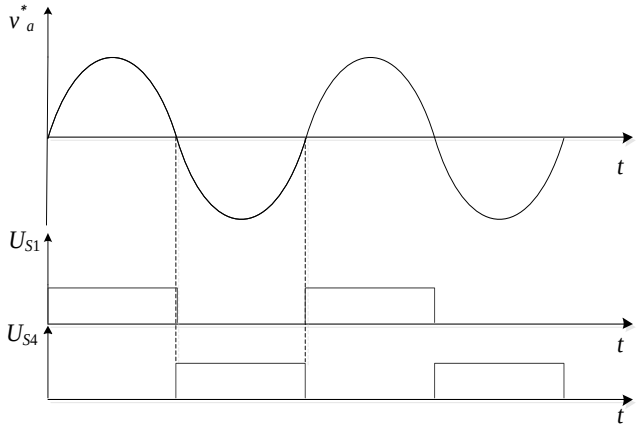


Fig.5. Conduction interval of the switch

To maintain the DC capacitor voltages stable, a slight phase difference between the system voltage and the STATCOM output voltage is needed to supply a small amount of active power to the STATCOM to compensate the devices losses. The PI regulator is adopted to regulate the DC capacitor voltage of the two-level converter, as shown in Fig.4(a).

3.2 Control of the Wave-Shaping Circuit

According to (3), the output voltages u_{wj} (j= a, b, c) of the wave-shaping circuit can be obtained as follows:

$$u_{wj}(t) = v_j(t) - u_{jN}(t) \tag{27}$$

According to (27), the reference output voltages u^*_{wj} (j= a, b, c) are determined by the reference output voltages v^*_j (j= a, b, c) and the reference phase voltages u^*_{jN} (j= a, b, c) of the two-level converter. When the switch signals of the two-level converter are obtained, the output line voltages of the two-level converter are determined by the converter itself, while the phase voltages of the two-level converter can be influenced by the output voltages of the wave-shaping circuit. Therefore, u^*_{jN} (j= a, b, c) are obtained from the output line voltages:

$$u^*_{aN} - u^*_{bN} = u_{ab} \tag{28}$$

$$u^*_{bN} - u^*_{cN} = u_{bc} \tag{29}$$

$$u^*_{aN} + u^*_{bN} + u^*_{cN} = 0 \tag{30}$$

where u_{ab}, u_{bc} are the line voltages at the AC terminal of the two-level converter. According to (28) to (30), u^*_{jN} (j= a, b, c) can be obtained as follows:

$$u_{aN}^{*} = \frac{2u_{ab} + u_{bc}}{3} \tag{31}$$

$$u_{bN}^{*} = \frac{u_{bc} - u_{ab}}{3} \tag{32}$$

$$u_{cN}^{*} = \frac{-u_{ab} - 2u_{bc}}{3} \tag{33}$$

As shown in Fig.4(b), the reference output voltages u^{*}_{wj} (j= a, b, c) of the wave-shaping circuit can be calculated by

$$u_{wj}^{*} = v_{j}^{*} - u_{jN}^{*} + \Delta u_{wj} \tag{34}$$

As shown in Fig.4(c), Δu_{wj} (j= a, b, c) is expressed by

$$\Delta u_{wj} = k_p i_j (U_c - U_{c\_ave}) \tag{35}$$

where U_{c_ave} is the average voltage of DC capacitors of the three-phase H-bridge sub-modules, U_{c_ave} can be expressed by

$$U_{c\_ave} = \frac{1}{3N}(\sum_{j=1}^{N} U_{cj(a)} + \sum_{j=1}^{N} U_{cj(b)} + \sum_{j=1}^{N} U_{cj(c)}) \tag{36}$$

In (35), Δu_{wj} (j= a, b, c) is used to regulate the DC capacitor voltages of the cascaded H-bridge sub-modules. The instantaneous power flowing through the wave-shaping circuit can be given by

$$\Delta P_j = \Delta u_{wj} * i_j = k_p i_j^{2} (U_c - U_{c\_ave}) \tag{37}$$

When $U_c > U_{c\_ave}$, the real power ΔP_j ($\Delta P_j > 0$) is required to inject into the wave-shaping circuit to increase the DC capacitor voltages to the rating U_c; When $U_c < U_{c\_ave}$, the wave-shaping circuit should deliver real power $-\Delta P_j$ ($\Delta P_j < 0$) to the system and the DC capacitor voltages will reduce to the rating U_c. Thus, the DC capacitor voltages of the wave-shaping circuit can be maintained by the controllers in Fig.4(b) and Fig.4(c).

Additionally, due to many sub-modules in high-voltage applications, the nearest level modulation (NLM) [23] is adopted for the simplicity of the whole control system, shown as Fig. 6, where RSF voltage balancing algorithm is illustrated in [24].

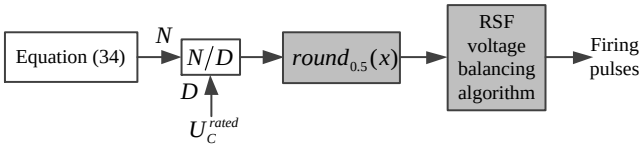


Fig.6. NLM method for wave-shaping circuit

4. SIZING OF THE DC CAPACITORS

DC capacitors comprise a large part of the total system cost and physical size of a STATCOM. Hence, optimal sizing of the DC capacitors is essential to reduce system cost, small physical size and high performance of the proposed STATCOM. In this section the DC voltage ripple equations and the criterion for sizing the DC capacitors of the two-level converter and the wave-shaping circuit are established respectively.

4.1 Sizing of DC Capacitor in the Two-Level Converter

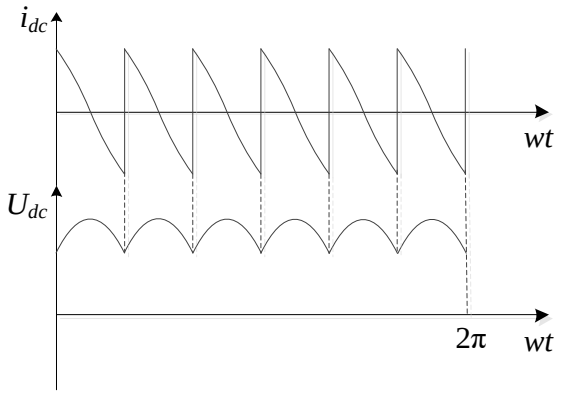


Fig.7. The DC voltage and current of the two-level converter

A relationship can be established between the DC current i_{dc}, the switching function S_{jp} (j= a, b, c) of the upper arms of the two-level converter, and the AC-side current i_j (j= a, b, c).

$$i_{dc} = \sum_{j=(a,b,c)} S_{jp} i_j \tag{38}$$

where

$$S_{jp} == \begin{cases} 1 & v_j(t) \geq 0 \\ 0 & v_j(t) < 0 \end{cases} \tag{39}$$

According to (38) and (39), the waveform of i_{dc} is illustrated in Fig.7. The cycle of the DC current i_{dc} is π/3. Thus, i_{dc} can be described as follows in the first cycle

$$i_{dc} = I_m \cos(\omega t + \pi/3) \qquad \omega t \in [0, \pi/3] \tag{40}$$

The behavior of the DC capacitor of the two-level converter is described as

$$C_d \frac{dU_{dc}}{dt} = i_{dc} \tag{41}$$

According to (40) and (41), it is clear that the DC output voltage U_{dc} includes a 6th order harmonic component, as shown in Fig.7. It can be derived as follows in the first cycle

$$U_{dc} = C_1 + \frac{I_m}{\omega C_d}\sin(\omega t + \pi/3) \qquad \omega t \in [0, \pi/3] \tag{42}$$

where C_1 is a constant. By solving (42), the DC capacitor peak–peak voltage ripple is obtained as

$$\Delta U_{dc} = (1 - \frac{\sqrt{3}}{2})\frac{I_m}{\omega C_d} \tag{43}$$

Once this ripple is specified, the size of the DC capacitor of the two-level converter can be calculated by

$$C_d = (1 - \frac{\sqrt{3}}{2})\frac{I_m}{\omega \Delta U_{dc}} \tag{44}$$

4.2 Sizing of DC Capacitors in the Wave-Shaping Circuit

The behavior of the DC capacitor in the H-bridge sub-module is expressed by

$$C_h \frac{du_c}{dt} = sw_a \cdot i_a \tag{45}$$

where, C_h denotes the capacitance, u_c denotes the capacitor voltage, sw_a denotes the switching function. According to (7), (21) and (22), the switching function can be expressed by

$$sw_a(t) = \frac{u_{wa}(t)}{NU_c} = \frac{4}{\sqrt{3}}\sin\omega t - 3M_a \tag{46}$$

Thus, (45) results in

$$\begin{aligned} C_h \frac{du_c}{dt} &= (\frac{4}{\sqrt{3}}\sin\omega t - 3M_a) \cdot I_m \cos\omega t \\ &= \frac{2}{\sqrt{3}} I_m \sin 2\omega t - 3M_a I_m \cos\omega t \end{aligned} \tag{47}$$

The voltage u_{wa} produced by the wave-shaping circuit is symmetrical, so only the first half cycle is taken into account. Hence, M_a can be expressed by

$$M_a = \begin{cases} 1/3 & \omega t \in [0, \pi/3] \\ 2/3 & \omega t \in [\pi/3, 2\pi/3] \\ 1/3 & \omega t \in [2\pi/3, \pi] \end{cases} \tag{48}$$

According to (47) and (48), the following results are obtained.

$$u_c(t)=\begin{cases}-\dfrac{I_m}{\sqrt{3}\omega C_h}\cos 2\omega t-\dfrac{I_m}{\omega C_h}\sin\omega t+C_2 & \omega t\in[0,\pi/3]\\ -\dfrac{I_m}{\sqrt{3}\omega C_h}\cos 2\omega t-\dfrac{2I_m}{\omega C_h}\sin\omega t+C_2+\dfrac{\sqrt{3}I_m}{2\omega C_h} & \omega t\in[\pi/3,2\pi/3]\\ -\dfrac{I_m}{\sqrt{3}\omega C_h}\cos 2\omega t-\dfrac{I_m}{\omega C_h}\sin\omega t+C_2 & \omega t\in[2\pi/3,\pi]\end{cases} \quad (49)$$

where C_2 is a constant. According to (49), the DC capacitor peak–peak voltage ripple of the H-bridge can be calculated by

$$\Delta u_c=(\frac{31\sqrt{3}}{24}-2)\frac{I_m}{\omega C_h} \quad (50)$$

Once this ripple is specified, the size of the DC capacitor of the H-bridge can be calculated by

$$C_h=(\frac{31\sqrt{3}}{24}-2)\frac{I_m}{\omega\Delta u_c} \quad (51)$$

5. COMPARISON OF THE PROPOSED STATCOM AND THE CASCADED H-BRIDGE STATCOM

The proposed STATCOM combines the features and advantages of both the cascaded H-bridge and two-level converters. To analyze the features of the proposed STATCOM, the number of IGBTs and H-bridge sub-modules, the number, size and stored energy of the DC capacitors, the DC-capacitor RMS current and power losses of the two STATCOMs are compared at the same voltage level and reactive power in this section. The capacitor is sized for a specified voltage ripple, typically 10% of the rated voltage. The rated voltage U_c (0.9 kV) of the H-bridge capacitors is also the rated voltage of IGBTs in the H-bridge sub-modules and the two-level converter.

5.1 Numbers of H-bridge Sub-Modules and IGBTs

Without redundant configuration, the number of the H-bridge sub-modules per phase of the cascaded H-bridge (CHB) STATCOM N_{CHB_STAT} can be expressed by

$$N_{CHB\_STAT}=\frac{U_{\mathrm{m}}}{U_c} \quad (52)$$

Thus, numbers of IGBTs and diodes in each phase of the CHB STATCOM both are $4U_m/U_c$, and the number of DC capacitors is U_m/U_c.

According to (22) and (52), the ratio of the H-bridge sub-module number of the proposed STATCOM to that of the CHB STATCOM is derived as

$$k_H = \frac{N}{N_{CHB\_STAT}} = \frac{\sqrt{3}}{4} = 0.433 \tag{53}$$

The number of the IGBTs or diodes per phase in the proposed STATCOM N_{HCMC_STAT} is

$$N_{HCMC\_STAT} = 4N + 2\frac{U_{dc}}{U_c} = 2.5\sqrt{3}\frac{U_{\mathrm{m}}}{U_c} \tag{54}$$

Thus, the ratio of the number of IGBTs or diodes of the proposed STATCOM to the CHB STATCOM is derived as

$$k_N = \frac{2.5\sqrt{3}}{4} = 1.08 \tag{55}$$

According to (53) and (55), it can be seen that the number of H-bridge sub-modules of the proposed STATCOM is only 0.433 times that of the CHB STATCOM, while the number of the IGBTs or diodes reaches 1.08 times.

5.2 the Number, Size and Stored Energy of total Capacitors

As analyzed before, the number of DC capacitors per phase of the CHB STATCOM is U_m/U_c, while there are only $0.433U_m/U_c$ DC capacitors in the wave-shaping circuit and one DC capacitor in the two-level converter of the proposed STATCOM.

The stored energy of the DC capacitors of the proposed STATCOM can be calculated by

$$W_{HCMC\_STAT} = W_1 + W_2 = \frac{3}{2}NC_hU_c^2 + \frac{1}{2}C_dU_{dc}^2 \tag{56}$$

where W_{HCMC_STAT}, W_1 and W_2 denote the energy stored in the whole STATCOM, WSC and two-level converter, respectively.

Assume $\Delta u_c = 0.1U_c$ and $\Delta U_{dc} = 0.1U_{dc}$, substituting (21), (22), (44) and (51) into (56) gives

$$W_{HCMC\_STAT} = (1.54 + 0.87)\frac{U_{\mathrm{m}}I_m}{\omega} = 2.41\frac{U_{\mathrm{m}}I_m}{\omega} \tag{57}$$

The size of the DC capacitors of the CHB STATCOM C_{h_CHB} is derived in [13], which can be calculated by

$$C_{h\_CHB} = \frac{I_m}{2\omega\Delta u_c} \tag{58}$$

According to (52) and (58), the stored energy of the DC capacitors in the CHB STATCOM can be expressed by

$$W_{CHB\_STAT} = \frac{3}{2}N_{CHB\_STAT}C_{h\_CHB}U_c^2 = 7.5\frac{U_{\mathrm{m}}I_m}{\omega} \tag{59}$$

According to (51) and (58), the ratio of the H-bridge sub-modules DC capacitor size of the proposed STATCOM to the CHB STATCOM is derived as

$$k_c = \frac{C_h}{C_{h\_CHB}} = 2(\frac{31\sqrt{3}}{24} - 2) = 0.474 \tag{60}$$

According to (57) and (59), the ratio of the DC capacitors stored energy of the proposed STATCOM to the cascaded H-bridge STATCOM is derived as

$$k_{sn} = \frac{W_{HCMC\_STAT}}{W_{CHB\_STAT}} = \frac{2.41}{7.5} = 0.321 \tag{61}$$

5.3 DC-Capacitor RMS Current

According to (40), the RMS current of the DC capacitor in the two-level converter can be obtained by

$$I_{dc} = \sqrt{\frac{6}{T}\int_0^{\frac{T}{6}} i_{dc}^2 dt} = I_m\sqrt{\frac{1}{2} - \frac{3\sqrt{3}}{4\pi}} = 0.294I_m \tag{62}$$

According to (47), the current through the DC capacitors of the H-bridge sub-modules can be derived as

$$i_h = \frac{2}{\sqrt{3}} I_m \sin 2\omega t - 3M_a I_m \cos \omega t \tag{63}$$

Thus, the RMS current of the DC capacitors of the H-bridge sub-modules can be derived as

$$I_h = \sqrt{\frac{1}{T}\int_0^T i_h^2 dt} = I_m\sqrt{\frac{5}{3} - \frac{11\sqrt{3}}{4\pi}} = 0.390I_m \tag{64}$$

The current through the DC capacitors of the cascaded H-bridge STATCOM, derived in paper [13], can be calculated by

$$i_{h\_CHB} = \frac{1}{2} I_m \sin 2\omega t \tag{65}$$

Hence, the RMS current of the DC capacitors of the CHB STATCOM can be calculated by

$$I_{h\_CHB} = \frac{1}{2\sqrt{2}} I_m = 0.354I_m \tag{66}$$

The ratio of the DC-capacitor RMS current of the H-bridge sub-modules of the proposed STATCOM to the cascaded H-bridge STATCOM is derived as

$$k_I = \frac{I_h}{I_{h\_CHB}} = 2\sqrt{2}\sqrt{\frac{5}{3} - \frac{11\sqrt{3}}{4\pi}} = 1.10 \tag{67}$$

5.4 Power losses

The CHB STATCOM and the HCMC STATCOM will be analyzed comprehensively in terms of power losses including conduction loss and switching loss. Because it is very complex to analytically calculate the switching frequency of nearest level modulation (NLM), loss simulations of Infineon IGBT module (FF600R17ME4) are performed to compare the two topologies. According to the datasheet of FF600R17ME4, the conduction voltage and switching loss curves can be represented by linear function and quadratic function, respectively.

$$V_{t(d)} = V_{t(d)0} + R_{t(d)} i \tag{68}$$

$$E_{sw} = ai^2 + bi + c \tag{69}$$

where $V_{t(d)}$ denotes conduction voltage of IGBT and diode, respectively; $V_{t(d)0}$, and $R_{t(d)}$ represent corresponding coefficients; E_{sw} denotes the switching loss; a, b and c denote corresponding coefficients; i denotes current flowing through the component.

Therefore, the conduction losses can be expressed by

$$E_{con} = V_{t(d)0} |i| + R_{t(d)} i^2 \tag{70}$$

Under the junction temperature 125 °C condition, the coefficients of (69) and (70) are shown as the following tables based on the datasheet.

Table I Coefficients of switching loss calculation

	a	*b*	c
IGBT switch on	0.0006	-0.0902	66.744
IGBT switch off	-0.00007	0.3304	7.18
Diode recovery	-0.00006	0.1488	72.25

Table II Coefficients of conduction loss calculation

	$V_{t(d)0}$ / V	$R_{t(d)}$ / ohm
IGBT	1.15	0.002
Diode	1.06	0.0014

CHB and HCMC loss simulations are performed under the same operating conditions, i.e. connected to 35kV AC grid, generating 50Mvar reactive power, NLM method employed, rated voltage of H-bridge 0.9kV. Thus, it can be calculated that the HCMC consists of 15 H-bridges and 90 IGBTs, while the CHB consists 36 H-bridges in each phase. The simulation results are shown in Table III,

which can be seen that the total loss of CHB is a little larger than that of HCMC.

Table III Loss comparison between CHB and HCMC

	Switching Loss	Conduction Loss	Total Loss
CHB	55.65 kW	428.39 kW	484.04 kW
HCMC	11.94 kW	453.21 kW	465.15 kW

The overall comparison is illustrated in Table IV, where it can be concluded that compared to the CHB STATCOM, the proposed STATCOM in this paper has much less number, smaller size and less energy stored in DC capacitors, while a slightly more numbers of IGBTs and a little larger capacitor current RMS.

Table IV Comparison between the HCMC STATCOM and the CHB STATCOM

	CHB STATCOM	HCMC STATCOM
Numbers of H-bridge SMs (capacitors)	1	0.433
Numbers of IGBTs and diodes	1	1.08
Size of capacitors in SMs	1	0.474
Energy stored in capacitors	1	0.321
Capacitor currents RMS	1	1.10

6. SIMULATION RESULTS

To verify the proposed topology and control strategy, a simulation of a ±50Mvar STATCOM connected to a 35kV grid is carried out on the time-domain simulation tool PSCAD/EMTDC. The number of H-bridge sub-modules per phase is set to be 15 while the rated voltage of each H-bridge sub-module is 900V. The main circuit parameters and controller parameters are listed in Table V and Table VI, respectively.

Table V Circuit parameters for simulation

Items	Symbols	Values
AC system line-line voltage	V_s	35kV
Rated reactive power	Q	±50Mvar
Rated frequency	f	50Hz
AC inductor	L	4.8mH
Two-level DC link voltage	U_{dc}	±39.4kV
Two-level DC capacitor peak-peak ripple	ΔU_{dc}	3.94kV

Two-level DC link capacitance	C_d	126μF
H-bridge DC link voltage	U_c	900V
H-bridge DC capacitor peak-peak ripple	Δu_c	90V
H-bridge DC link capacitance	C_h	9783μF
Sub-module number of per WSC	N	15

Table VI Control parameters for simulation

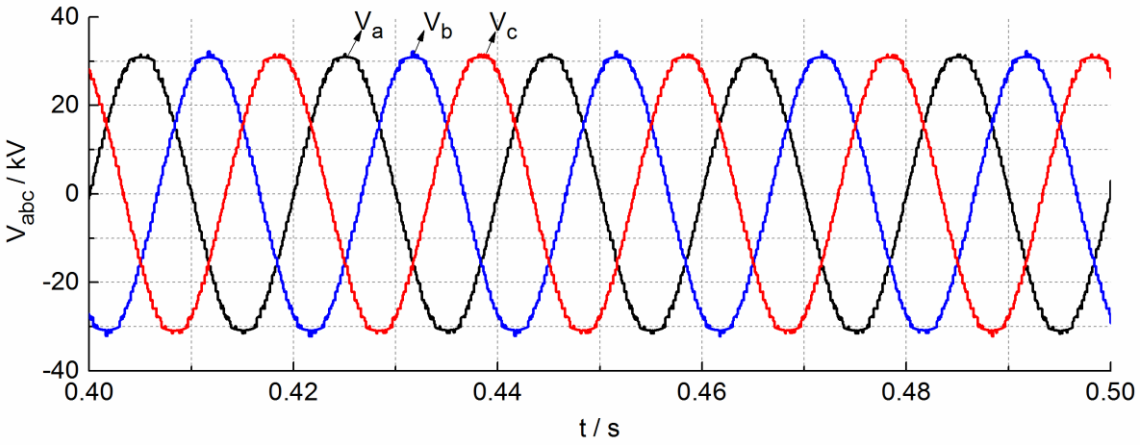
	Kp	Ki
PI1	0.1	100
PI2	4	0.01
PI3	4	0.01
K	20	/

6.1 Performance of Steady-State Operation

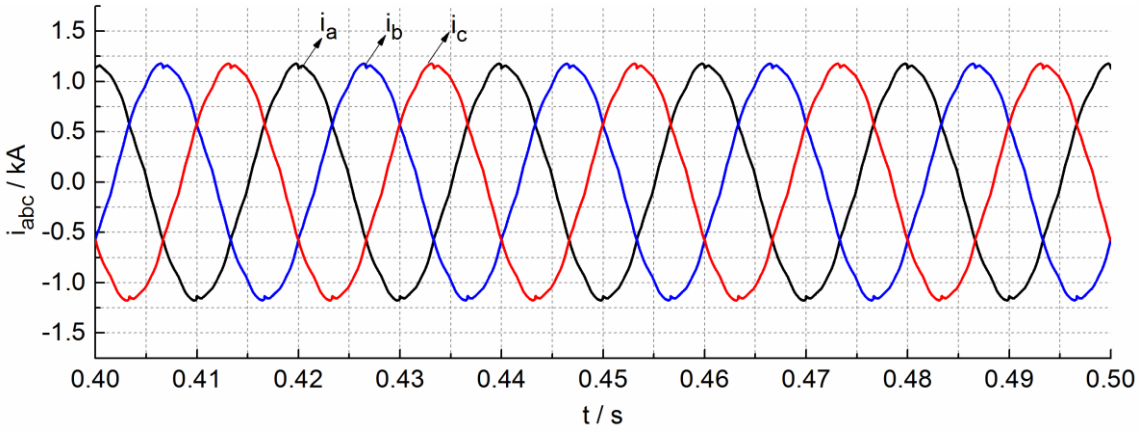
Fig.8 shows the steady operation characteristics: the three-phase AC output voltages of the STATCOM [Fig.8(a)], the three-phase AC system currents [Fig.8(b)], multilevel voltage generated by the wave-shaping circuit in phase *a* [Fig.8(c)] and phase voltage generated by the two-level converter in phase *a* [Fig.8(d)]. In the steady state, the STATCOM supplies 50 Mvar reactive power to the system. The fast Fourier transform (FFT) analysis results demonstrate that the system has good voltage quality and current quality, with low total harmonic distortion (THD) (i.e., 1% for AC voltages and 1.89% for AC currents.

Fig.9 shows the voltage ripple of the DC capacitors of the proposed STATCOM. It can be seen from Fig.9(a) that the voltage of DC capacitor in the two-level converter has 6^{th} harmonic order component and the peak–peak voltage ripple is almost close to the theoretical value 3.94 kV. Fig.9(b) illustrates the peak–peak voltage ripple of DC capacitors of the H-bridge sub-modules, which is about 90 V. Fig.9(a) and Fig.9(b) prove the correctness of the calculation method of sizing of DC capacitors.

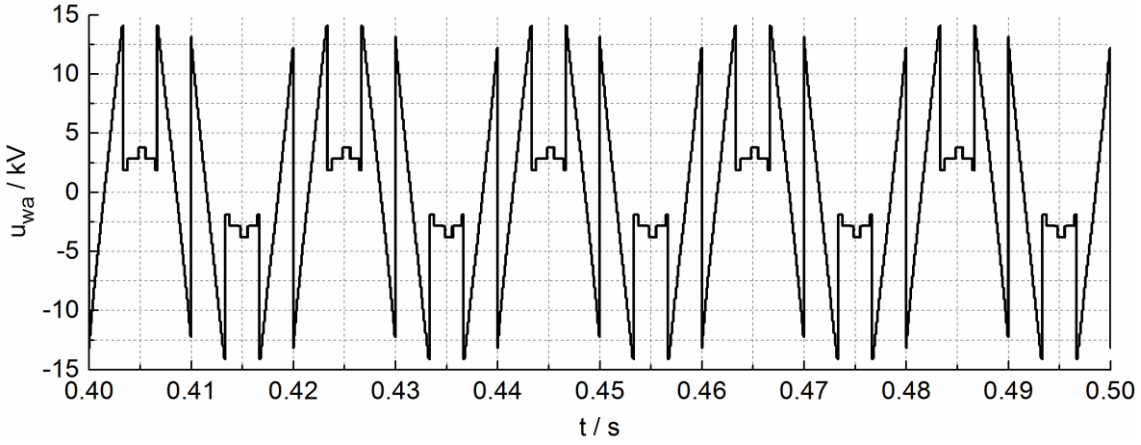
Fig.10 illustrates the trigger pulses of the IGBTs in both the WSC and the two-level converter. The switching frequency of the IGBTs in the WSC is more or less 300Hz (see Fig.10(a)), while the switching frequency of the IGBTs in the two-level converter is 50Hz (see Fig.10(b)) as analyzed before.



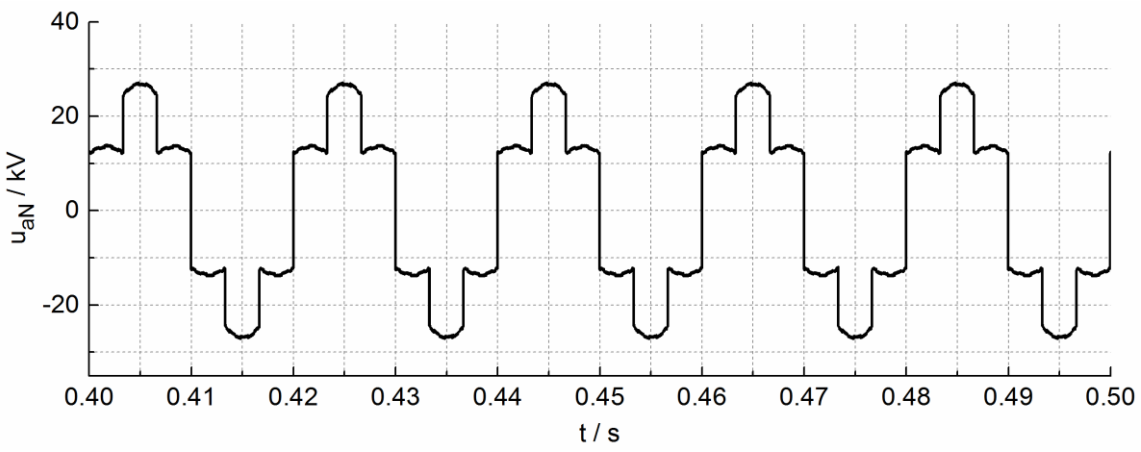
(a) Three-phase output voltage waveforms of the STATCOM



(b) Three-phase system current waveforms

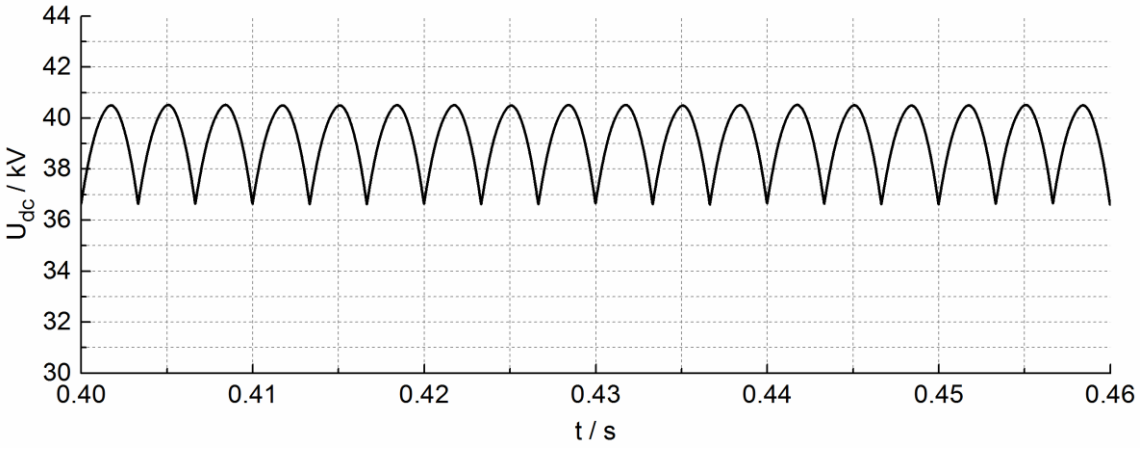


(c) Multilevel voltage waveform generated by the wave-shaping circuit in phase *a*

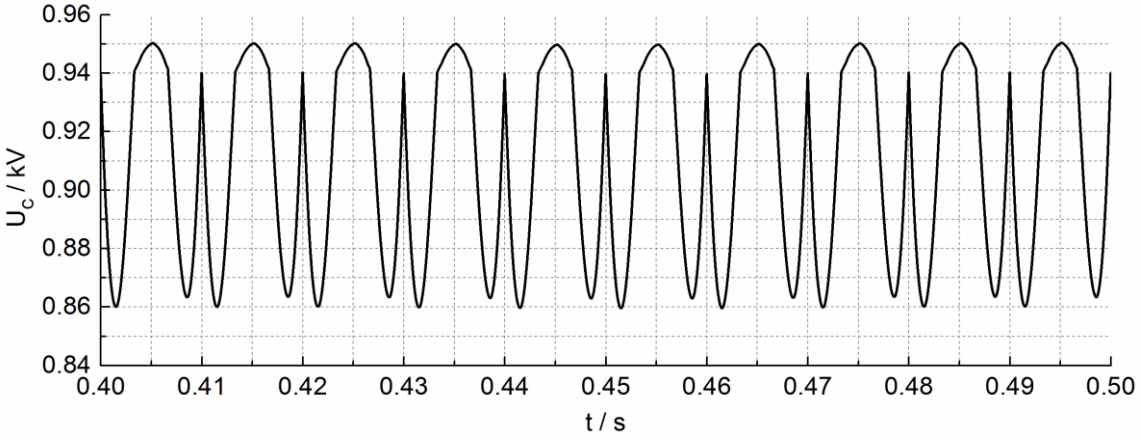


(d) Voltage waveform generated by the two-level converter in phase *a*

Fig.8. Steady-state operation performance of the STATCOM.

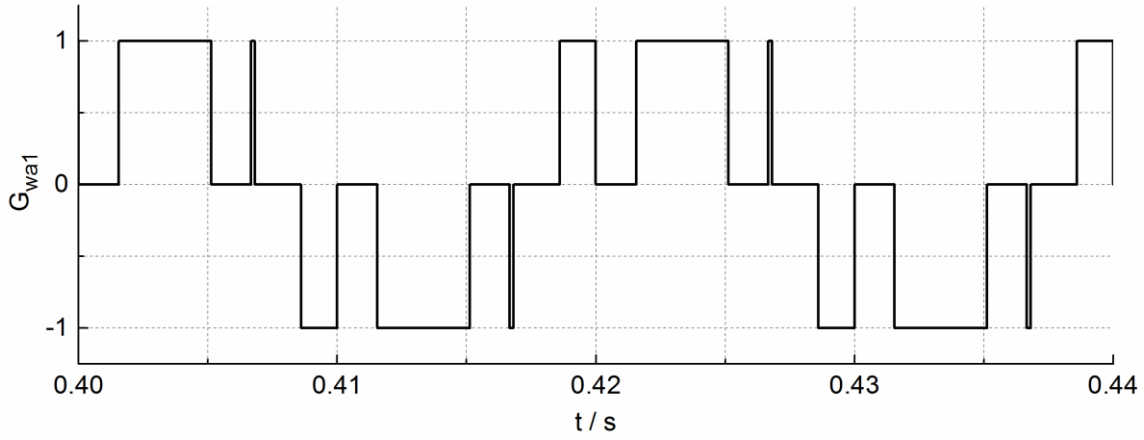


(a) Voltage variation of DC capacitor in the two-level converter

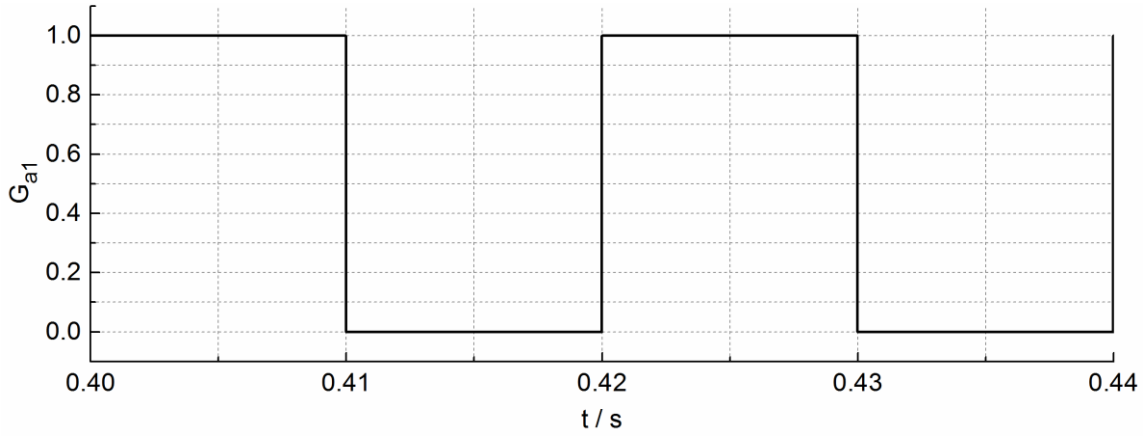


(b) Voltage variation of DC capacitors of the H-bridge sub-modules

Fig.9. Waveforms demonstrating the variation of DC capacitors voltage.



(a) The trigger pulse of the phase-*a* #1 SM of the WSC

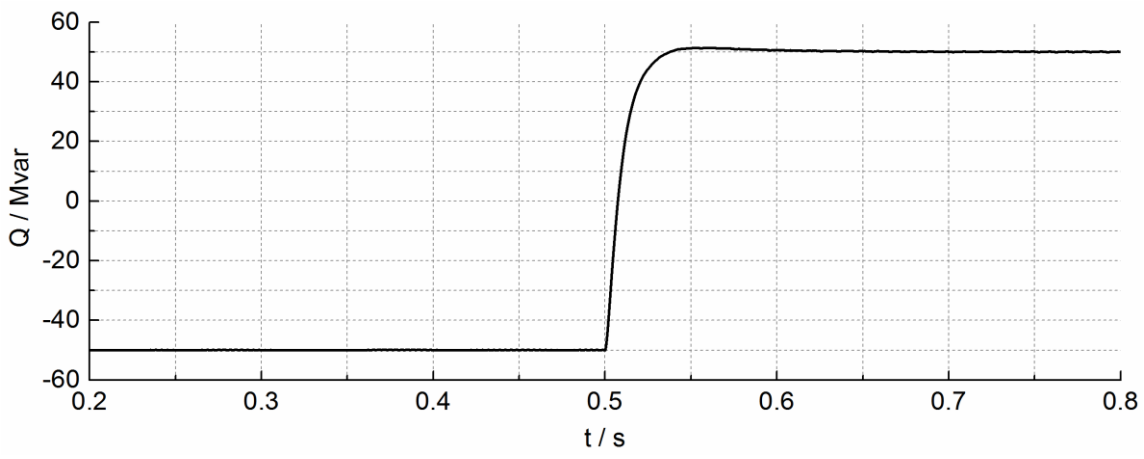


(b) The trigger pulse of the phase-*a* of the 2-level converter

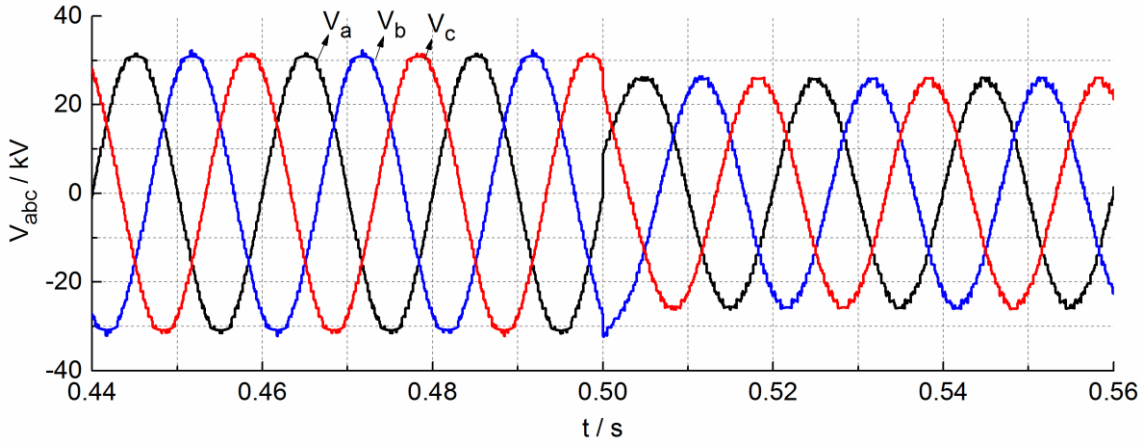
Fig.10. Tigger pulses of the WSC and 2-level converter

6.2 Dynamic Response to Reactive Power Demand

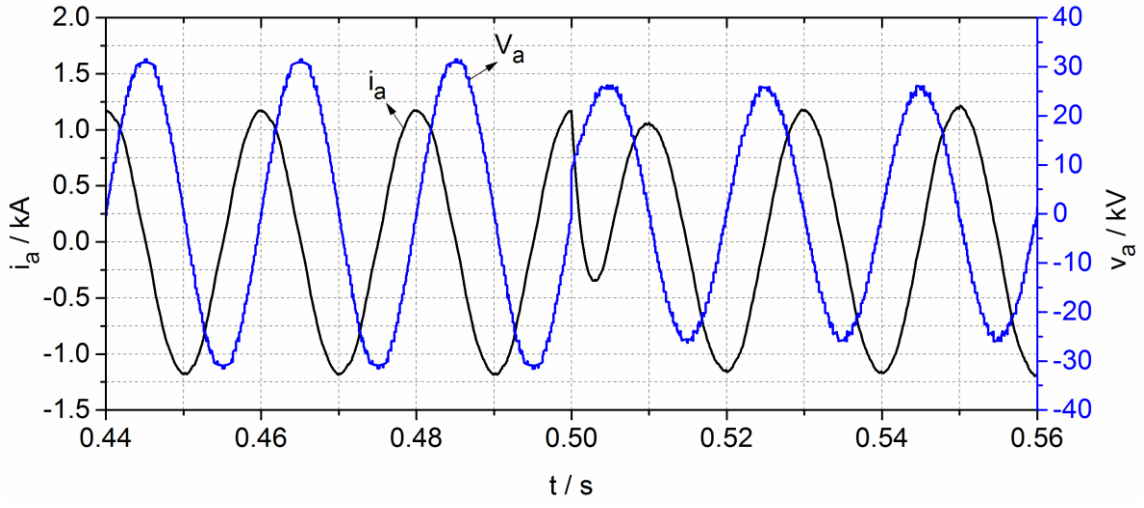
Fig.11 illustrates the dynamic behavior during changes of the reactive power command. The reactive power reference steps from 50 Mvar to -50 Mvar at 0.5 s. It is observed from this figure that the actual reactive power can track the command reference very well (see Fig.11(a)]. This simulation result demonstrates the extremely fast dynamic response of the proposed STATCOM. Fig.11(b) shows the output voltage of STATCOM in phase *a*. It can be seen that the magnitude of the output voltage becomes smaller after 0.5 s for the reactive power change. As depicted in Fig.11(c), the system current leads the system voltage by 90°before 0.5 s and the system current lags the system voltage by 90°after 0.5 s. Fig.11(d) illustrates the decrease of voltage generated by the wave-shaping circuit in phase *a* due to the decrease of the output voltage.



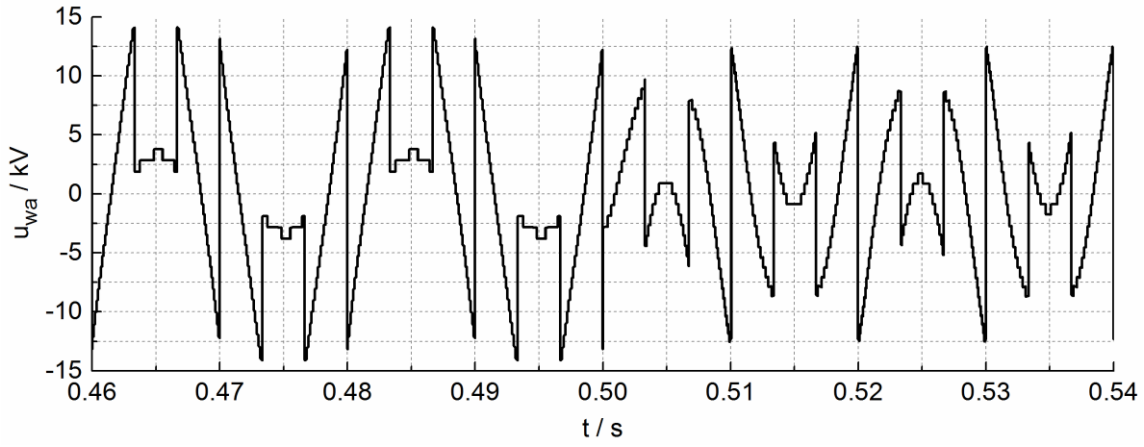
(a) Reactive power



(b) Response of the output voltage of STATCOM in phase *a*



(c) Response of system current in phase *a*



(d) Response of voltage generated by the wave-shaping circuit in phase *a*

Fig.11. Transient response of the system for reactive power reversal.

7. CONCLUSION

A new type of STATCOM based on hybrid cascaded multilevel converter has been proposed in this paper. The main circuit of this STATCOM is composed of several identical H-bridge sub-modules which are placed on the AC side of the two-level converter. This topology of STATCOM combines the features and advantages of both the cascaded H-bridge and two-level converters. It reduces switching loss and simplifies dynamic voltage sharing along the series string of IGBTs in the two-level converter. And compared with the cascaded H-bridge STATCOM, fewer H-bridge sub-modules are needed, reducing the required number and rating of DC capacitors.

To achieve the coordination and synchronization between the two-level converter and the wave-shaping circuit, a control scheme is proposed. The DC capacitor voltage ripple is theoretically analyzed and the criterion for sizing of DC capacitors is established. Comparison of numbers of IGBTs and H-bridge sub-modules, the number, size and stored energy of the DC capacitors and the DC-capacitor RMS current between the proposed STATCOM and the cascaded H-bridge STATCOM is analyzed. Simulations of the proposed STATCOM are carried out in PSCAD/EMTDC, verifying the correctness of the theoretical analysis.

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