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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
[10.1109/TPEL.2018.2858784](https://doi.org/10.1109/TPEL.2018.2858784)

Publication date:
2019

Document Version
Accepted author manuscript, peer reviewed version

[Link to publication from Aalborg University](#)

Citation for published version (APA):
Tang, Z., Su, M., Sun, Y., Cheng, B., Yang, Y., Blaabjerg, F., & Wang, L. (2019). Hybrid UP-PWM Scheme for HERIC Inverter to Improve Power Quality and Efficiency. *I E E E Transactions on Power Electronics*, 34(5), 4292-4303. [8418796]. <https://doi.org/10.1109/TPEL.2018.2858784>

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A Hybrid UP-PWM Scheme for HERIC Inverter to Improve Power Quality and Efficiency

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Abstract—The Highly Efficient and Reliable Inverter Concept (HERIC) inverter is a cost-effective topology, which has low leakage currents and a relatively high efficiency. Thus, it is very suitable for transformerless PV systems. However, with the reported modulation methods, it is difficult to simultaneously maintain the high efficiency, good power quality, and reactive power injection of the HERIC inverter. In this paper, a hybrid unipolar pulse width modulation (UP-PWM) scheme is thus proposed to achieve those performances. The hybrid scheme adopts the conventional UP-PWM in the case of generating the positive power. When generating the negative power, a modulation scheme, which only requires the operation of freewheeling switches, is specifically proposed. Additionally, in the region of the output voltage and current zero-crossing points (ZCP), an UP-PWM with modified dead time is introduced. In order to validate the effectiveness of the proposed scheme, simulations and experiments are performed on a 4-kW HERIC inverter system with a 20-kHz switching frequency. The results demonstrate that the proposed hybrid UP-PWM method achieves a better performance in terms of reactive power injection than the conventional UP-PWM scheme, and a higher efficiency than the UP-PWM with dead time. In addition, the proposed UP-PWM scheme also enables a better power quality.

Index Terms—HERIC inverter, pulse width modulation (PWM), hybrid unipolar PWM (UP-PWM), reactive power capability, efficiency, zero-crossing distortion (ZCD), power quality, photovoltaic (PV) systems

I. INTRODUCTION

PHOTOVOLTAIC (PV) energy is one of the favorite renewables due to its environment-friendly characteristic and also the still declining module price. In order to interconnect PV systems with the utility grid, massive power electronic converters are adopted as the interface. In order to improve the performance of power converters, many attempts

have been made in terms of topologies, modulation schemes, control methods, and so on [1]-[5]. In the case of grid-connected PV systems, problems like efficiency, reliability, power quality, and reactive power controllability are of high concern. In recent years, transformerless inverters have attracted much more attention than their counterparts (i.e., transformer-based systems) due to their high efficiencies, small size, and low costs. However, in order to ensure the safety of equipment and personnel, leakage currents in transformerless grid-connected systems should be suppressed to a certain level [6-7]. Thus, many modified topologies and modulation schemes have been reported in the literature to tackle this issue [8]-[14], e.g., the H5 topology [8], HERIC topology [9], H6 inverter with a hybrid modulation [11], and an efficient transformerless inverter [13].

Among various transformerless topologies, the HERIC is a promising candidate due to the simple structure and high efficiency. Moreover, the HERIC can suppress leakage currents with either the conventional bipolar pulse width modulation (BP-PWM) or UP-PWM scheme [15], [19]. The conventional BP-PWM scheme enables the inverter to provide reactive power upon demand, but the efficiency and power quality are compromised [15]. In contrast, the conventional UP-PWM method achieves lower switching losses and also lower inductor ripple currents, leading to a higher system efficiency and better power quality, but it cannot provide reactive power [16]. However, as defined in international standards (e.g., VDE-AR-N4105), the power factor in power generation systems or units must be adjustable within a range of 0.9 leading to 0.9 lagging [18]. In order to achieve so, various hybrid modulation schemes or novel transformerless topologies have been proposed [17]-[20]. For instance, a new transformerless inverter with a simple modulation method was proposed in [17], where the efficiency has also been increased. However, compared with the HERIC inverter, the hardware cost and complexity are relatively high due to the additional six diodes. In [18], a combination of the UP-PWM and BP-PWM schemes was proposed for the H5 inverter to achieve reactive power capability. Yet, additional switching losses and high current ripples are generated by the BP-PWM, as aforementioned. To tackle this issue, a modulation technique providing a bidirectional path during freewheeling periods was proposed for the H5 and HERIC topologies, to enhance the reactive power controllability [19]. Furthermore, with a simple modification in switching patterns by phase shifting the current reference, the same modulation method has been used for the H6 inverter to enable reactive power injection in [20]. Notably, this method requires large dead time between the switchover of phase-leg switches and AC bypass switches, to prevent

Manuscript received March 28, 2018; revised May 03, 2018; accepted July 12, 2018. This work was supported by the National Natural Science Foundation of China (Grant No. 51677195 and Grant No. 61622311), the Joint Research Fund of Chinese Ministry of Education under Grant 6141A02033514, and the Fundamental Research Funds in the Central South University under Grant 2018zzts530. (Corresponding author: Lina Wang.)

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2018.xxxxxxx

short-circuiting [21]. Although the dead time has negligible impact on power losses, it leads to distortions in the output current of the converter.

Additionally, the zero-crossing distortion (ZCD) degrading the power quality has not been discussed in above schemes. Generally, there are two ZCD cases in the grid-connected application. One is at the output voltage zero-crossing point (ZCP). In this case, the minimum pulse width limitation that ensures the normal operation of power switches will lead to ZCD in the injected currents [22]. To deal with this, a global sliding mode control method was proposed in [22], which can reduce the ZCD to some extent. However, the ZCD, which is actually induced by the restriction of modulation, has not been fully addressed yet in the literature. Another ZCD case is at the grid-connected current ZCP. In general, the polarity detection of the current plays an important role in modulation schemes. However, due to the noise effect, errors usually exist in the polarity detection. Then, the distortions (i.e., ZCD) appear, even the desired voltage cannot be built up. To alleviate the distortions, a bidirectional current path is necessary in the region of the current ZCP. In [23], the phase angle of the inverter output voltage reference (modified in the PWM scheme) was then shifted to reduce the ZCD at the current ZCP. In contrast, the phase angle of the grid-connected current reference was shifted in [17] to address this issue. However, the shifted area of both cannot cover all regions of the unclear polarity.

Nonetheless, any converter for transformerless PV systems has to be evaluated considering not only the high efficiency but also the high power quality and reactive power controllability [24]. However, as discussed in the above, the existing schemes cannot achieve so at the same time. Therefore, this paper proposes a hybrid UP-PWM scheme for the HERIC inverter. The main contribution of this paper can be summarized into two parts. Firstly, the proposed scheme combines three modulation methods, i.e., a conventional UP-PWM, an UP-PWM with the modified dead time, and a modulation that only requires the operation of AC bypass power switches. Therefore, the proposed hybrid UP-PWM method can achieve a better performance in terms of reactive power injection than the conventional UP-PWM. Additionally, it also achieves a higher efficiency than the UP-PWM with dead time. Secondly, with the modified dead time strategy, the proposed UP-PWM scheme can reduce the current ZCD in the region of the grid voltage and current ZCPs, and thus, an improved power quality is ensured.

The rest of this paper is organized as follows. In Section II, typical and common modulation schemes for the HERIC inverter are presented, and their corresponding performances and drawbacks are discussed. Then, the proposed hybrid UP-PWM scheme, which combines three common modulation methods, is introduced in Section III. The precise modification principle of the modulation in the region of the grid voltage and current ZCPs is also introduced in this section, where the switching power losses is then analyzed. Following, the hybrid UP-PWM method is verified on a 4-kW single-phase HERIC inverter by simulations and experiments. Results are shown in Section IV, which validates the effectiveness of the proposed modulation scheme for the HERIC inverter. Finally, Section V provides concluding remarks.

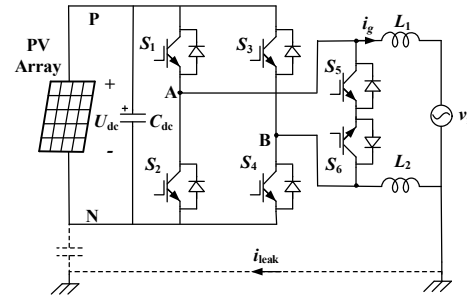


Fig. 1. Hardware schematic of the single-phase single-stage grid-connected HERIC inverter system, where i_{leak} is the leakage current.

II. PRIOR-ART MODULATION SCHEMES

Fig. 1 shows the schematic diagram of the HERIC inverter. According to the Kirchhoff's Voltage Law (KVL), the dynamic equation for the grid current can be obtained as

$$v_L(t) = L \frac{di_g(t)}{dt} = v_{AB}(t) - v_g(t) \quad (1)$$

where $L = L_1 + L_2$ with L_1 and L_2 being the grid filter, $i_g(t)$ is the grid-connected current, $v_g(t)$ is the grid voltage, and $v_{AB}(t)$ is the differential-mode voltage. Since only the modulation method of the single-phase single-stage grid-connected HERIC inverter is discussed, the DC-link voltage U_{dc} is assumed constant. Furthermore, the forward current is defined as the direction of i_g in Fig. 1.

A. Typical Modulation Schemes

Typical modulation schemes for the HERIC inverter including the conventional UP-PWM and UP-PWM with dead time are demonstrated in Fig. 2(a) and (b), respectively, where v_{ref} is the output voltage reference. Fig. 2(a) shows the principle of the conventional UP-PWM, where the AC bypass power devices $S_{5,6}$ are switched at the grid fundamental frequency, and the power switches $S_{1,4}$ operate at a high frequency. The principle of the UP-PWM with dead time is shown in Fig. 2(b), where the power devices $S_{1,4}$ and the AC bypass switches $S_{5,6}$ are operated at a high frequency. The modulation scheme will inevitably increase the total power losses due to the undesired switching states during dead time. In addition, the inserted dead time will also lead to high ripple currents, deteriorating the power quality.

B. Reactive power Controllability

The flexible reactive power control enables a better integration of renewable generation systems into low-voltage networks [18]. In the current grid requirements, the reactive power from PV systems should be flexibly regulated (e.g., for dynamic fault ride-through and also static voltage support).

According to the principle shown in Fig. 2(a), when $v_{ref} \geq 0$, S_6 is ON, and $S_{1,4}$ operate at a high frequency. The forward current flows through S_6 and D_5 to achieve zero voltages. However, there is no path for the reverse current. Similarly, when $v_{ref} < 0$, S_5 is ON, and $S_{2,3}$ operate at a high frequency. The reverse current flows through S_5 and D_6 to generate zero voltages. However, the forward current cannot find a flowing path either. Thus, the conventional UP-PWM does not have reactive power capability [18]. In Fig. 2(b), when $v_{ref} \geq 0$, $S_{5,6}$ and $S_{1,4}$ operate at a high frequency. When $v_{ref} < 0$, $S_{5,6}$ and $S_{2,3}$ operate at a high frequency. The dead time is inserted into the

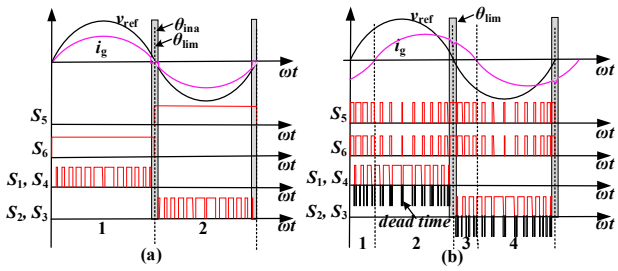


Fig. 2. Modulation schemes for the HERIC inverter: (a) the conventional UP-PWM and (b) the UP-PWM with dead time, where θ_{lim} and θ_{ma} are ZCD regions near the voltage ZCP and current ZCP, respectively.

commutation process to avoid short-circuiting. Since $S_{5,6}$ are all ON for zero voltages, there is a bidirectional path for the current. Therefore, the UP-PWM with dead time can provide reactive power.

C. Zero Crossing Distortion Analysis

Another issue for the HERIC inverter is the ZCD. In this section, the causes of the ZCD in the HERIC inverter are thus analyzed.

(1) *ZCD at the output voltage ZCP*: The minimum pulse width must be limited to a suitable value to prevent damage to power switches. Assuming that the grid voltage is $v_g(t) = V_m \sin(\omega t)$ and the grid current is $i_g(t) = I_m \sin(\omega t - \alpha)$, where α is the power factor angle. According to (1), then

$$v_{AB} = V_m \sin(\omega t) + L\omega I_m \cos(\omega t - \alpha) \quad (2)$$

Since the second part of (2) is very small, it can then be neglected. According to Fig. 2(a), the duty cycle d_d of $S_{1,4}$ or $S_{2,3}$ can be expressed as

$$d_d = \left\lfloor \frac{V_m \sin(\omega t)}{U_{dc}} \right\rfloor \quad (3)$$

where $v_{AB} = -d_d U_{dc}$. Assuming that the minimum pulse width limitation is d_{lim} . Then

$$\left\lfloor \frac{V_m \sin(\omega t)}{U_{dc}} \right\rfloor < d_{lim} \quad (4)$$

By solving (4), the obtained distortion region can be expressed as

$$\omega t \in [-\theta_{lim}, \theta_{lim}], \quad \theta_{lim} = \arcsin\left(\frac{d_{lim} U_{dc}}{V_m}\right) \quad (5)$$

Thus, the minimum pulse width limitation happens around the grid voltage ZCP.

When the condition in (5) holds, there are two methods to deal with the minimum pulse width limitation. One way assigns $d_d = 0$, and the other sets $d_d = d_{lim}$.

1) In the first method (i.e., $d_d = 0$), the derivative of the real grid current is expressed as

$$\frac{di_g(t)}{dt} = \frac{-V_m \sin(\omega t)}{L} \quad (6)$$

However, the desired grid current i_g^* can be given as

$$\frac{di_g^*(t)}{dt} = \frac{d_d U_{dc} - V_m \sin(\omega t)}{L} \quad (7)$$

Therefore, the current distortion Δi can be obtained as

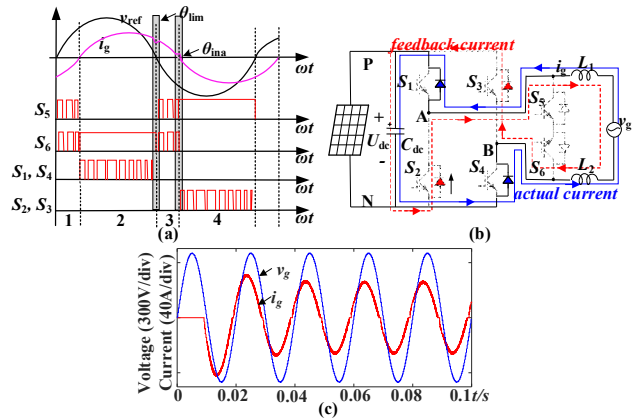


Fig. 3. Impact of the inaccuracy polarity: (a) the ideal modulation scheme, (b) the current flowing paths, and (c) simulation results.

$$|\Delta i| = \int_{\pi - \theta_{lim}/2}^{\pi} \left(\frac{d_d U_{dc} - V_m \sin(\omega t)}{\omega L} - \frac{-V_m \sin(\omega t)}{\omega L} \right) d\omega t = \frac{d_d U_{dc} \theta_{lim}}{2\omega L} \quad (8)$$

2) In the second method (i.e., $d_d = d_{lim}$), the derivative of the real grid current is expressed as

$$\frac{di_g(t)}{dt} = \frac{d_{lim} U_{dc} - V_m \sin(\omega t)}{L} \quad (9)$$

Subsequently, the current distortion Δi can be obtained in a similar manner as

$$|\Delta i| = \int_{\pi - \theta_{lim}/2}^{\pi} \left(\frac{d_{lim} U_{dc} - V_m \sin(\omega t)}{\omega L} - \frac{d_d U_{dc} - V_m \sin(\omega t)}{\omega L} \right) d\omega t = \frac{(d_{lim} - d_d) U_{dc} \theta_{lim}}{2\omega L} \quad (10)$$

Clearly, the grid current at the ZCP of the grid voltage will be distorted no matter what method of the two is adopted.

(2) *ZCD at the grid-connected current ZCP*: Usually, the polarity of the grid current is important for the implementation of modulation schemes. However, it is difficult to accurately determine the polarity of the grid current accurately near the ZCP due to measurement noises. The misjudgement of the current polarity happens around the ZCP, where the current is very small. The following demonstrates the ZCD at the grid-connected current ZCP.

An ideal modulation for the reactive power injection is shown in Fig. 3(a). When generating the positive power, the operation principle is the same as the conventional UP-PWM. When generating the negative power, only the AC bypass switches operate at a high frequency. The current flows through the four diodes to produce the positive or negative v_{AB} and flows through S_5 (D_5) and D_6 (S_6) to achieve zero voltages. In theory, the modulation method in Fig. 3(a) can not only achieve low ripple currents and high efficiency like the conventional UP-PWM, but also it can inject reactive power. However, if a misjudgement of the current polarity happens around the ZCP, e.g., as demonstrated in Fig. 3(b), where $v_{AB} < 0$, and the actual current $i_g < 0$ but the measured one is positive, i_g will be limited to zero crossing for a long period. Fig. 3(c) exemplifies the case. Nevertheless, as shown in Fig. 3(b), the actual current is expressed as

$$\frac{di_g(t)}{dt} = \frac{v_{AB} - V_m \sin(\omega t)}{L} \quad (11)$$

However, the desired grid current i_g^* is expressed as

$$\frac{di_g^*(t)}{dt} = \frac{-v_{AB} - V_m \sin(\omega t)}{L} \quad (12)$$

Therefore, the current distortion Δi can be obtained as

$$|\Delta i| = \left| \frac{-v_{AB} - V_m \sin(\omega t)}{L} - \frac{v_{AB} - V_m \sin(\omega t)}{L} \right| T_{sw} = \left| \frac{-2v_{AB} T_{sw}}{L} \right| \quad (13)$$

Moreover, in the worst case, the distortion may trigger the inverter protection, leading to a system shut down. This phenomenon is shown as the first cycle in Fig. 3(c). The current is limited to zero crossing for a long period. Then, the error between the reference current and the actual current accumulates. Therefore, the overshoot appears in the grid current, as shown in Fig. 3(c). The simulation results show that the overshoot value has been more than 1.5 times of the rated current, which is the maximum overcurrent capacity specified in most standards (notably, this can be changed according to the specific application.). This condition may trigger the overcurrent protection in practical application.

As mentioned previously, the inaccuracy is mainly related to signal noises. The signal noise generally includes sampling noise, transmission noise, and current ripples. The current ripples are mainly responsible for the inaccuracy. In the hardware design, the current ripple rate r should be controlled to an optimum value [28]. Generally, the current ripple rate r should be designed to be under 0.2 in most engineering design. To avoid this, the inaccuracy of the current polarity, which can be a fixed value, must contain the maximum noise value. Thus, the inaccuracy is set to be between $-0.1i_{crms}$ and $0.1i_{crms}$ (notably, this can be changed according to the specific design), where i_{crms} is the root mean square (RMS) of the rated output current of the inverter i_c . Then, the inaccuracy range can be expressed as

$$\omega t \in [-\theta_{ina}, \theta_{ina}], \quad |\theta_{ina}| = \frac{\pi}{2} \frac{0.1i_{crms}}{i_{grms}} \quad (14)$$

in which θ_{ina} is the boundary, and i_{grms} is the RMS of real-time grid current. To address this impact due to the misjudgement of the current polarity, the desired voltage in the region of the grid current ZCP must be built up arbitrarily.

In all, the ZCD issues exist in the above modulation schemes for the HERIC inverter. With the conventional UP-PWM in the unity power factor operation, the ZCD regions θ_{lim} and θ_{ina} coincide. However, under the UP-PWM with inserted dead time, only the ZCD at the voltage ZCP is obvious. When the HERIC inverter adopts the modulation method in Fig. 3(a) with the non-unity power factor operation, both ZCD regions will appear as discussed in the above. As a consequence, the modulation schemes should be enhanced to mitigate the corresponding distortions.

III. PROPOSED HYBRID UP-PWM TECHNIQUE

To achieve a high efficiency, good power quality, and proper reactive power capability, a hybrid UP-PWM technique for the HERIC inverter is proposed in this section. The operation principles are illustrated in Fig. 4. When the inverter is

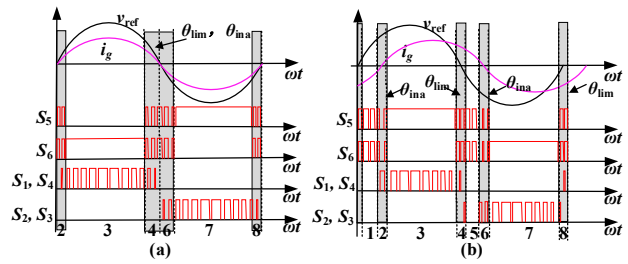


Fig. 4. Proposed hybrid UP-PWM for the HERIC inverter to improve the power quality and efficiency: (a) at the unity power factor operation and (b) at the non-unity power factor operation.

operating at a non-unity power factor, the operation can be partitioned into eight regions as shown in Fig. 4(b). Regions 2, 4, 6 and 8 should be specially considered. As the output voltage or current of the inverter is very small, the operation of power switches is limited and their polarities are difficult to determine. On the contrary, regions 1, 3, 5 and 7 are much easier to cope with. In this regard, the proposed hybrid UP-PWM strategy adopts different modulation schemes according to the operational regions. There are three modulation schemes:

(1) Conventional UP-PWM in regions 3 and 7. The conventional UP-PWM strategy can achieve low switching power losses and low ripple currents.

(2) UP-PWM with dead time in regions 2, 4, 6 and 8. Due to the polarity uncertainty of the grid current, the UP-PWM with dead time is adopted to ensure a stable operation of the inverter system. In addition, the adverse effect of the minimum pulse width limitation can be improved by modifying the dead time.

(3) UP-PWM for negative power generation in regions 1 and 5. To provide reactive power and also reduce the switching power losses, the modulation, only requiring the operation of AC bypass switches like Fig. 3(a), is applied to the HERIC inverter.

It should be pointed out that regions 1 and 5 are absent in the case of the unity power factor operation. Thus, only two operation modes (i.e., the conventional UP-PWM and UP-PWM with dead time) are active in the proposed strategy, as shown in Fig. 4(a).

According to Fig. 5, the operation principle of the proposed hybrid UP-PWM scheme for the HERIC inverter is elaborated in detail as follows:

Region 1: As shown in Fig. 5(a) and (b), all the four-leg power switches are in off-state, while the additional two power switches are operating at a high frequency. The grid-connected current i_g flows through the diodes D_1 and D_4 to build up a positive voltage v_{AB} , while flows through S_5 and D_6 to generate a zero voltage.

Region 2: At the current ZCP, the leg power switches S_1 , S_4 and the additional two power switches S_5 , S_6 operate at a high frequency. In that case, there are two current paths. 1) As shown in Fig. 5(c) and (d), the current i_g continues flowing through D_1 and D_4 to ensure a positive voltage v_{AB} , and the current i_g also flows through S_5 and D_6 to achieve a zero voltage. 2) As shown in Fig. 5(e) and (f), the grid-connected current polarity changes, and it flows through S_1 and S_4 , resulting in a positive voltage v_{AB} ; while a zero voltage v_{AB} is built up, when the current flows through S_6 and D_5 . The dead time must be inserted between operation mode changes.

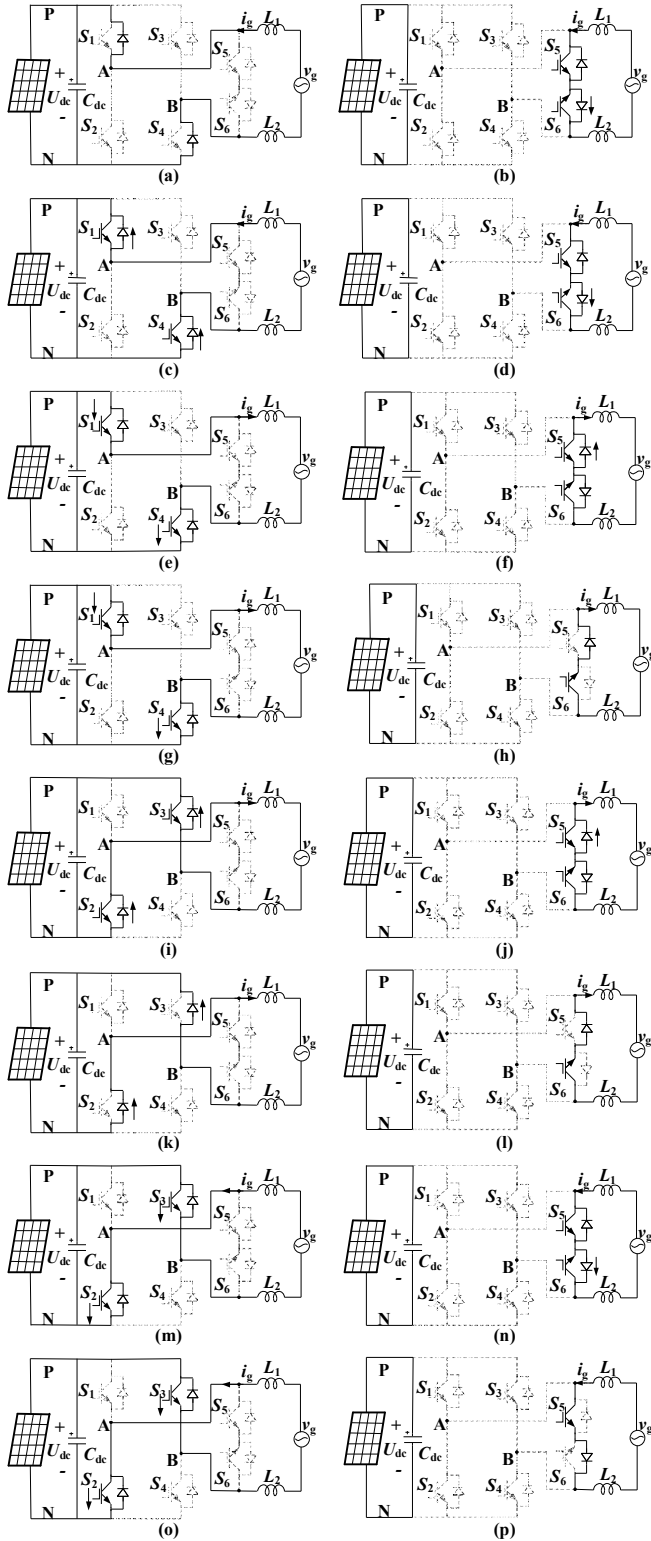


Fig. 5. Operation modes of the proposed hybrid UP-PWM for the HERIC inverter.

Region 3: As shown in Fig. 5(g) and (h), S_6 is always in on-state, while S_1 and S_4 are switched at a high frequency in this operational region. The grid-connected current i_g then flows through S_1 and S_4 for a positive voltage v_{AB} , while flows through S_6 and D_5 for a zero voltage.

Region 4: At the voltage ZCP, there are two transitioning modes. 1) S_1 and S_4 are in on-state to generate a positive voltage v_{AB} , as shown in Fig. 5(e) and (f), and the current i_g flows through S_1 and S_4 . Then, S_5 and S_6 are switched-on to achieve a zero voltage, and then the current i_g flows through S_6 and D_5 . 2) As shown in Fig. 5(i) and (j), S_2 and S_3 are in on-state, leading to a negative voltage v_{AB} , and the current i_g flows through D_2 and D_3 . Following, S_5 and S_6 are in on-state for a zero voltage, and the grid-connected current i_g flows through S_6 and D_5 . During the mode transitions, the dead time should be applied to avoid short-circuiting the DC side.

Region 5: As illustrated in Fig. 5(k) and (l), all the four leg power devices are switched-off, while S_5 and S_6 operate at a high frequency. The grid-connected current i_g then continues flowing through D_2 and D_3 for a negative voltage v_{AB} , while through S_6 and D_5 to generate a zero voltage.

Region 6: Near the current ZCP, the switches S_2 , S_3 and additional switches S_5 , S_6 operate at a high frequency. There are two current paths. 1) Fig. 5(i) and (j) show that the current i_g flows through D_2 and D_3 , which gives a negative voltage v_{AB} , and then through S_6 and D_5 for a zero voltage. 2) As shown in Fig. 5(m) and (n), the grid-connected current i_g flows through S_2 and S_3 to ensure a negative voltage v_{AB} , and then through S_5 and D_6 for a zero voltage. The dead time must be inserted between mode transitions.

Region 7: As shown in Fig. 5(o) and (p), S_5 is always in ON, while S_2 and S_3 are switched at a high frequency. The grid-connected current i_g flows through S_2 and S_3 to generate a negative voltage v_{AB} , while through S_5 and D_6 to achieve a zero voltage.

Region 8: At the voltage ZCP, there are two modes. 1) As shown in Fig. 5(m) and (n), S_2 and S_3 are in on-state to ensure a negative voltage v_{AB} , and the grid-connected current i_g flows through S_2 and S_3 . Then, S_5 and S_6 are switched to achieve a zero voltage, and the grid-connected current i_g flows through S_5 and D_6 . 2) As shown in Fig. 5(c) and (d), S_1 and S_4 are in on-state for a positive voltage v_{AB} , and the grid-connected current i_g flows through D_1 and D_4 . Then, S_5 and S_6 are in on-state to achieve a zero voltage, and the grid-connected current i_g flows through S_5 and D_6 . The dead time is required during the operation mode transitions.

A. Elimination of the ZCD at the Voltage ZCP

When adopting the UP-PWM with inserted dead time at the voltage ZCP, the dead time impacts the reference output voltage. As mentioned previously, the minimum pulse width limitation should be considered near the voltage ZCP. When the duty cycle d_d is less than the minimum pulse width ratio d_{lim} , d_d is forced to zero or d_{lim} . Hence, the current cannot exactly follow the reference. To tackle those issues, the compensation for the dead time and minimum pulse width limitation is needed. As a consequence, the duty cycle of the improved compensation method can further be expressed as

$$D = d_d + 3\varepsilon \quad \text{and} \quad \varepsilon = \begin{cases} \varepsilon & , d_d > d_{lim} \\ d_{plu} / 2, & d_d \leq d_{lim} \end{cases} \quad (15)$$

where ε is the duty cycle of the dead time, and d_{plu} is the added duty cycle of the dead time to compensate the minimum pulse width limitation. To ensure an effective switching operation, d_{plu} should be two times of d_{lim} . Notably, d_{lim} is always determined

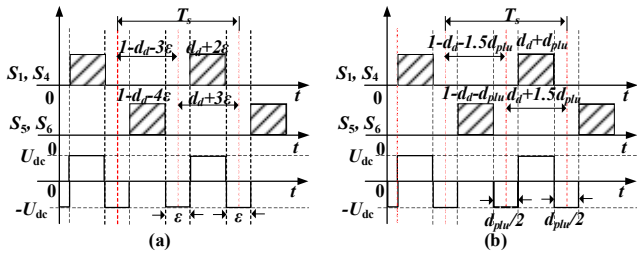


Fig. 6. Compensation principle for the dead time and minimum pulse width limitation.

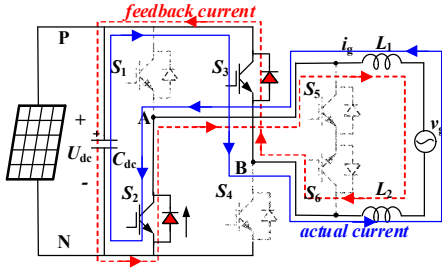


Fig. 7. Current flowing path of the proposed modulation scheme.

by the switching speed of the power devices. Generally, d_{lim} is equal to $2(t_{on}+t_{off})$, where t_{on} and t_{off} are the turn-on time and the turn-off time of switches, respectively. Then, d_{plu} is equal to $4(t_{on}+t_{off})$. The turn-on time and turn-off time of the power devices can be obtained from the device datasheet.

(1) When $d_d > d_{lim}$, the compensation principle of dead time is exemplified in Fig. 6(a). As it is observed, there are two dead times intervals in one switching period, T_s . Due to the negative voltage in the dead time, the duty cycle is then changed to $D = d_d + 3\varepsilon$, according to (15). In this case, the inverter output voltage can be obtained as

$$v_{AB}|_{T_s} = (d_d + 2\varepsilon)U_{dc} + (1 - d_d - 4\varepsilon)0 + 2\varepsilon(-U_{dc}) = d_d U_{dc} \quad (16)$$

(2) When $d_d \leq d_{lim}$, the compensation principle of the minimum pulse width limitation is shown in Fig. 6(b). The duty cycle must be larger than the minimum pulse width ratio d_{lim} . According to (10), the inverter output voltage can be given by

$$v_{AB}|_{T_s} = (d_d + d_{plu})U_{dc} + (1 - d_d - 1.5d_{plu})0 + d_{plu}(-U_{dc}) = d_d U_{dc} \quad (17)$$

Therefore, in the improved methods, the desired output voltage can be achieved. The compensation principle is also suitable for the UP-PWM with inserted dead time at the current ZCP.

B. Elimination of the ZCD at the Current ZCP

Compared with the modulation in Fig. 3(a), the UP-PWM with dead time is adopted in the region $[-\theta_{ina}, \theta_{ina}]$ at the grid current ZCP in the proposed scheme. With this, the desired output voltage can still be guaranteed even when the polarity of the feedback current is misjudged. For example, the grid current ZCP in Fig. 3(a) is similar to that in the region 6 of Fig. 4(b). The power switches $S_{2,3}$ and the additional switches $S_{5,6}$ operate at a high frequency. When the current is positive, the current flows through D_2 and D_3 to obtain the desired inverter voltage $-v_{AB}$, which is shown by the red dotted line in Fig. 7. When the current is negative, the desired voltage $-v_{AB}$ can also be achieved due to the current flow through S_2 and S_3 , which is shown as the blue

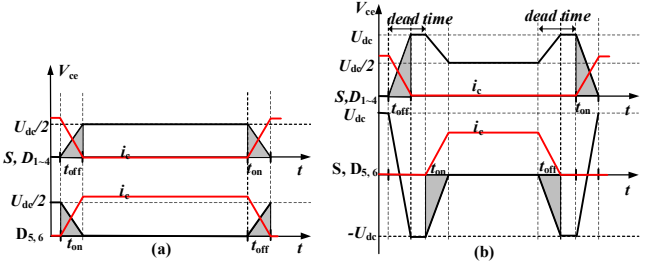


Fig. 8. Switching losses with different modulation strategies: (a) the conventional UP-PWM and (b) the UP-PWM with dead time.

solid line in Fig. 7. In all, the proposed modulation scheme provides a bidirectional path for the current commutation by adopting the UP-PWM with dead time in the region at the grid-connected current ZCP. Thus, the ZCD induced by the inaccuracy current polarity can be alleviated.

C. Switching Losses

Power semiconductor losses consist of conduction losses and switching losses. Generally, the conduction losses are always independent of the modulation strategies but the system load. Modulation methods, however, affect the profile of switching losses. As it has been discussed in [26] and [27], the switching losses of the IGBT with an anti-parallel diode can be obtained as

$$P_{SW} = P_M + P_D = [(E_{onM} + E_{offM}) + E_{onD}] \cdot f_s \cdot \frac{V_{cc} i_c}{V_{CC} I_{CC}} \quad (18)$$

where P_{SW} is the total switching losses, P_M is the losses in the IGBT, P_D is the losses in the diode, f_s is the switching frequency, and E_{onM} , E_{offM} , and E_{onD} are the turn-on energy losses, turn-off energy losses, and diode reverse-recovery energy losses, correspondingly, which are provided in the datasheet under certain test conditions. The test voltage V_{CC} and current I_{CC} are the reference commutation voltage and current, respectively [26]. Thus, according to (18), during the switching interval, the instantaneous collector-emitter voltage V_{ce} and the collector current i_c will affect the total power losses, which is related to the modulation scheme.

In the case of the conventional UP-PWM, V_{ce} and i_c are illustrated in Fig. 8(a). Due to the grid fundamental frequency operation, the switching losses of $S_{5,6}$ only include diode losses. Hence, the total switching losses can be obtained as

$$P_{SW_L} = P_{M_S1-4} + P_{D_S1-6} = [2(E_{onM} + E_{offM}) + 3E_{onD}] \cdot f_s \cdot \frac{U_{dc} i_c / 2}{V_{CC} I_{CC}} \quad (19)$$

However, the switching losses of the UP-PWM with inserted dead time, which is shown in Fig. 8(b), are given as

$$P_{SW_H} = P_{M_S1-6} + P_{D_S1-6} = [(E_{onM} + E_{offM}) + E_{onD}] \cdot 3f_s \cdot \frac{U_{dc} i_c}{V_{CC} I_{CC}} \quad (20)$$

Assuming that t_{off} and t_{on} are the same, the switching losses of the UP-PWM with dead time are more than twice the switching losses of the conventional UP-PWM. The differential-mode voltage v_{AB} is equal to 0 with inserted dead time. Moreover, v_{AB} in the case of the conventional UP-PWM changes from U_{dc} to 0, while in the UP-PWM with dead time from U_{dc} to $-U_{dc}$. Thus, the ripple currents of the conventional

TABLE I
PARAMETERS OF THE SINGLE-PHASE SINGLE-STAGE HERIC INVERTER SYSTEM.

Symbols	Parameters	Values
P	Output power	4 kW
U_{dc}	DC-link voltage	360 V
v_g	Grid voltage (RMS)	220 V
f	Grid frequency	50 Hz
C_{dc}	Input DC capacitor	2800 μ F
L_1, L_2	Filter inductor	1 mH
f_s	Switch frequency	20 kHz
ε	Dead time	1.5 μ s

UP-PWM are small. Additionally, in the proposed scheme, the modulation that only requires the operation of AC bypass switches has the same ripple currents and switching losses, compared to the conventional UP-PWM.

Notably, in most cases, the proposed hybrid UP-PWM method operates with the conventional modulation strategy and the modulation that only requires the operation of AC bypass switches. Only in the compensation range, regions 2, 4, 6 and 8 in Fig. 4(b), the UP-PWM with dead time should be applied. Therefore, the efficiency and ripple currents of the proposed hybrid UP-PWM scheme are close to that of the conventional UP-PWM scheme. The hybrid UP-PWM method takes the advantages of the three modulation methods to achieve low switching power losses, good power quality, and also reactive power capability. The performances of the proposed method are validated in the following section.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

In order to verify the proposed modulation scheme and the above discussions, simulations are carried out using the Piecewise Linear Electrical Circuit Simulation (PLECS) software. The main system parameters are listed in Table I. In order to analyze the efficiency of the HERIC inverter, a thermal-loss model of the power switches is established for calculations according to the datasheet of Infineon IKW3N65EL5 IGBT. The comparison between the conventional UP-PWM, the UP-PWM with dead time, and the proposed hybrid UP-PWM is performed. As mentioned previously, there are two methods to deal with the minimum pulse width limitation in the conventional UP-PWM and the UP-PWM with dead time. One method is to set $d_d = 0$, and the other assigns $d_d = d_{lim}$. In the simulation and experiment, d_d is set to be zero (i.e., $d_d = 0$) when the minimum pulse width limitation appears.

Fig. 9 shows the performance of the proposed hybrid UP-PWM scheme at different power factors. The simulation results illustrate that v_{AB} changes between U_{dc} and $-U_{dc}$ at a high frequency just in the ZCP regions of i_g and v_g , as the proposed hybrid UP-PWM scheme adopts the UP-PWM with the modified dead time in those ZCP regions. Additionally, v_{AB} changes between U_{dc} and 0 or $-U_{dc}$ and 0 at a high frequency in others regions, which is the same as the conventional UP-PWM. It is worth noting that the ZCP regions of the grid current and

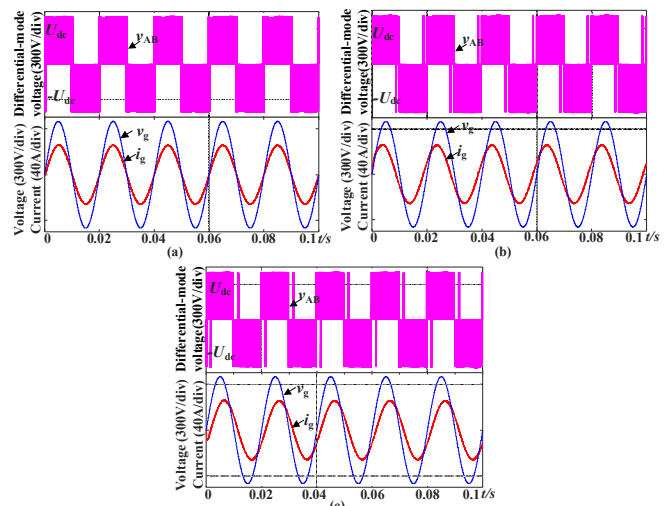


Fig. 9. Simulation results (the differential-mode voltage: v_{AB} , the grid-connected current i_g , and the grid voltage v_g) with the proposed hybrid UP-PWM method. (a) at the unity power factor, (b) with i_g leading v_g ($\cos\varphi = 0.9$), and (c) with i_g lagging v_g ($\cos\varphi = -0.9$).

voltage coincide at the unity power factor, as shown in Fig. 9(a). Moreover, v_{AB} performs differently, as it can be observed clearly in Fig. 9(b) and (c) (i.e., $\cos\varphi = 0.9$ and -0.9). It is also seen in Fig. 9 that the ZCD impact is eliminated in all cases. The above results verify the effective operation of the proposed modulation scheme.

Fig. 10 compares the performances of the three modulation schemes at the unity power factor and the non-unity power factor (i.e., $\cos\varphi = \pm 0.9$) operation. The grid voltage v_g , the grid current i_g , the reference current i_{ref} , and the ripple current i_{rip} are shown in Fig. 10. It can be observed in Fig. 10(c) that with the proposed modulation strategy, the ZCD is smaller than that in Fig. 10(a) and (b) with the conventional UP-PWM or the UP-PWM with dead time, respectively. The ripple currents of the conventional UP-PWM, the UP-PWM with dead time, and the proposed hybrid modulation strategy are 1.40 A, 1.80 A, and 1.44 A, which are shown in Fig. 10(a)-(c), correspondingly. After applying the Fast Fourier Transformation (FFT) to the grid current i_g , the Total Harmonic Distortion (THD) levels of the grid currents are obtained as 2.4%, 3.1%, and 1.6% for the three modulation strategies operating at the unity power factor. It is thus verified that the power quality with the proposed hybrid modulation strategy is better than that of the conventional UP-PWM and the UP-PWM with dead time at the unity power factor.

In the case of a non-unity power factor operation, as shown in Fig. 10(d)-(g), the proposed hybrid UP-PWM achieves better performances than the UP-PWM with dead time, especially at the grid voltage and current ZCP. Fig. 10(d) and (f) show the simulation results of the UP-PWM with dead time and the proposed hybrid UP-PWM when i_g leads v_g (i.e., $\cos\varphi = 0.9$). Fig. 10(e) and (g) show the simulation results of those when i_g lags v_g (i.e., $\cos\varphi = -0.9$). As mentioned previously, the conventional UP-PWM has no reactive power capability. Therefore, the operation of the conventional UP-PWM in the non-unity power factor is not performed. Obviously, the ZCD and ripple current of the proposed hybrid modulation scheme are smaller than those of the UP-PWM with dead time, as

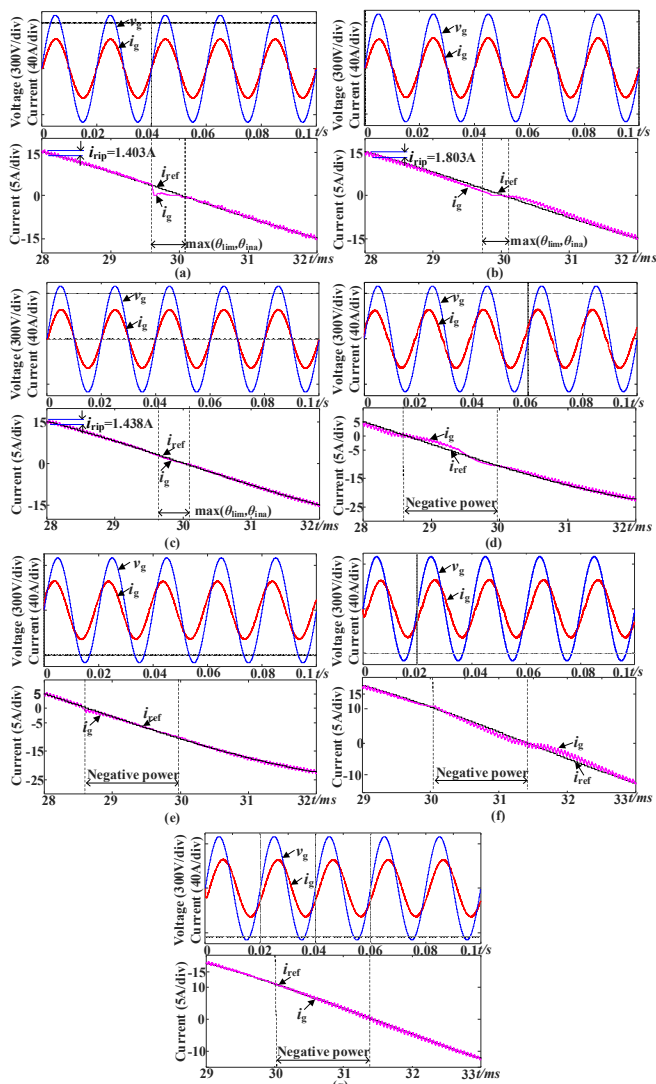


Fig. 10. Simulations of the single-phase single-stage grid-connected HERIC inverter with different modulation schemes: (a) the conventional UP-PWM at the unity power factor, (b) the UP-PWM with dead time at the unity power factor, (c) the hybrid UP-PWM at the unity power factor, (d) the UP-PWM with dead time and i_g leading v_g ($\cos\phi = 0.9$), (e) the hybrid UP-PWM with i_g leading v_g ($\cos\phi = 0.9$), (f) the UP-PWM with dead time and i_g lagging v_g ($\cos\phi = -0.9$), and (g) the hybrid UP-PWM with i_g lagging v_g ($\cos\phi = -0.9$).

demonstrated in Fig. 10(d)-(g). Moreover, the current THD levels are 3.3%, 2.0%, 3.18%, and 2.02% in Fig. 10(d)-(g), respectively. The results illustrate that the proposed modulation strategy not only has the reactive power capability but also has a better performance than the UP-PWM with dead time in terms of power quality.

Furthermore, the power semiconductor losses include conduction losses and switching losses. Therefore, the power semiconductor losses of all IGBTs are calculated and simulated by the PLECS software at different power levels (1 kW to 4 kW). The Fig. 11 shows the results of conduction losses (as shown in the solid lines) and switching losses (as shown in the dotted lines) with different modulation methods. It can be observed in Fig. 11 that the total switching losses of the HERIC inverter with the proposed modulation scheme are close to those with the conventional UP-PWM, and less than a half of

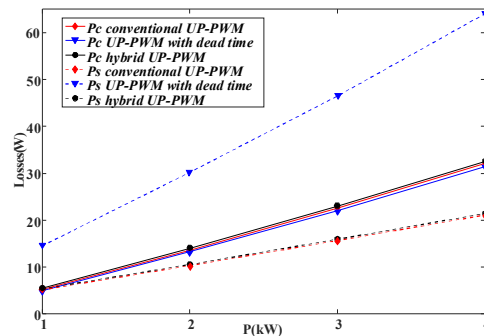


Fig. 11. Power losses analysis of the HERIC inverter by simulations (the conduction losses and switching losses in PLECS), where P_c and P_s are the conduction losses and the switching losses, correspondingly.

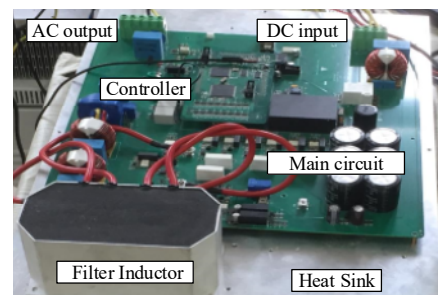


Fig. 12. Experimental setup of a 4-kW single-stage single-phase grid-connected HERIC inverter.

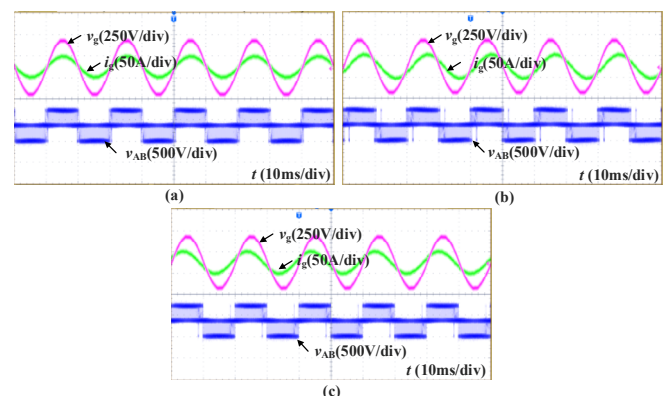


Fig. 13. Experimental results (the differential-mode voltage: v_{AB} , the grid current: i_g and the grid voltage: v_g) of the HERIC inverter with the proposed hybrid UP-PWM method. (a) at the unity power factor, (b) with i_g leading v_g ($\cos\phi = 0.9$), and (c) with i_g lagging v_g ($\cos\phi = -0.9$).

the total with the UP-PWM with dead time. Notably, the conduction losses of the three modulation schemes are almost the same, as depicted in Fig. 11. The simulation results have verified that the hybrid UP-PWM scheme can improve the power quality without compromising the conversion efficiency. Simulation results are in a close agreement with the theoretical analysis.

B. Experimental Results

A 4-kW single-stage single-phase prototype of the HERIC inverter was built up as shown in Fig. 12 in order to further verify the effectiveness of the proposed hybrid UP-PWM technique. The experimental setup includes a Tektronix DPO3014 Oscilloscope, a Fluke 4341 Power Quality Analyzer, and a HIOKI 3390 Power Analyzer. The modulation algorithms

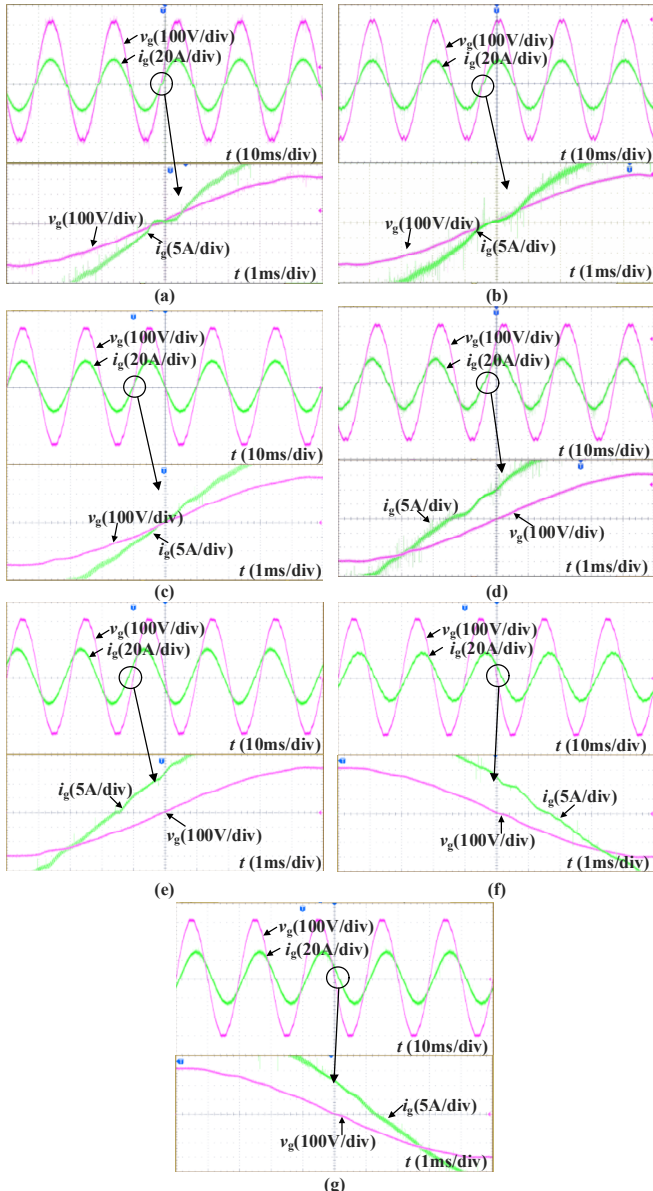


Fig. 14. Performance of the 4-kW single-stage single-phase grid-connected HERIC inverter system with different modulation schemes: (a) the conventional UP-PWM at the unity power factor, (b) the UP-PWM with dead time at the unity power factor, (c) the hybrid UP-PWM at the unity power factor, (d) the UP-PWM with dead time and i_g leading v_g ($\cos\phi = 0.9$), (e) the hybrid UP-PWM with i_g leading v_g ($\cos\phi = 0.9$), (f) the UP-PWM with dead time and i_g lagging v_g ($\cos\phi = -0.9$), and (g) the hybrid UP-PWM with i_g lagging v_g ($\cos\phi = -0.9$).

were implemented on a TI TMS320F28335 floating-point digital signal processor (DSP) and the gate signals of the IGBTs are generated by Altera EP2C8T144C8N FPGA. The parameters of the system are the same as those in simulations, which are listed in Table I. In addition, the input voltage was provided by a DC power supply, and the output was connected to the real power grid.

The performance of the HERIC inverter with the proposal modulation strategy at the unity power factor and non-unity power factor (i.e., $\cos\phi = \pm 0.9$) are shown in Fig. 13. The experimental results are in close agreement with the simulation results shown in Fig. 9. The differential-mode voltage v_{AB}

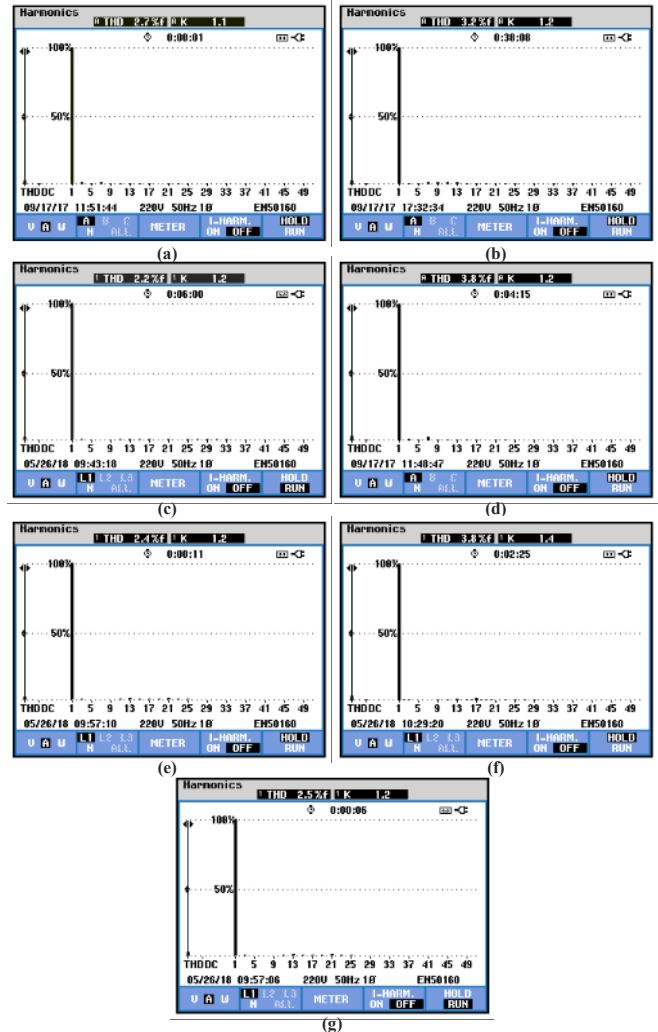


Fig. 15. Measured THD levels and harmonic distortion of the grid currents of the HERIC inverter with different modulation strategies: (a) the conventional UP-PWM at the unity power factor, (b) the UP-PWM with dead time at the unity power factor, (c) the hybrid UP-PWM at the unity power factor, (d) the UP-PWM with dead time and i_g leading v_g ($\cos\phi = 0.9$), (e) the hybrid UP-PWM with i_g leading v_g ($\cos\phi = 0.9$), (f) the UP-PWM with dead time and i_g lagging v_g ($\cos\phi = -0.9$), and (g) the hybrid UP-PWM with i_g lagging v_g ($\cos\phi = -0.9$).

changes between U_{dc} and $-U_{dc}$ at a high frequency in the region of the grid current and voltage ZCP, which is shown clearly in Fig. 13(b) and (c). When the power factor is unity, the ZCP regions of the grid current and voltage coincide, as shown in Fig. 13(a). Both simulation and experimental results indicate that v_{AB} reflects the modulation principle of the proposed hybrid UP-PWM scheme at different power factors.

The performance of the HERIC inverter at the unity power factor with the three modulation strategies (i.e., the conventional UP-PWM, the UP-PWM with dead time, and the hybrid UP-PWM) is shown in Fig. 14, which indicates that experimental results agree well with the simulation results shown in Fig. 10. The grid current ZCD when the proposed hybrid modulation scheme is adopted can be seen in Fig. 14(c), which is lower than that in Fig. 14(a) and (b) with the conventional UP-PWM and the UP-PWM with dead time, respectively. The THD levels of the grid currents at the unity

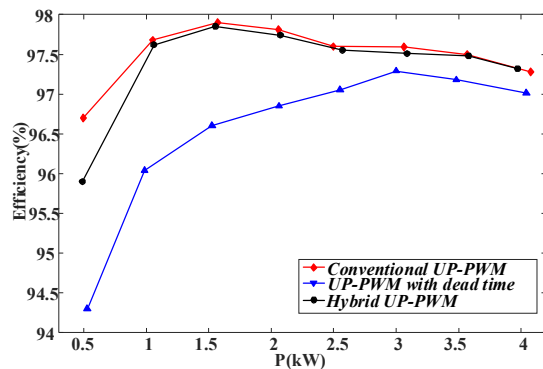


Fig. 16. Measured efficiency of the HERIC inverter with different modulation schemes.

power factor are 2.7%, 3.2%, and 2.2%, as also observed in Fig. 15(a)-(c), correspondingly. The results have validated that the hybrid UP-PWM scheme can achieve better performance than the other two methods at the unity power factor.

In the case of the non-unity power factor operation with the UP-PWM with dead time and the proposed hybrid UP-PWM, the experimental results of the HERIC inverter are shown in Fig. 14(d)-(g). The corresponding THD levels with i_g leading v_g are 3.8% and 2.4%, as shown in Fig. 15(d) and (e). The THDs with i_g lagging v_g are 3.8% and 2.5%, as shown in Fig. 15(f) and (g). Furthermore, it can be seen in Fig. 14(e) and (g) that the resultant grid current ZCD with the proposed strategy is lower than that in Fig. 14(d) and (f) when the UP-PWM with dead time is employed. Notably, the THD level of the real grid voltage keeps in the range of 1.5%~1.6% in the experiment. Thus, the experimental results of those three modulation methods are effective. In all, both simulations and experiments have verified the effectiveness of the proposed scheme with the duty-cycle compensation, which not only improves the power quality but also provides reactive power supporting.

The efficiency of the proposed system is measured by a HIOKI 3390 Power Analyzer as shown in Fig. 12. The power analyzer measures the input power and output power to obtain the efficiency of the HERIC inverter. Therefore, the losses of the filter inductor are also included in the total power losses of the system. The experimental efficiencies of the HERIC inverter system are depicted in Fig. 16, which shows that the proposed scheme achieves almost the same efficiency profile under different power levels as the conventional UP-PWM. Since the inaccuracy range of current polarity is set to be between $-0.1i_{erms}$ to $0.1i_{erms}$ (i.e., -1.8 A to 1.8 A). Correspondingly, $|\theta_{ma}|$ is 0.4π when the output power is 500 W. Thus the regions that adopt the UP-PWM with dead time are so large that the efficiency is lower than the conventional UP-PWM. That is, the UP-PWM with dead time has the lowest efficiency. This is in agreement with the simulation results (power losses in Fig. 11). Notably, the efficiency measured in the experiments considers the inductor power losses, and thus the efficiency is not in a linear relationship with the power levels. In a word, the above simulations and experimental tests have verified the effectiveness of the proposed hybrid UP-PWM for the HERIC inverter in terms of improved efficiency, enhanced power quality, and also enabled the reactive power capability.

V. CONCLUSION

In this paper, a hybrid UP-PWM strategy for the HERIC inverter was proposed. The proposed method takes the advantages of the conventional UP-PWM, the UP-PWM with dead time and the modulation strategy of reactive power capability. In the operational mode of generating the positive power, the proposed scheme adopts the conventional UP-PWM. Furthermore, only two additional power switches are operating at a high frequency when the negative power generation is enabled. In that case, the proposed PWM scheme can achieve low switching power losses and small ripple currents. Moreover, the UP-PWM with dead time is used at the voltage and current ZCPs to ensure a stable operation of the inverter system and also lower distortions. To further improve power quality, the effects of the dead time and minimum pulse width limitation were compensated through the hybrid UP-PWM scheme. The simulation and experimental results have verified the effectiveness of the hybrid UP-PWM scheme in terms of enhanced power quality, improved efficiency, and more importantly, flexible reactive power controllability.

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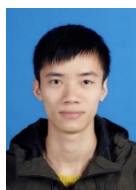
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