Modified Secondary-Control-Based Fault Current Limiter for Inverters

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A Modified Secondary-Control-Based Fault Current Limiter for Four-Wire Three-Phase DGs

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***Abstract*— Fault Current Limiters (FCLs) are one of the main solutions to upcoming challenges in microgrid protection. Regarding the high penetration of distributed generations (DGs) in future power system, designing cheap and effective FCL is a necessity. The present study addresses this issue by proposing an embedded FCL operating based on modifying the secondary control of four-wire DG. As this method is presented for a four-wire system, besides very low implementing cost, it has independency and flexibility to only limit the current of DG faulted phase. This study also provides real-time simulation results by OPAL-RT to compare the proposed method with a virtual-impedance-based FCL to validate its effectiveness. Finally, experimental results are presented to validate the effectiveness of the proposed FCL.**

***Index Terms*— Fault current limiter, moving average filter (MAF), protection, secondary control.**

I. Introduction

DURING the recent decades, different types of Fault Current Limiters (FCLs) including passive FCL (PFCL), superconducting FCL (SFCL), solid state FCL (SSFCL), and controlled-based FCL have been proposed [1]. PFCLs use passive elements to limit the fault current. Although it is the cheapest and simplest type of FCL, the voltage drop during the normal condition is the main drawback of this approach. SFCLs are classified into resistive and inductive types. Both types have the advantages of low power loss during the normal conditions and fast response. Whereas, high weight/size, requiring of an advanced cooling system, and high cost are their main drawbacks [2]. With the recent advances in the semiconductor technology, implementing the SSFCL has become more realistic and cost-efficient [3]. SSFCL have fast response and low weight/size; however it has high commutation and on-state losses [4]. Recently, wide bandgap power switches, which are mostly constructed based on Silicon Carbide (SiC) and Gallium Nitride (GaN) materials, have been developed and commercialized [5].

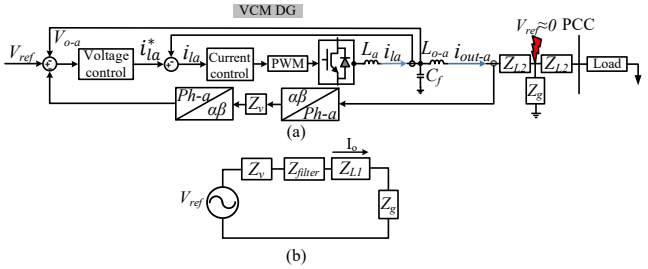

Fig. 1. (a) Model of a VCM-VSI connected to a load. (b) Equivalent model of the system from VCM-VSI perspective.

These devices have characteristics such as, low on-state loss, low thermal loss, high frequency, and high voltage capability. Thanks to these properties, wind band gap devices are a promising solution to address high loss of the SSFCL. In addition to these external FCLs, virtual impedance (VI)-based FCL had been proposed as a cost-efficient and low power loss solution to reduce fault current [6]. In this method, the VI is set to zero when the peak current is lower than its threshold and increases to a positive non-zero value when the peak current is larger than its threshold. However, due to no usage of any filters for current if a high level of current harmonics exists in the grid, the peak value of current is not a constant anymore. As a consequence, VI oscillates between zero and non-zero values, which results in loss of controlling. Furthermore, fixed value of maximum VI for all fault conditions, which is chosen in [6], leads to the same behavior. Because VI fluctuates between a zero and nonzero value when the required VI is lower than selected maximum values.

The objective of this study, which is an extension of the work proposed in [7], is addressing the aforementioned problems of VI-based FCL. To this end, a secondary control-based FCL is presented to limit the fault current to twice its nominal value for a four-wire three-phase DG working in the Voltage-Control Mode (VCM). The proposed FCL has a fast response and low implementation cost. The real-time simulation results as well as experimental results are presented to validate the efficiency of the proposed method over the VI-FCL.

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II. MULTILOOP CONTROL OF FOUR-WIRE THREE-PHASE INVERTER

In low-voltage microgrids, the three-phase four-wire system is a commonly used topology to support single-phase and unbalanced loads by building a path for the zero-sequence current of the loads. The three-leg inverter with split dc-link capacitors is one of the most widely used configuration where the midpoint of the dc-link is connected to a neutral point [8]. It must be noted that, four leg inverters can be used with the same purpose. In the islanded operation mode of the microgrid, at least one DG has to operate in the VCM to control both voltage and frequency.

Each VCM Voltage Source inverter (VCM-VSI) control system composes of a primary, secondary, and tertiary control. In the primary level, the droop control and virtual impedance is utilized to regulate the power sharing as well as stabilizing the voltage and frequency. In a VCM-VSI, the generated voltage reference is fed into inner control loops consisting of outer voltage loop and inner current loop to regulate the capacitor voltage.

In the steady state, voltage and frequency may deviate from their nominal values. In this case, the secondary control could be used to restore the voltage and frequency to their nominal values. In the secondary control level, proportional integral (PI) controllers are applied to generate proper control signals to be followed by droop controllers and restore both frequency and voltage to their nominal values. The related equations are as follows [9]:

$$\delta E = k_{PE}(E^*_{MG} - E_{MG}) + k_{iE}\int\left((E^*_{MG} - E_{MG})\right)dt \qquad (1)$$

$$\delta f = k_{Pf}(f^*_{MG} - f_{MG}) + k_{if}\int\left((f^*_{MG} - f_{MG})\right)dt \qquad (2)$$

where, f_{MG}, f^*_{MG}, E_{MG}, E^*_{MG}, and $k_{PE}(k_{Pf})$ as well as $k_{iE}(k_{if})$ denote the actual frequency, reference frequency, actual voltage, reference voltage, and the parameters of PI controllers, respectively. Once these correction values of voltage and frequency are obtained, these signal values are sent to the primary control of each DG units.

III. PROPOSED METHOD

As mentioned before, the secondary control is used to manipulate voltage and frequency references to restore voltage and frequency, respectively. However, under faulty conditions a high compensation term has to be added to the voltage reference to approach output voltage to its nominal value. This approach results in the injection of a large current to the grid. Hence, the secondary control must be modified to avoid damage to the VCM-VSI.

The model of a simple microgrid that composes of a VCM DG, connected to a constant load is shown in Fig. 1 (a). For a fault happening between the VCM-VSI and PCC, the equivalent model of microgrid from the VCM-VSI perspective is presented in Fig. 1 (b).

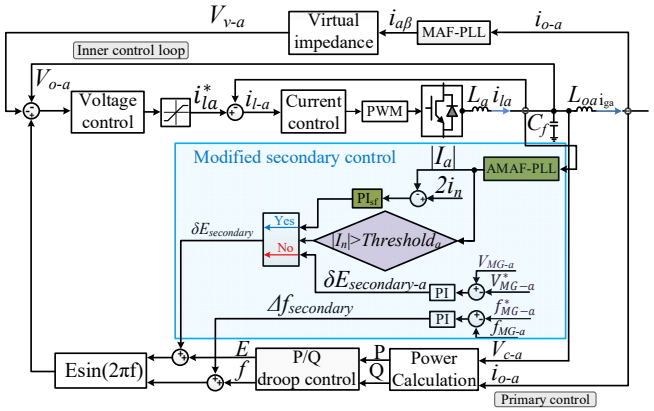

Fig. 2. Proposed FCL for voltage-control of phase-a of the three-phase four-wire VCM DG with a split dc capacitors.

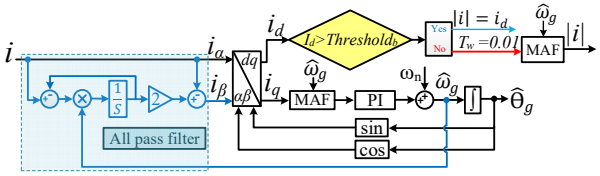

Fig. 3. Proposed FCL for voltage-control of phase-a of the three-phase four-wire VCM DG with a split dc capacitors.

According to this Figure, the output current amplitude of VCM-VSI can be calculated as follows:

$$|\vec{I_o}| = \left|\frac{\vec{V_{ref}}}{Z_v + Z_{filter} + Z_{L11} + Z_g}\right| = \left|\frac{|\vec{V_{ref}}|}{|Z_{eq}|}\right| < |\vec{I_o}|_{max} \qquad (3)$$

where, Z_v, Z_{filter}, Z_{L11}, and Z_g are VI, filter impedance, line impedance from DG to ground fault, and ground impedance, respectively. According to (3), the output current can be limited by reducing the reference voltage or increasing the VI. However, applying VI will convey current transient or current harmonics to voltage reference and it exerts disturbance to the grid in the first couple of cycles. In addition, determination of optimum VI for all fault locations and different fault impedances is not easy. Finally, it is necessary to determine an appropriate current threshold for the activation of VI during the fault. On the other hand, the modified secondary control has numerous advantages including simplicity in obtaining optimum value of the secondary voltage value during the faulty condition, robustness against the disturbance in current signal, and fast time response in comparison with VI method.

A. Fault current limiter strategy

According to the traditional secondary control operation, if a current limiting threshold is not applied during the faulty conditions, a high amount of voltage amplitude is added to voltage reference of VCM-VSIs to keep microgrid voltage within an accepted level. This would lead to current considerable increase in the VSI output current. On the other hand, a converter-based DG has to protect itself from being damaged by limiting its output current. In order to have the capability of limiting fault current, this study presents a multifunctional secondary control that has two objectives:

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keeping the voltage amplitude at its nominal value during the normal operation and limiting output current of VCM-VSI to twice its nominal value. In the normal conditions, each voltage and frequency errors is passed through slow PI controllers to generate voltage and frequency compensation references, respectively. As it is shown in Fig. 2, where sf in PI_{sf} is abbreviation of Secondary for Fault, this is val id while the current amplitude is below a definite threshold, $Threshold_a$. However, once the current amplitude is above $Threshold_a$, the objective of secondary control is changed from keeping voltage to its reference to keeping VCM-VSI current to twice its nominal current by reducing voltage reference. In the faulty condition, the amplitude of each phase is calculated by an Adaptive Moving Average Filter-based Phase Locked Loop (AMAF-PLL). As shown in Fig. 3, the single-phase AMAF-PLL utilizes a first-order all pass filter (APF), APF(s)=(ω_g-s)/(ω_g+s), to generate a fictitious orthogonal signal. Although, APF has several benefits such fast dynamic response and low computation burden, it has no harmonic filtering ability. To deal with this issue, a MAF, which has high harmonic filtering, is used to provide a smooth dc signal in d and q frames [10]. The MAF is a rectangular window filter with the windows length of T_ω and can be described in the s-domain as:

$$G_{MAF}(s) = \frac{1 - e^{-T_\omega s}}{T_\omega s} \tag{4}$$

From (4), it can be conceived that a wide window length results in a slow transient response. By substituting s=jω, and performing some mathematical simplification, the magnitude and phase expression of MAF can be written as:

$$G_{MAF}(j\omega) = \left|\frac{\sin(\omega T_\omega/2)}{\omega T_\omega/2}\right| \angle -\omega T_\omega/2 \tag{5}$$

According to (5), in the zero frequency, the MAF gain is unity and for the frequencies equals to n/T_ω, the gain is zero. The characteristics of MAF for two different window lengths are visualized in Fig. 4. As it can be seen, for T_ω=0.01 s, all integer multiples of 100 Hz would be blocked by MAF. When the grid distortion pattern is unknown, it is recommended to consider T_ω=0.02 s to eliminate the dc offset as well as all harmonics. It is reported that the MAF-PLL with T_ω=0.02 s has a slow dynamic response [10]. This would result in delay in operation of the proposed FCL for the first couple of cycles. To address this issue, when the amplitude of current regarding all harmonic is above the $Threshold_b$, this value is considered as current amplitude to improve transient response at the expense of low harmonic filtering. This idea is implemented and visualized in Fig. 3 and 5, respectively. In addition to the AMAV-PLL, a saturation block with the value of 3 p.u. is used to limit the inner current loop reference. This block prevents a large inrush current in the inverter output.

B. Optimization of the proposed FCL

As shown in Figs. 2 and 3, parameters including $Threshold_a$, $Threshold_b$ as well as k_p and k_i of PI_{sf} are unknown.

In order to find the optimum values of unknown parameters, the following optimization problem must be solved:

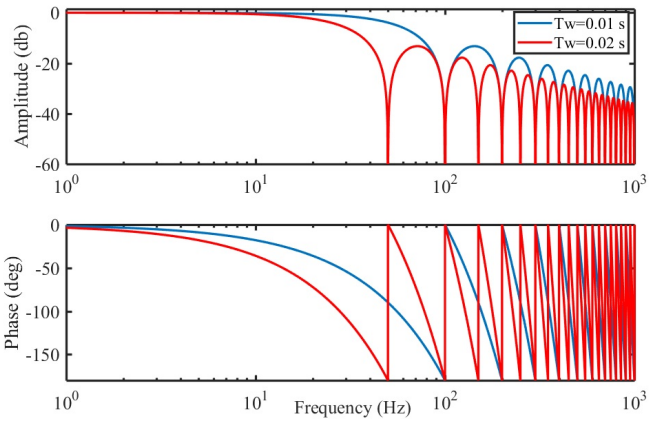

Fig. 4. Bode plot of MAF for T_ω=0.01 s, and T_ω=0.02 s.

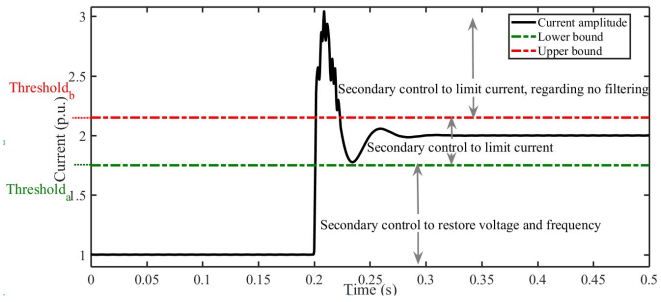

Fig. 5. Behaviour of secondary-control, regarding *Tω=0.02 s*, during the three levels.

$$Minimize: \sum_{i=1}^{N} \left|i_{ref}(i) - \left|i_{one-phase}(i)\right|\right| \Delta T_s$$

$$i_{ref} = \begin{cases} 1\,p.u. & for\ \left|i_{one-phase}(i)\right| < Threshold_a \\ 2\,p.u. & for\ \left|i_{one-phase}(i)\right| > Threshold_a \end{cases}$$

$$Subjected\ to: \begin{cases} 0 \le k_p \le 1000 \\ 0 \le k_i \le 10000 \\ 1.6\,p.u. \le Threshold_a \le 2.2\,p.u. \\ 2.2 \le Threshold_b \end{cases} \tag{6}$$

The lower bound of the $Threshold_a$ is a triggering level for activation of the proposed FLC. This value must be higher than the VCM-VSI current magnitude during the maximum possible loads in the grid. In this letter, 1.6 p.u. is chosen as the minimum value of the $Threshold_a$. The upper bound of the $Threshold_a$, which is equal to the lower bound of $Threshold_b$, triggers acceleration of limiting fault current only for the first couple of cycles by measuring current amplitude regarding all current harmonics. As a result, the maximum value of $Threshold_a$ or the minimum value of the $Threshold_b$ must bechosen in such a way to avoid harmonic effects during the faulty condition. Considering current harmonic of the inverter, 2.2 p.u. is selected for the minimum value of the $Threshold_b$. In this study, optimization problem of (6) is solved by utilizing particle swarm optimization (PSO) algorithm [11]. It must be noted that the optimization procedure must be carried out for the harshest fault condition.

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IV. Real-time Simulation Results

The model of Fig. 1 is implemented in OPAL-RT with sampling time of fixed 20 μs. Other control parameters of VCM can be found in Table I.

In order to investigate the effectiveness of the proposed method, both the VI-based FCL and the proposed FCL are optimized for *scenario 1*. Then, those FCLs are investigated for *scenario 2* and *3*:

TABLE I
System parameters

Type	Parameters		Value
	Symbol	Quantity	
Electrical setup	V_{dc}	DC Voltage	650 V
	V_{MG}	Nominal voltage	311 V
	F	Nominal Frequency	50 Hz
	C	Filter Capacitance	9 μF
	L	Filter Inductance	1.8 mH
	L_o	Output Inductance	1.8 mH
	P_{load1}	Load active power (For real-time system)	2 kW
	R_{load2}, R_{load3}	Linear load impedance (For experimental setup)	230/115 Ω
		Nonlinear load impedance (For real-time system)	46 μF,8.4 mH, and 500 Ω
		Nonlinear load impedance (For experimental setup)	235μF, 0.084 mH, and 115 Ω
	Z_{line1}	Line impedance between constant power load/nonlinear load and inverter (for real-time setup)	1.2 Ω +5.4 mH
	Z_{line2}	Line impedance between Nonlinear load and inverter (for experimental setup)	0.1 Ω +1.8 mH
Inner Loops (VCM)	k_{pV}	Proportional coefficients of voltage	0.05
	k_{rV}	Resonant coefficients of voltage	10
	k_{pI}	Proportional coefficients of current	33
	k_{rI}	Resonant coefficients of current	666
	ω_{cV}	cut-off frequency of voltage loop	2 Hz
	ω_{cI}	cut-off frequency of control loop	2 Hz
Droop Control	k_{pP}	Active power droop term	0.0003
	k_{iP}	Active power droop integral term	0.0015
	k_{pQ}	Reactive power droop term	0.2 VAr/V
Secondary Control	k_{pf}	Frequency proportional term	0.001
	k_{if}	Frequency integral term	1 s^{-1}
	k_{pE}	Voltage proportional term	0.001
	k_{iE}	Voltage integral term	0.5 s^{-1}

- *Scenario 1*: A three-phase ground fault with R_f=0.1 Ω. at the PCC. In this scenario a constant power load with 2 kW is connected to the VSI through a line with Z_{line1}=1.2 Ω +5.4 mH.
- *Scenario 2*: A three-phase ground with R_f=1 Ω and the load same as Scenario 1.
- *Scenario 3*: A three phase ground fault with R_f=1 Ω. In this scenario. In this scenario a nonlinear load including three-phase diode rectifier, inductor with 46 μF, 8.4 mH, and resistance equaled to 500 Ω is connected to the VSI through a line with Z_{line1}=1.2 Ω +5.4 mH.

Regarding the proposed method, (6) is solved for *scenario1* and the best parameters are obtained by PSO algorithm: $Threshold_a$=1.6 p.u., $Threshold_b$= 2.236 p.u., k_p= 78.19, and k_i= 5000. Similarly, the optimum values of VI for *scenario 1* is Z_{VI}=24.1-j0.991.

As it can be seen in Fig. 6(a) and (b), *scenario* 1 is applied at 0.1s and the voltage and current of the VSI are deviated from their nominal values to 0.2804 p.u. and 5.22 p.u, respectively. According to Fig. 6 (c) and (d), the VI-based FCL applies optimal value to limit the fault after 60 ms. However, for both *scenario 2* and *scenario 3*, the VI-FCL has no ability to limit the output current (see Fig. 6 (e) and (f)). As it can be seen, for these two *scenarios*, the VI fluctuates between zero and its optimum value. This process continues until the fault is isolated.

In the proposed approach, thanks to optimum values of $Threshold_a$ and $Threshold_b$, the tuned PI controller adds proper additional negative values to voltage reference to limit the fault current to twice its nominal current in steady state for all considered *Scenarios* in around 40 ms (see Fig. 7(a),(b),(c)). The saturation block applied at the generated current reference will limit the first peak of fault current to 3.0 p.u.. Because of this saturation block, the VSI will not experience transient inrush current, and it would be safe against any harsh condition. In addition, *the proper value of* $threshold_b$ helps limiting fault current to its predifined value in the shortest possible time. Similarly for the *Scenario 2 and 3*, the proposed FCL confines the inverter current to twice its nominal value in 45 ms (See Fig. 7 (b) and (c)). It must be noted that since the proposed FCL is tuned for the worst condition, *Scenario 1* (see Fig.7 (f)), the proposed FCL will not cause any instability problem for other higher fault impedances.

V. Experimental Results

To further support the effectiveness of the proposed method, some experimental results are presented in this section. The experimental setup is shown in Fig. 8. The setup consists of a Danfoss inverter (2.2-kW inverter with an LCL filter), dSPACE1006 for control and monitoring, two resistive loads, and a nonlinear load.

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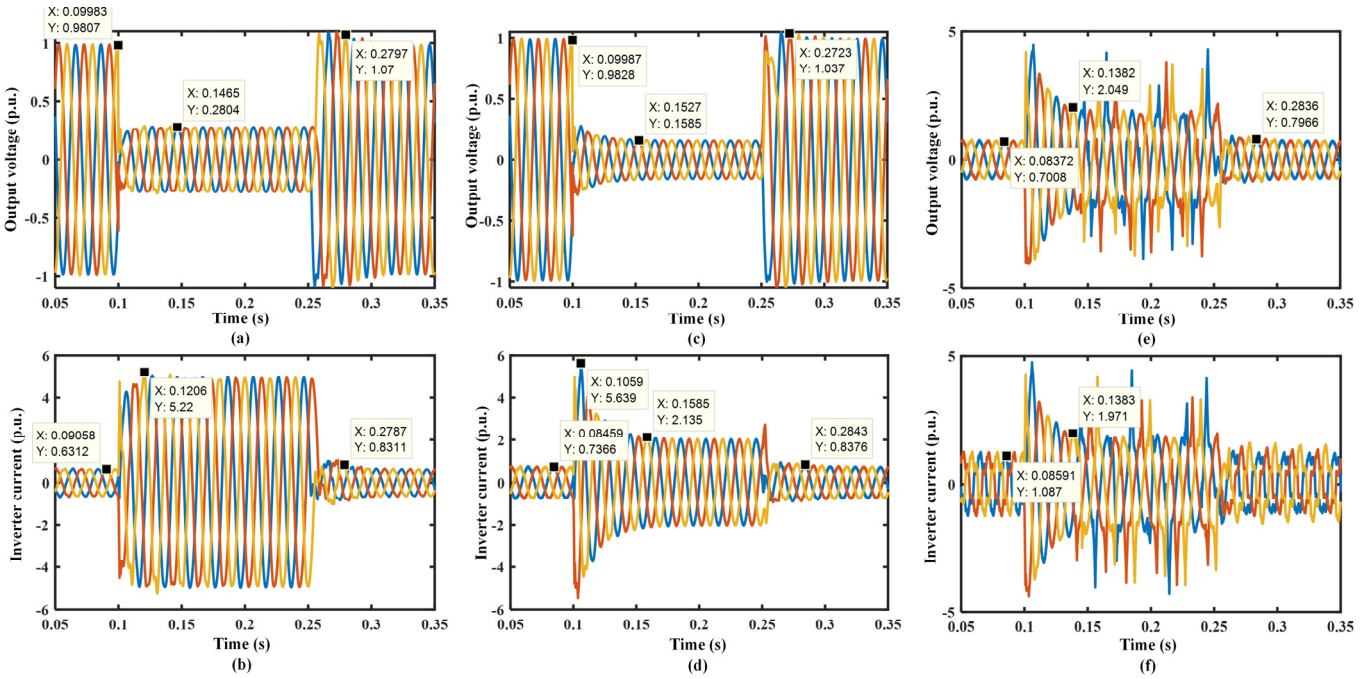

Fig. 6. VCM-VSI performance under VI-based FCL: (a) V_{out} without applying FCL, (b) $I_{inverter}$ without applying FCL, (c) V_{out} for *scenario 1* (d) $I_{inverter}$ for *scenarios 1*; (e) $I_{inverter}$ for *scenarios 2*; (f) $I_{inverter}$ for *scenarios 3*.

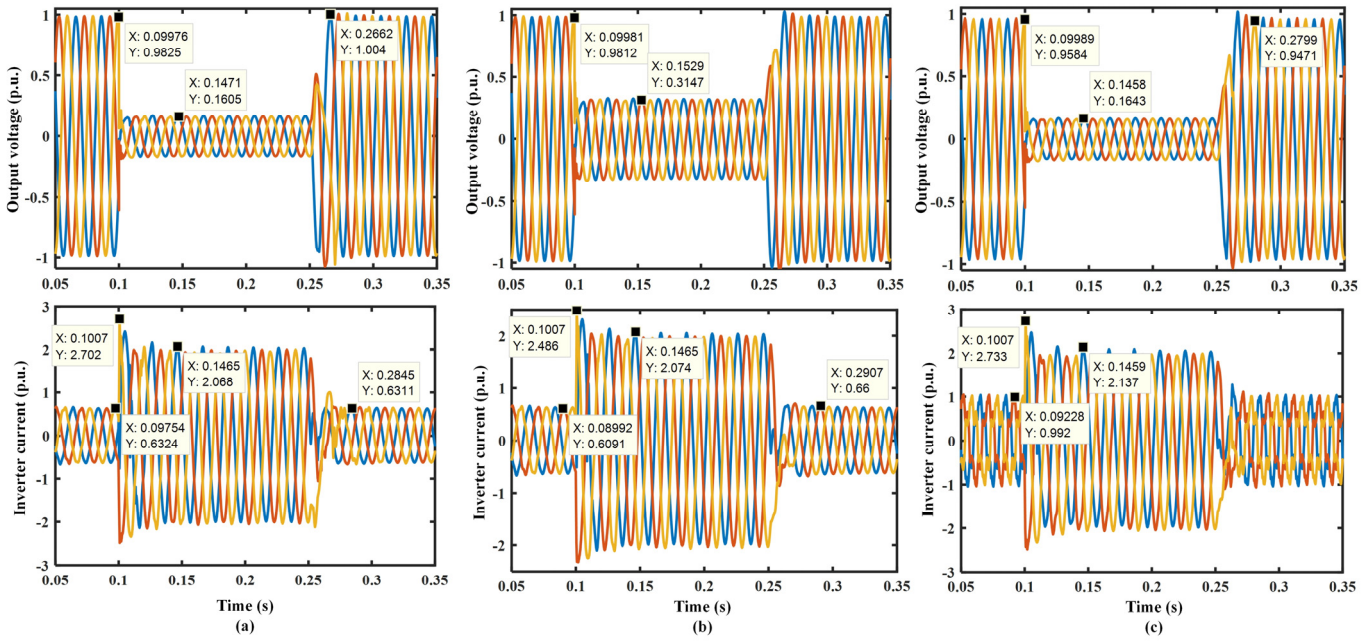

Fig. 7. VCM-VSI performance under the preposed FCL: (a) *Scenario 1* (b) *Scenario 2*, (c) *Scenario 3.*

The setup specifications are presented in Table I. Due to experimental limitations, instead of the fault scenarios, two overcurrent scenarios are emulated.

- *Scenario 1:* First, the inverter is connected to a load with R_{load2}=230 Ω. Then a load with R_{load3}=115 Ω is connected to the inverter.
- *Scenario 2:* First, the inverter is directly connected to the load with R_{load2}=230 Ω, then nonlinear load including three-phase diode rectifier, a capacitor with 235μF, an inductor with 0.084 mH, and a resistance equaled to 115 Ω is added to the inverter through a line with Z_{line2}=0.1 Ω +1.8 mH.

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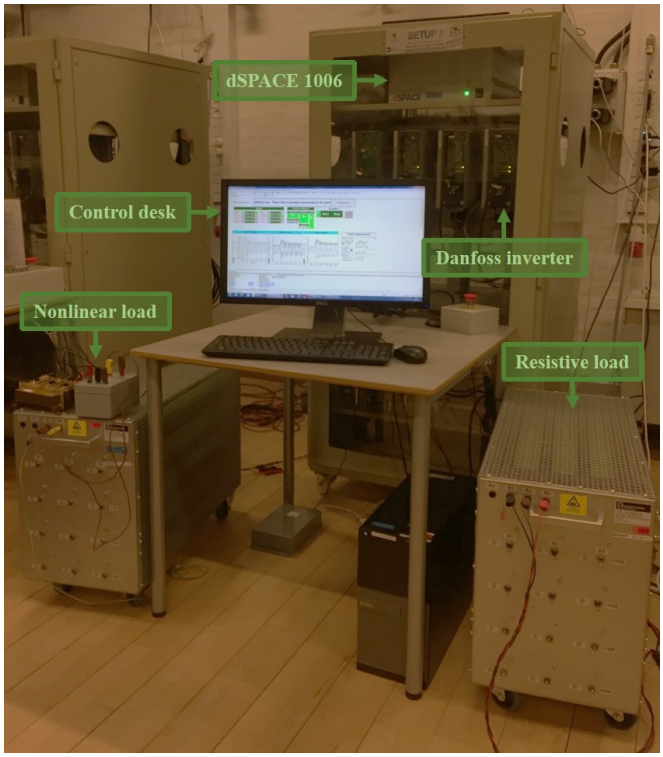

Fig. 8. Experimental setup.

These two scenarios result in overcurrent around 6 p.u., which are shown in Fig. 9 (a) and 10 (a). In the first scenario, while the amplitude of the inverter current exceeds the $Threshold_a$, the proposed FCL starts to operate. As it can be seen in Fig. 9 (b), thanks to the saturation block, the first peak current of the inverter is fixed to 3 p.u. As a result, the inverter is kept safe from being damaged by transient inrush current. In addition, the inverter current approaches 2 p.u. in around 50 ms. Fig. 10 (b) shows the voltage and current of inverter for the second scenario where the inverter current has harmonics. As can be seen in this figure, the proposed FCL is kept safe from being damaged by limiting transient inrush current to 3 p.u. In addition, the inverter current approaches 2 p.u. in around 50 ms. These experimental results demonstrate that the proposed method is quite robust to the harmonics caused by the nonlinear loads.

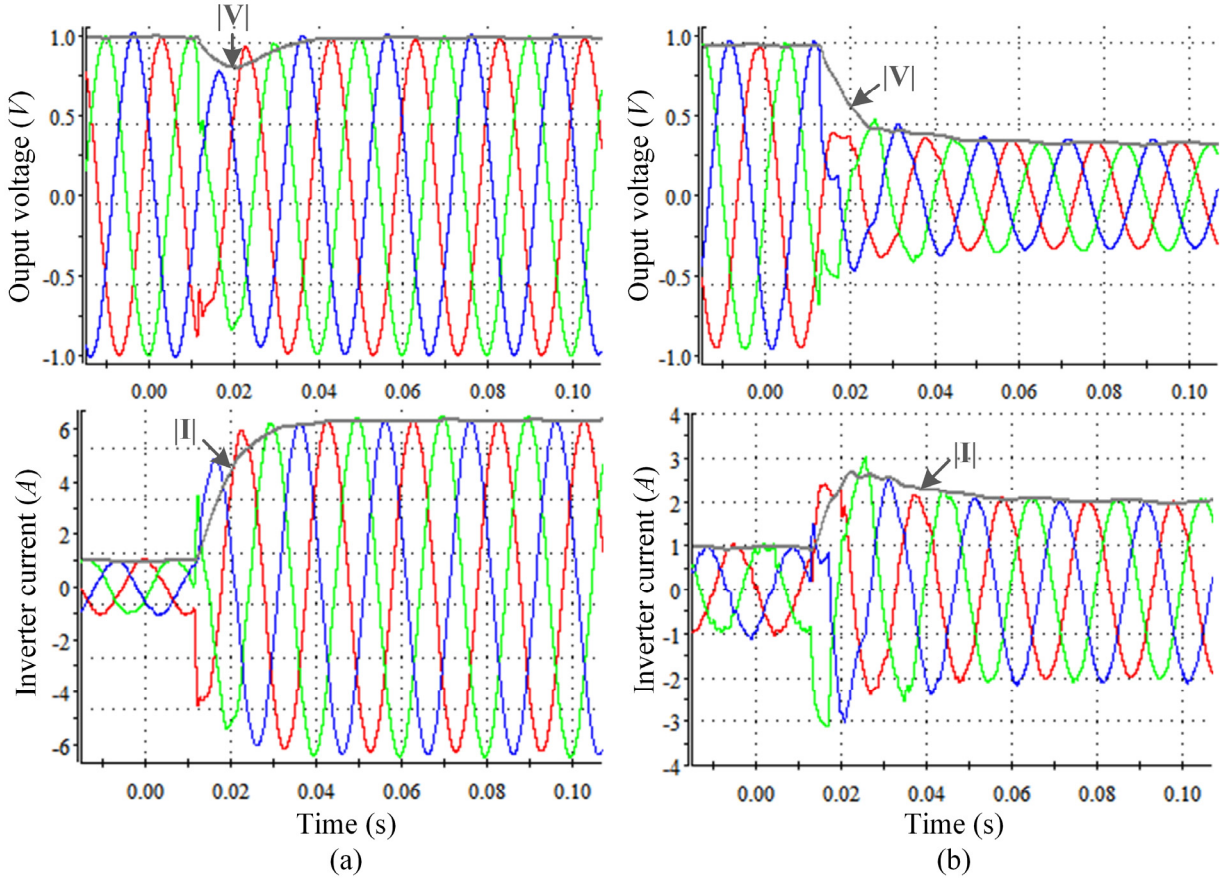

Fig. 9. Inverter performance with/without applying the proposed FCL for scenario 1: (a) *Without the proposed FCL*, (b) *Using the proposed FCL*.

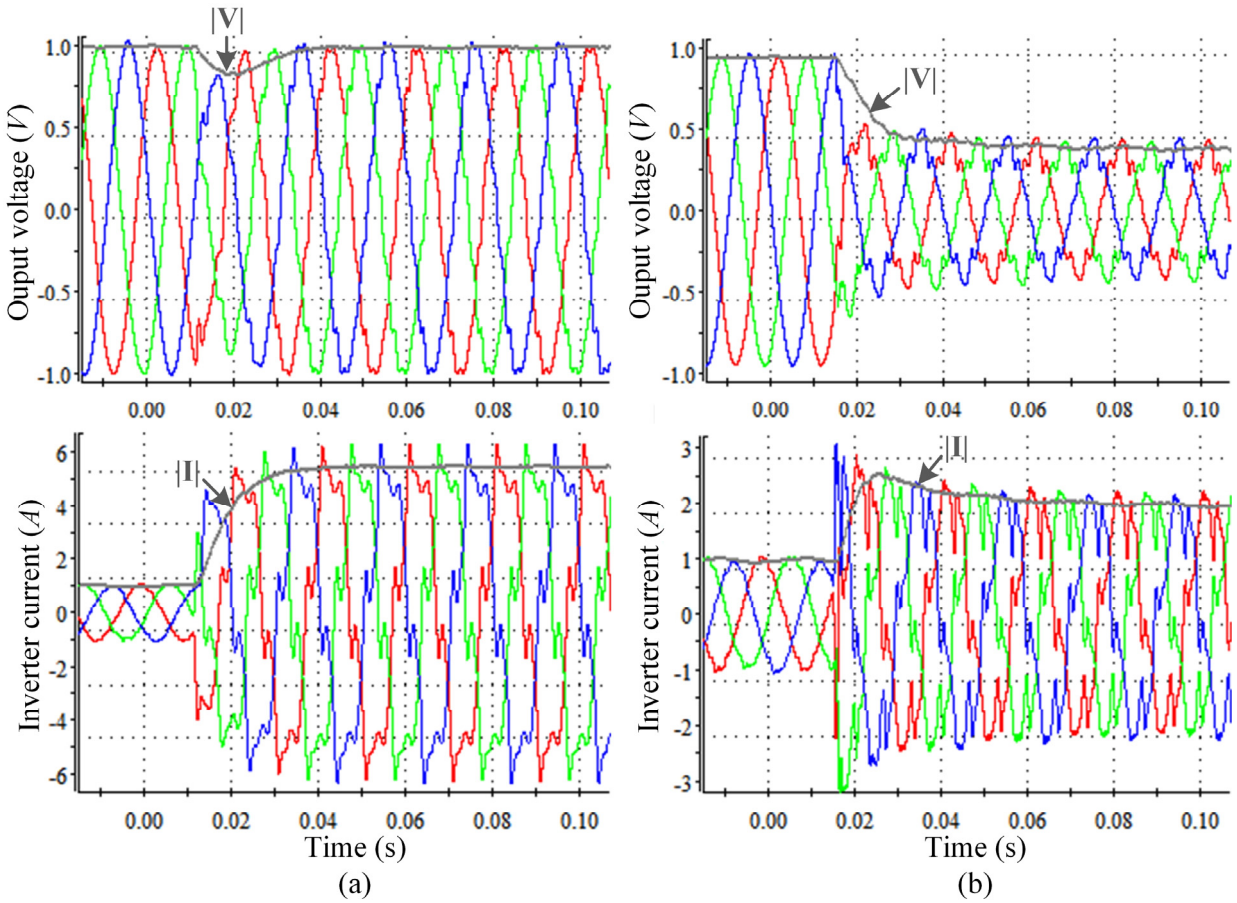

Fig. 10. Inverter performance with/without applying the proposed FCL for scenario 2: (a) Without the proposed FCL, (b) Using the proposed FCL.

VI. Conclusion

This paper proposes a modified secondary control with two objectives of keeping voltage and frequency to their nominal. values in the normal conditions as well as limiting the fault current in faulty conditions. To evaluate the efficiency of the proposed method, two different values of fault impedances as well as connecting the nonlinear load are considered. It is shown that the VI-FCL method [6] could lose ability to limit current in some cases. However, the modified secondary control is stable through the worst possible conditions and can limit current of the VCM-VSI in less than 50 ms.. Finally, the performance of the proposed FCL is validated by experimental results in two different conditions.

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