Modeling, Analyzing, and Designing Advanced Synchronization Techniques for Power Converters

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MODELING, ANALYZING, AND DESIGNING ADVANCED SYNCHRONIZATION TECHNIQUES FOR POWER CONVERTERS

BY
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PH.D. DISSERTATION

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He is currently working towards the Ph.D. degree in the Department of Energy Technology, Aalborg University, Denmark. His research interests include phase-locked loop and nonlinear filtering techniques for power engineering applications and control of power converters.

ENGLISH SUMMARY

Synchronization, in simple words, can be defined as the procedure of coordinating a generator (here, a power converter with its DC source) and the main grid so that they are able to effectively work in parallel. This procedure involves extracting the grid voltage parameters (i.e., phase, frequency, and amplitude). This task is often carried out using phase-locked loops (PLLs) and frequency-locked loops (FLLs), which are closed-loop synchronization techniques, or in an open-loop manner using different filtering techniques.

The main challenge that all synchronization techniques regardless of their nature are facing with is growing power quality issues (i.e., the presence of harmonics, DC offset, imbalance, voltage sag and swell, etc.) in the grid voltage. These disturbances, which are mainly attributable to the high penetration of distributed generation systems and nonlinear power electronics-based loads in the distribution system, adversely affect the performance of synchronization technique. To deal with this challenge, some research efforts have been made in the literature. The main objective of this dissertation is to provide an analysis of these efforts and make further contributions to the field by designing more advanced synchronization techniques. These contributions cover the major categories of synchronization techniques, i.e., PLLs, FLLs, and open-loop techniques, as explained below.

The main contributions to the PLL field are as follows. First, the small-signal modeling of a large number of advanced single-phase and three-phase PLLs is conducted. These models make the stability assessment, performance analysis, and tuning the control parameters of these PLLs straightforward and effective. Second, some advanced PLLs are designed. Roughly speaking, these PLLs improve the speed/accuracy tradeoff of the state-of-the-art PLLs while maintaining simplicity.

Regarding FLLs, the following contributions are made in this thesis. First, it is demonstrated how the small-signal modeling of typical and advanced single-phase and three-phase FLLs should be conducted. Thanks to these models, the FLLs tuning and stability analysis can now be easily and effectively carried out. Second, a performance comparison among some advanced FLLs is conducted to better understand their properties. Third, the concept of inloop filter for designing more effective FLLs is introduced. Fourth, it is proved that FLLs are mathematically equivalent to PLLs. It means that FLLs and PLL are practically the same control systems that are implemented in different reference frames. Finally, through establishing a resemblance between the average model of a single-phase grid-connected converter with a proportional-resonant (PR) current controller and a typical single-phase FLL, it is demonstrated that the frequency estimation capability can be easily added to the resonant term of the PR controller. In this way, the need

for a separate synchronization unit (like a PLL) is removed, which leads to a simpler and more compact structure.

Some contributions to open-loop synchronization (OLS) techniques are also made in this dissertation. First, a true OLS technique for three-phase systems is designed, which does not use any feedback in its structure and works effectively under frequency drifts without requiring any knowledge of the grid frequency. This synchronization technique benefits from a low computational burden and offers a fast dynamic response and a high customizability to deal with different grid scenarios. Second, a moving average filter-based OLS technique for single-phase applications is designed. This synchronization method offers interesting advantages such as the zero average phase/frequency/amplitude error under nominal/off-nominal frequencies, a complete DC offset rejection ability, a complete (effective) filtering of the grid voltage harmonics under a nominal (off-nominal) frequency, and a fast dynamic response.

Keywords: Amplitude extraction, filters, frequency estimation, frequency-locked loops, grid-connected converters, grid voltage imbalance, harmonic distortion, open-loop techniques, phase detection, phase-locked loops, power electronics, quadrature signal, single-phase systems, synchronization, three-phase systems.

DANSK RESUME

Synkronisering, i enkle ord, kan defineres som proceduren for at koordinere en generator (her en power converter med dens DC-kilde) og el-nettet, så de effektivt kan arbejde parallelt. Denne fremgangsmåde involverer ekstraktion af spændingsparametrene (dvs. fase, frekvens og amplitude). Denne opgave udføres ofte ved hjælp af faselåste sløjfer (Phase Lock Loop - PLL) og frekvenslåsede sløjfer (Frequency Lock Loop - FLL), som er synkroniseringsteknikker med closed-loop eller på en open-loop måde ved anvendelse af forskellige filtreringsteknikker.

Den største udfordring, at alle synkroniseringsteknikker uanset deres natur står overfor, er ved at voksende problemer med strømkvaliteten (dvs. harmoniske komponenter, DC-offset, ubalance, svingende spænding osv.) i net spændingen. Disse forstyrrelser, som hovedsageligt kan henføres til den høje penetration af distribuerede generationssystemer og ikke-lineære strømelektronikbaserede belastninger i distributionssystemet, påvirker synkroniserings-teknologiens ydeevne negativt. For at klare denne udfordring er der gjort nogle forskningsindsatser i litteraturen. Hovedformålet med denne afhandling er at levere en analyse af disse indsatser og yde yderligere bidrag til feltet ved at designe mere avancerede synkroniseringsteknikker. Disse bidrag dækker alle kategorier af synkroniseringsteknikker, dvs. PLL'er, FLL'er og open-loop teknikker, som forklaret nedenfor.

De vigtigste bidrag til PLL-feltet er som følger. For det første udføres små signalmodellering af et stort antal avancerede enfasede og trefasede PLL'er. Disse modeller gør stabilitetsvurderingen, præstationsanalysen og justering af kontrolparametrene for disse PLL'er ligetil og effektiv. For det andet er nogle avancerede PLL'er også designet. Tilnærmelsesvis forbedrer disse PLL'er hastigheden / nøjagtigheden af de state-of-the-art PLL'er, samtidig med at der opretholdes enkelhed.

Med hensyn til FLL'er, er følgende bidrag lavet i denne afhandling. For det første er det demonstreret, hvordan små signalmodellering af typiske og avancerede enfase- og trefasede FLL'er skal udføres. Takket være disse modeller kan FLLs tuning og stabilitetsanalyse nu nemt og effektivt udføres. For det andet udføres en sammenligning blandt nogle avancerede FLL'er for at bedre forstå deres egenskaber. For det tredje indføres begrebet "in-loop filter" til design af mere effektive FLL'er. For det fjerde er det bevist, at FLL'er er matematisk ækvivalente med PLL'er. Det betyder, at FLL og PLL er praktisk de samme styresystemer, der implementeres i forskellige referencerammer. Endelig er det demonstreret at den gennemsnitlige model af en enkeltfaset nettilsluttet frekvensomformer med en "proportionel resonant" (PR) strømstyring og en typisk enfaset FLL, at frekvensberegningsevnen let kan tilføjes til PR-regulatorens resonante del. På denne måde fjernes behovet for

en separat synkroniseringsenhed (som en PLL), hvilket fører til et enkelt og mere kompakt struktur.

Nogle bidrag til open-loop synkronisering (OLS) teknikker er også lavet i denne afhandling. For det første er der udviklet en ægte OLS-teknik til trefasesystemer, som ikke bruger nogen feedback i sin struktur og fungerer effektivt under frekvensdrift uden at kræve kendskab til netfrekvensen. Denne synkroniseringsteknik har fordele ved en lav beregningsbyrde og giver et hurtigt dynamisk respons og en høj tilpassbarhed til at håndtere forskellige gridscenarier. For det andet er der udviklet en bevægende gennemsnitlig filterbaseret OLS-teknik til enkeltfaseprogrammer. Denne synkroniseringsmetode giver spændende fordele, såsom nul-middelfase / frekvens / amplitudefejl under nominelle / off-nominelle frekvenser, en komplet DC-offset afvisningsevne, en fuldstændig (effektiv) filtrering af harmoniske komponenter under en nominel (off-nominel) frekvens og et hurtigt dynamisk respons.

Nøgleord: Amplitude-ekstraktion, filtre, frekvens estimation, frekvenslåsede sløjfer, netforbundne omformere, nettospændingsbalance, harmonisk forvrængning, åbenløbsteknikker, faseopdagelse, faselåste sløjfer, strømelektronik, kvadratur signal, enkeltfasesystemer, synkronisering, trefasesystemer.

THESIS DETAIL AND PUBLICATIONS

Thesis Title: Modeling, Analyzing, and Designing Advanced Synchronization Techniques for Power Converters

Ph.D. Student: Saeed Golestan

Supervisor: Prof. Josep M. Guerrero, Aalborg University

Co-supervisor: Associate Prof. Juan C. Vasquez, Aalborg University

Publications

- S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1894-1907, Mar. 2017.
- S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: A review of recent advances," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9013-9030, Dec. 2017.
- S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, J. Doval-Gandoy, and F. D. Freijedo, "Small-signal modeling, stability analysis and design optimization of single-phase delay-based PLLs," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3517-3527, May 2016.
- S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki "Research on variable-length transfer delay and delayed signal cancellation based PLLs," *IEEE Transactions on Power Electronics*, (accepted for the publication).
- S. Golestan, J. M. Guerrero, A. M. Abusorrah, M. M. Al-Hindawi, and Y. Al-Turki "An adaptive quadrature signal generation based single-phase phase-locked loop for grid-connected applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2848-2854, Apr. 2017.
- S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Steady-state linear Kalman filter-based PLLs: A second look", *IEEE Transactions on Industrial Electronics*, (accepted for the publication).
- S. Golestan, J. M. Guerrero, and J. C. Vasquez, "DC-offset rejection in phase-locked loops: A novel approach," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4942-4946, Aug. 2016.
- S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, and J. Doval-Gandoy, "PLL with MAF based prefiltering stage: Small-signal modeling and performance enhancement," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4013- 4019, Jun. 2016.

- S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki "Modeling, tuning, and performance comparison of advanced second-order generalized integrator-based FLLs", *IEEE Transactions on Power Electronics*, (accepted for the publication).
- S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki "A study on three-phase FLLs," *IEEE Transactions on Power Electronics*, (under review).
- S. Golestan, E. Ebrahimzadeh, J. M. Guerrero, and J. C. Vasquez, "An adaptive resonant regulator for single-phase grid-tied VSCs," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1867-1873, Mar. 2018.
- S. Golestan, J. M. Guerrero, and J. C. Vasquez, "An open-loop grid synchronization approach for single-phase applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5548-5555, July 2018.
- S. Golestan, A. Vidal, A. G. Yepes, J. M. Guerrero, J. C. Vasquez, and J. Doval-Gandoy, "A true open-loop synchronization technique," *IEEE Transactions on Industrial Informatics*, vol. 12, no. 3, pp. 1093-1103, Jun. 2016.

This present report combined with the above listed scientific papers has been submitted for assessment in partial fulfillment of the Ph.D. degree. The thesis is based on the submitted or published scientific papers which are listed above. Parts of the papers are used directly or indirectly in the extended summary of the thesis. The scientific papers are not included in this version due to copyright issues. Detailed publication information is provided above and the interested reader is referred to the original published papers. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty of Engineering and Science, Aalborg University

PREFACE

This thesis, which is a collection of papers and submitted as a partial fulfillment of the requirements for the Danish Ph.D. degree, has been conducted under the supervision of Prof. Josep M. Guerrero and Prof. Juan. C. Vasquez at the Department of Energy Technology, Aalborg University.

I would like to express my gratitude to my advisor and co-advisor, Prof. Josep M. Guerrero and Prof. Juan. C. Vasquez, for their support and friendship during the course of this work. I would also like to thank my family for their encouragement, support, and patience.

TABLE OF CONTENTS

CHAPTER 1. INTRODUCTION

1.1. BACKGROUND AND MOTIVATION

In recent years, with growing awareness regarding the environmental damages of the generation of electrical energy using fossil fuels, which around 80% of the world electrical energy generation is based on them [1], raising energy demand, and technological advances in power electronics and digital signal processors, producing the electrical energy using renewable sources, particularly photovoltaic and wind, has received a considerable attention. This fact can be supported by the energy road-maps planned by industrial and developing countries. For example, according to Denmark's roadmap, this country should produce around 50% of its electrical energy needs using wind energy by the year 2025 [2].

The renewable energy-based generation systems often need an interface for connecting to the main grid and/or local loads because their output voltage may be a DC or a variable-frequency (or high-frequency) AC signal. This interface is often a power electronic converter and is responsible for extracting the highest possible power from the renewable energy source and deliver a high-quality power to the grid and/or local loads [3]. These converters may have different topologies depending on the application in hand and performance requirements. The most popular option is probably a pulse-width modulated voltage source converter (VSC).

A highly important unit in the control of power converters is the synchronization part. This unit is responsible to perform a series of action so that the power converter and the main grid are able to safely and effectively work in parallel [4]-[6]. The information provided by the synchronization unit may also be used for different monitoring and protection purposes, such as islanding detection [7]-[8], fault detection [9], [10], etc.

The synchronization techniques in power converters may be broadly categorized into open-loop and closed-loop approaches [11], [12]. The closed-loop synchronization (CLS) methods are those approaches whose implementation involve feeding back one or more signals. The frequency-locked loops (FLLs) and phase-locked loops (PLLs) are two main categories of the CLS techniques. The open-loop synchronization (OLS) methods, nevertheless, are free from any feedback signals in their structures. The diagram illustrated in Fig. 1.1 illustrates this classification of synchronization techniques. These synchronization techniques will be discussed in more details later.

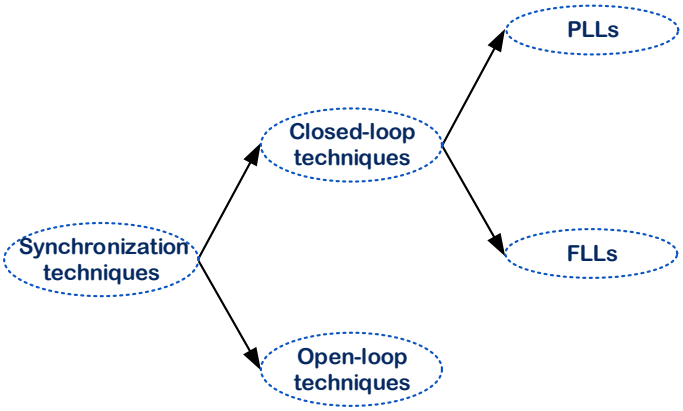

Fig. 1.1: A classification of synchronization techniques.

Roughly speaking, all synchronization techniques, regardless of their structural differences, work satisfactorily under an ideal condition, in which the grid voltage is free from any noise. This situation, however, almost never happens in practice because of ever-increasing power quality issues (i.e., the presence of harmonics, interharmonics, DC offset, asymmetrical voltage sags, etc.) in the power systems [13]. These power quality problems may be caused by different factors. For example, the DC component may appear in the grid voltage signal because of power system faults, geomagnetic phenomena, half-wave rectification, cycloconverters, and the direct current injection by distributed generation systems, particularly PV inverters, into the grid [14]-[17]. And the grid voltage harmonics and interharmonics are mainly attributable to the nonlinear loads, particularly power electronics-based equipment, which their penetration in the power system is continuously increasing [18]-[20].

The power quality issues adversely affect the performance of synchronization techniques. To be more exact, they cause oscillatory and offset errors in the estimated quantities (phase, frequency, and amplitude) by the synchronization units [5], [6], [21], [22]. To deal with this problem, some efforts for designing more efficient synchronization methods have been made recently. Roughly speaking, these efforts often result in complicated structures that suffer from one or more of the following shortcomings: 1) high computational burden, 2) implementation complexity, 3) difficulty of modeling and stability analysis, 4) inefficiency under large frequency drifts. In what follows, this fact is discussed with more details for different categories of synchronization techniques. Before that, a general description of these categories is presented.

1.1.1. PHASE-LOCKED LOOPS (PLLS)

Focusing on power and energy applications, a PLL is a feedback control system with a nonlinear nature that is implemented in the synchronous reference frame and synchronizes its output signal with the fundamental component of the grid voltage, which is its input signal [5], [6]. In addition to synchronizing power converters, PLLs are widely employed for different applications such as islanding detection [7]-[8], fault detection [9]-[10], measurement of synchrophasors [23], [24], harmonics extraction [25], [26], computation of power quality factors [27], [28], etc.

Regardless of the application in hand, three parts are found in almost all PLLs [5], [6], [29], [30]. These elements are the phase detector (PD), which is mainly responsible for generating a signal containing the phase error information, the loop filter (LF), also known as the loop controller, which drives the phase error signal to zero, and voltage-controlled oscillator (VCO), which produces a synchronized unit vector in its output [5], [6], [29], [30].

1.1.1.1 Three-phase PLLs

1.1.1.1.1 Standard Three-phase PLL

Fig. 1.2 illustrates a standard three-phase PLL, which is called the conventional SRF-PLL [5], [21], [22]. As the conventional SRF-PLL is the basic structure for implementing almost all advanced PLLs, a brief description of its operating principle and properties is first presented.

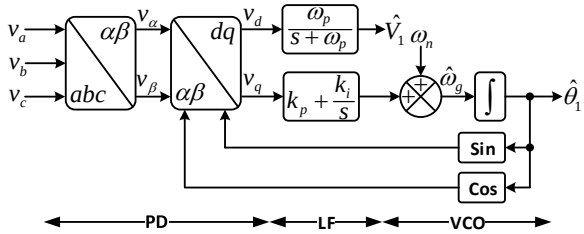

Fig. 1.2: Conventional SRF-PLL.

In the conventional SRF-PLL, Clarke's and Park's transformations are applied to the grid voltage signals for transferring them to the synchronous (*dq*) reference frame. The resultant *dq*-axis signals contain the phase error and amplitude information. The signal containing the phase error, here v_q, is passed through the LF, which is a proportional-integral (PI) regulator. The cooperation of this regulator and the VCO guarantees a zero average phase tracking error in the nominal and off-nominal frequencies in the steady state. Notice that the unit vector generated by the VCO [i.e., $\sin(\hat{\theta})$ and $\cos(\hat{\theta})$] is used by the PD (the Park's transformation) for generating

the phase error and amplitude information. Notice also that the PI controller output and the *d*-axis signals are estimations of the grid voltage frequency and amplitude, respectively. The *d*-axis signal is fed to a low-pass filter (LPF) to reject/attenuate possible noise/disturbances and accurately estimate the grid voltage amplitude.

Assume that the three-phase input voltages of the SRF-PLL are as follows

$$\begin{aligned} v_a(\mathrm{t}) &= \mathrm{V}_1\cos(\theta_1) + \sum_{\substack{h=-\infty \\ h\neq 1}}^{+\infty} \mathrm{V}_h\cos(\theta_h) \\ v_b(\mathrm{t}) &= \mathrm{V}_1\cos(\theta_1 - 2\pi/3) + \sum_{\substack{h=-\infty \\ h\neq 1}}^{+\infty} \mathrm{V}_h\cos(\theta_h - 2\pi/3) \\ v_c(\mathrm{t}) &= \mathrm{V}_1\cos(\theta_1 + 2\pi/3) + \sum_{\substack{h=-\infty \\ h\neq 1}}^{+\infty} \mathrm{V}_h\cos(\theta_h + 2\pi/3) \end{aligned} \tag{1.1}$$

where V_h is the amplitude of *h*-order harmonic component in the PLL input and θ_h is its phase angle. In this case, the *dq*-axis signals can be expressed as

$$\begin{aligned} v_d(\mathrm{t}) &= \mathrm{V}_1\overbrace{\cos(\theta_1 - \hat{\theta}_1)}^{\approx 1} + \overbrace{\sum_{\substack{h=-\infty \\ h\neq 1}}^{+\infty} \mathrm{V}_h\cos(\theta_h - \hat{\theta}_1)}^{D_d(\mathrm{t})} \approx \mathrm{V}_1 + D_d(\mathrm{t}) \\ v_q(\mathrm{t}) &= \mathrm{V}_1\underbrace{\sin(\theta_1 - \hat{\theta}_1)}_{\approx(\theta_1 - \hat{\theta}_1)} + \underbrace{\sum_{\substack{h=-\infty \\ h\neq 1}}^{+\infty} \mathrm{V}_h\sin(\theta_h - \hat{\theta}_1)}_{D_q(\mathrm{t})} \approx \mathrm{V}_1(\theta_1 - \hat{\theta}_1) + D_q(\mathrm{t}). \end{aligned} \tag{1.2}$$

Using (1.2) and the block diagram of the SRF-PLL (see Fig. 1.2) and by defining $\hat{\theta}_1 = \theta_n + \Delta\hat{\theta}_1$, $\theta_1 = \theta_n + \Delta\theta_1$, $\hat{\omega}_g = \omega_n + \Delta\hat{\omega}_g$, $\omega_g = \omega_n + \Delta\omega_g$, $\hat{V}_1 = V_n + \Delta\hat{V}_1$, and $V_1 = V_n + \Delta V_1$ ($\theta_n = \int \omega_n dt$, ω_n and V_n are the nominal angular frequency and amplitude, respectively, and Δ refers to a small perturbation), the SRF-PLL linearized model can be developed as depicted in Fig. 1.3.

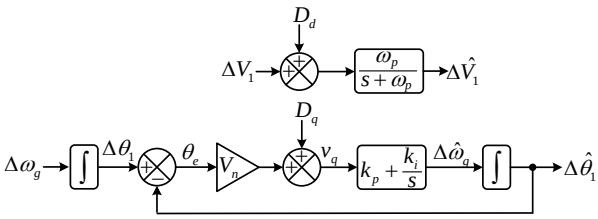

Fig. 1.3: SRF-PLL linearized model.

According to this model, the SRF-PLL open-loop and closed-loop transfer functions may be determined as follows

$$\Delta\hat{\theta}_1(s) = \frac{V_n(k_p s + k_i)}{s^2}\theta_e(s) \tag{1.3}$$

$$\Delta\hat{\theta}_1(s) = \frac{V_n(k_p s + k_i)}{s^2 + V_n k_p s + V_n k_i}\Delta\theta_1(s) + \frac{(k_p s + k_i)}{s^2 + V_n k_p s + V_n k_i}D_q(s). \tag{1.4}$$

$$\Delta\hat{\omega}_g(s) = \frac{V_n(k_p s + k_i)}{s^2 + V_n k_p s + V_n k_i}\Delta\omega_g(s) + \frac{s(k_p s + k_i)}{s^2 + V_n k_p s + V_n k_i}D_q(s). \tag{1.5}$$

$$\Delta\hat{V}_1(s) = \frac{\omega_p}{s + \omega_p}\Delta V_1(s) + \frac{\omega_p}{s + \omega_p}D_d(s). \tag{1.6}$$

Notice that in determining the open-loop transfer function (1.3), the presence of the disturbance input D_q has been neglected.

The transfer functions (1.3)-(1.6) provide valuable information about the SRF-PLL characteristics, which is summarized as follows [5].

- According to (1.3), the open-loop transfer function, which relates the phase error signal to the estimated phase angle, has two poles at the origin. It means that, from the phase angle estimation point of view, the SRF-PLL is a control system of type II [5], [21]. Consequently, it can follow a phase jump and a phase ramp (which corresponds to a frequency jump) with a zero error in the steady state. It, nevertheless, may not be able to follow a parabolic phase input (which corresponds to a frequency ramping change) with a zero error. The phase error during the frequency ramping change can be reduced by increasing the PLL bandwidth. It, nevertheless, degrades the SRF-PLL noise immunity.
- According to (1.3), the SRF-PLL loop gain depends on the grid voltage amplitude. Consequently, any change in the amplitude of the grid voltage (for example, because of a fault), changes the SRF-PLL loop gain and, hence, its dynamic and stability characteristics [5], [31], [32].
- According to (1.4)-(1.6), the phase angle, frequency, and amplitude estimated by the SRF-PLL suffer from the disturbance inputs D_q and D_d. These signals, as expressed in (1.2), are resulting from the grid voltage disturbances. Notice that the grid voltage DC offset and fundamental-frequency negative sequence (FFNS) component appear as the fundamental-frequency and double-frequency components in D_q and D_d, respectively, and a harmonic of order h appears as a harmonic of order

$h-1$. Therefore, the presence of the DC offset, FFNS component, and an *h*-order harmonic component in the SRF-PLL input, respectively, cause the fundamental-frequency, double-frequency, and $h-1$-order harmonic frequency ripples on the estimated phase, frequency, and amplitude.

- The SRF-PLL has a very limited capability to mitigate the grid voltage disturbances. This is particularly true when the DC offset and FFNS component exist in the SRF-PLL input because, as mentioned before, they appear as fundamental-frequency and double-frequency disturbances inside the SRF-PLL control loop. Notice that these are low-order disturbances and even a narrow-bandwidth SRF-PLL cannot effectively mitigate them. Notice also that narrowing the SRF-PLL bandwidth significantly degrades its dynamic response.

These drawbacks and shortcomings of the SRF-PLL have been the main motivation behind recent efforts for designing more efficient PLLs in three-phase applications [5]. In what follows, these efforts are very briefly analyzed.

1.1.1.1.2 Three-phase PLLs with Frequency Ramp Tracking Capability

As mentioned before, the inability in tracking frequency ramps with a zero phase error in the steady-state is a drawback of the conventional SRF-PLL. This may be a serious problem in some applications, such as the synchrophasor measurement [23], speed control of electrical motors [33], synchronization and control of converters in more electric aircraft [34], etc. To tackle this issue, a type-III PLL may be used. The type-III PLLs can be implemented in several ways [5]. A simple approach is replacing the PI controller in the conventional SRF-PLL by the following controller [35]

$$LF(\mathrm{s}) = k_1 + \frac{k_2}{s} + \frac{k_3}{s^2} \tag{1.7}$$

in which k_1, k_2, and k_3 are the control parameters. Using this controller causes three open-loop poles at the phase open-loop transfer function of the PLL and, therefore, ensures a zero phase error in response to frequency ramps. The problem is that using (1.7) as the SRF-PLL LF results in a negative gain margin in dB, which may cause instability when the loop gain reduces [35]. This situation may happen under voltage sags and faults. Notice that the PLL loop gain depends on the amplitude of the grid voltage fundamental component, which drops under voltage sags and faults.

An alternative approach is using the steady-state linear Kalman filter-based PLL (SSLKF-PLL) [8], [34]. In this PLL, a three-state physical model for describing the grid voltage dynamics is considered, and the grid voltage parameters are estimated using a prediction/correction filter. Fig. 1.4 depicts the general block diagram of the SSLKF-PLL.

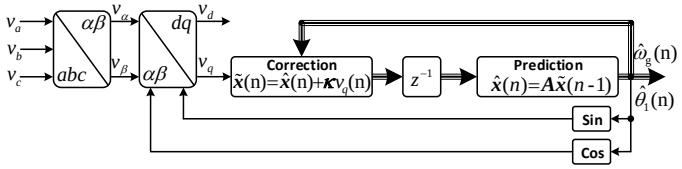

Fig. 1.4: General Block diagram of the SSLKF-PLL.

The reported results in [34] demonstrate that the SSLKF-PLL ensures a zero steady-state phase error in response to phase jumps, frequency jumps, and frequency ramps. The advantages and disadvantages of this structure compared to a typical type-III SRF-PLL, nevertheless, is unclear.

1.1.1.1.3 Three-Phase PLLs with Enhanced DC-Offset Rejection Ability

It was discussed before that the SRF-PLL is highly vulnerable to the DC offset presence in its input. The reason is that even a small DC component in the SRF-PLL input may cause large fundamental-frequency oscillations in its estimated phase, frequency, and amplitude [36]. It has also been proved recently that in the presence of this disturbance, the SRF-PLL unit vector (i.e., the sine and cosine of the estimated phase angle) contains a DC component [36]. Considering that the PLL unit vector is often employed for the reference current generation in grid-connected current-controlled converters, a DC component appears in the converter reference current in this condition, which (depends on the converter current control loops) may lead to injecting a DC current by the converter to the grid [36]. It should be emphasized here that the international standards have limited injecting the DC current by grid-tied converters. According to standards IEC61727 [37] and IEEE 1547-2003 [38], this limit is 1% and 0.5% of the nominal current of the converter, respectively. This discussion highlights the importance of a high DC rejection ability for PLLs.

To enhance the SRF-PLL DC-offset filtering ability, some research efforts have been made. A basic approach is including two moving average filters (MAFs) in the SRF-PLL structure, as illustrated in Fig. 1.5 [39], [40]. The MAF is a rectangular window filter with the following *s*-domain transfer function, in which T_w is called the window length.

$$G_{MAF}(s)=\frac{1-e^{-T_w s}}{T_w s} \tag{1.8}$$

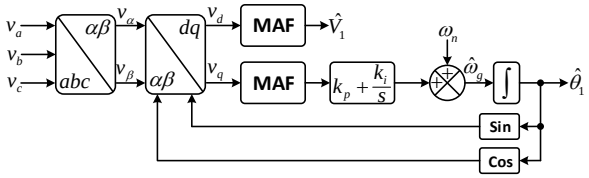

Fig. 1.5: SRF-PLL with in-loop MAF.

As discussed before, the DC component presence in the input of the SRF-PLL leads to fundamental-frequency ripples in the *dq*-axis signals (after the Park's transformation). Considering that the MAF passes the zero frequency component and filters all harmonics whose frequencies are m/T_w $(m=1,2,3,\cdots)$, removing the fundamental-frequency oscillations using the MAF requires a window length equal to the grid fundamental period [39]. As MAFs are within the control loop of SRF-PLL, such a wide window length leads to a large inloop phase delay and, hence, an extremely slow dynamic behavior. It should be emphasized here that, the MAF with a window length equal to the grid fundamental period, removes all harmonics up to aliasing frequency in addition to the fundamental-frequency disturbance component [39].

An alternative approach to support the SRF-PLL in rejecting the DC offset is including the so-called *dq*-frame delayed signal cancellation (*dq*DSC) operator in the SRF-PLL structure [41]-[43]. The resultant PLL structure is the same as Fig. 1.5 except that the MAFs are replaced with *dq*DSC operators.

The *dq*DSC operator is a nonrecursive filter with the following s-domain transfer function [41]-[43]

$$dq\text{DSC}_n(\text{s}) = \frac{1+e^{-\frac{Ts}{n}}}{2} \tag{1.9}$$

in which T denotes the fundamental period of grid voltage and n is the delay factor. As removing a fundamental-frequency disturbance component using the *dq*DSC operator is concerned here, the delay factor n should be set equal to 2. Such an operator, for sure, effectively rejects the fundamental-frequency ripples caused by the DC component. But, similar to the MAF, it causes a large inloop phase delay. This delay, of course, is not as large as that is caused by a MAF with $T_w = T$. But, it is still quite large, and hence, leads to a slow transient response for the SRF-PLL.

A more interesting approach than previous ones is including the delayed signal cancellation operator in the SRF-PLL input. It is referred to as the *αβ*-frame delayed signal cancelation (*αβ*DSC) operator and is described in the *s*-domain as follows [36], [41], [42], [45]

$$\alpha\beta DSC_n(s) = \frac{1 + e^{\frac{j2\pi}{n}} e^{-\frac{Ts}{n}}}{2}. \quad (1.10)$$

Similar to the *dq*DSC operator case, removing the DC offset using this filter requires a delay factor equal to 2. Compared to the previous options, i.e., the *dq*DSC operator and in-loop MAF, this filter results in a less adverse effect on the SRF-PLL dynamic behavior because it is placed in the SRF-PLL input. However, there is still room for improvement because a half cycle delay for removing only the DC component sounds too large. This is particularly true when rejecting the even-order harmonics is not required.

1.1.1.1.4 Three-phase PLLs with Enhanced Imbalanced and Harmonic Rejection Ability

It was briefly discussed before that the grid voltage imbalance, which may be caused by asymmetrical loading, grid faults, and the line impedance imbalance, results in a double-frequency oscillatory ripple, and a harmonic component of order *h* leads to an *h-1* order harmonic frequency ripple in the SRF-PLL estimated parameters. These ripples significantly degrade the SRF-PLL accuracy. To enhance the SRF-PLL imbalance and harmonic rejection capability some efforts have been made in recent years [5]. The most advanced solutions are examined in what follows.

A possible approach to making the SRF-PLL immune to the disturbing effects of the grid voltage harmonics, imbalance, and even DC offset, is using a MAF-based prefilter in its input, as shown in Fig. 1.6 [44]. This prefilter includes two MAFs in the SRF. The window length of MAFs and the rotating angle of its SRF are adapted to the grid frequency changes by employing an additional frequency detector. It should be noted that the phase and frequency detected by the SRF-PLL may not be used for adapting the MAF-based prefilter. The reason is that, from the control point of view, it corresponds to include the MAFs within the control loop of SRF-PLL, which results in a very slow dynamic response.

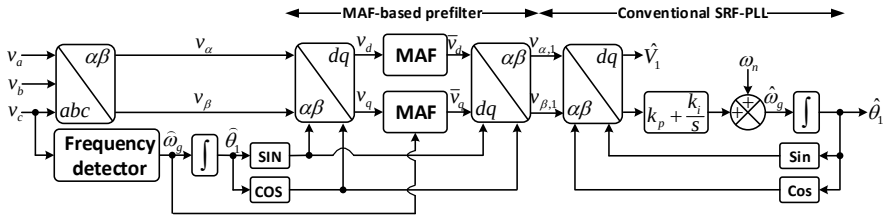

Fig. 1.6: SRF-PLL with a MAF-based prefilter.

The performance of the SRF-PLL with the MAF-based prefiltering stage highly depends on the frequency detector. In other words, the efficient operation of this PLL demands a highly accurate frequency detector, which is corresponding to an increased complexity and computational burden.

An alternative approach to enhance the SRF-PLL harmonic/imbalance rejection capability is using a chain of $\alpha\beta$DSC operators as its prefiltering stage [41], [42], [45]-[48]. Different combinations of $\alpha\beta$DSC operators may be used in the chain. Selecting a proper combination depends on the grid voltage distortion pattern. A common practice is assuming an unknown pattern for the grid voltage distortions, which implies that the presence of all harmonics in the grid voltage is possible. In this condition, a chain of five $\alpha\beta$DSC operators with the delay factors 2, 4, 8, 16, and 32 is employed in the SRF-PLL input, as shown in Fig. 1.7 [41], [42]. Notice that the delay length of operators is variable. These delays are adapted to the variations of the grid frequency using a frequency feedback loop. This task most often involves employing interpolation techniques because the approximation of fractional delays is almost always required. When the sampling frequency is high, a linear interpolation technique is good enough. But, in high-power converters, where the switching frequency and, hence, the sampling frequency are low, a high-order interpolation is needed, which results in a high computational burden and implementation complexity. Besides, using variable-length delays in the CDSC-PLL complicates its modeling and, consequently, analyzing its stability and selecting its control parameters. No one has yet been able to obtain the linearized model of this PLL structure.

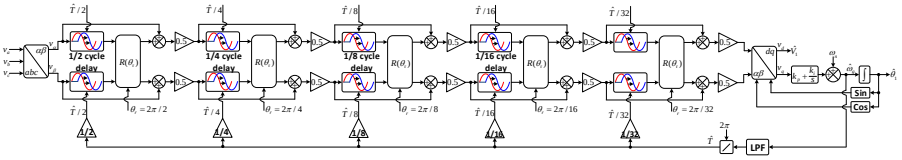

Fig. 1.7: $\alpha\beta$-frame cascaded delayed signal cancellation-based PLL (briefly called the CDSC-PLL).

To avoid feeding back the estimated frequency for adapting the length of delays, a different structure referred to as the generalized delayed signal cancellation-based PLL (GDSC-PLL) is proposed [45]-[47]. This structure includes two chains of identical operators and two SRF-PLLs. One chain is nonadaptive and the other one is frequency-adaptive. The nonadaptive chain and its associated SRF-PLL are responsible to provide an initial estimation of the frequency of grid voltage for adjusting the length of delays of the frequency-adaptive chain. In this way, it can be ensured that the PLL structure always remains stable. This advantage is at the cost of a considerably higher computational burden. Notice that the computational burden of the GDSC-PLL is almost twice that of the CDSC-PLL. Notice also that the small-signal modeling and efficient tuning of the GDSC-PLL, similar to the CDSC-PLL, has not been conducted yet.

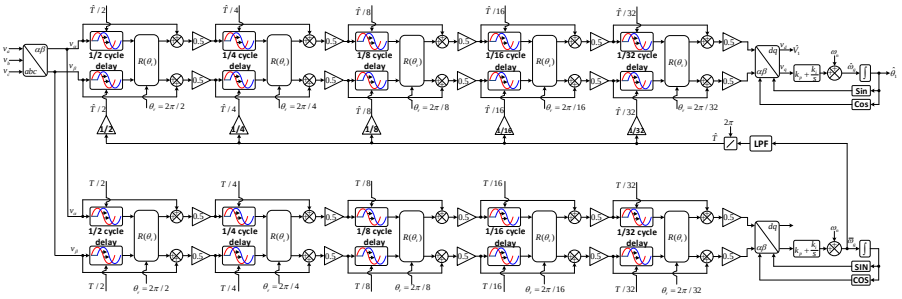

Fig. 1.8: Generalized delayed signal cancellation-based PLL (GDSC-PLL).

1.1.1.2 Single-phase PLLs

1.1.1.2.1 Standard Single-phase PLL

Fig. 1.9 depicts the block diagram of a standard single-phase PLL, which is often called the power-based PLL (pPLL) [6], [29], [31], [49]. The pPLL characteristic is using a product-type PD, which results in a simple structure. This simplicity, nevertheless, is at the cost of a poor performance. The reason is that the product-type PD, in addition to the phase error information, causes a very large double-frequency disturbance component in its output, which results in large oscillatory and offset errors [6], [29], [31], [49]. In addition, making the pPLL dynamics decoupled from the amplitude variations of grid voltage is not possible as the pPLL does not extract the grid voltage amplitude [6].

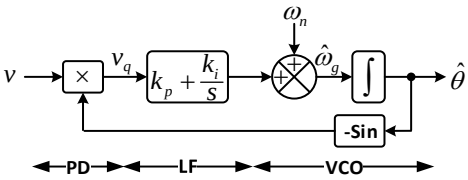

Fig. 1.9: Power-based PLL (pPLL).

Solving the drawbacks of the pPLL has been the main motivation behind developing more advanced single-phase PLLs [6]. These advanced single-phase PLLs may be divided into two main categories: Enhanced pPLLs and quadrature signal generation-based PLLs (QSG-PLLs) [6].

What almost all enhanced pPLLs have in common is adding a filtering stage inside the standard pPLL control loop to remove the double-frequency disturbance term. Using a high-order LPF [29], notch filter [50], and MAF [40] are some possible

options. A rather large in-loop phase delay and, therefore, a slow dynamic response is the cost of using these filters. For this reason, enhanced pPLLs have not received a wide attention.

The QSG-PLLs are the single-phase versions of the conventional SRF-PLL [6]. The common feature of almost all QSG-PLLs is generating a quadrature signal from the single-phase grid voltage [51]. This fictitious signal, which is used as the β-axis signal for the frame transformation, may be generated in different ways [6]. This is actually the main difference of QSG-PLLs compared to each other. Transfer delay [52], [53], second-order generalized integrator (SOGI) [30], [54], all-pass filter [55], [56], sliding discrete Fourier transform [25], [57], [58], inverse Park transformation [29], [30], [59], synchronous reference frame MAF [60], differentiator [61], and Hilbert transform [62], [63] are well-known options. In what follows, delay-based and SOGI-based approaches, which are probably the most popular options, are examined.

1.1.1.2.2 Transfer Delayed-based PLLs

Fig. 1.10 depicts the block diagram of a standard transfer delay-based PLL (TD-PLL), which uses a fixed-length quarter cycle delay for generating a β-axis signal for the conventional SRF-PLL. This structure works satisfactorily under a nominal (or very close to nominal) grid frequency. Under frequency drifts, nevertheless, the generated fictitious signal is nonorthogonal to the grid voltage fundamental component, which leads to offset and oscillatory errors.

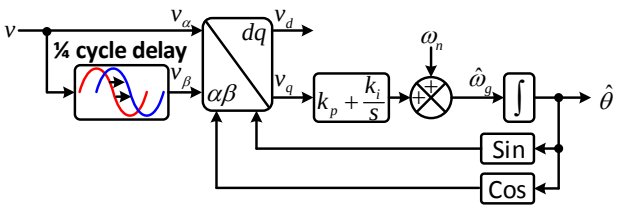

Fig. 1.10: Standard TD-PLL.

To correct offset and oscillatory errors of the TD-PLL with the fixed-length delay, some attempts have been made. For example, in [52] and [53], a structure referred to as the non-frequency-dependent TD-PLL (NTD-PLL) is suggested. Fig. 1.11 illustrates this idea. As shown, the NTD-PLL uses two fixed-length quarter cycle delays. The first one is for generating the quadrature signal v_β, and the second one is for correcting the phase offset error. This correction is carried out by generating $\cos(\hat{\theta})$ from $\sin(\hat{\theta})$ using a fixed-length delay.

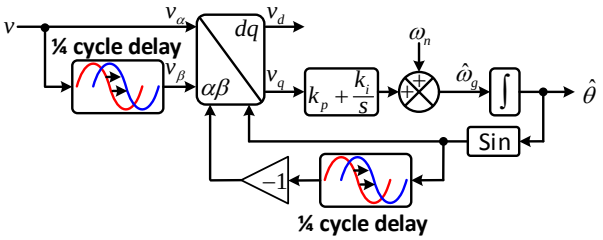

Fig. 1.11: Non-frequency-dependent TD-PLL (NTD-PLL).

The NTD-PLL benefits from a simple structure as it continues using fixed-length delays. In addition, it corrects the phase offset error of the standard TD-PLL under frequency drifts. It, nevertheless, is not able to solve the double-frequency problem. It is worth mentioning that the modeling and tuning of the NTD-PLL have not been carried out yet.

Another approach to solving the standard TD-PLL problems is adapting the length of its delay using a frequency feedback loop, as illustrated in Fig. 1.12. This procedure involves utilizing an interpolation technique as a fractional delay approximation is required. Selecting the interpolation polynomial depends on the sampling frequency and the required accuracy. At a high sampling frequency, which corresponds to a short distance between samples, a linear interpolation is good enough.

The VLTD-PLL is an effective PLL structure that corrects the offset and oscillatory errors of the standard TD-PLL. The VLTD-PLL implementation, however, as mentioned before, involves using a variable length delay, which complicates the modeling and, hence, the tuning and stability assessment. To the best of the Author's knowledge, no accurate model for the VLTD-PLL has yet been derived.

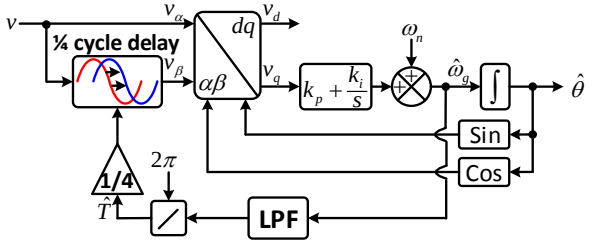

Fig. 1.12: Variable-length transfer delay-based PLL (VLTD-PLL).

1.1.1.2.3 Second-order Generalized Integrator-based PLLs

The standard SOGI-PLL (hereafter, just called the SOGL-PLL) is one of the most popular single-phase PLLs because it has a more or less simple structure and offers an acceptable harmonic filtering rejection ability. This PLL structure includes a SOGI-based quadrature signal generator (SOGI-QSG), which extracts the fundamental component of the grid voltage and generate its quadrature ($90°$ phase shifted) version, and a conventional SRF-PLL. There is a frequency feedback loop in this structure that adapts the SOGI resonance frequency to the grid frequency changes. This loop results in a strong coupling between the dynamics of the SOGI-QSG and SRF-PLL. The block diagram of the standard SOGI-PLL can be observed in Fig. 1.13 [54].

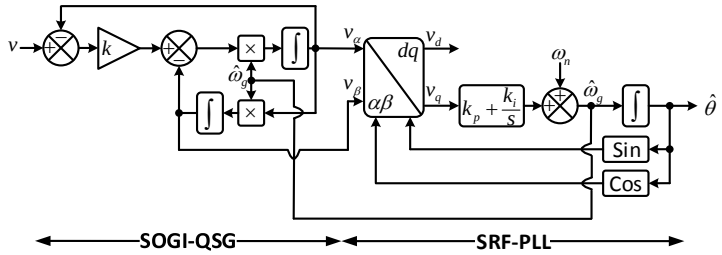

Fig. 1.13: Standard SOGI-PLL.

To further enhance the SOGI-PLL performance, some modifications to its structure have been suggested. The important ones are as follows

- The first one is adding an LPF in the frequency feedback loop [64]. This idea is probably intended to reduce the level of coupling between the SOGI-QSG and SRF-PLL.
- The second one is removing the frequency feedback loop and fixing the resonance frequency of the SOGI at the nominal frequency and employing a compensator for compensating the errors generated by the nonadaptive SOGI-QSG [65].
- The third one, similar to the previous one, is using a nonadaptive SOGI-QSG in the SRF-PLL input and adding a second nonadaptive SOGI-QSG in the phase feedback loop to compensate for errors [66].
- The fourth one is using two cascaded SOGI-QSG in the SRF-PLL input [67], [68]. Notice that the only input to the second SOGI-QSG is the α-axis output of the first one. In this way, the DC offset is completely removed. Notice also that these two SOGI-QSGs can be frequency-adaptive or not. In the latter case, correcting errors requires a compensator.
- The fifth one is making the SOGI-QSG self-adaptive [69]. In this way, the need for the frequency feedback loop is removed.

In summary, different researchers have recommended different modifications, and all of them claim that these modifications result in a considerable performance enhancement compared to the standard SOGI-PLL. These claims are just supported by some numerical results. It is, however, no evidence to confirm that the condition of comparison has been fair. Moreover, no information about the tuning procedure of these so-called enhanced SOGI-PLLs is available. The key to solving these problems is developing the small-signal models of these PLL structures. Accurate modeling of these enhanced SOGI-PLLs has not yet been carried out.

1.1.2. FREQUENCY-LOCKED LOOPS (FLLS)

FLLs, like PLLs, are classified under the category of closed-loop synchronization techniques. But, contrary to PLLs, they are implemented in the stationary reference frame[1]. In addition to the synchronization of power converters [71]-[77], FLLs are widely used in different industrial applications such as flux estimation for motor drives [78], [79], islanding detection [80], delay estimation of sinusoidal signals [81], estimation of electromagnetic oscillations [82], etc.

1.1.2.1 Single-phase FLLs

Implementing single-phase FLLs is often based on a generalized integrator. Fig. 1.14 illustrates the block diagram of a standard single-phase FLL, which is based on a SOGI [71].

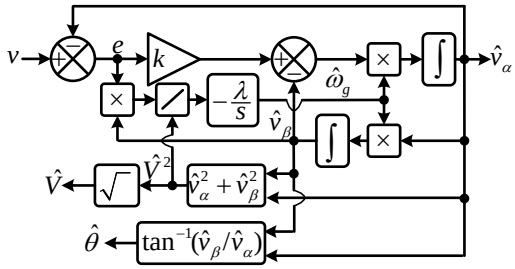

Fig. 1.14: Standard SOGI-FLL.

[1] Very recently, some so-called FLLs have been designed in the synchronous reference frame [70].

This structure extracts the grid voltage fundamental component and its quadrature version, i.e., $\hat{v}_\alpha$ and $\hat{v}_\beta$, using a SOGI-QSG. The phase and amplitude of the grid voltage fundamental component are then obtained as expressed below

$$\hat{\theta} = \tan^{-1}\left(\frac{\hat{v}_\beta}{\hat{v}_\alpha}\right) \tag{1.11}$$

$$\hat{V} = \sqrt{\hat{v}_\alpha^2 + \hat{v}_\beta^2}\,. \tag{1.12}$$

Adapting the SOGI center frequency is carried out based on the following differential equation

$$\frac{d\hat{\omega}_g}{dt} = -\frac{\lambda}{\hat{V}^2}\left(v - \hat{v}_\alpha\right)\hat{v}_\beta \tag{1.13}$$

in which λ is the frequency estimation gain.

The standard SOGI-FLL has a limited disturbance rejection ability. In addition, the accurate small-signal modeling of the SOGI-FLL has not yet been carried out.

To enhance the SOGI-FLL filtering capability, some research efforts have been made. For example, Fig. 1.15 illustrates a SOGI-FLL with prefilter (SOGI-FLL-WPF) [75]. The prefilter is a SOGI-QSG, but only its α-axis output is used. In this way, the SOGI-FLL-WPF is totally immune to the DC offset of the grid voltage. Using the prefilter is also expected to improve the SOGI-FLL ability in filtering the grid voltage harmonics. The modeling of this structure, however, has not yet been conducted. The lack of a small-signal model makes the tuning and stability analysis of the SOGI-FLL-WPF difficult.

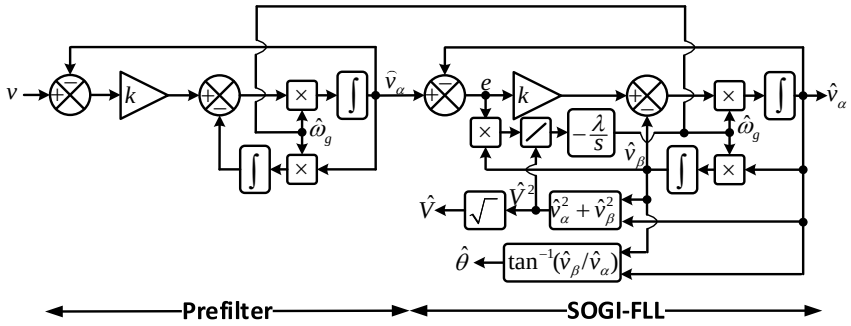

Fig. 1.15: SOGI-FLL with prefilter (SOGI-FLL-WPF).

In [76], an advanced FLL through establishing a structural resemblance between an LPF and SOGI-QSG is designed. The developing procedure of this FLL is as follows. It is first shown that if the loop integrator of a first-order LPF [see Fig.

1.16(a)] is replaced by a SOGI, the SOGI-QSG [see Fig. 1.16(b)] is obtained. Based on this structural resemblance, a four-order generalized integrator-based QSG (FOGI-QSG) [see Fig. 1.16(d)] is proposed in [76], which is obtained by substituting two integrators of a second-order LPF [see Fig. 1.16(c)] by two SOGIs. And finally, using this FOGI-QSG and the same frequency estimator as that of the standard SOGI-FLL, an advanced FLL as shown in Fig. 1.16(e) is developed.

The FOGI-FLL has been designed very recently, and its small-signal modeling, stability analysis, tuning procedure have not yet been carried out. In addition, its advantages and disadvantages compared to the SOGI-FLL-WPF are unclear.

Using a parallel configuration of multiple SOGIs centered at low-order harmonic frequencies is another approach for enhancing the SOGI-FLL performance [71]. A limitation of this approach is its computational burden as removing any additional harmonic requires an extra SOGI.

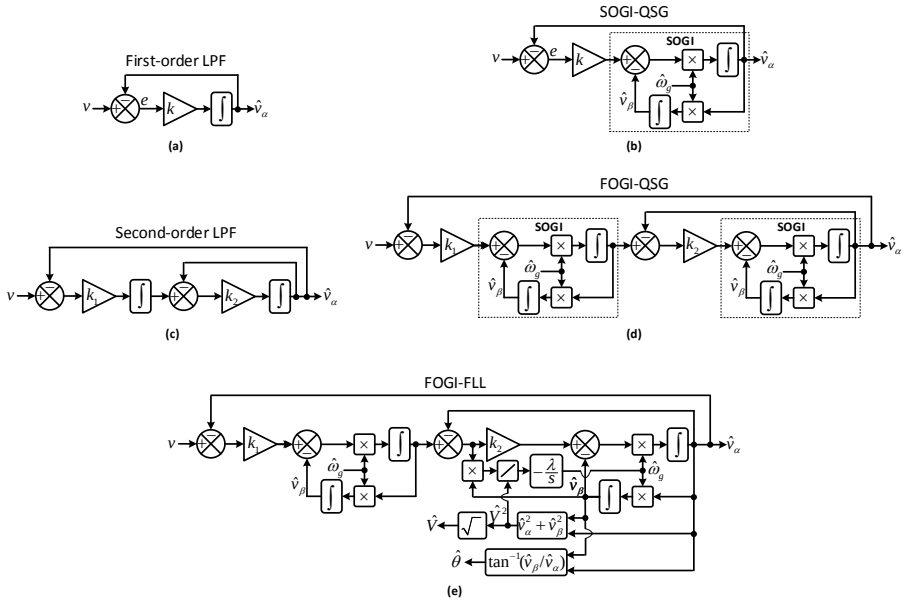

Fig. 1.16: Developing an advanced FLL through establishing a structural resemblance between an LPF and SOGI-QSG. (a) First-order LPF, (b) SOGI-QSG, (c) second-order LPF, (d) four-order generalized integrator-based QSG (FOGI-QSG), and (e) FOGI-FLL.

1.1.2.2 Three-phase FLLs

Implementing three-phase FLLs is based on the reduced-order generalized integrator (ROGI), which is described in the s-domain as $1/(s-j\omega_c)$ [83], where ω_c is the ROGI center frequency. Fig. 1.17 illustrates the block diagram of a standard three-phase FLL, which is called the ROGI-FLL.

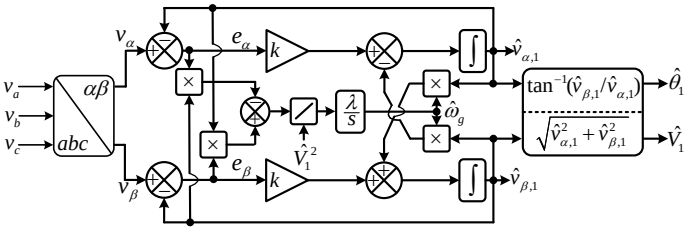

Fig. 1.17: Standard ROGI-FLL.

The ROGI-FLL is based on using a ROGI in a unity feedback structure, which results in a complex bandpass filter (CBF) centered at the fundamental frequency. Therefore, the signals $\hat{v}_{\alpha,1}$ and $\hat{v}_{\beta,1}$ at the ROGI-FLL outputs are the estimations of the grid voltage FFPS component. The ROGI resonance frequency, which is the CBF center frequency, is updated based on the following differential equation

$$\frac{d\hat{\omega}_g}{dt}=\frac{\lambda}{\hat{V}^2}\left(e_\beta\hat{v}_{\alpha,1}-e_\alpha\hat{v}_{\beta,1}\right) \tag{1.14}$$

in which λ is the frequency estimation gain. The phase and amplitude of the grid voltage are finally calculated using the extracted FFPS component as shown in Fig. 1.17. The ROGI-FLL has a limited filtering capability and its modeling has not been conducted yet.

The available methods for enhancing the ROGI-FLL filtering capability are similar to those described for the SOGI-FLL (i.e., using a parallel configuration of multiple ROGIs centered at low-order harmonic frequencies [84]-[87], designing a high-order FLL by establishing a structural resemblance between an LPF and CBF [76], etc.) Therefore, for the sake of brevity, they are not repeated here.

1.1.3. OPEN-LOOP SYNCHRONIZATION (OLS) TECHNIQUES

The key characteristic of an OLS technique, as mentioned before, is using no feedback signal in its structure, which results in an unconditional stability. It is probably the main benefit of an OLS technique compared to PLLs and FLLs.

Fig. 1.18 illustrates a standard three-phase OLS technique. The key part of this structure is a bandpass filter that extracts the grid voltage FFPS component. The frequency, phase, and amplitude are then calculated using this extracted FFPS component as $\hat{\omega}_g = (\dot{\hat{v}}_{\beta,1}\hat{v}_{\alpha,1} - \dot{\hat{v}}_{\alpha,1}\hat{v}_{\beta,1}) / (\hat{v}_{\alpha,1}^2 + \hat{v}_{\beta,1}^2)$, $\hat{\theta}_1 = \tan^{-1}(\hat{v}_{\beta,1}/\hat{v}_{\alpha,1})$ and $\hat{V}_1 = \sqrt{\hat{v}_{\alpha,1}^2 + \hat{v}_{\beta,1}^2}$, where $\dot{v}_x = dv_x / dt$. Simplicity, low computational burden, unconditional stability, and fast dynamic response are the key features of this structure. It, however, has a serious drawback: It may not work effectively under off-nominal frequencies as the BPF center frequency is not adaptive (it is fixed at the nominal frequency) [89]. To be more exact, a frequency change results in errors in the phase and amplitude of the extracted FFPS component and, hence, the estimated phase and amplitude. Solving this problem has been the main motivation behind developing advanced OLS techniques. A brief review is conducted below.

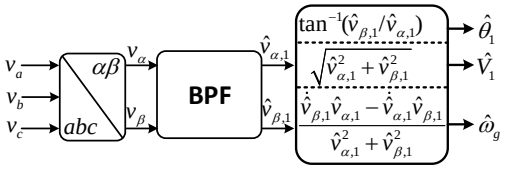

Fig. 1.18: A standard three-phase OLS technique.

An approach, which is sometimes used by researchers to solve the above-mentioned errors, is feeding back the estimated frequency for adapting the BPF to the grid frequency changes [90]. In such a case, however, the synchronization technique may not be regarded open-loop anymore.

Another method is employing a parallel frequency detector for extracting the grid frequency and adapting the BPF to the grid frequency changes [91], [92]. Fig. 1.19 illustrates this idea. This frequency detector needs to have its own filtering stage and should provide a fast yet accurate estimation of the grid frequency. Such requirement results in a considerable increase in the implementation complexity and computation burden.

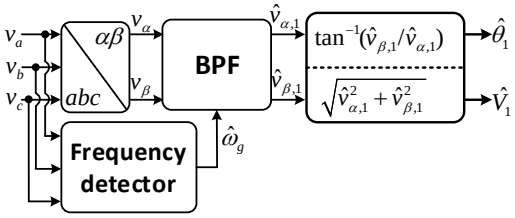

Fig. 1.19: Using a parallel frequency detector in an OLS technique to avoid errors under off-nominal frequency.

Some researchers do not follow the standard structure and use a totally different topology for implementing an open-loop technique. An example is shown in Fig. 1.20 [93], [94]. In this structure, the grid voltage angle is calculated by applying an arctangent function to the $\alpha\beta$-axis grid voltage signals. Then, an unwrapping algorithm is employed to remove the phase discontinuities. As the slope of the unwrapped phase angle is equal to the grid frequency, a differentiator/LPF is used for extracting the grid frequency. The unwrapped phase angle is also passed through an LPF and, subsequently, through a compensator to remove its oscillatory ripples and accurately detect the grid voltage phase angle. The compensator here is responsible to correct the phase offset caused by passing the unwrapped phase angle through the LPF. The grid voltage amplitude is also estimated by passing the *d*-axis signal through an LPF. The *dq*-axis signals are generated by applying the Park's transformation to the $\alpha\beta$-axis signals. The rotating angle of this Park's transformation is the estimated phase angle.

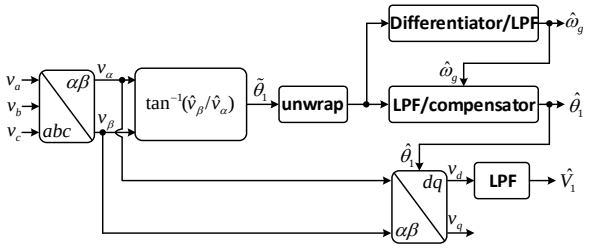

Fig. 1.20: A different way of implementing an OLS technique.

This OLS technique, however, may not be very practical. The main limitation here is unwrapping the phase angle. The reason is that, regardless of the implementation complexity of an efficient unwrapping method, the unwrapped phase angle continuously grows, which results in the DSP register overflow. It implies that a resetting system should be included. This resetting, however, causes phase discontinuities and, therefore, large transients in the estimated quantities.

In developing single-phase OLS techniques, the situation is even more complicated than before because, in addition to filter the signal-phase signal, its quadrature version should be provided. Fig. 1.21 illustrates the schematic diagram of a standard single-phase OLS technique.

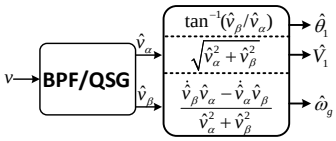

Fig. 1.21: A standard single-phase OLS technique.

1.2. THESIS OBJECTIVES

Advancing the state-of-the-art in the field is the overall objective of this thesis. To this end, the following specific objectives are considered.

Regarding PLLs, the following objectives are defined:

- The first objective is the modeling, stability analysis, tuning, and performance assessment of single-phase transfer delay-based PLLs (TD-PLLs) and three-phase delayed-signal cancellation based-PLLs (DSC-PLLs). Designing an approach to eliminate the need for adjusting the length of delays in these PLLs is also a part of this objective.
- The second objective is analyzing the steady-state linear Kalman filter-based PLLs (SSLKF-PLLs) and highlighting their advantages and disadvantages compared to a standard SRF-PLL and its close variants.
- The third objective is developing a simple, efficient, and general approach to deal with the DC-offset problem in three-phase PLLs.
- The last but not the least objective is designing a simple yet effective approach to eliminating the need for using a parallel frequency detector in the PLL with the MAF-based prefiltering stage. Deriving a small-signal modeling for this PLL is also a part of this objective.

Regarding FLLs, the following objectives are defined:

- The first objective is modeling, tuning, analyzing, and comparative performance evaluation of SOGI-based FLLs.
- The second objective is introducing the concept of inloop filter in FLLs.
- The third objective is finding a relationship between FLLs and PLLs.
- The last but not the least objective is using the FLL concept to design self-adaptive proportional-resonant (PR) controllers for the control of single-phase grid-interfaced power converters.

Regarding OLS techniques, the following objectives are defined:

- The objective is designing OLS techniques with a very fast dynamic response, efficient operation under nominal and off-nominal frequencies, high filtering capability, and simple structure for three-phase and single-phase applications.

1.3. THESIS OUTLINE

The rest of this thesis is organized as follows.

Chapter 2 presents the contributions of this thesis to modeling, analyzing, and designing PLLs. To be more exact, it presents the modeling and tuning procedures of some single-phase and three-phase TD-PLLs, and performs an analysis on SSLKF-PLLs. A general approach for the DC offset rejection in three-phase PLLs is also designed in this chapter. Finally, a method for eliminating the need for using a parallel frequency detector in the PLL with the MAF-based prefiltering stage is presented.

Chapter 3 summarizes the contributions of this thesis to modeling, analyzing, and designing FLLs. Demonstrating the modeling and tuning procedure of standard and advanced FLLs, introducing the concept of inloop filter in FLLs, demonstrating the relation between PLLs and FLLs, and designing an adaptive resonant regulator for single-phase grid-tied converters are the main parts of the chapter.

Chapter 4 presents the procedure of designing advanced single-phase and three-phase OLS techniques.

Chapter 5 summarizes the contributions of this thesis and the directions for the future research.

CHAPTER 2. MODELING, ANALYZING, AND DESIGNING PLLS

This chapter is a summary of contributions of this thesis to modeling, analyzing, and designing PLLs.

2.1. TRANSFER DELAY-BASED PLLS (TD-PLLS)

This part mainly deals with deriving small-signal models for the advanced single-phase and three-phase TD-based PLLs. To be more exact, the NTD-PLL, VLTD-PLL, CDSC-PLL, and GDSC-PLL are modeled. The tuning procedures of these PLLs are also briefly discussed. An adaptive single-phase TD-based PLL with a fixed-length delay is also designed and presented here.

2.1.1. STANDARD TD-PLL

The block diagram representation of a standard TD-PLL is observed in Fig. 2.1 [95]. The key part of this structure is a fixed-length quarter cycle delay, which provides a fictitious orthogonal signal (which is represented by v_β) for transferring information to the synchronous reference frame. This structure offers a great simplicity in the digital implementation; nevertheless, it has a serious drawback: the fictitious signal does not have exactly a $90°$ phase difference compared to the fundamental component of the grid voltage when its frequency deviates from the nominal value. This problem causes offset and oscillatory errors in the standard TD-PLL output. Fig. 2.2 clearly illustrates these two types of errors. Solving these errors has been the main motivation for developing more advanced single-phase TD-PLLs in the literature.

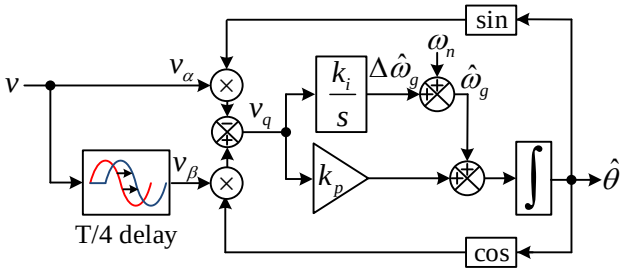

Fig. 2.1: Block diagram representation of the standard TD-PLL [95].

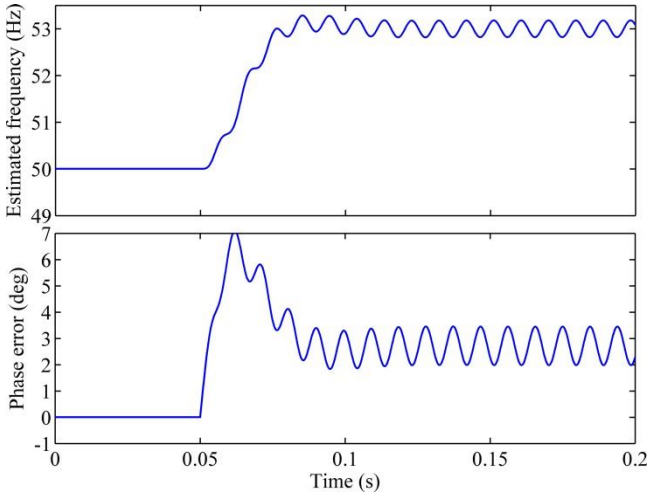

Fig. 2.2: Performance of the standard TD-PLL under a +3-Hz jump in the grid frequency [97].

2.1.2. NON-FREQUENCY-DEPENDENT TD-PLL (NTD-PLL)

The block diagram representation of the NTD-PLL, which has been proposed in [52] and [53], is seen in Fig. 2.3. The basic idea of the NTD-PLL, as mentioned before, is the indirect generation of the cosine of the estimated phase angle by delaying the sine of the estimated phase angle by a fixed-length quarter cycle delay. Preserving the implementation simplicity of the standard TD-PLL and solving its phase offset error are the key features of the NTD-PLL.

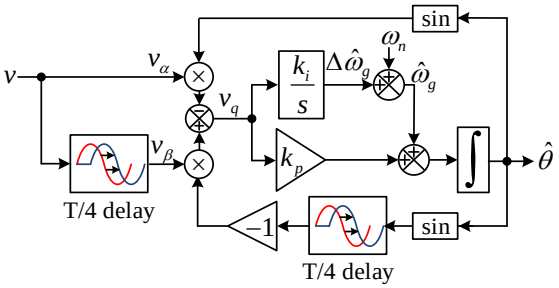

Fig. 2.3: Basic structure of the NTD-PLL [95].

As mentioned before, no small-signal model for this structure has yet been derived. As a result, the only available option for tuning the control parameters of this PLL is trial and error. In what follows, a small-signal model and a systematic tuning method for the NTD-PLL are presented.

2.1.2.1 Modeling of the NTD-PLL

In this section, the modeling procedure of the NTD-PLL is briefly presented. To see a more detailed procedure, refer to [95] (Paper 3 in Appendix).
For deriving the NTD-PLL small-signal model, it is assumed that the input signal is as follows

$$v(t) = v_\alpha(t) = V\cos(\theta) \tag{2.1}$$

in which V and θ denote the amplitude and phase angle of the input signal, respectively. Without loss of generality, $\theta = \omega_g t + \varphi$ is considered, where ω_g and φ are the angular frequency and initial phase angle, respectively.

Based on the aforementioned assumptions and the structure of the NTD-PLL in Fig. 2.3, the signal v_q in the input of the PI regulator may be expressed as

$$\begin{aligned} v_q(t) &= -v_\alpha(t)\sin\left(\hat{\theta}\right) - v_\beta(t)\sin\left(\hat{\theta}_d\right) \\ &= \frac{V}{2}\sin\left(\theta-\hat{\theta}\right) + \frac{V}{2}\sin\left(\theta_d-\hat{\theta}_d\right) - \frac{V}{2}\underbrace{\sin\left(\theta+\hat{\theta}\right)}_{D_2'(t)} - \frac{V}{2}\underbrace{\sin\left(\theta_d+\hat{\theta}_d\right)}_{D_2'(t-T/4)} \end{aligned} \tag{2.2}$$

in which $\theta_d(\mathrm{t}) = \theta(\mathrm{t}-\mathrm{T}/4)$ and $\hat{\theta}_d(\mathrm{t}) = \hat{\theta}(\mathrm{t}-\mathrm{T}/4)$. By defining $\theta = \theta_n + \Delta\theta$ and $\hat{\theta} = \theta_n + \Delta\hat{\theta}$, (2.2) can be approximated by

$$v_q(t) \approx \frac{V}{2}\left[\left(\Delta\theta - \Delta\hat{\theta}\right) + \left(\Delta\theta_d - \Delta\hat{\theta}_d\right) - D_2'(t) - D_2'(t-T/4)\right] \tag{2.3}$$

where $\Delta\theta_d(\mathrm{t}) = \Delta\theta(\mathrm{t}-\mathrm{T}/4)$ and $\Delta\hat{\theta}_d(\mathrm{t}) = \Delta\hat{\theta}(\mathrm{t}-\mathrm{T}/4)$.
In the *s*-domain, (2.3) is equivalent to

$$v_q(s) \approx V\frac{1+e^{-sT/4}}{2}\left[\Delta\theta(\mathrm{s}) - \Delta\hat{\theta}(\mathrm{s}) - D_2'(s)\right]. \tag{2.4}$$

Using (2.4) and Fig. 2.3, the small-signal model of the NTD-PLL may be obtained as depicted in Fig. 2.4.

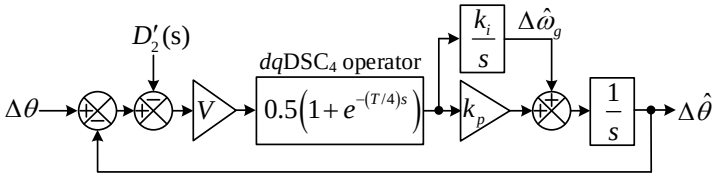

Fig. 2.4: NTD-PLL small-signal model [95].

To investigate the accuracy of this model, some standard tests (a phase jump and a frequency jump) are performed. The results of this investigation may be observed in Fig. 2.5. The model, as shown, is able to predict the NTD-PLL average behavior very accurately.

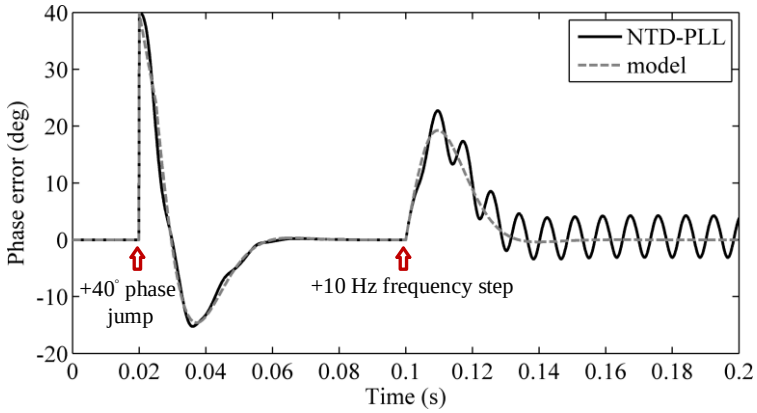

Fig. 2.5: Investigating the accuracy of the NTD-PLL model [95].

2.1.2.2 Tuning of the NTD-PLL

In this part, a method for tuning the NTD-PLL control parameters is briefly presented. For more details, refer to [95] (Paper 3 in Appendix).

According to the small-signal model of the NTD-PLL and by neglecting the disturbance input to its model, the open-loop transfer function of this PLL may be expressed as

$$G_{ol}(s)=\left.\frac{\Delta\hat{\theta}(\mathrm{s})}{\Delta\theta(\mathrm{s})-\Delta\hat{\theta}(\mathrm{s})}\right|_{D_2'(s)=0}=V\frac{1+e^{-(T/4)s}}{2}\frac{k_p s+k_i}{s^2}. \tag{2.5}$$

The equation (2.5) can be rewritten as (2.6) by replacing its delay term by the first-order Pade approximation.

$$G_{ol}(s)\approx V\frac{1}{(T/8)s+1}\frac{k_p s+k_i}{s^2} \tag{2.6}$$

Now the symmetrical optimum (SO) method is simply applied to (2.6), which gives the control parameters as follows

$$\begin{aligned} k_p &= \frac{1}{Vb(\mathrm{T}/8)} \\ k_i &= \frac{1}{Vb^3(\mathrm{T}/8)^2}. \end{aligned} \tag{2.7}$$

In (2.7), b is the phase margin (PM) determining factor, i.e., $\mathrm{PM}=\tan^{-1}\left(\frac{b^2-1}{2b}\right)$.

By choosing $b=\sqrt{2}+1$, which is corresponding to an optimum damping factor for

the closed-loop poles of the NTD-PLL and provides a PM equal to $45°$, the control parameters can be calculated as $k_p = 166$ and $k_i = 11371$.

2.1.3. VARIABLE-LENGTH TD-PLL (VLTD-PLL)

As discussed before, the standard TD-PLL suffers from oscillatory and offset errors and the NTD-PLL structure may only solve its phase offset problem. To correct both errors of the standard TD-PLL, a VLTD-PLL may be used. The block diagram representation of this PLL is illustrated in Fig. 2.6.

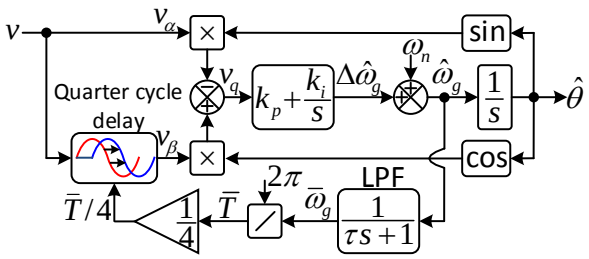

Fig. 2.6: Block diagram representation of the standard VLTD-PLL [96].

In the VLTD-PLL, the length of quarter cycle delay is not fixed anymore. Indeed, as mentioned before, it is adjusted using a frequency feedback loop in each sampling period. In this way, the signal v_β is always orthogonal to the grid voltage fundamental component and, therefore, no offset and oscillatory errors happen under frequency drifts. The presence of this variable length delay in the VLTD-PLL structure, nevertheless, makes the modeling procedure complicated. No small signal model for the VLTD-PLL has yet been derived. And because of the lack of a linearized model, the tuning procedure is carried out based on the trial and error, which is time-consuming. In what follows, a small-signal model for the VLTD-PLL is derived and a systematic tuning method for selecting its control parameters is presented.

2.1.3.1 Modeling of the VLTD-PLL

In this section, the modeling procedure of the VLTD-PLL is briefly presented. For a more detailed procedure, refer to [96] (Paper 4 in Appendix).
Similar to the case of the NTD-PLL, the input signal of the VLTD-PLL is considered to be as (2.1). Based on this assumption and the VLTD-PLL structure, the orthogonal signal v_β may be expressed as

$$v_\beta(t) = V\cos(\theta - \omega_g \bar{T}/4). \tag{2.8}$$

Considering (2.1), (2.8), and Fig. 2.6, we may express the signal v_q in the input of the PI regulator as

$$v_q(t) = \frac{V}{2}\Big[\cos(\theta - \hat{\theta} - \omega_g \bar{T}/4) + \sin(\theta - \hat{\theta}) \mathbf{- \sin(\theta + \hat{\theta}) + \cos(\theta + \hat{\theta} - \omega_g \bar{T}/4)}\Big]. \tag{2.9}$$

Notice that the highlighted terms cancel each other in the steady state. Notice also that $\omega_g \bar{T}/4$ is a nonlinear term and needs to be linearized. Considering that $\bar{T} = 2\pi/\bar{\omega}_g$ and defining $\bar{\omega}_g = \omega_n + \Delta\bar{\omega}_g$ and $\omega_g = \omega_n + \Delta\omega_g$, this term may be approximated by

$$\frac{\omega_g \bar{T}}{4} = \frac{2\pi}{4}\frac{1+\dfrac{\Delta\omega_g}{\omega_n}}{1+\dfrac{\Delta\bar{\omega}_g}{\omega_n}} \approx \frac{2\pi}{4}\left(1-\frac{\Delta\bar{\omega}_g}{\omega_n}\right)\left(1+\frac{\Delta\omega_g}{\omega_n}\right) \approx \frac{\pi}{2} - \frac{T}{4}\Delta\bar{\omega}_g + \frac{T}{4}\Delta\omega_g \tag{2.10}$$

By substituting (2.10) into (2.9) and considering the definitions made earlier for θ and $\hat{\theta}$, we have

$$v_q(t) \approx V\left[\frac{T}{8}\Delta\bar{\omega}_g - \Delta\hat{\theta} + \frac{\Delta\theta + \{\Delta\theta - (T/4)\Delta\omega_g\}}{2}\right] \tag{2.11}$$

which results in (2.12) in the *s*-domain.

$$v_q(s) \approx V\left[\frac{T}{8}\Delta\bar{\omega}_g(s) - \Delta\hat{\theta}(s) + \frac{1+e^{-(T/4)s}}{2}\Delta\theta(s)\right]. \tag{2.12}$$

Using (2.12) and the Fig. 2.6, the linear model of the VLTD-PLL is achieved as illustrated in Fig. 2.7.

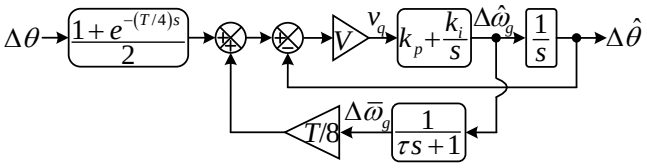

Fig. 2.7: VLTD-PLL model [96].

Similar to before, some standard tests are performed to investigate the model accuracy. Fig. 2.8 illustrates the results of this investigation. This figure clearly demonstrates the accuracy of the obtained model in predicting the average transient behavior of the VLDT-PLL.

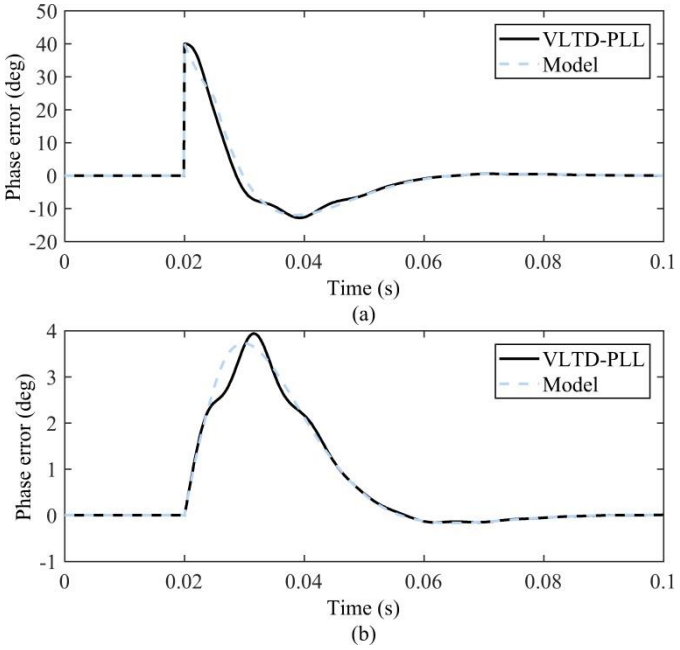

Fig. 2.8: A comparison between the VLTD-PLL and its model under (a) a 40° phase jump and (b) +2-Hz frequency step change [96].

2.1.3.2 Tuning of the VLTD-PLL

In this part, the tuning procedure of the VLTD-PLL control parameters is briefly discussed. For more details, refer to [96] (Paper 4 in Appendix).

According to the VLTD-PLL model, its closed-loop transfer function may be expressed as

$$G_{cl}(s)=\frac{\Delta\hat{\theta}(s)}{\Delta\theta(s)}=\frac{1+e^{-\frac{Ts}{4}}}{2}\frac{V\left(\tau s+1\right)\left(k_p s+k_i\right)}{\left(s^2+Vk_p s+Vk_i\right)\left(\tau s+1\right)-\frac{T}{8}Vs\left(k_p s+k_i\right)}. \tag{2.13}$$

Selecting $k_p/k_i=\tau$ results in a pole-zero cancellation and simplifies (2.13) as

$$G_{cl}(s)=\frac{1+e^{-(T/4)s}}{2}\frac{Vk_p s+Vk_i}{s^2+V\left(k_p-k_i T/8\right)s+Vk_i}. \tag{2.14}$$

Now, by defining $V\left(k_p-k_i T/8\right)=2\zeta\omega_n'$ and $Vk_i=\left(\omega_n'\right)^2$, where ζ is the damping factor and ω_n' is the natural frequency, the VLTD-PLL proportional and integrator gains may be expressed as

$$k_p = \frac{\left(\omega_n' T/8 + 2\zeta\right)\omega_n'}{V}$$
$$k_i = \frac{\left(\omega_n'\right)^2}{V} \tag{2.15}$$
$$\tau = \frac{k_p}{k_i} = \frac{T}{8} + \frac{2\zeta}{\omega_n'}.$$

Here, an optimum damping factor, i.e., $\zeta = 0.707$, and $\omega_n' = 2\pi 20$ rad/s are chosen which, according to (2.15), results in $k_p = 217$, $k_i = 15791$ and $\tau = 0.01375$.

2.1.4. ADAPTIVE TD-PLL (ATD-PLL)

The VLTD-PLL structure, as mentioned before, solves all errors of the standard TD-PLL. Its implementation, however, requires adjusting the length of a delay. This procedure almost always involves the fractional delay approximation. This task demands to apply interpolation methods, which makes the VLTD-PLL implementation a bit complicated. The aim of this part is presenting a PLL structure with exactly the same performance as the VLTD-PLL, but without the requirement for adapting its delay length. The design procedure is briefly presented in what follows. For a more detailed design procedure, refer to [97] (Paper 5 in Appendix).

As the starting point of the design procedure, consider the standard TD-PLL structure, which is shown in Fig. 2.1. By considering (2.1) as its input signal, the fictitious signal v_β (i.e., the output of the fixed-length quarter cycle delay) may be expressed as

$$v_\beta(t) = V\cos\left(\theta - \frac{\omega_g T}{4}\right). \tag{2.16}$$

Considering the definition of the grid frequency as a perturbation around the nominal frequency, i.e., $\omega_g = \omega_n + \Delta\omega_g$, (2.16) can be rewritten as

$$v_\beta(t) = V\sin\left(\theta - \frac{\Delta\omega_g T}{4}\right) = -\overbrace{V\cos(\theta)}^{v_\alpha}\sin\left(\frac{\Delta\omega_g T}{4}\right) + \overbrace{\boldsymbol{V\sin(\theta)}}^{v_\beta'}\cos\left(\frac{\Delta\omega_g T}{4}\right). \tag{2.17}$$

The highlighted (bold) term is the required orthogonal signal. This signal, according to (2.17), may be expressed as a function of the single-phase input signal (v_α) and the fixed-length quarter cycle delay output (v_β) as follows

$$v_\beta'(\mathrm{t}) = \frac{v_\alpha(t)\sin\left(\frac{\Delta\omega_g T}{4}\right) + v_\beta(t)}{\cos\left(\frac{\Delta\omega_g T}{4}\right)}. \tag{2.18}$$

Based on (2.18) and the standard TD-PLL structure (Fig. 2.1), the proposed PLL structure, which is briefly called the adaptive TD-PLL (ATD-PLL), is obtained as

illustrated in Fig. 2.9. Notice that the output of the PI regulator integrator is considered as an estimation of $\Delta\omega_g$ for the calculation of v'_β.

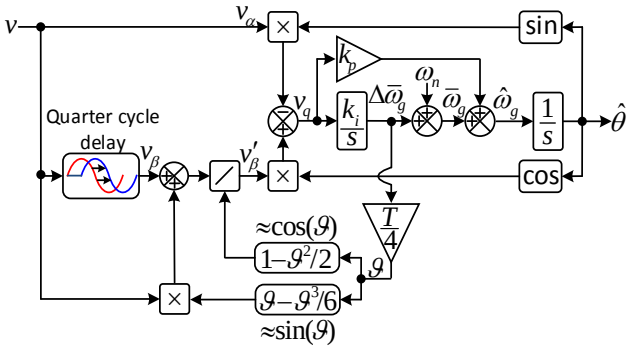

Fig. 2.9: Block diagram representation of the proposed ATD-PLL [97].

Notice also that, as the grid frequency variations are limited in practice, the trigonometric terms in the frequency feedback loop are approximated by the first two terms of their Taylor series expansions.

2.1.4.1 Modeling and Tuning of the ATD-PLL

In this part, the modeling and tuning procedure of the ATD-PLL are briefly discussed. For more details, refer to [97] (Paper 5 in Appendix).

By considering (2.1) as the input signal, the signal v'_β in the ATD-PLL structure may be expressed as

$$v'_\beta(t) = \frac{V\cos(\theta)\sin\left(\frac{\Delta\bar{\omega}_g T}{4}\right) + V\sin\left(\theta - \frac{\Delta\omega_g T}{4}\right)}{\cos\left(\frac{\Delta\bar{\omega}_g T}{4}\right)}. \tag{2.19}$$

Using (2.19), the signal v_q in the PI regulator input can be expressed as

$$v_q(t) = \frac{V}{2}\left[\sin(\theta-\hat{\theta}) + \tan\left(\frac{\Delta\bar{\omega}_g T}{4}\right)\cos(\theta-\hat{\theta}) + \frac{\sin\left(\theta - \frac{\Delta\omega_g T}{4} - \hat{\theta}\right)}{\cos\left(\frac{\Delta\bar{\omega}_g T}{4}\right)}\right] + \underbrace{\frac{V}{2}\left[-\sin(\theta+\hat{\theta}) + \tan\left(\frac{\Delta\bar{\omega}_g T}{4}\right)\cos(\theta+\hat{\theta}) + \frac{\sin\left(\theta - \frac{\Delta\omega_g T}{4} + \hat{\theta}\right)}{\cos\left(\frac{\Delta\bar{\omega}_g T}{4}\right)}\right]}_{D_2(t)} \tag{2.20}$$

It can be proved that $D_2(\mathrm{t}) \approx 0$ in the steady state. Based on this fact and the following approximations, (2.20) can be approximated by (2.22).

$$\begin{aligned}
&\sin(\theta - \hat{\theta}) \approx \theta - \hat{\theta} = \Delta\theta - \Delta\hat{\theta} \\
&\cos(\theta - \hat{\theta}) \approx 1 \\
&\tan\left(\frac{\Delta\bar{\omega}_g T}{4}\right) \approx \frac{\Delta\bar{\omega}_g T}{4} \\
&\cos\left(\frac{\Delta\bar{\omega}_g T}{4}\right) \approx 1 \\
&\sin\left(\theta - \frac{\Delta\omega_g T}{4} - \hat{\theta}\right) \approx \theta - \frac{\Delta\omega_g T}{4} - \hat{\theta} = \Delta\theta - \frac{\Delta\omega_g T}{4} - \Delta\hat{\theta}
\end{aligned} \tag{2.21}$$

$$v_q(\mathrm{t}) \approx V\left[\frac{T\Delta\bar{\omega}_g}{8} - \Delta\hat{\theta} + \frac{\Delta\theta + \left(\Delta\theta - \Delta\omega_g T/4\right)}{2}\right]. \tag{2.22}$$

In the *s*-domain, (2.22) is equivalent to

$$v_q(s) \approx V\left[\frac{T\Delta\bar{\omega}_g(\mathrm{s})}{8} - \Delta\hat{\theta}(\mathrm{s}) + \frac{1 + e^{-\frac{T}{4}s}}{2}\Delta\theta(\mathrm{s})\right]. \tag{2.23}$$

Based on (2.23) and Fig. 2.9, the ATD-PLL model may be obtained as illustrated in Fig. 2.10.

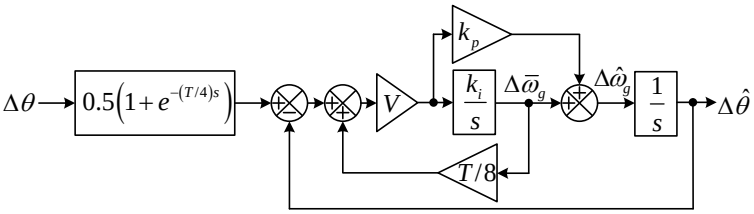

Fig. 2.10: ATD-PLL small-signal model [97].

The investigation of the accuracy of the ATD-PLL model, as before, is conducted using some standard tests. The results of this investigation, which is shown in Fig. 2.11, proves the model accuracy.

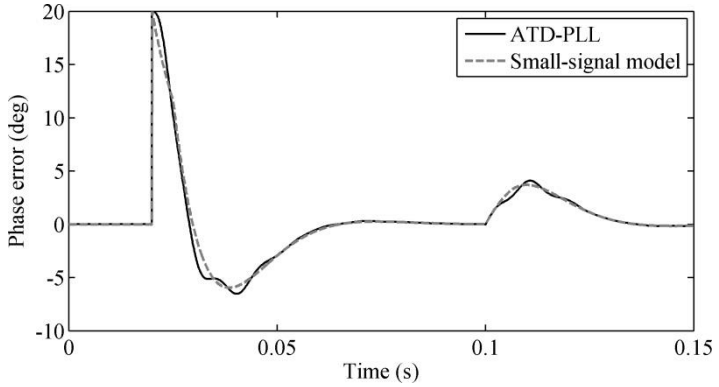

Fig. 2.11: A comparison between the ATD-PLL and its model under $20°$ phase jump and subsequently +2-Hz frequency step change [97].

According to the obtained model, the ATD-PLL closed-loop transfer function can be achieved as

$$G_{cl}(s)=\frac{1+e^{-(T/4)s}}{2}\frac{Vk_p s+Vk_i}{s^2+V\left(k_p-k_i T/8\right)s+Vk_i}. \tag{2.24}$$

This transfer function is the same as (2.14), i.e., the VLTD-PLL closed-loop transfer function. Therefore, the same tuning procedure and the same control parameters as those selected for the VLTD-PLL may be used here. These values are $k_p=217$ and $k_i=15791$. Having the same closed-loop transfer functions also implies that the ATD-PLL provides the same performance as good as that of the VLTD-PLL. The difference here is that the VLTD-PLL requires a variable-length delay. The ATD-PLL, however, uses a fixed-length delay, which results in a simplicity in the implementation.

2.1.4.2 Performance Comparison

In this section, the performance of the proposed ATD-PLL is compared with the NTD-PLL and VLTD-PLL using simulation tests in Matlab/Simulink and dSPACE-based experimental tests.

Fig. 2.12 illustrates the performance of the ATD-PLL and NTD-PLL in response to a +10 Hz/s ramping change in the grid frequency for a duration of 0.3 s. It can be observed that growing double-frequency oscillations appear in the NTD-PLL response. The performance of the proposed ATD-PLL, however, is free from such oscillations in the steady state.

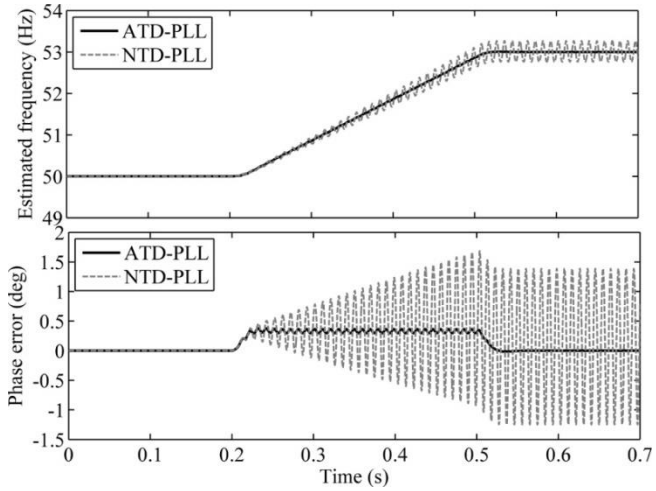

Fig. 2.12: A performance comparison between the ATD-PLL and NTD-PLL in response to a +10 Hz/s ramping change in the grid frequency for 0.3 s [97].

Fig. 2.13 compares the ATD-PLL and VLTD-PLL performance in response to two tests. The short description of tests can be found in the caption of this figure. It is observed that the ATD-PLL and VLTD-PLL demonstrate well-matched results in both cases. This equivalence was predicted before using the closed-loop transfer functions of these PLLs. The same performance of these PLLs and the implementation simplicity of the ATD-PLL compared to the VLTD-PLL suggest that the ATD-PLL is a better option.

2.1.5. DELAYED SIGNAL CANCELATION (DSC) BASED PLLS

As discussed before, the delayed signal cancellation (DSC) operator is highly popular for filtering disturbances in the SRF-PLL input. The DSC-based PLLs often involve a frequency feedback loop for adapting the length of delays of their operators to the changes of the grid frequency. The presence of variable-length delays in the structure of these PLLs makes their modeling procedure complicated. No small-signal model for these advanced PLLs has yet been presented. This gap is covered in this section. To facilitate understanding the procedure, the modeling of a basic DSC-PLL is first derived and it is then extended to two advanced cases. The tuning procedure and the performance analysis of these advanced DSC-based PLLs are also briefly discussed in this section. For a more detailed description of the content of this section, refer to [96] (Paper 4 in Appendix).

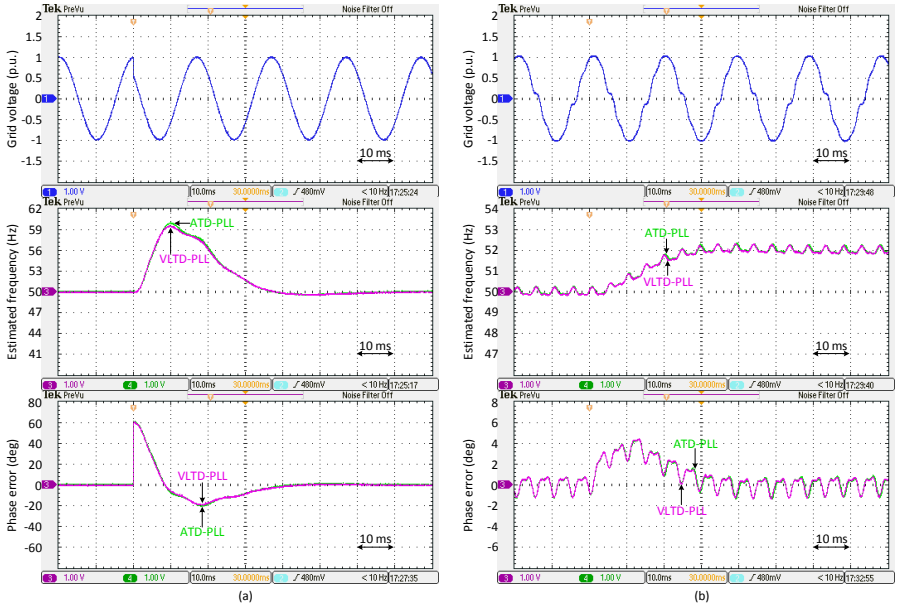

Fig. 2.13: ATD-PLL and VLTD-PLL performance under (a) a 60° jump in the phase angle, and (b) a distorted grid condition with +2-Hz frequency jump [96].

2.1.5.1 Modeling DSC-based PLLs

As mentioned before, the modeling procedure is started from a very simple case, in which the SRF-PLL only uses a single adaptive DSC operator in its input. Fig. 2.14 illustrates the block diagram representation of such a PLL, which is briefly referred to as the $\alpha\beta$DSC-PLL.

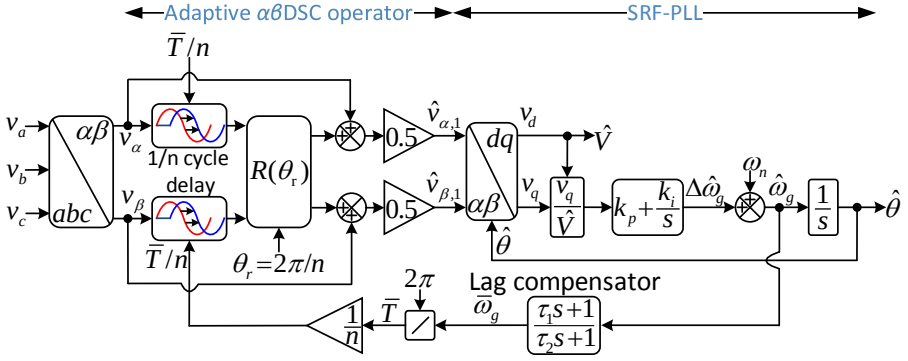

Fig. 2.14: Block diagram representation of the $\alpha\beta$DSC-PLL [96].

By considering the three-phase signals in the input of the $\alpha\beta$DSC-PLL as (2.25), the extracted fundamental component by the operator in the $\alpha\beta$ frame can be expressed as (2.26).

$$\begin{aligned} v_a(t) &= V\cos(\theta) \\ v_b(t) &= V\cos(\theta - 2\pi/3) \\ v_c(t) &= V\cos(\theta + 2\pi/3) \end{aligned} \tag{2.25}$$

$$\begin{aligned} \hat{v}_{\alpha,1}(t) &= \frac{V}{2}\left[\cos\left(\theta + \frac{2\pi}{n} - \frac{\omega_g \bar{T}}{n}\right) + \cos(\theta)\right] \\ \hat{v}_{\beta,1}(t) &= \frac{V}{2}\left[\sin\left(\theta + \frac{2\pi}{n} - \frac{\omega_g \bar{T}}{n}\right) + \sin(\theta)\right] \end{aligned} \tag{2.26}$$

Notice that $\omega_g \bar{T}/n$ in (2.26) is a nonlinear term, which needs to be linearized. Considering that $\bar{T} = 2\pi/\bar{\omega}_g$ and defining $\bar{\omega}_g = \omega_n + \Delta\bar{\omega}_g$ and $\omega_g = \omega_n + \Delta\omega_g$, this term may be approximated by

$$\frac{\omega_g \bar{T}}{n} \approx \frac{2\pi}{n} - \frac{T}{n}\Delta\bar{\omega}_g + \frac{T}{n}\Delta\omega_g. \tag{2.27}$$

Using (2.26), (2.27), and the $\alpha\beta$DSC-PLL structure, the signal v_q in Fig. 2.14 can be expressed as

$$\begin{aligned} v_q(t) &\approx \frac{V}{2}\left[\sin(\Delta\theta - \Delta\hat{\theta} + \Delta\bar{\omega}_g T/n - \Delta\omega_g T/n) + \sin(\Delta\theta - \Delta\hat{\theta})\right] \\ &\approx V\left[\frac{T\Delta\bar{\omega}_g}{2n} - \Delta\hat{\theta} + \frac{\Delta\theta + \left(\Delta\theta - T\Delta\omega_g/n\right)}{2}\right] \end{aligned} \tag{2.28}$$

or equivalently in the *s*-domain as

$$v_q(\mathrm{s}) \approx V\left[\frac{T\Delta\bar{\omega}_g(\mathrm{s})}{2n} - \Delta\hat{\theta}(\mathrm{s}) + \frac{1 + e^{-(T/\mathrm{n})s}}{2}\Delta\theta(\mathrm{s})\right]. \tag{2.29}$$

Based on (2.29), obtaining the $\alpha\beta$DSC-PLL model as shown in Fig. 2.15 is quite straightforward.

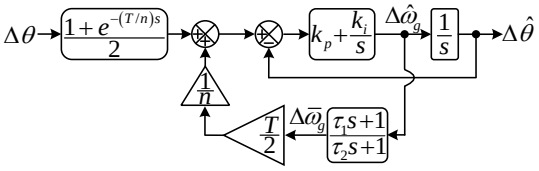

Fig. 2.15: Small-signal model of the $\alpha\beta$DSC-PLL.

Based on this model, the small-signal modeling of advanced DSC-based PLLs may be simply carried now. Figs. 2.16(a) and 2.17(a) illustrate two of such PLLs, namely the CDSC-PLL and GDSC-PLL. The obtained small-signal models for these PLLs are shown in Figs. 2.16(b) and 2.17(b). The results shown in Figs. 2.18 and 2.19 demonstrate the accuracy of these models.

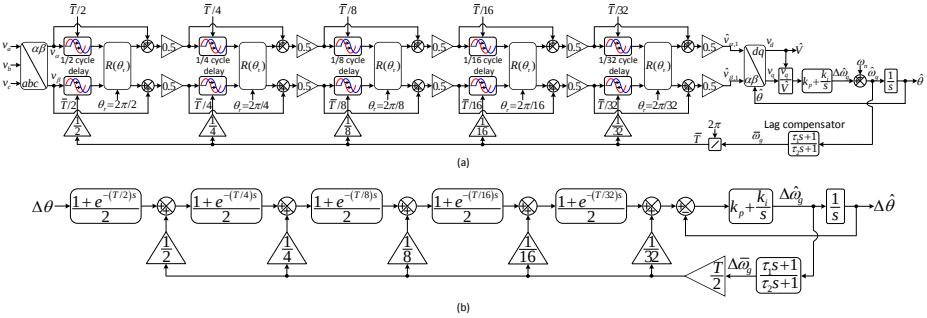

Fig. 2.16: (a) CDSC-PLL and (b) its model [96].

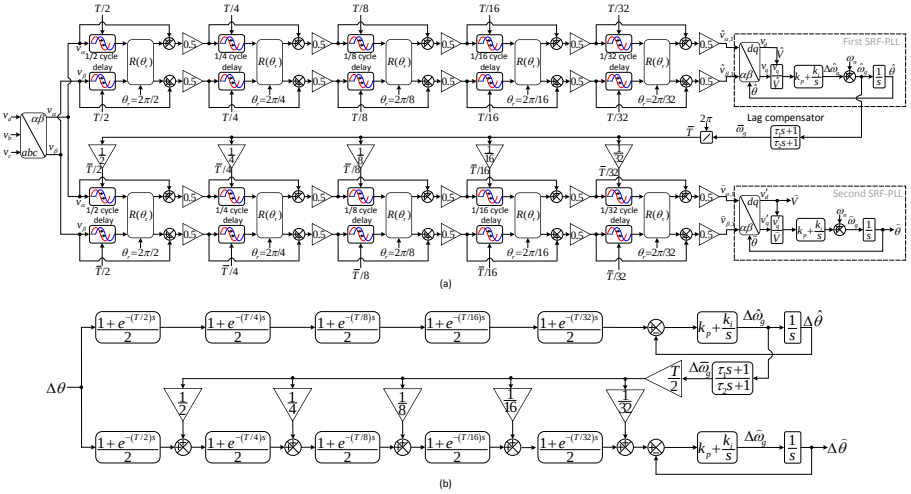

Fig. 2.17: (a) GDSC-PLL and (b) its model [96].

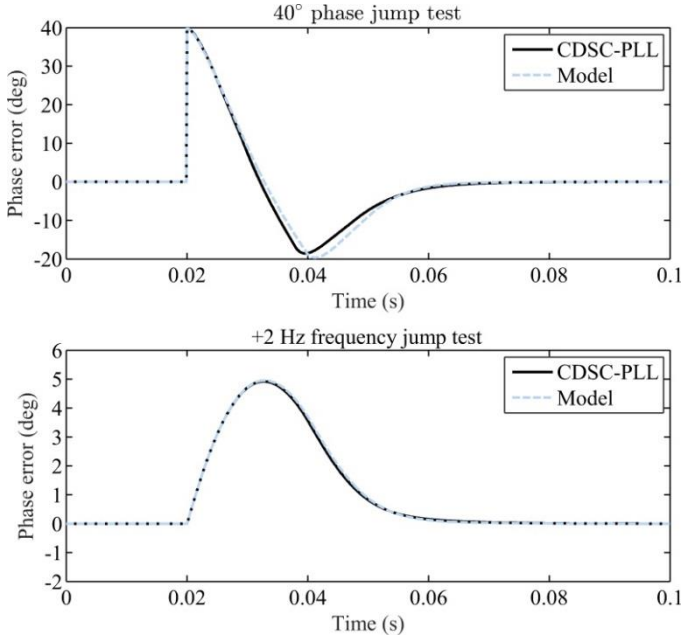

Fig. 2.18: Investigating the accuracy of the CDSC-PLL model [96].

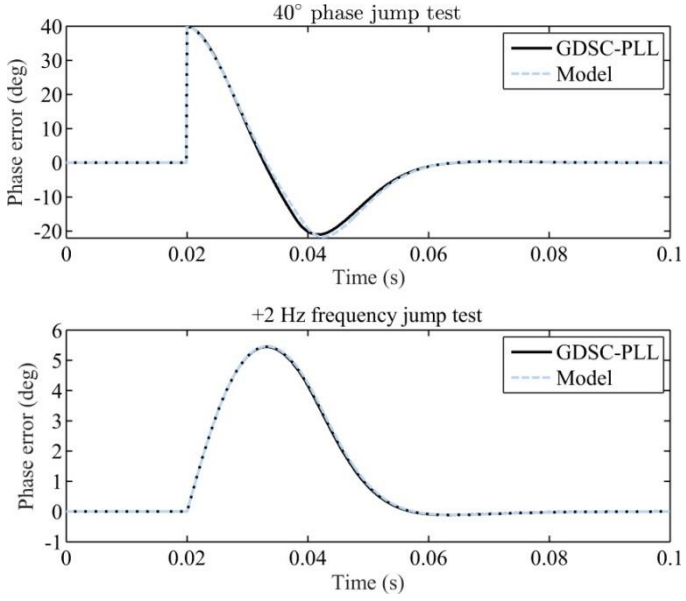

Fig. 2.19: Investigating the accuracy of the GDSC-PLL model [96].

2.1.5.2 Tuning of Advanced DSC-based PLLs

Using Fig. 2.16(b), the CDSC-PLL closed-loop transfer function can be expressed as

$$\Delta\hat{\theta}(s) = \left(\prod_{n=2,4,8,16,32} \frac{1+e^{-\frac{Ts}{n}}}{2}\right) \frac{k_p s + k_i}{s^2 + \left(k_p s + k_i\right)\left[1 - sH(s)L(s)\right]} \Delta\theta(s) \tag{2.30}$$

where

$$L(s) = \frac{1+\tau_1 s}{1+\tau_2 s} \tag{2.31}$$

$$H(s) = \frac{T}{64}\left[1 + \left(1+e^{-\frac{T}{32}s}\right) + \left(1+e^{-\frac{T}{16}s}\right)\left(1+e^{-\frac{T}{32}s}\right) + \left(1+e^{-\frac{T}{8}s}\right)\left(1+e^{-\frac{T}{16}s}\right)\left(1+e^{-\frac{T}{32}s}\right) + \left(1+e^{-\frac{T}{4}s}\right)\left(1+e^{-\frac{T}{8}s}\right)\left(1+e^{-\frac{T}{16}s}\right)\left(1+e^{-\frac{T}{32}s}\right)\right]. \tag{2.32}$$

Using model-order reduction techniques, it can be demonstrated that $H(s)$ in the low-frequency range can be approximated by

$$H(s) \approx \frac{\overbrace{31T/64}^{k_{dc}}}{\underbrace{(10T/64)}_{\tau_r} s + 1}. \tag{2.33}$$

Therefore, by choosing $\tau_1 = \tau_r$, a pole-zero cancellation in the product $H(s)L(s)$ in the denominator of (2.30) is obtained. In this case, (2.30) can be rewritten as

$$\Delta\hat{\theta}(s) \approx \left(\prod_{n=2,4,8,16,32} \frac{1+e^{-\frac{Ts}{n}}}{2}\right) \frac{\left(\tau_2 s+1\right)\left(k_p s + k_i\right)}{s^2\left(\tau_2 s+1\right) + \left(k_p s + k_i\right)\left(\tau_2 s + 1 - k_{dc} s\right)} \Delta\theta(s). \tag{2.34}$$

A second pole-zero cancellation is achieved by selecting $k_p / k_i = \tau_2$. This selection further simplifies (2.34) as

$$\Delta\hat{\theta}(s) \approx \left(\prod_{n=2,4,8,16,32} \frac{1+e^{-\frac{Ts}{n}}}{2}\right) \frac{k_p s + k_i}{s^2 + \left(k_p - k_{dc}k_i\right)s + k_i} \Delta\theta(s). \tag{2.35}$$

Now, by defining $k_p - k_{dc}k_i = 2\xi\omega_n'$ and $k_i = (\omega_n')^2$, k_p and k_i may be determined by selecting ζ and ω_n'. Here $\omega_n' = 2\pi 35$ rad/s and $\zeta = 1$ are chosen, which gives

the CDSC-PLL control parameters as $k_i = 48361$, $k_p = 908.3$, $\tau_1 = 0.003125$, and $\tau_2 = 0.01878$.

For the case of the GDSC-PLL, the closed-loop transfer function can be obtained using Fig. 2.17(b) as

$$\Delta\hat{\theta}(s) = \underbrace{\left(\prod_{n=2,4,8,16,32} \frac{1+e^{-\frac{Ts}{n}}}{2} \right)}_{\approx \frac{1}{(31T/64)s+1}} \left(1 + s\frac{\left[k_p s + k_i\right] H(s)L(s)}{s^2 + k_p s + k_i} \right) \frac{k_p s + k_i}{s^2 + k_p s + k_i} \Delta\theta(s) \qquad (2.36)$$

in which $L(s)$ and $H(s)$ are as expressed in (2.31) and (2.32), respectively.

Similar to before, selecting $\tau_1 = \tau_r$ causes a pole-zero cancellation in the product $H(s)L(s)$. Two other pole-zero cancellations are achieved by choosing $\tau_2 = \frac{k_p}{k_i} = \frac{31T}{64}$. These pole-zero cancellations simplify (2.36) as

$$\Delta\hat{\theta}(s) \approx \frac{k_i \left(s^2 + \left[k_{dc} k_i + k_p\right] s + k_i \right)}{(s^2 + k_p s + k_i)^2} \Delta\theta(s). \qquad (2.37)$$

Notice that the ratio of k_p / k_i has been already set to $31T/64$. Therefore, by defining $k_p = 2\zeta\omega_n'$ and $k_i = (\omega_n')^2$ and selecting the damping factor ζ, both k_p and k_i are determined. Similar to the case of the CDSC-PLL, $\zeta = 1$ is chosen. Notice that $\zeta < 1$ and $\zeta > 1$ both are not good choices here because the former one results in four complex-conjugate poles, which makes the GDSC-PLL dynamic response oscillatory, and the latter one results in an over-damped dynamic behavior.

With the selected value for the damping factor ζ, all control parameters of the GDSC-PLL can be calculated as $k_p = 412.9$, $k_i = 42622$, $\tau_1 = 0.003125$, and $\tau_2 = 0.0096875$.

2.1.5.3 Performance Assessment of Advanced DSC-based PLLs

In this section, a dSPACE-based experimental performance comparison between the CDSC-PLL and GDSC-PLL is conducted. The results of this comparison are shown in Fig. 2.20. It is observed that both PLLs demonstrate comparable results. To be more exact, both of them demonstrate a fast dynamic response and effectively reject the grid voltage disturbances. Considering the lower computational burden of the

CDSC-PLL compared to the GDSC-PLL, it can be concluded that the CDSC-PLL is a better option.

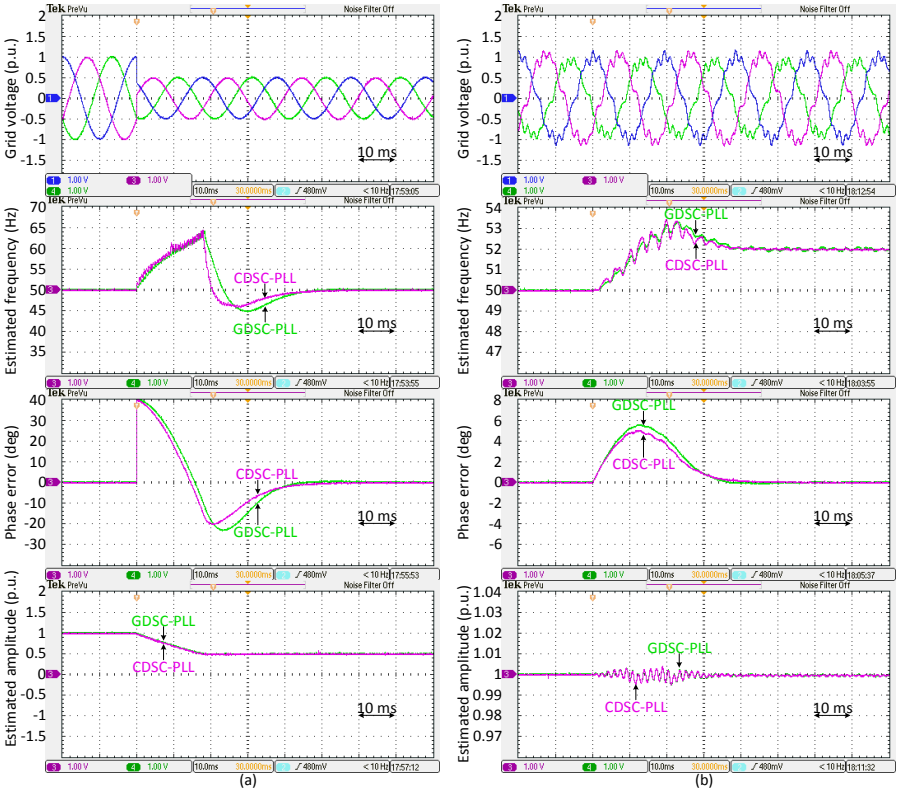

Fig. 2.20: Comparing the performance of the GDSC-PLL and CDSC-PLL under (a) a symmetrical voltage sag with 40° phase jump and (b) a distorted/imbalanced grid condition with a +2-Hz frequency jump [96].

2.2. STEADY-STATE LINEAR KALMAN FILTER (SSLKF) BASED PLLS

As discussed before, the SSLKF-PLLs have received a rather considerable attention for power and energy applications in recent years. A general block diagram representation of the SSLKF-PLL can be observed in Fig. 2.21. Two PLLs based on this concept have been recently designed and proposed in [8] and [34]. The aim of this section is conducting a study on these PLLs to highlight their advantages/disadvantages compared to the conventional SRF-PLL and its variants.

First, a two-state SSLKF-PLL and, then, a three-state SSLKF-PLL is considered and briefly analyzed. It should be mentioned that the content of this section is based on the reference [98] (Paper 6 in Appendix).

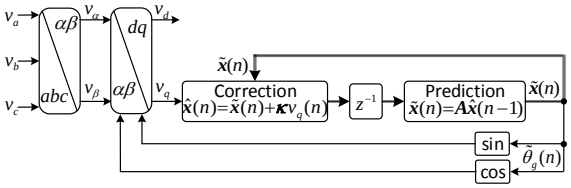

Fig. 2.21: Block diagram representation of the SSLKF-PLL in a general form [98].

2.2.1. TWO-STATE SSLKF-PLL

Designing the two-state SSLKF-PLL, which is hereafter referred to as the SSLKF-PLL2, is based on considering a two-state model for the prediction stage as follows

$$\underbrace{\begin{bmatrix}\theta_g(\mathrm{n})\\ \omega_g(\mathrm{n})\end{bmatrix}}_{\boldsymbol{x}(n)}=\underbrace{\begin{bmatrix}1 & T_s\\ 0 & 1\end{bmatrix}}_{\boldsymbol{A}}\underbrace{\begin{bmatrix}\theta_g(\mathrm{n}-1)\\ \omega_g(\mathrm{n}-1)\end{bmatrix}}_{\boldsymbol{x}(n-1)}$$
$$y(n)=\underbrace{\begin{bmatrix}1 & 0\end{bmatrix}}_{\boldsymbol{C}}\boldsymbol{x}(n) \tag{2.38}$$

in which T_s denotes the sampling period. ω_g and θ_g are the angular frequency and phase angle, respectively.

Based on the aforementioned model, the SSLKF-PLL2 performs the following steps to extract the grid voltage parameters.

- Step 1: State prediction at the next sample as $\tilde{\boldsymbol{x}}(n)=\boldsymbol{A}\,\hat{\boldsymbol{x}}(n-1)$.
- Step 2: Prediction error correction as $\hat{\boldsymbol{x}}(n)=\tilde{\boldsymbol{x}}(n)+\boldsymbol{\kappa}\theta_e(n)$, where $\theta_e(n)$ denotes the phase error information, and $\boldsymbol{\kappa}=[\kappa_1 \quad \kappa_2]^{\mathrm{T}}$ is the correction vector.

Based on these steps and Fig. 2.21, which illustrates a general SSLKF-PLL, the schematic diagram of the SSLKF-PLL2 may be obtained as shown in Fig. 2.22(a). Based on the block diagram algebra, another way of representing the SSLKF-PLL2 can be obtained as illustrated in Fig. 2.22(b). This structure in the *s*-domain is equivalent to Fig. 2.22(c), which is an SRF-PLL that tapes the frequency from the output of PI regulator integrator. Therefore, it can be concluded that the SSLKF-PLL2 and this SRF-PLL, which is often called the enhanced SRF-PLL (ESRF-PLL), are equivalent systems.

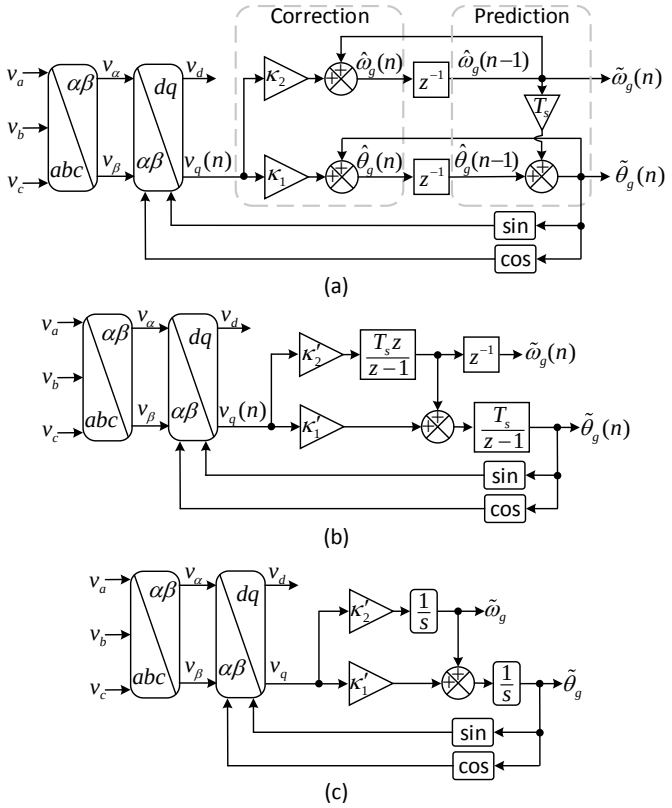

Fig. 2.22: (a) Block diagram representation of the SSLKF-PLL2. (b) Another way of representing the SSLKF-PLL2, in which $\kappa_1' = \kappa_1 / T_s$ and $\kappa_2' = \kappa_2 / T_s$. (c) The continuous-time equivalent of Fig. 2.22(b) [98].

2.2.2. THREE-STATE SSLKF-PLL

Designing a three-state SSLKF-PLL, which is hereafter briefly called the SSLKF-PLL3, is based on the same two steps that were mentioned before for the case of the SSLKF-PLL2. The only difference is that the prediction is based on a three-state model as (2.39). Fig. 2.23(a) illustrates the schematic of the SSLKF-PLL3.

$$\underbrace{\begin{bmatrix}\theta_g(\mathrm{n})\\ \omega_g(\mathrm{n})\\ a_g(\mathrm{n})\end{bmatrix}}_{\boldsymbol{x}(n)} = \underbrace{\begin{bmatrix}1 & T_s & T_s^2/2\\ 0 & 1 & T_s\\ 0 & 0 & 1\end{bmatrix}}_{\boldsymbol{A}} \underbrace{\begin{bmatrix}\theta_g(\mathrm{n}-1)\\ \omega_g(\mathrm{n}-1)\\ a_g(\mathrm{n}-1)\end{bmatrix}}_{\boldsymbol{x}(n-1)} \tag{2.39}$$

$$y(n) = \underbrace{\begin{bmatrix}1 & 0 & 0\end{bmatrix}}_{\boldsymbol{C}} \boldsymbol{x}(n)$$

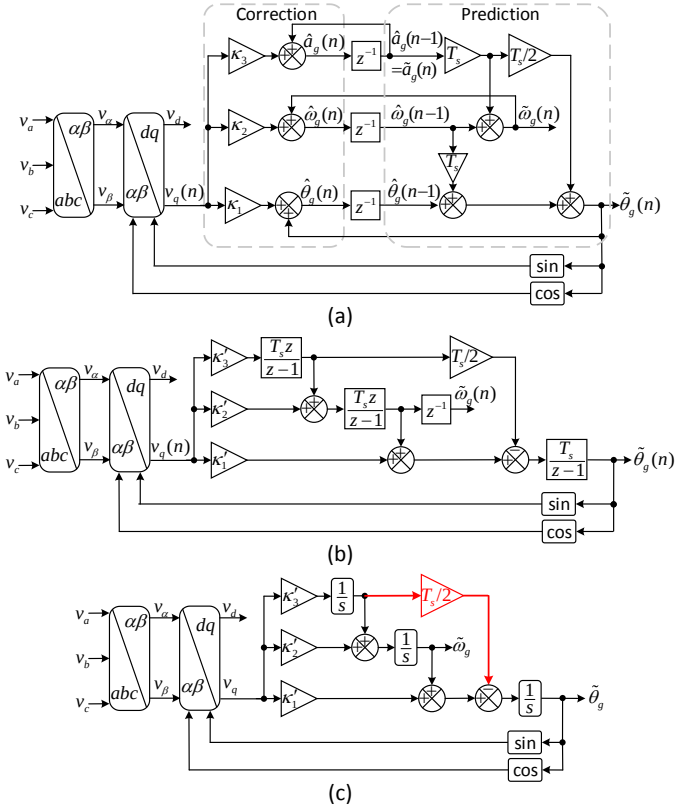

Fig. 2.23: (a) Block diagram representation of the SSLKF-PLL3. (b) Another way of representing the SSLKF-PLL3, in which $\kappa_1' = \kappa_1 / T_s$, $\kappa_2' = \kappa_2 / T_s$, and $\kappa_3' = \kappa_3 / T_s$. (c) The continuous-time equivalent of Fig. 2.23(b) [98].

If we apply the block diagram algebra to Fig. 2.23(a), another way of representing the SSLKF-PLL3 can be obtained as illustrated in Fig. 2.23(b). In the continuous-time domain, this structure is equivalent to Fig. 2.23(c). If we neglect the very small gain $T_s / 2$, which is highlighted by a red color in Fig. 2.23(c), it is observed that this structure is actually a type-3 SRF-PLL, here called the enhanced type-3 SRF-PLL (ET3-SRF-PLL). Therefore, it can be concluded that the SSLKF-PLL3 and ET3-SRF-PLL are practically equivalent systems.

2.2.3. EXPERIMENTAL RESULTS

In was proved theoretically before that the SSLKF-PLL2 and SSLKF-PLL3 are equivalent to the ESRF-PLL and ET3-SRF-PLL, respectively. To support this finding, a performance comparison among these four PLLs is conducted. Fig. 2.24 is

a result of this comparison. It can be observed that both SSLKF-PLLs demonstrate well-matched responses to their corresponding SRF-PLLs.

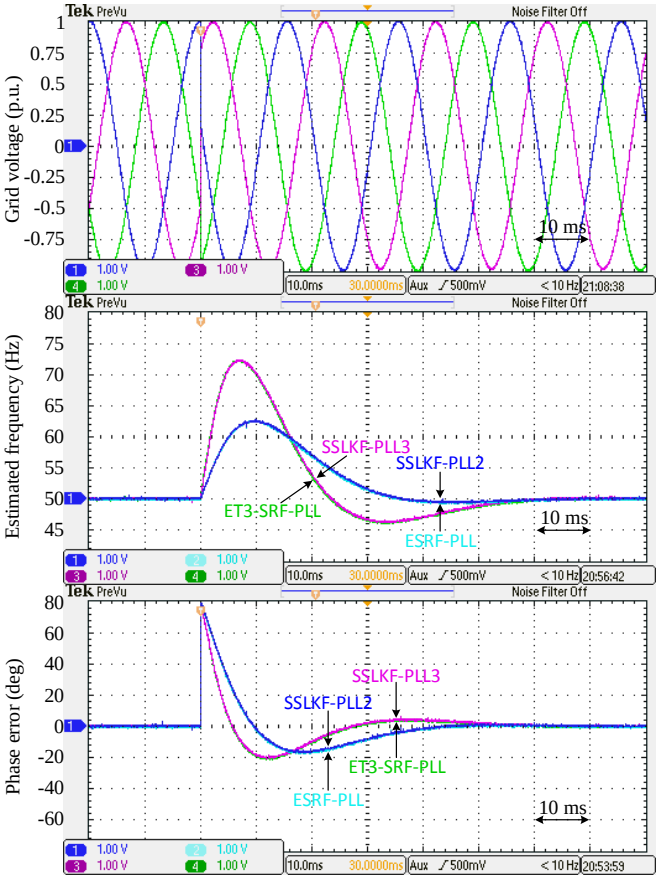

Fig. 2.24: Performance of the SSLKF-PLL2, SSLKF-PLL3, ESRF-PLL, and ET3-SRF-PLL in response to a 80° phase jump [98].

2.3. DESIGNING AN APPROACH FOR DC-OFFSET REJECTION IN THREE-PHASE PLLS

As discussed before, the DC offset is a serious issue in PLL applications and, therefore, demands a particular attention. The aim of this section is presenting a general yet simple and effective approach for filtering the DC offset in the input of three-phase PLLs. The design procedure, modeling, and tuning the control parameters are briefly discussed, and some numerical results are presented. It should be mentioned that the content of this section is based on the reference [99] (Paper 7 in Appendix).

2.3.1. DESIGN PROCEDURE

Assume that the grid voltage signals in the stationary frame are as follows

$$\begin{aligned} v_\alpha(t) &= v_{\alpha,dc} + \underbrace{V\cos(\theta)}_{v_{\alpha,1}(t)} \\ v_\beta(t) &= v_{\beta,dc} + \underbrace{V\sin(\theta)}_{v_{\beta,1(t)}} \end{aligned} \tag{2.40}$$

where $v_{\alpha,1}$ and $v_{\beta,1}$ are its fundamental components in the $\alpha\beta$ frame, and $v_{\alpha,\mathrm{dc}}$ and $v_{\beta,\mathrm{dc}}$ are its DC components. Again, without loss of generality, it is assumed that $\theta = \omega_g t + \varphi$, where φ and ω_g are the initial phase and angular frequency, respectively.

By assuming that the DC components in (2.40) are constant, delaying v_α and v_β gives

$$\begin{aligned} v_\alpha(t-\tau) &= v_{\alpha,dc} + v_{\alpha,1}(t-\tau) = v_{\alpha,dc} + v_{\alpha,1}(t)\cos(\tau\omega_g) + v_{\beta,1}(t)\sin(\tau\omega_g) \\ v_\beta(t-\tau) &= v_{\beta,dc} + v_{\beta,1}(t-\tau) = v_{\beta,dc} - v_{\alpha,1}(t)\sin(\tau\omega_g) + v_{\beta,1}(t)\cos(\tau\omega_g) \end{aligned} \tag{2.41}$$

where τ is the delay length.

Subtracting (2.41) from (2.40) and rearranging the results in the matrix form gives

$$\begin{bmatrix} v_\alpha(t) - v_\alpha(t-\tau) \\ v_\beta(t) - v_\beta(t-\tau) \end{bmatrix} = \underbrace{\begin{bmatrix} 1-\cos(\tau\omega_g) & -\sin(\tau\omega_g) \\ \sin(\tau\omega_g) & 1-\cos(\tau\omega_g) \end{bmatrix}}_{\boldsymbol{H}} \begin{bmatrix} v_{\alpha,1}(t) \\ v_{\beta,1}(t) \end{bmatrix}. \tag{2.42}$$

Multiplying both sides of (2.42) by the inverse of $\boldsymbol{H}$ results in

$$\begin{bmatrix} v_{\alpha,1}(t) \\ v_{\beta,1}(t) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & \cot(\tau\omega_g/2) \\ -\cot(\tau\omega_g/2) & 1 \end{bmatrix} \begin{bmatrix} v_\alpha(t) - v_\alpha(t-\tau) \\ v_\beta(t) - v_\beta(t-\tau) \end{bmatrix}. \tag{2.43}$$

The equation (2.43) describes the proposed method for rejecting the DC offset in the input of three-phase PLLs. The application of this method to the conventional SRF-PLL is observed in Fig. 2.25. The resultant structure is briefly referred to as the DC immune PLL (DCI-PLL). Notice that the frequency-dependent term in (2.43) is calculated using a frequency feedback loop to make the method robust to the grid frequency variations.

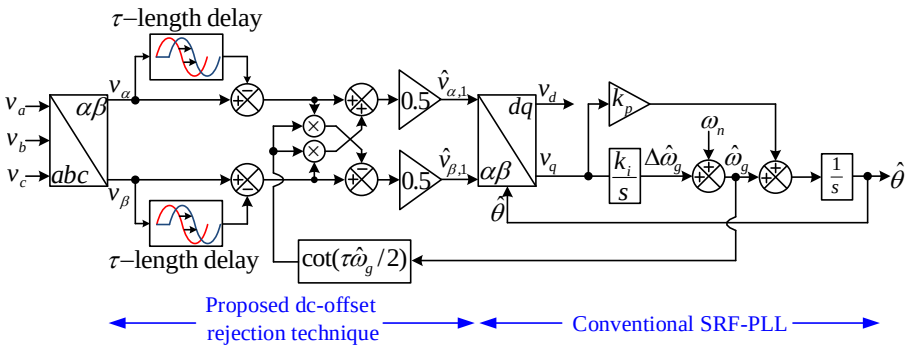

Fig. 2.25: A conventional SRF-PLL with the proposed DC-offset rejection method. It is briefly called the DCI-PLL [99].

2.3.2. MODELING, TUNING, AND STABILITY ANALYSIS

Considering (2.40) as the DCI-PLL input signals in the stationary frame, the signals $\hat{v}_{\alpha,1}$ and $\hat{v}_{\beta,1}$ in Fig. 2.25 can be obtained as

$$\begin{aligned}\hat{v}_{\alpha,1}(t) &= \frac{V}{2}\left\{\cos(\theta)-\cos(\theta-\tau\omega_g)+\cot(\tau\hat{\omega}_g/2)[\sin(\theta)-\sin(\theta-\tau\omega_g)]\right\}\\ \hat{v}_{\beta,1}(t) &= \frac{V}{2}\left\{\sin(\theta)-\sin(\theta-\tau\omega_g)-\cot(\tau\hat{\omega}_g/2)[\cos(\theta)-\cos(\theta-\tau\omega_g)]\right\}.\end{aligned} \tag{2.44}$$

Transferring these signals to the *dq*-frame gives the PI regulator input in Fig. 2.25 as

$$v_q(t)=\frac{V}{2}\left\{\cot(\tau\hat{\omega}_g/2)[\cos(\theta-\hat{\theta}-\tau\omega_g)-\cos(\theta-\hat{\theta})]-\sin(\theta-\hat{\theta}-\tau\omega_g)+\sin(\theta-\hat{\theta})\right\}. \tag{2.45}$$

The equation (2.45) under a quasi-locked state can be approximated by

$$v_q(t)\approx V\left[\frac{\tau\Delta\hat{\omega}_g}{2}-\Delta\hat{\theta}+\frac{\Delta\theta+\left(\Delta\theta-\tau\Delta\omega_g\right)}{2}\right] \tag{2.46}$$

or equivalently in the Laplace domain by

$$v_q(s)\approx V\left[\frac{\tau\Delta\hat{\omega}_g(s)}{2}-\Delta\hat{\theta}(s)+\frac{1+e^{-\frac{\tau}{2}s}}{2}\Delta\theta(s)\right]. \tag{2.47}$$

Using (2.47) and the DCI-PLL structure in Fig. 2.25, its model can be readily achieved as shown in Fig. 2.26.

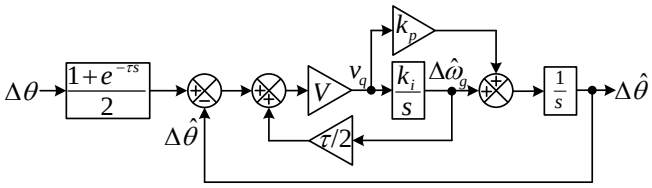

Fig. 2.26: Small-signal model of the DCI-PLL [99].

According to this model, the closed-loop transfer function may be obtained as

$$G_{cl}(s)=\frac{0.5V\left(1+e^{-\tau s}\right)(k_p s+k_i)}{s^2+V(k_p-k_i\tau/2)s+Vk_i}. \tag{2.48}$$

Using this transfer function and the Routh-Hurwitz criterion, it can be shown that the DCI-PLL remains stable if $k_p > k_i\tau/2$.

For selecting the control parameters of the DCI-PLL, we have to select the delay length τ in the DC-offset rejection stage first. Notice that the steady-state operation of this stage in blocking the DC component is independent of the delay length τ. To be more exact, for any value of τ, the proposed method totally rejects the grid voltage DC component in the steady state. This delay length, however, affects the high-frequency noise immunity and the dynamic performance of the PLL and, therefore, one has to find a satisfactory compromise. Here, $\tau = T/10$ is chosen.

Once the delay length is chosen, the following definitions are made and k_p and k_i are determined based on choosing proper values for the damping factor and the natural frequency of the closed-loop poles.

$$\begin{aligned} &V(k_p-k_i\tau/2)=2\zeta\omega_n' \\ &Vk_i=(\omega_n')^2 \end{aligned} \tag{2.49}$$

Here, $\omega_n'=2\pi 20$ rad/s and $\zeta=1/\sqrt{2}$ are considered, which result in $k_p=193.5$ and $k_i=15791$.

2.3.3. NUMERICAL RESULTS

In this section, the DCI-PLL performance is investigated and compared with the performance of an $\alpha\beta$DSC-PLL with the delay factor 2 [36]. The same natural frequency and damping factor as those of the DCI-PLL are considered for the case of the $\alpha\beta$DSC-PLL to ensure a fair condition for the comparison.

Figs. 2.27(a) and (b) demonstrate the obtained results of the performance comparison between the DCI-PLL and $\alpha\beta$DSC-PLL in response to decaying DC components and a $+20°$ phase jump, respectively. It can be observed that both PLLs effectively reject the DC component. The DCI-PLL, however, offers a faster dynamic behavior.

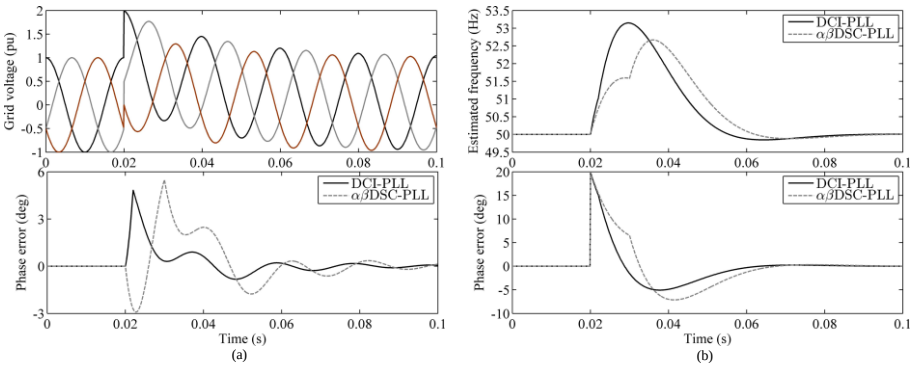

Fig. 2.27: Performance comparison between the DCI-PLL and $\alpha\beta$DSC-PLL in the presence (a) decaying DC components, and (b) a $+20°$ phase jump [99].

2.4. PLL WITH A MAF BASED PREFILTERING STAGE

A brief review of a three-phase PLL which uses a prefilter based on the MAF was conducted before. It was discussed that the main problem of this structure, which is briefly called the PMAF-PLL, is the requirement for a parallel frequency detector for adapting its prefilter to the changes in the grid frequency (See Fig. 1.6). The main aim of this section is presenting a simple yet effective approach to eliminate the need for a parallel frequency detector in the PMAF-PLL. The modeling, tuning and the performance assessment of the resultant structure, which is called the enhanced PMAF-PLL, is also briefly presented. It should be mentioned that the content of this section is based on the reference [100] (Paper 8 in Appendix).

2.4.1. ELIMINATING THE NEED FOR A PARALLEL FREQUENCY DETECTOR

Fig. 2.28 illustrates the block diagram representation of the PMAF-PLL without its parallel frequency detector.

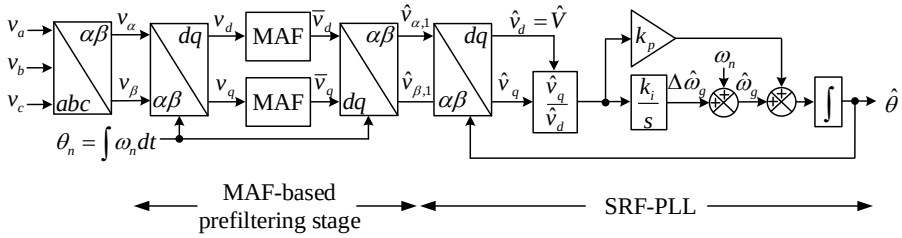

Fig. 2.28: PMAF-PLL without its parallel frequency detector [100].

From Fig. 2.28, the transfer function relating the output of the prefiltering stage to its input in the $\alpha\beta$ frame can be expressed in the Laplace domain as

$$\frac{\hat{v}_{\alpha,1}(s)+j\hat{v}_{\beta,1}(s)}{v_\alpha(s)+jv_\beta(s)}=G_{\mathrm{MAF}}(s-j\omega_n) \tag{2.50}$$

which is corresponding in the *z*-domain to

$$\frac{\hat{v}_{\alpha,1}(z)+j\hat{v}_{\beta,1}(z)}{v_\alpha(z)+jv_\beta(z)}=G_{\mathrm{MAF}}(ze^{-j\omega_n T_s}). \tag{2.51}$$

Considering the MAF transfer function in the *z*-domain as (2.52), where *N* is the number of samples within its window length, the frequency response of (2.51) at the fundamental frequency, i.e., $z=e^{j\omega_g T_s}$, can be obtained as (2.53).

$$G_{MAF}(z)=\frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}=\frac{1}{N}\sum_{m=0}^{N-1}z^{-m} \tag{2.52}$$

$$G_{\mathrm{MAF}}(z=e^{j\Delta\omega_g T_s})\approx|1-\underbrace{(T_w^2/24)}_{k_v}\Delta\omega_g^2|\angle-\underbrace{0.5(T_w-T_s)}_{k_\varphi}\Delta\omega_g \tag{2.53}$$

In (2.53), $T_w=NT_s$ is the window length of the MAF.

Equation (2.53) demonstrates that the PMAF-PLL (Fig. 2.28) suffers from a phase offset error equal to $-k_\varphi\Delta\omega_g$ and an amplitude scaling error equal to $1-k_v\Delta\omega_g^2$. As shown in Fig. 2.29, the amplitude scaling error can be simply corrected by dividing the estimated amplitude by an estimation of $1-k_v\Delta\omega_g^2$. The phase offset error may also be compensated by adding an estimation of the same phase error to the rotating angle of the SRF-PLL Park's transformation. In this way, the need for a parallel frequency is removed, and a more compact yet effective structure is obtained. The resultant PLL is called the enhanced PMAF-PLL.

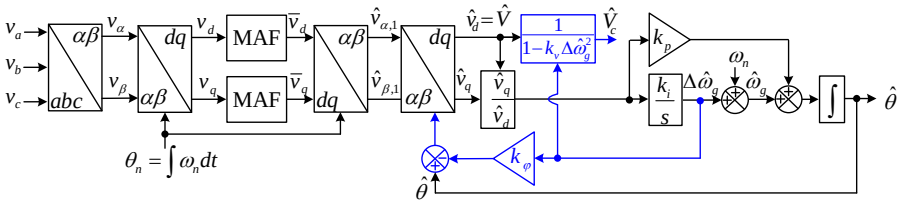

Fig. 2.29: Proposed enhanced PMAF-PLL [100].

2.4.2. MODELING AND TUNING

Performing the modeling procedure of the proposed enhanced PMAF-PLL in the *s*-domain is complicated. Therefore, it is conducted in the *z* domain here.

Assume that the $\alpha\beta$-axis input signals are as follows

$$\begin{aligned} v_\alpha(k) &= V\cos\left(\theta(k)\right) \\ v_\beta(k) &= V\sin\left(\theta(k)\right) \end{aligned} \tag{2.54}$$

in which k means the current sample. Based on (2.52) and (2.54), the MAFs output signals in Fig. 2.29 may be expressed as

$$\begin{aligned} \bar{v}_d(k) &= \frac{V}{N}\sum_{m=0}^{N-1}\cos\left(\Delta\theta(k-m)\right) \\ \bar{v}_q(k) &= \frac{V}{N}\sum_{m=0}^{N-1}\sin\left(\Delta\theta(k-m)\right) \end{aligned} \tag{2.55}$$

where $\Delta\theta=\theta-\theta_n$.

Transferring back these signals to the $\alpha\beta$ frame and then again to the dq frame as shown in Fig. 2.29 gives the signal $\hat{v}_q$ in the enhanced PMAF-PLL as

$$\begin{aligned} \hat{v}_q(k) &= \frac{V}{N}\sum_{m=0}^{N-1}\underbrace{\sin\left(\Delta\theta(k-m)-\Delta\hat{\theta}(k)+k_\varphi\Delta\hat{\omega}_g(k)\right)}_{\approx\left(\Delta\theta(k-m)-\Delta\hat{\theta}(k)+k_\varphi\Delta\hat{\omega}_g(k)\right)} \\ &\approx \frac{V}{N}\left[\sum_{m=0}^{N-1}\Delta\theta(k-m)\right]-V\Delta\hat{\theta}(k)+Vk_\varphi\Delta\hat{\omega}_g(k). \end{aligned} \tag{2.56}$$

Applying the *z*-transform to both sides of (2.56) results in

$$\hat{v}_q(z) \approx \underbrace{\frac{1}{N}\left[\sum_{m=0}^{N-1} z^{-m}\right]}_{G_{MAF}(z)} V\Delta\theta(z) - V\Delta\hat{\theta}(z) + Vk_\varphi\Delta\hat{\omega}_g(z). \tag{2.57}$$

In the *s*-domain, we have

$$\hat{v}_q(s) \approx V\left[G_{MAF}(s)\Delta\theta(s) - \Delta\hat{\theta}(s) + k_\varphi\Delta\hat{\omega}_g(s)\right]. \tag{2.58}$$

Considering (2.58) and the amplitude normalization before the PI regulator in Fig. 2.29, the small signal model of the enhanced PMAF-PLL may be obtained as shown in Fig. 2.30. Fig. 2.31 confirms the high accuracy of this model.

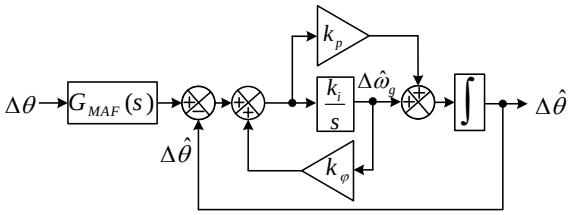

Fig. 2.30: Enhanced PMAF-PLL model [100].

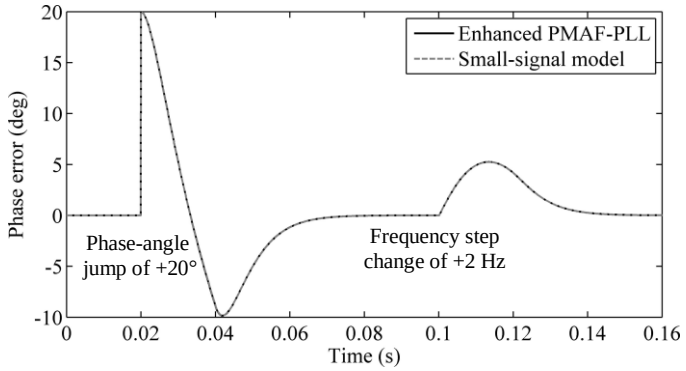

Fig. 2.31: Enhanced PMAF-PLL model accuracy assessment using typical tests [100].

For tuning the control parameters of the enhanced PMAF-PLL, the closed-loop transfer function is obtained from its model as

$$G_{cl}(s) = \underbrace{\frac{1-e^{-T_w s}}{T_w s}}_{G_{MAF}(s)} \frac{k_p s + k_i}{s^2 + \left(k_p - k_\varphi k_i\right)s + k_i}. \tag{2.59}$$

According to this transfer function and by defining $k_p - k_\varphi k_i = 2\zeta\omega_n'$ and $k_i = \omega_n'^2$,

the proportional and integral gains can be expressed as $k_i = \omega_n'^2$ and $k_p = 2\zeta\omega_n' + k_\varphi\omega_n'^2$ and, therefore, be determined by selecting ζ and ω_n'. Here, the selected values are $\omega_n' = 2\pi 32$ rad/s and $\zeta = 1$, which are corresponding to $k_i = 40426$ and $k_p = 804$.

2.4.3. EXPERIMENTAL RESULTS

In this section, some dSPACE-based comparative experimental tests are conducted to highlight the good performance of the enhanced PMAF-PLL. The quasi-type-1 PLL (QT1-PLL) and standard MAF-PLL [39] are selected for the comparison. Figs. 2.32 and 2.33 illustrate the obtained results in response to a frequency jump test and a harmonically distorted grid scenario. From the dynamic performance point of view, it can be observed that the enhanced PMAF-PLL offers the best performance. The QT1-PLL transient response is close to that of the proposed PLL and the standard MAF-PLL has a very sluggish dynamic response. In rejecting the grid voltage disturbances under an off-nominal frequency, the standard MAF-PLL and the enhanced PMAF-PLL have the best and second best performances, respectively. It should be emphasized here that when the grid frequency is close to the nominal value, as it is often the case, the disturbance rejection capability of the proposed PLL will be as good as that of the standard MAF-PLL.

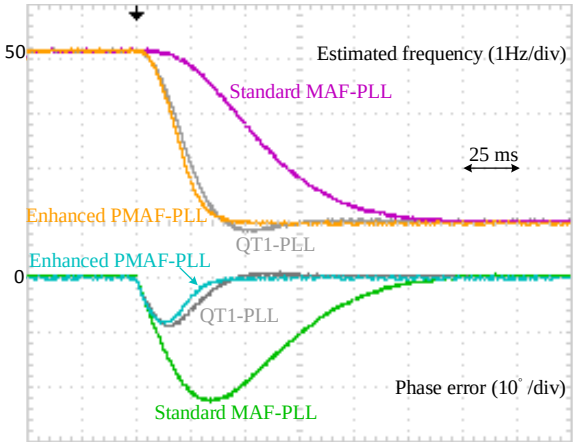

Fig. 2.32: A -3 Hz frequency jump test [100].

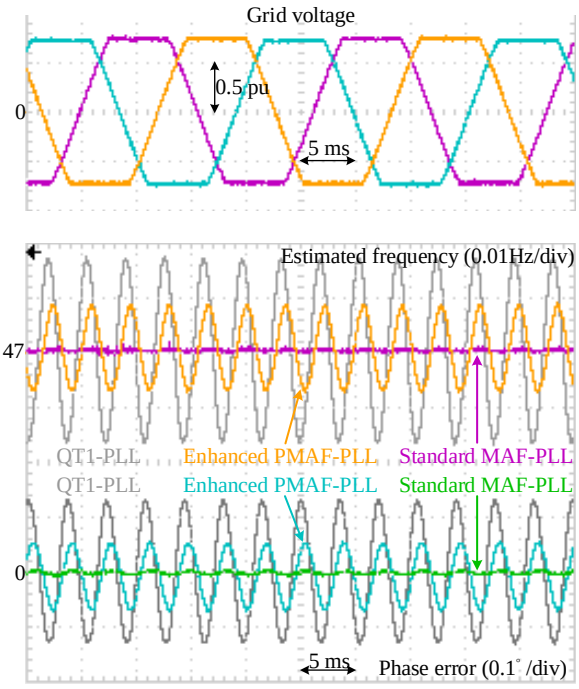

Fig. 2.33: A harmonically-distorted grid scenario. The frequency is fixed at – 47 Hz [100].

CHAPTER 3. MODELING, ANALYZING, AND DESIGNING FLLS

The main objectives of this section are deriving small-signal models for the standard and advanced FLLs, introducing the concept of inloop filter for designing more efficient FLLs, demonstrating the relation between FLLs and PLLs, and designing an adaptive resonant controller based on the FLL concept for single-phase grid-tied power converters.

3.1. SINGLE-PHASE FLLS

In this section, modeling, tuning, and performance assessment of the SOGI-FLL (which is a standard single-phase FLL) and its advanced versions are briefly presented. The content of this section is based on the reference [101] (Paper 9 in Appendix).

3.1.1. MODELING

Fig. 3.1 illustrates the block diagram representation of the SOGI-FLL, SOGI-FLL with prefilter (SOGI-FLL-WPF), and SOGI-FLL with inloop filter (SOGI-FLL-WIF), also known as the FOGI-FLL. The operating principles of these FLLs have been described before in Section 1.1.2.1. Therefore, it is not explained again to save the space.

First, a small-signal model for the SOGI-FLL is derived and it is then extended to its advanced versions. To this end, its single-phase input signal and its α- and β-axis outputs are considered as

$$v(t) = v_{\alpha}(t) = V\cos(\theta) \tag{3.1}$$

$$\hat{v}_{\alpha}(t) = \hat{V}\cos(\hat{\theta}) \tag{3.2}$$

$$\hat{v}_{\beta}(t) = \hat{V}\sin(\hat{\theta}) \tag{3.3}$$

where V and θ are the actual values of the grid voltage amplitude and phase angle, respectively, and $\hat{V}$ and $\hat{\theta}$ are their estimations.

According to the SOGI-FLL structure, the following equations may be easily obtained.

$$\dot{\hat{v}}_{\alpha} = \hat{\omega}_g\left[-\hat{v}_{\beta} + k\left(v_{\alpha} - \hat{v}_{\alpha}\right)\right] \tag{3.4}$$

$$\dot{\hat{v}}_{\beta} = \hat{\omega}_g\hat{v}_{\alpha} \tag{3.5}$$

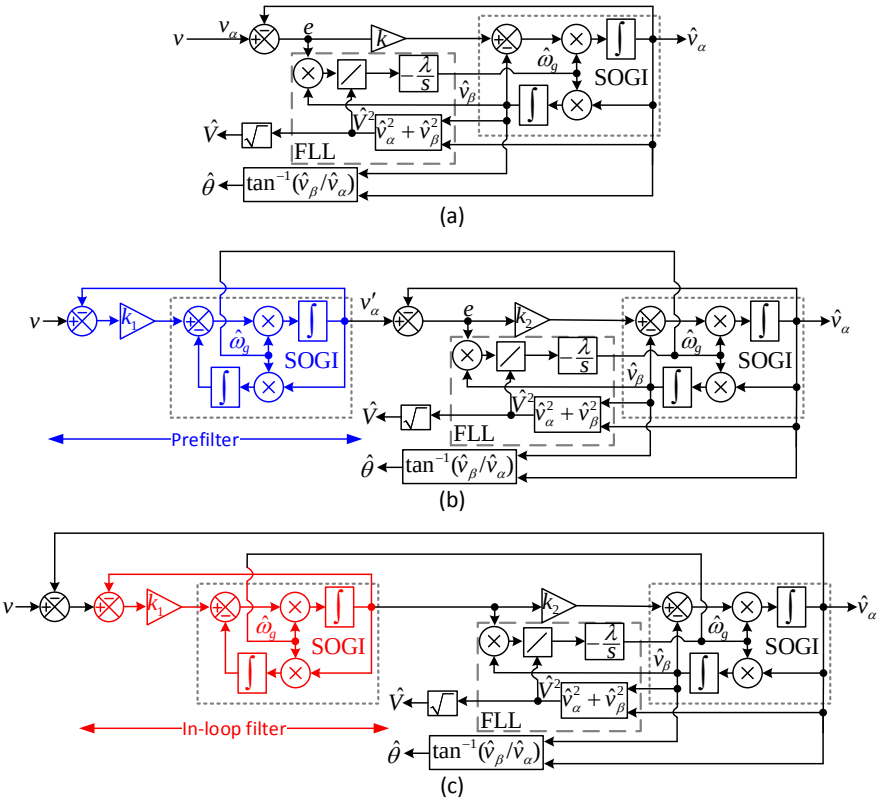

Fig. 3.1: Block diagram representation of (a) the SOGI-FLL, (b) the SOGI-FLL-WPF, and (c) the SOGI-FLL-WIF (also known as the FOGI-FLL) [101].

$$\dot{\hat{\omega}}_g = -\frac{\lambda}{\hat{V}^2}\hat{v}_\beta\left(v_\alpha - \hat{v}_\alpha\right) \tag{3.6}$$

$$\hat{\theta} = \tan^{-1}\left(\frac{\hat{v}_\beta}{\hat{v}_\alpha}\right) \tag{3.7}$$

$$\hat{V} = \sqrt{\hat{v}_\alpha^2 + \hat{v}_\beta^{\,2}}. \tag{3.8}$$

To derive a small-signal model for the SOGI-FLL, we have to find the linear differential equations describing the dynamics of the SOGI-FLL in the estimation of phase, frequency, and amplitude.

Substituting (3.2) and (3.3) into (3.6) gives

$$\dot{\hat{\omega}}_g = \frac{\lambda}{2\hat{V}}[\overbrace{\hat{V}\sin(2\hat{\theta})-V\sin(\theta+\hat{\theta})}^{\approx 0}+V\overbrace{\sin(\theta-\hat{\theta})}^{\approx(\theta-\hat{\theta})}] \approx \frac{\lambda}{2}(\theta-\hat{\theta}). \tag{3.9}$$

By differentiating from (3.7) and (3.8) and using equations (3.1)-(3.6), we may also obtain the following differential equations

$$\dot{\hat{\theta}} = \frac{\dot{\hat{v}}_\beta \hat{v}_\alpha - \dot{\hat{v}}_\alpha \hat{v}_\beta}{\hat{V}^2} = \hat{\omega}_g - \frac{k\hat{\omega}_g \overbrace{\hat{v}_\beta (v_\alpha - \hat{v}_\alpha)}^{-\hat{V}^2\dot{\hat{\omega}}_g/\lambda}}{\hat{V}^2} = \hat{\omega}_g + \frac{k\hat{\omega}_g}{\lambda}\dot{\hat{\omega}}_g \approx \hat{\omega}_g + \frac{k\omega_n}{\lambda}\dot{\hat{\omega}}_g \tag{3.10}$$

$$\begin{aligned}\dot{\hat{V}} &= \frac{\hat{v}_\alpha \dot{\hat{v}}_\alpha + \hat{v}_\beta \dot{\hat{v}}_\beta}{\hat{V}} = \frac{k\hat{\omega}_g \hat{v}_\alpha (v_\alpha - \hat{v}_\alpha)}{\hat{V}} \\ &= \frac{k\hat{\omega}_g}{2}[\overbrace{V\cos(\theta+\hat{\theta})-\hat{V}\cos(2\hat{\theta})}^{\approx 0}+V\overbrace{\cos(\theta-\hat{\theta})}^{\approx 1}-\hat{V}] \approx \frac{k\omega_n}{2}(V-\hat{V}).\end{aligned} \tag{3.11}$$

Based on (3.9)-(3.11), the SOGI-FLL model may be obtained as depicted in Fig. 3.2(a). Following a similar procedure as before, the SOGI-FLL-WPF and SOGI-FLL-WIF models can also be achieved as shown in Figs. 3.2(b) and (c). It can be demonstrated that all these models predict the average behavior of their corresponding FLLs with a high accuracy.

3.1.2. TUNING

For the case of the SOGI-FLL, tuning the control parameters is carried out based on the closed-loop transfer function relating the actual and estimated phase angle. This transfer function can be obtained using Fig. 3.2(a) as

$$\hat{\theta}(s) = \frac{(k\omega_n/2)s + \lambda/2}{s^2 + \underbrace{(k\omega_n/2)}_{2\zeta\omega_n'}s + \underbrace{(\lambda/2)}_{(\omega_n')^2}}\theta(s). \tag{3.12}$$

According to (3.12) and selecting an optimum damping factor $\zeta = 1/\sqrt{2}$, the FLL gain λ can be expressed as a function of the SOGI gain k as

$$\lambda = \frac{\omega_n^2 k^2}{8\zeta^2} = \frac{\omega_n^2 k^2}{4}. \tag{3.13}$$

Therefore, selecting k determines both parameters of the SOGI-FLL. Typically, $k = \sqrt{2}$ is recommended in the literature. However, as here the intention is performing a comparison between the SOGI-FLL and its advanced versions, $k = 1/\sqrt{2}$ is chosen. It will be demonstrated later that this section results in a fair condition for the comparison. With this selection, the FLL gain λ of the SOGI-FLL will be equal to $\lambda = 12337$.

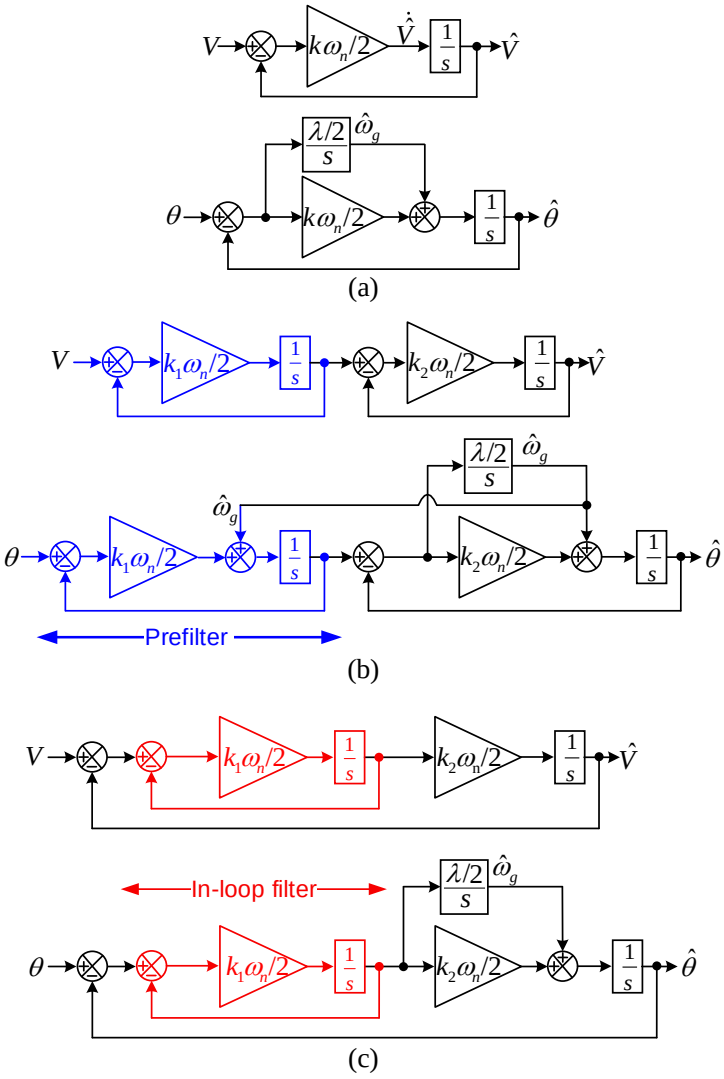

Fig. 3.2: Small-signal model of (a) the SOGI-FLL, (b) SOGI-FLL-WPF, and (c) SOGI-FLL-WIF [101].

For the case of the SOGI-FLL-WPF, the first step in the tuning procedure is optimizing the performance of its prefilter. By obtaining the transfer function relating the input and output signals of the prefilter in Fig. 3.1(b), it can be shown that $k_1 = \sqrt{2}$ is the best choice as it results in an optimum tradeoff between the settling-time and overshoot in the extraction of the grid voltage fundamental component. On the other hand, according to the following closed-loop transfer

function, which can be obtained from Fig. 3.2(b), it can be concluded that k_2 should be equal to k_1, i.e., $k_2 = k_1 = \sqrt{2}$, otherwise it results in an over-damped dynamic response.

$$\hat{V}(s) = \frac{(k_1\omega_n/2)(k_2\omega_n/2)}{(s+k_1\omega_n/2)(s+k_2\omega_n/2)}V(s) \tag{3.14}$$

Now, according to (3.15), which describes the characteristic polynomial of the closed-loop transfer function relating θ to $\hat{\theta}$ in Fig. 3.2(b), and considering the selected values for k_1 and k_2, the FLL gain λ can be expressed as (3.16).

$$s^3 + \left[\omega_n(k_1+k_2)/2\right]s^2 + \left[\omega_n^2 k_1 k_2/4\right]s + \omega_n k_1 \lambda/4 = \left[s+\gamma\omega_n'\right]\left[s^2 + 2\zeta\omega_n' s + (\omega_n')^2\right] \tag{3.15}$$

$$\lambda = \frac{2(\zeta+1)\omega_n^2}{(2\zeta+1)^3}. \tag{3.16}$$

Selecting an optimum damping factor $\zeta = 1/\sqrt{2}$ gives the FLL gain λ in the SOGI-FLL-WPF equal to $\lambda = 23948$.

Regarding the SOGI-FLL-WIF, the open-loop transfer function relating the phase error to the estimated phase angle in Fig. 3.2(c) is obtained and used for the tuning procedure. This transfer function is as follows

$$G_{ol}(s) = \frac{\hat{\theta}(s)}{\theta(s)-\hat{\theta}(s)} = \frac{(k_1\omega_n/4)\left[(k_2\omega_n)s+\lambda\right]}{s^2(s+k_1\omega_n/2)}. \tag{3.17}$$

Applying the SO method to (3.17) yields

$$\begin{aligned} k_1 &= \frac{2b\omega_c}{\omega_n} \\ k_2 &= \frac{2\omega_c}{\omega_n} \\ \lambda &= \frac{2\omega_c^2}{b} \end{aligned} \tag{3.18}$$

where *b*, as mentioned before, is the PM determining factor and ω_c is the crossover frequency. $b = 1+\sqrt{2}$ (which is corresponding to $\mathrm{PM} = 45°$ and an optimum damping factor $1/\sqrt{2}$ for the closed-loop poles) and $\omega_c = 2\pi 18.8$ rad/s (which is equal to the crossover frequency of the SOGI-FLL-WPF) are selected here. These selections, according to (3.18), give $k_1 = 1.815$, $k_2 = 0.752$, and $\lambda = 11559$.

3.1.3. PERFORMANCE COMPARISON

The aim of this part is conducting a performance comparison between the SOGI-FLL and its advanced versions to provide an insight into their advantages and disadvantages.
Fig. 3.3 compares the open-loop Bode plots of the SOGI-FLL, SOGI-FLL-WPF, and SOGI-FLL-WIF. As shown, all of them have a very close crossover response, which implies that the selected control parameters and, hence, the condition of comparison are fair. It also indicates that all these FLLs provide a close speed of response during transients. It can also be observed that the SOGI-FLL provides a higher PM compared to the other structures, which means that it offers a smoother dynamic behavior. Fig. 3.4(a), which demonstrates the obtained experimental results in response to a phase jump with a voltage sag, confirms all these theoretical predictions.

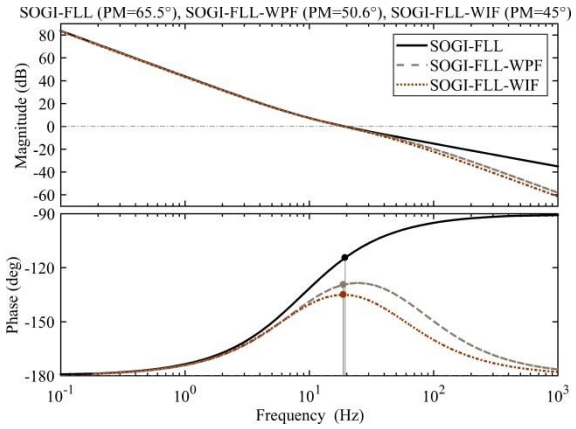

Fig. 3.3: Open-loop Bode plots [101].

Fig. 3.4(b) compares the performance of the SOGI-FLL and its advanced versions under harmonically-distorted grid conditions. It can be observed that the SOGI-FLL-WPF and SOGI-FLL-WIF offer a rather better harmonic filtering capability compared to the SOGI-FLL. It can also be shown that the SOGI-FLL is highly sensitive to the grid voltage DC component and subharmonics and suffers from large oscillatory errors in the presence of these disturbances. The SOGI-FLL-WPF and SOGI-FLL-WIF, however, effectively suppress these disturbances.

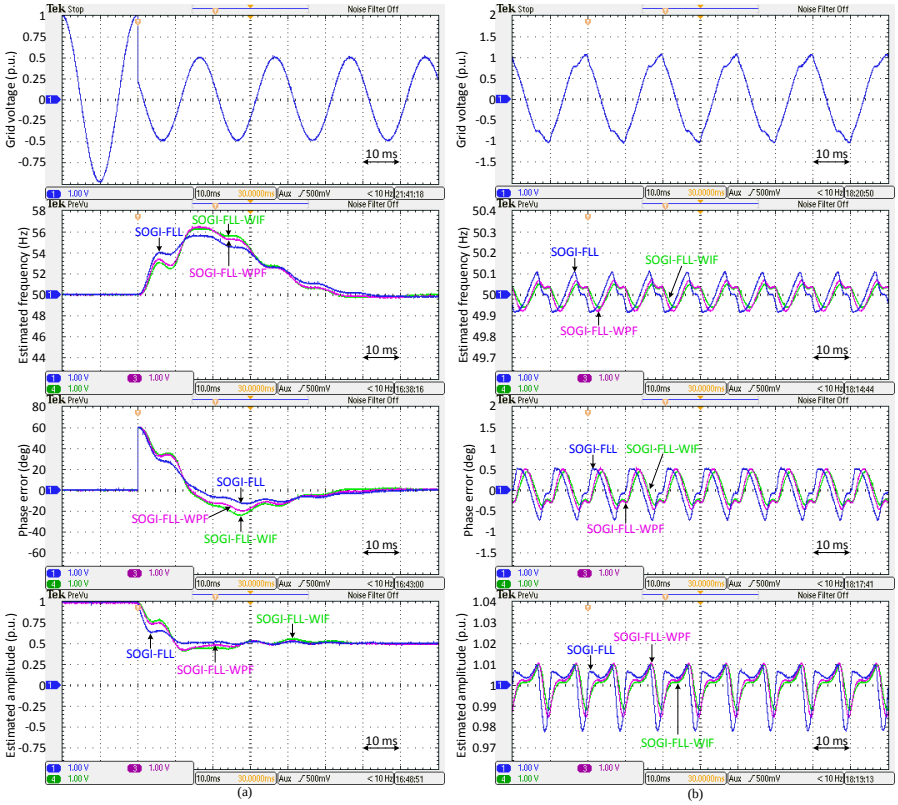

Fig. 3.4 Performance comparison between the SOGI-FLL, SOGI-FLL-WPF, and SOGI-FLL-WIF under (a) a 0.5 p.u. voltage sag with 60° phase jump, and (b) a harmonically-distorted grid condition [101].

3.2. THREE-PHASE FLLS

In this section, the concept of inloop filter for developing advanced three-phase FLLs is first introduced. Some design examples are presented and the modeling procedure of three-phase FLLs in the presence of an inloop filter is demonstrated. Finally, it is demonstrated that the FLLs and PLLs are equivalent systems in different reference frames. It should be mentioned here that the content of this section is based on reference [102] (Paper 10 in Appendix).

3.2.1. CONCEPT OF INLOOP FILTER

The operating principle of a standard three-phase FLL, called the ROGI-FLL, was already described in Section 1.1.2.2. The block diagram of this FLL, for the sake of convenience, is shown again in Fig. 3.5.

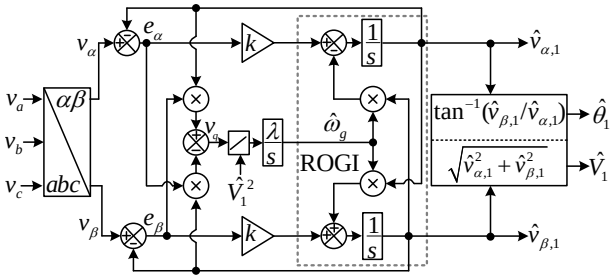

Fig. 3.5: Block diagram of the standard three-phase FLL, which is called the ROGI-FLL [102].

The equation (3.19) describes the transfer function relating the extracted fundamental component by the ROGI-FLL to its input signals in the space vector notation.

$$\frac{\hat{v}_{\alpha,1}(s)+j\hat{v}_{\beta,1}(s)}{v_\alpha(s)+jv_\beta(s)}=G_{\alpha\beta}(s)=\frac{k}{s-j\hat{\omega}_g+k} \tag{3.19}$$

As shown, this transfer function is a first-order complex bandpass filter (CBF). The ROGI-FLL disturbance rejection ability may be enhanced by considering a narrow bandwidth for this CBF. It, however, would be at the cost of a sluggish dynamic behavior.

To improve the ROGI-FLL filtering capability, the concept of inloop filter is suggested here. The block diagram representation of this concept can be observed in Fig. 3.6. The inloop filter, as shown, acts on the error signals and is responsible for attenuating/rejecting its disturbance components. Therefore, it should be a bandpass-like filter (preferably a complex-coefficient one) with the center frequency at the fundamental frequency. In what follows, some design examples for such an inloop filter is presented.

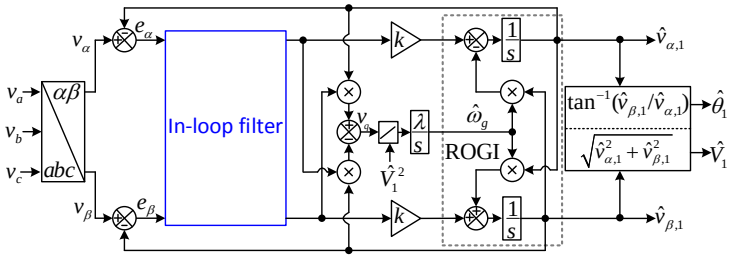

Fig. 3.6: ROGI-FLL with an inloop filter [102].

3.2.1.1 First Design Example: Using *αβ*DSC operators as the ROGI-FLL inloop filter

As the first design example, the application of the *αβ*DSC operators as the ROGI-FLL inloop filter is presented. A typical case where the grid voltage is unbalanced and contains non-triplen odd-harmonics is considered. For this case, two *αβ*DSC operators with the delay factors 4 and 24 are good enough. Fig. 3.7(a) illustrates the application of these operators as the ROGI-FLL inloop filter. This structure is briefly referred to as the DSC-FLL. The small-signal model of this FLL is shown in Fig. 3.7(b). Deriving this model involves finding some linear differential equations for describing the dynamics of the DSC-FLL in the estimation of the phase, frequency, and amplitude. For the sake of brevity, the modeling procedure is not presented here. The details of this procedure can be found in [102].

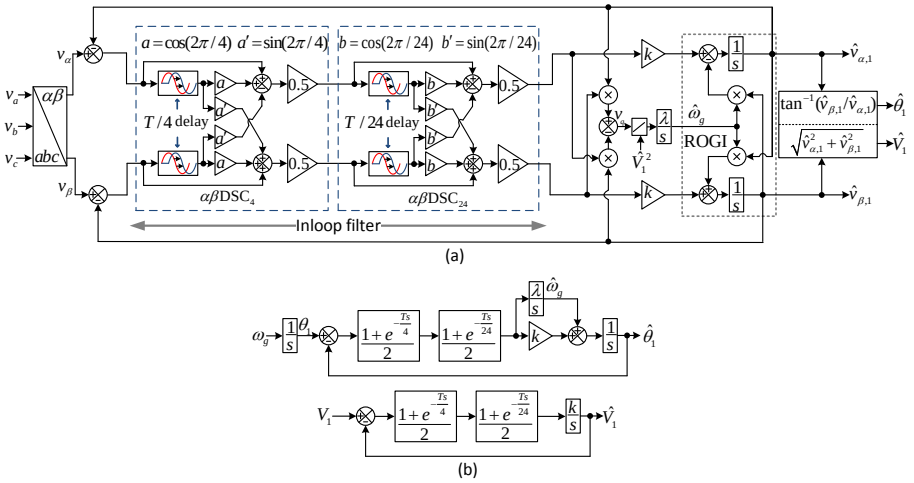

Fig. 3.7: Block diagram representation of (a) the DSC-FLL and (b) its model [102].

Tuning the DSC-FLL parameters can be carried out based on its phase open-loop transfer function, which is as follows

$$G_{ol}(s)=\frac{\hat{\theta}_1(s)}{\theta_1(s)-\hat{\theta}_1(s)}=\frac{1+e^{-\frac{Ts}{4}}}{2}\frac{1+e^{-\frac{Ts}{24}}}{2}\frac{ks+\lambda}{s^2}\approx\underbrace{\frac{1}{(7T/48)s+1}}_{T_d}\frac{ks+\lambda}{s^2}. \tag{3.20}$$

Applying the SO method to this open-loop transfer function gives (3.21), in which b as mentioned before is the PM determining factor.

$$\lambda=\frac{1}{b^3T_d^2}$$
$$k=\frac{1}{bT_d} \tag{3.21}$$

Selecting b=$1+\sqrt{2}$, which corresponds to $PM = 45°$, determines the control parameters as $\lambda = 8354$ and $k = 142$.

3.2.1.2 Second Design Example: Using a CBF as the ROGI-FLL Inloop Filter

As the second design example, a first-order CBF is considered as the ROGI-FLL inloop filter. Fig. 3.8(a) illustrates the block diagram representation of this idea. This structure is briefly called the CBF-FLL. The small-signal model of the CBF-FLL can be observed in Fig. 3.8(b).

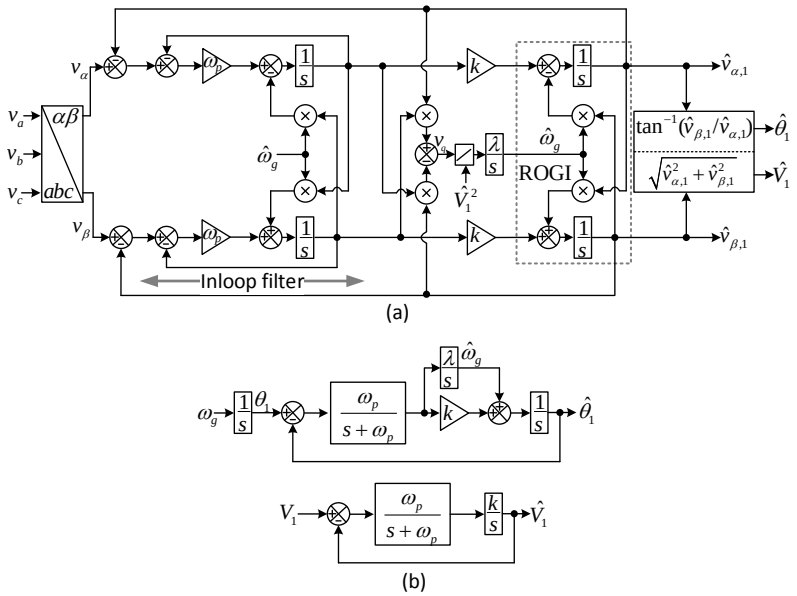

Fig. 3.8: Block diagram representation of (a) the CBF-FLL and (b) its model [102].

Tuning the CBF-FLL parameters, similar to the case of the DSC-FLL, is based on the phase open-loop transfer function. The equation (3.22) describes this transfer function.

$$G_{ol}(s) = \frac{\omega_p}{s+\omega_p}\frac{ks+\lambda}{s^2} \tag{3.22}$$

It can be observed that (3.20) and (3.22) are the same if $\omega_p = 1/T_d$. Therefore, to have a fair condition for the comparison, the same parameters as those of the DSC-FLL are selected for the CBF-FLL. Equation (3.23) summarizes the values of the CBF-FLL control parameters.

$$\omega_p = 1/T_d = 48/(7\,\mathrm{T}) = 343$$
$$k = 142 \qquad (3.23)$$
$$\lambda = 8354.$$

3.2.1.3 Performance Comparison

In this section, to provide an insight into the advantages/disadvantages of using inloop filters in the FLL structure, an experimental performance comparison among the ROGI-FLL, DSC-FLL, and CBF-FLL is conducted. Fig. 3.9(a) illustrates the obtained results in response to 20° phase jump and 0.5 p.u. symmetrical voltage sag. All FLLs have almost the same speed of response. However, the DSC-FLL and CBF-FLL suffer from rather larger overshoots compared to the ROGI-FLL. It implies that an inloop filter reduces the FLL stability margin. This fact can be verified using Bode plots.

Fig. 3.9(b) demonstrates the performance of FLLs under an adverse grid condition. A frequency jump also happens in this test. It can be observed that the CBF-FLL and, particularly, the DSC-FLL offer a much better disturbance rejection capability compared to the ROGI-FLL. Therefore, it can be concluded that an inloop filter can considerably improve the standard FLL filtering capability.

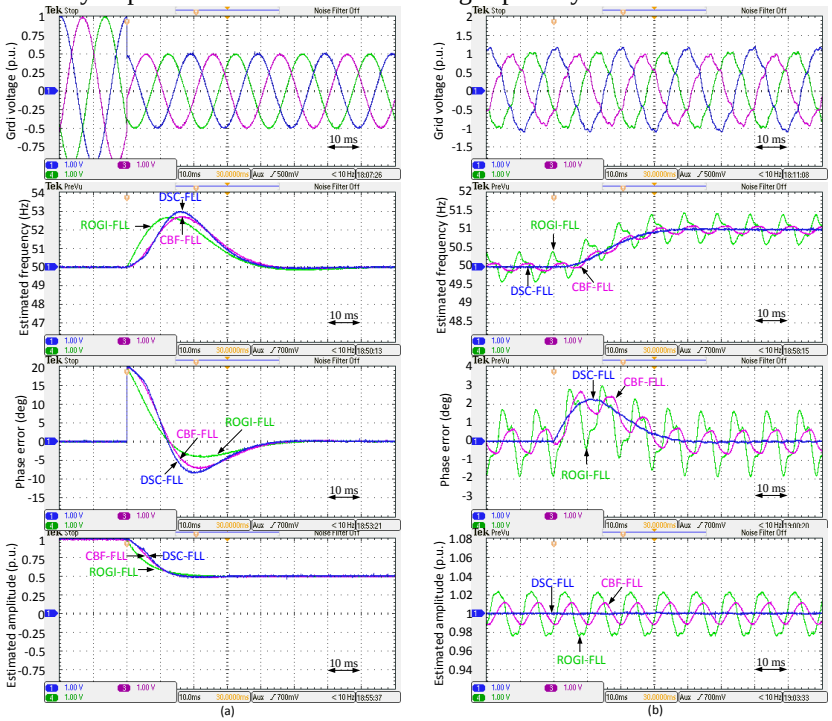

Fig. 3.9: Experimental performance comparison among the ROGI-FLL, DSC-FLL, and CBF-FLL in response to (a) 20° phase jump and 0.5 p.u. symmetrical voltage sag, and (b) a +1-Hz frequency jump under an imbalanced and distorted grid condition [102].

3.2.2. RELATION BETWEEN PLLS AND FLLS

It has already been proved in [5] and briefly discussed in [102] that the ROGI-FLL and the SRF-PLL shown in Fig. 3.10 are equivalent if

- the proportional gain k_p and the LPF cutoff frequency k_v in the *d*-axis of the SRF-PLL are both equal to the CBF cutoff frequency k.
- the integral gain k_i in the SRF-PLL is equal to the FLL gain λ in the ROGI-FLL.

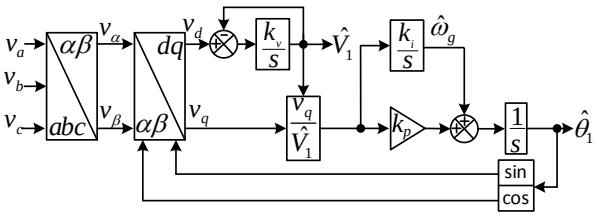

Fig. 3.10: An SRF-PLL [102].

This equivalence suggests that there should be a similar relation between advanced FLLs and PLLs. As an example, consider the CBF-FLL and its model in Fig. 3.8. An SRF-PLL with first-order LPFs in its control loops (see Fig. 3.11) has exactly the same small-signal model as that of the CBF-FLL. This fact suggests that such a PLL, which is briefly called the LPF-PLL, is equivalent to the CBF-FLL, at least from the small-signal point of view. Fig. 3.12, which provides a performance comparison between the CBF-FLL and LPF-PLL, confirms this equivalence. Notice that the small differences between the estimated amplitude of the CBF-FLL and LPF-PLL in some tests are attributable to their amplitude normalization stages.

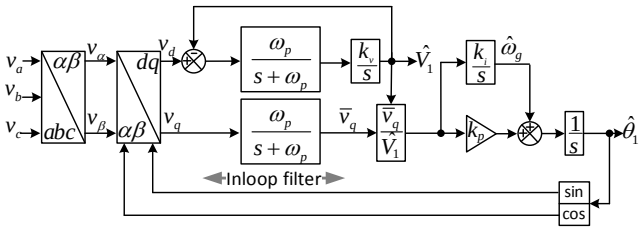

Fig. 3.11: An SRF-PLL with inloop LPF, briefly called the LPF-PLL [102].

In a similar manner, it can be proved that the DSC-FLL is equivalent to the PLL structure shown in Fig. 3.13, which is an SRF-PLL with *dq*-frame DSC (*dq*DSC) operators in its control loops.

The results of this section suggest that FLLs and PLLs are actually the same systems which are implemented in different reference frames.

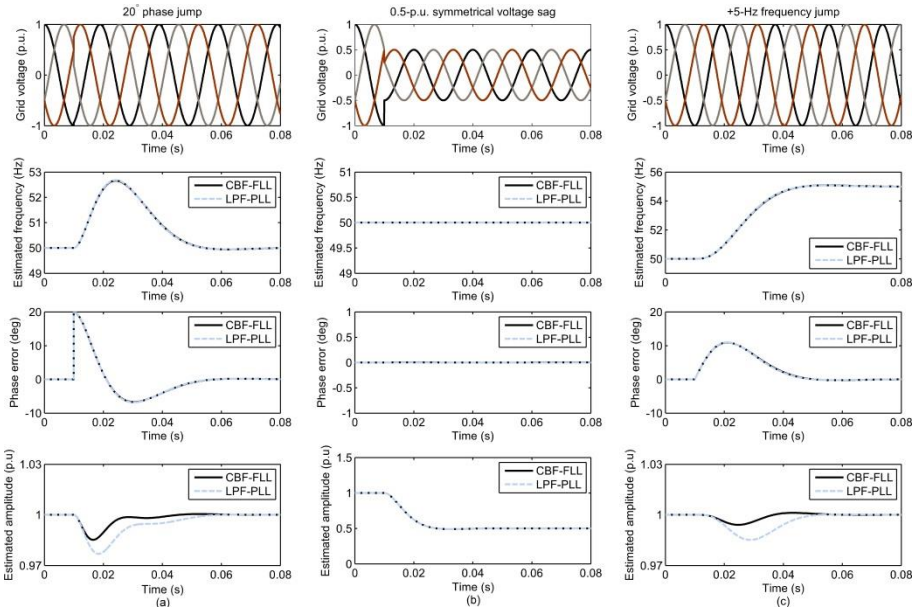

Fig. 3.12: A numerical performance comparison between the CBF-FLL and CBF-FLL under different tests [102].

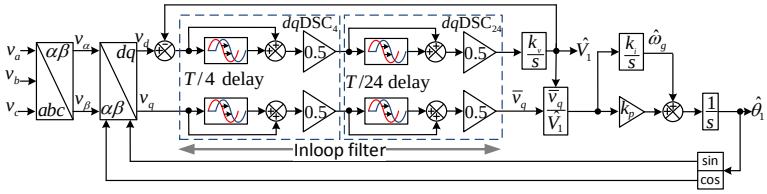

Fig. 3.13: An SRF-PLL with *dq*DSC operators in its control loop [102].

3.3. DESIGNING AN ADAPTIVE RESONANT REGULATOR

Using the resonant regulator is probably the most popular approach for the control of grid-connected current-controlled power converters. This regulator provides an infinite open-loop gain at the fundamental frequency and, therefore, ensures a zero current tracking error. To eliminate the need for a dedicated synchronization technique while maintaining a zero current tracking error under nominal and off-nominal frequencies, an adaptive resonant regulator based on the FLL concept is presented in this section. It should be mentioned here that the content of this section is based on the reference [103] (Paper 11 in Appendix).

3.3.1. DESIGN

Fig. 3.14(a) illustrates a typical proportional-resonant (PR) based current controller, in which a PLL is used for generating the reference current and adapting the center frequencies of the resonant regulators to the grid frequency changes. The harmonics compensator in this structure is responsible for rejecting the disturbance effect of the grid voltage harmonics on the current controller. Fig. 3.14(b) illustrates a second structure in which the reference current is directly generated from the grid voltage as $i_{L,ref} = \kappa v_g$ (κ is the output of the DC-link voltage control loop). As a result, the reference current is synchronized with the grid voltage without using a synchronization unit. This modification makes the current controller more compact. It, however, causes two problems. The first issue is that, in addition to the grid voltage harmonics, the current controller should attenuate/reject the disturbances of the reference current. To tackle this issue, the harmonic compensator and the proportional gain are both connected to the feedback current signal. The second problem is the lack of the information about the grid frequency for adapting the current controller to the grid frequency changes. The aim of this section is solving this issue based on the FLL concept.

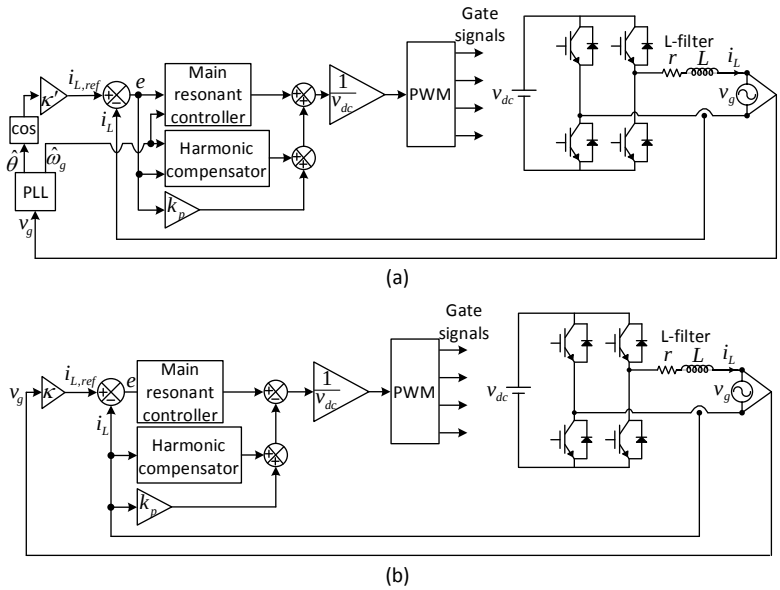

Fig. 3.14: (a) PLL-based and (b) PLL-less PR current controllers for a single-phase grid-connected converter [103].

The structure shown in Fig. 3.15 without its FLL part is exactly the same as the structure shown in Fig. 3.14(b). The main resonant regulator in this structure is similar to the SOGI in the SOGI-FLL [see Fig. 3.1(a)]. Therefore, an FLL similar to

that of the SOGI-FLL may be used for the adapting the center frequencies of the main resonant regulator and the harmonic compensator. This is the basic idea behind the proposed adaptive resonant regulator, which is highlighted in Fig. 3.15.

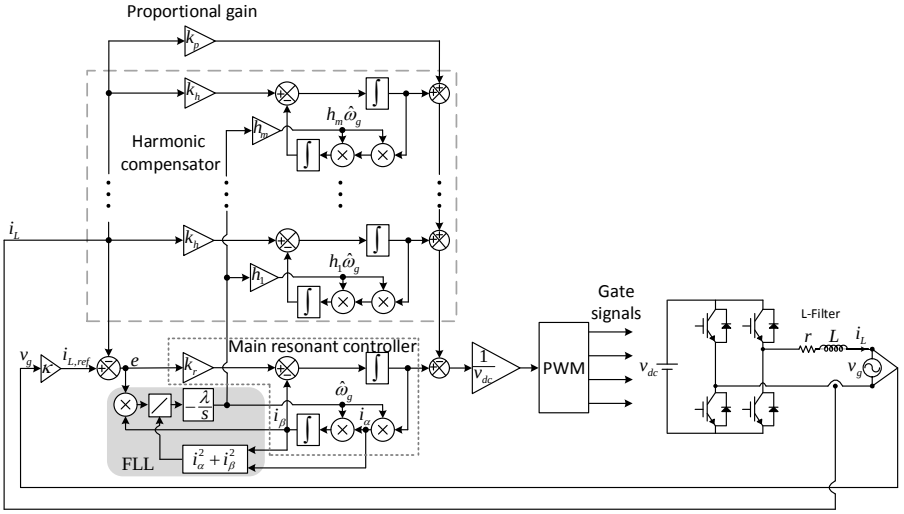

Fig. 3.15: Proposed adaptive resonant current controller. k_p, k_r, and k_h are the proportional gain, main resonant controller gain, and harmonic compensator gain, respectively. It is assumed that $k_r = k_h$ [103].

3.3.2. MODELING AND TUNING

The main objective here is obtaining a simple yet accurate model for describing the dynamics of the proposed controller in estimating the grid frequency. Such a model makes the tuning procedure quite straightforward.

Fig. 3.16(a) illustrates the average model of the structure shown in Fig. 3.15. As the grid voltage disturbance effect is effectively suppressed by the main resonant regulator and harmonic compensator in the steady state, it can be neglected here. The harmonic compensator and the delay are also neglected as they have a small effect on the frequency estimation dynamics. Based on these assumptions, Fig. 3.16(a) can be simplified as Fig. 3.16(b). The transfer function of the dashed box in this structure is as $1/(Ls+r+k_p)$, which is a first-order LPF with a non-unity DC gain. As this LPF has a high cutoff frequency, it can be well approximated by its DC gain. Based on this approximation, Fig. 3.16(c) can be obtained, which is quite similar to the SOGI-FLL. Based on a similar procedure as that described for the SOGI-FLL modeling, the following transfer function for describing the frequency estimation dynamics of the proposed adaptive resonant controller can be obtained.

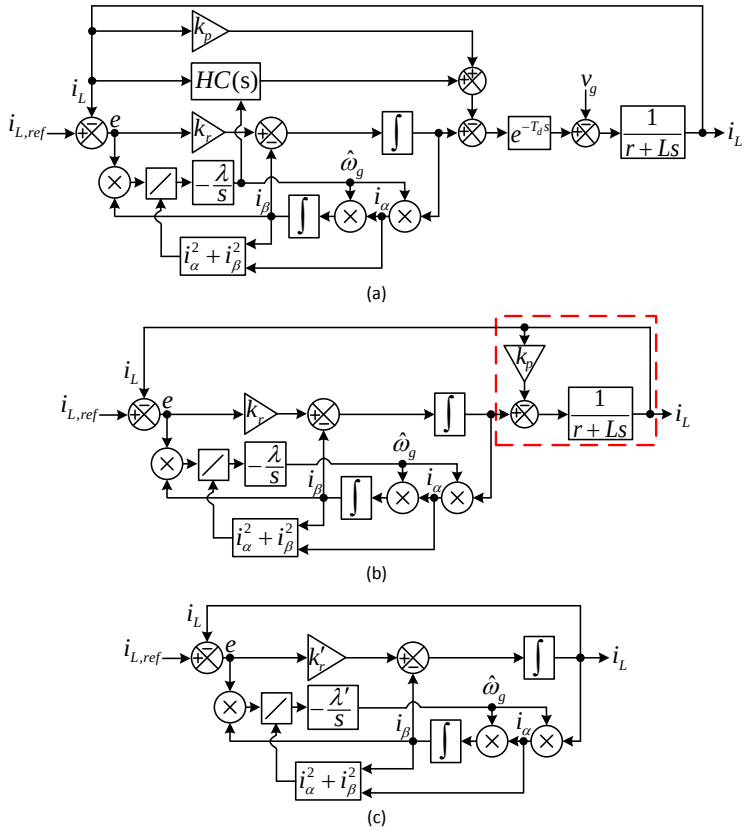

Fig. 3.16: (a) Average model of Fig. 3.15. (b) Simplifying the average model by neglecting the grid voltage disturbance effect, delay, and the harmonic compensator. (c) Further simplifying the average model, by approximating the transfer function of the dashed box by its DC gain. $k_r' = k_r/(k_p + r)$ and $\lambda' = \lambda/(k_p + r)$ [103].

$$\hat{\omega}_g(s) = \frac{\lambda'/(2\omega_n)}{s^2 + \underbrace{(k_r'/2)}_{2\zeta\omega_n'}\, s + \underbrace{\lambda'/(2\omega_n)}_{(\omega_n')^2}}\, \omega_g(s). \tag{3.24}$$

Considering the definitions of k_r' and λ', i.e., $k_r' = k_r/(k_p + r)$ and $\lambda' = \lambda/(k_p + r)$, and also the definitions made in (3.24), we have

$$\begin{aligned} k_r' &= \frac{k_r}{k_p + r} = 4\zeta\omega_n' \quad \Rightarrow \quad k_r = 4\zeta\omega_n'\left(k_p + r\right) \\ \lambda' &= \frac{\lambda}{k_p + r} = 2\omega_n\left(\omega_n'\right)^2 \quad \Rightarrow \quad \lambda = 2\omega_n\left(\omega_n'\right)^2\left(k_p + r\right) \end{aligned} \tag{3.25}$$

in which ω_n and ω_n' are the nominal and natural frequencies, respectively, and ζ is the damping factor. Therefore, after selecting appropriate values for ζ and ω_n', k_r and λ will be only functions of k_p. It means that selecting a value for k_p determines all control parameters. This task can be carried out based on the closed-loop transfer function relating the converter output current to the actual one. The average model shown in Fig. 3.16(a) should be used for this purpose.

3.3.3. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed adaptive resonant controller, some experimental results are presented here. A Danfoss 2.2 kVA converter with an *L* filter in its output is used for this purpose. A Chroma 61845 grid simulator acts as the grid here. The converter is controlled using a dSPACE 1006 platform. As a reference, the structure shown in Fig. 3.14(b), which is here briefly called the standard structure, is also implemented and compared with the proposed controller. The obtained results under a +2 Hz frequency jump test can be observed in Fig. 3.17. As shown in Fig. 3.17(a), the proposed controller estimates the grid frequency fast and, therefore, its current error converges to zero in a short period after the frequency change. However, as can be seen in Fig. 3.17(b), the standard structure suffers from a considerable error after the frequency jump.

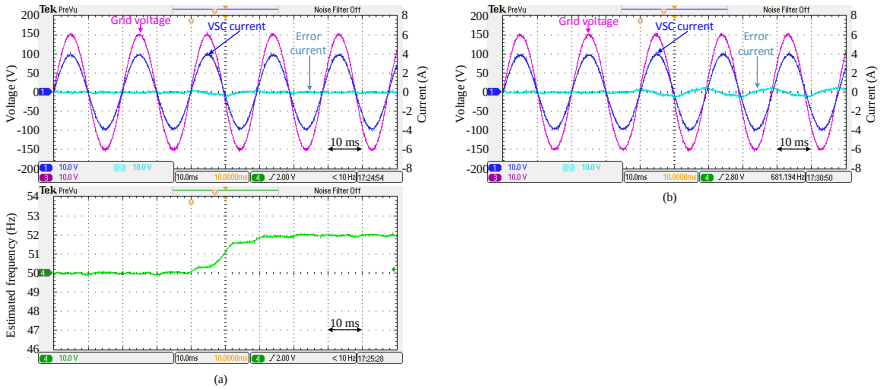

Fig. 3.17: A performance comparison between (a) the proposed controller and (b) the standard one under a +2-Hz frequency jump test [103].

CHAPTER 4. ANALYZING AND DESIGNING OLS TECHNIQUES

The aim of this section is designing advanced single-phase and three-phase open-loop synchronization (OLS) techniques. The design procedures of these OLS methods are briefly presented and their effectiveness is evaluated using some experimental tests.

4.1. DESIGNING A SINGLE-PHASE OLS TECHNIQUE

In this part, an efficient OLS technique for single-phase applications is designed and presented. It should be mentioned here that the content of this section is based on the reference [104] (paper 12 in Appendix).

4.1.1. DESIGN PROCEDURE

4.1.1.1 First Step: Designing Bandpass Filter/Quadrature Signal Generator (BPF/QSG)

The BPF/QSG, as mentioned before and shown in Fig. 1.21, is the key part of a standard single-phase OLS technique. This unit is responsible to extract the fundamental component of the grid voltage and its quadrature version. It implies that this unit should be able to reject the grid voltage DC offset and its harmonics. Here, the cascade connection of two MAFs in a generic synchronous reference frame is proposed as the BPF/QSG. Fig. 4.1 illustrates the block diagram representation of the proposed BPF/QSG.

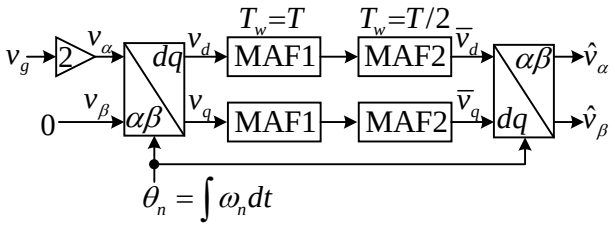

Fig. 4.1: Proposed BPF/QSG [104].

Notice that the first MAF has a window length equal to the grid fundamental period and, therefore, it totally rejects the grid voltage DC offset and its entire harmonics

(up to the aliasing point) under a nominal frequency. In the presence of frequency drifts, nevertheless, it can only attenuate the harmonic components. For this reason, a second MAF with a window length equal to half the grid period is cascaded with the first one to assist it in rejection harmonics under frequency drifts while maintaining a fast dynamic response.

The transfer functions relating the output signals of the proposed BPF/QSG to the grid voltage input signal can be obtained as

$$G_{\alpha}(\mathrm{s}) = \frac{\hat{v}_{\alpha}(s)}{v_g(s)} = \frac{4(s^2-\omega_n^2)}{T^2(s^2+\omega_n^2)^2}(1-e^{-Ts})(1+e^{-Ts/2}) \tag{4.1}$$

$$G_{\beta}(\mathrm{s}) = \frac{\hat{v}_{\beta}(s)}{v_g(s)} = \frac{8\omega_n s}{T^2(s^2+\omega_n^2)^2}(1-e^{-Ts})(1+e^{-Ts/2}). \tag{4.2}$$

The frequency response of these transfer functions can be expressed as

$$G_{\alpha}(j\omega_g) = \overbrace{\frac{\boldsymbol{16(\omega_n^2+\omega_g^2)}}{T^2(\omega_n^2-\omega_g^2)^2}\left|\cos(T\omega_g/4)\sin(T\omega_g/2)\right|}^{|G_{\alpha}(j\omega_g)|}\overbrace{\angle\frac{3\pi}{2}-\frac{3T\omega_g}{4}}^{\angle G_{\alpha}(j\omega_g)} \tag{4.3}$$

$$G_{\beta}(j\omega_g) = \overbrace{\frac{\boldsymbol{32\omega_n\omega_g}}{T^2(\omega_n^2-\omega_g^2)^2}\left|\cos(T\omega_g/4)\sin(T\omega_g/2)\right|}^{|G_{\beta}(j\omega_g)|}\overbrace{\angle\pi-\frac{3T\omega_g}{4}}^{\angle G_{\beta}(j\omega_g)}. \tag{4.4}$$

Based on these frequency responses, which can be visualized in Fig. 4.2, the following observations are made:

- The DC offset is completely rejected by the BPF/QSG. The grid voltage harmonics are also totally blocked under a nominal frequency and significantly attenuated under off-nominal frequencies.
- When the grid frequency has its nominal value, the $\alpha-$axis and $\beta-$axis outputs of the proposed BPF/QSG both have the same amplitude as the grid voltage fundamental component. In this condition, the $\alpha-$axis output is in-phase and the $\beta-$axis output has $90°$ phase difference compared to the grid voltage fundamental component.
- Under an off-nominal frequency, the $\alpha-$axis and $\beta-$axis outputs have different amplitude compared to each other and compared to the grid voltage fundamental component. In this condition, the $\alpha-$axis output is not in-phase and the $\beta-$axis output is not orthogonal to the grid voltage fundamental component.
- The $\alpha-$axis and $\beta-$axis outputs always have $90°$ phase difference compared to each other, which is an interesting advantage.

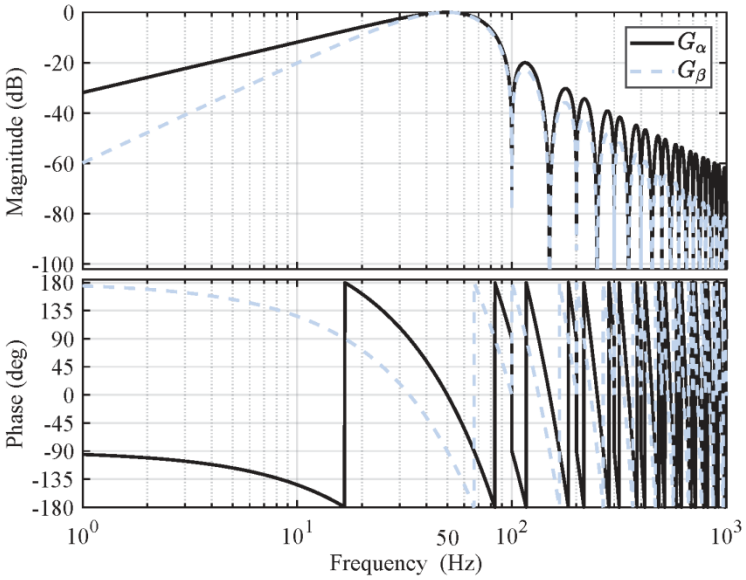

Fig. 4.2: Bode plots of (4.1) and (4.2) [104].

Solving the aforementioned problems of the proposed BPF/QSG is the objective of the rest of the design procedure.

4.1.1.2 Second Step: Designing A Frequency Estimator

As it will be shown later, an accurate estimation of the grid frequency is required for correcting the BPF/QSG problems. Using the traditional frequency estimation method, which is expressed in (4.5), is not suitable here as the $\alpha-$axis $\beta-$axis outputs of the proposed BPF/QSG are imbalanced under frequency drifts and, therefore, cause large double-frequency oscillations.

$$\hat{\omega}_g = \frac{\hat{v}_\alpha(t)\dot{\hat{v}}_\beta(t) - \hat{v}_\beta(t)\dot{\hat{v}}_\alpha(t)}{\hat{v}_\alpha^2(t) + \hat{v}_\beta^2(t)} \tag{4.5}$$

A better option here is the three equidistant samples (3ES) method, which can be described as (4.6) or equivalently as (4.7).

$$\hat{v}_x(k) - 2\hat{v}_x(k-n)\cos(nT_s\hat{\omega}_g) + \hat{v}_x(k-2n) = 0 \tag{4.6}$$

$$\hat{\omega}_g = \frac{1}{T_s n}\cos^{-1}\left(\frac{\hat{v}_x(k-2n) + \hat{v}_x(k)}{2\hat{v}_x(k-n)}\right) \tag{4.7}$$

In (4.6) and (4.7), $\hat{v}_x$ can be the $\alpha-$ or $\beta-$axis output of the proposed BPF/QSG,

and k and n denote the current sample and the distance between samples, respectively.

The problem here is that when $\hat{v}_x(k-n)$ in (4.7) is close to zero, a numerical ill-conditioning happens. A possible approach to deal with this problem is engaging both the $\alpha-$ or $\beta-$axis outputs in the 3ES-based frequency estimation, which results in

$$\hat{\omega}_g = \frac{1}{T_s n}\cos^{-1}\left(\frac{\left[\hat{v}_\alpha(k-2n)+\hat{v}_\alpha(k)\right]\hat{v}_\alpha(k-n)+\left[\hat{v}_\beta(k-2n)+\hat{v}_\beta(k)\right]\hat{v}_\beta(k-n)}{2\left[\hat{v}_\alpha^2(k-n)+\hat{v}_\beta^2(k-n)\right]}\right). \quad (4.8)$$

Notice that the denominator of (4.8) no longer becomes zero, which solves the aforementioned problem.

4.1.1.3 Third Step: Amplitude Imbalance Correction

Now, with an estimation of the grid frequency, which is provided by the frequency estimator, it is possible to correct the BPF/QSG problems. The first issue is the difference between the amplitude of the $\alpha-$ and $\beta-$axis outputs under off-nominal frequencies. This difference is because of the highlighted (bold) terms in (4.3) and (4.4). Therefore, by calculating the ratio of these terms using the estimated frequency as expressed in (4.9) and multiplying the $\beta-$axis output by it, the amplitude difference under off-nominal frequencies is corrected.

$$k_u = \frac{16(\omega_n^2+\hat{\omega}_g^2)}{32\hat{\omega}_g\omega_n} \quad (4.9)$$

4.1.1.4 Fourth Step: Amplitude Estimation

With correcting the aforementioned amplitude difference, the amplitude of both the $\alpha-$ and $\beta-$axis signals is equal to $\left|G_\alpha(j\omega_g)\right|V$ in the steady state. Therefore, an accurate amplitude estimation can be provided by multiplying the estimated amplitude by $1/\left|G_\alpha(j\omega_g)\right|$. Equation (4.10) provides an approximation of $1/\left|G_\alpha(j\omega_g)\right|$.

$$k_v = 1/\left|G_\alpha(j\hat{\omega}_g)\right| \approx \frac{(\omega_n+\hat{\omega}_g)^2}{2\left(1-5T^2(\hat{\omega}_g-\omega_n)^2/96\right)(\omega_n^2+\hat{\omega}_g^2)} \quad (4.10)$$

4.1.1.5 Fifth Step: Phase Estimation

As the $\alpha-$ and $\beta-$axis signals have the same amplitude and $90°$ phase difference, applying an inverse tangent function to their ratio gives an initial estimation of the grid voltage phase angle. The problem is that this estimation is not the same as the grid voltage phase angle under off-nominal frequencies. The reason is that, according to (4.3), the phase of the $\alpha-$axis signal is not the same as the grid voltage phase angle under off-nominal frequencies. This phase difference is equal to

$$\angle G_{\alpha}(j\omega_g) = -\underbrace{\left(\frac{3T}{4}\right)}_{k_{\varphi}}\Delta\omega_g. \tag{4.11}$$

Therefore, adding an approximation of (4.11), which can be calculated using the estimated frequency, to the output of the inverse tangent function corrects the phase offset error.

Based on Fig. 4.1 and equations (4.8), (4.9), (4.10), and (4.11), the block diagram representation of the proposed single-phase OLS technique can be obtained as shown in Fig. 4.3.

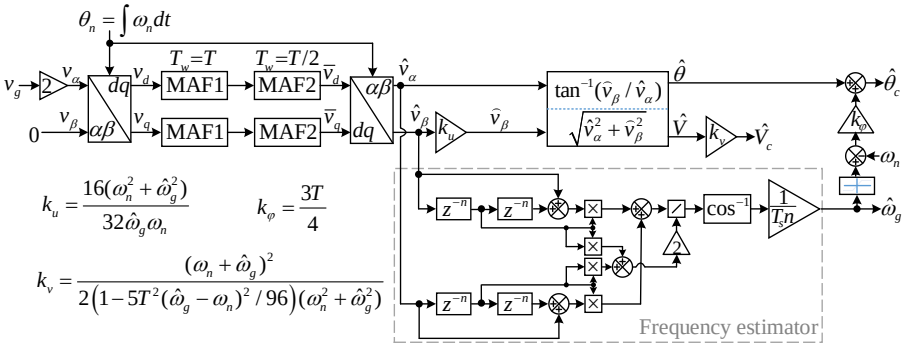

Fig. 4.3: Proposed single-phase OLS technique [104].

4.1.2. EXPERIMENTAL RESULTS

In this section, the performance of the proposed OLS technique is investigated using some experimental results. A pPLL with an in-loop MAF, which is briefly called the MAF-pPLL [39], [40], and a SOGI-FLL with prefilter (SOGI-FLL-WPF) [75] are selected for the comparison with the proposed OLS technique. Fig. 4.4 illustrates the results of this comparison. It can be observed that the proposed technique offers the best performance.

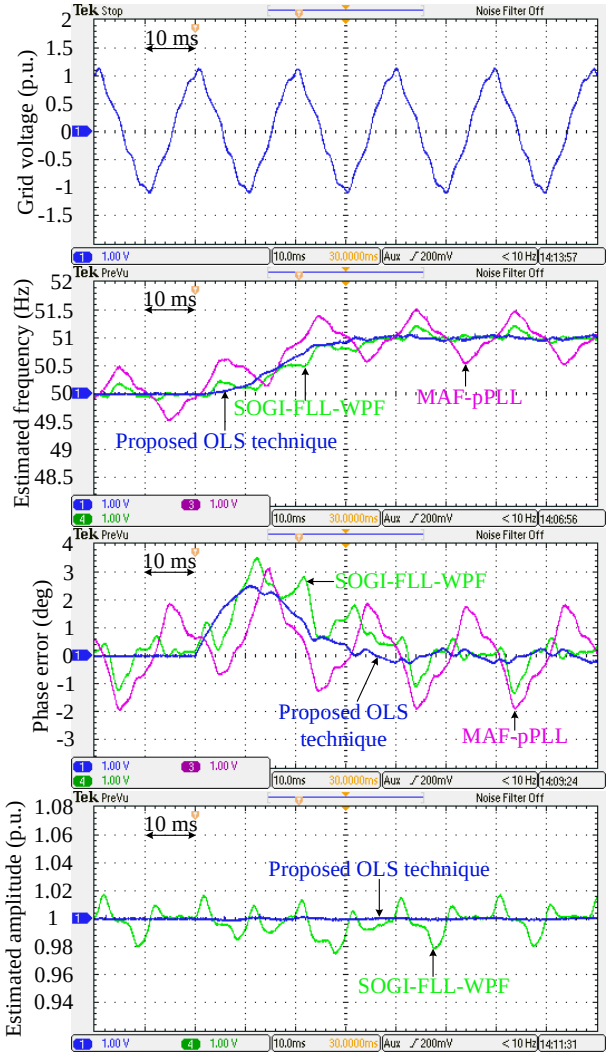

Fig. 4.4: A performance comparison between the proposed OLS technique, MAF-pPLL, and SOGI-FLL under a harmonically distorted grid condition with a frequency jump. Notice that the MAF-pPLL does not provide an estimation of the grid voltage amplitude [104].

4.2. DESIGNING A THREE-PHASE OLS TECHNIQUE

In this section, a true OLS technique for three-phase applications is presented. Designing this synchronization method is based on the $\alpha\beta$DSC operators. The design procedure is discussed briefly and some experimental results are presented to verify its effectiveness. It should be mentioned here that the content of this section is based on the reference [105] (paper 13 in Appendix).

4.2.1. DESIGN PROCEDURE

As shown in Fig. 1.18, designing a three-phase OLS technique requires a BPF (preferably a complex-coefficient one) for extracting the FFPS component of the grid voltage. Here, a chain of $\alpha\beta$DSC operators is considered for this purpose. Equation (4.12) describes the transfer function of a chain of such operators in the general form, in which $n_i\,(i=1,2,...,m)$ is the delay factor of operators [41], [47].

$$\alpha\beta\text{CDSC}_{n_1,n_2,\ldots,n_m}(s)=\prod_{i=1}^{m}\underbrace{\left(\frac{1+e^{\frac{j2\pi}{n_i}}e^{-\frac{T}{n_i}s}}{2}\right)}_{\alpha\beta\text{DSC}_{n_i}(s)} \tag{4.12}$$

Such a chain of operators can extract the grid voltage FFPS component and totally block some harmonics (depending on the number of operators and their delay factors) under a nominal frequency. The problem is that, under off-nominal frequencies, the extracted FFPS undergoes a phase shift and amplitude scaling compared to the grid voltage actual fundamental component. The reason is that the chain of operators is nonadaptive. Solving these errors is discussed in what follows.

4.2.1.1 Compensator Design

To avoid the phase and amplitude errors in the extraction of the grid voltage fundamental component using a chain of operators without having any knowledge about the grid frequency, a compensator needs to be cascaded with the chain so that a flat frequency response around the fundamental frequency is achieved. Designing this compensator is presented in what follows.

By approximating the delay term in the transfer function of a single operator, it can be shown that this transfer function can be approximated by

$$\alpha\beta\text{DSC}_{n_1}(s)\approx\frac{1}{\frac{T}{2}\frac{1}{n_1}(s-j\omega_n)+1} \tag{4.13}$$

where $\omega_n=2\pi/T$.

In a similar matter, for the case of two cascaded $\alpha\beta$DSC operators, we have

$$\overbrace{\alpha\beta\mathrm{DSC}_{n_1}(s)\times\alpha\beta\mathrm{DSC}_{n_2}(s)}^{\alpha\beta\mathrm{CDSC}_{n_1,n_2}(s)}\approx\frac{1}{\frac{T}{2}\left(\frac{1}{n_1}+\frac{1}{n_2}\right)(s-j\omega_n)+1}. \tag{4.14}$$

Considering this pattern, it can be concluded that for a general chain of $\alpha\beta$DSC operators, which is described by (4.12), the first-order approximation of its transfer function is as follows

$$\alpha\beta\mathrm{CDSC}_{n_1,n_2,\ldots,n_m}(s)\approx\frac{1}{\underbrace{\frac{T}{2}\left(\frac{1}{n_1}+\frac{1}{n_2}+\cdots+\frac{1}{n_m}\right)}_{T_d}(s-j\omega_n)+1}. \tag{4.15}$$

To evaluate the accuracy of this approximation, Fig. 4.5 demonstrates the frequency response of a chain of four operators with the delay factors 4,8,16, and 32 and also the frequency response of its first-order approximation. These results confirm the accuracy of the first-order counterpart, particularly around the nominal frequency.

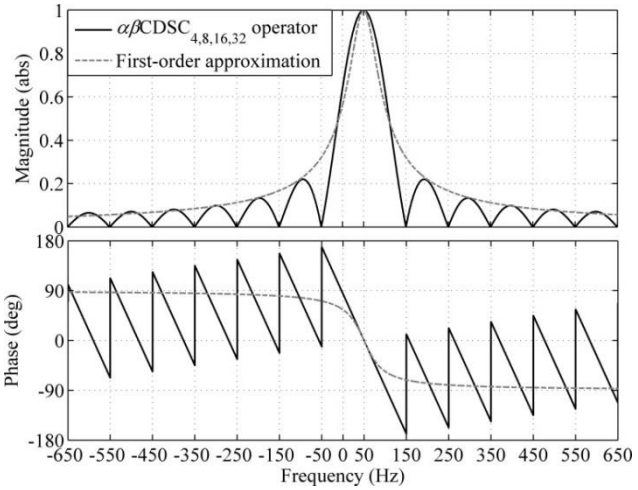

Fig. 4.5: Frequency response of a chain of four operators with delay factors 4,8,16,32 and its first-order approximation [105].

Considering that a chain of operators and its first-order counterpart have a close frequency response, the inverse of the first-order counterpart can be considered as the intended compensator. Based on this idea and using (4.15), the compensator transfer function for a general case, i.e., the case in which the chain includes *m* operators with delay factors $n_1, n_2, \cdots, n_m$, can be obtained as

$$G_c(\mathrm{s}) = \frac{1}{\alpha\beta\mathrm{CDSC}_{n_1,n_2,\ldots,n_m}(s)} \approx T_d(s - j\omega_n) + 1. \tag{4.16}$$

Based on this idea, the block diagram representation of the proposed OLS technique, which includes a chain of four operators with delay factors 4,8,16,32 and its corresponding compensator, can be obtained in Fig. 4.6. This structure is briefly called the true OLS (TOLS) technique.

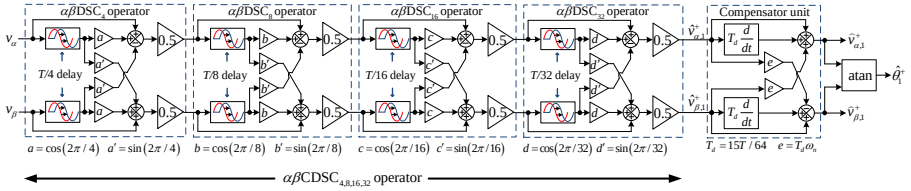

Fig. 4.6: Block diagram representation of the TOLS technique [105].

To provide a better filtering capability in extracting the grid voltage parameters, more operators with the same or different delay factors may be used. For example, Fig. 4.7 illustrates a structure which includes two identical $\alpha\beta\mathrm{CDSC}_{4,8,16,32}$ operators and a compensator. The repeated use of the same operators in this structure results in an enhanced harmonic filtering capability under frequency drifts. Therefore, it is called the enhanced TOLS (ETOLS) technique.

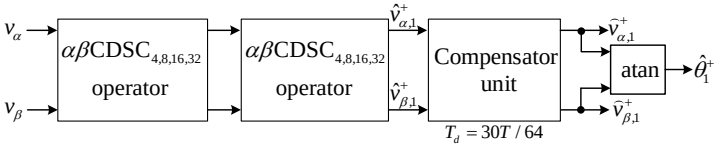

Fig. 4.7: Block diagram representation of the ETOLS technique [105].

4.2.1.2 Frequency Estimator Design

The TOLS and ETOLS techniques, which were presented in the previous section, can extract the grid voltage fundamental component and its phase and amplitude under nominal and off-nominal frequencies without any requirement for having the grid frequency information. However, as the information of the grid voltage frequency is required in the most applications, a frequency estimator is also designed and added to the TOLS and ETOLS techniques.

Equation (4.17) describes applying a standard frequency detector to the FFPS component extracted by the chain of operators in the TOLS or ETOLS technique.

$$\hat{\omega}_g = \frac{\hat{v}^+_{\alpha,1}(t)\dot{\hat{v}}^+_{\beta,1}(t) - \hat{v}^+_{\beta,1}(t)\dot{\hat{v}}^+_{\alpha,1}(t)}{[\hat{v}^+_{\alpha,1}(t)]^2 + [\hat{v}^+_{\beta,1}(t)]^2}. \tag{4.17}$$

Considering the backward difference formula, which is most often used for the digital approximation of the continuous differentiations in the aforementioned equation, it can be shown that the estimated frequency by (4.17) is equal to

$$\hat{\omega}_g = \sin\left(T_s\omega_g\right)/T_s = \omega_g - \overbrace{\frac{\omega_g^3 T_s^2}{3!} + \frac{\omega_g^5 T_s^4}{5!} - \frac{\omega_g^7 T_s^6}{7!} + \cdots}^{\text{error terms}} \tag{4.18}$$

where ω_g is the actual grid frequency and T_s is the sampling period. It can be observed that there are some error terms. These terms, which depend on the sampling frequency, are not negligible in applications where the sampling frequency is low. Therefore, they need to be compensated.

By defining the actual grid frequency as $\omega_g = \omega_n + \Delta\omega_g$, substituting it into (4.18), and neglecting small error terms, it can be shown that

$$\omega_g \approx \omega_n + \overbrace{\left(\frac{1}{1-0.5T_s^2\omega_n^2}\right)}^{\gamma}(\hat{\omega}_g - \omega_n + \overbrace{T_s^2\omega_n^3/6}^{\psi}). \tag{4.19}$$

Based on (4.17) and (4.19), the proposed frequency estimator is obtained as shown in Fig. 4.8. Notice that a MAF is also incorporated in this frequency detector to enhance its filtering capability.

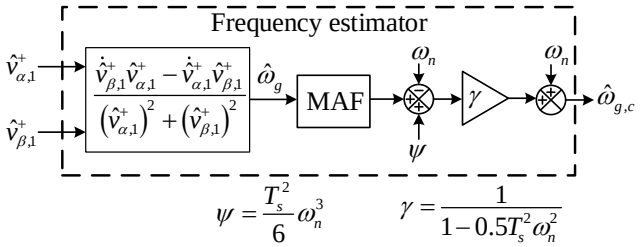

Fig. 4.8: Proposed frequency detector for including into the TOLS and ETOLS methods [105].

4.2.2. EXPERIMENTAL RESULTS

In this section, some experimental results are presented to investigate the performance of TOLS and ETOLS techniques. To have a reference for the comparison, the conventional SRF-PLL is also implemented. Fig. 4.9 demonstrates the obtained results in response to a step change in the grid frequency. It can be

observed that the phase errors of the TOLS and ETOLS techniques, like the conventional SRF-PLL, are zero after the frequency jump in the steady state. It implies that the designed compensators for these OLS techniques work effectively. It can also be observed that the proposed OLS techniques, particularly, the TOLS technique, have a shorter settling time compared to the SRF-PLL.

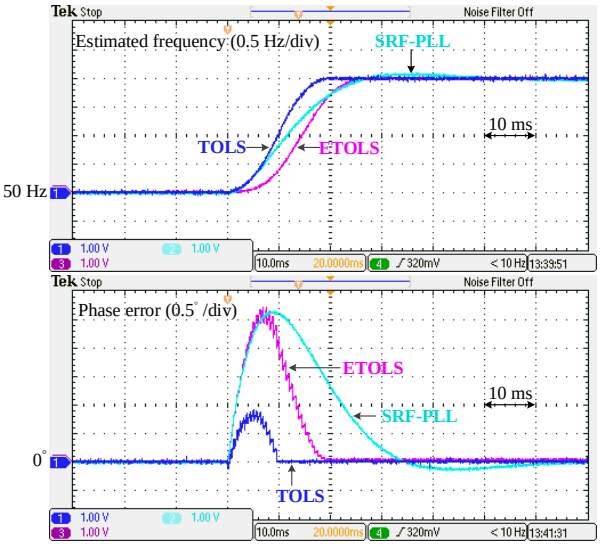

Fig. 4.9: Performance assessment of the TOLS and ETOLS techniques and the conventional SRF-PLL in response to +2 Hz frequency jump [105].

Fig. 4.10 shows the obtained results under a harmonically-distorted and imbalanced grid condition. Based on these results, the following observations are made

- The performance of the SRF-PLL is not affected by the grid frequency changes and it suffers from rather large oscillatory ripples in both the nominal and off-nominal frequencies.
- The TOLS and ETOLS techniques totally reject the grid voltage imbalance and its harmonics when the grid frequency is at its nominal value.
- Under an off-nominal frequency, the disturbance rejection capability of the ETOLS technique is still much better than the SRF-PLL. It is, however, not the case for the TOLS technique.

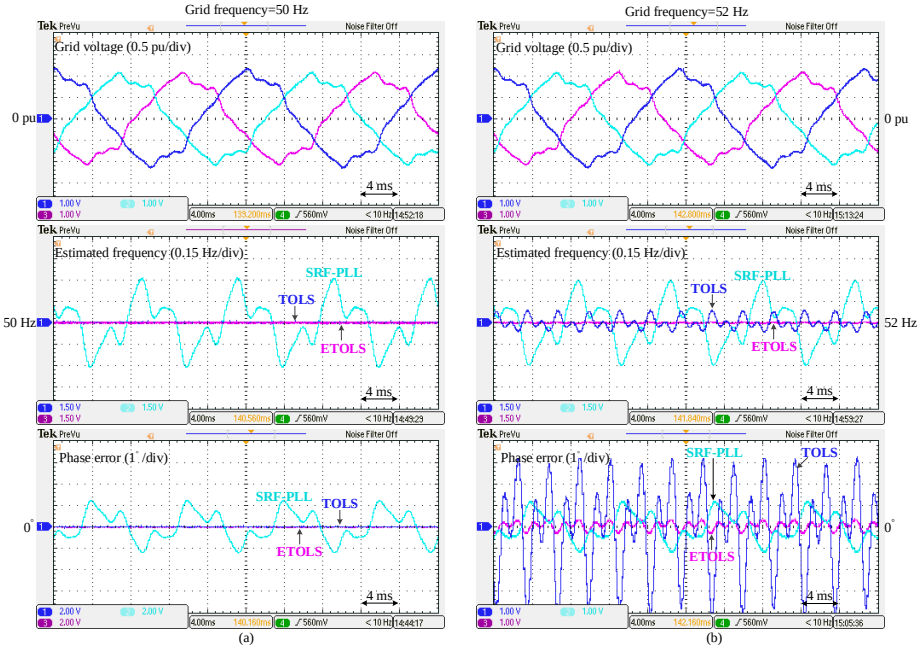

Fig. 4.10: Performance assessment of the TOLS and ETOLS techniques and the conventional SRF-PLL under a harmonically-distorted and imbalanced grid condition. (a) The grid frequency is at its nominal value. (b) The grid frequency is 52 Hz. The grid voltage harmonics in both cases are of order -5, +7, -11, and +13 [105].

Based on the aforementioned information, it can be concluded that the TOLS technique is an interesting option for applications where the grid frequency is always close to its nominal value. If a large frequency drift is expected, the ETOLS is a better option that the TOLS technique.

CHAPTER 5. CONCLUDING REMARKS

This thesis made some contributions to modeling, analyzing, and designing advanced synchronization techniques (including PLLs, FLLs, and OLS methods) for power converters.

Regarding PLLs, the following contributions were made:

- A study on single-phase TD-PLLs was conducted. The study was started by the analysis of the standard TD-PLL. It was demonstrated that this PLL, which uses a fixed-length quarter cycle delay, suffers from oscillatory and offset errors under off-nominal frequencies. Two advanced single-phase TD-PLLs, namely the NTD-PLL and VLTD-PLL, were then considered. The small-signal modeling of these PLLs was demonstrated and systematic approaches for tuning their control parameters were presented. It was shown that the VLTD-PLL solves both oscillatory and offset errors of the standard TD-PLL. The NTD-PLL, however, can only solve the phase offset problem.
- Designing an adaptive quadrature signal generator for single-phase PLLs was presented. This technique is based on a fixed-length quarter cycle delay and a nonlinear frequency feedback structure, which ensures that the generated fictitious signal is always orthogonal to the single-phase grid voltage signal under both nominal and off-nominal frequency. It was demonstrated using experimental results that the proposed PLL (ATD-PLL) has the same performance as the VLTD-PLL. Considering this fact and the implementation simplicity of the ATD-PLL compared to the VLTD-PLL, it was concluded that the ATD-PLL is a better option.
- A research on variable-length DSC operators-based PLLs was conducted. The CDSC-PLL and GDSC-PLL, which are two well-known three-phase PLLs and use cascaded adaptive $\alpha\beta$-frame DSC operators for rejecting harmonics and other disturbances in their input, were considered as the case studies. The modeling procedure of these PLLs was demonstrated, some control design guidelines were presented, and comparative experimental tests conducted to highlight their advantages/disadvantages. It was demonstrated that there is no large performance difference between these PLLs. Based on this fact and the implementation simplicity of the CDSC-PLL compared to the GDSC-PLL, it was concluded that the CDSC-PLL is a better option.
- An analysis of SSLKF-PLLs was conducted. Two-state SSLKF-PLL (SSLKF-PLL2) and three-state SSKLF-PLL (SSLKF-PLL3), which respectively are designed by considering a two-state and three-state physical model, were considered in this study. It was demonstrated that the SSLKF-PLL2 and SSLKF-PLL3, respectively, are equivalent to the ESRF-

PLL and ET3-SRF-PLL, which are closed variants of the conventional SRF-PLL.

- A method to completely remove the DC component in the three-phase PLLs input was proposed. It was shown that this technique is simple and efficient and has a less adverse effect on the PLL dynamic behavior compared to the state of the art techniques.
- A study on a well-known three-phase PLL, briefly called the PMAF-PLL, was conducted. This PLL includes an SRF-PLL, a MAF-based prefiltering stage for removing the DC offset and all harmonics up to the aliasing point, and a parallel frequency detector for adapting the prefilter to variations in the grid frequency. An effective yet simple approach to eliminate the need for the parallel frequency detector was first proposed. The resultant structure was named the enhanced PMAF-PLL. A small-signal model for the enhanced PMAF-PLL was then derived, and tuning its control parameters was performed. Finally, some comparative experimental results were shown to demonstrate the effectiveness of the EPMAF-PLL.

Regarding FLLs, the following contributions were made:

- A research on single-phase SOGI-FLLs, including the standard SOGI-FLL, SOGI-FLL-WPF, and SOGI-FLL-WIF (also known as the FOGI-FLL) was conducted. The small-signal modeling of these FLLs, their tuning procedure, and their performance analysis under different grid scenarios were presented. It was demonstrated that, under a fair condition of comparison, the SOGI-FLL-WPF and SOGI-FLL-WIF have almost same the speed of response, a rather better harmonic filtering capability, and a much better dc offset and subharmonic rejection capability compared to the standard SOGI-FLL. These advantages of the SOGI-FLL-WPF and SOGI-FLL-WIF, however, are at the cost a lower stability margin, a larger overshot during transients, and a rather higher computational burden.
- The concept of in-loop filter for designing more advanced three-phase FLLs was proposed. Two design examples were then considered. The first one was using a chain of the $\alpha\beta$DSC operators as the FLL in-loop filter, and the second one was employing a first-order CBF as the in-loop filter. The modeling and tuning of the resultant advanced FLLs were then carried out, and a theoretical and experimental performance comparison between them and a standard FLL (ROGI-FLL) was conducted. It was demonstrated that an in-loop filter enhances the disturbance rejection capability of an FLL, but reduces its stability margin. A connection between PLLs and FLLs was also established. It was demonstrated that PLLs and FLLs are practically equivalent systems which are implemented in different reference frames.
- Based on the FLL concept, an adaptive resonant regulator for single-phase grid-tied VSCs was designed. This resonant controller does not require a dedicated synchronization system as it automatically adjusts its resonance

frequency according to the grid frequency variations. The proposed resonant controller was applied to a grid-connected Danfoss converter. The experimental results demonstrated that the proposed controller ensures a zero current tracking error under nominal and off-nominal frequencies even when the grid voltage is highly distorted with harmonics.

Regarding OLS techniques, the following contributions were made:

- An OLS technique for single-phase applications was developed. The basic building block of this synchronization method was a MAF-based BPF/QSG, which removes all harmonics and DC offset of the grid voltage and extracts its fundamental component and its quadrature version. An enhanced 3ES based method was then designed and used for detecting the grid frequency. The frequency estimated by the enhanced 3ES method was then employed for correcting the amplitude imbalance, phase offset error, and amplitude scaling error caused by the MAF-based BPF/QSG. Finally, through comparative experimental results, the effectiveness of the proposed OLS technique was demonstrated.
- An OLS technique for three-phase applications was designed. This OLS technique includes 1) a chain of $\alpha\beta$-frame DSC operators for extracting the grid voltage fundamental component, 2) a compensator which is connected in series with the operators and corrects errors caused by them under off-nominal frequencies without requiring any knowledge of the grid frequency, 3) a standard frequency detector which is connected to the output of the operators and extracts the grid frequency, and 4) a correction scheme, which corrects the standard frequency detectors errors. Through experimental tests, it was demonstrated that the proposed OLS technique provides a fast transient behavior and high harmonic rejection ability. Low computational burden and implementation simplicity are other characteristics of this OLS technique.

As future works, the following suggestions are given:

- It is known that, under a weak grid condition, the dynamic interaction between a PLL (or FLL) and the grid-tied power converter may make the PLL (or FLL) and, consequently, the converter unstable. Such a dynamic interaction between an OLS technique and the grid-connected converter has not been studied before.
- An adaptive resonant controller for single-phase grid-connected converters was designed. In this work, an *L*-filter was considered in the converter output and a unity power factor operation was assumed. The extension of the idea for the case of a multi-functional converter with an LCL output filter can be an interesting topic for the future works.

- All linearized models developed in this thesis have a linear time-invariant (LTI) nature. Therefore, it may be a good idea to develop linear time-periodic models for them and evaluate their accuracy in predicting the stability and dynamic behavior of synchronization techniques compared to the LTI ones.
- The large signal modeling and stability analysis of synchronization techniques based on these models have also received a little attention in the literature. Therefore, it can be a good direction for the future works.

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APPENDIX. PAPERS

Paper 1: Reference [5]

Three-phase PLLs: A Review of Recent Advances

S. Golestan, J. M. Guerrero, and J. C. Vasquez

The paper has been published in
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Paper 2: Reference [6]

Single-phase PLLs: A Review of Recent Advances

S. Golestan, J. M. Guerrero, and J. C. Vasquez

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Paper 3: Reference [95]

Small-Signal Modeling, Stability Analysis and Design Optimization of Single-Phase Delay-Based PLLs

S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, J. Doval-Gandoy, and F. D. Freijedo

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Paper 4: Reference [96]

Research on Variable-length Transfer Delay and Delayed Signal Cancellation Based PLLs

S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki

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Paper 5: Reference [97]

An Adaptive Quadrature Signal Generation Based Single-Phase Phase-Locked Loop for Grid-Connected Applications

S. Golestan, J. M. Guerrero, A. M. Abusorrah, M. M. Al-Hindawi, and Y. Al-Turki

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Paper 6: Reference [98]

Steady-State Linear Kalman Filter-based PLLs: A Second Look

S. Golestan, J. M. Guerrero, and J. C. Vasquez

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Paper 7: Reference [99]

DC-Offset Rejection in Phase-Locked Loops: A Novel Approach

S. Golestan, J. M. Guerrero, and J. C. Vasquez

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Paper 8: Reference [100]

PLL with MAF-Based Prefiltering Stage: Small-Signal Modeling and Performance Enhancement

S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, and J. Doval-Gandoy

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Paper 9: Reference [101]

Modeling, Tuning, and Performance Comparison of Advanced Second-Order Generalized Integrator-based FLLs

S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki

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Paper 10: Reference [102]

A Study on Three-Phase FLLs

S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki

The paper has been submitted to
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and is currently under review.

Paper 11: Reference [103]

An Adaptive Resonant Regulator for Single-Phase Grid-Tied VSCs

S. Golestan, E. Ebrahimzadeh, J. M. Guerrero, and J. C. Vasquez

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Paper 12: Reference [104]

An Open-Loop Grid Synchronization Approach for Single-Phase Applications

S. Golestan, J. M. Guerrero, and J. C. Vasquez

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Paper 13: Reference [105]

A True Open-Loop Synchronization Technique

S. Golestan, A. Vidal, A. G. Yepes, J. M. Guerrero, J. C. Vasquez, and J. Doval-Gandoy

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