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A SiC MOSFET Power Module With Integrated Gate Drive for 2.5 MHz Class E Resonant Converters

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Abstract

Industrial processes are still relying on high frequency converters based on vacuum tubes. Emerging silicon carbide semiconductor devices have potential to replace vacuum tubes and bring benefits for converters in the high frequency range. At high switching frequencies hard-switched gate drivers can enable high power density design, but suffer from high temperatures and require low inductive design. This paper addresses the two issues through integrated packaging. Integrating the hard-switched gate driver in the power module ensures a low inductive and high thermal conductive package design. The required gate-source loop inductance is calculated and obtained in the design through use of the simulation software ANSYS Q3D Extractor. Two silicon carbide MOSFET power module prototypes are manufactured on a AlN substrate and FR4 PCB, to compare the thermal performance of the gate driver in the two cases. The electrical performance of the final power module is verified at 2.5 MHz in a Class E resonant converter.

1 Introduction

High frequency converters used for industrial processes, such as induction and dielectric heating, are still relying on vacuum tubes. Conventional silicon (Si) based power devices cannot operate at the high switching frequencies, high voltages and high powers required for such applications [1]. New wide band gap semiconductor devices, such as silicon carbide (SiC) MOSFETs, provide higher breakdown voltage, higher thermal conductivity and reduced on state resistance when compared with Si. A SiC MOSFET has smaller chip area when compared with a Si chip of similar voltage and current ratings. As a consequence, SiC devices have lower gate charge requirements, which enable higher operating frequencies [2]. Replacing vacuum tubes with new solid state devices, results in both smaller, cheaper and more efficient high frequency converters [3]. However, limited packages are available with SiC devices which utilize these benefits for the high frequency industry applications. Thus, the topic of this paper is on the development of a custom packaged SiC MOSFET power module and uses a 2.5 MHz Class E resonant converter as a test platform.

For switching frequencies in the MHz-range the gate losses of MOSFETs become significant, and resonant gate drivers are often preferred. Compared with conventional hard-switched gate driver integrated circuits (ICs), resonant gate drivers recover some of the gate energy, thereby lowering losses in the gate circuitry. Resonant gate drivers have lower requirements to gate-source loop inductance, as it is included in the resonant loop design [4]. However, resonant gate drivers are more complex to design. More components, i.e. capacitors and inductors, share the losses which makes it easier to cope with the high gate losses [5]. But this comes at the expense of decreased power density

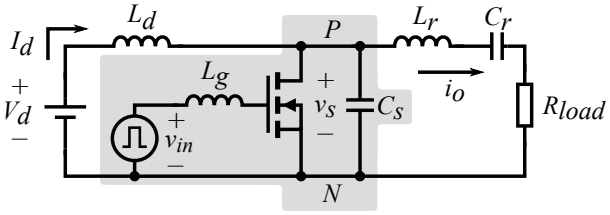

Figure 1 Class E resonant converter schematic, with marked components for integration in package.

[6]. Maintaining the high power density and simplicity of hard-switched gate driver ICs at high frequencies, requires low inductive design and high thermal conductance [7]. Packaging methods such as printed circuit board (PCB) embedded dies [8], [9] or PCBs molded on top of a direct bonded copper (DBC) substrate offer very low inductive design [10]. However, the hard-switched gate driver ICs are still mounted on the low thermally conductive PCB material. A solution is to mount the hard-switched gate driver IC directly on the DBC to dissipate the higher gate losses, but requires bond wires to interconnect the gate driver IC and the die which increase inductance [11], [12]. However, this may be acceptable if the parasitics of the gate-loop are designed properly.

In this paper, a SiC MOSFET power module with integrated hard-switched gate driver IC on DBC is designed for a Class E resonant converter operating at 2.5 MHz. The hard switched gate driver IC is included in the package to more effectively dissipate its losses (see **Figure 1**). In literature, analysis of existing packaging for fast switching applications, shows the importance in maintaining low inductive design combined with an auxiliary source connection for the gate driver circuit [3], [13]. Additionally, when the switch in the Class E resonant converter turns on/off the current shifts from being conducted through the parallel

capacitance, C_s, to the switch, and vice versa. Thus the parallel capacitance, C_s, is also included in the package to ensure low inductance between the two. The gate-source inductance is analysed to ensure fast switching without gate voltage overshoot and ringing. A three dimensional (3D) model of the power module is created and circuit parasitics are extracted using the simulation software ANSYS Q3D Extractor. Two power modules are manufactured to experimentally evaluate the thermal performance of mounting the gate driver IC on DBC and PCB. The power module design is verified by operation in a Class E resonant converter at 2.5 MHz.

2 Design of integrated module

The gate-source inductance must be designed low enough to ensure good transient response [14]. Applying Kirchoffs voltage law on a generic gate-source loop (see **Figure 2**), including the gate loop inductance L_g, gate resistance R_g and gate-source capacitance C_{gs}, results in

$$v_{in}(t) = L_g \frac{\mathrm{d}i(t)}{\mathrm{d}t} + i(t)R_g + v_{gs}(t) \tag{1}$$

By inserting that $i(t) = C_{gs}\frac{\mathrm{d}v_{gs}(t)}{\mathrm{d}t}$, the Laplace transform of (1) is written as

$$\frac{V_{gs}(s)}{V_{in}(s)} = \frac{\frac{1}{L_g C_{gs}}}{s^2 + \frac{R_g}{L_g}s + \frac{1}{L_g C_{gs}}} \tag{2}$$

This transfer function includes the dynamics from the hard-switched gate driver IC to the gate-source voltage on the SiC MOSFET. To analyze the dynamics of this equation, it is compared to the standard form of a second order system [15], given by

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3}$$

where ζ is the damping ratio and ω_n the natural frequency. Comparing (2) with the standard form in (3) an expressing for the inductance in the loop is found as

$$L_g = \frac{C_{gs}R_g^2}{4\zeta^2} \tag{4}$$

Here no external gate resistance is used to achieve fast switching speed. A critically damped response $\zeta = 1$ is chosen as a case, and by inserting values of the CPM2-1200-0160B die [16] to (4) the inductance is

$$L_g = \frac{521\,\mathrm{pF}\cdot(6.5\,\Omega)^2}{4\cdot 1^2} = 5.5\,\mathrm{nH} \tag{5}$$

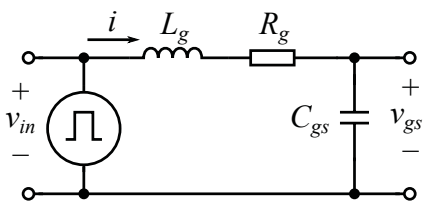

Figure 2 Schematic of generic gate-source loop.

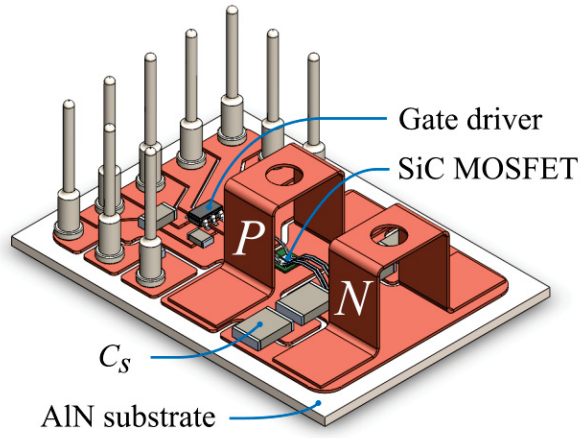

Figure 3 3D model of designed SiC MOSFET power module.

A gate loop inductance above the value in (5) causes an underdamped gate-source voltage, which results in some overshoot. Any value below results in an overdamped response, meaning no overshoot of gate-source voltage is present.

A SiC MOSFET power module with an integrated gate driver directly on the DBC was designed (see **Figure 3**). The UCC27531 gate driver from Texas Instruments is used [17], and placed close to the SiC MOSFET. Decoupling capacitors for the +20 V and -5 V supply voltages are also included inside the module. Plate power terminals placed symmetrically around the die ensure low inductance. The capacitance in parallel with the switch is $C_s = 880\,\mathrm{pF}$. The capacitors making up C_s are arranged symmetrically in respect to the drain-source path, to improve the current sharing between the capacitors.

The designed 3D model of the power module is imported into ANSYS Q3D Extractor, to extract the parasitic inductance of three main loops. The three loops are the drain-source, gate-source and die to external capacitors, C_s (see **Figure 4**).

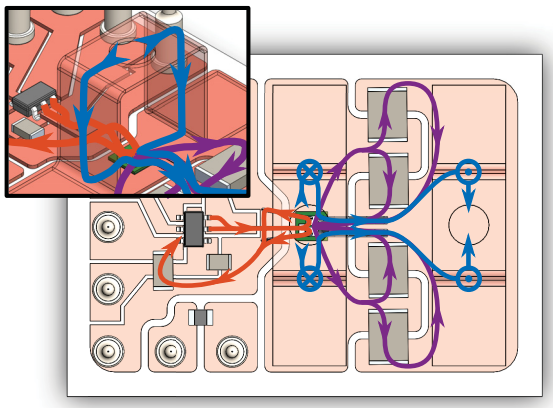

Figure 4 Extracted loop inductance of gate-source (red), drain-source (blue) and die to external capacitance (purple). Here ⊗ indicates direction inward and ⊙ outward.

The inductances are extracted for a frequency of 2.5 MHz, similar to the fundamental component of operation in the Class E resonant converter. To extract the gate-source loop inductance, gate and source pads of the SiC MOSFET model are shorted. In ANSYS Q3D Extractor the loop is simulated as 4.6 nH, which is slightly below the target value calculated in (5), required to obtain a critically damped gate-source voltage. To calculate the drain-source loop inductance, drain and source pads of the SiC MOSFET are shorted. Capacitors are left as open-circuits. The loop is defined from the top surface of power terminal pin *P* to *N* (see **Figure 3**). The drain-source power loop inductance is 6.3 nH. For the inductance between die and external capacitors, initially both drain-source of the MOSFET and terminals of capacitors are modelled as shorts. This results in a loop inductance of 2.1 nH. Current distribution reveals that current crowds at the two inner capacitors closest to the die. Thus, 2.1 nH is considered the minimum inductance for the loop. Due to inductances there might be an instantaneous imbalance in voltage distribution between capacitors. To have equal voltage, they should have equal charge rate, which implies equal current sharing. The maximum inductance path involves the loop of only the two outer capacitors. In order to assess the impact of this loop inductance, a case is simulated where the two inner capacitors are modelled as open-circuits. For this case the loop inductance is simulated as 3.6 nH. The effective loop inductance at 2.5 MHz is within the range 2.1 to 3.6 nH, but is dependent on the inductance between capacitors, their equivalent series resistance and equivalent series inductance. The issue of imbalance is not treated in more detail in this paper.

To manufacture the power modules, the copper layout is etched. A solder stencil with thickness of 125 μm is used to ensure a uniformly distributed solder layer. The SiC MOSFET die, gate driver IC, capacitors and pins are all soldered in a vacuum vapor phase oven. The SiC MOSFET die is wirebonded using 250 μm thick aluminium wire. A single wire is used for the gate pad. A total of four source bond wires are used for the power loop, of which two are chain-bonded and also work as auxiliary source connections for the gate drive circuit (see **Figure 5**).

The thermal benefit of mounting the gate driver on the DBC instead of the conventional placement on a PCB is investigated experimentally. Thus, two power modules were manufactured with the same layout. One was designed on a 1 mm thick AlN DBC substrate with 0.3 mm copper, while the other on a conventional 2-layer PCB of 1.5 mm thick FR4 material and 35 μm copper.

3 Experimental tests

The gate driver circuit is tested before the power module is encapsulated in protective gel. This is done to experimentally measure the temperature of the gate driver IC when driving the SiC MOSFET at 2.5 MHz. Temperatures are logged using a FLIR E40 infrared camera. Initially, a calibration test is done to ensure the correct emissivity coefficient is used on the FLIR E40. The calibration test is done

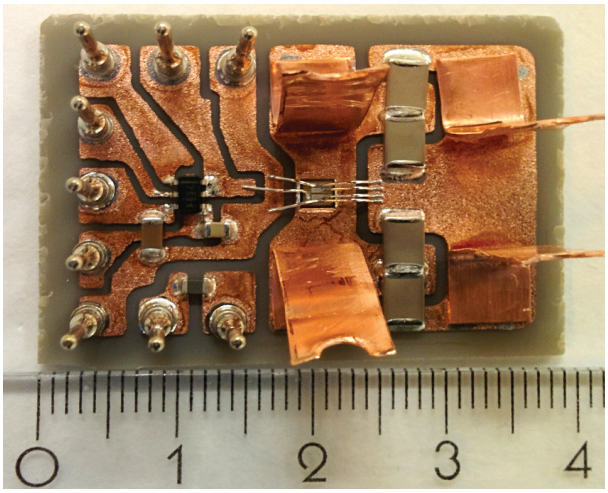

Figure 5 Manufactured module on 1 mm AlN DBC.

in the temperature range from 30 to 110 °C, by placing the gate driver IC on a hotplate. The temperature readings are compared with temperature measurements of the thermocouple on a Fluke 179 and optical temperature sensors OTG-M280 from Opsens. The calibration concludes that an emissivity coefficient of 0.95 results in complying temperature readings in the range tested.

After calibration, the gate driver IC is tested by driving the SiC MOSFET gate at a frequency of 2.5 MHz, between voltage levels -5 V and 20 V. During this test no bias is applied to the drain-source of the SiC MOSFET. The FLIR E40 is configured to automatically detect the point of highest temperature within a region (see **Figure 6**), and also measures the temperature of the heat sink. The heat sink is coated with black painting to have similar emissivity coefficient as the gate driver IC. The test is done with no forced convection, thus temperature dissipation from the gate driver IC is mainly through conduction to the heatsink and natural convection from its case surface.

The case top temperature is logged at a frequency of 30 Hz (see **Figure 7**). At the end of test the maximum case temperatures logged are 69 °C and 120 °C for the gate driver mounted on a DBC and PCB, respectively. This clearly shows a benefit from placing the gate driver IC directly on the DBC in terms of thermal performance.

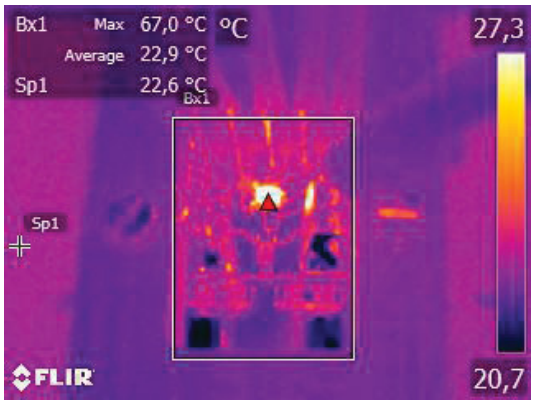

Figure 6 Image from FLIR E40 during test.

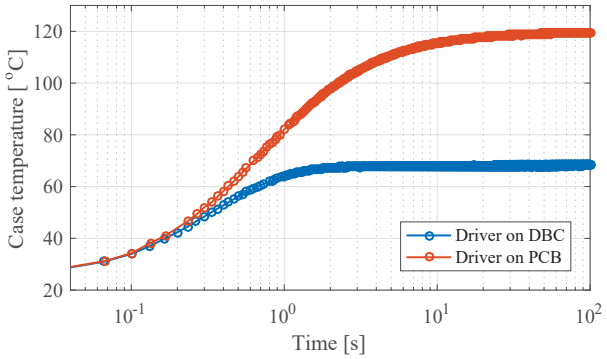

Figure 7 Measured top case temperature of gate driver.

3.1 Estimation of gate driver junction temperature

The UCC27531 gate driver has a maximum allowable junction temperature, $T_{J,max}$, of 150 °C [17]. Only measurements of the top case temperature, T_C, and ambient temperature, T_A are available, thus the actual operating margin is unknown. In the following section an attempt to estimate the junction temperature, T_J, is made. From the datasheet of the UCC27531 gate driver IC [17] its thermal resistances are available as case-to-ambient $R_{CA} = 163.6\frac{\text{K}}{\text{W}}$, junction-to-case $R_{JC} = 14.7\frac{\text{K}}{\text{W}}$ and junction-to-board $R_{JB} = 28.3\frac{\text{K}}{\text{W}}$ (see **Figure 8**).

The thermal resistances are complying with the specifications found in the JESD51 standard, and are given for conditions of only natural convection and when steady state is reached. This is similar conditions as the temperature measurements presented in this paper, and thus the stated thermal resistances are deemed accurate for estimating the junction temperature.

From the thermal network of the gate driver, it is found that the power dissipation through the top case surface is

$$P_C = \frac{T_C - T_A}{R_{CA}} \tag{6}$$

From this information the junction temperature is estimated from

$$T_J = T_C + P_C \cdot R_{JC} \tag{7}$$

By using (6) and (7) on the temperatures obtained in the previous test, the maximum junction temperatures calculated are 72 °C and 129 °C using the DBC and PCB, respectively.

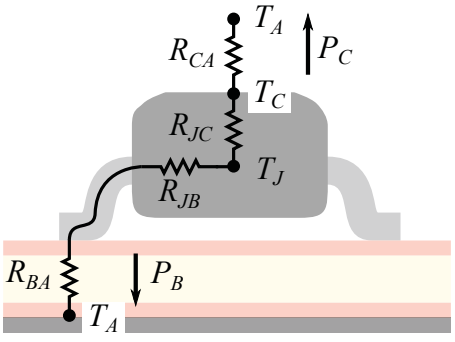

Figure 8 Thermal network of the gate driver IC.

During the test, power is supplied to the gate driver circuit through a GW Instek GPS-4303 power supply. The combined power consumption in the gate circuit is measured as an average value of 1.83 W. It is useful to estimate how much of this power is dissipated in the gate driver IC. Power is dissipated in both the gate driver IC and the gate resistance of the SiC MOSFET, but the distribution between the two is unknown. One approach is to estimate the gate power loss of the CPM2-1200-0160B die by using its available SPICE model [16], and setting up a LTSpice simulation using the parasitics extracted in Section 2. By doing this, the loss in the SiC MOSFET gate is found to be 0.78 W at 2.5 MHz. Thus the remaining power of 1.05 W is dissipated in the gate driver IC. With this information it is possible to estimate a thermal resistance from junction to ambient, R_{JA}, as

$$R_{JA} = \frac{T_J - T_A}{P_{IC}} \tag{8}$$

By employing (8) the thermal resistance R_{JA} is found as 46 $\frac{\text{K}}{\text{W}}$ and 98 $\frac{\text{K}}{\text{W}}$ for the gate driver placed on DBC and PCB, respectively. For the conditions tested, the thermal resistance junction-to-ambient of a gate driver IC placed on a PCB is more than two times higher when compared to placement on a 1 mm AlN DBC substrate.

3.2 Class E electrical measurement

Before testing the power module in the Class E resonant application, it is encapsulated to withstand the required drain-source voltage bias. This is done by a custom made housing which is mounted and the module is poured with silicone gel, through a hole in the housing (see **Figure 9**). The power module is placed in a vacuum chamber during curing of the gel, to avoid trapped air bubbles that could cause unwanted corona or partial discharges, due to lower electric field breakdown strength of air compared with silicone gel. The Class E resonant converter setup used for test is based on the findings in [18]. It has an input inductance of $L_d = 25\,\mu\text{H}$, the resonant tank consists

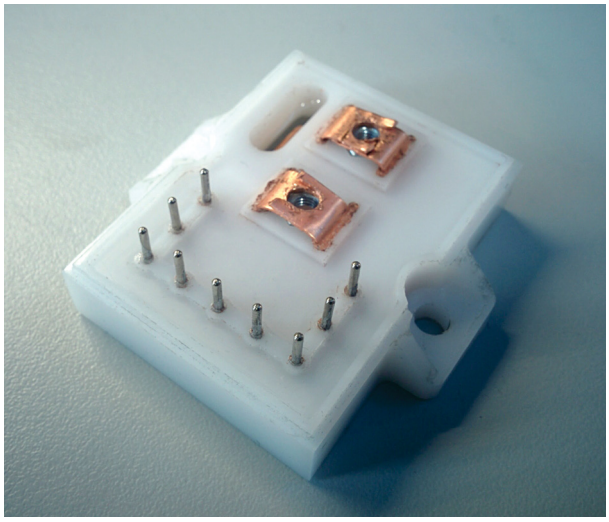

Figure 9 Picture of final module after attaching the housing and potting of protective gel.

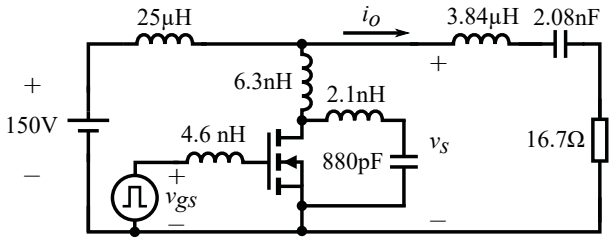

Figure 10 Circuit diagram used for simulation.

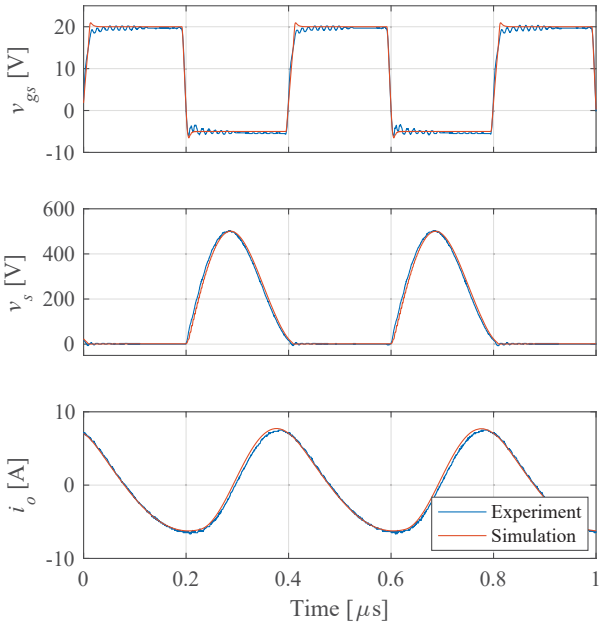

Figure 11 Experimental and simulated Class E waveforms, imported to MATLAB for plotting.

of $C_r = 2.08\,\text{nF}$, $L_r = 3.84\,\mu\text{H}$ and the output resistance is $R_{load} = 16.7\,\Omega$. The inductors are wound on powdered iron cores, and the capacitance is achieved by parallel connecting surface mounted NP0 ceramic capacitors. The experiments are evaluated at an input voltage of V_d =150 V. The circuit diagram used for simulation includes the parasitic inductances calculated for each loop (see **Figure 10**). The SPICE model of the CPM2-1200-0160B SiC MOSFET [16] is imported and the circuit is simulated using LTSpice. The gate-source voltage, v_{gs}, switch voltage, v_s, and output current, i_o, waveforms are measured experimentally and compared with the simulation results (see **Figure 11**). The average voltage and input current are measured, resulting in an input power of 461 W. The output power is 406 W, calculated from the root mean square value of the measured output current, i_o, and the output load, R_{load}. The efficiency of the converter is 88 %. The peak switch voltage is 503 V and a sinusoidal output current is observed. There is a very good agreement between the simulation and the experimental results. Due to the low inductive design, neither drain-source voltage, v_s, or the output current, i_o, is disturbed during switching events. The gate-source voltage waveform is undisturbed by the switching, and its response is nearly critically damped. This is the result of achieving proper gate-source loop inductance and by using an auxiliary source connection. This verifies the functionality and operation of the SiC MOSFET power module.

As demonstrated, the gate driver tests show a benefit in terms of thermal performance by integrating the gate driver IC on the DBC of the power module. However, the test was performed with no drain-source bias and no power dissipation from the SiC MOSFET except for its gate losses. For future work, the thermal performance of the combined system will be investigated to see how the gate driver IC is affected by the losses dissipated from the SiC MOSFET during operation. Temperature measurements using the thermistor inside the power module can be used as a metric. Alternatively, by modifying the housing an optical temperature sensor could be used to measure surface temperatures of components inside the power module [19]. Integrating gate driver IC and ceramic capacitors on DBC changes the thermal stress when compared to conventional placing outside the power module, which could affect the overall reliability. The temperature measurements could be used in a reliability study of the designed power module.

The prototype SiC MOSFET power module shows good electrical performance, which proves the design methodology. Thus in the future the power module concept will be extended to higher voltage and power levels to meet the requirements of the industrial applications. SiC MOSFET dies for 10 and 15 kV are now available [20]-[22], but are yet to be used in the MHz-frequency range which is required for some industrial processes.

4 Conclusion

A SiC MOSFET power module with integrated hard-switched gate driver was designed and manufactured. The CPM2-1200-0160B die requires a gate-source inductance of 5.5 nH for a critically damped gate-source voltage when exposed to a step input from the gate driver. The inductive design was attained through the ANSYS Q3D Extractor software. The achieved drain-source loop inductance is 6.3 nH. The inductance loop of MOSFET die and parallel capacitance is calculated to be in the range 2.1 to 3.6 nH. Substantial lower thermal resistance is achieved by including the gate driver IC on the DBC, when compared to conventional mounting on PCB. The junction-to-ambient thermal resistance was estimated as 46 $\frac{\text{K}}{\text{W}}$ by placing the gate driver IC on the power module DBC, compared with 98 $\frac{\text{K}}{\text{W}}$ when placed on a PCB. This allows hard-switched gate drivers to operate at higher frequency. The performance of the integrated power module was tested through operation in a 2.5 MHz Class-E resonant converter. The gate-source voltage is nearly critically damped and not disturbed by switching, due to the auxiliary source connection. Due to low inductive design switch voltages and output current is unaffected by switching transients. The results show a very good coherence between experiment and simulation. This proves the applicability of the design methodology and software tools used. Due to the successful results, the concept will be extended in the future for new power modules using 10 and 15 kV SiC MOSFETs.

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