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Triangle Carrier based Discontinuous PWM for Three-Level NPC Inverters

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***Abstract*—This paper proposes a triangle carrier based discontinuous PWM (TCB-DPWM) implement method for three-level neutral-point-clamped (3L-NPC) inverters. The function equivalent relationship of proposed TCB-DPWM and space vector based discontinuous PWM (SVB-DPWM) is mathematically analyzed in this paper. The proposed TCB-DPWM method effectively simplified the implementation of the SVB-DPWM by injecting twice common mode voltages (CMVs) to original modulation signals, where different DPWM methods can be easily obtained in a unified scheme by setting different values of proportional allocation factor for small vectors in different sectors. In addition, a TCB-DPWM based neutral point voltage balancing method is investigated to demonstrate its application. The polarity of the CMV injection is regulated according to the polarity of the proportional allocation factor to realize the neutral point voltage balancing. Finally, the proposed TCB-DPWM and neutral point voltage balancing method are both verified by simulation and experimental results. The results show that the proposed TCB-DPWM can effectively simplify the implementation of modulation and improve system efficiency.**

***Index Terms*—Three-level neutral-point-clamped inverter, voltage source inverter, discontinuous PWM, neutral point voltage balancing.**

I. Introduction

Three-level neutral-point-clamped (3L-NPC) voltage source inverters are widely used in many medium- and high-power applications. Compared with traditional two-level inverters, the 3L-NPC inverter is with better performances of efficiency, harmonics and power capability [1-3]. Recently, the T-type 3L-NPC is proposed to alternate the traditional NPC to improve the efficiency [4] [5]. The topology diagram of a T-type 3L-NPC inverter is shown in Fig.1. The main advantage of the T-type 3L-NPC inverter is the lower voltage rating of the employed devices, as the two switches of neutral point have a peak inverse voltage of half of that required in the conventional 3L-NPC inverter. Furthermore, the structure of T-TYPE 3L-NPC inverter provides lower conduction losses, compared to conventional 3L-NPC of the same ratings [6].

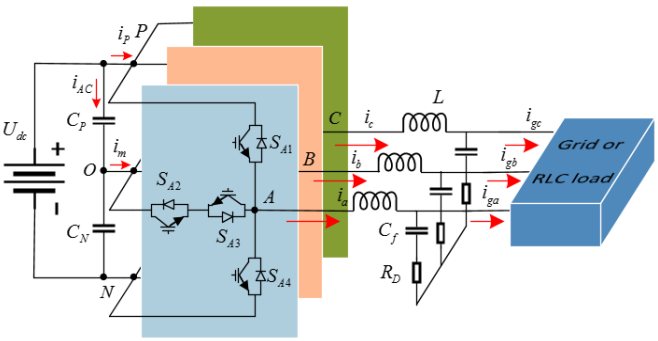

Fig.1. The topology of the T-type 3L-NPC inverter.

It is well-known that the performance of inverter depends on the modulation strategy. In terms of modulation signal forms, modulation strategies can be classified into two categories including continuous PWM (CPWM) and discontinuous PWM (DPWM). In CPWM, the modulating signals are never clamped during the period of the fundamental voltage, whereas in DPWM, the modulating signals could be clamped to constant voltage levels [7]. Sinusoidal triangle pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) are two typical CPWMs which are widely used in many applications because of its low output voltage/current harmonic distortion. For three-phase inverters with DPWM, each phase is clamped to one constant voltage level for one-third of the fundamental period. Thus, compared with the losses of the inverter with CPWM, the switching losses of the inverter with DPWM are significantly reduced at the average of 33.3% [7-8].

The DPWM is successfully used in conventional two-level inverters [7-14]. If different phases are clamped to different voltage levels at different angles of the reference vector, different types of DPWM will be obtained. Generally speaking, there is four basic space vector based DPWMs for two-level inverters: DPWM I [10], DPWM II [11], DPWM III [12], DPWM IV [7]. Different DPWM methods performances difference. With different objectives of optimization, different optimized DPWMs are investigated in literature [7, 13-14]. In order to minimize the switching losses, a direct digital

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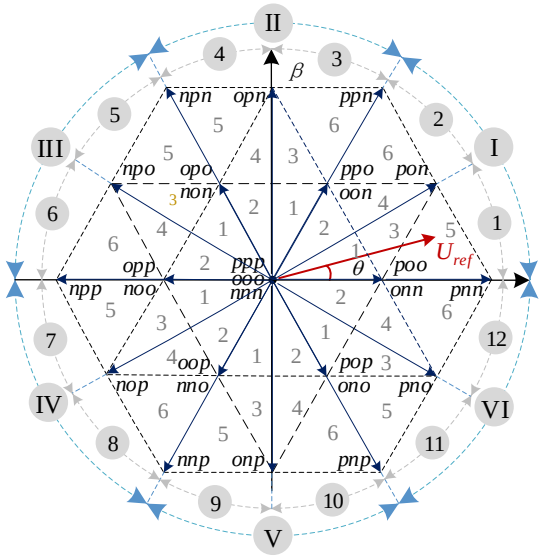
technique implementation of general DPWM (DDT-GDPWM) was proposed in [7]. For the purpose of reducing common mode voltage (CMV), a CMV reduction DPWM (CMVR-DPWM) was proposed in [13-14]. Actually, the space vector base DPWM can be functionally equivalent to sine-triangle carrier based DPWM [15]. In most of the practical applications, the modulation strategy is implemented by a microprocessor or digital signal processor (DSP). However, it is easier to realize sine-triangle carrier based modulation in practical applications.

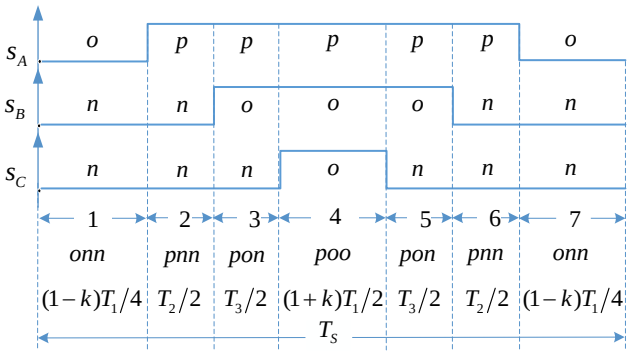
The four basic DPWMs in the two-level inverter, DPWM I-IV, can also be extended to three-level inverters [16-18]. For 3L-NPC inverters with DPWM, an additional option of clamping voltage level is added. The clamped phases can be clamped to positive DC bus or neutral point or negative DC bus [19]. The clamped phases, clamped voltage levels and the clamped durations can also be optimally designed according to the optimization requirements. The DPWMs aimed at reducing the switching losses [18-20], reducing the CMV [20-21] and balancing neutral point voltage [20, 22, 23] were proposed in literature. However, the existing implementation methods of above mentioned DPWMs for three-level inverters are very complex in applications, especially in the above optimization situations because they are based on space vector and requiring three procedures: sector judgment, function time calculation and pulse pattern generation. Although literature [24, 25] adopt triangular carrier based DPWM, the procedures to obtain the final modulation signals are also not easy, because the procedures to calculate CMV are divided into many situations. Furthermore, the equivalent relationship analysis between the TCB-DPWM and SVB-DPWM for 3L-NPC inverters is not seen in the existing literature.

In order to simplify the implementation of space vector based discontinuous PWM, this paper proposes a TCB-DPWM for 3L-NPC inverters. In addition, the relationships between the proposed TCB-DPWM and the conventional SVB-DPWM are mathematically analyzed based on [26]. Different DPWMs can be realized in a unified scheme by setting different values of proportional allocation factor for small vectors in different sectors. In order to demonstrate its applications in optimization situations, a TCB-DPWM based neutral point voltage balancing method is also proposed. The neutral point voltage can be controlled by regulating the polarity of the proportional allocation factor in TCB-DPWM. The proposed TCB-DPWM and the neutral point voltage balancing method are both verified by simulations and experiments.

This article is organized as follows: Conventional SVB-DPWMs are reviewed in Section II. In Section III, the TCB-DPWM and its implementation method for 3L-NPC inverters are proposed. In addition, the relationships of TCB-DPWM and SVB-DPWM are mathematically analyzed. Based on the proposed TCB-DPWM, a neutral point voltage balancing method is investigated in Section IV. The effectiveness of the proposed scheme is verified by simulations and experiments in Section V. Section VI summarizes the conclusions and contributions of this paper.



(a) Vector space.



(b) Pulse patterns.

Fig.2. Vector space and pulse patterns of the 3L-NPC inverter.

II. Conventional SVB-DPWMs For 3L-NPC Inverter

The modulation strategies for the T-type 3L-NPC inverter and conventional 3L-NPC inverter are the same. The proposed modulation strategy is suitable for both types of the 3L-NPC inverter. This paper takes a T-type 3L-NPC inverter shown in Fig.1 as an example to demonstrate the proposed method. C_P and C_N are the DC bus capacitors. U_{dc} denotes the DC voltage. L and C_f are the inductance and capacitor of the LC filter respectively. R_D is the damping resistor of the LC filter. Currents $i_{a,b,c}$ and $i_{ga,gb,gc}$ denote the inverter side and load side three-phase currents respectively. i_m denotes the current flowing out of neutral point O. i_{AC} denotes the current of DC capacitor.

The vector space for the 3L-NPC inverter is shown in Fig.2(a). There are 27 space vectors for 3L-NPC inverters, including 3 zero vectors (*ppp*, *ooo* and *nnn*), 12 small vectors (*poo*, *onn*, *ppo*, *oon*, *opo*, *non*, *opp*, *noo*, *oop*, *nno*, *pop* and *ono*), 6 medium vectors (*pon*, *opn*, *npo*, *nop*, *onp* and *pno*) and 6 long vectors (*pnn*, *ppn*, *npn*, *npp*, *nnp* and *pnp*). For example, the space vector *pon* denotes that the switching states for phase *A*, *B* and *C* are *p*, *o* and *n*, respectively. Switching state *p*, *o* and *n* denote the corresponding phase (*A*, *B*, *C*) is connected to positive DC bus *P*, neutral point *O*, and negative DC bus *N*, respectively. All vectors have 19 locations in the

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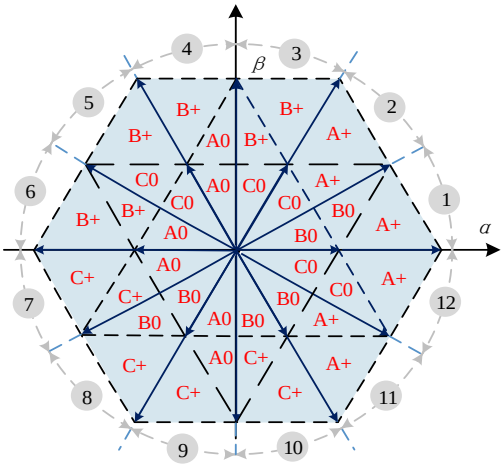
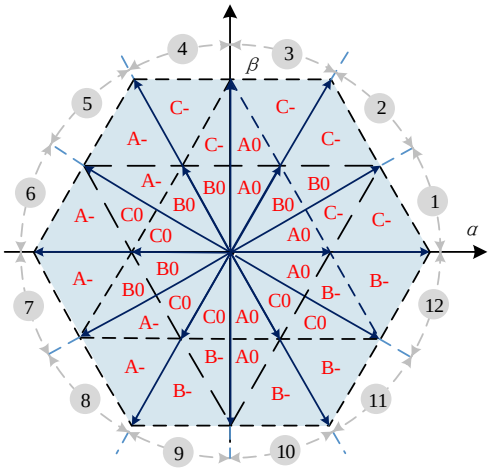
Table I.
The values of k in different sectors for SVB-DPWMs.

SVB-DPWMs	Sectors											
	1	2	3	4	5	6	7	8	9	10	11	12
DPWM I	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1
DPWM II	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1
DPWM III	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
DPWM IV	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1



(a) k=1.



(b) k=-1.

Fig.3. The clamped phases and clamped voltage levels in each sector.

vector space. Zero vectors and small vectors are redundancy vectors [27].

Conventional SVPWM adopts the nearest three vectors to synthesize the reference vector and to generate seven stages pulse patterns [28]. For a reference vector U_{ref} in Fig.2(a), its pulse patterns are shown in Fig.2(b), where the vectors *poo* and *onn* are a couple of redundancy small vectors. In Fig.2(b), k ($-1 \le k \le 1$) is defined as the proportional allocation factor for redundancy small vectors, which determines the following different situations.

1) If k=1: positive small vector *poo* is used, point *A* in Fig.1 is clamped to positive DC bus *P*.

2) If k=-1: negative small vector *onn* is used, point *C* in Fig.1 is clamped to negative DC bus *N*.

3) If -1<k<1: no phase are clamped to any voltage levels.

Normally, when k=1 or k=-1, one of the three phases will be clamped to positive DC bus *P* or neutral point *O* or negative DC bus *N*, thus, DPWM will be obtained. Table I shows four basic SVB-DPWMs including DPWM I~IV [16-18], where k has different values (1 or -1) in different sectors.

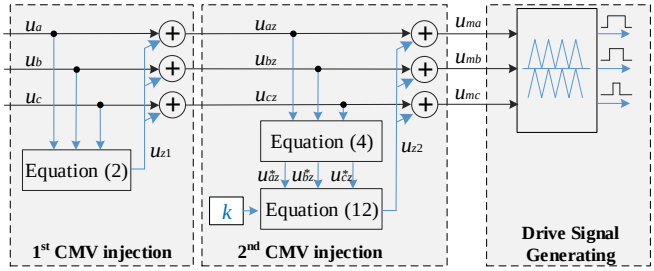


Fig.4. The unified scheme of TCB-DPWM.

Fig.3(a) and Fig.3(b) show the clamped phases and clamped voltage levels for k=1 and k=-1 respectively, where, *A*+ means that point *A* in Fig.1 is clamped to positive DC bus *P*; *A*0 means that point *A* is clamped to neutral point *O*; *A*- means that point *A* is clamped to negative DC bus *N*. For the four basic SVB-DPWMs in Table I, the clamped phase and clamped voltage level can refer to Fig.3 according to the value of k in the corresponding sector.

III. Proposed TCB-DPWM For 3L-NPC Inverter

A. Proposed TCB-DPWM

The TCB-DPWM is proposed, as shown in Fig.4, to simplify the implementation of the SVB-DPWMs through injecting proper CMV to original modulation signals including the 1st CMV injection u_{z1} and the 2nd CMV injection u_{z2}. Three original reference signals u_a, u_b and u_c are the output of the basic voltage/current control [29]. After twice CMV injections, the final modulation signals of u_{ma}, u_{mb} and u_{mc} will be obtained. Drive signals for switching devices are generated by comparing two phase disposition triangle carriers with final modulation signals.

In TCB-DPWM, the definition, meaning and range of k are the same as SVB-DPWM, where, k is the proportional allocation factor of redundancy small vectors. Different PWM methods, as well as SVB-DPWMs, can be obtained by setting different values of k into the unified scheme shown in Fig.4. The functions of inverters with TCB-DPWM and SVB-DPWM are equivalent when the same k are set. The procedure to realize the proposed TCB-DPWM will be interpreted in the following sections.

B. 1st CMV injection

The three reference signals u_a, u_b and u_c in Fig.4 can be expressed by:

$$\begin{cases} u_a = U_m \times \cos(\omega t) = (m \times U_{dc}/\sqrt{3}) \times \cos(\omega t) \\ u_b = U_m \times \cos(\omega t + 2\pi/3) = (m \times U_{dc}/\sqrt{3}) \times \cos(\omega t + 2\pi/3) \\ u_c = U_m \times \cos(\omega t + 4\pi/3) = (m \times U_{dc}/\sqrt{3}) \times \cos(\omega t + 4\pi/3) \end{cases} \quad (1)$$

where, U_m is the peak value of reference voltage, ω is the angular frequency of reference voltage, $m = \sqrt{3}U_m/U_{dc}$ is the modulation index.

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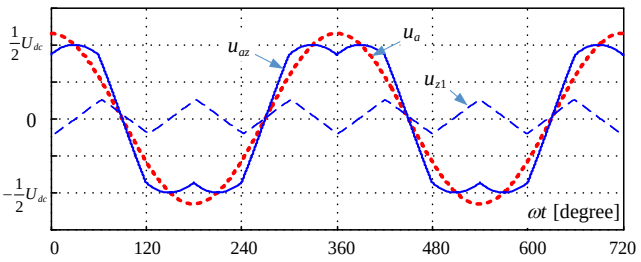

Fig.5. Modulation signals and 1st CMV injection at m=1.

In Fig.4, the 1st CMV injection u_{z1}, as shown in (2), is injected to the original three reference signals to improve the modulation index (DC voltage utilization) to its maximum value 1. The maximum modulation index of the proposed method will be the same as that for SVPWM.

$$u_{z1} = -0.5 \times MAX(u_a, u_b, u_c) - 0.5 \times MIN(u_a, u_b, u_c) \quad (2)$$

where, *MAX* and *MIN* are the functions to obtain the maximum and minimum values, respectively.

After the 1st CMV injection, three modulation signals u_{az}, u_{bz} and u_{cz} are given by

$$u_{xz} = u_x + u_{z1},\ x = a, b, c \quad (3)$$

Fig.5 shows an example of the original modulation signal u_a, the first CMV injection u_{z1} and the modulation signal u_{az} at the maximum value of modulation index. It can be seen from Fig.5 that the modulation signal u_{az} will be located within the reachable voltage band from $-U_{dc}/2$ to $U_{dc}/2$ because of the 1st CMV injection.

C. 2nd CMV injection

The 2nd CMV injection is used to obtain the functional equivalent relationships between SVB-DPWM and TCB-DPWM. If the pulse patterns of SVB-DPWM and TCB-DPWM are the same, the functional equivalent relationships will be achieved.

This section also takes the reference vector U_{ref} shown in Fig.2(a) as an example; its pulse patterns are replotted in Fig.6(a). For a three-level inverter, two phase disposition triangle carriers u_t^+ and u_t^-, as shown in Fig.6(b), are used to generate the pulse patterns. The laws to generate pulse patterns are as follows [15]:

1) Case a: if modulation signal is bigger than positive carrier u_t^+, switching state *p* will be generated.

2) Case b: if modulation signal is smaller than negative carrier u_t^-, switching state *n* will be generated.

3) Case c: if modulation signal is bigger than negative carrier u_t^- and smaller than positive carrier u_t^+, switching state *o* will be generated.

In order to generate the same pulse patterns shown in Fig.2(a), the final modulation signals of TCB-DPWM for each phase should be u_{ma}, u_{mb} and u_{mc} as shown in Fig.6(b).

However, it is very difficult to obtain the relationship of u_{mx} and u_{xz} in the frame of two phase disposition triangle carriers. In order to simplify the procedure, a conversion defined in (4) is used to convert the frame of two phase disposition triangle carriers to the frame of one virtual common triangle carrier.

$$u^* = \begin{cases} u - U_{dc}/4, & if\ u \ge 0 \\ u + U_{dc}/4, & if\ u < 0 \end{cases} \quad (4)$$

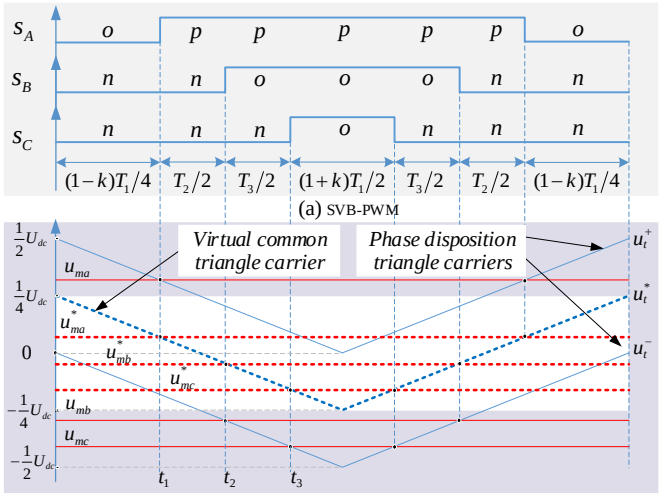

Fig.6. Relationships between SVB-PWM and TCB-PWM.

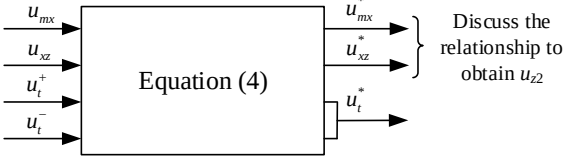

Fig.7. Signals conversion.

As shown in Fig.7, modulation signals u_{mx}, u_{xz} are converted to u_{mx}^*, u_{xz}^*, respectively. The two phase disposition triangle carriers u_t^+ and u_t^- are converted to one virtual common triangle carrier u_t^*.

The relationships of u_{mx}^* and u_{xz}^* will be discussed in the frame of one virtual common triangle carrier to obtain the 2nd CMV injection u_{z2}. In the frame of one virtual common triangle carrier, the CMV injection is labeled as u_{z2}^*. Thus, the relationships of u_{mx}^* and u_{xz}^* are given by:

$$u_{mx}^* = u_{xz}^* + u_{z2}^*,\ x = a, b, c \quad (5)$$

After the conversions, modulation signals and triangle carrier are all located in the common voltage band from $-U_{dc}/4$ to $U_{dc}/4$ as shown in the white background zone of Fig.6(b). According to the virtual common triangle carrier in Fig.6(b), its mathematical equation in $t \in [0, T_s/2]$ can be expressed as follows:

$$u_t^*(t) = \frac{U_{dc}}{4} \times (1 - \frac{4}{T_s} \times t),\ 0 \le t \le \frac{T_s}{2} \quad (6)$$

where $u_t^*(t)$ is the instantaneous value of u_t^* at the time of t, T_s is the carrier wave period.

As shown in Fig.6(b), u_{ma}^*, u_{mb}^* and u_{mc}^* are the values of $u_t^*(t)$ at the instant of t_1, t_2 and t_3, respectively.

$$\begin{cases} u_{ma}^* = u_t^*(t_1),\ t_1 = \dfrac{1-k}{4} \times T_1 \\ u_{mb}^* = u_t^*(t_2),\ t_2 = t_1 + \dfrac{1}{2} \times T_2 \\ u_{mc}^* = u_t^*(t_3),\ t_3 = t_2 + \dfrac{1}{2} \times T_3 \end{cases} \quad (7)$$

According to the similar triangles in Fig.6(b), the following equations can be obtained:

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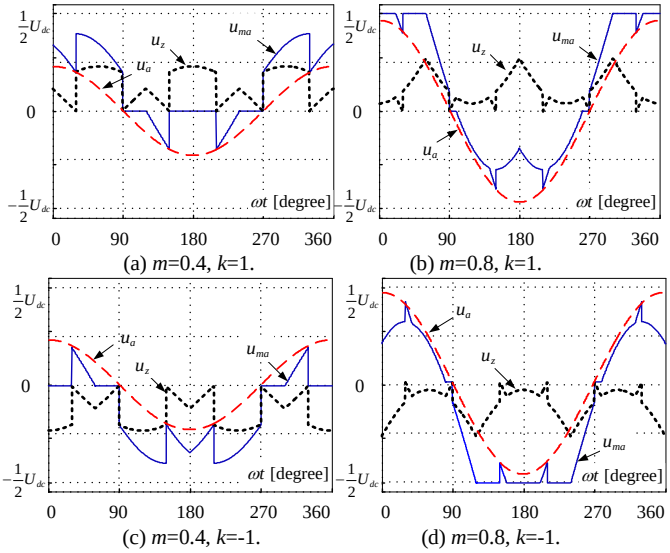

(a) m=0.4, k=1. (b) m=0.8, k=1.

(c) m=0.4, k=-1. (d) m=0.8, k=-1.

Fig.8. Modulation signals and total CMV injection of TCB-DPWM.

$$\begin{cases} 0.5\times U_{dc}\times T_2=\left(u_{ma}^*-u_{mb}^*\right)\times T_s \\ 0.5\times U_{dc}\times T_3=\left(u_{mb}^*-u_{mc}^*\right)\times T_s \\ T_1=T_s-T_2-T_3 \end{cases} \tag{8}$$

According to (5), in the frame of one virtual common triangle carrier, the relative positions of two modulation signals of u_{mx}^* are the same as the relative positions of the corresponding two modulation signals of u_{xz}^*. Thus, the following equations can be obtained.

$$\begin{cases} u_{ma}^*-u_{mb}^*=u_{az}^*-u_{bz}^* \\ u_{mb}^*-u_{mc}^*=u_{bz}^*-u_{cz}^* \end{cases} \tag{9}$$

According to the equations (5) ~ (9), the CMV injection u_{z2}^* in the frame of one virtual common triangle carrier can be obtained.

$$u_{z2}^*=-\frac{1+k}{2}\times u_{az}^*-\frac{1-k}{2}\times u_{cz}^*+k\times\frac{U_{dc}}{4} \tag{10}$$

In the example sector, u_{az}^* and u_{cz}^* are the maximum and minimum values of u_{xz}^*, respectively.

Similarly, for a reference vector in other sectors, similar conclusions can also be obtained. In summary, the CMV injection u_{z2}^* in the frame of one virtual common triangle carrier is given by:

$$\begin{aligned} u_{z2}^*=&-\frac{1+k}{2}\times MAX\left(u_{az}^*,u_{bz}^*,u_{cz}^*\right) \\ &-\frac{1-k}{2}\times MIN\left(u_{az}^*,u_{bz}^*,u_{cz}^*\right)+k\times\frac{U_{dc}}{4} \end{aligned} \tag{11}$$

Converting u_{mx}^* and u_{xz}^* to the frame of two phase disposition triangle carriers according to reverse conversion of (4), it will be obtained that the CMV injection u_{z2}^* is equal to the 2nd CMV injection u_{z2}. Thus, the 2nd CMV injection is given by:

$$\begin{aligned} u_{z2}=&-\frac{1+k}{2}\times MAX\left(u_{az}^*,u_{bz}^*,u_{cz}^*\right) \\ &-\frac{1-k}{2}\times MIN\left(u_{az}^*,u_{bz}^*,u_{cz}^*\right)+k\times\frac{U_{dc}}{4} \end{aligned} \tag{12}$$

The total CMV injection u_z can be obtained

$$u_z=u_{z1}+u_{z2} \tag{13}$$

Table II.
Computation burden comparison.

	Operation					Total
	Plus/ Minus	Mult.	Shifts	Comp.	Lookup Tables	
Proposed	10	3	3	9	0	34
SVB-DPWM	18	16	5	0	1	>87

After the twice CMV injections, three target modulation signals of TCB-PWM u_{ma}, u_{mb} and u_{mc} can be obtained:

$$u_{mx}=u_x+u_z,\ x=a,b,c \tag{14}$$

Fig.8 shows the modulation signals generated by the proposed TCB-DPWM when m=0.4, 0.8 and k=1, -1. The red dash line u_a is the original reference signal of phase A. The black dotted line u_z is the total CMV injection. The blue solid line u_{ma} is the final modulation signal to drive signal generating module. The final modulation signals in Fig.8 are consistent with the clamped phase and clamped voltage levels in Fig.3.

D. Discussions

According to the above analysis, the procedures to realize the proposed TCB-DPWM just need a few arithmetic operations to obtain the final modulation signals and will be very easy to implement in applications. On the contrary, the procedures to realize SVB-DPWM are more complex, which require three procedures: sector judgment, function time calculation and pulse pattern generation.

In practical applications, the control and modulation strategies for inverters are realized by a microprocessor or digital signal processor. The computation burden for the proposed strategy and SVPWM are summarized in Table II.

As shown in Table II, the proposed algorithm may require about 34 machine cycles for the microprocessor in one carrier wave period. However, in the conventional SVB-DPWM methods such as [16-18], it would require more than 87 machine cycles for microprocessor in one carrier wave period, which is more than two times of that in the proposed method.

IV. Proposed TCB-DPWM Based Neutral Point Voltage Balancing Method

In this paper, neutral point voltage balancing is used to demonstrate the application of the proposed TCB-DPWM. Among different method of neutral point voltage balancing for 3L-NPC, controlling the function time of redundant small vectors is the simplest and most effective method from the space vector modulation point of view [30]. Based on the same basic idea and the proposed TCB-DPWM, this paper proposes an equivalent implement method as hysteresis control in [30] from the triangle carrier modulation point of view. It should be noted that there is some literature [31, 32] adopting DPWM to control the neutral point voltage. The DPWM in these papers is based on once offset injection. Its maximum modulation index is not as high as the proposed method.

A. Analysis of Neutral Point Voltage

As shown in Fig.1, the voltage of C_P and C_N are U_P and U_N. Thus, the voltage difference ΔU_C of DC side capacitors is given by:

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Table III.
The relationships between ΔU_C and i_m.

If	Then		
i_m>0	U_N↓	U_P↑	ΔU_C↓
i_m<0	U_N↑	U_P↓	ΔU_C↑

$$\Delta U_C = U_N - U_P \tag{15}$$

The value of ΔU_C depends on the neutral point current i_m. As shown in Table III, when $i_m > 0$, current flows out of neutral point O, the voltage U_N of C_N will lower, the voltage U_P of C_P will arise. Thus, the difference voltage ΔU_C of DC side capacitor will reduce. Similarly, when $i_m < 0$, current flows into neutral point O, the voltage U_N of C_N will arise, the voltage U_P of C_P will lower, thus, the difference voltage ΔU_C of DC side capacitor will arise. The neutral point voltage can be controlled by controlling the neutral point current i_m.

When the switching state of one phase is o, its current will flow into or out of the neutral point O. Thus, the neutral point current i_m is determined by the magnitude and polarity of the corresponding phase current and the function time of switching state o. As shown in Fig.6, the function time of switching state o in a switching period is normally determined by the modulation signal as

$$T_{xo} = (1 - \frac{|u_{mx}|}{U_{dc}/2}) \times T_s,\ x = a,b,c \tag{16}$$

where, T_{xo} is the function time of switching state o caused by the modulation signal u_{mx}.

Suppose that the current flowing out of bridge is positive, as shown in Fig.1, the average neutral point current in a switching period can be obtained.

$$\begin{aligned} \bar{i}_m &= \frac{1}{T_s}\left(i_a T_{ao} + i_b T_{bo} + i_c T_{co}\right) = \\ & i_a\left(1 - \frac{|u_{ma}|}{U_{dc}/2}\right) + i_b\left(1 - \frac{|u_{mb}|}{U_{dc}/2}\right) + i_c\left(1 - \frac{|u_{mc}|}{U_{dc}/2}\right) \end{aligned} \tag{17}$$

For a three-wire three-phase inverter, the sum of i_a, i_b and i_c is zero. Thus, equation (17) can be simplified as:

$$\begin{aligned} \bar{i}_m &= \frac{2}{U_{dc}}\left(-i_a \times |u_{ma}| - i_b \times |u_{mb}| - i_c \times |u_{mc}|\right) \\ &= \frac{2}{U_{dc}}\left(-i_a \times |u_{az} + u_{z2}| - i_b \times |u_{bz} + u_{z2}| - i_c \times |u_{cz} + u_{z2}|\right) \end{aligned} \tag{18}$$

According to Section III, it can be observed that the modulation waves of u_x, u_{xz} and u_{mx} have the same polarity because the added CMV will not change the polarity of each modulation signals. For example, if $u_a \geq 0$, then $u_{az} \geq 0$ and $u_{ma} \geq 0$; if $u_a \leq 0$, then $u_{az} \leq 0$ and $u_{ma} \leq 0$. Thus, $\bar{i}_m$ in (18) can be discussed according to the polarity of the original reference voltage u_x. According to Fig.2(a) and (18), it can be seen that the polarity of u_x and the average neutral point current $\bar{i}_m$ will have six situations as listed in Table IV.

According to Table IV, (18) can be rewritten as:

$$\begin{aligned} \bar{i}_m &= \frac{2}{U_{dc}}\left(-sign(u_a) i_a u_{az} - sign(u_b) i_b u_{bz} - sign(u_c) i_c u_{cz}\right) \\ &+ \frac{4}{U_{dc}}\left(-sign(u_j) i_j u_{z2}\right) \end{aligned} \tag{19}$$

where, $sign()$ is the function to acquire the sign of input. j ($j \in$ {a, b, c}) is the related phase that can affect the neutral point voltage, the values of j in different sectors are: j =a, in sectors 1, 6, 7 and 12; j=b, in sectors 4, 5, 10 and 11; j=c, in sectors 2, 3, 8 and 9.

Table IV.
The average neutral point current in different situations.

Sectors	Voltage relation.	$\bar{i}_m$	j
12 & 1	u_a>0, u_b<0, u_c<0	$\frac{2}{U_{dc}}\left(\underbrace{-i_a \times u_{az} + i_b \times u_{bz} + i_c \times u_{cz}}_{\text{Output reference part}} \underbrace{-2i_a \times u_{z2}}_{\text{Controlled part}}\right)$	a
2 & 3	u_a>0, u_b>0, u_c<0	$\frac{2}{U_{dc}}\left(\underbrace{-i_a \times u_{az} - i_b \times u_{bz} + i_c \times u_{cz}}_{\text{Output reference part}} \underbrace{+2i_c \times u_{z2}}_{\text{Controlled part}}\right)$	c
4 & 5	u_a<0, u_b>0, u_c<0	$\frac{2}{U_{dc}}\left(\underbrace{i_a \times u_{az} - i_b \times u_{bz} + i_c \times u_{cz}}_{\text{Output reference part}} \underbrace{-2i_b \times u_{z2}}_{\text{Controlled part}}\right)$	b
6 & 7	u_a<0, u_b>0, u_c>0	$\frac{2}{U_{dc}}\left(\underbrace{i_a \times u_{az} - i_b \times u_{bz} - i_c \times u_{cz}}_{\text{Output reference part}} \underbrace{+2i_a \times u_{z2}}_{\text{Controlled part}}\right)$	a
8 & 9	u_a<0, u_b<0, u_c>0	$\frac{2}{U_{dc}}\left(\underbrace{i_a \times u_{az} + i_b \times u_{bz} - i_c \times u_{cz}}_{\text{Output reference part}} \underbrace{-2i_c \times u_{z2}}_{\text{Controlled part}}\right)$	c
10 & 11	u_a>0, u_b<0, u_c>0	$\frac{2}{U_{dc}}\left(\underbrace{-i_a \times u_{az} + i_b \times u_{bz} - i_c \times u_{cz}}_{\text{Output reference part}} \underbrace{+2i_b \times u_{z2}}_{\text{Controlled part}}\right)$	b

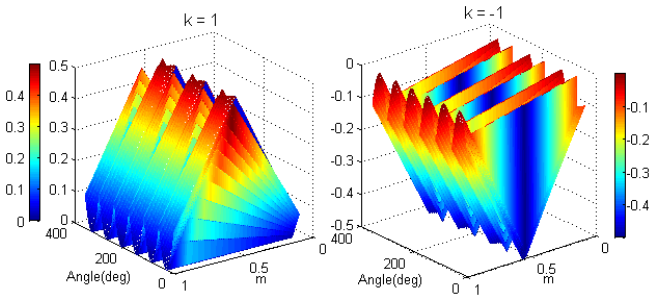

Fig.9. Value of u_{z2} at different m and different θ(normalized by U_{dc}/2)

Table V.
The relationships between k and $\bar{i}_m$ in different conditions.

If				Then	
k	u_{z2}	$sign(u_j)i_j$	$sign(u_j i_j)$	$-sign(u_j)i_j \times u_{z2}$	$\bar{i}_m$
1	≥0	>0	1	≤0	↓
		<0	-1	≥0	↑
-1	≤0	>0	1	≥0	↑
		<0	-1	≤0	↓

From (19), it can be obviously seen that the $\bar{i}_m$ can be regulated by u_{z2}, while the value of u_{z2} can be decided by k as:

1) k=1, then

$$u_{z2(k=1)} = \frac{U_{dc}}{4} - MAX(u_{az}^*, u_{bz}^*, u_{cz}^*) \tag{20}$$

2) k=-1, then

$$u_{z2(k=-1)} = MIN(u_{az}^*, u_{bz}^*, u_{cz}^*) - \frac{U_{dc}}{4} \tag{21}$$

The second CMV injection u_{z2} at different modulation index m and different reference voltage angle θ are shown in Fig.9. According to (20), (21) and Fig.9, it can be obtained that the polarity of u_{z2} is determined by the polarity of k. In other words, when k=1, $u_{z2} \geq 0$; when k=-1, $u_{z2} \leq 0$.

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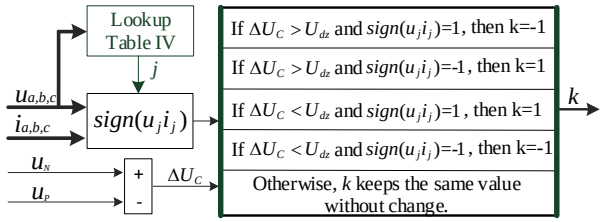


Fig.10. Proposed TCB-DPWM based neutral point voltage balancing method.

Table VI.
Parameters in simulation and experiment.

System Parameters	Value
Filter inductance L	1.2mH;
Filter capacitor C_f	20μF;
Damping Resistance R_D	0.5Ω;
Switching frequency f_s	9k Hz;
Carrier wave period T_s	111μs
AC frequency	50Hz;
Dead time	3μs.

According to above analysis, the average neutral point current $\bar{i}_m$ can be regulated by k as shown in Table V. It can be observed that $\bar{i}_m$ can be controlled to increase or decrease by setting different values of k according to the polarity of $u_j i_j$. Thus, the neutral point voltage can be controlled by k according to Table III and Table V.

B. *Proposed Neutral Point Voltage Balancing Method*

According to the above analysis, the TCB-DPWM based neutral point voltage control method is shown in Fig.10. The capacitor voltage balancing is controlled by the regulation of k. The value of k is calculated by the proposed control strategy according to three phase currents i_{abc}, reference voltage signals u_{abc} and the DC capacitor voltages u_N, u_P. The reference voltages u_{abc} is used to obtaining the related phase j by looking up Table IV. Then, according to the polarity of $u_j i_j$ and the voltage difference ΔU_C, the value of k can be obtained by the logic judgment in Fig.10. Finally, drive signals are generated by the proposed TCB-DPWM according to the value of k. Note that U_{dz} (U_{dz}>0) is the threshold value and can also be seen as the acceptable deviation of neutral point voltage.

In summary, the proposed strategy for controlling the neutral point voltage is shown as follows:

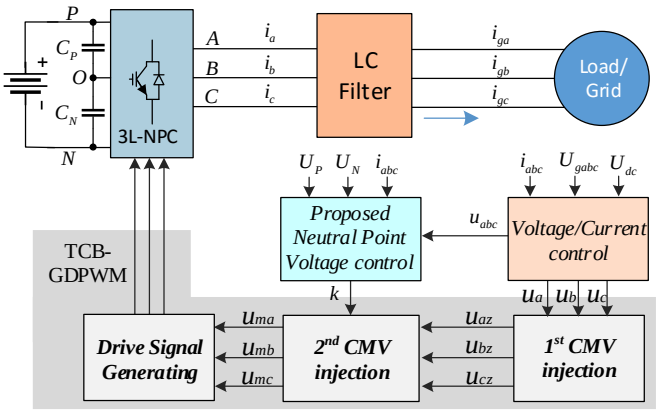
1) Case a: If $\Delta U_c > U_{dz}$ and $sign(u_j i_j)$=1, k is set to -1, then, the average neutral point current $\bar{i}_m$ will increase, ΔU_C will decrease.

2) Case b: If $\Delta U_c > U_{dz}$ and $sign(u_j i_j)$=-1, k is set to 1, then, the average neutral point current $\bar{i}_m$ will increase, ΔU_C will decrease.

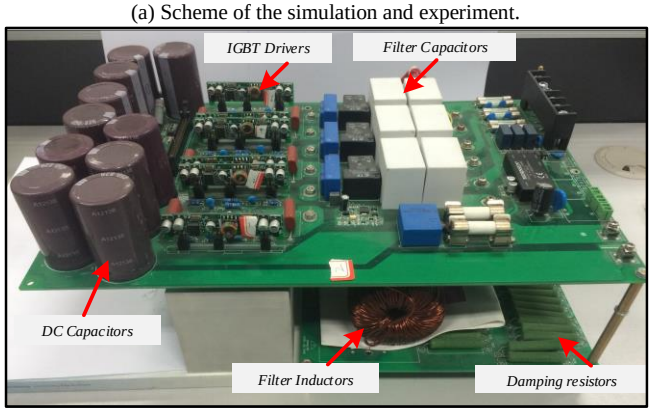
3) Case c: If $\Delta U_c < -U_{dz}$ and $sign(u_j i_j)$=1, k is set to 1, then, the average neutral point current $\bar{i}_m$ will decrease, ΔU_c will increase.

4) Case d: If $\Delta U_c < -U_{dz}$ and $sign(u_j i_j)$=-1, k is set to -1, then, then, the average neutral point current $\bar{i}_m$ will decrease, ΔU_c will increase.

5) Case e: If ΔU_c and $sign(u_j i_j)$ are not the above four situations, the value of k will not be changed.



(a) Scheme of the simulation and experiment.



(b) The figure of the experimental platform.

Fig.11. Simulation and experimental setup.

V. Simulation and Experimental Validation

A. *Simulation and Experimental Platform*

A Matlab/Simulink model and experimental platform are used to validate the effectiveness of the proposed methods. The scheme of simulation and experiment are shown in Fig.11(a).

Both the main circuits in simulation and experiment are T-type 3L-NPC inverters with LC filter. The simulation and experiment are tested in inverter mode with passive load or utility grid. DC voltage is supplied by a DC power source. The experimental platform is shown in Fig.11(b). In the experiment, control and modulation strategies are realized by a DSP (TMS320F28335). The switches and diodes in each phase are standard T-type three-level module M260F produced by Vincotech company. Inverters parameters and control parameters are shown in Table VI.

B. *Validation of the Proposed TCB-DPWM*

In order to validate the proposed TCB-DPWM, simulation and experimental results are shown in Fig.12. The simulation and experimental results are tested in inverter open loop mode with a resistive load to avoid the negative affection caused by both the current control and utility grid. The DC voltage is 100V. Both of DC capacitors C_P and C_N are 4100μF. The modulation index m is 0.8. Four basic DPWMs, realized by the unified scheme of Fig.4, are tested to validate the proposed TCB-DPWM.

As shown in Fig.12, the output phase voltage to neutral point O u_{AO}, the difference of DC capacitors ΔU_c, the current

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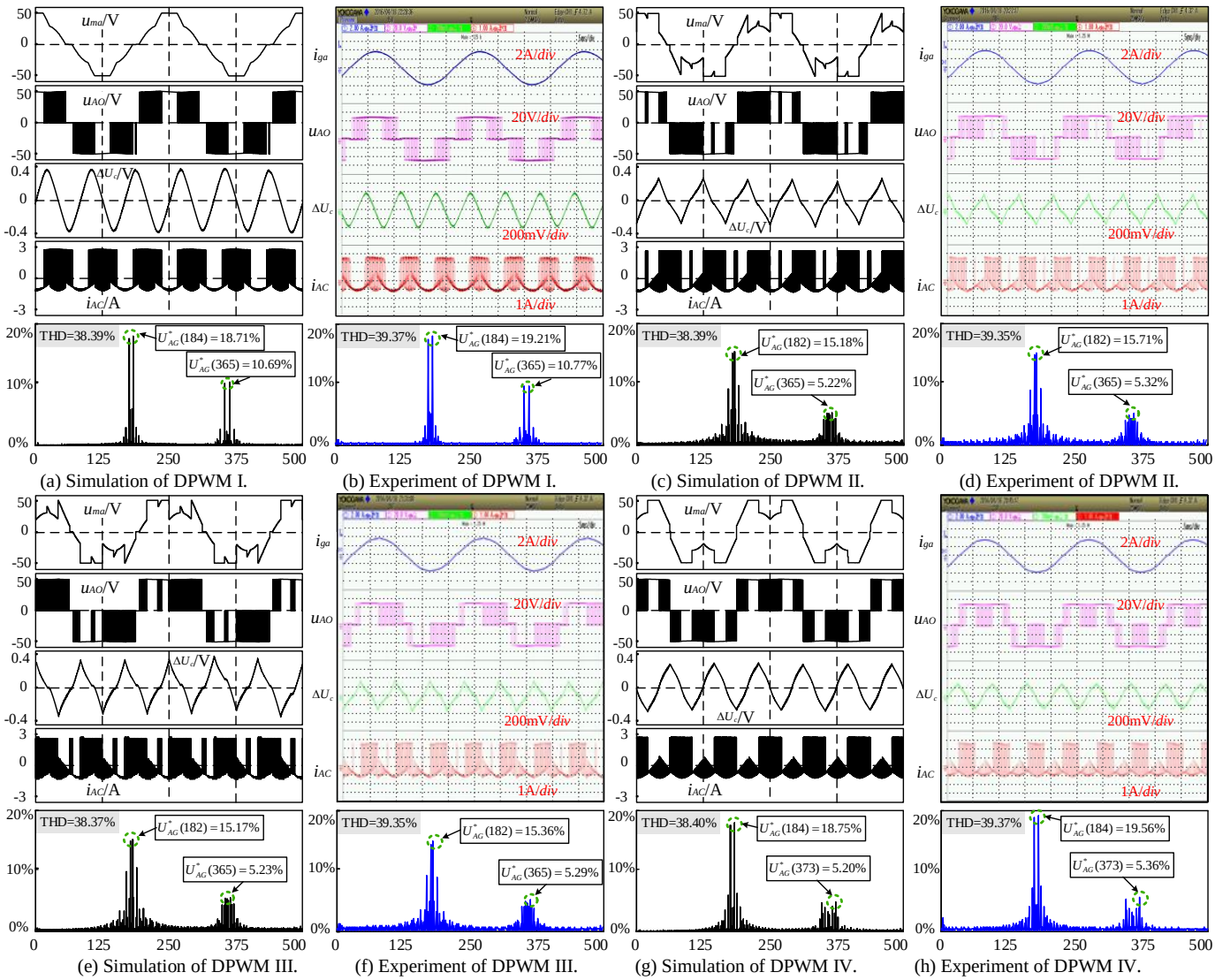

Fig.12. Simulation and experimental results for the proposed TCB-DPWM

of DC capacitor i_{AC} and the frequency spectrum for u_{AG} (output phase voltage to neutral star point of load) are measured in both simulations and experiments. In addition, the modulation waveform u_{ma}, the output phase current i_{ga} are measured in simulations and experiments, respectively.

The waveforms u_{ma} and u_{AO} show that phase A is clamped to the positive bus or neutral point or negative bus in different sectors (refer to Fig.3). The difference of DC capacitors ΔU_C fluctuates at the frequency of three times of the fundamental frequency. However, the phases of ΔU_C for different DPWMs are different. For example, the waveforms of ΔU_C for DPWM II and DPWM III have almost 180° phase shift. That means that k=1 and k=-1 have opposite functions on neutral point voltage. This phenomenon means that the neutral point voltage can be controlled by k. Meanwhile, these results verify the analysis of neutral point voltage in Section IV. The total harmonic distortions (THDs) of output phase voltage u_{AG} are from 38.37% to 39.37%. As we know, the maximum harmonic component for SVPWM is the twice switching frequency harmonic (360th). While for the proposed strategy, the biggest harmonic component is located at the switching frequency(180th). Since filter has higher harmonic attenuation at higher frequency, the THD of grid/load side current of inverter with proposed strategy will be bigger than that of SVPWM. After the LC filter, the output phase currents i_{ga} for each DPWM methods show a good sinusoidal output wave. Both the simulation and experimental results are consistent with the theoretical analysis.

C. Validation of the Proposed TCB-DPWM based Neutral Point Voltage Balancing Method

In order to validate the proposed TCB-DPWM based neutral point voltage balancing method, simulation results are given in Fig.13. The simulations are tested in inverter mode with RL load at the DC voltage of 600V. The value of DC capacitors C_P and C_N are 4100μF(820μF×5) and 3280μF (820μF×4) respectively. U_{dz} is set as 1.5V. Waveforms in the Fig.13 from up to down are: modulation wave u_{ma}, proportional allocation factor k, output voltage u_{AO}, output phase current i_{ga}, DC capacitor voltage U_N with a U_{dc}/2 shift.

At the beginning of the simulations, standard SVPWM are used. Because of the different values of DC capacitor, the neutral point voltages are unbalanced. The proposed neutral point voltage control method starts to work at 0.1s. The

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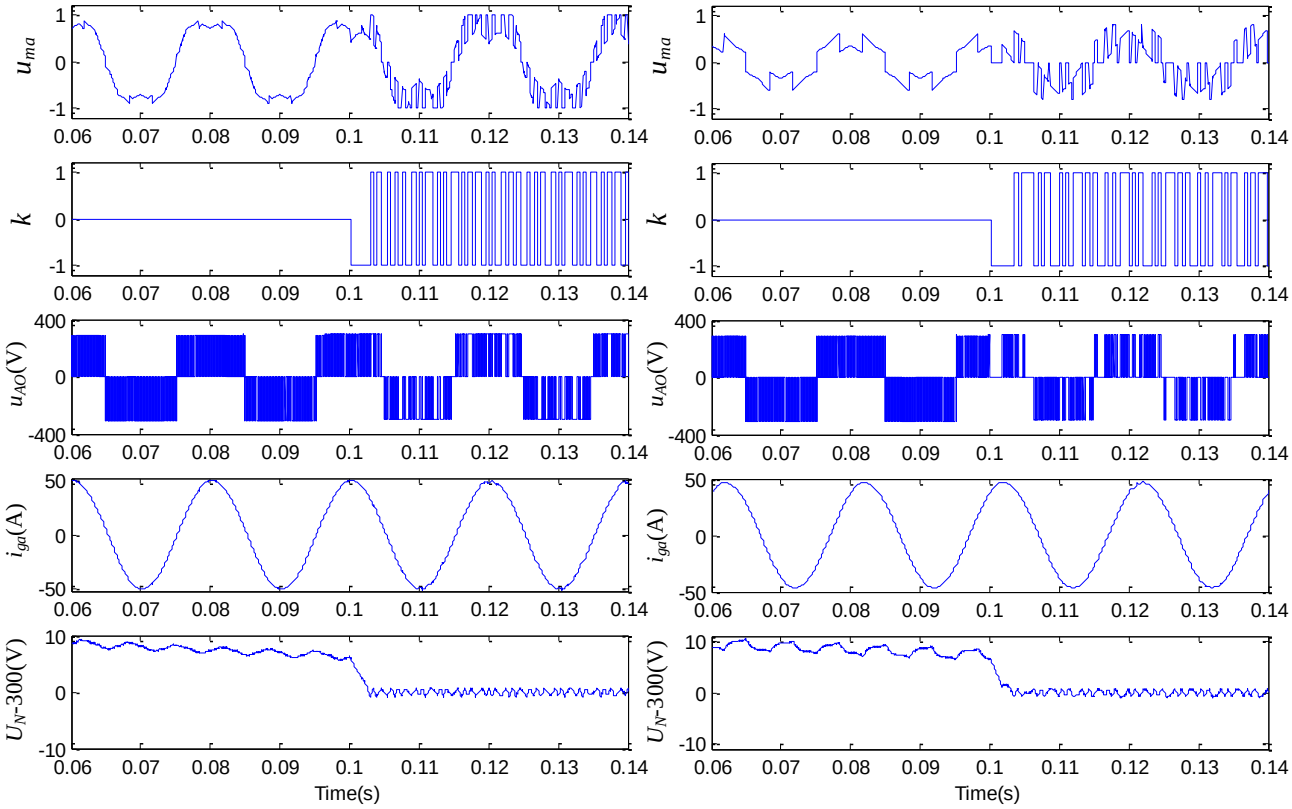

(a) m=0.8, power factor angle φ=0.

(b) m=0.4, power factor angle φ=30.

Fig.13. Simulation results of the TCB-DPWM based neutral point voltage control.

Table VII.
Performance comparisons.

Test conditions	Parameters	
	THD	SLF
m = 0.8, φ = 0, t < 0.1	1.03%	1
m = 0.8, φ = 0, t > 0.1	1.96%	0.66
m = 0.4, φ = 30, t < 0.1	0.43%	1
m = 0.4, φ = 30, t > 0.1	1.35%	0.71

neutral point voltage can be adjusted to balance in about two milliseconds. It can be seen from the result that the neutral point voltages are controlled very well and just fluctuates in a small range of -1.5~ 1.5V. The output voltage u_{AO} can be clamped to positive voltage or negative voltage at m=0.8. The output voltage u_{AO} can be clamped to neutral point voltage at m=0.4. Thus, the switching losses will be greatly reduced because of the great reduced number of power devices switching in the clamped phase.

In order to evaluate other performances of the TCB-DPWM, the performance comparisons in THD of output current and switching losses function (SLF) [33] are shown in Table VII. It shows that the switching losses are greatly reduced (more than 29%) with the proposed method. The cost to achieve this goal is the slightly harmonic distortion increase (less than 0.93%).

In order to validate the proposed TCB-DPWM based neutral point voltage balancing method, experimental results are shown in Fig.14 and Fig.15. Fig.14 is tested in the situation of m=0.8, φ=0. While, Fig.15 is tested in the situation of m=0.8, φ=30. The experimental results are tested in grid tied inverter mode at the DC voltage of 300V. DC capacitors C_P are consisted of 5 capacitors with a rated value of 820μF. DC capacitors C_N are consisted of 4 capacitors with a rated value of 820μF. U_{dz} is set as 0.5V. Waveforms in the experimental results from up to down are: output phase voltage to neutral point O u_{AO}, voltage of DC bus capacitor U_P, voltage of DC bus capacitor U_N, output phase current i_{ga}.

As shown in Fig.14(a) and Fig.15(a), standard SVPWMs without neutral point voltage control are used at the beginning of the experiment. Because the voltages of the upper capacitor are bigger than the voltage of the lower capacitor, the voltages of DC capacitors are unbalanced. The output current is greatly distorted because of the unbalance neutral point voltage. When the proposed TCB-DPWM based neutral voltage balancing method starts working, the voltages of DC capacitors become balanced. When the neutral point voltages are balancing, the waveform of u_{AO} become better, at the same time, the distortion of output current becomes smaller. As shown in Fig.14(b) and Fig.15(b), the neutral point voltages keep balancing even when the output current reference step changes. The results show the proposed method are effective in neutral point voltage balancing.

In order to validate the proposed method in low switching frequency condition, Fig.16 shows the results at f_s=2kHz. As shown in Fig.16, standard SVPWMs without neutral point voltage control are used at the beginning of the experiment. The output current is greatly distorted because of the

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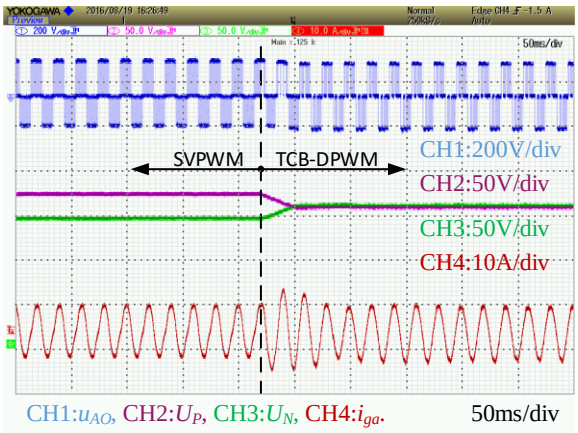
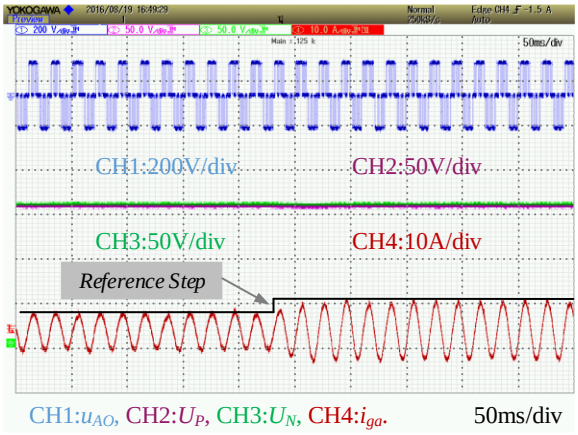
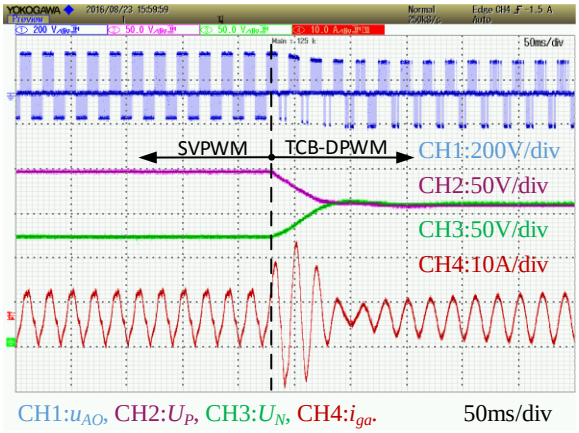


(a) Constant power output.

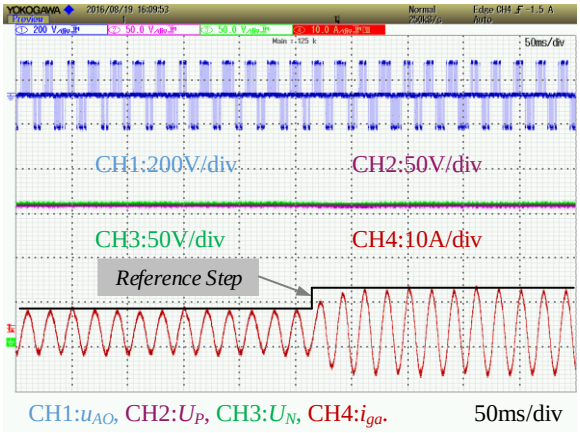


(b) Power output step.

Fig.14. Experimental results neutral point voltage control at m=0.8, φ=0 (f_s=9kHz).

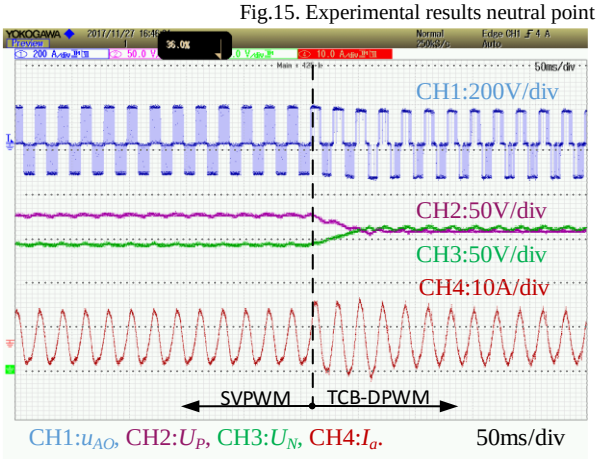


(a) Constant power output.

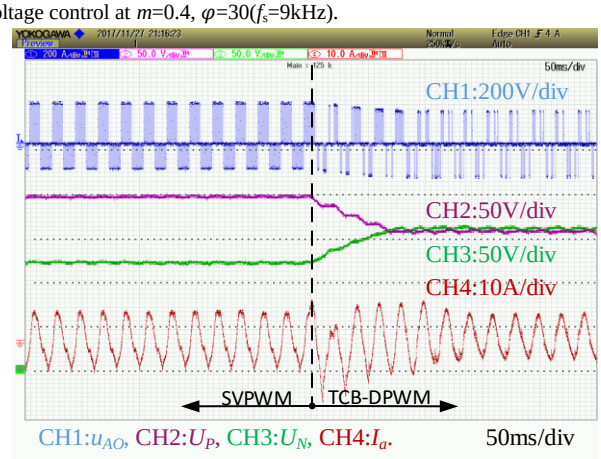


(b) Power output step.

Fig.15. Experimental results neutral point voltage control at m=0.4, φ=30(f_s=9kHz).



(a) m=0.8, φ=0.



(b) m=0.4, φ=30.

Fig.16. Experimental results neutral point voltage control at the low switching frequency(f_s=2kHz).

unbalance neutral point voltage. When the proposed TCB-DPWM based neutral voltage balancing method starts working, the voltages of DC capacitors become balanced. When the neutral point voltages are balancing, the waveform of u_{AO} become better. Meanwhile, the distortion of output current becomes smaller. Although the neutral point voltage fluctuations become higher than that in high switching frequency, the neutral point voltage is acceptable.

It is worth noting that the essence of the proposed neutral point voltage balancing method is allocating redundancy small vectors. The proposed method has the same limitation as for the method of allocating redundancy small vectors. This limitation on neutral point voltage balancing is discussed in many papers, for example Fig.9 in [30] and Fig.8 in [34]. The proposed method in this paper provides another way to realize the neutral point voltage balancing. For a given value of k, the computation time for the proposed TCB-DPWM strategy is 6.7μs in a DSP with CPU frequency of 80MHz. The calculation of k for the proposed neutral point voltage balancing method needs 8.8μs. While for the vector base PWM without neutral point voltage balancing, the

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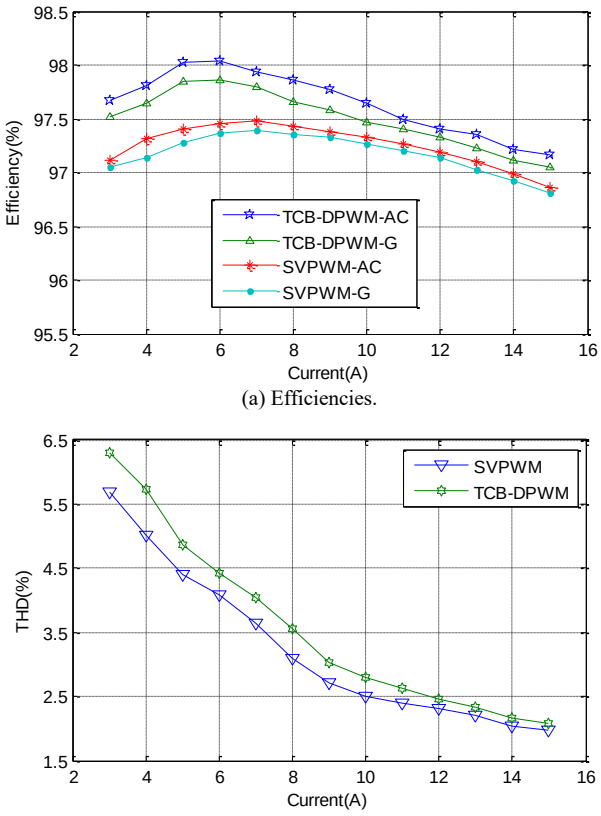

(a) Efficiencies.

(b) Total harmonic distortions.

Fig.17. Performance comparisons for SVPWM and TCB-DPWM.

computation time is 19.2μs. The advantage of the proposed method is easy implementation and low computation burden.

In order to evaluate other performances of the TCB-DPWM, efficiencies of inverters and THDs of grid current are shown in Fig.17, which are tested in the conditions of the same rated values of DC capacitor ($C_P = C_N = 5 \times 820\mu F$) to avoid the affections by the neutral point voltage unbalance.

In Fig.17(a), the suffix –AC denotes the efficiency of the inverter disregarding the power losses of the LC filter, the suffix –G denotes the efficiency of the inverter including the power losses of the LC filter. Curves of SVPWM-AC and TCB-DPWM-AC are efficiencies of the inverter with conventional SVPWM and proposed TCB-DPWM, respectively. Curves of SVPWM-G and TCB-DPWM-G are efficiencies of the inverter with conventional SVPWM and proposed TCB-DPWM, respectively. Both the efficiencies of TCB-DPWM-AC and TCB-DPWM-G are higher than that of SVPWM-AC and SVPWM-G. The efficiency of TCB-DPWM-G is higher than SVPWM-G for 0.2 to 0.5 percentages. When the grid current increase, the change of k will increase, and the efficiency improvement is lower. The reason for lower efficiency improvement is that a turn on and turn off will occur every time of k changing. Fig.17(b) shows the THD curves of inverters with SVPWM and the proposed TCB-DPWM. The THD of the proposed TCB-DPWM is slightly higher than that of SVPWM. At the rated power point (15A), the THD for SVPWM is 1.98%, while, the THD for the proposed method slightly increase to 2.09%. When one phase voltage is clamped, the pulse pattern is changed from seven segments to five segments. From the Harmonic Distortion Factor point of view in [15], the symmetric center distribution of redundancy small vectors can minimize the harmonic flux trajectories. Thus, SVPWM will have better performance in harmonic distortion than TCB-DPWM. Thus, the cost for neutral point voltage balance and efficiency improvement is the slightly harmonic distortion increase.

VI. Conclusion

This paper proposed a triangle carrier based discontinuous PWM for 3L-NPC inverters. Different types of DPWM can be obtained by setting proportional allocation factor k into the proposed unified scheme of TCB-DPWM. The proposed method effectively simplified the implementations of convention SVB-DPWMs. The proposed TCB-DPWM was verified by simulation and experimental results. In addition, a neutral point voltage balancing method was investigated based on the proposed TCB-DPWM where the neutral point voltage was controlled by controlling the polarity of k. The proposed neutral point voltage balancing method was also verified by both simulation and experimental results. The results showed that the proposed neutral point voltage balancing method has good performance at neutral point voltage control and switching losses reduction. Furthermore, the proposed neutral point voltage balancing method is based on logic judgment and table lookup, so it is very convenient to be implemented in applications.

References

[1] S. Kouro, M. Malinowski, K. Gopakumar, *et al*., "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[2] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219-2230, July 2010.

[3] K. Ma and F. Blaabjerg, "Modulation Methods for Three-Level Neutral-Point-Clamped Inverter Achieving Stress Redistribution Under Moderate Modulation Index," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 5-10, Jan. 2016.

[4] M. Schweizer and J. W. Kolar, "High efficiency drive system with 3-level T-type inverter," Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, 2011, pp. 1-10.

[5] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899-907, Feb. 2013.

[6] M. Aly, G. M. Dousoky and M. Shoyama, "Design and validation of SVPWM algorithm for thermal protection of T-type three-level inverters," 2015 IEEE International Telecommunications Energy Conference (INTELEC), Osaka, 2015, pp. 1-6.

[7] T. D. Nguyen, J. Hobraiche, N. Patin, G. Friedrich and J. P. Vilain, "A Direct Digital Technique Implementation of General Discontinuous Pulse Width Modulation Strategy," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4445-4454, Sept. 2011.

[8] L. Asiminoaei, P. Rodriguez and F. Blaabjerg, "Application of Discontinuous PWM Modulation in Active Power Filters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1692-1706, July 2008.

[9] K. Taniguchi, Y. Ogino and H. Irie, "PWM technique for power MOSFET inverter," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 328–334, Jul. 1988.

[10] M. Depenbrock, "Pulse width control of a 3-phase inverter with nonsinusoidal phase voltages," in *Proc. Int. Semicond. Power Converter Conf.*,1977, pp. 399–403.

[11] S. Ogasawara, H. Akagi, and G. Stanke, "A novel PWM scheme of voltage source inverters based on space vector theory," in *Proc. EPE Conf.*, 1989, pp. 1197–1202.

[12] K. Kolar, H. Ertl, and F. C. Zach, "Minimization of the harmonic rms content of the main current of a PWM converter system based on the

solution of an extreme value problem," in *Proc. ICHPC*, Jul. 1990, pp. 234–243.

[13] D. Zhang, F. Wang, R. Burgos and D. Boroyevich, "Common-mode circulating current control of paralleled interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3925–3935, Dec. 2011.

[14] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulse width modulation techniques for three-phase grid connected converters," *IEEE Trans. Power Electron.,* vol. 28, no. 4, pp. 1971–1979, Apr. 2013.

[15] D. G. Holmes and T. A.Lipo, "Pulse width modulation for power converters: principles and practice," John Wiley & Sons, 2003.

[16] T. Bruckner and D. G. Holmes, "Optimal pulse-width modulation for three-level inverters," *IEEE Trans. Power Electron.,* vol. 20, no. 1, pp. 82-89, Jan. 2005.

[17] A. R. Beig, S. Kanukollu and A. Dekka, "Space vector-based three-level discontinuous pulse-width modulation algorithm," *IET Power Electron.,* vol. 6, no. 8, pp. 1475-1482, Sept. 2013.

[18] A. R. Beig, S. Kanukollu, K. Al Hosani and A. Dekka, "Space-Vector-Based Synchronized Three-Level Discontinuous PWM for Medium-Voltage High-Power VSI," *IEEE Trans. Ind. Electron.,* vol. 61, no. 8, pp. 3891-3901, Aug. 2014.

[19] N. Nho-Van, N. Bac-Xuan, and L. Hong-Hee, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," *IEEE Trans. Ind. Electron.,* vol. 58, no. 9, pp. 3958-3966, Sept.2011.

[20] Y. Jiao, F. C. Lee and S. Lu, "Space Vector Modulation for Three-Level NPC Converter With Neutral Point Voltage Balance and Switching Loss Reduction," *IEEE Trans. Power Electron.,* vol. 29, no. 10, pp. 5579-5591, Oct. 2014.

[21] P. C. Loh, G. H. H. Pang and D. G. Holmes, "Multi-level discontinuous pulse width modulation: common mode voltage minimisation analysis", *IEE Proc. Electric Power Appl.,* vol. 151, no. 4, pp. 477–486, Jul. 2004.

[22] U. M. Choi, H. H. Lee and K. B. Lee, "Simple Neutral-Point Voltage Control for Three-Level Inverters Using a Discontinuous Pulse Width Modulation," *IEEE Trans. Energy Convers*., vol. 28, no. 2, pp. 434-443, June 2013.

[23] T. Ghennam, E. M. Berkouk and B. Francois, "A Novel Space-Vector Current Control Based on Circular Hysteresis Areas of a Three-Phase Neutral-Point-Clamped Inverter," *IEEE Trans. Ind. Electron.,* vol. 57, no. 8, pp. 2669-2678, Aug. 2010.

[24] N. Nho-Van, N. Bac-Xuan, and L. Hong-Hee, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3958-3966, Sept.2011.

[25] J. S. Lee and K. B. Lee, "Time-Offset Injection Method for Neutral-Point AC Ripple Voltage Reduction in a Three-Level Inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1931-1941, Mar. 2016.

[26] K. Li, M. Wei, C. Xie, F. Deng, J. M. Guerrero, J. C. Vasquez, "A Generalized Discontinuous PWM based Neutral Point Voltage Balancing Method for Three-Level NPC Voltage Source Inverter with Switching Losses Reduction," accepted by APEC2017.

[27] S. K. Mondal, B. K. Bose, V. Oleschuk and J. O. P. Pinto, "Space vector pulse width modulation of three-level inverter extending operation into overmodulation region," *IEEE Trans. Power Electron.,* vol. 18, no. 2, pp. 604-611, Mar 2003.

[28] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Applicat.,* vol.37, no.2, pp.637-641, Mar/Apr 2001.

[29] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, vol.52, no.2, pp.1114-1128, 2011.

[30] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters, " *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242-249, Mar 2000.

[31] S. Mukherjee, S. K. Giri and S. Banerjee, "A discontinuous PWM scheme for capacitor voltage balancing in three level NPC traction inverter drive," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1756-1761.

[32] J. S. Lee, S. Yoo, and K. B. Lee, "Novel discontinuous PWM method of a three-level inverter for neutral-point voltage ripple reduction," IEEE Trans. Ind. Electron, vol. 63, no. 6, pp. 3344-3354, Jun. 2016.

[33] A. M. Hava, R. J. Kerkman and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Applicat.*, vol. 34, no. 5, pp. 1059-1071, Sep/Oct. 1998.

[34] J. Pou, R. Pindado, D. Boroyevich and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1582-1588, Dec. 2005.

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