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Zarei, Seyed Fariborz ; Ghasemi, Mohammad Amin; Peyghami, Saeed; Davari, Pooya; Mokhtari, Hossein; Blaabjerg, Frede

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Characterization of Proportional-Integral-Resonant Compensator for DC Link Voltage Control

Seyed Fariborz Zarei

*The Center of Excellence in Power
System Management & Control
Department of Electrical Engineering
Sharif University of Technology
Tehran, Iran
zareifariborz@ee.sharif.edu*

Mohammad Amin Ghasemi

*Department of Electrical Engineering
BuAliSina University
Hamadan, Iran
ma.ghasemi@basu.ac.ir*

Saeed Peyghami

*Department of Energy Technology
Aalborg University
Aalborg, Denmark
sap@et.aau.dk*

Pooya Davari

*Department of Energy Technology
Aalborg University
Aalborg, Denmark
pda@et.aau.dk*

Hossein Mokhtari

*The Center of Excellence in Power
System Management & Control
Department of Electrical Engineering
Sharif University of Technology
Tehran, Iran
mokhtari@sharif.edu*

Frede Blaabjerg

*Department of Energy Technology
Aalborg University
Aalborg, Denmark
fbl@et.aau.dk*

Abstract—Voltage unbalance and short circuits in distribution networks adversely affect the performance of grid-tied voltage source inverters (VSIs). Consequently, the dc-link voltage ripple may significantly increase leading to operation of VSI in an unsatisfactory manner. Conventionally in order to maintain the negative sequence current under unbalanced conditions, low-pass/trap filter in the current control loop are required which significantly reduce the controller bandwidth. In order to minimize the dc-link voltage ripple without impairing the controller bandwidth, this paper investigates the design and performance of Proportional–Integral–Resonant (PIR) controller in improving the performance of the VSI under unbalanced condition. The proposed design methodology is validated through simulations and experimental results.

Keywords—DC link voltage control, grid-tied VSI, unbalanced AC grid, unbalanced voltage sag.

I. INTRODUCTION

Voltage source inverters (VSIs) are commonly used AC-DC interfaces for integration of DC renewable energy resources such as photovoltaic systems to the grid. Because of employing fast bidirectional switches, they are fully controllable, and their control methods are matured. However, VSI's operation may adversely affected under unbalanced and asymmetrical fault conditions which requires further investigation [1, 2]. Specifically, low and medium power renewable energy resources are directly connected to the low and medium voltage distribution systems which are intrinsically unbalanced [3]. In this situation, pulsating power drawn from DC link capacitor leads to double-line frequency ripples on DC link voltage, which decrease the VSI performance. There are two main approaches in the literature to control the VSI's DC link voltage under such circumstances which are *i*) the method based on control of negative sequence currents such that the output pulsating powers are forced to zero [4, 5], *ii*) using Proportional–Integral–Resonant (PIR) compensator for DC link controller to produce the necessary

negative sequence currents references in a closed loop system [6, 7]. In methods based on the first remedy, the power control system is kind of an open loop control, and the current and voltage control loops should be separated to avoid any interferences [8]. Then, it necessitates the reduction of the DC link voltage control loop bandwidth (BW) to ensure the stability. Then, inappropriate transient response is expected. Also, the system is sensitive to system parameters mismatch [9]. The second approach overcomes the mentioned problems with the cost of higher controller design complexity.. In this respect, there is a lack of fundamental study on systematic controller design procedure and stability of the system. In other words, it is a complicated task to tune a PIR controller with at least five unknown parameters which requires detailed modeling of the system and stability analysis. In this paper, considering the detailed model of inverter control loops and the delays, a systematic approach is proposed to select the PIR controller coefficients based on stability requirements.

The rest of the paper is organized as follows. Section II describes the conventional control of grid-tied VSIs under unbalanced condition. The proposed method is presented in section III. Sections IV and V present obtained simulation and experimental results, respectively. Finally, the paper is concluded in section VI.

II. CONVENTIONAL CONTROL OF GRID-TIED VOLTAGE SOURCE INVERTERS UNDER UNBALANCED CONDITION

A. Conventional Control of a VSI under Balanced Condition

DC link voltage, reactive power, and output current control loops are cascaded control loops in grid connected VSIs as shown in Fig. 2. This figure shows the power circuit schematic and dynamic control model of a grid-connected VSI. Also, V_{gd} , i_{tdq} are the grid voltages and inverter currents in dq frame. Notably, the DC link voltage and the reactive power are the outer control loops and the third one is the inner

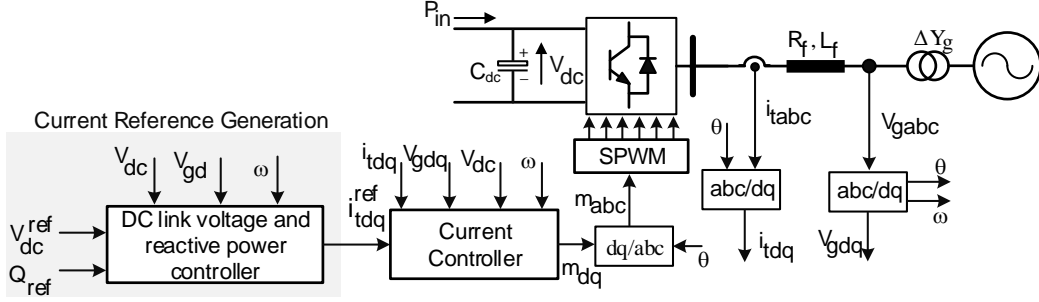


Fig. 2. Power circuit schematic and dynamic control model of a Grid-connected VSI.

control loop. In this scheme, the DC link and reactive power controllers generate current references. It is well known that controlling the DC side capacitor energy instead of its voltage magnitude can further simplify the DC-link controller design [10]. This approach indirectly controls the DC link voltage and simplifies the controller design by eliminating the nonlinearities in the control system [10]. Also, the current controller generates the VSI terminal voltage references to set the output currents at the reference values.

Fig. 1 represents the conventional DC link energy and terminal current control block diagrams. It is a well-known procedure to use (1) as current controller compensator which results in a first order closed loop transfer function, where τ^{-1} is the current control loop BW [11].

$$G_i = \frac{1}{\tau} \cdot \frac{L_f s + R_f}{s} \quad (1)$$

It is worth to note that the BW is limited by VSI's sampling frequency. In this regard, $\tau^{-1} \ll 2\pi \cdot f_{sw}$ can be used, where f_{sw} is the switching frequency [10, 11].

B. Conventional Control of a VSI under Unbalanced Condition

Under unbalanced condition, the waveforms can be demonstrated by positive and negative sequence components as shown in (2), where f is an arbitrary quantity, and f^+ and f^- are positive and negative sequence components amplitude, respectively. In this condition, the inverter apparent power (i.e. S) is given by (3) where $e^{+j\omega t}$ and $e^{-j\omega t}$ represent synchronous rotational dq frames in positive and negative direction [12].

$$f = e^{+j\omega t} \cdot f^+ + e^{-j\omega t} \cdot f^- \quad (2)$$

$$S = (e^{+j\omega t} \cdot V_{gdq}^+ + e^{-j\omega t} \cdot V_{gdq}^-) \times (e^{+j\omega t} \cdot I_{gdq}^+ + e^{-j\omega t} \cdot I_{gdq}^-) \quad (3)$$

By separating real and imaginary part, the active and reactive powers can be achieved as shown in (4). The coefficients can be calculated by (5).

$$\begin{aligned} P_g(t) &= P_0 + P_{c2} \cdot \cos(2\omega t) + P_{s2} \cdot \sin(2\omega t) \\ Q_g(t) &= Q_0 + Q_{c2} \cdot \cos(2\omega t) + Q_{s2} \cdot \sin(2\omega t) \end{aligned} \quad (4)$$

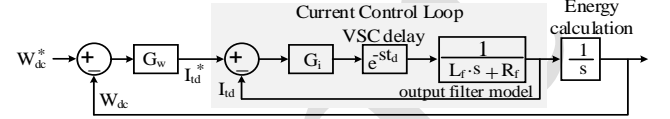


Fig. 1. DC link energy and terminal current control block diagram.

$$\begin{cases} P_0 = 1.5(V_{gd}^+ \cdot I_{td}^+ + V_{gq}^+ \cdot I_{tq}^+ + V_{gd}^- \cdot I_{td}^- + V_{gq}^- \cdot I_{tq}^-) \\ P_{c2} = 1.5(V_{gd}^+ \cdot I_{td}^- + V_{gq}^+ \cdot I_{tq}^- + V_{gd}^- \cdot I_{td}^+ + V_{gq}^- \cdot I_{tq}^+) \\ P_{s2} = 1.5(V_{gq}^- \cdot I_{td}^+ - V_{gd}^- \cdot I_{tq}^+ - V_{gq}^+ \cdot I_{td}^- + V_{gd}^+ \cdot I_{tq}^-) \\ Q_0 = 1.5(V_{gq}^+ \cdot I_{td}^+ - V_{gd}^+ \cdot I_{tq}^+ + V_{gq}^- \cdot I_{td}^- - V_{gd}^- \cdot I_{tq}^-) \\ Q_{c2} = 1.5(V_{gq}^+ \cdot I_{td}^- - V_{gd}^+ \cdot I_{tq}^- + V_{gq}^- \cdot I_{td}^+ - V_{gd}^- \cdot I_{tq}^+) \\ Q_{s2} = 1.5(V_{gd}^+ \cdot I_{td}^- + V_{gq}^+ \cdot I_{tq}^- - V_{gd}^- \cdot I_{td}^+ - V_{gq}^- \cdot I_{tq}^+) \end{cases} \quad (5)$$

As shown in these equations, there are only four independent variables ($I_{td}^+, I_{tq}^+, I_{td}^-, I_{tq}^-$) for six equations [13]. Then, only four equations can be selected to find the independent variables for control of corresponding coefficients. In case of DC link voltage control, the first goal is to control output power P_0 , and then, it is preferred to force P_{c2} and P_{s2} to zero. This can be achieved by solving the first four equations for independent variables as given in (6) [14]. The independent variables are the references for output current. In normal condition, it is preferred to set reactive power to zero in order to achieve maximum power injection to the grid.

$$\begin{bmatrix} +V_{gd}^+ & +V_{gq}^+ & +V_{gd}^- & +V_{gq}^- \\ +V_{gd}^- & +V_{gq}^- & +V_{gd}^+ & +V_{gq}^+ \\ +V_{gq}^- & -V_{gd}^- & -V_{gq}^+ & +V_{gd}^+ \\ +V_{gq}^+ & -V_{gd}^+ & +V_{gq}^- & -V_{gd}^- \end{bmatrix} \cdot \begin{bmatrix} I_{td}^+ \\ I_{tq}^+ \\ I_{td}^- \\ I_{tq}^- \end{bmatrix} = \frac{2}{3} \begin{bmatrix} P_0 \\ 0 \\ 0 \\ Q_0 \end{bmatrix} \quad (6)$$

In the aforementioned output current references, the output filter inductances have been ignored. Therefore, in order to include the effect of output filter inductance, (5) can be rewritten as [4].

$$\begin{cases} P_0 = 1.5 \times (V_{gd}^+ \cdot I_{td}^+ + V_{gd}^- \cdot I_{td}^- + V_{gq}^- \cdot I_{tq}^-) \\ P_{c2} = 1.5 \times (V_{gd}^+ \cdot I_{td}^- + V_{gd}^- \cdot I_{td}^+ + V_{gq}^- \cdot I_{tq}^+) \\ \quad + 3L_f \omega (I_{td}^+ \cdot I_{tq}^- - I_{td}^- \cdot I_{tq}^+) \\ P_{s2} = 1.5 \times (V_{gq}^- \cdot I_{td}^+ - V_{gd}^- \cdot I_{tq}^+ + V_{gd}^+ \cdot I_{tq}^-) \\ \quad - 3L_f \omega (I_{td}^+ \cdot I_{td}^- + I_{tq}^+ \cdot I_{tq}^-) \\ Q_0 = 1.5 \times (V_{gq}^+ \cdot I_{td}^+ + V_{gq}^- \cdot I_{td}^- - V_{gd}^- \cdot I_{tq}^-) \end{cases} \quad (7)$$

Notably, it is assumed that $V_{gq}^+ = 0$.

It can be concluded from (7) that the filter inductance adds nonlinearity to the equations, which makes current references calculation a non-trivial task utilizing linear approximation. Thereby, as addressed in [4], I_{td}^+ and I_{tq}^+ are given by measured values based on P_0 and Q_0 . Then, the equations can be simplified to two linear equations as follows (8).

$$\begin{bmatrix} 1.5V_{gd}^+ - 3L_f\omega I_{tq}^+ & 3L_f\omega I_{td}^+ \\ -3L_f\omega I_{td}^+ & 1.5V_{gd}^+ - 3L_f\omega I_{tq}^+ \end{bmatrix} \begin{bmatrix} I_{td}^- \\ I_{tq}^- \end{bmatrix} = \frac{3}{2} \begin{bmatrix} -V_{gd}^- \cdot I_{td}^+ - V_{gq}^- \cdot I_{tq}^+ \\ -V_{gq}^- \cdot I_{td}^+ + V_{gd}^- \cdot I_{tq}^+ \end{bmatrix} \quad (8)$$

As a result, the negative sequence currents are calculated which results in reducing pulsating powers in the inverter output. To control the sequence currents, the control based on dual double synchronous reference frame is a commonly used method [4]. In this method, the positive and negative sequence currents are controlled independently in two positive and negative synchronous dq frames. Fig. 3 simply shows the d -axis negative sequence current control loop for this method.

As shown in this figure, the band-trap filter in the control loop removes the double line-frequency pulsating components from the measured quantity which gives the negative sequence current amplitude. The closed loop transfer function of this system is as shown in (9). Considering the equation, by selecting even high values for current control loop gain (τ^{-1}), the current control loop bandwidth is limited to about $2\omega_0$ (in this case 628 rad/sec) as shown in Fig. 4 in which the system closed loop bode diagram has plotted for different gains. Furthermore, the current controller gain should be selected even lower to avoid positive gains around $2\omega_0$. Then, the BW of the current and consequently DC link voltage control loops should be much lower than $2\omega_0$. This is the reason that the method based on negative sequence current control has slow transient response. In this paper, PIR compensator has been chosen for DC link voltage control purpose as described in the following section.

$$G_{CL-i} = \frac{s^2 + \omega^2}{\tau \cdot s^3 + (1 + 2\xi\omega\tau) \cdot s^2 + \tau\omega^2 s + \omega^2} \quad (9)$$

III. PROPOSED COMPENSATOR DESIGN APPROACH

In this section, the proposed scheme for PIR controller design is presented to enhance the performance of the grid-tied VSIs under unbalanced and asymmetrical fault conditions.

A. PIR Configuration Selection

From control system theory perspective both i) series connected PI and PR compensators, and ii) parallel connected PI and PR compensators can effectively provide ripple free DC link voltage. On the other hand, from control system design point of view, the controllers parameters should be tuned simultaneously which complicates the tuning procedure. In parallel configuration, the output transient efforts of both compensators have physical interpretation.

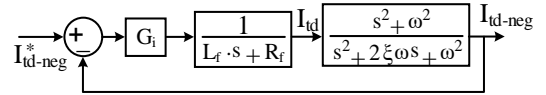


Fig. 3. Negative sequence current control loop.

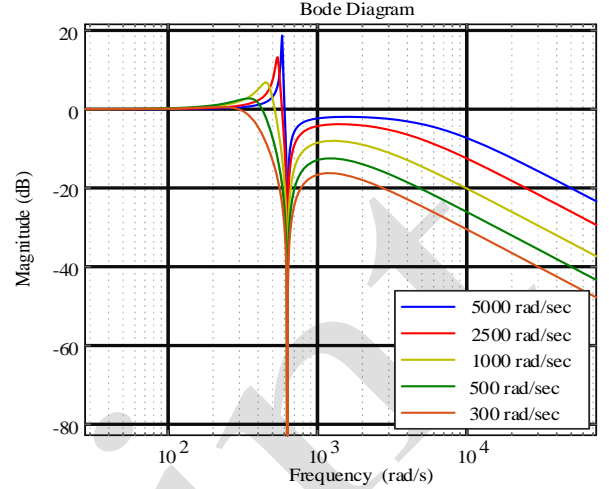


Fig. 4. Bode diagram of current control closed loop transfer function (following (9)) for different current controller gain values.

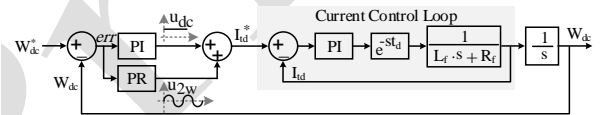


Fig. 5. DC link voltage (energy) control loop with PIR controller and VSI's time delay.

This is due to the fact that the outputs of PI and PR compensators are constant and pulsating quantities in steady state, respectively. Then, each compensator generates its own control effort independently in steady state condition, and this feature can be used to simplify the control system design process. For this reason and considering the proposed control design method in the next section, the parallel connected structure is used in this paper. Fig. 5 shows the parallel PIR system in which u_{dc} and u_{2w} correspond to PI and PR compensators control efforts, respectively. In this system, u_{2w} is a double line-frequency control effort in steady state, which is a translation of the negative sequence output currents in the abc frame. The control effort produced by the PI compensator, u_{dc} , is a constant quantity which is the translation of the positive sequence output currents in the abc frame. Considering these compensators, a zero steady state errors at the frequencies of 0 and $2\omega_0$ are ensured for the DC link voltage control loop, if the control loop is stable. Then, not only the DC link voltage is regulated at its nominal value, but also its double frequency ripples are eliminated.

B. Current Control Loop Modeling

Since the current control loop is the inner loop in the system, it can be modeled by unity gain when its BW is considerably lower than the BW of the outer DC link voltage control loop. Otherwise, it is well-known procedure to use a first order transfer function with time constant of equal to

inverse of the control loop BW. However, detailed modeling of VSI with corresponding delays is a mandatory requirement for stability analysis studies, an issue which is not covered for DC link voltage control in the literature. In this case, the VSI is modeled by corresponding computational and PWM sampling delays, e^{-st_d} as shown in Fig. 5, where $t_d = 1.5/f_{sw}$, and f_{sw} is switching frequency of the VSI. The delay function can be changed to common pole-zero representation form using first order Pade approximation as shown in (10).

$$e^{-st_d} = \frac{1 - 0.5t_d s}{1 + 0.5t_d s} \quad (10)$$

Then, (1) as the current controller, the closed loop transfer function can be derive as:

$$G_{CL-i} = \frac{-0.5t_d s + 1}{0.5\tau t_d s^2 + (\tau - 0.5t_d)s + 1} \quad (11)$$

Considering this equation and using Routh-Hurwitz criterion for second degree polynomials, the current control loop is stable if $\tau > 0.5t_d$. Since the switching frequency is chosen considerably higher than the current control loop BW, this requirement is always met which ensures the current control loop stability. However, the positive zero in the closed loop transfer function of the current control loop affects the stability of the outer control loop. It means that improper selection of DC link voltage controller may lead to system instability when the delay is considered. In the following a detailed discussion is presented.

C. PIR Compensator Design Procedure

Following the illustrated control block diagram in Fig. 5, the PI and PR compensators are in the forward path of the DC link voltage control loop. PI compensator is responsible for control of DC component, and PR compensator controls the pulsating component. The overall characteristics of the control loop depends on both of them, and their mutual interaction must be considered in the controller design. Then, it is necessary to analyze the control loop stability and response in the presence of both controllers. This requirement increases the order of the controller and complicates the controller design and the parameters tuning. In order to simplify the design procedure without losing the generality, an effective design methodology is presented.

Eq. (12) represents the PR compensator form mathematically, in which “ k_{pr} ”, “ ξ ”, “ ω ” are the compensator parameters.

$$C_{pr} = k_{pr} \frac{s^2 + 2\xi\omega s + \omega^2}{s^2 + (2\omega_0)^2} \quad (12)$$

In the first step of design procedure, the PR controller's coefficients are selected assuming that there is no PI compensator in the control loop as shown in Fig. 6. With this assumption, the control loop is simplified to ones in which the PR controller is the only controller of the system. Equation (13) represents the open loop transfer function of the DC link

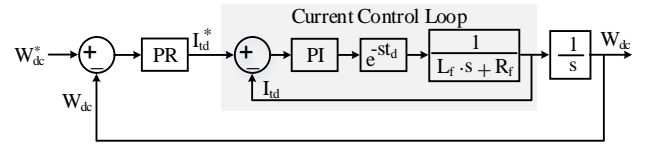


Fig. 6. Simplified DC link voltage (energy) control loop with PR controller.

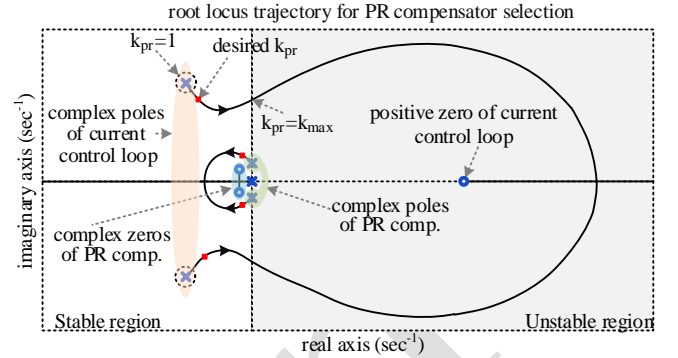


Fig. 7. Root locus trajectory for PR compensator selection.

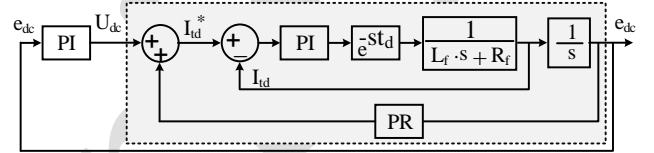


Fig. 8. DC link voltage control loop associated with PI compensator tuning step.

voltage control loop (G_{OP-v}) for this step in which “ k_{pr} ”, “ ξ ”, “ ω ” are unknown parameters.

$$G_{OL-pr} = k_{pr} \cdot \frac{s^2 + 2\xi\omega s + \omega^2}{s^2 + (2\omega_0)^2} \times \frac{-0.5t_d s + 1}{0.5\tau t_d s^2 + (\tau - 0.5t_d)s + 1} \cdot \frac{1}{s} \quad (13)$$

As a proper suggestion, “ ξ ” and “ ω ” can be selected such that the distance of the PR compensator complex zeros from origin to be at least ten times less than that of current control loop poles which ensures the overall stability. Using these values, root locus trajectory is as given in Fig. 7. As shown in this figure, for $k_{pr} < k_{max}$ the system is stable. Also, knowing the required BW for voltage control loop, the desired value for “ k_{pr} ” can be achieved. In this respect, damping ratio of the complex poles and zeros can be used as another supplementary criteria for selection of “ k_{pr} ”. As a suggestion, damping ratio in the range of 0.4-0.6 is an appropriate value.

In the next step, the PI compensator is tuned, considering that the PR compensator is a part of the system as shown in Fig. 5. Using this method, the mutual interaction between the PI and the PR controllers is considered in the final controller design. For this purpose, it is necessary to find the transfer function of e_{dc} to u_{dc} which includes the PR controller as shown in Fig. 8. Then, the PI compensator is designed using PID tuning tool in the MATLAB software to get the highest possible BW and desired phase margin (40-60°).

Considering the above-mentioned controller design procedure, the coefficients of parallel PI and PR compensators

are calculated. In the following, the performance of the PIR compensator has been examined using simulation results.

IV. SIMULATION RESULTS

To show the performance of the DC link voltage controller consisting of PI and PR compensators (PIR) against conventional methods, the test system of Fig. 2 is simulated in MATLAB/SIMULINK environment. In this respect, two conventional methods *i)* filtering the double the nominal frequency components from the measured currents in dq frame and using single conventional dq frame, and *ii)* control of positive and negative sequence currents in dual synchronous reference dq frames have been considered for comparison purposes. In the first method, the control system is similar to the control system of Fig. 1 in which the measured currents are filtered in dq frame to remove the pulsating components. In the second one, there are four current control loops which consist of positive and negative sequence currents control in d and q axes, one of them is shown in Fig. 3.

It should be noted that the conventional PI compensator of (1) is used for current controller in both conventional and PIR compensators. The system parameters are given in Table I. Also, the DC link capacitor energy controllers are as given in (14)-(15) for conventional methods and PIR compensator, respectively. The phase locked loop compensator used for three methods is also given in (16) in which double line-frequency components are removed by employing a mid-reject filter at this frequency.

$$G_{conventional} = 416 \times \frac{s + 50}{s} \times \frac{s + 314}{s + 2600} \quad (14)$$

$$G_{PIR} = 315 \frac{s + 116}{s} + 468 \frac{s^2 + 500s + 68125}{s^2 + 394784} \quad (15)$$

$$G_{PLL} = 46 \cdot \frac{s^2 + 394784.2}{s^2 + 888.4s + 394784.2} \cdot \frac{s + 21.8}{s} \quad (16)$$

In the simulations, one single-line-to-ground (SLG) fault has been applied in the grid side of transformer which causes 20% voltage sag. In inverter side, the voltage unbalance ratio is 10% due to transformer ΔY_g connection as shown in Fig. 9. Under such unbalanced condition, inverter DC side input power is increased 25 kW twice at 0.6 sec and 0.9 sec. Since the grid is unbalanced, injecting the currents causes double frequency oscillations on DC link voltage. Fig. 10 shows the error on DC link capacitor energy for different cases. As it was expected, the method based on filtering the double line-frequency components from measured currents and control of positive sequence current in single dq frame has maximum oscillations among other methods. On the other hand, the control of negative sequence current in DSRF avoids these oscillations. However, this method is a kind of open loop system, and its transient response is worse than positive sequence current control method. Also, PIR compensator by employing higher bandwidth provides the most proper response.

The results given in Fig. 10 shows the performance of PIR compensator in double frequency ripples elimination. Also, it is shown that the low BW of the method based on negative sequence current control in DSRF leads to change in the DC link voltage in transient condition, which requires the use of larger DC link capacitor. In other words, using PIR controller, the DC link capacitor can be reduced if it is needed.

To more discuss on the results, Fig. 11 demonstrates the terminal currents of VSI for three mentioned methods. As shown in this figure, the currents for method *i* is considerably unbalanced since there is no control on negative sequence currents. Fig. 12 shows the corresponding sequence current components for this method. As shown in this figure, the negative sequence currents are not affected by change in the output power command since they are determined based on grid imbalance status. Also, based on current waveforms of Fig. 11, the steady state currents are the same for two other methods, however PIR compensator provides much better transient response.

Finally, to show the performance of PIR compensator for lower DC link capacitor value, Fig. 13 shows the DC link capacitor energy error for a 500 μ F capacitor. The results also verifies the performance of PIR compensator for this lower capacitor value.

V. EXPERIMENTAL VERIFICATION

In this section, experimental results for PIR compensator performance evaluation has been presented. Test system is as shown in Fig. 14 in which a regenerative rectifier in series with a resistor is used as a primary DC source. Also, the grid simulator is programmed to generate unbalanced voltages. The DC voltage of primary source is fixed at 680 V, then, the DC link voltage reference is decreased during the test to control the injected power to the grid. Fig. 15 demonstrates the grid voltages in dq frame. As shown in this figure, the voltages are unbalanced with an unbalance ratio of $V_2/V_1 = 10\%$, same as the condition considered for simulation results section. Fig. 16 shows the measured DC link voltage in which ten 5 V step changes on DC link voltage references are applied to control the current and power flow from DC side to AC side. It is concluded that the PIR compensator tracks the reference changes with proper transient and steady state response. Also, DC and double-frequency components of the measured voltage are extracted and depicted in this figure. As shown in Fig. 16, the amplitude of the double-frequency components are negligible. Considering the pure sinusoidal voltages generated by grid simulator, other variations on DC link voltage comes from primary DC source which works based on PWM switching scheme to control the DC link voltage. Finally, considering the waveforms of Fig. 16, it is concluded that the PIR compensator could effectively control the DC link voltages under grid unbalance condition and different loading conditions.

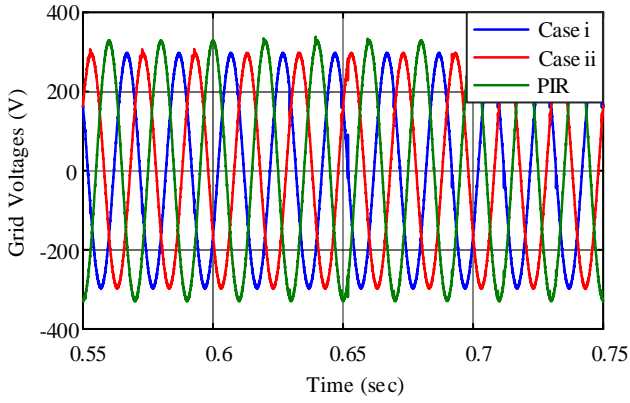


Fig. 9. Unbalanced voltage waveforms in inverter side of transformer due to 20% voltage sag in grid side ($V_2/V_1=10\%$).

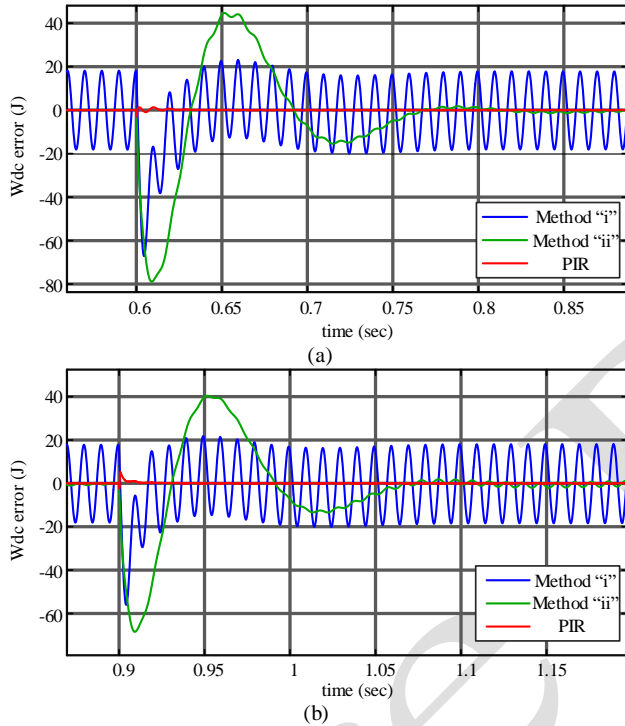


Fig. 10. DC link energy error under unbalanced grid condition with $V_2/V_1=10\%$ and $C_{dc} = 2500 \mu\text{F}$ for method "i" based on single dq frame and currents double frequency filtering, method "ii" based on dual dq frame and positive and negative sequence current control, and PIR compensator (a) first 25 kW step change in inverter active power at $t = 0.6$ sec, (b) second 25 kW step change in the inverter active power at $t = 0.9$ sec.

Table I. parameters of the system

Description	Symbol	Value
Apparent power	S_n	50 kVA
Nominal voltage	V_n	400 V
Switching frequency	f_{sw}	5 kHz
Sampling frequency	$f_{sampling}$	10 kHz
Current control loop BW (PI & PIR)	τ^{-1}	2500 rad/sec
Current control loop BW (DSRF)	τ_{DSRF}^{-1}	300 rad/sec
Output filter resistance	R_f	5 m Ω
Output filter inductance	L_f	3 mH
DC link capacitor capacitance	C_{dc}	2500 μF
DC link voltage	V_{dc}	1 kV
discretization method	-	'tustin'
Transformer Ratio	-	400(D)/400(YG)
Unbalanced grid voltages ($V_2/V_1=10\%$)	V_{ga}	335 \angle 0
	V_{gb}	281 \angle -110
	V_{gc}	320 \angle +130

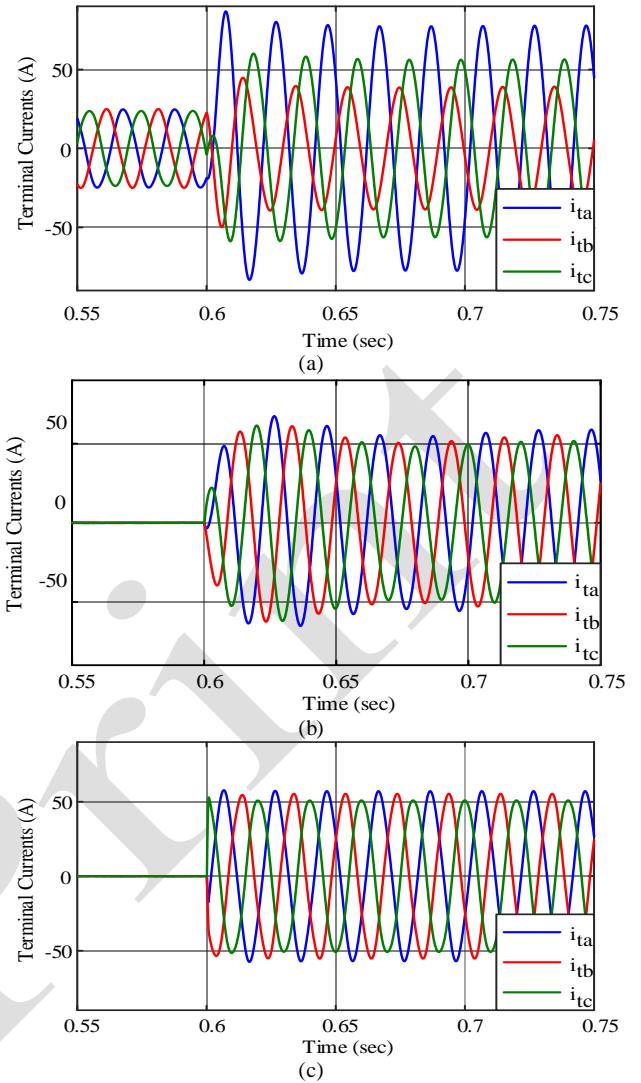


Fig. 11. Inverter terminal currents under unbalanced grid condition with $V_2/V_1=10\%$ and $C_{dc} = 2500 \mu\text{F}$ for 25 kW step change in inverter active power (a) method "i" based on single dq frame and currents double frequency filtering, (b) method "ii" based on dual dq frame and positive and negative sequence current control, and (c) PIR compensator.

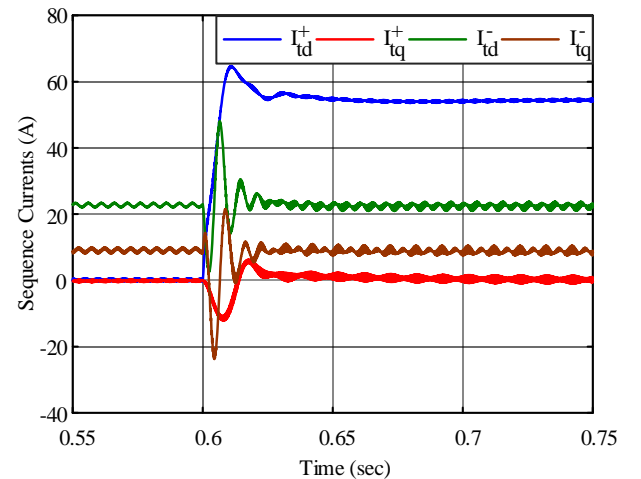


Fig. 12. Inverter terminal currents positive and negative sequence components in "d" and "q" axis under unbalanced grid condition with $V_2/V_1 = 10\%$ and $C_{dc} = 2500 \mu\text{F}$ for 25 kW step change in inverter active power at $t = 0.6$ sec.

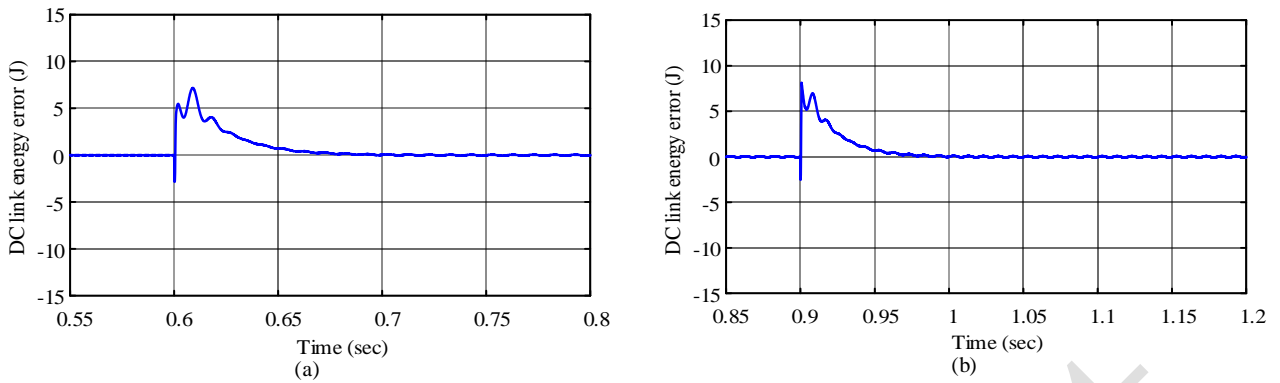


Fig. 13. DC link energy error under unbalanced grid condition with $V_2/V_1 = 10\%$ and $C_{dc} = 500 \mu\text{F}$ for PIR compensator (a) first 25 kW step change in inverter active power at $t = 0.6$ sec, (b) second 25 kW step change in the inverter active power at $t = 0.9$ sec.

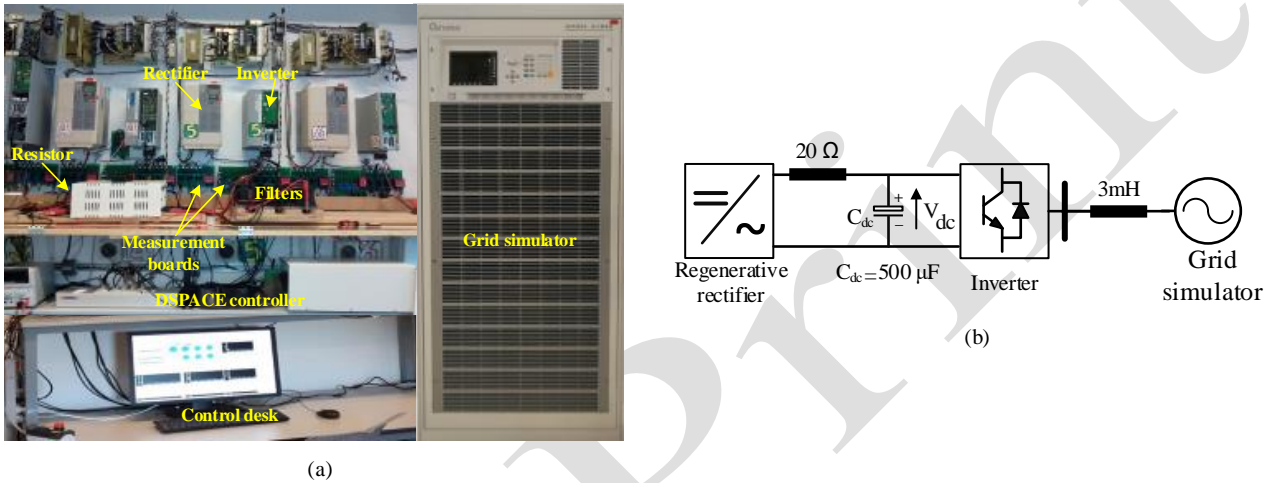


Fig. 14. Experimental test setup consisting of a 10 kW regenerative rectifier as a dc source, a 5.5 kW inverter as VSI, Three-phase grid simulator (a) Hardware, (b) Circuit schematics.

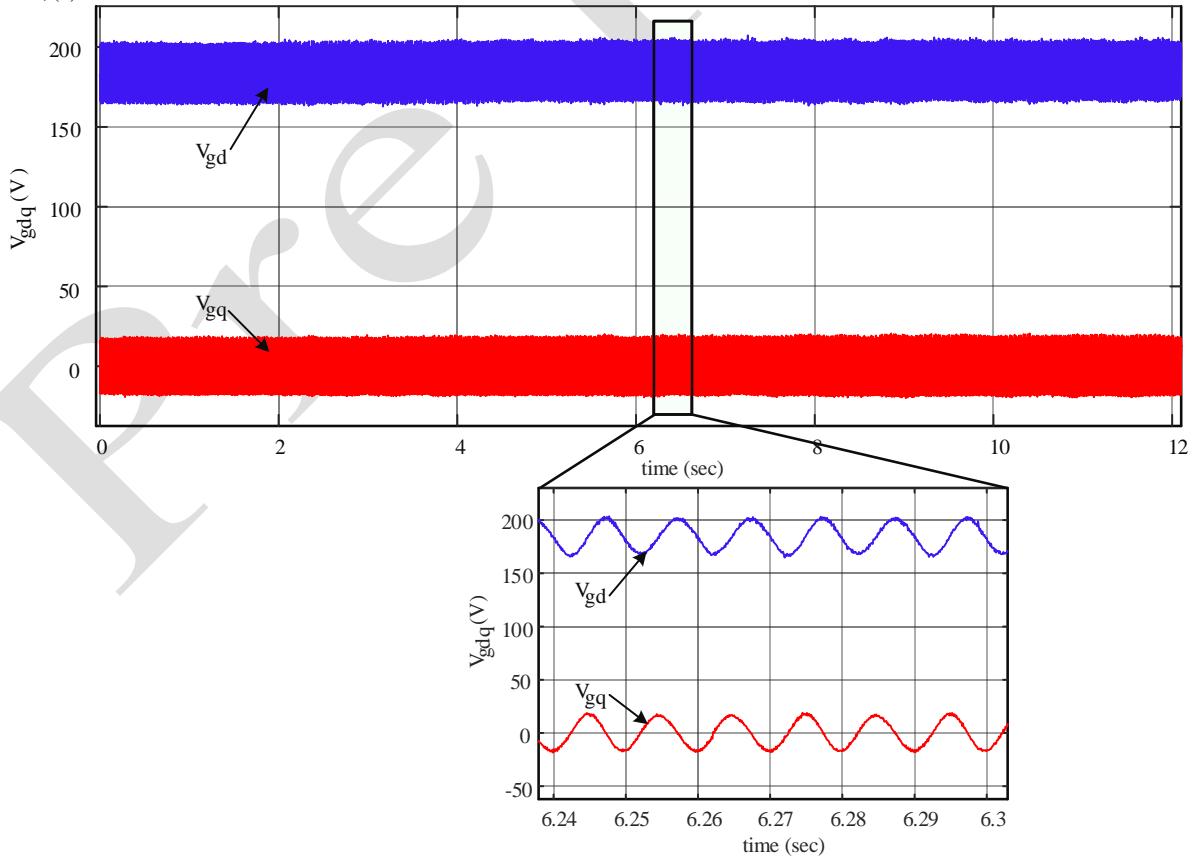


Fig. 15. Measured unbalanced grid voltages in dq frame generated by grid simulator with unbalance ratio of $V_2/V_1 = 10\%$ and with RMS values of $V_a = 126.7 \pm 0$, $V_b = 126.7 \pm 249.4$, $V_c = 144.3 \pm 124.7$.

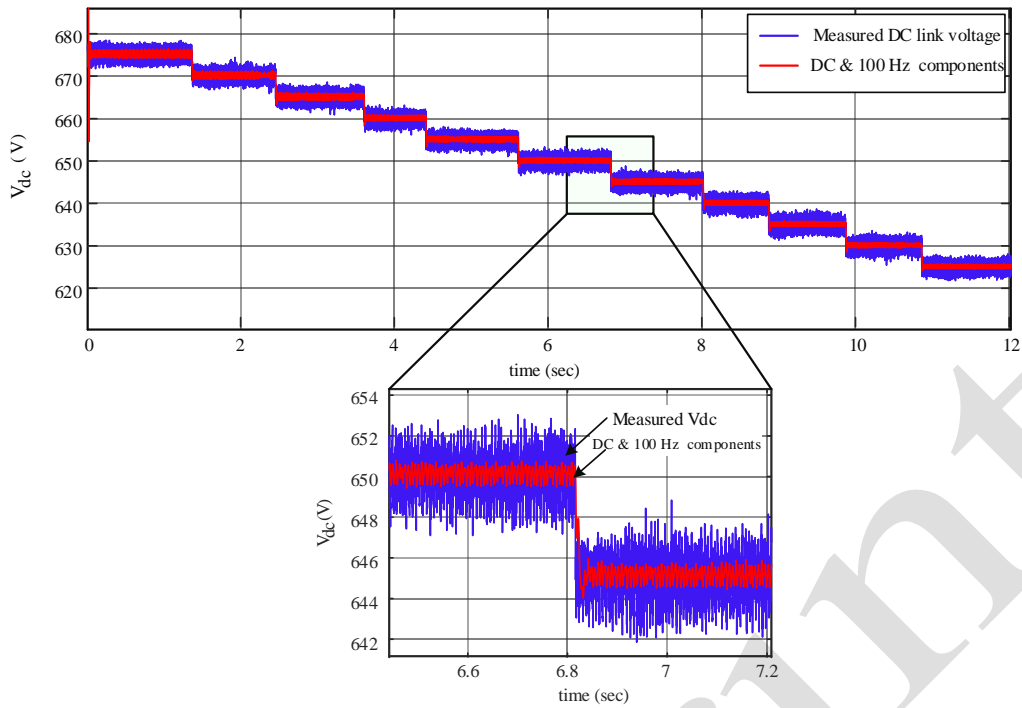


Fig. 16. DC link capacitor voltage under unbalanced grid condition ($V_2/V_1 = 10\%$) with different 5V step changes on DC link voltage reference

VI. CONCLUSION

DC link voltage control of grid-tied VSIs in unbalanced condition is a challenge in which double line-frequency ripples appear on the dc link voltage. Using PIR compensator for DC link voltage control decreases the dc link voltage ripples in a closed loop control system. This paper proposes a systematic design procedure in order to select the PIR compensator parameters according to the stability analysis. In this study, all the control loops are modeled considering the VSI's PWM and computation delays. It is shown that the inverter delay leads to a positive zero in the DC link voltage control loop which may cause instability in case of improper controller parameter selection. Considering this effect, root locus analysis is employed for compensator's parameter selection to avoid approaching to the instability region. Also, different design steps are proposed to find remaining parameters in a systematic way. The designed PIR compensator can properly control the dc link voltage and double-frequency ripples under different unbalanced voltages. Furthermore, the performance of the PIR compensator has been compared to the conventional approaches implying a better dynamic and steady state response. The functionality of the PIR compensator is also validated using discrete time-domain simulations. Moreover, experimental test results provided to show the transient performance of the proposed approach. Future work concerns deeper analysis of the performance of the control approach for different unbalance condition and short circuit faults in a large power electronic based power system.

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