An Enhanced Control Scheme for Uninterruptible Power Supply

Lu, Jinghang; Savaghebi, Mehdi; Wei, Baoze; Guerrero, Josep M.

Published in:
Proceedings of 2017 IEEE Energy Conversion Congress and Exposition (ECCE)

DOI (link to publication from Publisher):
10.1109/ECCE.2017.8096408

Publication date:
2017

Document Version
Accepted author manuscript, peer reviewed version

An Enhanced Control Scheme for Uninterruptible Power Supply

Jinghang Lu, Mehdi Savaghebi, Baoze Wei and Josep Guerrero
Department of Energy Technology
Aalborg University
Aalborg, Denmark
{jgl,mes,bao,joz}@et.aau.dk

***Abstract*—To address the active power feeding issue in the parallel Uninterruptible Power Supply (UPS) system, a DC-link Voltage Protection (DCVP) control strategy is proposed in this paper. The proposed control method only relies on local load information, which increases the system reliability and robustness. Moreover, virtual resistance based regulation strategies are proposed for solving the active power sharing imbalance caused by the active power feeding and harmonic power sharing imbalanced caused by the line resistance mismatching. In addition, an anti-windup based consensus distributed controller is proposed to solve the overshoot issue during the transient time in voltage and frequency restoration. With the proposed anti-windup controller, large overshoot issue is alleviated. Finally, the feasibility of the proposed methods is verified by experimental results from the parallel UPS prototypes.**

Keywords—Anti-windup; DC-link Voltage Protection; Uninterruptible Power Supply (UPS); Power sharing; Virtual resistance;

I. INTRODUCTION

Last few years have witnessed the widespread application of Uninterruptible Power Supply (UPS) system in the network center, financial institution and hospital [1]. Meanwhile, the strong need for UPS system to provide more reliable, efficient and secure electrical power supply for the modern digital equipment[2] propels the growing attention of UPS technology by the engineers and academic researchers.

According to the European Standard EN 62040-3 [2], the UPS system is divided into on-line, off-line and line-interactive UPS in compliance with the power delivery to the critical load predominantly coming from the grid or inverters in the normal mode of operation. On-line UPS system is mostly popular and widely configured for sensitive load, as it provides excellent characteristic in being immune to grid frequency variation, voltage irregularity, and other power issues [3]. The on-line UPS system is usually comprised of AC/DC (rectifier), DC/AC (inverter), battery and a static bypass switch[4]. To realize more reliable power to the load, parallel UPS modules are connected to deliver the power to the load. Based on the IEC 62040-3:2011[4], parallel UPS system is classified into Single DC Bus (SDB) UPS and Dual DC Bus (DDB) UPS system, as is shown in Fig.1, where it is observed that SDB UPS system connects all the inverters with only one DC bus, whereas DDB UPS system divides all the inverters into two groups, which presents higher reliability and redundancy compared with SDB UPS system, such as the DC voltage fault on one bus does not affect the other DC bus.

For the normal operation of DDB UPS system, master-slave control [5], average load sharing control [6], droop control [7] and circular chain control has been proposed to regulate power delivery. Among these control strategies, droop control strategy has been mostly adopted. As the droop control is able to regulate the voltage amplitude and frequency without intercommunication between UPS modules, which increased system stability and reliability. However, the droop control is a load dependent strategy that can not recover the frequency and voltage deviation caused by the load. Consequently, secondary control strategy such as consensus [8] based distributed controller has been employed to compensate the frequency and voltage amplitude deviation. However, the consensus control strategy may generate large overshoot for the frequency and voltage amplitude during compensation process, which may be harmful to the sensitive load. But this issue has not been reported in previous literature.

Moreover, in DDB parallel UPS system, under light load, fault or temporarily overshoot situation that occurs in one of the inverter's output voltage, the voltage difference between the UPS modules will inevitably lead to power feeding from higher output voltage to lower output voltage. As a result, the feeding power results in an excessively high voltage of the DC link to trip the UPS system [9]. In addition, the active power feeding issue exists as well when the UPS system shifts its operation from the normal mode to Eco-mode [10]. During the transition, the active power feeding may occur if the grid voltage suffers from temporary overvoltage. Finally, considering the active power imbalance caused by the active power feeding and harmonic power imbalance caused by the line resistance mismatching, these active power and harmonic power sharing errors lead to the circulating fundamental and harmonic current, which is harmful to the stable operation of UPS system. The abovementioned issues need to be investigated and discussed.

In this paper, first, a DCVP method is proposed for the DDB UPS system to solve the active power feeding issue caused by output voltage difference and overvoltage during the mode transition of UPS system. Based on the proposed method, the active power back-feeding issue is significantly mitigated and does not cause the damage of DC link capacitor. Moreover, the

virtual resistance based control strategy for mitigating the active power and harmonic power imbalance is proposed as well. Finally, an anti-windup dynamic consensus algorithm (ADCA) is applied for voltage amplitude and frequency restoration, which alleviate the large overshoot issue. The feasibility and effectiveness of the proposed methods are validated by a dSPACE 1106 based experimental prototype.

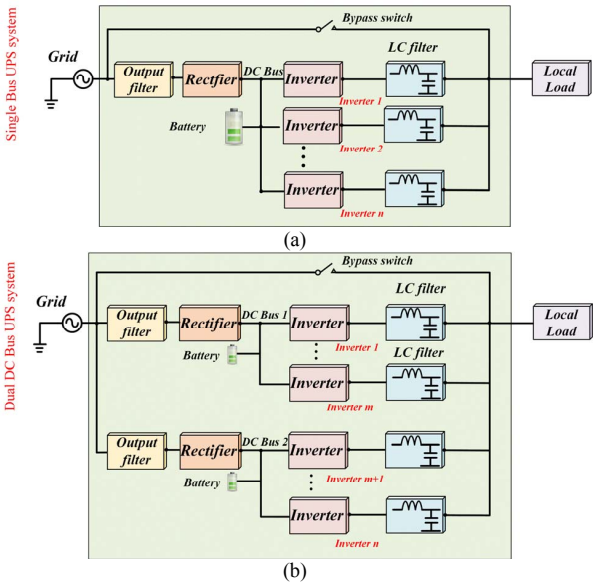


Fig. 1. Categories of parallel UPS system

II. Power Flow Analysis for UPS System

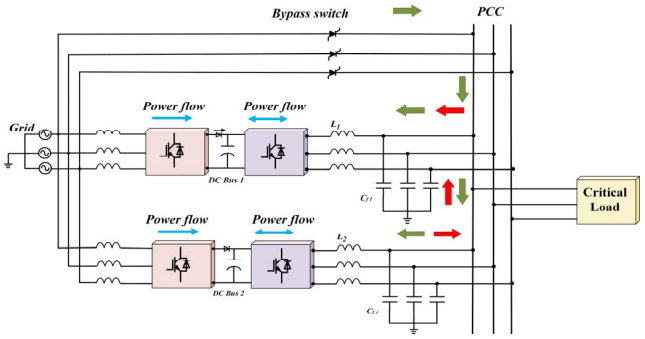


Fig.2. Power flow in UPS system

In this paper, the DDB parallel UPS system (Fig.1(b)), which is composed of two AC/DC (rectifiers), two DC/AC groups (inverters), two energy storage systems and a bypass switch, is adopted in this paper. The rectifier is responsible for the power delivery from AC input to the DC link and charging the battery. Normally, the SCR rectifier or PWM rectifier with a diode in the DC link is widely used in high power or low power UPS system to prevent the power back-feeding from the DC link to the grid. The inverter works in Voltage Control Mode (VCM) to directly regulate the output filter's capacitor voltage and inner loop inverter side inductor's current. The bypass switch will be closed in case of overloading or when the UPS is intended to work in Eco-mode. In addition, the LC type filters are adopted to avoid the resonance brought by LCL type filter. Some critical information such as each UPS's active power is intercommunicated among the UPS modules.

To simplify the configuration of Fig.1(b), the configuration of two inverters is adopted as shown in Fig.2. Based on IEC 62020-3:2011 standard [7], for the on-line, off-line and line-interactive UPS system, the battery is fully charged and works in standby mode in normal operation. The PWM converter with DC-link clamped diode is adopted as the rectifier to deliver the power in a unidirectional direction (Fig.2 blue arrow) from the grid to the DC link. In the meantime, the inverter is able to operate in bi-direction (Fig.2 blue arrows). As is shown in Fig.2, under light load and due to the tolerance between the output voltage of parallel inverters or because of the one inverter's output voltage fault, the UPS module with higher output voltage can feed effective active power into the other UPS module (red arrow in Fig.2). Consequently, the increase of the DC-link voltage (in this case V_{DC1}) may exceed the upper voltage limitation of the DC-link capacitor, and eventually damage the DC-link capacitor without the DCVP. In addition, when UPS's operation shifts to Eco-mode, the bypass switch needs to be closed, In this case, the grid voltage amplitude may be higher than the voltage at PCC if grid suffers from temporarily overvoltage. In this scenario, grid power may feed into both UPS modules (Fig.2 green arrow), which may lead to excessively high DC link voltage of both UPS modules and consequently interruption of inverter's operation. Therefore, it is imperative to explore a DC-link voltage protection control algorithm.

III. Proposed Method for DC-Link Protection and Current Sharing

A. Proposed method for DCVP

The principle of the DCVP is based on equipping a local DCVP controller in each inverter, each inverter detects its own local output active power P_{LPF}(Fig.3), if the detected active power P_{LPF} falls below zero, which indicates this UPS module is absorbing active power($P_{LPF} < 0$) ,at this time, the falling edge of active power signal(P_{LPF}) will be employed to activate the DCVP controller. By comparison of zero (reference active power is set to be zero) and the negative active power P_{LPF}, the error goes through a proportional controller K_p to generate an additional voltage amplitude referenceΔE_{comp}. This additional voltage amplitude reference ΔE_{comp} will be added to the original voltage amplitude reference E_1 from *P-E* droop controller to elevate the voltage reference in order to generate more active power. As a result, the additional active power counteracts the injected active power and prevent the DC link voltage from further increasing. Finally, the DC link voltage is stabilized and operated in a new steady state point.

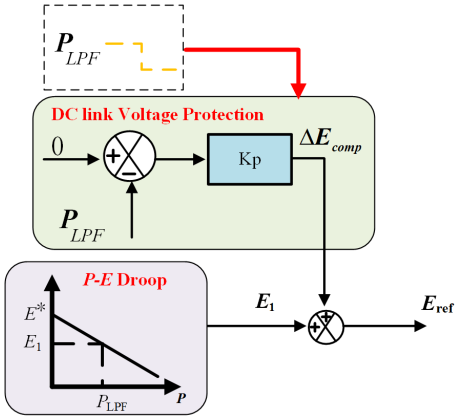


Fig.3. DC link voltage protection in UPS system

The control strategy is expressed as:

$$\Delta E_{comp} = (0 - P_{LPF}) \cdot K_p \quad (1)$$

To have a better understanding of the proposed method principle, first, it is assumed that output voltage of UPS 2 module drifts up (Fig.2), the excessive active power is injected into UPS1, leading to the active power direction reverse in UPS 1 (Fig.2 red arrow). Due to the injected active power, the DC link voltage of UPS1 begins to increase. At the same time, the UPS local DCVP controller keeps on monitoring its own output active power, once it detects the active power falling below zero, DCVP controller is activated, the difference between 0 and the negative active power is employed to generate the additional reference voltage amplitude for UPS 1 to increase the output voltage amplitude of UPS 1 and generate more active power to counteract the injected active power. Therefore, by increasing the output voltage amplitude of UPS 1, the DC-link voltage of UPS 1 is stabilized. With the same DCVP controller, the proposed controller can be applied to prevent the active power feeding in during the transition from normal mode to Eco-mode, where bypass switch needs to be closed in order to feed the active power to the load directly from the grid. Normally, before the closing of the bypass switch, the voltage amplitude and frequency between the PCC voltage and grid voltage should be synchronized. However, if grid voltage suffers from temporary overvoltage during transition process, the extra active power provided by the grid injects into the UPS modules, leading to overvoltage of DC bus 1 and DC bus2 and possibly damage the DC-link capacitor. However, with equipping the DCVP method, it can effectively prevent the power feeding from the grid.

B. Proposed method for active power and harmonic power sharing

In parallel UPS system, the active power sharing imbalance may be provoked by line resistance mismatching or the active power feeding. Therefore, the active power strategy among the UPS modules should be carried out to mitigate the active power sharing imbalance. First, the principle of active power and harmonic power sharing should be investigated. For the UPS system with *LC* filter, line impedance is quite small and mainly resistive, the virtual resistance that is embedded in the control strategy dominates the total resistance and make sure the system is stably operated [4]. Therefore, the reactive power-frequency and active power-voltage magnitude droop control are adopted in the LC filter type UPS system and expressed as:

$$\omega = \omega^* + D_Q Q_{LPF} \quad (2)$$

$$E = E^* - D_p P_{LPF} \quad (3)$$

where ω^* and ω are the UPS nominal and reference angular frequency, E^* and E are the UPS nominal and reference voltage amplitude. P_{LPF} and Q_{LPF} are the output active and reactive power through a low pass filter with cut-off frequency ω_c. D_p and D_Q are the droop coefficients for regulating the UPS active power and reactive power, respectively. Fig.4 (a) shows the parallel UPS modules are modeled as the controlled voltage source (V_{ref}) with virtual resistance $R_{v,f}$ at fundamental frequency. $R_{line,f}$ indicates the line resistance at the fundamental frequency. It is noted that the $R_{Line,f}$ can not be omitted even it is a small value. PCC linear load is modeled as passive *RL* load.

Normally, for the power flow through the feeder that consists of inductance and resistance, the voltage drop on the impedance leads to the following expression [13]:

$$\Delta V = \frac{X \cdot Q + R \cdot P}{E^*} \quad (4)$$

where *P* and *Q* are the active and reactive power, *R* and *X* are the corresponding resistive and inductive component of the line impedance. E^* is the nominal voltage magnitude, ΔV is the voltage magnitude drop on the impedance.

In the UPS system, by neglecting the line inductance, the voltage drop on the resistance is expressed as:

$$\Delta V = \frac{R \cdot P}{E^*} \quad (5)$$

Therefore, the relationship between the UPS output voltage and PCC voltage is expressed as:

$$V_{ref1} = V_{pcc} + \frac{R_{e1} \cdot P_1}{E^*} \quad (6)$$

$$V_{ref2} = V_{pcc} + \frac{R_{e2} \cdot P_2}{E^*} \quad (7)$$

Where R_{e1} and R_{e2} are the total resistance that include line resistance and virtual resistance and expressed as: $R_{e1} = R_{v,f1} + R_{Line,f1}$, $R_{e2} = R_{v,f2} + R_{Line,f2}$.

It is noted that the reactive power sharing with the droop control strategy should be always accurate in steady state in UPS system as the frequency is a global parameter for all UPS modules. Hence, by combining (6) and (7), it is seen that the active power sharing error is expressed as:

$$P_2 - P_1 = \frac{(V_{ref2} - V_{pcc})E^*}{R_{e2}} - \frac{(V_{ref1} - V_{pcc})E^*}{R_{e1}} \quad (8)$$

It can be observed from (8) that the active power sharing error is related with two factors that include the total resistance difference (R_{e1} *and* R_{e2}) of the two UPS system and the voltage magnitude difference (V_{ref1} *and* V_{ref2}). If the active power sharing error is caused by the output voltage difference between output voltages (V_{ref1} *and* V_{ref2}) or line resistance mismatching (R_{Line1} *and* R_{Line2}), the best way to mitigate the active power sharing error is to adjust each UPS's virtual resistance (R_{v1} *and* R_{v2}).

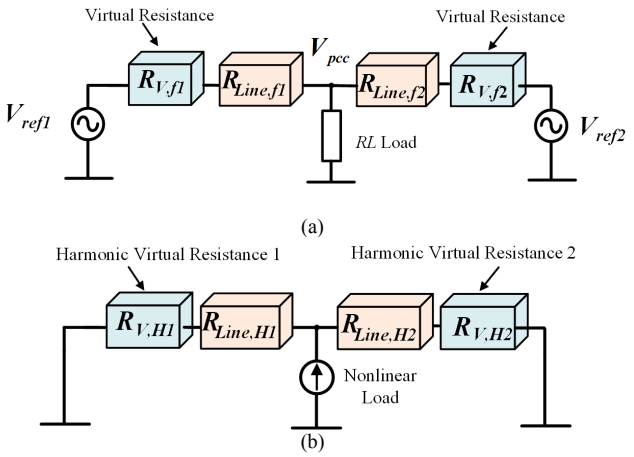


Fig.4. Equivalent circuit for UPS (a) at fundamental frequency and (b) at harmonic frequency

Meanwhile, the equivalent circuit at the harmonic frequencies when connecting a nonlinear load to PCC is shown in Fig.4(b). The harmonic resistance is expressed as:

$$R_H = R_{Line,H} + R_{v,H} \tag{9}$$

where $R_{line,H}$ and $R_{v,H}$ are the physical feeder at the harmonic frequencies and virtual resistance at the harmonic frequencies respectively. It is noted that at harmonic frequencies, voltage source is considered as short circuit, as the controlled harmonic voltage source is considered as zero in the system. It can be seen from Fig.4(b) that the decrease of the any equivalent UPS harmonic resistance leads to the increase of the corresponding harmonic current and vice versa. Therefore, by proper control of the virtual harmonic resistance, the circulating harmonic current can be mitigated due to line resistance mismatching

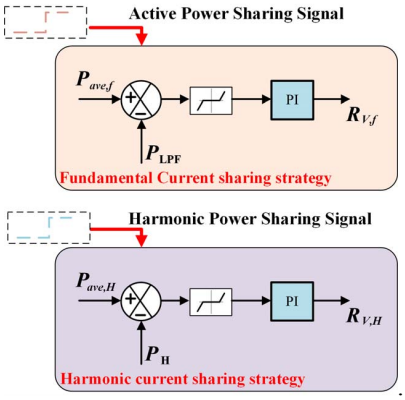


Fig.5 Fundamental and harmonic current sharing strategy

The proposed method for active power sharing and harmonic power sharing are shown in Fig.5. First, it is assumed that the distance from each UPS module to the critical load is different, which results in mismatching of feeder's resistance. Moreover, the DC link voltage protection controller has been activated due to the active power feeding. At this moment, the active power sharing errors (due to line resistance mismatching and power feeding) and harmonic power sharing errors (due to line resistance mismatching) both exist in the parallel UPS system. When the active power sharing signal activates the controller by changing the flag from 0 to 1, the active power of each UPS module will compare with the average active power reference, the error of comparison goes through a PI controller to generate additional adaptive fundamental virtual resistance until the output active power for all UPS modules become equalized. The controller is expressed as:

$$R_{V,af} = (P_{ave,f} - P_{LPF\_i}) \cdot (K_{p,f} + \frac{K_{i,f}}{s}) \tag{10}$$

where $P_{ave,f} = \frac{1}{N}\sum_{i=1}^{n} P_{LPF\_i}$, $P_{ave,f}$ is the active power reference for all UPS modules, and P_{LPF_i} indicates the active power of the i th UPS module. For each UPS module, the active power is expressed as:

$$P_{LPF} = \frac{3\omega_c}{2(s+\omega_c)}(V_{c\alpha} \cdot I_{\alpha,f} + V_{c\beta} \cdot I_{\beta,f}) \tag{11}$$

$V_{c\alpha}$ and $V_{c\beta}$ are the measured sinusoidal UPS voltage in stationary frame, $I_{\alpha,f}$ and $I_{\beta,f}$ are the UPS fundamental positive sequence current. The ripples of active and reactive power are attenuated by the low-pass filter with cut-off frequency ω_c.

Similarly, if the harmonic power sharing signal is flipped from zero to one, the harmonic power error will be employed to regulate the harmonic virtual resistance $R_{V,H}$ at the selected harmonic frequencies as:

$$R_{V,H} = (P_{ave,H} - P_{H\_i}) \cdot (K_{p,H} + \frac{K_{i,H}}{s}) \tag{12}$$

where $P_{ave,H} = \frac{1}{N}\sum_{i=1}^{n} P_{H\_i}$, $P_{ave,H}$ is the harmonic power reference for all UPS modules, P_{H_i} indicates the harmonic power of i^{th} UPS module. For each UPS module, the harmonic power is expressed as:

$$P_H = \frac{3}{2}E^* \left(\sqrt{(I^-_{\alpha,5})^2 + (I^-_{\beta,5})^2 + (I^+_{\alpha,7})^2 + (I^+_{\beta,7})^2} \right) \tag{13}$$

where E^* is the rated UPS phase voltage. $I^-_{\alpha,5}$ and $I^-_{\beta,5}$ are the negative sequence component of UPS fifth harmonic current. $I^+_{\alpha,7}$ and $I^+_{\beta,7}$ are the positive sequence component of UPS seventh harmonic current. It should be noted that in the harmonic power calculation, only low order harmonic currents are employed to calculate the harmonic power as 5^{th} and 7^{th} harmonic current are the main components of harmonic orders. Finally, fundamental and harmonic current of UPS can be separated by the SOGI based sequence decomposition method [19].

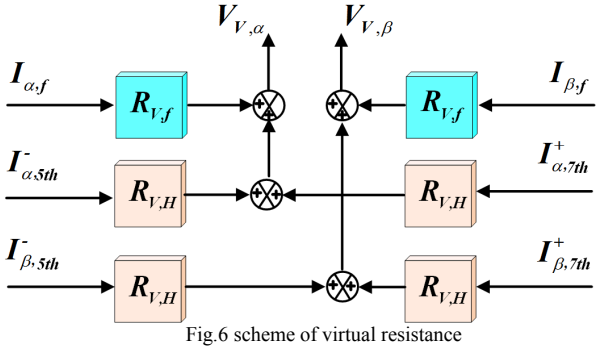


Fig.6 scheme of virtual resistance

In addition, once the virtual resistance is determined, the voltage drop on its corresponding virtual resistance can be calculated in stationary frame. The voltage drop calculation is

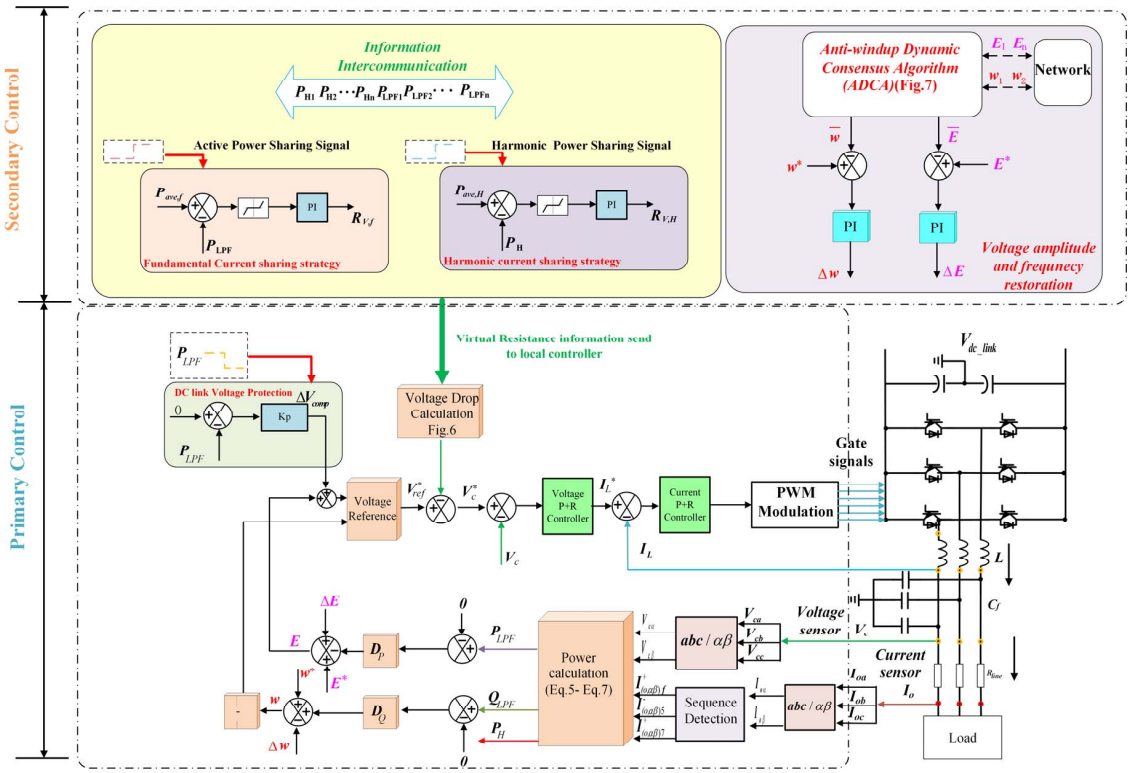


Fig.8 Complete diagram of the UPS module with the proposed control method

shown in Fig.6, where $R_{V,f}$, $R_{V,H}$ are the fundamental and harmonic virtual resistance, respectively. Anti-windup Dynamic Consensus Algorithm.

The dynamic consensus algorithm (DCA), which has been successfully employed for secondary distributed control [20] in microgrid to achieve effective information sharing among Distributed Generation system(DGs), can be applied to UPS system as well.

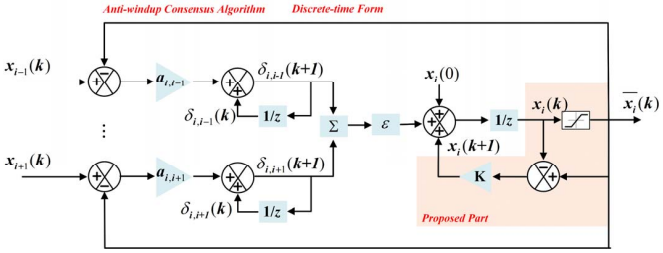


Fig.7 Control structure for ADCA

However, it needs to be pointed out that the voltage amplitude and frequency restoration process may suffer from large overshoot when the DCA is implemented in the secondary control. This issue is caused by the difference between fast dynamic response of DCA and slow dynamic response of PI controllers in secondary control strategy. Therefore, in this section, an anti-windup dynamic consensus algorithm (ADCA) is proposed to reduce the fast dynamic response of DCA, in this way the overshoot issue can be alleviated. The details of ADCA is shown in Fig.7,

First, consider that the discrete form of consensus algorithm is presented as:

$$x_i(k+1) = x_i(k) + \varepsilon \cdot \sum_{j \in N} a_{ij}(x_j(k) - x_i(k)) \quad (14)$$

where $x_i(k)$ is indicated the information status of agent i at iteration k, a_{ij} is the connection status between node i and node j, ε is the consensus edge weight used for tuning the dynamic of DCA.

In order to ensure the convergence of consensus to accurate value in dynamic system, a modified algorithm is applied in the paper and expressed as [21]:

$$x_i(k+1) = x_i(0) + \varepsilon \cdot \sum_{j \in N} \delta_{ij}(k+1) \quad (15)$$

$$\delta_{ij}(k+1) = \delta_{ij}(k) + a_{ij} \cdot (x_j(k) - x_i(k)) \quad (16)$$

where $\delta_{ij}(k)$ stores the cumulative difference between the two agents.

In this paper, $x_i(k)$ may indicate the frequency and voltage amplitude. As it is seen in Fig.7, the saturation block is inserted between $x_i(k)$ and $\bar{x}_i(k)$ to prevent the frequency or voltage amplitude from exceeding the permitted value and reducing the overshoot. However, only adding the satuation block in the consensus algorithm will lead to the long time windup. In order to prevent windup and slow down the dynamic response , the back calculation method [22] is adopted to calcualte the $x_i(k+1)$. Therefore, the updated $x_i(k+1)$ is expressed as:

$$x_i(k+1) = x_i(0) + \varepsilon \cdot \sum_{j \in N} \delta_{ij}(k+1) + K \cdot (\bar{x}_i(k) - x_i(k)) \quad (17)$$

From Eq.(17), it is seen that in steady state $x_i(k)$ does not exceeds the saturation value, $\bar{x}_i(k) = x_i(k)$, therefore, Eq.(17) equals with Eq.(15). However, in dynamic restoration process, $x_i(k)$ exceeds the saturation block value, the anti-windup part will force the $x_i(k)$ to be lower than upper limitation value of saturation block to alleviate the frequency and voltage amplitude overshoot.

The complete diagram of each UPS module is shown in Fig.8, which includes primary and secondary control strategy. In primary control layer, Droop control strategy, DC-link voltage protection control strategy, voltage loop and current loop are adopted. In the secondary control level, the active power sharing and harmonic power sharing strategy and ADCA strategy to restore the frequency and amplitude is implemented. It should be pointed out that in order to achieve voltage tracking, a double loop voltage control strategy with harmonic voltage compensators are adopted in the paper. The outer loop is voltage controller to regulate the output capacitor's voltage and inner loop is a current controller to regulate the inverter side current. The controllers are expressed as:

$$G_v(s) = k_{pv} + \frac{k_{rv}s}{s^2+(\omega_o)^2} + \sum_{h=5,7} \frac{k_{vh}s}{s^2+(h\omega_o)^2} \quad (18)$$

$$G_v(s) = k_{pi} + \frac{k_{ri}s}{s^2+(\omega_o)^2} \quad (19)$$

where k_{pv} and k_{pi} are the proportional terms, k_{rv} and k_{ri} are the resonant term coefficient at $\omega_o = 50Hz$. k_{vh} is the resonant coefficient term for the harmonics h (5^{th}, 7^{th}). The inner current loop is designed to provide sufficient damping and protect the inductor's current from overcurrent. Finally, it should be pointed that the DCVP control strategy is to prevent the power back-feeding which may damage the DC link capacitor and trip the system. Distributed current sharing strategy can be applied after activation of DCVP to share the currents among the UPS modules. It can be applied in current sharing due to the line resistance mismatching as well. ADCA is implemented for secondary control strategy in normal mode of operation in UPS system.

IV. Experimental Results

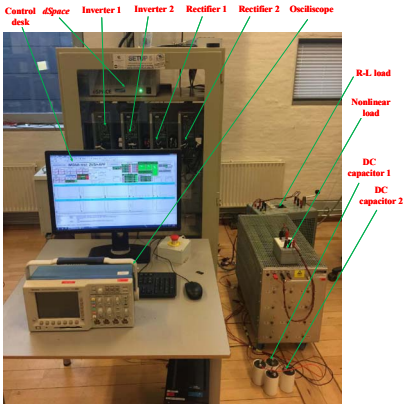


Fig.9 Experimental setup.

In order to validate the feasibility of the proposed control strategies, a two parallel DDB UPS system shown in Fig.2 is built up as shown in Fig. 9, which consists of two AC/DC rectifiers and two DC/AC inverters. Two DC buses are formed by DC link capacitors. The control algorithm is tested in dSPACE 1006 platform for real-time control. The system parameters are listed in Table I. Waveforms are captured by both oscilloscope and Control Desk.

TABLE I. System Parameters

System Parameter	
Filter Inductor L_f	$1.8mH$
ESR of Inductor	0.02ohm
Filter Capacitor C_f	$27uF$
DC link Capacitor	$2200uF$
Sampling frequency	10kHz
Rated Line to Line RMS voltage	120V
R-L load	$50\Omega - 1.8mH$
Nonlinear load (R-L-C type)	C=20uf, L=1.8 mH, R=20Ω
DC link Voltage Protection	
Proportional gain K_p	0.2
Active Power Sharing Control strategy	
Proportional gain K_{p_f}	$2e-4$
Integral gain K_{i_f}	$1e-4$
Harmonic Power Sharing Control strategy	
Proportional gain K_{p_H}	$2e-4$
Integral gain K_{i_H}	$1e-4$
Droop Coefficient	
Frequency droop D_q	0.0001
Voltage droop D_p	0.00005
Voltage Control Parameter	
Proportional gainK_{pv}	0.2
Resonant gain K_{iv}	100
Current controller Parameter	
Proportional K_{p_i}	5.6
Resonant gain K_{i_i}	500
ADCA Parameter	
Parameter K in ADCA	0.2

A. Parallel UPS Transient Response in start-up process

First, the power sharing capability between the two UPS modules is evaluated in the UPS start-up process (Fig.10(a)), where it is shown that the active and reactive power are equally shared during the transient process. The output current for the two UPS modules and their errors are shown in Fig.10 (b), where it is seen that the circulating current is almost zero due to the accurate active and reactive power sharing. It is noted that the background noise is caused by the connection of D/A board with scope.

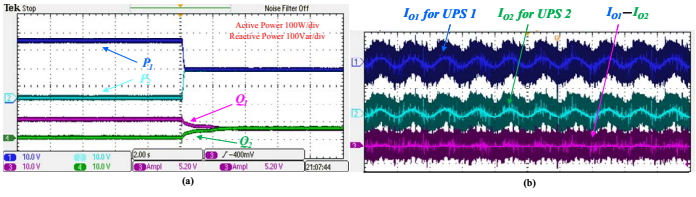


Fig.10 UPS parallel Power sharing performance, (a) process of active and reactive power sharing, (b) current of UPS1 and UPS2 after power sharing

B. Active Power feeding without DC link voltage protection

The active power feeding test is presented with additional 3% drifts up from 100V output voltage at 2.5s, during the period

between 2.5s and 2.9s, it is observed from Fig.11 that the DC link voltage V_{DC1} keeps increasing from 550V to 600V (the DC link voltage upper limit), which eventually triggered the protection for the PWM driving circuit, leading to the stop operation of inverter 1(after 2.9s).

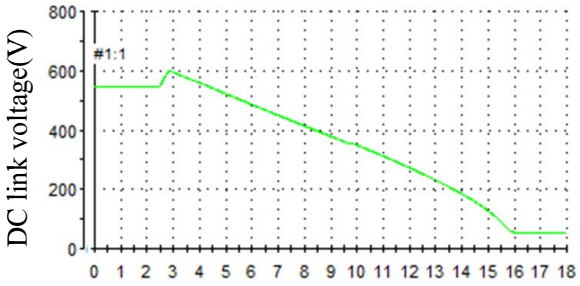


Fig.11 DC link voltage of UPS 1 without DCVP strategy

C. *Power feeding without DC link voltage protection*

When the UPSs are equipped with the DCVP controller, at 4.4s, the same output voltage drifts up from 100V to 103V, which leads to the active power feeding from UPS 2 to UPS 1. When the active power in UPS 1 falls below zero, the falling edge signal activates the DCVP controller which increases the voltage reference of UPS1 to prevent the further feeding of active power, which can be observed in Fig.12. It can be seen that at the time 4.5s, the active power feeding occurs and active power of UPS 1 quickly drops below zero, at this time, the DCVP is activated and increases the voltage reference amplitude of UPS1 to generate more active power and counteract the injected power. Therefore, at the time 4.6s, the active power increased from -50W to 170W. Moreover, the DC link voltage of V_{DC1} are shown in Fig.13, it is seen that DC link voltage of UPS1 V_{DC1} increases from 549V at 4.4s but stabilized at 555V at 4.6s. However, due to the power feeding, the active power P_2 is greater than the P_1, leading to the significant fundamental circulating current between the two UPS modules(Fig.14). This issue will be solved in the next subsection.

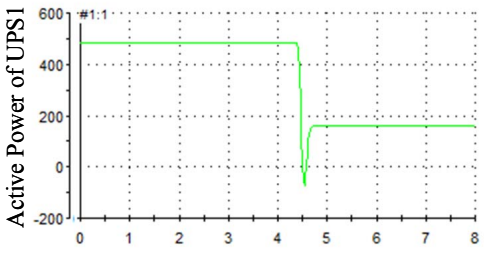


Fig.12 UPS 1's active power with DCVP

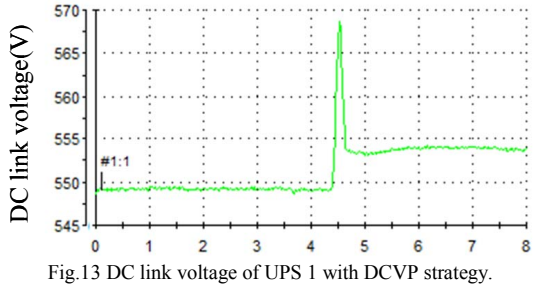


Fig.13 DC link voltage of UPS 1 with DCVP strategy.

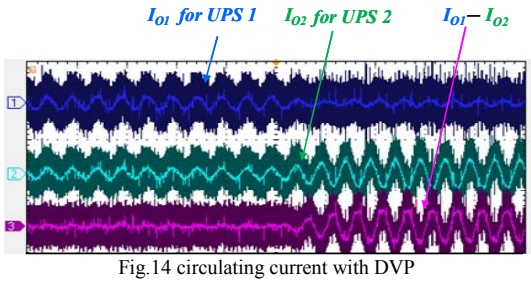


Fig.14 circulating current with DVP

D. *Active Power Sharing Activation*

As seen in the previous subsection, after enabling the DCVP controller, the circulating current caused by the active power feeding exists in the UPS system. Thus, the active power sharing strategy should be activated to mitigate the circulating current. Therefore, a signal flag enables the activation of the active power current sharing controller at t_3. As is shown in Fig.15, due to on-line adjustment of the virtual resistance in the control strategy, with the fundamental current sharing strategy activation, active power equalization for P_1 and P_2 is achieved, the circulating current between I_{o1} and I_{o2} are minimized, which can be observed in Fig.15.

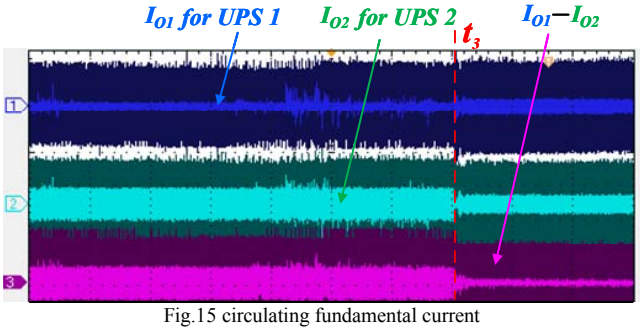


Fig.15 circulating fundamental current

E. *Harmonic Power Sharing Activation*

Line impedance mismatching may lead to the harmonic power sharing errors when the nonlinear load is connected at the terminal. In this section, three phase R-L-C type nonlinear load is connected at the terminal. 0.4Ω of line resistance in UPS 1 and 0.2Ω of line resistance in UPS2 are connected, respectively. Before harmonic power sharing strategy activation. The line resistance mismatching (the small value of line resistance in UPS 2 side) leads to the higher output harmonic current, as is shown in Fig.16. When the harmonic power sharing signal flips from zero to 1, the harmonic power begins to share as shown in Fig.17, the process of harmonic current sharing takes 250s. After completion of harmonic current sharing, the output harmonic current of UPS1 and UPS2 are equalized, as is shown in Fig.18 (a)-(b). the circulating harmonic current is minimized.

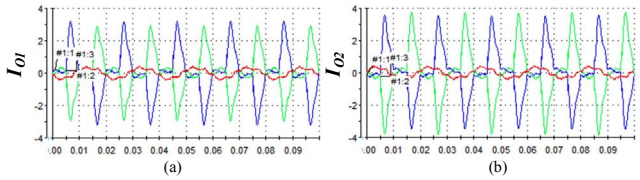


Fig.16 output current for UPS1 and UPS2 without harmonic current sharing

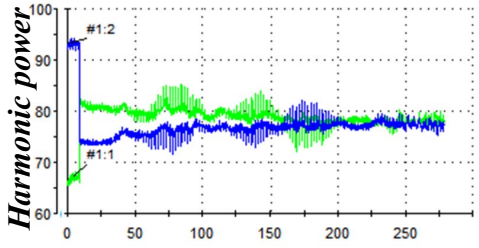
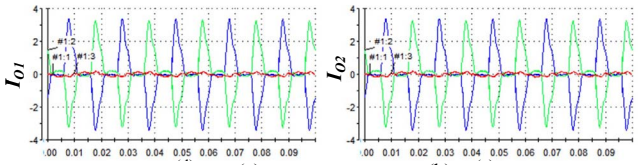


Fig.17 harmonic power sharing process

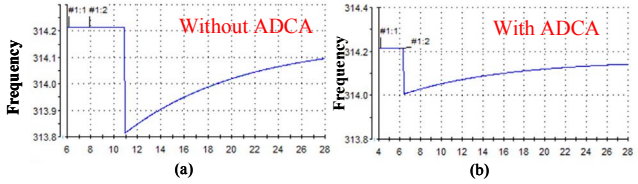


(a) (b)

Fig.18 Output current for UPS1 and UPS2 after harmonic current sharing

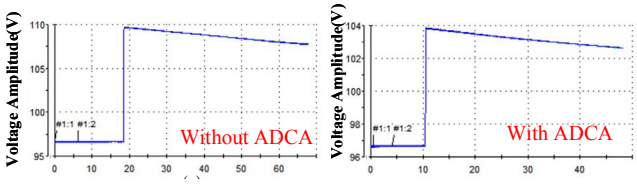
F. Transient performance for the frequency and voltage amplitude restoration under load change

The transient frequency and voltage amplitude performance under load disturbance is examined by comparing the DCA and ADCA strategy. When the UPS's load switch from full load to half load, the frequency drops from 314.19Hz to313.8Hz(Fig.19(a)) with only DCA while the frequency's deviation reduced by 50% when adopting ADCA(Fig.19(b)). By comparison, it is seen that frequency undershoot alleviated due to the ADCA strategy. Meanwhile, the voltage amplitude steps up to 110V with only DCA as shown in Fig.20(a). However, the voltage amplitude deviation drop to 104V with ADCA.



(a) (b)

Fig.19 Comparison of frequency deviation with ADCA and DCA



(a) (b)

Fig.20. Comparison of voltage amplitude deviation with ADCA and DCA

V. CONCLUSION

This paper discussed an enhanced control scheme for parallel UPS system, first, a DC link voltage protection strategy was proposed to prevent the power back feeding. With the DCVP control strategy, the power back feeding issue can be greatly mitigated. Moreover, the active power sharing and harmonic power sharing strategy for UPS system is proposed for the current sharing caused by line resistance mismatching or power back feeding. Finally, an anti-windup dynamic consensus algorithm is proposed to alleviate the overshoot issue in the frequency and voltage amplitude restoration process. Experimental results show the effectiveness of the proposed methods.

REFERENCES

[1] G. N. Rajani, "Emerging trends in Uninterrupted Power Supplies: Patents view," in *2016 Biennial International Conference on Power and Energy Systems: Towards Sustainable Energy (PESTSE)*, 2016, pp. 1-5.

[2] M. S. Racine, J. D. Parham, and M. H. Rashid, "An overview of uninterruptible power supplies," in *Proceedings of the 37th Annual North American Power Symposium, 2005.*, 2005, pp. 159-164.

[3] "EN 62040-3 Uninterruptible power systems (UPS) – Part 3: Method of specifying the performance and test requirements."

[4] C. Zhang, J. M. Guerrero, J. C. Vasquez, and E. A. A. Coelho, "Control Architecture for Parallel-Connected Inverters in Uninterruptible Power Systems," *IEEE Transactions on Power Electronics,* vol. 31, no. 7, pp. 5176-5188, 2016.

[5] C. Zhang, J. M. Guerrero, J. C. Vasquez, and C. M. Seniger, "Modular Plug and Play Control Architectures for Three-Phase Inverters in UPS Applications," *IEEE Transactions on Industry Applications,* vol. 52, no. 3, pp. 2405-2414, 2016.

[6] E. K. Sato, M. Kinoshita, Y. Yamamoto, and T. Amboh, "Redundant High-Density High-Efficiency Double-Conversion Uninterruptible Power System," *IEEE Transactions on Industry Applications,* vol. 46, no. 4, pp. 1525-1533, 2010.

[7] "IEC_62040-3-2011 Uninterruptible power systems (UPS) –Part 3: Method of specifying the performance and test requirements."

[8] C. Zhang, E. A. A. Coelho, J. M. Guerrero, and J. C. Vasquez, "Modular Online Uninterruptible Power System Plug n Play Control and Stability Analysis," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 6, pp. 3765-3776, 2016.

[9] P. Yunqing, J. Guibin, Y. Xu, and W. Zhaoan, "Auto-master-slave control technique of parallel inverters in distributed AC power systems and UPS," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, vol. 3, pp. 2050-2053 Vol.3.

[10] S. Xiao, L. Yim-Shu, and X. Dehong, "Modeling, analysis, and implementation of parallel multi-inverter systems with instantaneous average-current-sharing scheme," *IEEE Transactions on Power Electronics,* vol. 18, no. 3, pp. 844-856, 2003.

[11] H. Shang-Hung, K. Chun-Yi, L. Tzung-Lin, and J. M. Guerrero, "Droop-controlled inverters with seamless transition between islanding and grid-connected operations," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2196-2201.

[12] K. Piboonwattanakit and W. Khan-ngern, "Design of the Two Parallel Inverter Modules by Circular Chain Control Technique," in *2007 7th International Conference on Power Electronics and Drive Systems*, 2007, pp. 1518-1522.

[13] J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, "Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters," *Industrial Electronics, IEEE Transactions on,* vol. 60, no. 4, pp. 1271-1280, 2013.

[14] Q. Shafiee, J. M. Guerrero, and J. C. Vasquez, "Distributed Secondary Control for Islanded Microgrids—A Novel Approach," *Power Electronics, IEEE Transactions on,* vol. 29, no. 2, pp. 1018-1031, 2014.

[15] M. Lexuan *et al.*, "Distributed Voltage Unbalance Compensation in Islanded Microgrids by Using a Dynamic Consensus Algorithm," *Power Electronics, IEEE Transactions on,* vol. 31, no. 1, pp. 827-838, 2016.

[16] H. P. Glauser, M. Keller, A. Pluss, M. Schwab, and R. Scherwey, "New inverter module with digital control for parallel operation," in *TELESCON 2000. Third International Telecommunications Energy Special Conference (IEEE Cat. No.00EX424)*, 2000, pp. 265-269.

[17] N. Rasmussen, "Eco-mode: Benefits and Risks of Energy-saving Modes of UPS Operation," 2012.

[18] L. Giuntini, "Active damping control of multi-mode UPS for power quality improvement," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-10.

[19] F. Xiao, L. Dong, L. Li, and X. Liao, "A Frequency-Fixed SOGI-Based PLL for Single-Phase Grid-Connected Converters," *IEEE Transactions on Power Electronics,* vol. 32, no. 3, pp. 1713-1719, 2017.

[20] J. Schiffer, T. Seel, J. Raisch, and T. Sezi, "Voltage Stability and Reactive Power Sharing in Inverter-Based Microgrids With Consensus-Based Distributed Voltage Control," *Control Systems Technology, IEEE Transactions on,* vol. 24, no. 1, pp. 96-109, 2016.

[21] M. Mehyar, D. Spanos, J. Pongsajapan, S. H. Low, and R. M. Murray, "Asynchronous Distributed Averaging on Communication Networks," *IEEE/ACM Transactions on Networking,* vol. 15, no. 3, pp. 512-520, 2007.

[22] A. R. Teel, "Windup in Control: Its Effects and Their Prevention (by Hippe, P.; 2006)," *IEEE Transactions on Automatic Control,* vol. 53, no. 8, pp. 1976-1977, 2008.