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Research On Variable-Length Transfer Delay and Delayed Signal Cancellation Based PLLs

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***Abstract*—In power and energy applications, implementing a large number of phase-locked loops (PLLs) involves using transfer delays. These delays are employed for different control and filtering purposes, such as creating a fictitious orthogonal signal (which is required for the frame transformation in single-phase PLLs) and filtering harmonics, dc offset, and other disturbances. Depending on the application in hand and the expected variation range of the grid frequency, the length of these delays may be variable or fixed. Roughly speaking, the variable-length delays are often preferred for applications where large frequency drifts are anticipated and a high accuracy is required. To the best of authors' knowledge, the small-signal modeling of a variable-length delay-based PLL has not yet been conducted. The main aim of this paper is to cover this gap. The tuning procedure and analysis of these PLLs are then presented. As design examples, some well-known single-phase and three-phase PLLs are considered.**

***Index Terms*—Delayed signal cancelation, orthogonal signal, phase-locked loop (PLL), single-phase systems, synchronization, three-phase systems, transfer delay.**

I. Introduction

TRANSFER delay is highly popular for creating a fictitious orthogonal signal in single-phase phase-locked loops (PLLs) [1]–[5]. This signal is needed for the frame transformation. For this purpose, the single-phase signal is delayed by a quarter cycle[1] to create 90° phase shift. A PLL with such orthogonal signal generator (OSG) is often referred to as the transfer delayed-based PLL (TD-PLL). A review of different TD-PLLs can be found in [11].

The transfer delay is also a key element in implementing finite impulse response (FIR) filters, which are widely used for enhancing the PLL filtering capability under adverse grid conditions. The most popular FIR filter in the PLL applications is probably the delayed signal cancellation (DSC) operator [12], [13], mainly because it offers a high customizability[2] to deal with different grid scenarios. Notice that this operator may be used as a prefilter before the PLL input or as an in-loop filter inside its control loop [14]–[21]. The former type [here referred to as the $\alpha\beta$-frame DSC ($\alpha\beta$DSC) operator] is often preferred as it leads to a faster dynamic behavior.

A delay-based OSG and $\alpha\beta$DSC operators are both highly sensitive to the grid frequency variations and may not operate effectively in this condition [11], [22]. To deal with this problem, two approaches may be used. The first approach is keeping the length of their delays fixed and using some simple compensators for correcting errors [5], [21]. Roughly speaking, this method offers a great simplicity, but it is efficient only for applications where the grid frequency deviation from its nominal value is not very large. The second approach is adjusting the length of delay(s) using an estimation of the grid frequency, which may be provided by a frequency feedback loop from the PLL output [1], [2], [16], [17] or through a parallel frequency detector [14], [15], [18]. This method works effectively even for large frequency drifts, but increases the PLL implementation complexity and modeling.

Developing the small-signal model for a PLL is highly beneficial, as it makes its dynamics assessment and tuning procedure easy yet effective. For the single-phase and three-phase fixed-length delay-based PLLs, the small-signal modeling procedures have already been described in [5] and [21], respectively. However, to the best of authors' knowledge, the modeling of variable-length delay-based PLLs has not yet been conducted. Covering this gap is the main objective of this paper.

II. Modeling, Analysis, and Tuning of a Variable-Length TD-PLL (VLTD-PLL)

A. Description and Modeling

Fig. 1(a) shows the block diagram of a VLTD-PLL, in which $\hat{\omega}_g$ and $\hat{\theta}$ are estimations of the grid voltage angular frequency, and phase angle, respectively, and ω_n is the nominal frequency. k_i and k_p denote the integral and proportional gains of the loop controller, which is a proportional-integral (PI) regulator, and τ is the time constant of the low-pass filter (LPF) used in the frequency feedback loop. This PLL uses a quarter cycle delay for creating a fictitious orthogonal signal, i.e., v_β. The length of this delay is variable and it is adjusted using an estimation of the grid voltage period, which is calculated using the frequency

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[1]Creating a fictitious orthogonal signal using a delay length less than a quarter cycle is also possible [6]–[10]. But, it may reduce the PLL high-frequency noise immunity and, therefore, it should be used carefully under a noisy environment.

[2]Depending on the grid distortion pattern, a particular number of DSC operators with different delay lengths can be cascaded.

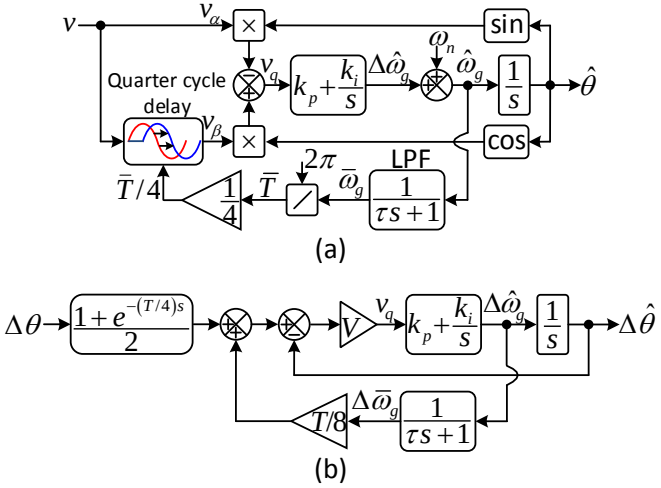

Fig. 1. Block diagram of (a) the VLTD-PLL, and (b) its small-signal model.

detected by the PLL. In what follows, the modeling procedure of this PLL is shown.

Assume that the input signal of the VLTD-PLL is as

$$v(t) = v_\alpha(t) = V\cos(\overbrace{\omega_g t+\varphi}^{\theta}) \tag{1}$$

where θ, V, ω_g, and φ denote its phase angle, amplitude, angular frequency, and initial phase angle, respectively. In this case, the orthogonal signal v_β can be expressed as

$$v_\beta(t) = v(t-\bar{T}/4) = V\cos(\theta-\omega_g\bar{T}/4) \tag{2}$$

where $\bar{T}=2\pi/\bar{\omega}_g$ is an estimation of the grid voltage period.

Using (1) and (2), the signal v_q (the PI regulator input signal) in Fig. 1(a) can be obtained as

$$\begin{aligned} v_q(t) &= -v(t)\sin(\hat{\theta})+v_\beta(t)\cos(\hat{\theta}) \\ &= -V\cos(\theta)\sin(\hat{\theta})+V\cos(\theta-\omega_g\bar{T}/4)\cos(\hat{\theta}). \end{aligned} \tag{3}$$

Applying trigonometry identities to (3) results in

$$\begin{aligned} v_q(t) = \frac{V}{2}\Big[&\sin(\theta-\hat{\theta})+\cos(\theta-\omega_g\bar{T}/4-\hat{\theta}) \\ &+\cos(\theta-\omega_g\bar{T}/4+\hat{\theta})-\sin(\theta+\hat{\theta})\Big]. \end{aligned} \tag{4}$$

By defining $\omega_g=\omega_n+\Delta\omega_g$ and $\bar{\omega}_g=\omega_n+\Delta\bar{\omega}_g$, the nonlinear term $\omega_g\bar{T}/4$ in (4) can be expressed as

$$\begin{aligned} \omega_g\bar{T}/4 &= \frac{2\pi}{4}\frac{\omega_g}{\bar{\omega}_g} = \frac{2\pi}{4}\frac{\omega_n+\Delta\omega_g}{\omega_n+\Delta\bar{\omega}_g} \\ &= \frac{2\pi}{4}(1+\Delta\omega_g/\omega_n)\frac{\mathbf{1}}{\mathbf{1+\Delta\bar{\omega}_g/\omega_n}}. \end{aligned} \tag{5}$$

Replacing the highlighted term in (5) by the first two terms of its Taylor series expansion about zero results in

$$\begin{aligned} \omega_g\bar{T}/4 &\approx \frac{2\pi}{4}(1+\Delta\omega_g/\omega_n)(1-\Delta\bar{\omega}_g/\omega_n) \\ &= \frac{2\pi}{4}(1+\Delta\omega_g/\omega_n-\Delta\bar{\omega}_g/\omega_n-\overbrace{\Delta\omega_g\Delta\bar{\omega}_g/\omega_n^2}^{\text{negligible}}) \\ &\approx \frac{\pi}{2}+\frac{T}{4}\Delta\omega_g-\frac{T}{4}\Delta\bar{\omega}_g. \end{aligned} \tag{6}$$

Substituting the nonlinear term $\omega_g\bar{T}/4$ in (4) by its linear approximation, i.e., (6), yields

$$\begin{aligned} v_q(t) \approx \frac{V}{2}\Big[&\sin(\theta-\hat{\theta})+\sin\left(\theta-\hat{\theta}-[T/4][\Delta\omega_g-\Delta\bar{\omega}_g]\right) \\ &+\mathbf{\sin\left(\theta+\hat{\theta}-[T/4][\Delta\omega_g-\Delta\bar{\omega}_g]\right)-\sin\left(\theta+\hat{\theta}\right)}\Big]. \end{aligned} \tag{7}$$

Assuming that $\Delta\omega_g \approx \Delta\bar{\omega}_g$, the double-frequency terms (highlighted terms) in (7) cancel each other. In this case, by defining $\theta=\theta_n+\Delta\theta$ and $\hat{\theta}=\theta_n+\Delta\hat{\theta}$, where $\theta_n=\int\omega_n dt$, and assuming that $\Delta\theta\approx\Delta\hat{\theta}$, (7) can be approximated by

$$v_q(t) \approx V\left[\frac{\Delta\theta+\Delta\theta-(T/4)\Delta\omega_g}{2}-\Delta\hat{\theta}+\frac{T}{8}\Delta\bar{\omega}_g\right]. \tag{8}$$

Applying the Laplace transform to (8) results in

$$v_q(s) \approx V\left[\frac{1+e^{-(T/4)s}}{2}\Delta\theta(s)-\Delta\hat{\theta}(s)+\frac{T}{8}\Delta\bar{\omega}_g(s)\right]. \tag{9}$$

Using (9), the model depicted in Fig. 1(b) can be derived.

B. Tuning and Stability Analysis

Based on Fig. 1(b), the closed-loop transfer function of the VLTD-PLL can be determined as

$$\begin{aligned} G_{cl}(s) &= \frac{\Delta\hat{\theta}(s)}{\Delta\theta(s)} \\ &= \frac{1+e^{-\frac{Ts}{4}}}{2}\frac{V\left(k_p s+k_i\right)(\tau s+1)}{(\tau s+1)\left(s^2+Vk_p s+Vk_i\right)-\frac{T}{8}V\left(k_p s+k_i\right)s}. \end{aligned} \tag{10}$$

Selecting $\tau=k_p/k_i$ leads to a pole-zero cancelation and simplifies (10) as

$$G_{cl}(s) = \frac{1+e^{-(T/4)s}}{2}\frac{V\left(k_p s+k_i\right)}{s^2+\underbrace{V\left(k_p-k_i T/8\right)}_{2\zeta\omega_n'}s+\underbrace{Vk_i}_{(\omega_n')^2}} \tag{11}$$

where ω_n' and ζ represent the natural frequency and the damping factor of the closed-loop poles, respectively. Using this transfer function, the tuning procedure can be easily conducted.

For tuning the control parameters, appropriate values for ω_n' and ζ should first be selected. Effects of these two parameters on the PLL dynamics have been well discussed in the literature [23]. In summary, ζ dictates the damping of dynamic response and ω_n is the major factor in determining the bandwidth and, consequently, the speed of dynamic response and noise immunity. Here, $\zeta=0.707$, which is an optimum damping factor[3], and $\omega_n'=2\pi 20$ rad/s are chosen. Based on these

[3]If a more damped dynamic response is preferred, $\zeta=1$ may be selected.

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selected values and the relation of ζ and ω_n' with k_p and k_i [see (11)], the control parameters can be calculated as

$$\begin{aligned} k_i &= \frac{(\omega_n')^2}{V} = 15791 \\ k_p &= \frac{\omega_n'\,(2\zeta + \omega_n' T/8)}{V} = 217 \\ \tau &= k_p/k_i = 0.01375. \end{aligned} \tag{12}$$

Notice that $V = 1$ p.u. is assumed.

For the stability analysis, the Routh-Hurwitz criterion is applied to the characteristic polynomial of (11). The result is as follows

$$\begin{aligned} k_i &> 0 \\ k_p &> \frac{T}{8} k_i. \end{aligned} \tag{13}$$

C. Model Accuracy Assessment

As the tuning and stability analysis of the VLTD-PLL was based on its small-signal model, a model accuracy evaluation needs to be performed. For this purpose, the performance of the VLTD-PLL and its model in response to two tests (a phase jump test and a frequency jump test) are compared. The results of these tests, which are conducted in the Matlab/Simulink environment, can be observed in Fig. 2. These results demonstrate that the model derived for the VLTD-PLL can predict its average behavior accurately and, consequently, is trustable for its dynamics assessment.

It is worth mentioning here that there are some double-frequency oscillations in the transient response of the VLTD-PLL where the model cannot predict. This is because of neglecting the double-frequency terms in (7) during the modeling procedure. Taking into account these terms results in a more accurate model (particularly for the stability analysis when the PLL bandwidth is high), and is going to be presented in a future work.

D. Performance Evaluation

In this section, the performance of the VLTD-PLL is evaluated using some dSPACE-based experimental results. The VLTD-PLL control parameters can be found in (12). The sampling and nominal frequencies are set to 8 kHz and 50 Hz, respectively. A linear interpolation method is used when a fractional delay approximation is required. Such situation happens when the grid frequency deviates from its nominal value and the delay length (which is a quarter cycle) is not divisible by the sampling period.

As a reference for comparison, a very recently designed PLL, referred to as the adaptive TD-PLL (ATD-PLL) [3] is considered. The ATD-PLL block diagram is shown in Fig. 3(a) and its small-signal model can be observed in Fig. 3(b) [3]. The ATD-PLL uses a fixed-length quarter cycle delay for generating the quadrature signal and a nonlinear frequency feedback system to correct the quadrature signal errors under frequency drifts. Notice that the ATD-PLL considers the PI controller integrator output as the estimated frequency.

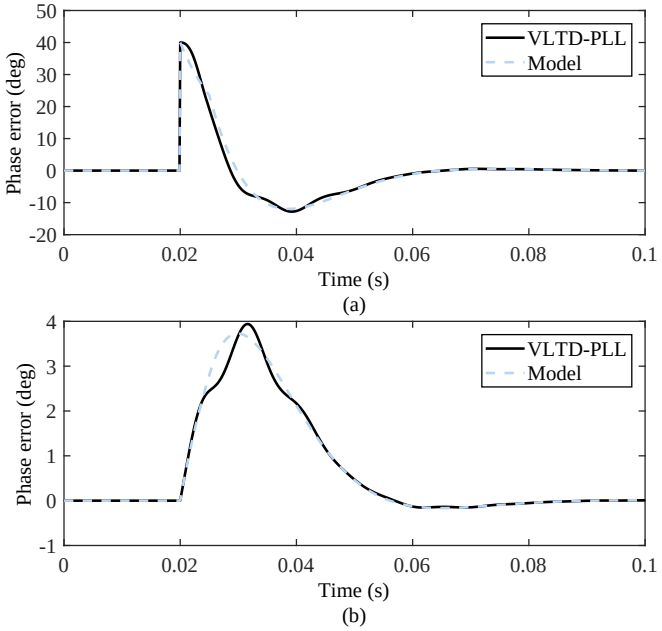

Fig. 2. Model accuracy assessment of the VLTD-PLL in response to (a) $+40^\circ$ phase jump and (b) +2 Hz frequency jump. Control parameters: $k_i = 15791$, $k_p = 217$, $\tau = 0.01375$ s. The nominal and sampling frequencies are 50 Hz and 8 kHz, respectively.

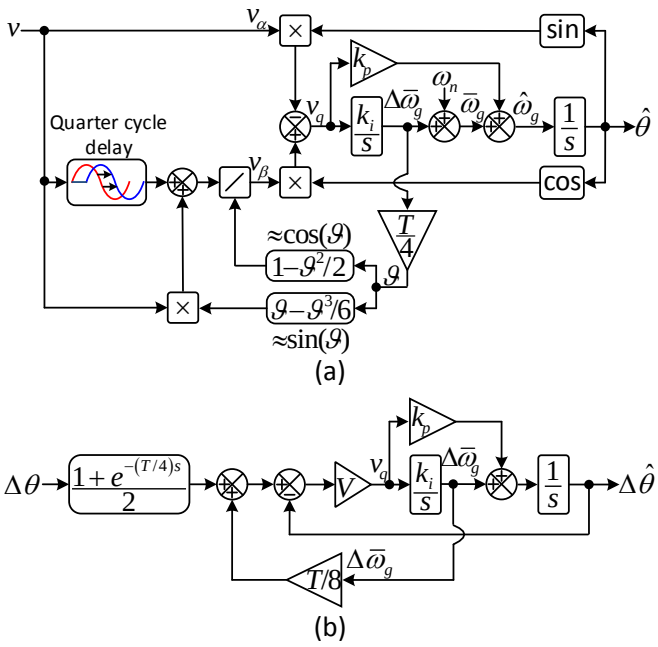

Fig. 3. Block diagram of the ATD-PLL and (b) its small-signal model [3].

Using Fig. 3(b), the closed-loop transfer function of the ATD-PLL can be obtained as

$$G_{cl}(s) = \frac{1 + e^{-(T/4)s}}{2} \frac{V\,(k_p s + k_i)}{s^2 + V\,(k_p - k_i T/8)\,s + V k_i}. \tag{14}$$

This transfer function is the same as (11). It means that the VLTD-PLL and ATD-PLL are equivalent, at least from a small-signal perspective. Consequently, to have a fair comparison, the proportional and integral gains of the ATD-PLL

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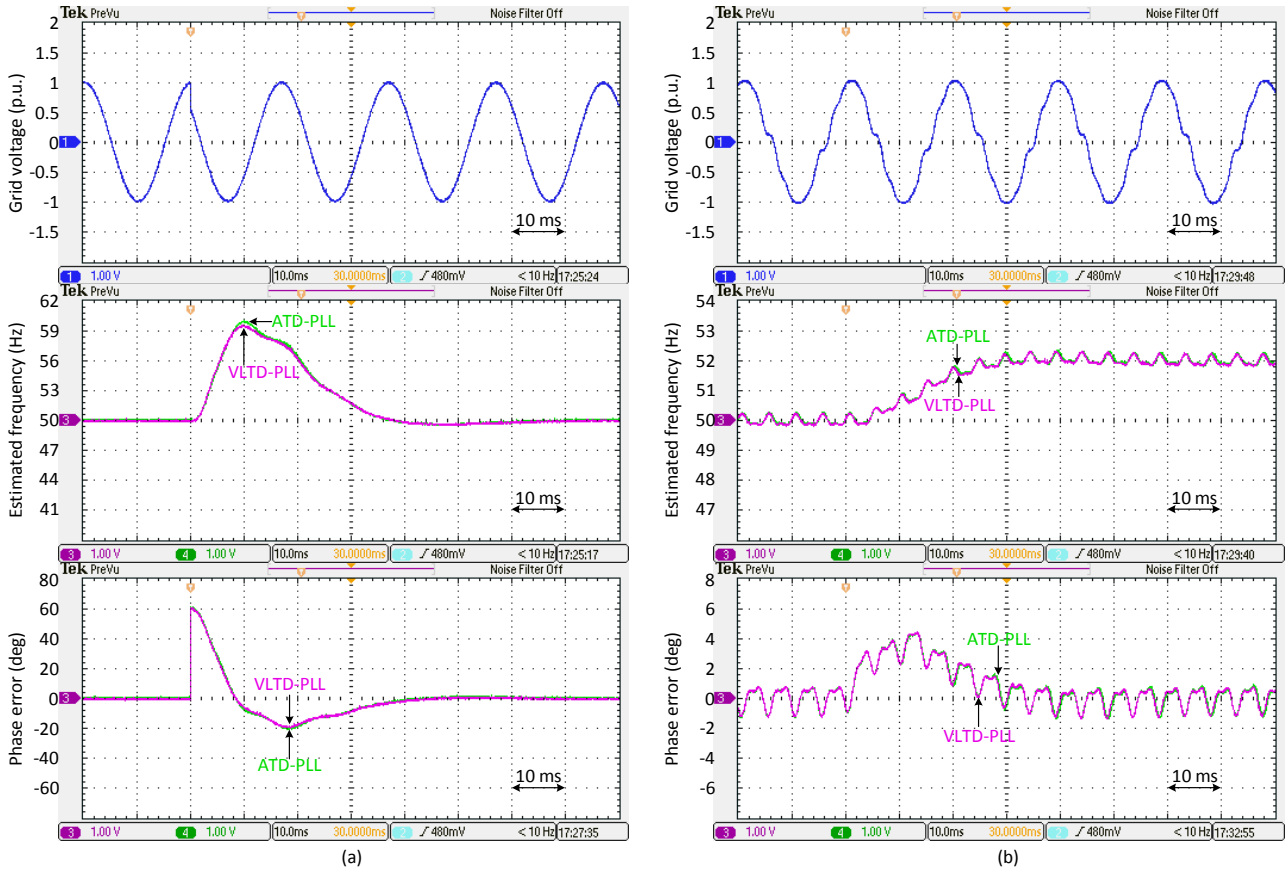

Fig. 4. Performance comparison between the VLTD-PLL and ATD-PLL in response to (a) a 60° phase-angle jump, and (b) a +2-Hz frequency jump under a harmonically distorted grid. In both the VLTD-PLL and ATD-PLL, the signal $\bar{\omega}_g$ is considered as the estimated frequency.

should be the same as those of the VLTD-PLL. Notice that (11) is obtained by arranging a pole-zero cancellation in the original closed-loop transfer function of the VLTD-PLL [i.e., (10)]. Therefore, the equivalence of the VLTD-PLL and ATD-PLL is valid as long as the pole-zero cancellation is considered. It should be emphasized here that this pole-zero cancellation is an optimum choice in the tuning procedure of the VLTD-PLL.

Fig. 4(a) compares the VLTD-PLL and ATD-PLL performance in response to a 60° phase-angle jump, and Fig. 4(b) evaluates their performance under a harmonically-distorted (5% third harmonic, 4% fifth harmonic, 5% seventh harmonic, and 3% ninth harmonic) and frequency-varying environment. As expected, both PLLs demonstrate practically identical results (a settling time around two cycles of the nominal frequency during transients and a rather acceptable harmonic filtering capability), which means they are equivalent systems. This equivalence and more straightforward implementation of the ATD-PLL (which is because of its fixed-length delay) suggest that the ATD-PLL is a better option than the VLTD-PLL.

III. Modeling, Analysis, and Tuning of Adaptive $\alpha\beta$DSC Operator-Based PLLs

A. A Simple Case

In this section, the modeling procedure of a three-phase PLL with an adaptive $\alpha\beta$DSC operator-based prefiltering stage (briefly referred to as the $\alpha\beta$DSC-PLL) is presented. This procedure is extended to the more advanced versions of this PLL later. It should be emphasized here that the $\alpha\beta$DSC-PLL is the simplest possible form of advanced PLLs developed in [14] and [17].

Fig. 5(a) shows the block diagram of the $\alpha\beta$DSC-PLL, which consists of an $\alpha\beta$DSC operator with variable-length delays and a conventional synchronous reference frame PLL (SRF-PLL). The operator is responsible to reject some disturbances and extract the grid voltage fundamental component. The length of delays of the operator, which is adjusted using the estimated period, is $1/n$ cycle, where n is referred to as the delay factor. The rotation matrix $R(\theta_r)$ in the operator is expressed as

$$R(\theta_r) = \begin{bmatrix} \cos(\theta_r) & -\sin(\theta_r) \\ \sin(\theta_r) & \cos(\theta_r) \end{bmatrix} \tag{15}$$

where $\theta_r = 2\pi/n$.

Assume that the three-phase input signals of the $\alpha\beta$DSC-PLL are as

$$\begin{aligned} v_a(t) &= V\cos(\overbrace{\omega_g t + \varphi}^{\theta}) \\ v_b(t) &= V\cos(\theta - 2\pi/3) \\ v_c(t) &= V\cos(\theta + 2\pi/3). \end{aligned} \tag{16}$$

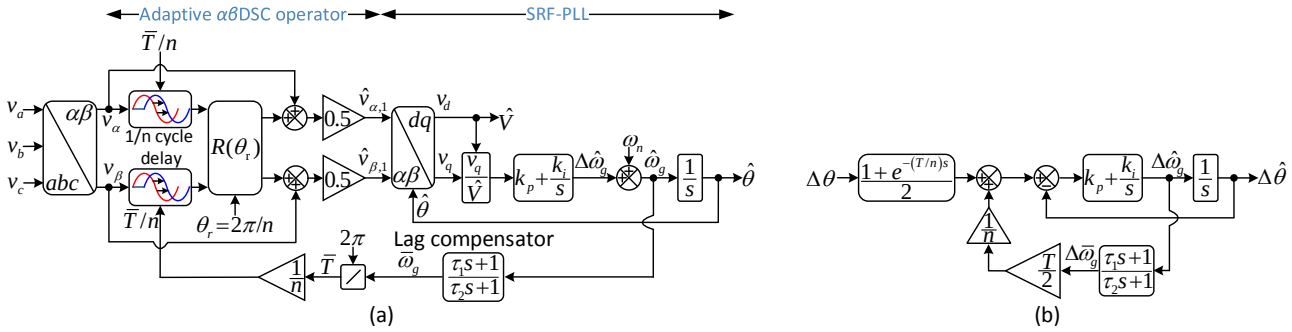

Fig. 5. (a) Block diagram of the $\alpha\beta$DSC-PLL, and (b) its small-signal model.

In the $\alpha\beta$-frame, these signals are corresponding to

$$\begin{aligned} v_\alpha(t) &= V\cos(\theta) \\ v_\beta(t) &= V\sin(\theta). \end{aligned} \tag{17}$$

Using (15), (17), and Fig. 5(a), the output signals of the $\alpha\beta$DSC operator can be expressed as

$$\begin{aligned} \hat{v}_{\alpha,1}(t) &= 0.5\big[v_\alpha(t) + \cos(2\pi/n)\, v_\alpha(t-\bar{T}/n) \\ &\quad - \sin(2\pi/n)\, v_\beta(t-\bar{T}/n)\big] \\ &= 0.5V\left[\cos(\theta) + \cos(\theta - \omega_g\bar{T}/n + 2\pi/n)\right] \end{aligned} \tag{18}$$

$$\begin{aligned} \hat{v}_{\beta,1}(t) &= 0.5\big[v_\beta(t) + \sin(2\pi/n)\, v_\alpha(t-\bar{T}/n) \\ &\quad + \cos(2\pi/n)\, v_\beta(t-\bar{T}/n)\big] \\ &= 0.5V\left[\sin(\theta) + \sin(\theta - \omega_g\bar{T}/n + 2\pi/n)\right] \end{aligned} \tag{19}$$

where $\bar{T} = 2\pi/\bar{\omega}_g$, as shown in Fig. 5(a), is an estimation of the grid voltage period.

Using (18), (19), and Fig. 5(a), the signal v_q (the PI controller input signal) can be obtained as

$$\begin{aligned} v_q(t) &= -\sin(\hat{\theta})\hat{v}_{\alpha,1}(t) + \cos(\hat{\theta})\hat{v}_{\beta,1}(t) \\ &= 0.5V\left[\sin(\theta-\hat{\theta}) + \sin(\theta-\hat{\theta}+2\pi/n - \omega_g\bar{T}/n)\right]. \end{aligned} \tag{20}$$

By following the same procedure described in Section II-A, it can be shown that the nonlinear term $\omega_g\bar{T}/n$ in (20) can be approximated by

$$\omega_g\bar{T}/n \approx \frac{2\pi}{n} + \frac{T}{n}\Delta\omega_g - \frac{T}{n}\Delta\bar{\omega}_g. \tag{21}$$

Substituting (21) into (20) and considering the definitions $\theta = \theta_n + \Delta\theta$ and $\hat{\theta} = \theta_n + \Delta\hat{\theta}$ yield

$$\begin{aligned} v_q(t) \approx 0.5V\Big[&\sin(\Delta\theta - \Delta\hat{\theta}) \\ &+ \sin(\Delta\theta - \Delta\hat{\theta} - \Delta\omega_g T/n + \Delta\bar{\omega}_g T/n)\Big]. \end{aligned} \tag{22}$$

Approximating sine terms by their arguments results in

$$v_q(t) \approx V\left[\frac{\Delta\theta + \Delta\theta - \Delta\omega_g T/n}{2} + \Delta\bar{\omega}_g T/(2n) - \Delta\hat{\theta}\right]. \tag{23}$$

Applying the Laplace transform to (23) gives

$$v_q(s) \approx V\left[\frac{1+e^{-(T/n)s}}{2}\Delta\theta(s) + \{T/(2n)\}\,\Delta\bar{\omega}_g(s) - \Delta\hat{\theta}(s)\right]. \tag{24}$$

Based on (24), the $\alpha\beta$DSC-PLL model can be derived as shown in Fig. 5(b). Notice that, because of the amplitude normalization, the amplitude V does not appear in the model.

B. An Advanced Case: Cascaded Delayed Signal Cancellation PLL (CDSC-PLL)

1) Description and Modeling: Fig. 6(a) illustrates the block diagram of an advanced three-phase PLL, referred to as the CDSC-PLL [16], [17]. This PLL uses five cascaded $\alpha\beta$DSC operators with the delay length of $1/2$, $1/4$, $1/8$, $1/16$, and $1/32$ cycle. Notice that this combination of operators can remove the dc component and almost all harmonics[4] in the SRF-PLL input. Notice also that the length of the delays of the operators is adjusted using a frequency feedback loop. It should be emphasized here that the original CDSC-PLL [16], [17] uses a first-order LPF in its frequency feedback loop. Here, it is replaced by a lag compensator, as it provides a higher design flexibility.

In Section III-A, the modeling procedure of a simple version of the CDSC-PLL was described. Based on that procedure, the model shown in Fig. 6(b) can be derived for the CDSC-PLL. By applying the block diagram algebra to Fig. 6(b), Fig. 6(c) can be achieved in which

$$\begin{aligned} H(s) = \frac{T}{2}\Bigg[&\frac{1}{32} + \frac{1}{16}\frac{1+e^{-(T/32)s}}{2} \\ &+ \frac{1}{8}\frac{1+e^{-(T/16)s}}{2}\frac{1+e^{-(T/32)s}}{2} \\ &+ \frac{1}{4}\frac{1+e^{-(T/8)s}}{2}\frac{1+e^{-(T/16)s}}{2}\frac{1+e^{-(T/32)s}}{2} \\ &+ \frac{1}{2}\frac{1+e^{-(T/4)s}}{2}\frac{1+e^{-(T/8)s}}{2}\frac{1+e^{-(T/16)s}}{2}\frac{1+e^{-(T/32)s}}{2}\Bigg]. \end{aligned} \tag{25}$$

2) Tuning and Stability Analysis: Using Fig. 6(c), the closed-loop transfer function of the CDSC-PLL can be expressed as

$$\begin{aligned} \Delta\hat{\theta}(s) = &\frac{1+e^{-\frac{Ts}{2}}}{2}\frac{1+e^{-\frac{Ts}{4}}}{2}\frac{1+e^{-\frac{Ts}{8}}}{2}\frac{1+e^{-\frac{Ts}{16}}}{2}\frac{1+e^{-\frac{Ts}{32}}}{2} \\ &\frac{k_p s + k_i}{s^2 + [1 - sH(s)L(s)]\,(k_p s + k_i)}\Delta\theta(s) \end{aligned} \tag{26}$$

[4]Harmonics of order -31, $+33$, -63, $+65$,... are not removed.

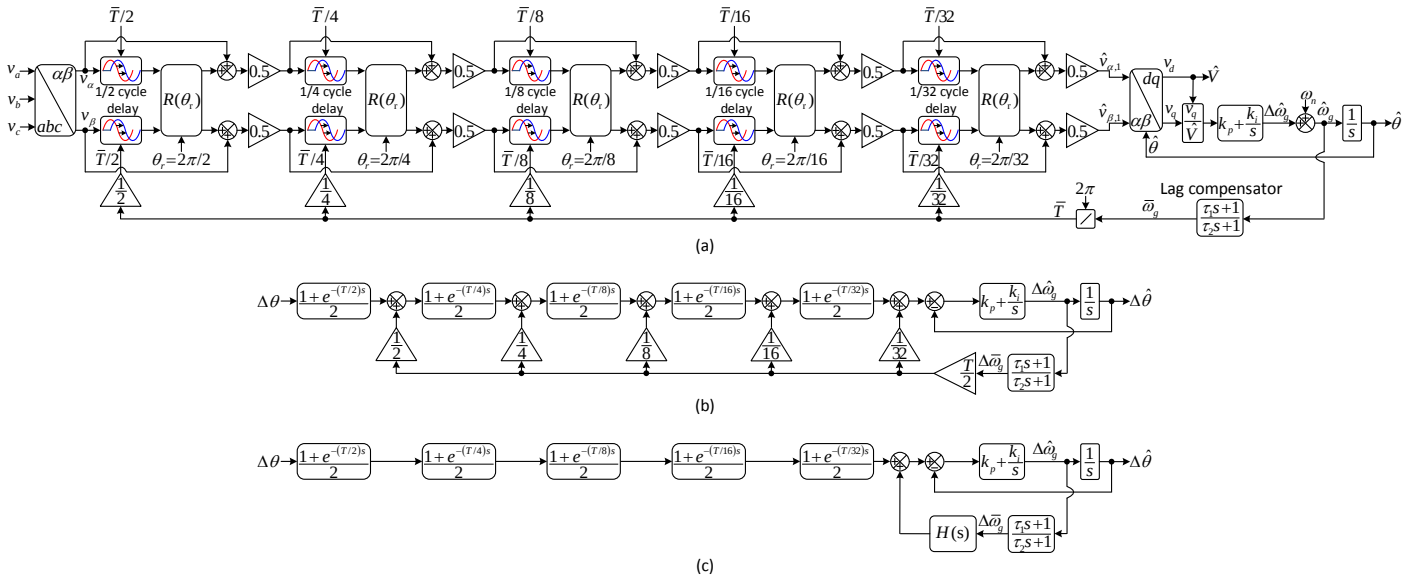

Fig. 6. (a) Block diagram of CDSC-PLL, (b) its small-signal model, and (c) the alternative representation of this model. $\bar{T}$ is an estimation of the grid voltage period, and $T = 0.02$ s is its nominal value.

where $L(s) = \frac{\tau_1 s+1}{\tau_2 s+1}$ denotes the lag compensator.

In the Appendix A, it is shown that the transfer function $H(s)$ in the low-frequency range can be approximated by $H(s) \approx \frac{k_{dc}}{\tau_r s+1}$, where $k_{dc} = 31T/64$ and $\tau_r = 10T/64$. By selecting $\tau_1 = \tau_r = 10T/64$, the product $H(s)L(s)$ can be approximated by

$$L(s)H(s) \approx \frac{\tau_1 s+1}{\tau_2 s+1}\frac{k_{dc}}{\tau_r s+1} = \frac{k_{dc}}{\tau_2 s+1}. \tag{27}$$

Substituting (27) into (26) yields

$$\Delta\hat{\theta}(s) \approx \frac{1+e^{-\frac{Ts}{2}}}{2}\frac{1+e^{-\frac{Ts}{4}}}{2}\frac{1+e^{-\frac{Ts}{8}}}{2}\frac{1+e^{-\frac{Ts}{16}}}{2}\frac{1+e^{-\frac{Ts}{32}}}{2} \frac{(k_p s+k_i)(\tau_2 s+1)}{(\tau_2 s+1)s^2+(\tau_2 s+1-k_{dc}s)(k_p s+k_i)}\Delta\theta(s). \tag{28}$$

By selecting $\tau_2 = k_p/k_i$, a pole-zero cancellation is achieved and (28) can be simplified as

$$\Delta\hat{\theta}(s) \approx \frac{1+e^{-\frac{Ts}{2}}}{2}\frac{1+e^{-\frac{Ts}{4}}}{2}\frac{1+e^{-\frac{Ts}{8}}}{2}\frac{1+e^{-\frac{Ts}{16}}}{2}\frac{1+e^{-\frac{Ts}{32}}}{2} \frac{k_p s+k_i}{s^2+\underbrace{(k_p-k_{dc}k_i)}_{2\xi\omega_n'}s+\underbrace{k_i}_{(\omega_n')^2}}\Delta\theta(s). \tag{29}$$

Now, by selecting appropriate values for the natural frequency ω_n' and the damping factor ζ, the control parameters k_p and k_i are determined. Notice that the $\alpha\beta$DSC operators in the SRF-PLL input completely remove the dc component and all harmonics (except for some high-order harmonics, i.e., those of order $-31, +33, -63, +65, ...$). Therefore, in selecting the natural frequency, there is no need to be worried about these disturbances. Indeed, selecting this parameter should be mainly based on a tradeoff decision between high-frequency noise immunity and transient behavior [21], [22]. The presence of inter-harmonics in the grid voltage is another factor that may need to be considered in designing this parameter in some applications. Here, $\zeta = 1$ and $\omega_n' = 2\pi 35$ are chosen, which results in the following parameters

$$\begin{aligned} k_i &= (\omega_n')^2 = 48361 \\ k_p &= 2\zeta\omega_n' + k_{dc}k_i = 908.3 \\ \tau_2 &= k_p/k_i = 0.01878 \\ \tau_1 &= \tau_r = 10T/64 = 0.003125. \end{aligned} \tag{30}$$

For the stability analysis, the Routh-Hurwitz stability test should be applied to the characteristic polynomial of the closed-loop transfer function (26). The presence of $H(s)$ [see (25)] in this polynomial, however, makes it very complicated. Therefore, the characteristic polynomial of the reduced-order closed-loop transfer function (29) is considered and the Routh-Hurwitz criterion is applied to it, which gives the small-signal stability condition as

$$\begin{aligned} k_i &> 0 \\ k_p &> k_{dc}k_i. \end{aligned} \tag{31}$$

3) Model Accuracy Assessment: Fig. 6(c), as mentioned before, is mathematically equivalent to Fig. 6(b), and is regarded as the original model of the CDSC-PLL here. For the stability analysis and tuning procedure, however, a reduced-order model, which is obtained by replacing $H(s)$ in the original model [Fig. 6(c)] by its first-order counterpart [equation (36)], was used. In this section, the accuracy of both the original model and reduced-order model in predicting the dynamics of the CDSC-PLL is evaluated under phase and frequency jump tests. These tests are conducted in the Matlab/Simulink environment with a sampling frequency of 8 kHz, and their results can be observed in Fig. 7. It is observed that both the original and reduced-order models demonstrate a good accuracy.

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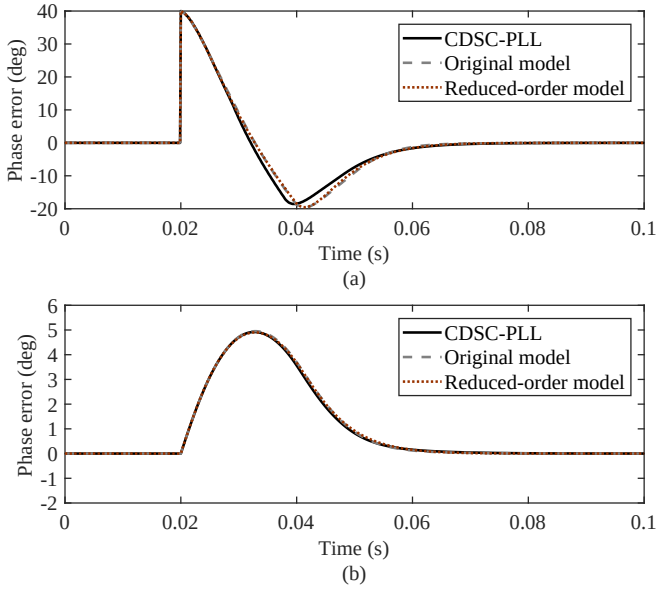

Fig. 7. Model accuracy assessment of the CDSC-PLL in response to (a) $+40^\circ$ phase jump and (b) +2 Hz frequency jump. The original and reduced-order models both refer to Fig. 6(c). The difference is that, in the reduced-order model, $H(s)$ is replaced by its first-order approximation, i.e., (36).

C. An advanced Case: Generalized Delayed Signal Cancellation PLL (GDSC-PLL)

1) Description and Modeling: Fig. 8(a) illustrates the block diagram of the GDSC-PLL [14], which is an advanced three-phase PLL. This structure includes two chains of $\alpha\beta$DSC operators and two SRF-PLLs. Each chain includes five cascaded operators with delay lengths of $1/2$, $1/4$, $1/8$, $1/16$, and $1/32$ cycle. Their only difference is that the first chain is nonadaptive (its operators use fixed-length delays) while the second one is frequency-adaptive (its operators use variable-length delays). The knowledge of the grid frequency, which is required for adjusting the length of delays of the second chain, is provided by the first SRF-PLL. And the outputs of the second SRF-PLL are considered as the estimated grid voltage parameters.

In [21], modeling an SRF-PLL with a chain of nonadaptive $\alpha\beta$DSC operators (i.e., operators with fixed-length delays) in its input was shown. And in Section III-B1, modeling an SRF-PLL with a chain of adaptive $\alpha\beta$DSC operators (i.e., operators with variable-length delays) was demonstrated. Based on these models, developing a model as shown in Fig. 8(b) for the GDSC-PLL is quite straightforward. By applying the block diagram algebra to Fig. 8(b), it can be rearranged as shown in Fig. 8(c), in which the transfer function $H(s)$ is as expressed in (25).

2) Tuning and Stability Analysis: Using Fig. 8(c), the closed-loop transfer function of the GDSC-PLL can be expressed as

$$\Delta\widehat{\theta}(s) = \frac{1+e^{-\frac{Ts}{2}}}{2}\frac{1+e^{-\frac{Ts}{4}}}{2}\frac{1+e^{-\frac{Ts}{8}}}{2}\frac{1+e^{-\frac{Ts}{16}}}{2}\frac{1+e^{-\frac{Ts}{32}}}{2} \left(1+s\frac{H(s)L(s)\left[k_p s+k_i\right]}{s^2+k_p s+k_i}\right)\frac{k_p s+k_i}{s^2+k_p s+k_i}\Delta\theta(s) \quad (32)$$

where $L(s)=\frac{\tau_1 s+1}{\tau_2 s+1}$ denotes the lag compensator.

Substituting the product $H(s)L(s)$ by its first-order approximation [see Section III-B2, particularly, equation (27)] gives

$$\Delta\widehat{\theta}(s) \approx \overbrace{\frac{1+e^{-\frac{Ts}{2}}}{2}\frac{1+e^{-\frac{Ts}{4}}}{2}\frac{1+e^{-\frac{Ts}{8}}}{2}\frac{1+e^{-\frac{Ts}{16}}}{2}\frac{1+e^{-\frac{Ts}{32}}}{2}}^{\approx\frac{1}{(31T/64)s+1}} \left(1+\frac{k_{dc}k_i s}{\tau_2 s+1}\frac{(k_p/k_i)\,s+1}{s^2+k_p s+k_i}\right)\frac{k_i\left[(k_p/k_i)\,s+1\right]}{s^2+k_p s+k_i}\Delta\theta(s). \quad (33)$$

As highlighted in (33), the product of the delay-dependent terms can be approximated in the low-frequency range by $1/[(31T/64)s+1]$. Considering this approximation, two pole-zero cancellations can be arranged by choosing $k_p/k_i=\tau_2=31T/64$. And with this selection, (33) can be simplified as

$$\Delta\widehat{\theta}(s) \approx \frac{k_i\left(s^2+\left[k_p+k_{dc}k_i\right]s+k_i\right)}{\left(s^2+\underbrace{k_p}_{2\zeta\omega_n'}s+\underbrace{k_i}_{(\omega_n')^2}\right)^2}\Delta\theta(s). \quad (34)$$

To avoid an oscillatory dynamic response[5], $\zeta=1$ is chosen. Considering this selection and the ratio of k_p and k_i, which is $k_p/k_i=31T/64$, the natural frequency ω_n' can be calculated as $\omega_n'=\frac{2\zeta}{(k_p/k_i)}=\frac{128}{31T}=206.45$ rad/s. Now, all control parameters can be calculated as follows

$$\begin{aligned} k_i &= (\omega_n')^2 = 42622 \\ k_p &= 2\zeta\omega_n' = 412.9 \\ \tau_2 &= 31T/64 = k_p/k_i = 0.0096875 \\ \tau_1 &= \tau_r = 10T/64 = 0.003125. \end{aligned} \quad (35)$$

Regarding the small-signal stability analysis of the GDSC-PLL, it is clear from the closed-loop transfer function (32) that all roots of the characteristic polynomial are in the left half plane and, therefore, the PLL is stable if the control parameters have positive values.

3) Model Accuracy Assessment: The objective of this section is evaluating the accuracy of the small-signal model developed for the GDSC-PLL. Fig. 8(c), which is mathematically equivalent to Fig. 8(b), is regarded as the original model of GDSC-PLL, and replacing $H(s)$ in this model by its first-order approximation, i.e., (36), results in its reduced-order model. This model accuracy evaluation is conducted under the same condition described in Section III-B3. Fig. 9 illustrates the results of this assessment. As shown, the original and reduced-order models, which demonstrate almost identical results, represent a high accuracy in predicting the GDSC-PLL dynamics.

D. Performance Evaluation

In this section, a performance comparison between the CDSC-PLL [Fig. 6(a)] and GDSC-PLL [Fig. 8(a)] is performed. This study is conducted using a dSPACE 1006 platform. For the sake of convenience, the PLLs input signals are generated inside the dSPACE. The control parameters of the CDSC-PLL and GDSC-PLL can be found in (30) and

[5]According to (34), selecting $\zeta<1$ results in four complex-conjugate poles and, therefore, makes the GDSC-PLL dynamic response oscillatory.

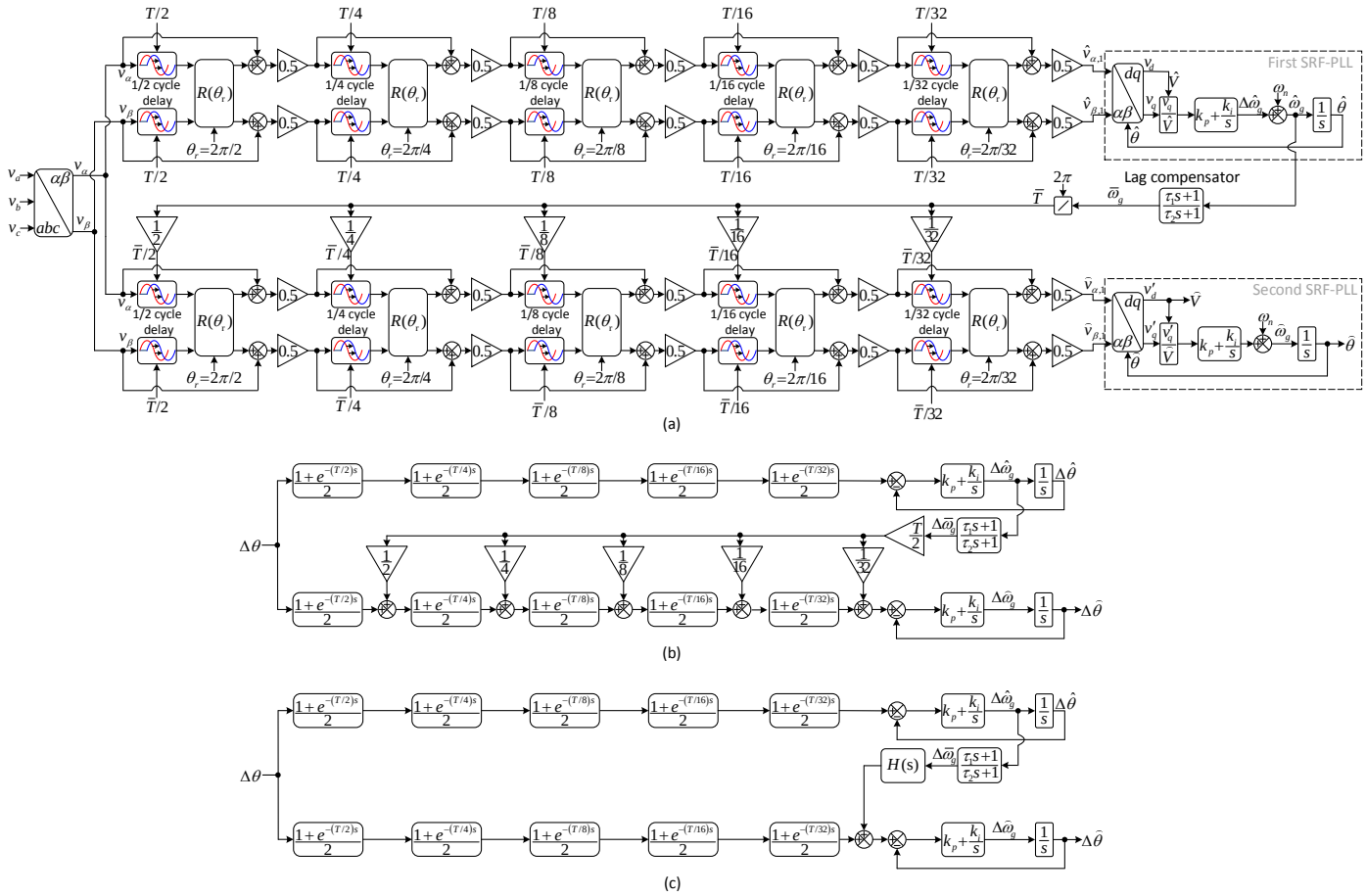

Fig. 8. (a) GDSC-PLL, (b) its small-signal model, and (c) the alternative representation of this model.

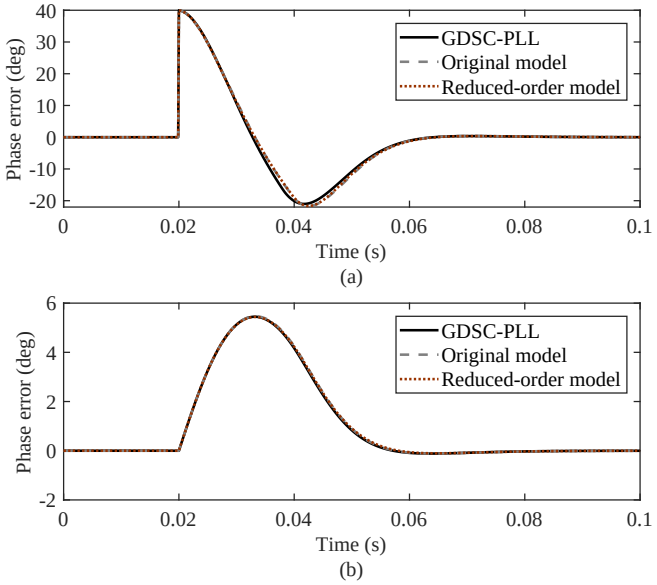

Fig. 9. Model accuracy assessment of the GDSC-PLL in response to (a) $+40°$ phase jump and (b) +2 Hz frequency jump. The original and reduced-order models both refer to Fig. 8(c). The difference is that, in the reduced-order model, $H(s)$ is replaced by its first-order approximation, i.e., (36).

(35), respectively. The sampling and nominal grid frequencies are 8 kHz and 50 Hz, respectively. The variable-length delays in both the CDSC-PLL and GDSC-PLL are realized using a linear interpolation technique.

The following tests are considered.

- Test 1: The grid voltage experiences a 0.5-p.u. symmetrical voltage sag and, at the same time, a $40°$ phase angle jump. The grid frequency is fixed at 50 Hz.
- Test 2: The grid voltage is unbalanced and harmonically distorted and it suddenly experiences a +2-Hz frequency jump. The grid voltage components in this test are $V_{+1} = 1$, $V_{-1} = 0.1$, $V_{+5} = 0.02$, $V_{-5} = 0.07$, $V_{+7} = 0.05$, $V_{-7} = 0.02$, $V_{+11} = 0.01$, $V_{-11} = 0.06$, $V_{+13} = 0.05$, $V_{-13} = 0.01$ p.u., where $+$ and $-$ denotes the sequence of the harmonic components.
- Test 3: Suddenly, an exaggeratedly large DC component (0.1 p.u.) is added to a phase of the grid voltage. The grid frequency is fixed at 50 Hz.

Results of test 1 are shown in Fig. 10(a). Both PLLs demonstrate a close dynamic behavior. The phase and frequency settling times in both PLLs are around 2 cycles of the nominal frequency and the amplitude settling time is around one cycle.

Fig. 10(b) and 10(c) demonstrate the performance of PLLs in response to test 2 and 3, respectively. Again, it can be observed that both PLLs represent a close performance and

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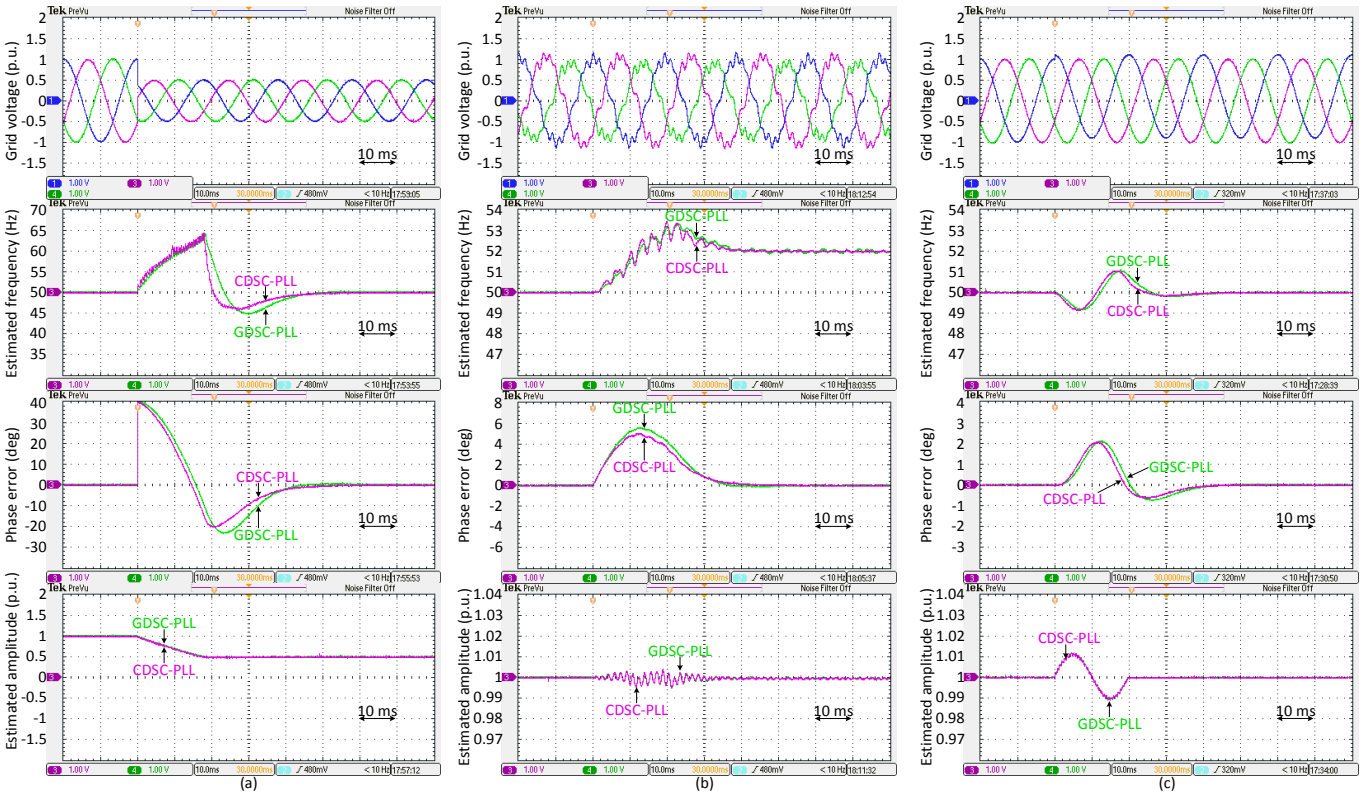

Fig. 10. Performance comparison between the CDSC-PLL and GDSC-PLL in response to (a) test 1, and (b) test 2, and (c) test 3.

effectively reject the grid voltage harmonics, unbalance, and DC offset.

In summary, there is no large performance difference between the CDSC-PLL and GDSC-PLL. The CDSC-PLL, however, demands a much lower computational effort than the GDSC-PLL. Notice that the CDSC-PLL consists of an SRF-PLL and a chain of five $\alpha\beta$DSC operators, but the GDSC-PLL structure requires two SRF-PLLs and two chains of operators. Considering this fact, the CDSC-PLL [Fig. 6(a)] is a better option than the GDSC-PLL [Fig. 8(a)].

IV. Conclusion

A research on variable-length delay-based PLLs was conducted in this paper. The focus was first on a single-phase PLL with a variable-length transfer delay-based quadrature signal generator (briefly called the VLTD-PLL). A small-signal model for this PLL was derived, which makes its tuning procedure and dynamics assessment straightforward. A performance comparison between this PLL and an advanced fixed-length transfer delay-based PLL, referred to as the ATD-PLL, was then conducted. It was proved theoretically and experimentally that the VLTD-PLL and ATD-PLL are equivalent. Considering this equivalence and the more straightforward implementation of the ATD-PLL (which is because of using a fixed-length delay) it can be concluded that the ATD-PLL is a better option than the VLTD-PLL. The research was then focused on three-phase PLLs with adaptive $\alpha\beta$DSC operators-based prefilters. Two well-known configurations of such PLLs, known to as the CDSC-PLL and GDSC-PLL, were considered and their small-signal modeling, tuning, and stability analysis were conducted. Finally, a performance comparison between them was carried out. It was shown that there is no considerable performance difference between these PLLs. Considering this fact and the lower computational burden of the CDSC-PLL, it can be concluded that the CDSC-PLL is a better option than the GDSC-PLL.

Appendix A
Model Order Reduction

The solid line in Fig. 11 illustrates the frequency response of the transfer function $H(s)$ [see (25)]. It can be observed that it has a behavior like a first-order LPF with a non-unity dc gain in the low-frequency range. Therefore, we should be able to approximate its low-frequency dynamics with such an LPF. Equation (36) describes this LPF in a general form, in which k_{dc} and τ_r are its dc gain and time constant, respectively.

$$H_r(s) = \frac{k_{dc}}{\tau_r s + 1} \tag{36}$$

In what follows, the procedure of finding the values of k_{dc} and τ_r is described.

Replacing the exponential terms in (25) by their first-order

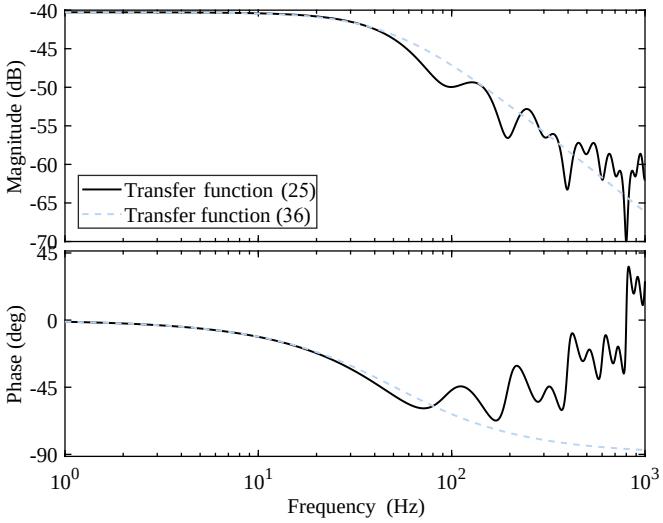

Fig. 11. Frequency response of (25) and its first-order counterpart, i.e., (36), with $k_{dc} = 31T/64$ and $\tau_r = 10T/64$.

Padé approximations yields

$$H(s) \approx \frac{T}{2}\left[\frac{1}{32} + \frac{1}{16}\frac{1}{(T/64)\,s+1} + \frac{1}{8}\frac{1}{(T/32)\,s+1}\frac{1}{(T/64)\,s+1} + \frac{1}{4}\frac{1}{(T/16)\,s+1}\frac{1}{(T/32)\,s+1}\frac{1}{(T/64)\,s+1} + \frac{1}{2}\frac{1}{(T/8)\,s+1}\frac{1}{(T/16)\,s+1}\frac{1}{(T/32)\,s+1}\frac{1}{(T/64)\,s+1}\right]. \tag{37}$$

Combining the fractions of (37) into a single fraction gives

$$H(s) \approx \frac{31T}{64}\frac{\frac{T^4}{8126464}s^4 + \frac{T^3}{32768}s^3 + \frac{5T^2}{2048}s^2 + \frac{5T}{64}s + 1}{\frac{T^4}{262144}s^4 + \frac{15T^3}{32768}s^3 + \frac{35T^2}{2048}s^2 + \frac{15T}{64}s + 1}. \tag{38}$$

The second- and higher-order terms in the numerator and denominator of (38) have very small coefficients and, therefore, barely affect the low-frequency dynamics. Consequently, they are neglected, which results in

$$H(s) \approx \frac{31T}{64}\frac{\frac{5T}{64}s + 1}{\frac{15T}{64}s + 1}. \tag{39}$$

The dc gain of (36) and (39) should be equal. It is corresponding to $k_{dc} = 31T/64$. The transfer functions (36) and (39) should also have a close phase-frequency response in the low-frequency range. Using (40) and (41), which describe the phase-frequency response of these transfer functions, it can be concluded that τ_r should be equal to $10T/64$.

$$\angle H_r(j\omega) = -\tan^{-1}(\tau_r\omega) \tag{40}$$

$$\begin{aligned}\angle H(j\omega) &\approx \tan^{-1}(5T\omega/64) - \tan^{-1}(15T\omega/64)\\ &= -\tan^{-1}\left(\frac{10T\omega/64}{1 + 75T^2\omega^2/4096}\right)\\ &\approx -\tan^{-1}(10T\omega/64)\end{aligned} \tag{41}$$

The dashed line in Fig. 11 illustrates the frequency response of (36) with $k_{dc} = 31T/64$ and $\tau_r = 10T/64$. It can be observed that (25) and (36) have a close frequency response in the low-frequency range.

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