Analog Neural Network based on Memristor Crossbar Arrays

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Abstract

In this paper, a new feed forward analog neural network is designed using a memristor based crossbar array architecture. This structure consists of positive and negative polarity connection matrices. In order to show the performance and usefulness of the proposed circuit, it is considered a sample application of iris data recognition. The proposed neural network implementation is approved by the simulation in Cadence design environment using 0.35µm CMOS technology. The results obtained are promising for the implementation of high density neural network.

1. Introduction

Many investigations on the implementation of analog neural networks field are presented in the literature [1-4]. A neural network is made up of a number of artificial neurons and a huge number of interconnections between them. A typical block-diagram of a feed-forward neural network is shown in Fig.1 [5].

The main task in realizing high efficient analog neural network is to implement the basic block which operates as a linear weighted summer. This block is also referred to as synaptic interconnection stage.

Multilayer feed forward networks, a widely used neural network architecture, require large number of synaptic interconnections (multipliers). Therefore, careful design of multiplier is critical in achieving compact silicon area, minimizing power consumption and improving input range [6-8].

On the other hand, with the discovery of the memristor (memory element) and its efficient use in crossbar arrays offering dense and regular structures [9-11], it is possible to perform multiplication and addition operations in the analog domain in a very effective way [12-14].

As is known from the literature, the memristor element has a number of advantages, such as low power consumption, non-volatile storage element, excellent scalability and integration [15]. Therefore, the fact that the memristor can be implemented as an electronic synapse in neural network applications, makes this element extremely attractive.

In this paper we discuss the realization of the feed-forward neural network using memristive crossbar. The circuit is realized in cadence design environment using the macro model of memristor. Proper operation of the neural network is illustrated using iris data as a benchmark.

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The paper is planned as follows: In section2, the dynamic model of the memristor element and its function in a crossbar array are briefly explained. Proposed neuron circuit realization with memristor crossbar array is presented in Section 3. The simulation results are given in Section 4. Finally, conclusion part is presented in Section 5.

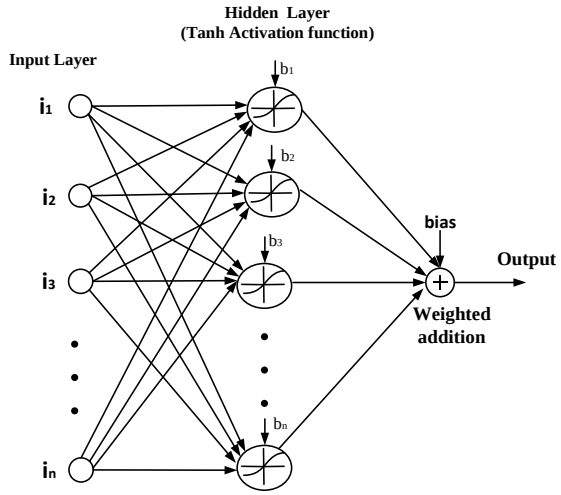


Fig.1. General structure of feed-forward neural network

2. Memristor Device

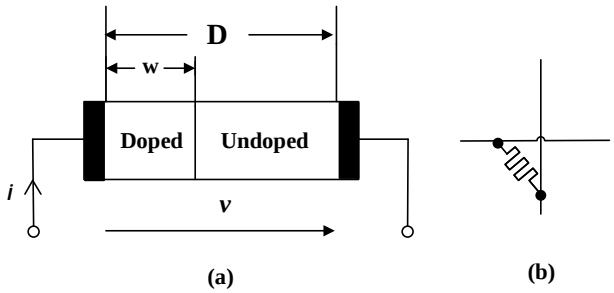


Fig.2. (a) Memristor structure, (b) Circuit notation

The memristor is the fourth fundamental element conjectured by Chua in 1971 [16]. The physical memristor device is first introduced by HP Labs 37 years after [17]. The fact that the conceptual Chua's memristor can be realized using HP Lab's nanoscale device inspired the researchers to use this element in the implementations of high density systems, such as non-volatile memory implementations and synapse realizations in neural network circuits.

The schematic and crossbar circuit symbol of the memristor is shown in Fig. 2. The element has two states, one corresponding to the closed state, where the element displays a low resistance with w ≅ D, (R_{ON}); while the other corresponds to the open state, where the element shows a high resistance (w ≅ 0), (R_{OFF}).
The total resistance R_{MEM} of the memristor can be shown by the following relation:

$$R_{MEM}(x) = R_{ON}x + R_{OFF}(1-x), \quad (1)$$

$$\text{where } x = \frac{w}{D} \ \epsilon\ (0,1) \quad (2)$$

The relationship between the current and voltage of the memristor can be defined as follows:

$$v(t) = R_{MEM}(w)i(t) \quad (3)$$

Depending on R_{ON} resistance, passing current and other factors, the speed of movement of the boundary between the doped and undoped regions can be shown as follows:

$$\frac{dx}{dt} = k\, i(t) f(x), \qquad k = \frac{\mu_v R_{ON}}{D^2} \quad (4)$$

where μ_v is called as dopant mobility and the value of μ_v is approximately is 10^{-14} $m^2 s^{-1} V^{-1}$.
Figure.3 shows device schematic and crossbar circuit notation of a memristor. This circuit can be used to effectively realize the synaptic weights of neural networks. The conductance of each memristor represents a weight. Since memristor is an element with memory, the use of the memristive crossbar adds dynamical characteristics to the synaptic weights. Beside this, the availability of the nanoscale devices allows the implementation of the neural network very effectively in a very small physical area.
Analog input values are represented by symmetrical current or voltage pulses and outputs are obtained as voltage pulses. Thanks to this future, many of the basic arithmetic operation such as summing and multiplication can be realized very effectively in a single step [18].

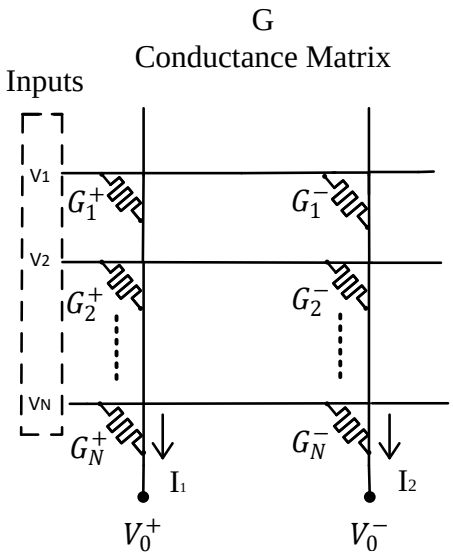


Fig.3. The principle of analog vector-matrix multiplication with memristor array [19].

As it can be seen clearly from Fig.3, the vector multiplication can be naturally processed by directly utilizing the Kirchoff's law. Through Kirchhoff's laws, the applied voltages, V_i are multiplied by the conductances G_i^+ and G_i^- to give output voltages:

$$V_0^+ - V_0^- = \sum \frac{V_i(G_i^+ - G_i^-)}{G_0} \quad (5)$$

where $G_0 = G_1^+ + G_2^+ \ldots G_N^+ = G_1^- + G_2^- \ldots G_N^-$

3. Proposed Neuron Circuit Realization with Memristor Crossbar Array

In this work, the design of neural network using memristor crossbar arrays is presented. In this way, a new memristor-based architecture is realized which suits well high density circuit implementation thanks to the nanoscale realization of memristors. As it can be seeen from the Fig. 4, neural network consists of one hidden layer with tanh type nonlinearity and one linear output neuron.

The MOS transistor at the input layer realize tanh type activation functions as shown in Fig1. The output neuron is a simple linear perceptron, that is why, we use two voltage dividers in order to scale down the signal levels applied to the inputs of the output transistors which ensures the linear operation of these transistors. In addition to, the proposed circuit occupies small area on chip which is very important advantage from IC realization point of view.

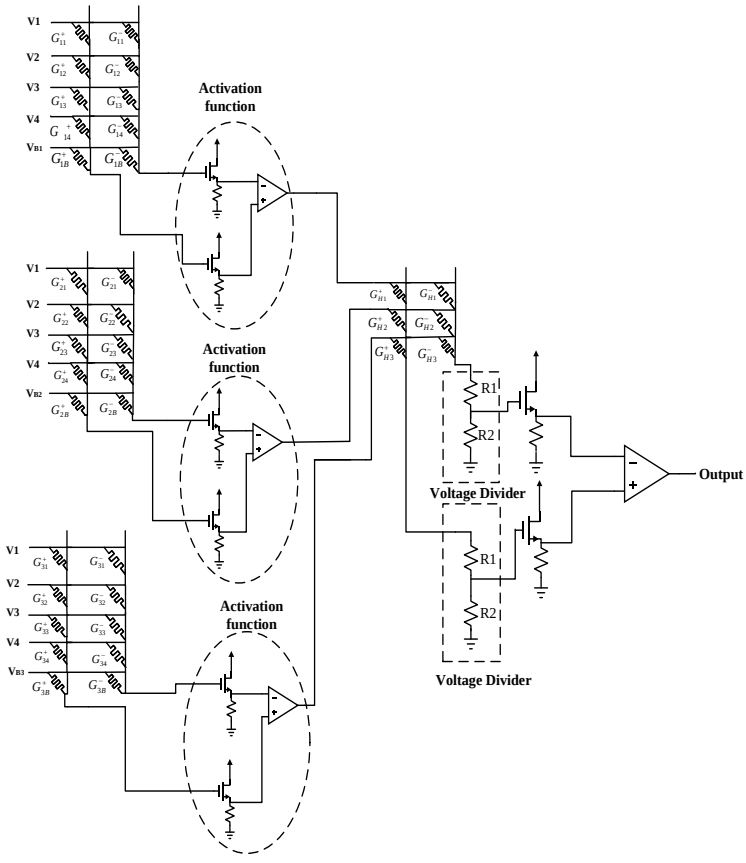


Fig.4. Circuit diagram of the proposed neural network.

In the simulation of the proposed neural network (Fig.4), the equivalent circuit shown in Fig.5 is used for each memristor element.

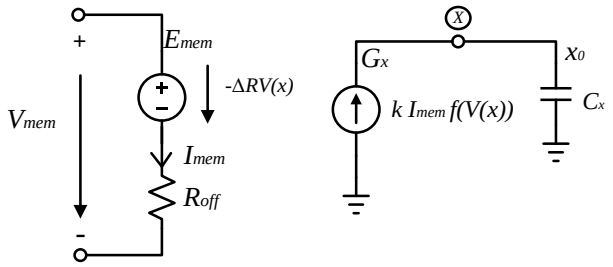


Fig.5. Structure of the SPICE model [20]

The equation shown in (eq.1) can be rearranged as follows:

$$R_{MEM}(x) = R_{OFF} - x\Delta R, \;\; \Delta R = R_{OFF} - R_{ON} \tag{6}$$

In this model, the initial width of the doped region is modeled by the initial voltage of the capacitor. This initial voltage can be given in terms of the physical quantities as follows:

$$x_0 = \frac{R_{OFF} - R_{INIT}}{\Delta R} \tag{7}$$

4. Simulation Results

In order to verify the feasibility of the proposed neural network with memristive crossbar synapsis, we simulated the proposed circuit in Cadence design environment using 0.35um CMOS technology. The circuit is biased at ±1V. Baluns are realized using differential pair [21]. In order to realize the memristors in the crossbar, we use the model of Biolek [20]. The memristive weights are obtained by training the network using iris data which is conventionally used in the literature as a benchmark. The parameters of the memristors in neural network in Fig.4 are trained using backpropagation algorithm set-up on MATLAB environment and these parameters are inserted to the Cadence netlist. The input signals are applied as a pulse with a 10% duty cycle. The amplitude of the pulses is set according to the iris data.

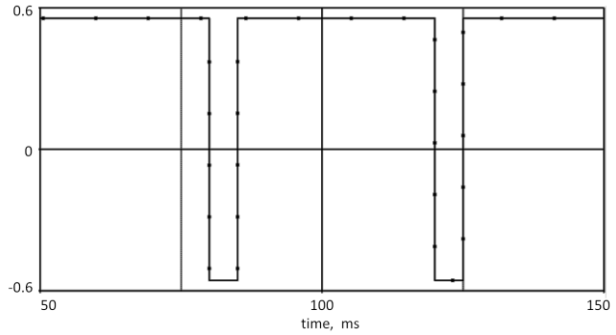
As it can be seen from Fig.4, there are three memristor crossbar arrays in the input layer and one crossbar array in the output layer.

The waveform of a typical input signal applied to the neural network is given in Fig. 6a. The amplitude of this pulse signal is set to the scaled data corresponding to the sampled iris flower. The signal in Fig. 6a is the first input of the sample shown in Table. 1.

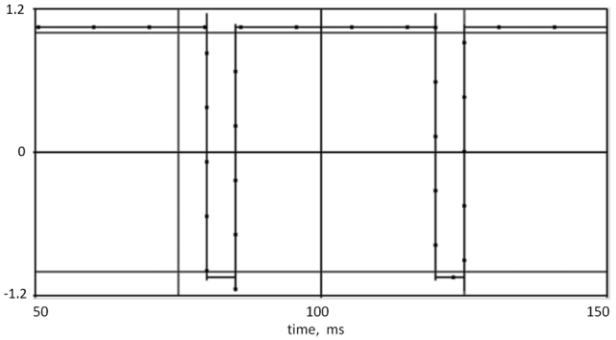
In order to train the circuit, we have extracted mathematical model of the circuit, that is all memristors are modelled by the differential equation in Eqs. (1-4). The subcircuits consisting of MOS transistors and Baluns (used for converting from differential signal to the single ended signal) are modelled with tanh function. The overall system model thus obtained is inserted to the Simulink Matlab and trained based on iris flower data set [22] using back propagation algorithm.

Table.1 The simulation results of the neural network for three sample inputs.

	V_{i1}	V_{i2}	V_{i3}	V_{i4}	$V_{0,\,ideal}$	V_0
Sample1	-0.556	0.250	-0.864	-0.917	-1.048	-1.13
Sample2	-0.111	-0.167	0.390	0.417	0.727	0.8
Sample3	0.333	-0.083	0.559	0.917	1.07	1.1



(a)



(b)

Fig.6 a) Typical signal shown for V_{i1}=-0.556 V applied to neural network input b) The corresponding output signal (V_{out}=-1.13 V)

5. Conclusions

In this paper, the design of analog neural network with memristor crossbar arrays is considered. The required activation functions are realized using sub-circuits consisting of Baluns and CMOS transistors. Iris data recognition application is used to test the performance of the proposed neural network. For this purpose, the back propagation algorithm is used in MATLAB environment and then obtained parameters are used in Cadence netlist. Thus, the performance of the proposed circuit is verified for the application of the iris data recognition.

6. References

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