creative commons
COMMONS DEED

저작자표시-비영리-변경금지 2.0 대한민국

이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:

저작자표시. 귀하는 원저작자를 표시하여야 합니다.

비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.

변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 이용허락규약(Legal Code)을 이해하기 쉽게 요약한 것입니다.

Disclaimer

dCollection

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Doctoral Thesis

Self-Calibrated, Low-Jitter and Low-Reference-Spur Injection-Locked Clock Multipliers

Seyeon Yoo

Department of Electrical Engineering

Graduate School of UNIST

2020

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Self-Calibrated, Low-Jitter and Low-Reference Spur Injection-Locked Clock Multipliers

Seyeon Yoo

Department of Electrical Engineering

Graduate School of UNIST

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Self-Calibrated, Low-Jitter and Low-Reference Spur Injection-Locked Clock Multiplier

A thesis/dissertation
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Seyeon Yoo

12/04/2019

Approved by

Advisor
Kyuho Lee

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Self-Calibrated, Low-Jitter and Low-Reference Spur Injection-Locked Clock Multiplier

Seyeon Yoo

This certifies that the thesis/dissertation of Seyeon Yoo is approved.

12/04/2019

Advisor: Professor Kyuho Lee

Thesis Committee Member: Professor Jaehyouk Choi

Thesis Committee Member: Professor Seong-Jin Kim

Thesis Committee Member: Professor Kyung Rok Kim

Thesis Committee Member: Professor Hyun Jong Yang

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Abstract

This dissertation focuses primarily on the design of calibrators for the injection-locked clock multiplier (ILCM). ILCMs have advantage to achieve an excellent jitter performance at low cost, in terms of area and power consumption. The wide loop bandwidth (BW) of the injection technique could reject the noise of voltage-controlled oscillator (VCO), making it thus suitable for the rejection of poor noise of a ring-VCO and a high frequency *LC*-VCO. However, it is difficult to use without calibrators because of its sensitiveness in process-voltage-temperature (PVT) variations. In Chapter 2, conventional frequency calibrators are introduced and discussed. This dissertation introduces two types of calibrators for low-power high-frequency *LC*-VCO-based ILFMs in Chapter 3 and Chapter 4 and high-performance ring-VCO-based ILCM in Chapter 5.

First, Chapter 3 presents a low power and compact area LC-tank-based frequency multiplier. In the proposed architecture, the input signals have a pulsed waveform that involves many high-order harmonics. Using an LC-tank that amplifies only the target harmonic component, while suppressing others, the output signal at the target frequency can be obtained. Since the core current flows for a very short duration, due to the pulsed input signals, the average power consumption can be dramatically reduced. Effective removal of spurious tones due to the damping of the signal is achieved using a limiting amplifier. In this work, a prototype frequency tripler using the proposed architecture was designed in a 65 nm CMOS process. The power consumption was 950 μW, and the active area was 0.08 mm^2. At a 3.12 GHz frequency, the phase noise degradation with respect to the theoretical bound was less than 0.5 dB.

Second, Chapter 4 presents an ultra-low-phase-noise ILFM for millimeter wave (mm-wave) fifth-generation (5G) transceivers. Using an ultra-low-power frequency-tracking loop (FTL), the proposed ILFM is able to correct the frequency drifts of the quadrature voltage-controlled oscillator of the ILFM in a real-time fashion. Since the FTL is monitoring the averages of phase deviations rather than detecting or sampling the instantaneous values, it requires only 600μW to continue to calibrate the ILFM that generates an mm-wave signal with an output frequency from 27 to 30 GHz. The proposed ILFM was fabricated in a 65-nm CMOS process. The 10-MHz phase noise of the 29.25-GHz output signal was −129.7 dBc/Hz, and its variations across temperatures and supply voltages were less than 2 dB. The integrated phase noise from 1 kHz to 100 MHz and the rms jitter were−39.1 dBc and 86 fs, respectively.

Third, Chapter 5 presents a low-jitter, low-reference-spur ring voltage-controlled oscillator (ring VCO)-based ILCM. Since the proposed triple-point frequency/phase/slope calibrator (TP-FPSC) can accurately remove the three root causes of the frequency errors of ILCMs (i.e., *frequency drift*, *phase*

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

offset, and *slope modulation*), the ILCM of this work is able to achieve a low-level reference spur. In addition, the calibrating loop for the *frequency drift* of the TP-FPSC offers an additional suppression to the in-band phase noise of the output signal. This capability of the TP-FPSC and the naturally wide bandwidth of the injection-locking mechanism allows the ILCM to achieve a very low RMS jitter. The ILCM was fabricated in a 65-nm CMOS technology. The measured reference spur and RMS jitter were −72 dBc and 140 fs, respectively, both of which are the best among the state-of-the-art ILCMs. The active silicon area was 0.055 mm^2, and the power consumption was 11.0 mW.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Contents

ABSTRACT V

CONTENTS VII

LIST OF FIGURES IX

LIST OF TABLES XII

Chapter 1. Introduction 1

1.1. Motivation 1

1.2. Dissertation Organization 3

Chapter 2. Prior ILCMs with Real-Time Frequency Calibration 4

2.1. ILCMs with a PLL-Based Frequency Calibrator 4

2.2. ILCMs with a Frequency Calibrator Using a Replica-VCO or a Replica-Cell-Based Delay Line. 5

2.3. ILCMs with a Period-Detector-Based Calibrator 7

2.4. ILCMs with a Frequency Calibrator Detecting Phase Shift 9

2.4.1. Phase-Shift Detector Using a TDC 10

2.4.2. Phase-Shift Detector Using a Pulse Gating Technique 11

2.4.3. Phase-Shift Detector Using Delay Cells 12

Chapter 3. An Ultra-Low Power and Compact LC-Tank-Based Frequency Tripler 13

3.1. Motivation 13

3.2. Circuit Designs 15

3.3. Measurement Results 18

3.4. Discussion 21

Chapter 4. A Low-IPN mm-Wave Injection-Locked Frequency Multiplier for 5G 22

4.1. Motivation 22

4.2. Limits of Prior Frequency-Tracking-Loop Architectures for mm-Wave ILFMs 25

4.3. Proposed ILFM With an Ultra-Low-Power FTL Using the Averages of the Phase Deviations 30

4.3.1. Overall Architecture 30

4.3.2. V-to-I Amplifier and the QVCO 33

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

4.3.3. Quadrature Generator, the Pulse Generator, and the Switched *RC*-filters 35
4.3.4. Coarse Frequency Selector....36
4.4. Analysis of Phase Noise and Static Frequency Offset....38
4.4.1. Phase Noise of the Proposed ILFM....38
4.4.2. Static Frequency Offset by Mismatch Effects in the FTL....42
4.5. Experimental Results....44
4.6. Discussion....51

Chapter 5. A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Using a Triple-Point Background Calibrator....52
5.1. Motivation....52
5.2. Analysis on Frequency Error Generation Mechanisms of Root Causes and Limits of Conventional Calibrators....55
5.2.1. Three Root Causes of Frequency Errors and Limits of Conventional Calibrators....55
5.2.2. How Slope Modulation Generates Phase Error and thus Frequency Error...60
5.3. ILCM Using the Proposed Background TP-FPSC....63
5.3.1. Overall Architecture of the ILCM with the Background TP-FPSC....63
5.3.2. Three Error Detection Mechanisms of the TP-FPSC....65
5.3.3. Settling Behaviors of Three Calibrations of the TP-FPSC....68
5.4. Design of Sub-Building Blocks: Slope Controller, VCO, and VCDL....69
5.5. Experimental Results....71
5.6. Discussion....78

Chapter 6. Conclusion....79

REFERENCES....81

ACKNOWLEDGMENTS....89

PUBLICATIONS....90

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

List of Figures

Figure 1.1. (a) phase realignment mechanism of the injection locking technique (b) reference spur over f_{ERR}'s 2
Figure 2.1. ILCM with a conventional PLL-based frequency calibrator. 4
Figure 2.2. ILCM with a frequency calibrator using a replica-VCO or a replica-cell-based delay line. 5
Figure 2.3. (a) ILCM with a period-detector-based calibrator. (b) Timing diagram. 7
Figure 2.4. (a) ILCM with a TDC-based frequency calibrator. (b) Timing diagram. 10
Figure 2.5. (a) ILCM with a pulse gating frequency calibrator. (b) Timing diagram. 11
Figure 2.6. (a) ILCM with a frequency calibrator using delay cells. (b) Timing diagram. 12
Figure 3.1. Frequency triplers: (a) conventional self-mixing architecture [35] (b) proposed architecture 14
Figure 3.2. Overall architecture of the proposed *LC*-based frequency multiplier using a pulsed input signal 15
Figure 3.3. Waveforms of the output of the proposed architecture with a different *Q* from (1) and simulations 16
Figure 3.4. Reference spurs at the outputs of the *LC*-resonator and the D-to-S amplifier, ($V_O+ - V_O–$) and V_{OUT}, respectively 17
Figure 3.5. Chip micrograph of the proposed frequency tripler 18
Figure 3.6. Measured spectrum of the 3.12 GHz output signal of the proposed frequency tripler 18
Figure 3.7. Measured and simulated reference spur level with respect to the input reference clock frequency 19
Figure 3.8. Measured phase noise of the 3.12 GHz output signal and the 1.04 GHz reference clock. . 19
Figure 4.1. LO generation with a gigahertz-range PLL and a cascaded mm-wave ILFM for multi-band and multi-standard cellular communications. 23
Figure 4.2. (a) Lock range f_L(%) and maximum deviation of the free-running frequency f_{DEV}(%) over temperature of an *LC*-VCO injected by a 2.25-GHz tone, when the target harmonic factor *N* is changed. (b) Degradations of the10-MHz phase noise with respect to f_{DEV} for different *N*'s 26
Figure 4.3. ILFMs with different FTLs using (a) a replica-VCO; (b) a TDC; (c) a mixer; (d) an envelope detector. 29
Figure 4.4. (a) Conceptual diagram of the cascaded architecture of an mm-wave LO generator. (b) Principle of the proposed frequency-tracking loop (FTL). 30
Figure 4.5. Proposed mm-wave ILFM with the ultra-low power FTL. (a) Overall architecture. (b) Conceptual timing diagram. 32
Figure 4.6. Schematics of (a) V-to-I amplifier and (b) QVCO 34
Figure 4.7. (a) Schematics of the CFS. (b) Conceptual timing diagram of the CFS. 36

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Figure 4.8. Noise model of the proposed mm-wave ILFM. 38
Figure 4.9. NTFs of building blocks based on (5) – (9). (b) Estimated phase noise from the noise model. 40
Figure 4.10. Linear model of static frequency offset due to mismatch effect of FTL. 42
Figure 4.11. (a) Die photograph. (b) Power-breakdown table. 44
Figure 4.12. Measured spectrum and phase noise of the output signal with 29.25 GHz (f_{INJ} = 2.25 GHz, N = 13) with estimated phase noise from the noise model in Section 4.4. 45
Figure 4.13. Measured spectrum and phase noise of the output signal with 30.0 GHz (f_{INJ} = 2.0 GHz, N = 15). 46
Figure 4.14. Measured phase noise at the frequency of 9.75 GHz (29.25 GHz /3) over (a) temperatures and (b) supply-voltages, when the FTL was on or off. 48
Figure 4.15. Measured phase noise at f_{DIV3} across (a) temperatures for five different chips and (b) output frequencies from 27.4 to 30.8 GHz (f_{INJ} changed with a fixed N of 13). 49
Figure 5.1 Level of reference spur with respect to f_{ERR}. 53
Figure 5.2. Three causes of the frequency error in ILCMs. 55
Figure 5.3. (a) First cause of f_{ERR} in ILCMs, i.e., *frequency drift*; (b) mechanism of the generation of f_{ERR} due to *frequency drift*. 56
Figure 5.4. (a) Second of f_{ERR}, i.e., *phase offset,* in conventional frequency calibrators; (b) mechanisms of f_{ERR} generation due to *phase offset*. 57
Figure 5.6. (a) Third causes of f_{ERR}, i.e., *slope modulation,* in conventional frequency calibrators; (b) mechanisms of f_{ERR} generation due to *slope modulation*. 58
Figure 5.5. Conventional frequency calibrators for removing f_{DF} & ϕ_{OS} based on (a) DTC; and (b) DCDL. 58
Figure 5.7. Mechanism of the *slope modulation* generating phase shift in S_{OUT} (a) five-stage ring VCO having the injection of S_{INJ}; (b) difference in slopes fades after a chain of inverters, but the phase shift remains. 60
Figure 5.8. (a) Simulated phase shifts due to the *slope modulation* assuming neither f_{DF} nor ϕ_{OS} without any calibrators; (b) simulated reference spur with a calibrator removing f_{DF} and ϕ_{OS} (red) or without any calibrators (black). 61
Figure 5.9. Overall architecture of the proposed ILCM with the triple-point frequency/phase/slope calibrator (TP-FPSC). 63
Figure 5.10. Implementation of TP-FPSC. 64
Figure 5.11. Three causes detection mechanisms of the TP-FPSC; (a) *frequency drift*, (b) *phase offset*, and (c) *slope modulation*. 66
Figure 5.12. The settling behaviors of three control voltages in the TP-FPSC. 68
Figure 5.13. Schematics of (a) slope controller, (b) VCO, and (c) VCDL. 70

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Figure 5.14. (a) Die photograph. (b) Power-breakdown table. 71
Figure 5.15. Measured spectrum of the output signal with a frequency of 2.4 GHz, when (a) TP-FPSC was turned off, (b) f_{DF} and ϕ_{OS} calibrations were turned on, but ΔSL calibration was turned off, (c) TP-FPSC was fully turned on. (d) Measured spectrum of the output signal with 2.5 GHz. 73
Figure 5.16. Variations of reference spurs over output frequencies in five different sample chips. 73
Figure 5.17. Measured phase noise, when the TP-FPSC was turned on and off at (a) 2.4 GHz and; (b) 2.5 GHz. 74
Figure 5.18. Variations of integrated RMS-jitter over output frequencies in five different sample chips. 75
Figure 5.19. Benchmark of performances of this work and state-of-the-art ring-VCO-based ILCMs. 75

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

List of Tables

Table 1. Comparison with State-of-the-Art Frequency Triplers 20
Table 2. Performance Comparison with State-of-the-Art mm-Wave ILFMs 50
Table 3 Comparison with Ring-VCO-Based ILCMs 76

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Chapter 1.

Introduction

1.1. Motivation

For modern high-speed digital systems, especially mobile applications, the demand for further improvement in the performance of the jitter of clock signals is increasing. To date, phase-locked loop (PLL)-based architectures using a *LC*-type voltage-controlled oscillator (*LC*-VCO) have been used dominantly in many applications for generating high-performance clocks, but their low level of integration has hindered the effort to lower the implementation cost. Recently, multiplying delay-locked-loop (MDLL)-based architectures [1] – [4] and a subharmonic injection-locked clock multiplier (ILCM)-based architectures [5] – [22] are considered as alternatives to conventional PLL-based architectures. Due to the phase realignment mechanism of the injection locking technique, without external loop, those architectures are able to generate precise clock signals with the excellent jitter performance. Although they use a ring-type oscillator or a high-frequency *LC*-VCO that provides poor spectral purity, the ILCM can suppress the jitter of the VCO and provides high-performance clocks. The ILCM is thus widely used in a mm-wave band for low-power multipliers and in a gigahertz-range for compact low-jitter clock multipliers.

However, an ILCM has critical problems in that excellent performance of the RMS jitter and reference spur can be maintained only when the frequencies of the free-running VCO, f_{VCO}, is sufficiently close to target harmonic of the injection signal, $N \cdot f_{REF}$, where f_{REF} is the frequency of the reference clock and N is the target harmonic index. In general, the amount of the possible frequency drifts of the VCO due to process-voltage-temperature (PVT) variations is much larger than the lock range of the injection. If the frequency drift is out of the locking range, the ILCM will fail in the lock acquisition [5]. For an ILCM to stay within the lock range, f_{VCO} can be adjusted to be close to $N \cdot f_{REF}$. Nonetheless, ILCMs still suffer from the high level of reference spur, caused by the periodic phase-shift (or deterministic jitter) of the VCO, as shown in Fig. 1.1(a), when it is injection-locked. This is because the level of the reference spur sharply increases as f_{VCO} deviates from $N \cdot f_{REF}$, i.e., $\text{Spur}_{\text{dBc}} \approx 20\log(N \cdot |f_{ERR}|)$ where $f_{ERR} = (f_{VCO} - N \cdot f_{REF})/(N \cdot f_{REF})$ [6]. Fig. 1.1(b) shows, when N is 10, as α increases to just 0.1%, the spur-level rises exponentially by 20 dB and reaches −40 dBc. Consequently, to minimize not only phase noise, but also the reference spur in ILCMs, they need to be required to have

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

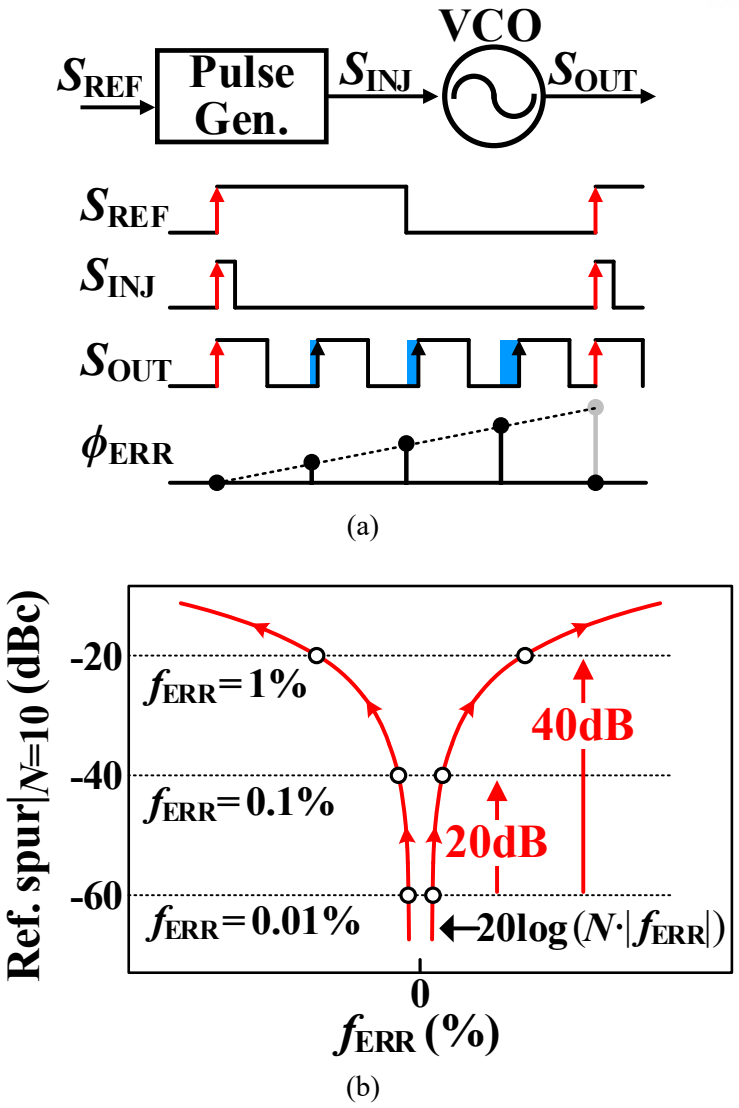


Figure 1.1. (a) phase realignment mechanism of the injection locking technique (b) reference spur over f_{ERR}'s

a very precise frequency calibrator.

In this dissertation, we propose two designs of frequency calibrators. First, we present an ultra-low-power frequency calibrator for mm-wave ILCMs. Despite the high frequency, the proposed frequency calibrator can correct the drifts of f_{VCO} and requires low power without the use of high-frequency circuits. It was the first calibrator to calibrate real-time drifts of f_{VCO} in mm-wave band with ultra-low power consumption of less than 1mW. Second, we present a high-performance versatile calibrator. This versatile calibrator can remove three major causes of f_{ERR}s, especially calibrating the slope modulation for the first time which is caused by the injection. Thanks to this calibrator, the ILCM achieved the lowest reference spur, while using a small area and little power.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

1.2. Dissertation Organization

This dissertation focuses primarily on calibration techniques for ILCMs to generate low-jitter and low-reference-spur signals using a compact silicon area and low power. We introduce the calibration techniques in mm-wave band. Also, we analyze all causes of the frequency error that interfere with the accurate frequency calibration and degrade the performance of the ILCMs. This dissertation is organized as follows:

Chapter 2 introduces and discuss conventional frequency calibrators for ILCMs. The advantages and disadvantages of each structure is explained.

Chapter 3 presents a design of a low-power and compact open-loop ILFM. In this work, due to the pulsed input signals, the core current flows for a very short duration and the average power consumption can be dramatically reduced. In Chapter 3, design consideration on an LC tank of the multiplier and a differential-to-single amplifier are analyzed. We present the measurement results from a prototype chip fabricated in 65-nm CMOS technology.

In Chapter 4, a PVT-robust, low-PN mm-wave band ILFM with an ultra-low-power frequency calibrator is presented. The reason why the frequency drifts of the VCO are critical in mm-wave bands is discussed. Using the noise model of the proposed ILFM, the noise contribution of each building blocks is analyzed. The static frequency offset due to mismatches along the signal paths of the calibrator is also analyzed. The implementation of this work is then explained, and we present the measurement results of a prototype chip fabricated in 65-nm CMOS technology.

Chapter 5 presents a low-rms-jitter and low-reference-spur ring-VCO-based ILCM using a background triple-point frequency/phase/slope calibrator (TP-FPSC). The three causes of frequency errors and the limits of conventional calibrators are discussed. The reference spur caused by *slope modulation* was simulated and analyzed. The architecture and mechanism of the proposed TP-FPSC is explained. Finally, we describe the implementation of the calibrator and the VCO, and we present the measurements results from a prototype chip fabricated in 65-nm CMOS technology.

Finally, Chapter 6 summarizes the proposed works and concludes this dissertation.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Chapter 2.

Prior ILCMs with Real-Time Frequency Calibration

2.1. ILCMs with a PLL-Based Frequency Calibrator

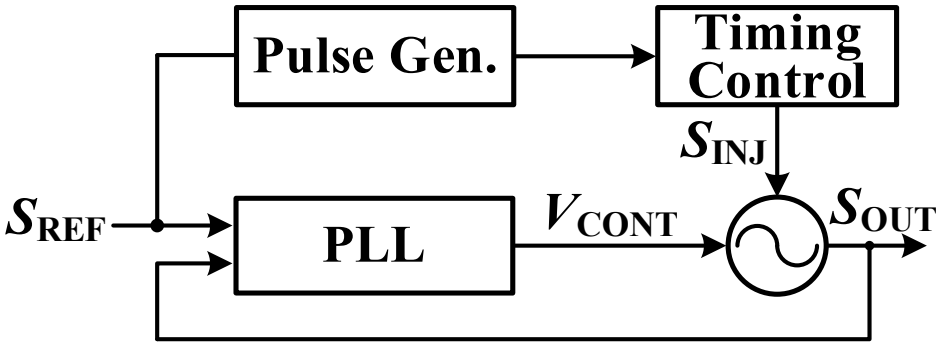


Figure 2.1. ILCM with a conventional PLL-based frequency calibrator.

To date, the most popular method to calibrate the free-running frequency of the VCO is to use the phase-locked loops (PLL). There have thus been some attempts to use the PLL-based frequency calibrator in ILCMs, as shown in Fig. 2.1 [7], [8], [12], [13], [23]. However, these structures have a serious problem with the frequency error, f_{ERR}, detection. In the conventional PLLs, when f_{ERR} exists, the phase error is accumulated over the N cycles of the VCO signal and this accumulated phase error is detected by the phase detector (PD). However, in the ILCM, the rising edge of S_{OUT} is realigned by that of S_{REF}, so this phase error of the VCO is periodically reset to zero by S_{INJ} before the PLL detects it. as shown in Fig. 1.1(a). Therefore, the PLL-based calibrator is not suitable for the real-time frequency calibration. Even if it could detect the phase error, it is not efficient due to poor detection gain. Although it cannot well prevent the real-time f_{ERR} of the VCO due to temperature or voltage variations, it can correct static f_{ERR} due to process variations. Therefore, PLL is mainly used to bring f_{VCO} into the lock range of the injection locking at the initial stage or start-up stage before the VCO is injection-locked.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

2.2. ILCMs with a Frequency Calibrator Using a Replica-VCO or a Replica-Cell-Based Delay Line.

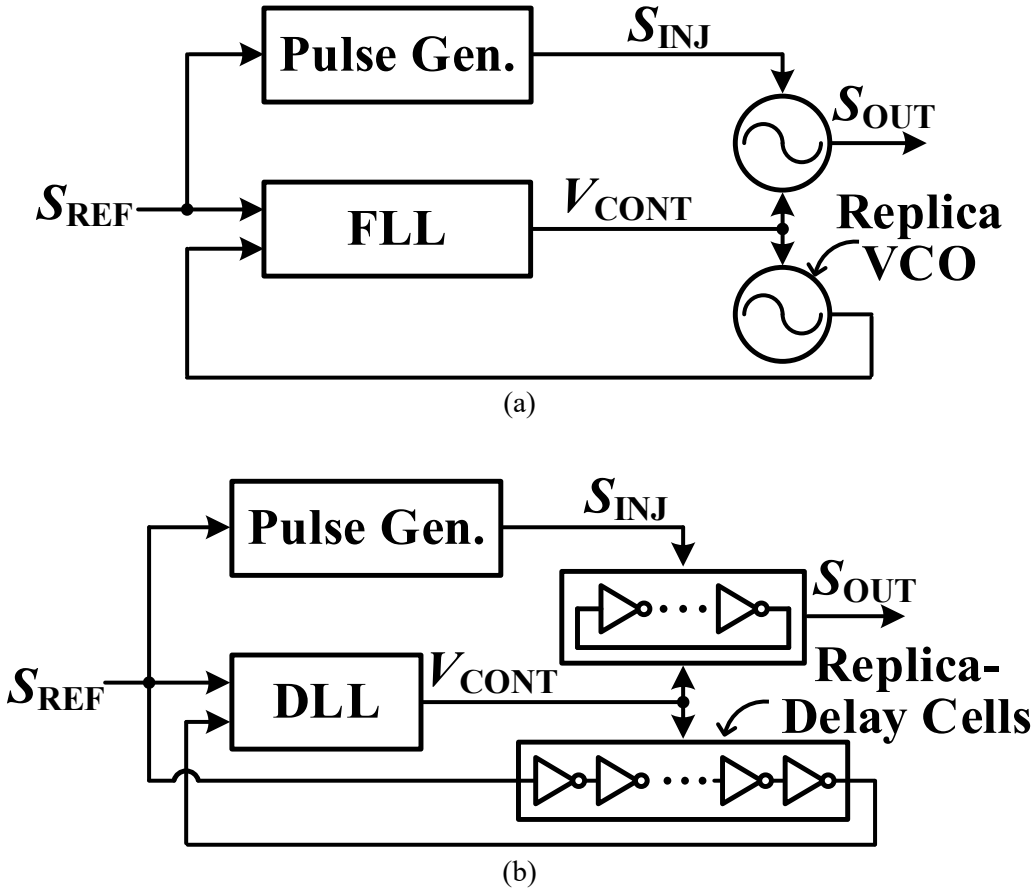


Figure 2.2. ILCM with a frequency calibrator using a replica-VCO or a replica-cell-based delay line.

To detect the real-time frequency drifts of the VCO due to temperature or voltage variations without the effect of injection, a replica-VCO [16] – [20] or a replica-cell-based delay line [24], [25] can be used, as shown in Fig. 2.2. Since the replica-VCO or the replica-delay cells are equally affected by voltage or temperature variations with the main-VCO in the ILCM, the free-running frequency of the main-VCO can be easily detected by monitoring the frequency of the replica-VCO or the delay of the replica-cell-based delay line. The PLL or DLL can bring frequency of the replica-VCO or delay of the replica-cell-based delay line to the target frequency and share the same control-voltage, V_{CONT}, to correct the main-VCO's frequency.

These structures have three serious problems. First, the replica-VCO or this delay line are supposed to spend the same power consumption as the main-VCO. Second, mismatches between the main-VCO and replica-VCO limit the accuracy of the calibration and degrades the jitter performance and the level

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

of the reference spur in the ILCM. Third, the noise of the replica-VCO and main-VCO are uncorrelated to each other; this frequency calibrator thus cannot suppress the noise of the main-VCO. Rather, shared control-voltage, V_{CONT}, brings the noise of the replica-VCO into the in-band noise of the output signal in the ILCM. In conclusion, this structure suffers from the issues that the VCO consumes twice the power, while doubling the noise of the VCO.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

2.3. ILCMs with a Period-Detector-Based Calibrator

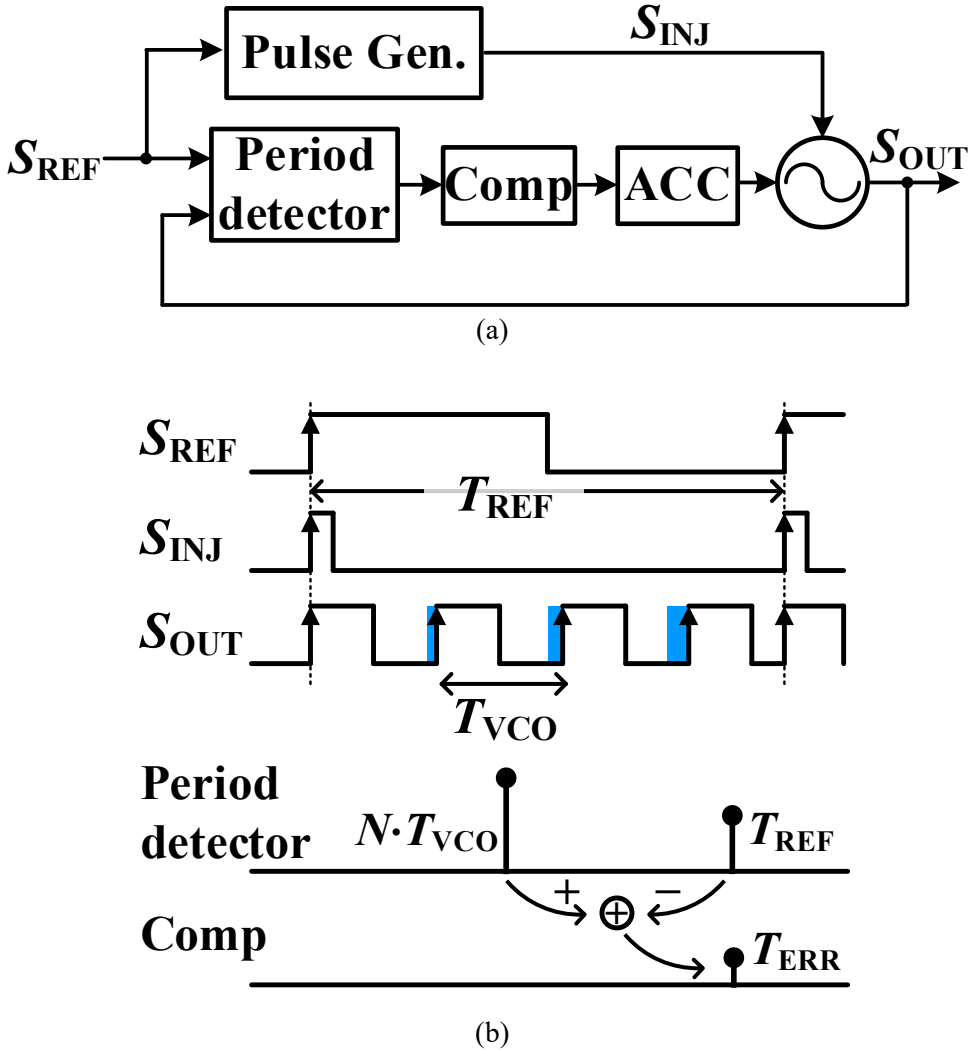


Figure 2.3. (a) ILCM with a period-detector-based calibrator. (b) Timing diagram.

The main reason why it is difficult to detect f_{ERR} in ILCM is that the phase error is reset to zero every reference period. However, during the intervals in which injection pulses are not injected, S_{OUT} preserves the information of the VCO's free-running period, T_{VCO}. By comparing N-times T_{VCO} to the period of S_{REF}, T_{REF}, f_{ERR} can be detected. Fig. 2.3 shows a period-detector-based calibrator to monitor T_{VCO} without the effect of the injection [26]. As shown in Fig. 2.3(b), the period detector measures the period of $N \cdot T_{VCO}$ and T_{REF} using the charge pump or TDC. Then, the comparator detects the error period, T_{ERR} and passes this error to the accumulator. By accumulating T_{ERR}, these structures can correct f_{ERR} of the injection locked VCO.

These structures have two issues. First, measuring the period is very vulnerable to noise because the

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

detector must be turned on for a long time. To measure the period of the VCO precisely, the noise of the period detector should be lower than that of the VCO. If not, according to the noise transfer function, the noise of the detector degrades in-band noise of the ILCM. To lower the noise, the detector must use more power than the VCO during measuring periods. Second, since T_{ERR} is very small compared to T_{REF}, the detection gain of the frequency error is small. For example, the charge-pump-based period detector always have a constant voltage value corresponding to T_{REF}. However, the voltage value corresponding to T_{ERR} is small compared to the constant voltage value. To get a high detection gain, the current in the charge pump needs to be increased, which is difficult because of the voltage headroom. This small detection gain makes these structures more susceptible to the noise of the loop components.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

2.4. ILCMs with a Frequency Calibrator Detecting Phase Shift

As shown in Fig. 1.1, when f_{ERR} exists, the phase is shifted in proportion to f_{ERR} by S_{INJ}. It would be nice if this phase shift, $\Delta\phi_{shift}$, could be detected simply, but as mentioned in Chapter 1, it is difficult to do so due to the phase reset. To overcome this issue, recently, there have been many efforts to develop new architectures for the frequency calibration [6], [27] – [31], which use the time-to-digital converter (TDC) [6], pulse-gating technique [27], [28], or delay cells [29] – [31] to detect $\Delta\phi_{shift}$.

Phase-shift-detector-based calibrators have two general advantages. First, the in-band VCO noise at low frequency offset such as flicker noise can be further suppressed. As the gate length of the transistor gets smaller and flicker noise worsens, this noise reduction effect is very efficient for producing low-jitter clocks. Second, the detection gain of the frequency error and phase error is large, since the phase shift includes error information accumulated during N VCO cycles. This large detection gain reduces the noise contribution of the loop components at S_{OUT}, thus reducing the power consumption of the calibrator. However, these architectures still contain disadvantages, which are discussed in this subsection.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

2.4.1. Phase-Shift Detector Using a TDC

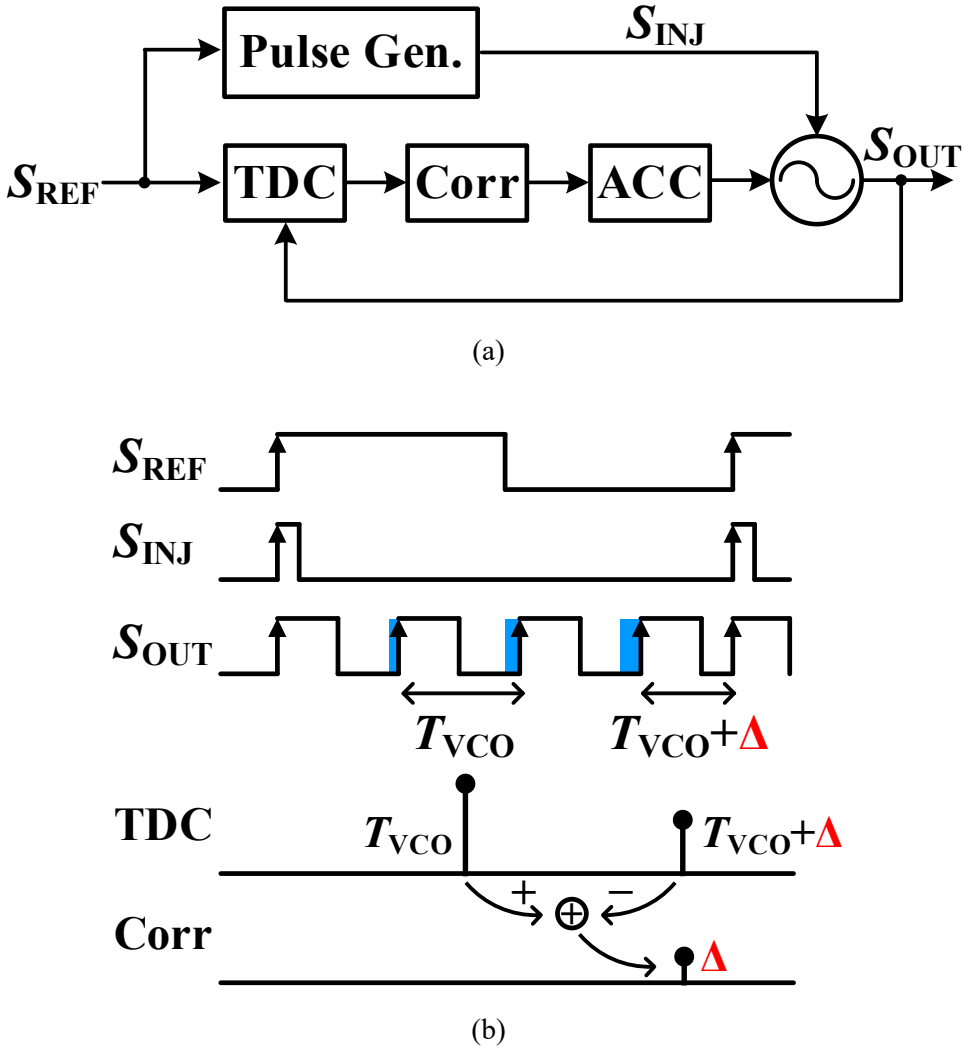


Figure 2.4. (a) ILCM with a TDC-based frequency calibrator. (b) Timing diagram.

Fig. 2.4 shows a frequency calibrator that used a TDC to detect f_{ERR} [6]. As shown in Fig. 2.4(b), the TDC measures free-running period of the VCO, T_{VCO}, and the injection-altered period, $T_{VCO} + \Delta$. The correlator compares T_{VCO} to $T_{VCO} + \Delta$ and generates the error signal Δ. By accumulating Δ, this calibrator can detect real-time f_{ERR}.

These structures have two issues. First, to measure the period of the VCO, the TDC has to be turned on for a long time and becomes vulnerable to noise of the TDC. Second, there is a trade-off between the resolution and the power consumption in the TDC. In conclusion, since this phase-shift-detector requires a lot of power to lower the noise of the TDC and increase the resolution of the TDC, it did not achieve good figure of merit (FoM) considering the noise performance and power consumption.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

2.4.2. Phase-Shift Detector Using a Pulse Gating Technique

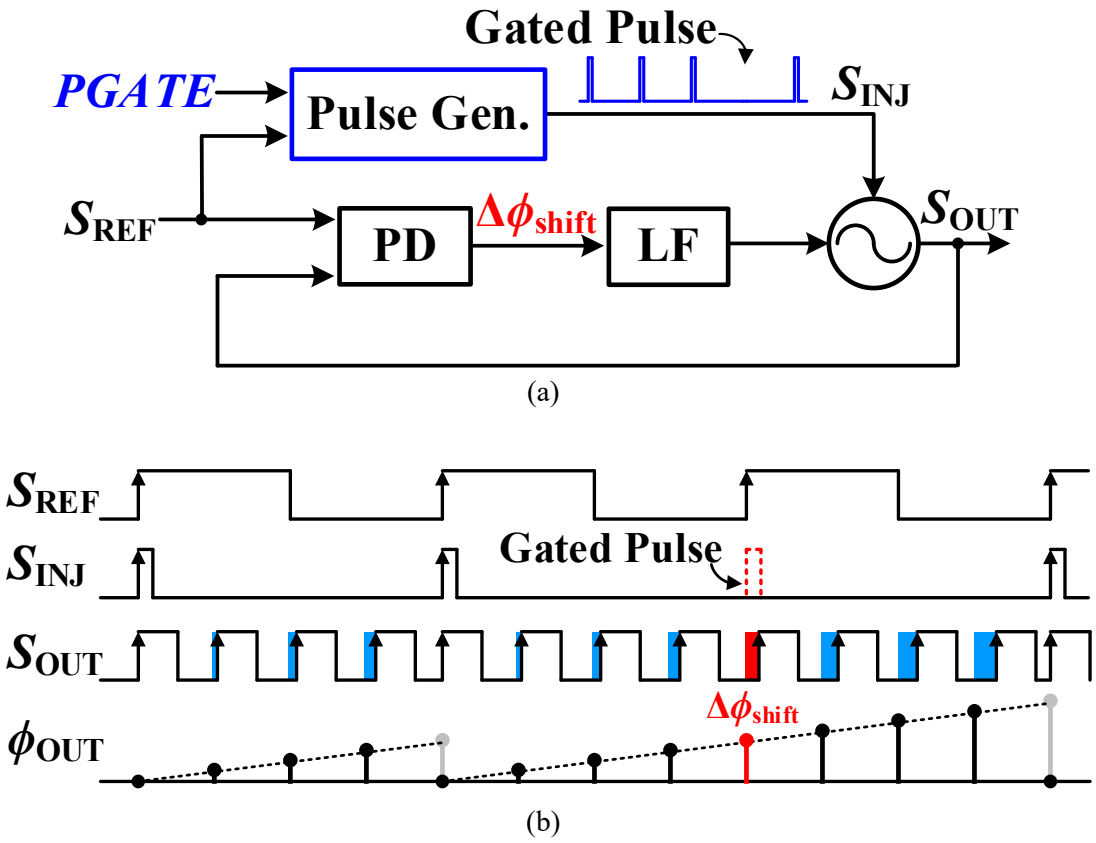


Figure 2.5. (a) ILCM with a pulse gating frequency calibrator. (b) Timing diagram.

Fig. 2.5 shows a frequency calibrator using a pulse gating technique to detect f_{ERR} [27], [28]. As shown in Fig. 2.5(a), the pulse generator generates an injection pulse signal from rising edge of S_{REF} depending on a gating signal, *PGATE*. In Fig. 2.5(b), we see how this calibrator detects the phase shift, $\Delta\phi_{shift}$, using the gated pulse signal. When the injection pulse is gated, the accumulated phase error of the VCO is not realigned and preserves the phase error, and the PD can thereby detect $\Delta\phi_{shift}$ and frequency error.

These structures have two problems. First, the VCO's noise reduction effect due to calibrator is decreased because the calibration is possible only when the injection pulse is gated, not every time. Since the bandwidth of the f_{ERR} and phase error calibration is slow, this calibrator does not effectively remove flicker noise of the VCO. However, frequently gating the injection pulse to widen the bandwidth of the calibration, the effect of the injection will be reduced, and the overall noise also may worsen. Second, the periodical gating of injection could generate in-band spurs, which degrade the noise performance of the ILCM.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

2.4.3. Phase-Shift Detector Using Delay Cells

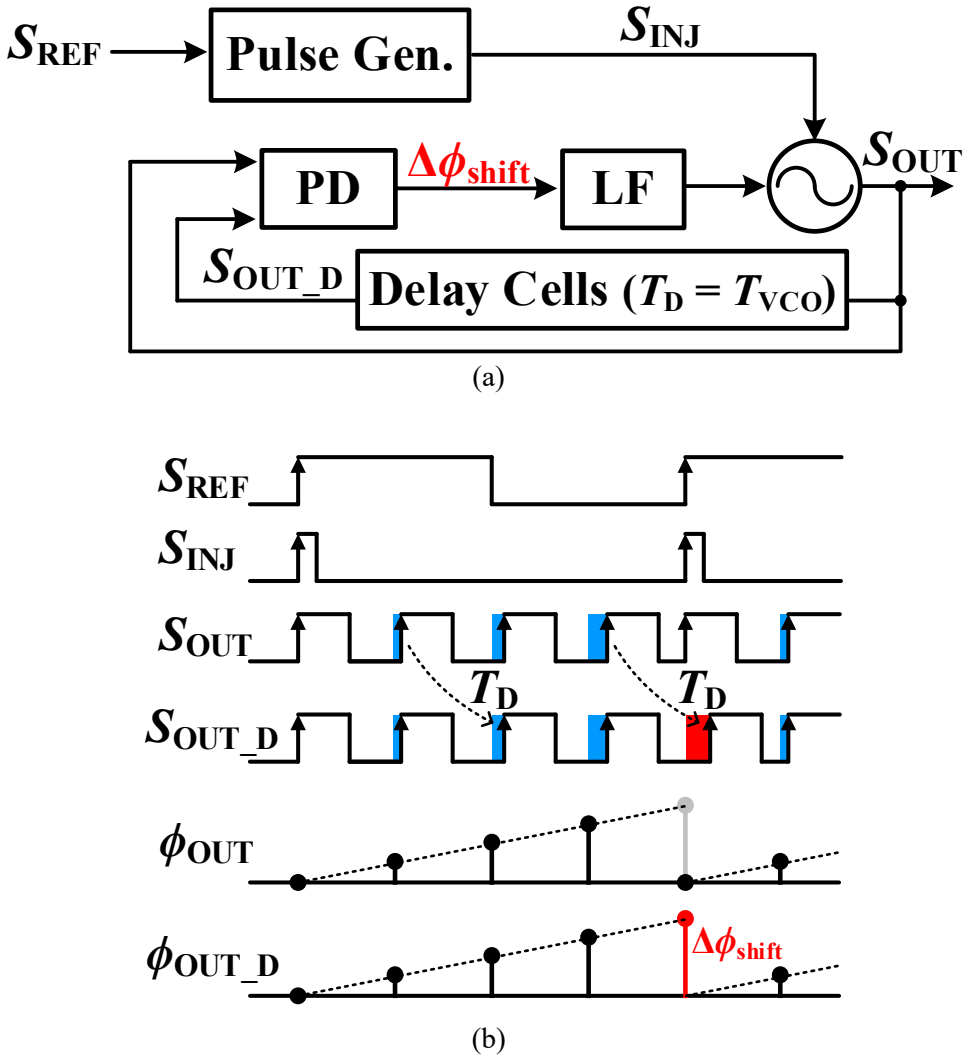


Figure 2.6. (a) ILCM with a frequency calibrator using delay cells. (b) Timing diagram.

Fig. 2.6 shows a frequency calibrator using delay cells to detect f_{ERR} [29] – [31]. As shown in Fig. 2.6(a), the delay cells delay S_{OUT} by the free-running period of the VCO, T_{VCO}, and generate a delayed signal of S_{OUT}, S_{OUT_D}. As shown in Fig. 2.6(b), since the delay cells receive and delay the signal of the VCO before injection, they can preserve the intrinsic phase information of the VCO without the effect of the injection. Then, the PD compares the phase difference between S_{OUT} and S_{OUT_D}, and $\Delta\phi_{shift}$ can be detected. Since this method can detect f_{ERR} with the simple structure, it requires low power and small silicon area. In addition, the calibrator can detect $\Delta\phi_{shift}$ at each reference period, so the bandwidth of the frequency calibration can be wide enough to suppress the flicker noise of the VCO. However, the accuracy of the $\Delta\phi_{shift}$ detection could be degraded by the delay error of delay cells and the input offset of the PD, so the additional offset calibration is crucial.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Chapter 3.

An Ultra-Low Power and Compact LC-Tank-Based Frequency Tripler

3.1. Motivation

Generating a low phase noise, high frequency signal is one of the most important tasks in designing a modern electronic system. Especially for mobile applications, low-cost implementation, in terms of power consumption and silicon area, must be the primary goal. An open-loop frequency tripler is a good candidate for meeting these design goals without the need for the loop-building blocks of a phase-locked loop (PLL) or a delay-locked loop (DLL)-based architecture. To date, many frequency triplers have been reported [32] – [35]. References [32], [33] presented architectures that use a current-reused subharmonic mixer, but they must have input signals with four quadrature-phases. In the architectures of [34], [35], shown in Fig. 3.1(a), the signal at the second order harmonic frequency was extracted by the shunt-peaking inductor, and it was mixed with the original signal. However, they included multiple area-hungry inductors. Furthermore, [32] – [35] are unsuitable for low-power applications since the transistors in mixers must keep consuming static power due to their sinusoidal inputs.

In this work, we propose a new ultra-low power and compact open-loop frequency multiplier, as shown in Fig. 3.1(b). In the proposed architecture, input signals have a pulsed waveform with a narrow pulse width that includes many high-order harmonics of the reference frequency, f_{REF}. When the resonant frequency of the *LC*-tank, f_{LC}, is tuned close to a specific harmonic, the signal component at that harmonic frequency is amplified, while other components are filtered out. Thus, by changing f_{LC} any different multiplication factors, *N*s, can be obtained. The use of an *LC*-tank as a load to select the target harmonic was presented in frequency doublers [36], [37]. However, as they used differential sinusoidal inputs, only the second harmonic component was available for amplification; moreover, no odd-order harmonics could be present at all. In addition, in the proposed architecture, due to the pulsed input signals that briefly turn on the input transistors, the core current flows for a very short duration. Thus, the average power consumption can be dramatically reduced. The proposed architecture also has

* © 2016 IEEE. Part of this chapter is reprinted, with permission, from S. Yoo, S. Choi, T. Seong, and J. Choi, "An Ultra-Low Power and Compact *LC*-Tank-Based Frequency Tripler Using Pulsed Input Signals," in *IEEE Microwave and Wireless Components Letters* (MWCL), vol. 26, no. 2, pp. 140-142, February 2016.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

small silicon area, since it includes only one inductor. In this work, a prototype frequency tripler was designed in a 65 nm CMOS technology. Depending on the selection of f_{LC}, the proposed architecture can be implemented as a frequency multiplier with an arbitrary multiplication factor.

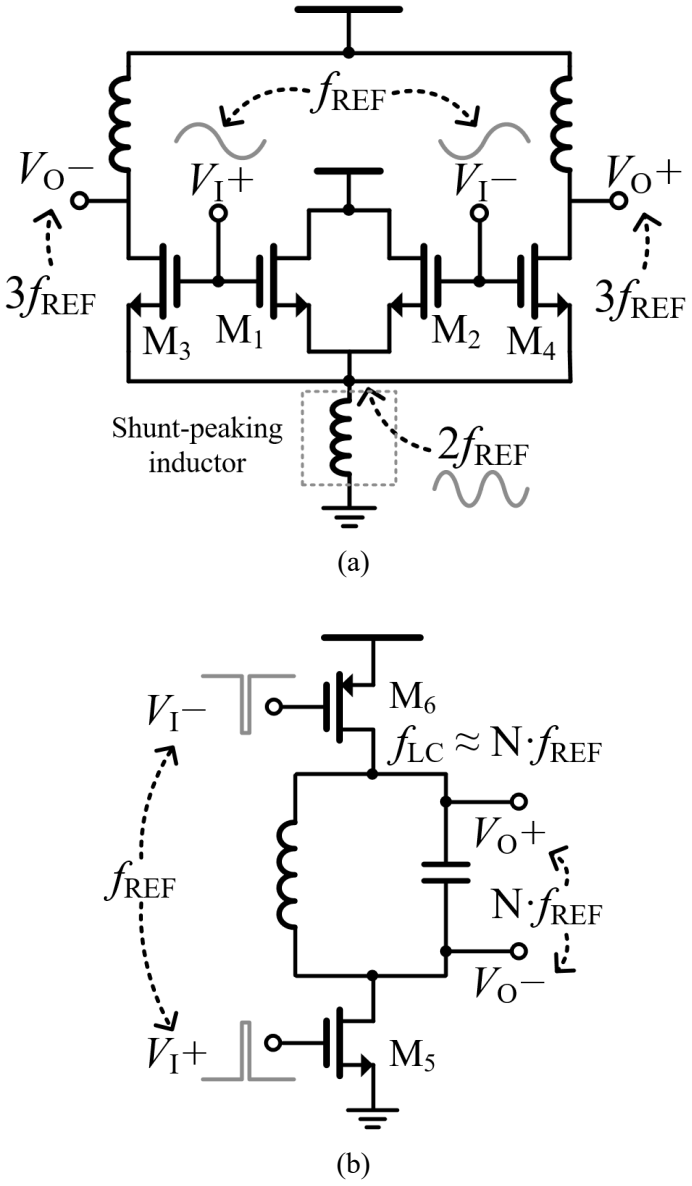
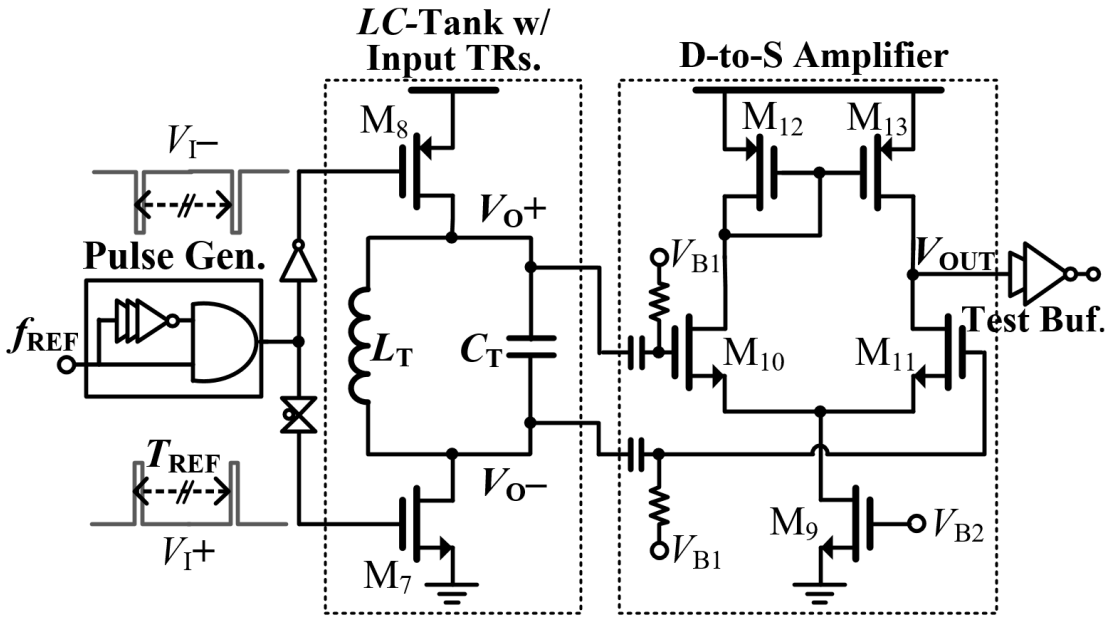


Figure 3.1. Frequency triplers: (a) conventional self-mixing architecture [35] (b) proposed architecture

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

3.2. Circuit Designs



(b)

Figure 3.2. Overall architecture of the proposed *LC*-based frequency multiplier using a pulsed input signal

Fig. 3.2 shows the overall architecture of the proposed frequency multiplier, consisting of a pulse generator, an *LC*-tank with the input transistors, M_7 and M_8, and a differential-to-single (D-to-S) amplifier. The mechanism of the proposed architecture can be easily understood in the time domain as follows. From the reference clock, the pulse generator produces narrow differential pulses, which continue to turn on and off M_7 and M_8. When M_7 and M_8 are turned on briefly by the pulsed input signals in every reference period, the *LC*-tank receives energy differentially through the closed paths from the supply and the ground. When M_7 and M_8 are turned off, the commuting current in the *LC*-tank generates the output signals. If the loss of the tank were ideally zero, this signal would be sustained permanently. However, due to the finite parallel resistance of the *LC*-tank and the leakages of M_7 and M_8, the amplitude of the signal decays. Thus, to prevent the amplitude of the signal from being diminished, the C_T of the tank must be periodically recharged. The decay of the differential magnitude of the output voltages, ($V_O+ - V_O-$), can be estimated from the impulse response of the *LC*-tank, $h(t)$, as

$$h(t) = \frac{1}{C_T} \cdot \exp\left(-\frac{\pi f_{LC}}{Q} \cdot t\right) \cdot \left[\cos\left(\pi\sqrt{4 - 1/Q^2} \cdot f_{LC} \cdot t\right) - \frac{\sin\left(\pi\sqrt{4 - 1/Q^2} \cdot f_{LC} \cdot t\right)}{\sqrt{4Q^2 - 1}}\right] \quad (1)$$

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

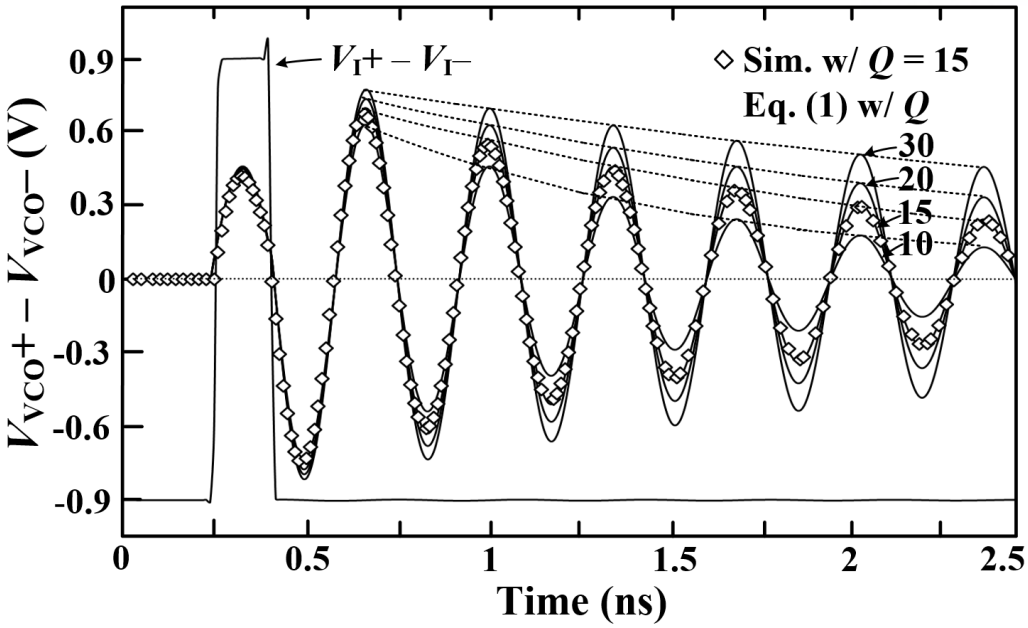


Figure 3.3. Waveforms of the output of the proposed architecture with a different Q from (1) and simulations

where Q, and f_{LC} are the loaded Q-factor and the LC-resonant frequency, respectively. Fig. 3.3 shows the waveforms of the convolution of $h(t)$ and a rectangular pulse with a pulse width of $1/2f_{LC}$ and an amplitude of 0.9 V, when the f_{LC} is 3.12 GHz and Q is varied from 10 to 30. When Q is 30, the decay of the amplitude is slow since the time constant of $h(t)$ is large, but it becomes gradually steeper as Q decreases. This is because the energy stored in the LC-tank dissipates faster as the tank loss increases. Thus, if the Q of the tank is maximized, the frequency of the recharging process can be reduced, which implies that a high multiplication number is possible. Fig. 3.3 also shows the differential output voltage, ($V_O+ - V_O-$), from the transient simulation with Q of 15, which is matched precisely to the theoretical estimation, based on (1).

In the proposed architecture, the excessive damping of the amplitude of the output signal can be prevented by a periodical recharging process. However, a significant periodic amplitude modulation (AM) is still problematic. Along with the phase modulation (PM), due to the difference between the frequencies of the LC-tank and the target harmonic of the reference clock [1], the amplitude modulation (AM) as shown in Fig. 3.3 could increase the level of the reference spur. To remove the AM component, the LC-tank is followed by the D-to-S amplifier, which amplifies V_O+ and V_O- in order to be clipped to the supply voltage [38]. Fig. 3.4 shows the level of the reference spur at the output of the resonator, ($V_O+ - V_O-$), and the D-to-S amplifier, V_{OUT}, when Q varies from 4 to 20. As shown in Fig. 3.4, the level of the spur was suppressed significantly by the D-to-S amplifier that eliminated the AM disturbance. Even if the AM disturbance can be suppressed by the D-to-S amplifier, the swings of V_O+

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

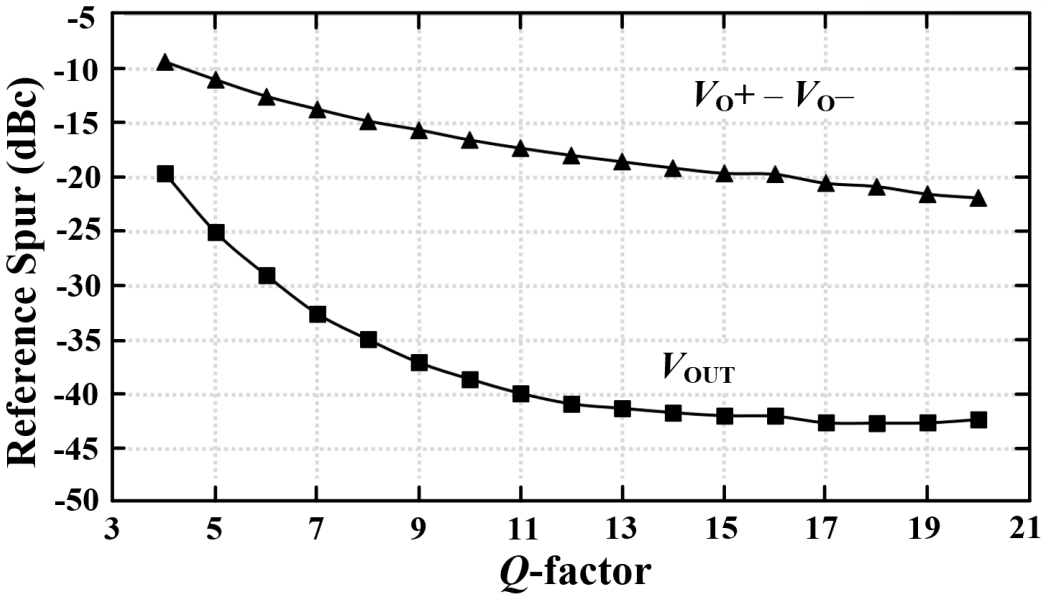


Figure 3.4. Reference spurs at the outputs of the *LC*-resonator and the D-to-S amplifier, ($V_O+ - V_O-$) and V_{OUT}, respectively

and V_O- that are too small demand that the D-to-S amplifier consume large power. As shown in Fig. 3.3, when Q is 15, a reasonable value for an on-chip *LC*-tank, the amplitude of the fourth peak is reduced to 53.3% of that of the first (or the highest) peak. To guarantee safe operation while also minimizing the power consumption of the D-to-S amplifier, we fixed the frequency multiplication number, N, at 3 in this work. However, by relaxing the power budget or the requirement for spurious tones, N can be extended to a higher value. In this work, L_T, C_T, and Q values of the tank were 2 nH, 1.4 pF, and 15 at 3 GHz, respectively. With a Q of 15, the reference spur can be minimized to less than −40 dBc, as shown in Fig. 3.4.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

3.3. Measurement Results

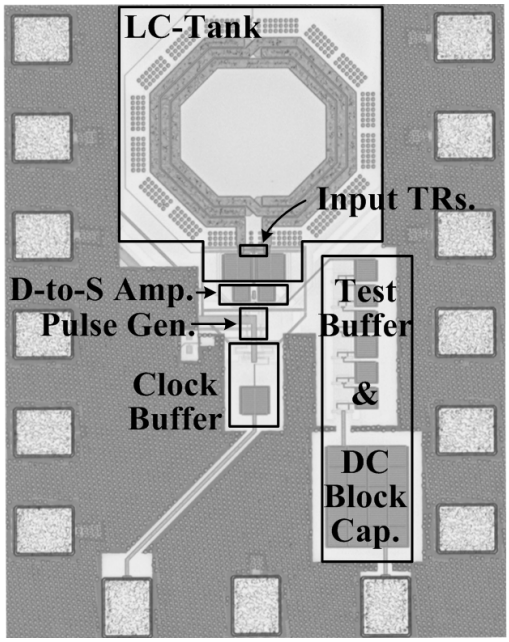


Figure 3.5. Chip micrograph of the proposed frequency tripler

The prototype frequency tripler using the proposed LC-tank-based frequency multiplier was fabricated in a TSMC 65 nm CMOS process. A test chip was mounted on a test board, and received the reference clock from a signal generator, Holzworth HS9002A. To measure output-signal performance, a spectrum analyzer, Agilent PXA N9030A, and a phase noise analyzer, Agilent E5052B, were used. In measurement, the proposed frequency tripler consumed 950μW from a 0.9-V supply voltage, where the tank core consumed only 600μW. As shown in Fig. 3.5, the frequency tripler occupied an active area of 0.08 mm^2.

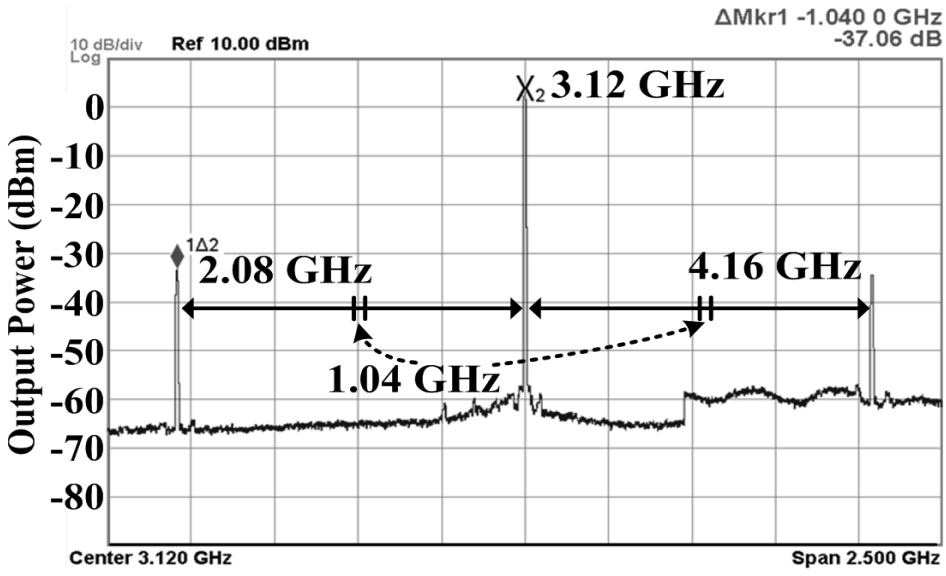


Figure 3.6. Measured spectrum of the 3.12 GHz output signal of the proposed frequency tripler

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Fig. 3.6 shows the measured spectrum of the output signal with a 3.12 GHz frequency, which is the third harmonic of the 1.04 GHz reference frequency. As shown in the spectrum in Fig. 3.6, the level of the reference spur was −37 dBc. Fig. 3.7 shows the measured and the simulated levels of the reference spur when the reference clock frequency, f_{REF}, was swept. The spur level was minimized when the third harmonic of f_{REF} was close to the resonant frequency of the *LC*-tank, but it increased as f_{REF} deviated.

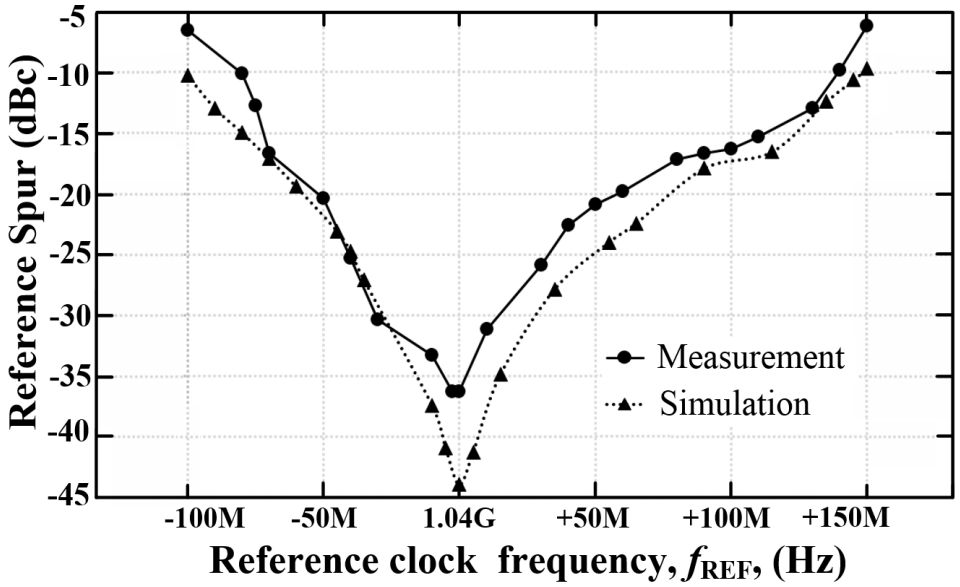


Figure 3.7. Measured and simulated reference spur level with respect to the input reference clock frequency

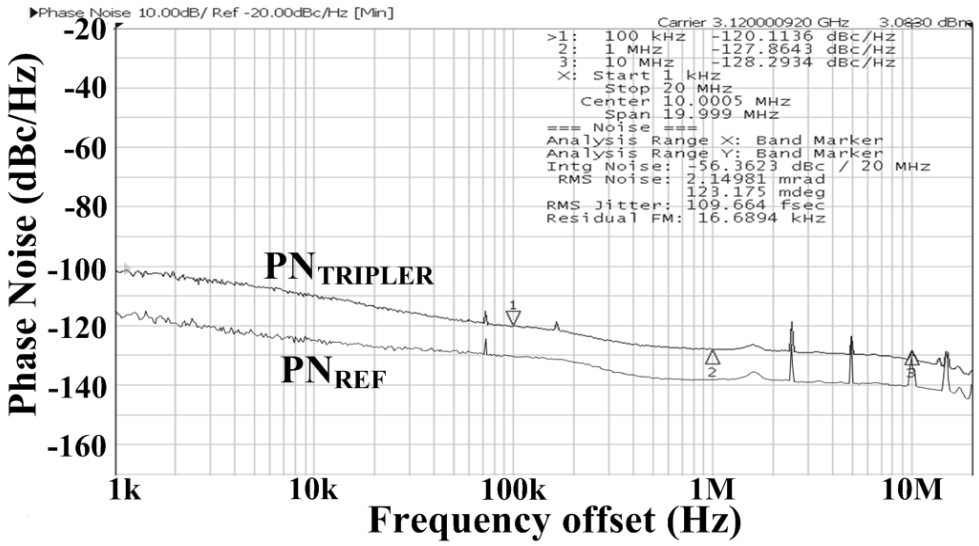


Figure 3.8. Measured phase noise of the 3.12 GHz output signal and the 1.04 GHz reference clock.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Fig. 3.8 shows the measured phase noises of the reference clock and the output signal with a 1.04 GHz and a 3.12 GHz frequency, respectively. The phase noise of the output signal at the 1MHz offset was −127.8 dBc/Hz, and the jitter, integrated from 1 kHz to 20 MHz, was 110 fs. The difference between the two phase-noise curves was very close to 9.5 dB (20·log 3dB), which is the theoretical bound. Table 1 compares the proposed work with state-of-the-art frequency triplers [32] – [35]. The proposed work had lowest power consumption, while restricting the degradation of phase noise from the theoretical boundary, PN_{DEG}, to less than 0.5 dB. In addition, the proposed frequency tripler had the smallest silicon area with one inductor.

Table 1. Comparison with State-of-the-Art Frequency Triplers

	[32]	[33]	[34]	[35]	This work
Process (CMOS)	**180 nm**	**180 nm**	**180 nm**	**180 nm**	**65 nm**
Output freq. (GHz)	**3.0**	**21.0**	**21.83**	**19.5**	**3.12**
PN_{DEG}@1MHz (dB)*	**< 0.5**	**< 0.5**	**< 1.0**	**< 0.5**	**< 0.5**
Ref. spur (dBc)	**−26**	**−16**	**−18**	**−29**	**−37**
P_{DC} (mW)	**68**	**7.5**	**8.1**	**18.8**	**0.95**
Active area (mm^2)	**0.42**	**0.36**	**0.39**	**0.84**	**0.08**

* PN_{DEG} @1MHz = $PN_{TRIPLER}$(1MHz) − 20·log(3) − PN_{REF}(1MHz)
** Power consumption of the frequency tripler only

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

3.4. Discussion

In this work, we proposed a low power, compact area *LC*-tank-based frequency multiplier. By using input signals with a pulsed waveform to minimize the duration of the core current flow, the proposed architecture was able to reduce power consumption dramatically. With the *LC*-tank having a resonant frequency close to the target frequency, the signal component of the target harmonic was effectively amplified while other components were suppressed. AM spurs, caused by the damping of the signal due to the tank loss, were removed using the D-to-S amplifier. The proposed frequency tripler had a low power consumption of less than 1 mW and a compact silicon area of 0.08 mm^2. It also achieved excellent phase noise performance; the deviation from the theoretical bound was less than 0.5 dB.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Chapter 4.

A Low-IPN mm-Wave Injection-Locked Frequency Multiplier for 5G

4.1. Motivation

Fifth-generation (5G) wireless systems have attracted attention as the next-generation cellular standard because they provide super-fast communication speeds. To meet the requirement of high data rates, RF transceivers for the 5G standard must satisfy an extremely low error vector magnitude (EVM) specification over a very wide bandwidth in a millimeter wave (mm-wave) frequency band. From this demand, one of the fundamental challenges in the design of a 5G transceiver is to generate an ultra-low-phase-noise local oscillator (LO) signal to suppress integrated phase noise (IPN) over a wide bandwidth. For example, to satisfy the EVM requirements of high-order modulations, such as 16 quadrature amplitude modulation (QAM) and 64 QAM, the IPN of an LO signal should be reduced to less than −30 dB at mm-wave frequencies [39] – [42]. Moreover, LO-signal generators also must provide quadrature signals with a very small I/Q mismatch.

The most straightforward architecture that can be used to generate the required LO signals is a high-frequency phase-locked loop (PLL) that directly generates mm-wave signals [43] – [47]. However, this architecture is not such a good solution in terms of its power consumption and phase noise. First, to synthesize a high-frequency signal in mm-wave bands, the PLL must involve power-hungry frequency dividers that operate at the target frequencies. Using typical CMOS technologies, it is difficult to design a frequency divider that operates at a high frequency, such as more than 30 GHz. Even if the design itself were possible, it would require a great amount of power to suppress the elevation of a noise floor. Second, also with respect to phase noise, a PLL that directly generates mm-wave signals is not an effective solution. According to [48], when the phase noises of recent CMOS PLLs with different output frequencies are normalized, the PLLs that have output frequencies around 3–5 GHz have much better performance with respect to phase noise than PLLs that have output frequencies greater than 10 GHz.

* © 2018 IEEE. Part of this chapter is reprinted, with permission, from S. Yoo, S. Choi, J. Kim, H. Yoon, Y. Lee, and J. Choi, “Low-Integrated-Phase-Noise 27–30-GHz Injection-Locked Frequency Multiplier With an Ultra-Low-Power Frequency-Tracking Loop for mm-Wave-Band 5G Transceivers,” in *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 375-388, February 2018.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

One of the major reasons why this occurs is that the *LC*-tank of a voltage-controlled oscillator (VCO) does not have a sufficiently high quality factor (*Q*-factor) at mm-wave frequencies. This degradation of the overall *Q*-factor is mainly because of the significant decrease in the *Q*-factor of capacitive components in the *LC*-tank, caused at high frequencies [49], [50]. As above, if we consider power consumption and phase noise, it is obvious that a more efficient way to generate an mm-wave-band LO

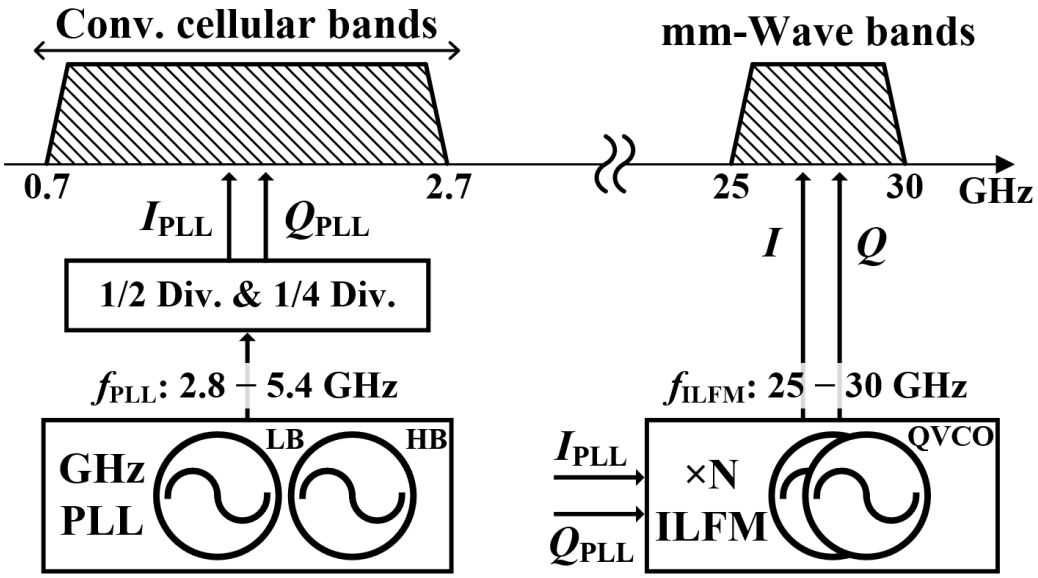


Figure 4.1. LO generation with a gigahertz-range PLL and a cascaded mm-wave ILFM for multi-band and multi-standard cellular communications.

signal is to obtain an output frequency in the range of 3–5 GHz from a PLL and increase it to a higher frequency using a low-noise frequency multiplier.

Fig. 4.1 shows the architecture proposed to generate LO signals for multi-standard, multi-band cellular transceivers. The proposed LO generator consists of a gigahertz-range PLL, an mm-wave-band, quadrature, and injection-locked frequency multiplier (ILFM). Since a gigahertz-range PLL can generate an output signal with a good phase-noise performance, if the following ILFM multiplies the frequency of the signal without degrading the noise performance, the proposed LO generator must be able to achieve sufficiently low IPN that satisfies the stringent requirement of the 5G standard. Another important advantage of the proposed architecture is that it can support the backward compatibility. Fig. 4.1 shows that a gigahertz-range PLL can be used to support conventional cellular frequency bands, i.e., 0.7–2.7 GHz [51], [52], when they are designed to have output frequencies between 2.8 and 5.4 GHz.

The key building block of the proposed multi-standard LO generator in Fig. 4.1 is a low-phase-noise mm-wave-band quadrature ILFM. However, the inherent design challenge of an ILFM is the

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

vulnerability of its operation and phase noise to process–voltage–temperature (PVT) variations [28], [29], [53], [54]. The normal operation of an ILFM with a low phase noise is available only when the free-running frequency of the VCO f_{VCO} is sufficiently close to the target frequency $N{\cdot}f_{INJ}$ where N and f_{INJ} are the multiplication factor and the injection frequency, respectively. In other words, the deviation of f_{VCO} from $N{\cdot}f_{INJ}$, f_{DEV}, should be kept small with respect to the lock range of the ILFM f_L. The vulnerability is more problematic for an mm-wave ILFM, where f_L is the typically restricted to less than 3% of f_{VCO} [55] – [57]. To alleviate this problem, the mm-wave ILFM in [58] uses a technique to extend the lock range, but it involves increases in power consumption and design complexity. In recent years, there have been many efforts to design frequency-tracking loop (FTL) architectures [15], [17], [19], [20], [25], [56], [57] that continue to adjust f_{VCO} so that it remains close to $N{\cdot}f_{INJ}$ in a real-time fashion. However, these architectures still have practical problems, so they are inadequate for use for an mm-wave ILFM that must provide extremely low phase noise. The prior FTL architectures and their problems are discussed in Section 4.2. To multiply frequencies into an mm-wave band, the cascaded PLL in [59] uses a sub-sampling PLL (SSPLL) instead of an ILFM. However, the SSPLL requires a large amount of power due to the use of a sample-and-hold phase detector and a voltage-to-current converter, which operates at the frequency of the precedent PLL, i.e., around 7 GHz.

In this work, we present an mm-wave-band ILFM that can continue to provide ultra-low-phase-noise quadrature output signals, irrespective of PVT variations [60]. By monitoring the distortions between the output phases of the injection-locked quadrature VCO (QVCO) of the ILFM that are caused when f_{VCO} deviates from the target frequency, the proposed FTL can correct the drifts of f_{VCO} and continuously suppress phase noise without the loss of the injection lock. The FTL monitors the averages of the phase deviations rather than detecting or sampling the instantaneous values, so it only operates at a very low frequency. Since it does not use any high-frequency circuits, the FTL should have ultra-low-power consumption.

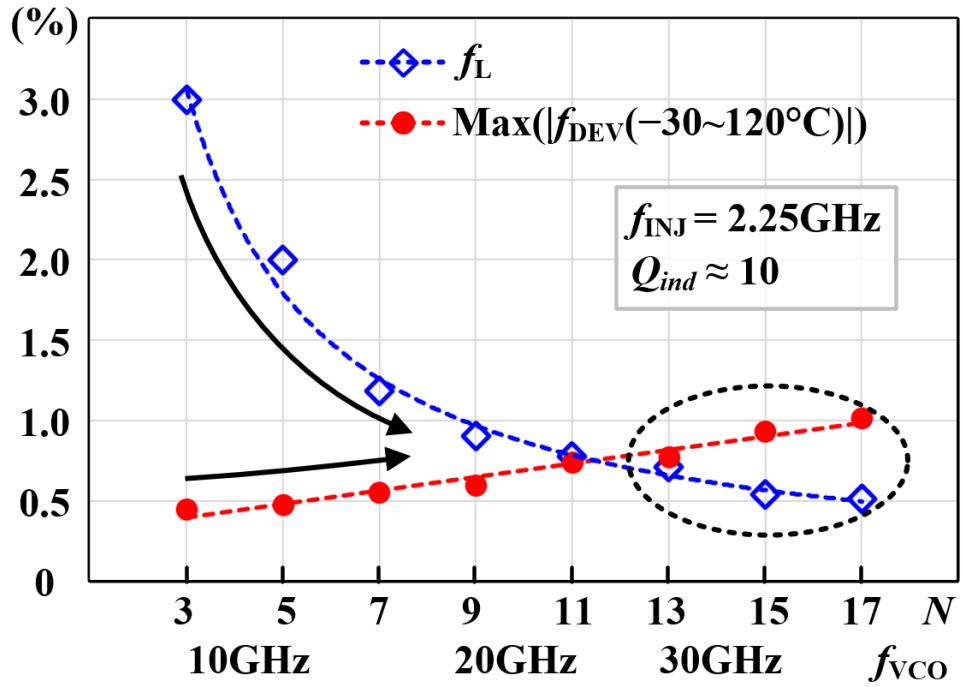
The rest of this Chapter is organized as follows. Section 4.2 shows why the drifts of f_{VCO} are critical in mm-wave bands and presents the limits of prior FTLs. In Section 4.3, the concept and the design of the proposed FTL and ILFM are presented. Section 4.4 describes the analysis of the phase noise and the static frequency offset due to the mismatches along the signal paths of the FTL. Experimental results and conclusions are presented in Sections 4.5 and 4.6, respectively.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

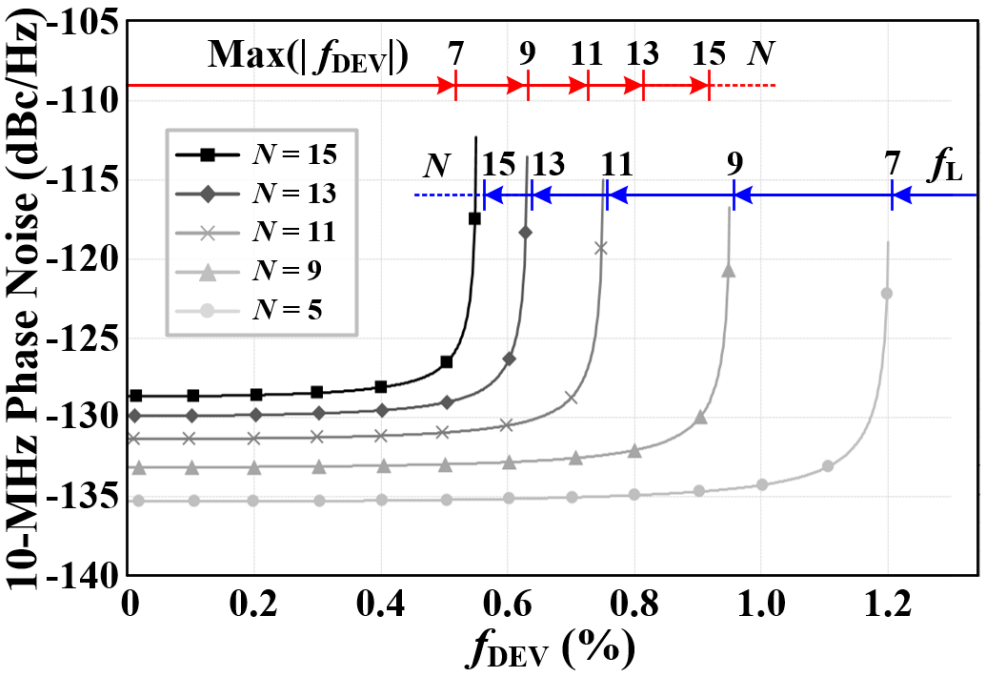
4.2. Limits of Prior Frequency-Tracking-Loop Architectures for mm-Wave ILFMs

As aforementioned, the degradation of the phase noise of an ILFM due to PVT variations becomes more severe as f_{VCO} increases. Fig. 4.2(a) shows the results of the simulation of the maximum f_{DEV}(%) of a free-running *LC*-VCO according to frequency drifts due to temperature variations. It also shows f_L(%) of the same VCO, when a 2.25-GHz signal is injected. According to N from 3 to 17, the inductance of the *LC*-tank was scaled to maintain the same *Q*-factor (Q_{ind}) despite the change in f_{VCO}. Fig. 4.2(a) shows the maximum f_{DEV} for the temperature range of −30 °C to 120 °C increases gradually as N increases. This is due to the increase in the contribution of the PVT-sensitive parasitic capacitances of the core transistors when f_{VCO} is defined. Contrary to the increase in f_{DEV}, f_L continues to decrease as N increases. This is because the effective current of the injection signal's Nth harmonic component decreases with respect to the VCO's current, thereby reducing the strength of the injection [61], [62]. Consequently, the increase in f_{DEV} along with the decrease in f_L for a larger N makes the performance of an ILFM more vulnerable to environmental variations. Fig. 4.2(b) shows the changes of the 10-MHz phase noise with respect to f_{DEV} for different N's. The noise data were obtained from the same VCOs and the injection signal used in Fig. 4.2(a), and the graphs were plotted by MATLAB using the equation of the theoretical phase noise of an ILFM in [63]. As shown in Fig. 4.2(b), when f_{DEV} is relatively small with respect to f_L, the level of the phase noise approaches the theoretical minimum boundary, i.e., $20 \cdot \log N$ above the phase noise of the injection signal. However, as f_{DEV} approaches f_L due to drifts of f_{VCO}, the phase noise is degraded significantly, and, finally, the lock is released. This problem becomes more severe as N increases, i.e., a possible f_{DEV} increases even greater than f_L, when N is more than 13. Thus, to ensure the robust operation with a low phase noise irrespective of environmental variations, an mm-wave ILFM must be equipped with a dedicated FTL that can continue to correct the frequency of the VCO during real-time frequency drifts.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(a)



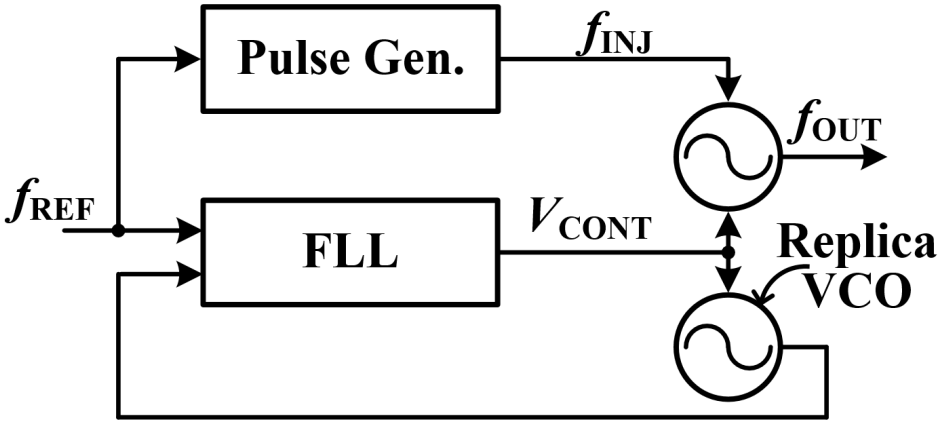
(b)

Figure 4.2. (a) Lock range f_L(%) and maximum deviation of the free-running frequency f_{DEV}(%) over temperature of an *LC*-VCO injected by a 2.25-GHz tone, when the target harmonic factor *N* is changed. (b) Degradations of the10-MHz phase noise with respect to f_{DEV} for different *N*'s.

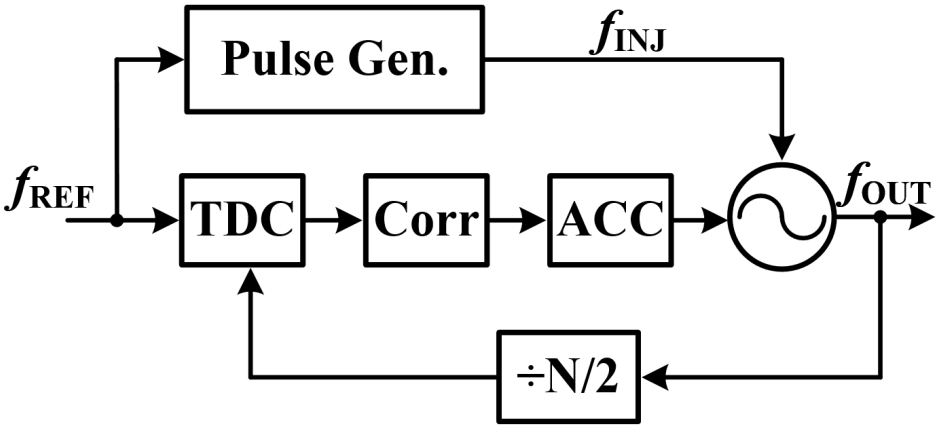
ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

For calibrating f_{VCO} over PVT variations, many FTLs have been reported for ILFMs [15], [17], [19], [20], [25], [56], [57]. However, to detect the information of f_{DEV}, each architecture in those conventional FTLs has used building blocks operating at f_{VCO}. Since the power consumption of these circuits is supposed to grow proportionally as f_{VCO} increases, conventional FTLs are not suitable for mm-wave ILFMs. Fig. 4.3(a) shows a replica-VCO-based FTL using a replica-VCO that has the same control voltage as the main VCO [17], [19], [20]. In this architecture, the replica-VCO is not injection locked; thus, a frequency-locked loop (FLL) can continue to detect and correct any drifts in its frequency. Then, by sharing the control voltage of the FLL, the f_{VCO} of the injection-locked VCO can stay close to the target frequency. This calibration method has an advantage in that it can operate regardless of whether the VCO is injection locked or not. However, the critical problem of this architecture when it is used for an mm-wave ILFM is that the replica-VCO has to consume the same amount of power as the main VCO. As a variation, the architecture in [25] uses a delay-locked loop (DLL) consisting of replica-delay cells to track the drifts of f_{VCO}, but the DLL also must use the same amount of power as the VCO. Fig. 4.3(b) shows the time-to-digital converter (TDC)-based architecture that uses TDC to detect the instantaneous phase shift of the output of the VCO at the moment a pulse is injected from the reference clock [15]. Although these FTLs are popular for calibrating frequency drifts at gigahertz-range frequencies, they should not be used at mm-wave frequencies, at which circuits, such as frequency dividers and TDCs, use excessive power. The ILFM in [56], shown in Fig. 4.3(c), is targeted for generating the output signals at an mm-wave frequency, but since a mixer and dividers, operating at high frequencies, are included, the FLL consumes a large amount of power, more than 60 mW. To overcome the problem of excessive power usage of the calibrating circuits for mm-wave ILFMs, the architecture in [57] presents an FTL using an envelope detector, as shown in Fig. 4.3(d). Based on the observation that the envelope of the output of the VCO becomes constant when the injection lock is acquired, but it fluctuates when the lock is not acquired, this FTL can determine whether injection locking has been acquired or not. Since this architecture is supposed to track the change of the envelope, much slower than the change of the output of the VCO, it can be designed only using building circuits that operate at low frequencies; thus, low-power calibration is available even for an mm-wave ILFM. However, tracking of the envelope provides hardly any additional information after the injection lock is acquired. Thus, while this architecture can be used to overcome the static change of f_{VCO} across process corners, it cannot be used to correct real-time drifts of f_{VCO} from the target frequency due to temperature changes or to prevent the degradation of phase noise.

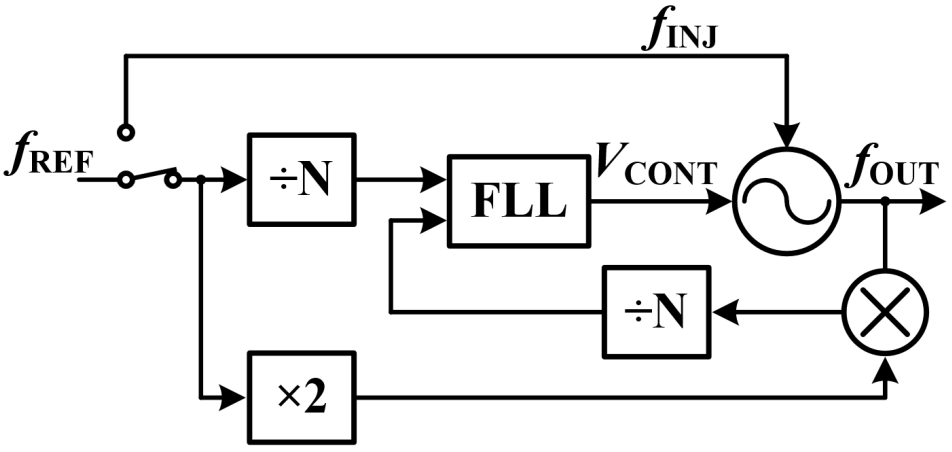
ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(a)

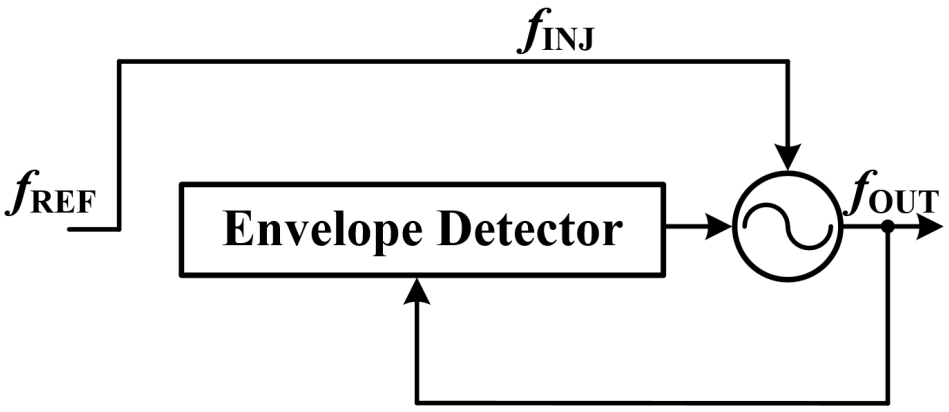


(b)



(c)

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(d)

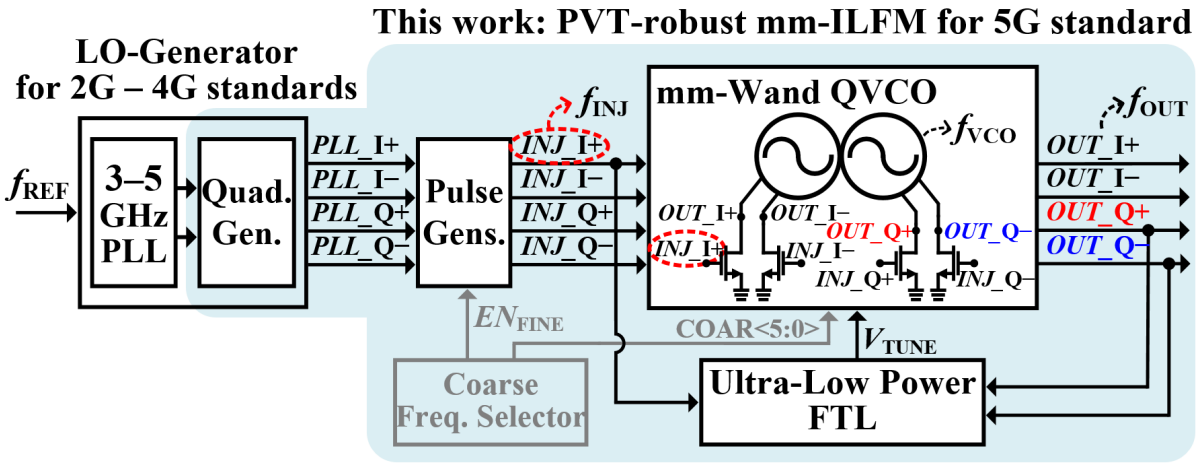
Figure 4.3. ILFMs with different FTLs using (a) a replica-VCO; (b) a TDC; (c) a mixer; (d) an envelope detector.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

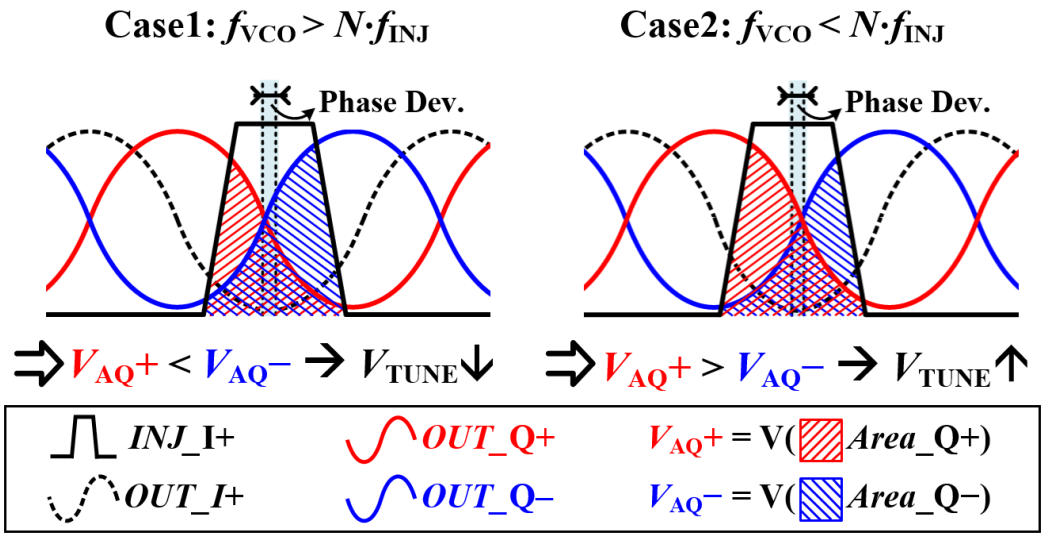
4.3. Proposed ILFM With an Ultra-Low-Power FTL Using the Averages of the Phase Deviations

4.3.1. Overall Architecture

Fig. 4.4(a) shows the proposed ILFM, which consists a quadrature generator, QVCO, pulse generators (PGs), coarse frequency selector (CFS), and low-power FTL. Since an on-chip PLL was not designed in this work, an external RF-signal generator or external PLL is used to provide input signals to the quadrature generator. The PGs receive the quadrature signals and generate the injection pulses, i.e., INJ_I+, INJ_I−, INJ_Q+, and INJ_Q−, where the frequency is f_{INJ}. These pulses are injected to the



(a)



(b)

Figure 4.4. (a) Conceptual diagram of the cascaded architecture of an mm-wave LO generator. (b) Principle of the proposed frequency-tracking loop (FTL).

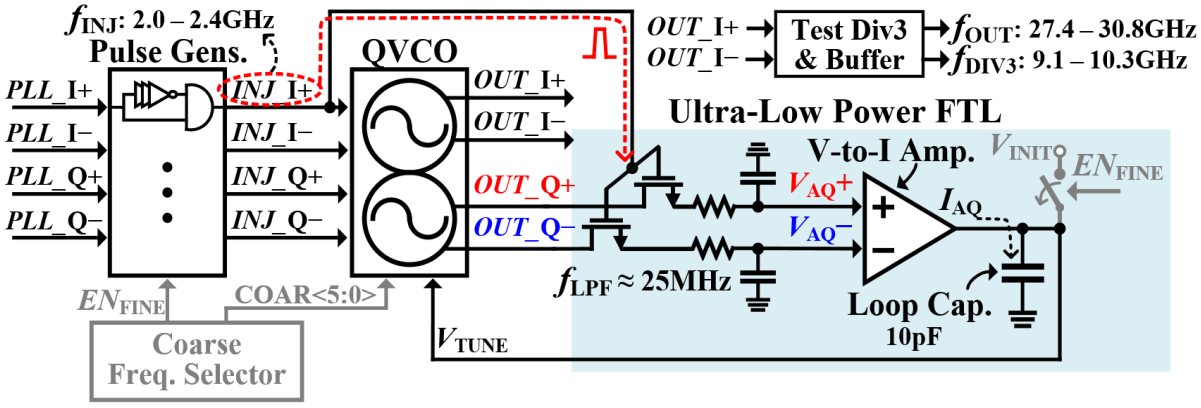
ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

gates of the injection transistors, where the drains are connected to the outputs of the QVCO. When an injection pulse enters the gate, the corresponding output the QVCO is pulled down, leading to instantaneous phase realignment. Fig. 4.4(b) shows the principle of the proposed FTL, which uses the relationship between the phases of INJ_I+, OUT_Q+, and OUT_Q−. At the moment when INJ_I+ is injected, the phase of OUT_I+ is realigned momentarily. However, OUT_Q+ and OUT_Q− still maintain their intrinsic phases independent of INJ_I+, since the coupling strength between the two VCOs of the QVCO is much less than the phase-realigning strength of the injection pulses. Thus, if f_{VCO} deviates from $N{\cdot}f_{INJ}$, the quadrature relationship between the outputs of the QVCO is distorted instantaneously, i.e., INJ_I+ becomes closer to either OUT_Q+ or OUT_Q−. This distortion can be detected by comparing the overlapped area of INJ_I+ with OUT_Q+ and that with OUT_Q−; the difference between the two areas is proportional to the difference between f_{VCO} and $N{\cdot}f_{INJ}$. In this paper, the information of the areas is obtained as voltages, i.e., V_{AQ}+ and V_{AQ}−, by multiplying INJ_I+ by OUT_Q+ and by multiplying INJ_I+ by OUT_Q−, respectively. As shown in Case 1 in Fig. 4.4(b), in which f_{VCO} is higher than $N{\cdot}f_{INJ}$, V_{AQ}+ should be lower than V_{AQ}− since INJ_I+ is closer to OUT_Q− than it is to OUT_Q+. Then, the control voltage V_{TUNE} decreases to lower f_{VCO}. When f_{VCO} is lower, as shown in Case 2, V_{AQ}+ is higher than V_{AQ}−, and, thus, V_{TUNE} must increase to adjust f_{VCO} to be higher.

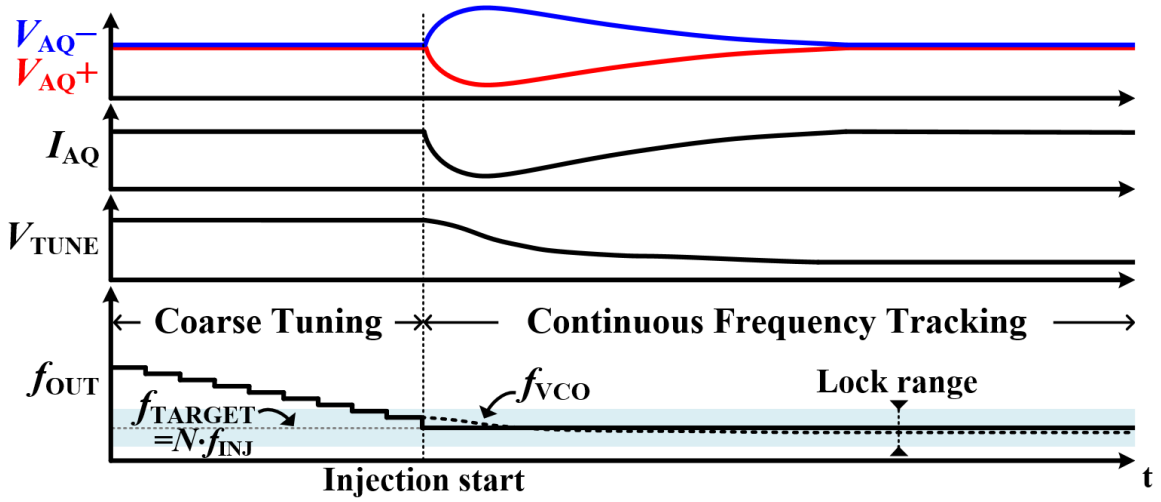
Fig. 4.5(a) and (b) shows the overall architecture and the conceptual transient behavior of the proposed FTL, respectively. When the coarse tuning is done by the CFS, the FTL starts continuous tracking of the frequency in order to monitor the average phase deviations. In the FTL, OUT_Q+ and OUT_Q− are transferred to the low-pass *RC*-filters through the NMOS switches, which are closed during the pulsewidth of INJ_I+. Since the effective bandwidth of the low-pass filters f_{LPF} (including the effect of the NMOS switches) is much lower than f_{INJ}, V_{AQ}+ and V_{AQ}− almost become dc voltages, implying the average values of the overlapped areas of OUT_Q+ and OUT_Q−, respectively. The series resistors in the *RC*-filters also have the role of preventing the reduction of the tank-Q of the VCO by the capacitors of the filters, while the switches are turned ON. The following V-to-I amplifier generates the current I_{AQ} depending on the difference between V_{AQ}+ and V_{AQ}−. As I_{AQ} charges or discharges the loop capacitor, V_{TUNE} is controlled to adjust f_{VCO} to be very close to $N{\cdot}f_{INJ}$. Since any drifts of f_{VCO} in steady-state operation would cause mismatches between V_{AQ}+ and V_{AQ}−, the FTL can keep correcting f_{VCO} without the loss of injection locking. The loop bandwidth of the FTL was approximately 2 MHz, whereas the f_L of the ILFM was 200 MHz. Since the loop bandwidth of the FTL is much less than f_L, the stability of the system can be ensured without any conflicts between two frequency-control mechanisms. To correct the frequency of a multi-phase ring VCO, the multi-phase generator in [64] uses a similar method. However, it uses the relationship between the output phases of the VCO themselves using a quadrature mixer, while the proposed FTL uses the relationship of the phases of the injection signal and the signals of the VCO. Due to this difference, the proposed FTL can achieve a

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

much higher loop gain, when it is used for an ILFM having a large N. In addition, to drive the quadrature mixer operating at f_{VCO}, the buffers need a relatively large power in [64].



(a)



(b)

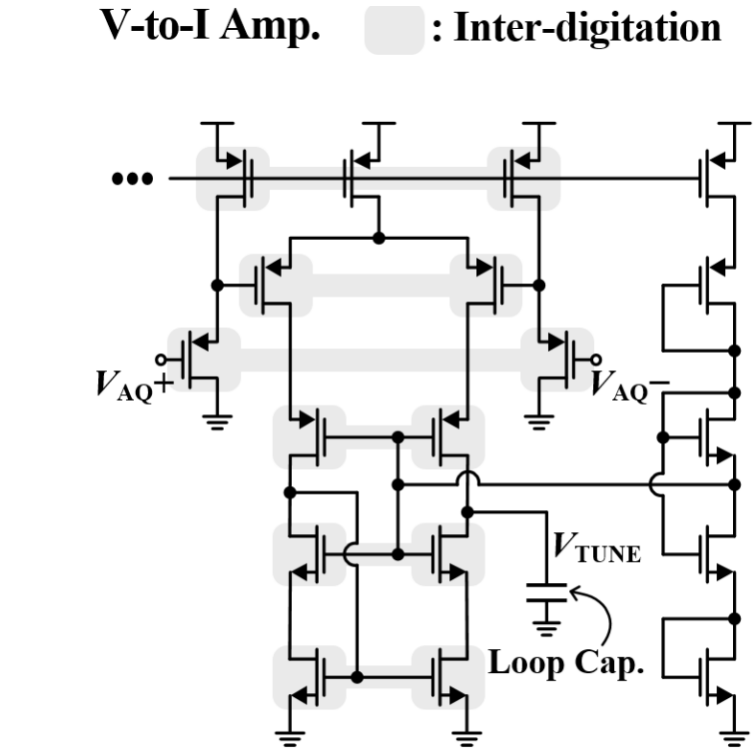
Figure 4.5. Proposed mm-wave ILFM with the ultra-low power FTL. (a) Overall architecture. (b) Conceptual timing diagram.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

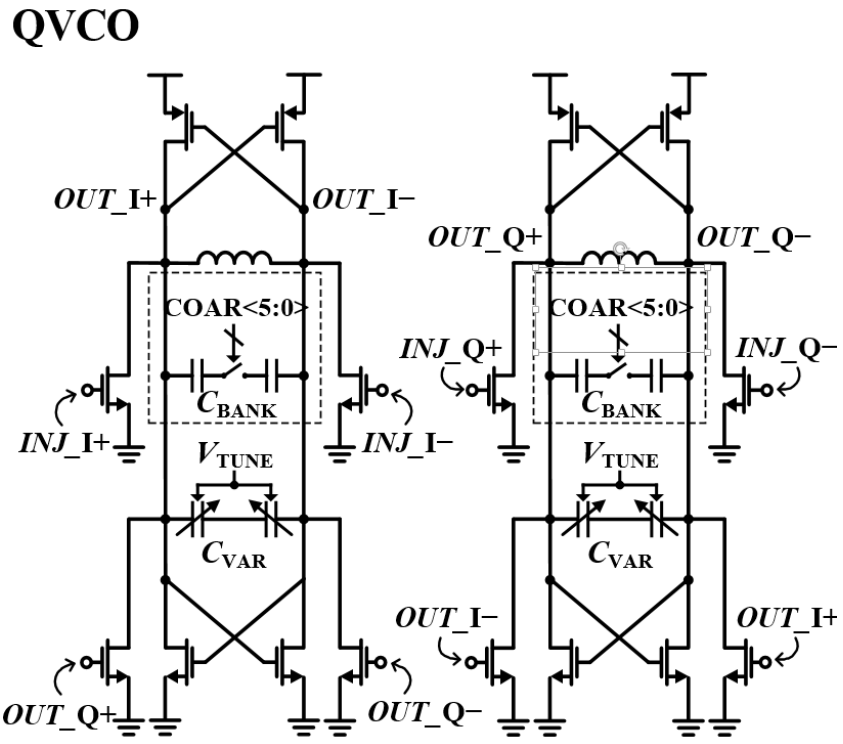
4.3.2. V-to-I Amplifier and the QVCO

Fig. 4.6(a) shows the schematics of the V-to-I amplifier of the FTL that consists of two stages. The first stage acts as a level shifter to shift up the operating points of the inputs, V_{AQ}+ and V_{AQ}−, from the level of the voltage of the precedent *RC*-filters. The second stage, based on an operational transconductance amplifier, has a cascode active load to enhance the gain and reduce mismatches in the currents. The inter-digitation technique is used in the layout of each transistor pair to improve the differentially. As shown in Fig. 4.6(b), the QVCO is composed of two CMOS-type VCOs. Along with the pairs of NMOS and PMOS gm-transistors, each VCO also has additional pairs of NMOS switches; one pair is for coupling the two VCOs, and the other is for applying the injection pulses from the reference clock. As in the foregoing discussion, the fundamental operation principle of the proposed FTL is to detect the instantaneous distortion of the quadrature relationship between OUT_I+ (or OUT_I−) and OUT_Q+ (or OUT_Q−) of the QVCO at the moment when the injection pulse is applied to OUT_I+ (or OUT_I−). This operation is based on the assumption that only the phase of OUT_I+ (or OUT_I−) is realigned instantaneously by the injection pulse, whereas OUT_Q+ (or OUT_Q−) maintains its intrinsic phase according to f_{VCO}. Therefore, to improve the efficiency of the detecting operation, the phase-realigning strength of the injection pulses must be greater than the strength of the internal coupling within the QVCO. To satisfy this condition, the ratio of the size of the NMOS switches for the injection to that for the coupling was designed to be nine to one. Despite the relatively weak coupling within the QVCO, the 3-sigma value of the quadrature error of the QVCO in this work was 1.8°, according to the Monte-Carlo simulation. Each VCO includes six-bit binary-weighted metal–oxide–metal capacitors and a varactor to adjust f_{VCO}. The six-bit capacitor bank is controlled by COAR<5:0> from the CFS in the coarse-tuning step. In the frequency-tracking mode, the varactor is adjusted continuously by V_{TUNE}, which is generated from the FTL.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(a)



(b)

Figure 4.6. Schematics of (a) V-to-I amplifier and (b) QVCO

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

4.3.3. Quadrature Generator, the Pulse Generator, and the Switched *RC*-filters

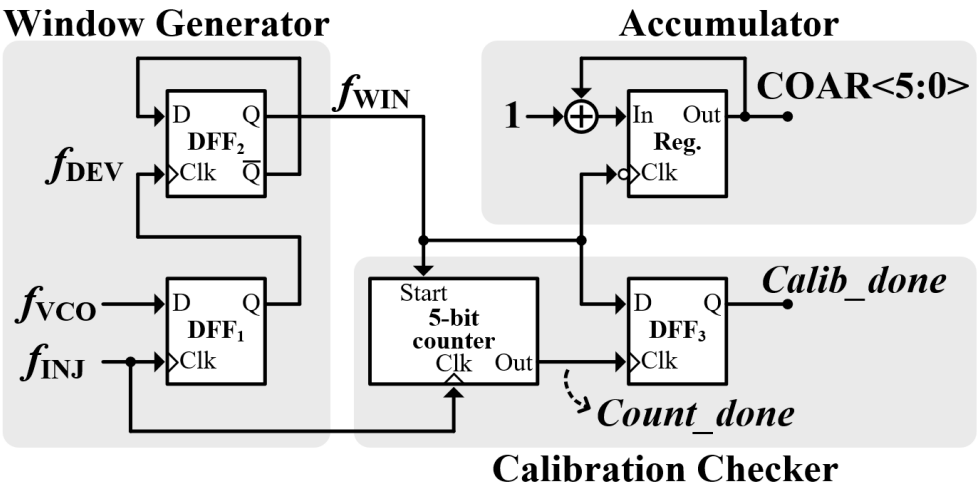
To realize the complete concept, as shown in Fig. 4.4(a), an on-chip PLL generating 3–5-GHz signals should be designed together with the proposed ILFM. Then, a simple divide-by-2 divider could easily generate quadrature signals from the differential signals of the PLL. However, in this work, since only the proposed mm-wave ILFM was implemented as a prototype, no internal differential signals were available. Thus, the quadrature generator is based on a divide-by-4 divider, receiving an input signal with a frequency of $4f_{INJ}$ from an external signal generator, and it consumes 2.2 mW. A quadrature error in the injection signals could lead to that in the output signals of the QVCO, which is more severe as N increases. However, this effect is significantly alleviated by the coupling within the QVCO. This is because although the coupling strength of the QVCO is weaker than the injection strength, it corrects the quadrature relationship of the output signals for a much longer time. According to the simulation, a 1°-quadrature error in the injection signals caused a 2.1°-quadrature error in the output signals. This value can be further reduced by increasing the coupling strength of the QVCO at the expense of a slow operation of the FTL.

Each of the four PGs consists of three inverters and a NAND gate. The width of the injection pulses PW was designed to be 15 ps, but it could change between 12 and 22 ps according to corner and temperature simulations. PW is an important factor to define the conversion gain $K_{\theta 2V}$ from the phase error of the VCO's signal to the dc voltage of $V_{AQ}+$ (or $V_{AQ}-$). From simulations to observe a change in the voltage of $V_{AQ}+$ (or $V_{AQ}-$) due to a phase error, $K_{\theta 2V}$'s were 0.39, 0.3, and 0.2 V/rad, when PW's were 12, 15, and 22 ps, respectively.

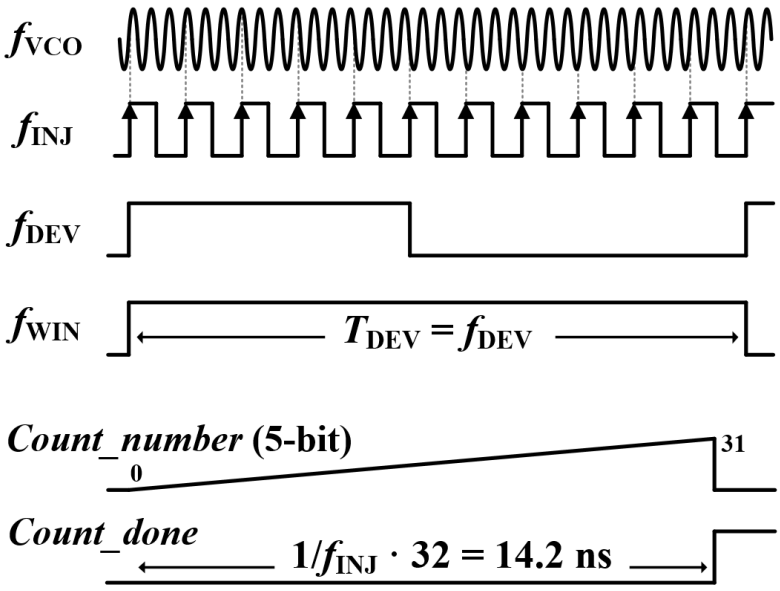
For the switched *RC*-filters, the resistance and the capacitance are approximately 2.1 kΩ and 100 fF, respectively. The NMOS switches used low threshold voltage devices, and the width and the length of the switches were designed to be 370 and 60 nm, respectively. To match capacitive loadings to the VCOs, dummy NMOS switches were also used for the outputs of VCO_I. Since the on-resistance of the NMOS switches was approximately 1.6 kΩ, the series resistors of the *RC*-filters were designed to have a resistance of 0.5 kΩ. The charge injection or sharing due to the switching of the *RC*-filters could cause undesired periodic phase shifts in the outputs of the VCO. However, from the simulation results, the phase shift due to this effect is almost negligible compared to other non-ideal factors, such as the quadrature error of the QVCO. This is because the size of the NMOS switches is very small, and the resistance of the switched *RC*-filters is large enough to suppress the charge sharing. Since the switched *RC*-filters are connected to the differential outputs of the VCO, the effects of delivered charges can be canceled out due to the nature of the differential signaling.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

4.3.4. Coarse Frequency Selector



(a)



(b)

Figure 4.7. (a) Schematics of the CFS. (b) Conceptual timing diagram of the CFS.

Fig. 4.7(a) and (b) shows the schematics and the conceptual timing diagram of the CFS [63]. As shown in Fig. 4.7(a), the CFS consists of a window generator, an accumulator, and a calibration checker. Initially, f_{VCO} is set to the maximum value with the lowest value of COAR<5:0>. As shown in Fig. 4.7(b), the window generator provides a window signal, where its length corresponds to the difference between f_{VCO} and $N \cdot f_{INJ}$. Every time when a window signal is generated, the calibration checker compares the length of the window signal with the reference time, i.e., 14.2 ns, generated by a five-bit counter. Then, if the length of the window is less than the reference time, the accumulator increases the value of COAR<5:0> by one, which decreases f_{VCO}. This process is iterated until the difference between

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

f_{VCO} and $N{\cdot}f_{INJ}$ is sufficiently reduced, and, thus, *Calib_done* goes high. The frequency resolution of the CFS is fixed at approximately one third of the lock range. Since the CFS was designed to detect the difference between f_{VCO} and $N{\cdot}f_{INJ}$ using a D-flip-flop, DFF_1, without the help of a frequency divider, it must suffer from a limited capture range. However, in this work, only one specific N is targeted for a given f_{INJ} to generate the output frequency around 30 GHz; thus, this CFS circuit is sufficient to initialize f_{VCO} before the operation of the continuous FTL.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

4.4. Analysis of Phase Noise and Static Frequency Offset

4.4.1. Phase Noise of the Proposed ILFM

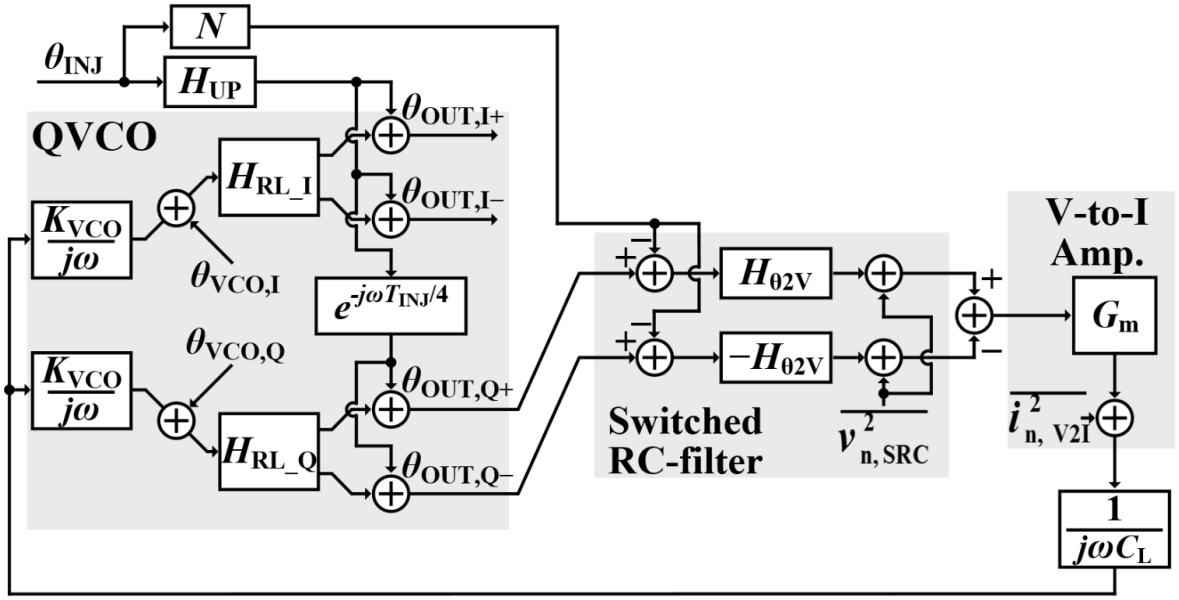


Figure 4.8. Noise model of the proposed mm-wave ILFM.

Fig. 4.8 shows the noise model of the proposed ILFM. The units of the gains of the VCO, K_{VCO}, the switched *RC*-filter, $H_{\theta 2V}$, and the V-to-I amplifier, G_m, are [rad/s/V], [V/rad], and [A/V], respectively. N is the multiplication factor, and C_L is the value of the loop capacitance followed by the V-to-I amplifier. The symbol θ_{INJ} is the output-referred phase error of the injection clock, and $\theta_{VCO,I}$ and $\theta_{VCO,Q}$ are the output-referred phase errors of the two VCOs of the QVCO. The terms $\overline{v_{n,SRC}^2}$ and $\overline{i_{n,V2I}^2}$ are the output-referred voltage noise of the switched *RC*-filter and the output-referred current noise of the V-to-I amplifier, respectively. The phase realignment by the injection clock can be modeled by the following three transfer functions:

$$H_{UP}(j\omega) = \frac{N \cdot \beta \cdot e^{-j\omega T_{INJ}/2}}{1+(\beta-1)e^{-j\omega T_{INJ}}} \frac{\sin(\omega T_{INJ}/2)}{\omega T_{INJ}/2}, \tag{1}$$

$$H_{RL\_I}(j\omega) = 1 - \frac{\beta \cdot e^{-j\omega T_{INJ}/2}}{1+(\beta-1)e^{-j\omega T_{INJ}}} \frac{\sin(\omega T_{INJ}/2)}{\omega T_{INJ}/2}, \tag{2}$$

and $$H_{RL\_Q}(j\omega) = 1 - \frac{e^{-j\omega T_{INJ}/4} \cdot \beta \cdot e^{-j\omega T_{INJ}/2}}{1+(\beta-1)e^{-j\omega T_{INJ}}} \frac{\sin(\omega T_{INJ}/2)}{\omega T_{INJ}/2}, \tag{3}$$

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

where T_{INJ} represents the period of injection clock and β is the phase realign factor that indicates the strength of the phase correction by the injection clock [7], ranging from zero to one. The transfer function of $H_{UP}(j\omega)$ in (1) represents the up-conversion of the injection signal noise to the output. In Fig. 4.8, $\theta_{OUT,I}$ represents the phase error of OUT_I+ (or OUT_I−), when its phase is realigned by INJ_I+ (or INJ_I−), and $\theta_{OUT,Q}$ represents the phase error of OUT_Q+ (or OUT_Q−), when its phase is realigned by INJ_Q+ (or INJ_Q−). The transfer functions of $H_{RL\_I}(j\omega)$ in (2) and $H_{RL\_Q}(j\omega)$ in (3) represent the effects of the phase realignment of the $\theta_{OUT,I}$ and $\theta_{OUT,Q}$ by the corresponding injection pulses, respectively. Since the phase of OUT_Q+ (or OUT_Q−) lags behind that of OUT_I+ (or OUT_I−) by a 90°, $H_{RL\_Q}(j\omega)$ in (3) includes the term of $\exp(-j\omega T_{INJ}/4)$, different from $H_{RL\_I}(j\omega)$ in (2). From the noise model in Fig. 4.8, the open-loop transfer function $LG(j\omega)$ can be obtained as

$$LG(j\omega) = 2 \cdot H_{\theta 2V}(j\omega) \cdot G_m \cdot \frac{1}{j\omega C_L} \cdot \frac{K_{VCO}}{j\omega} \cdot H_{RL\_Q}(j\omega), \quad H_{\theta 2V}(j\omega) = \frac{K_{\theta 2V}}{j\omega/\omega_{LPF} + 1}, \tag{4}$$

where ω_{LPF} is the effective bandwidth of the low-pass filters in radian. Using (1) – (4), the noise transfer functions (NTFs) to the output $\theta_{OUT,I}$ from the noise sources can be obtained as:

$$H_{INJ}(j\omega) = \frac{\theta_{OUT\_I}}{\theta_{INJ}} = H_{UP}(j\omega) + \left(H_{UP}(j\omega) \cdot e^{-j\omega T_{INJ}/4} - N\right) \cdot \frac{LG(j\omega)}{1 - LG(j\omega)} \cdot \frac{H_{RL\_I}(j\omega)}{H_{RL\_Q}(j\omega)}, \tag{5}$$

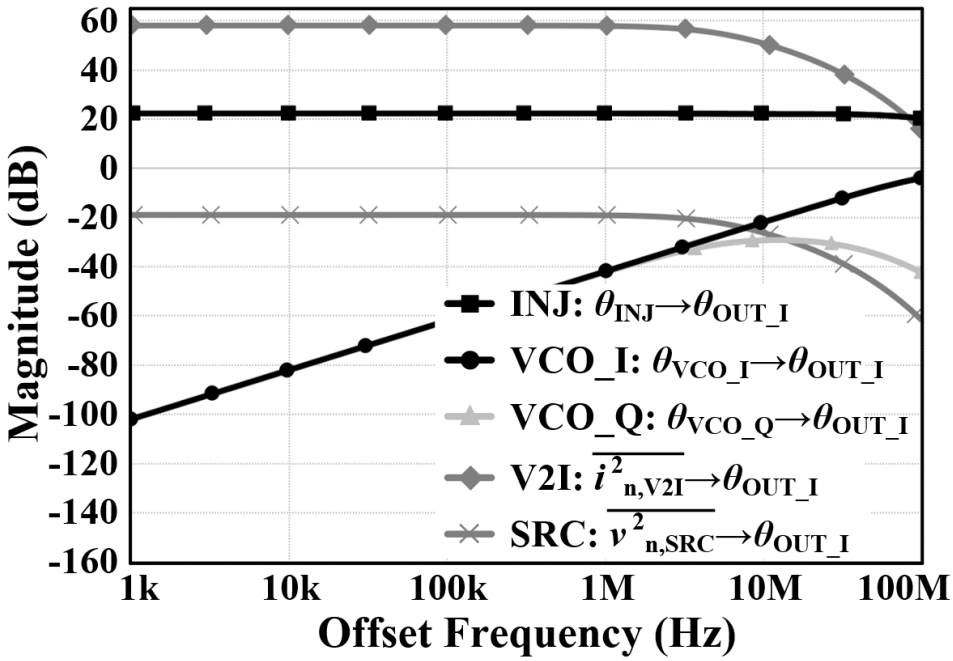
$$H_{VCO\_I}(j\omega) = \frac{\theta_{OUT\_I}}{\theta_{VCO\_I}} = H_{RL\_I}(j\omega), \tag{6}$$

$$H_{VCO\_Q}(j\omega) = \frac{\theta_{OUT\_I}}{\theta_{VCO\_Q}} = \frac{LG(j\omega)}{1 - LG(j\omega)} \cdot H_{RL\_I}(j\omega), \tag{7}$$

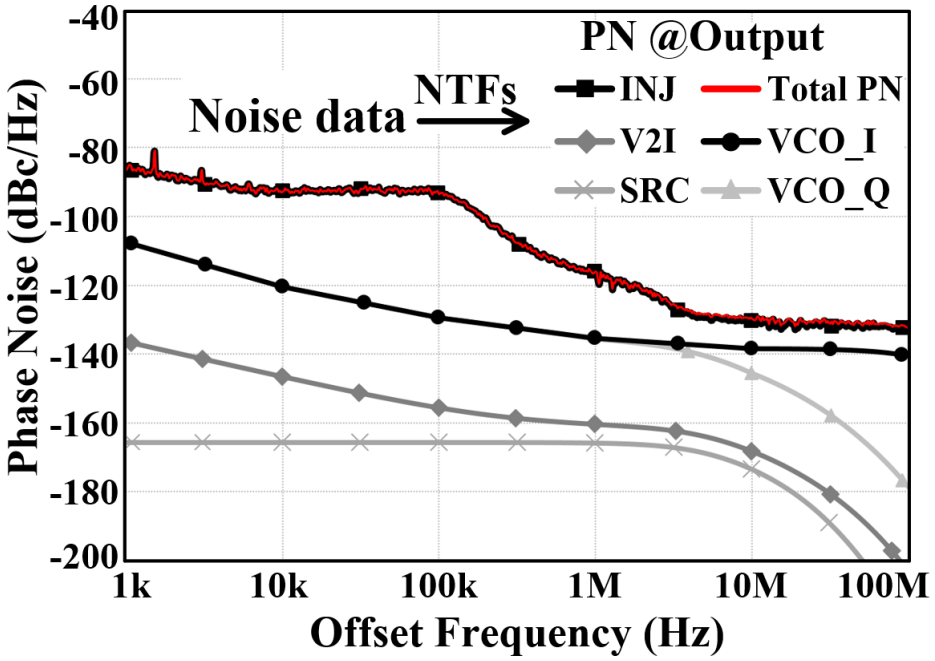
$$H_{V2I}(j\omega) = \frac{\theta_{OUT\_I}}{\overline{i_{n,V2I}^2}} = \frac{1}{1 - LG(j\omega)} \cdot \frac{1}{j\omega C_L} \cdot \frac{K_{VCO}}{j\omega} \cdot H_{RL\_I}(j\omega), \tag{8}$$

$$\text{and} \quad H_{SRC}(j\omega) = \frac{\theta_{OUT\_I}}{\overline{v_{n,SRC}^2}} = \frac{1}{1 - LG(j\omega)} \cdot \frac{G_m}{j\omega C_L} \cdot \frac{K_{VCO}}{j\omega} \cdot H_{RL\_I}(j\omega) \tag{9}$$

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(a)



(b)

Figure 4.9. NTFs of building blocks based on (5) – (9). (b) Estimated phase noise from the noise model.

In (5) – (7), $H_{INJ}(j\omega)$, $H_{VCO\_I}(j\omega)$, and $H_{VCO\_Q}(j\omega)$ represent the NTFs of the injection clock, the VCO_I, and the VCO_Q, respectively. Similarly, in (8) and (9), $H_{V2I}(j\omega)$ and $H_{SRC}(j\omega)$ are the NTFs of the V-to-I amplifier and the switched *RC*-filter, respectively. The NTFs of the building blocks, (5) – (9), are

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

plotted in Fig. 4.9(a). For the NTFs, K_{VCO}, ω_{LPF}, G_m, C_L, and N are 800 MHz/V, $2\pi \cdot 25$ Mrad/s, 150μA/V, 10 pF, and 13, respectively. The injection frequency is 2.25 GHz and β is 0.3. (The value of β can be obtained by measuring the phase shift of the output signal of the VCO by that of the injection signal through simulations, as explained in [7].) These NTFs are also used to estimate the total phase noise of the ILFM and the noise contribution of each building block. In Fig. 9(b), the phase noise of each building block at the output is plotted by passing the noise data through the corresponding NTF. The noise data of the injection clock are from measurements, and those of other circuits are from post-layout simulations. Fig. 4.9(b) shows that the total phase noise is dominated by the noise of the injection clock. The noise from the building blocks of the FTL does not make any considerable contribution to the total phase noise; thus, the proposed ILFM is able to achieve ultra-low phase noise, which is very close to the theoretical minimum.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

4.4.2. Static Frequency Offset by Mismatch Effects in the FTL

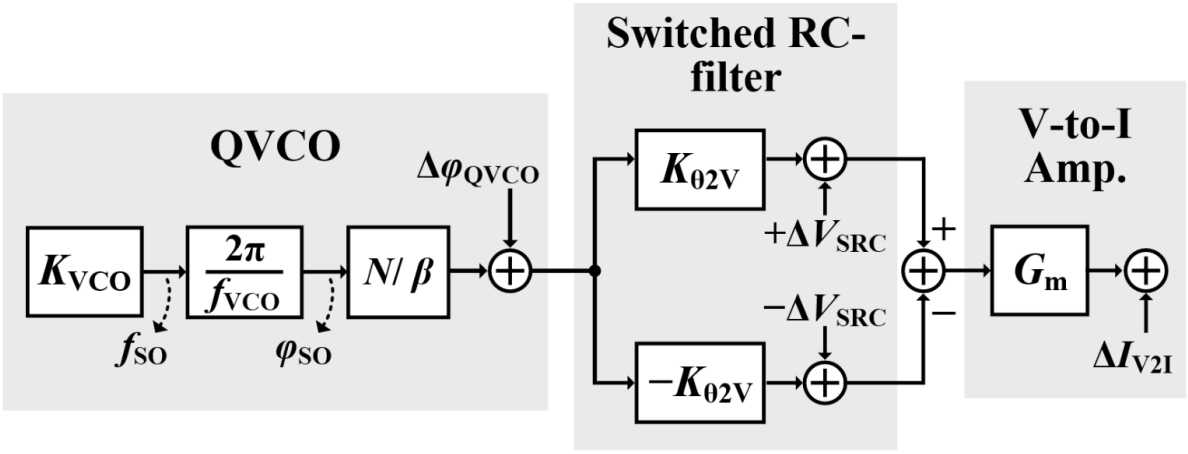


Figure 4.10. Linear model of static frequency offset due to mismatch effect of FTL.

As mentioned in Section 4.2, if the frequency error increases significantly with respect to the lock range, the performance of phase noise should be degraded. The fundamental mechanism of the proposed FTL for detecting the error in the frequency is to compare the relative phases of the differential output signals of a VCO with respect to the injection pulse. Therefore, if there were a mismatch between the two parallel lines, through which the differential outputs of the VCO proceed to the comparator, the precision of the FTL would be degraded severely. Fig. 4.10 shows the linear model, representing the effects of various mismatch factors from the QVCO to the V-to-I amplifier. In the modeling of the QVCO part, φ_{SO} represents the static phase offset of the VCO output from the ideal position, corresponding to the static frequency offset of the VCO, f_{SO}, with respect to the target frequency. When the injection pulse is applied to the VCO, φ_{SO} is supposed to extend by N/β [7]. This effect is included as the last term in the model of the QVCO. According to the model in Fig. 10, f_{SO} is determined mainly by the following three factors: 1) the quadrature phase mismatch of the QVCO $\Delta\varphi_{QVCO}$; 2) the mismatch between the pair of the switched *RC*-filters ΔV_{SRC}; and 3) the up/down current mismatch of the V-to-I amplifier ΔI_{V2I}. Considering the input-referred value and using these three error factors, f_{SO} can be represented as:

$$f_{SO} = \frac{f_{VCO}}{2\pi} \cdot \frac{\beta}{N} \cdot \left(\Delta\varphi_{QVCO} + \frac{1}{K_{\theta 2V}} \cdot 2\Delta V_{SRC} + \frac{1}{K_{\theta 2V} \cdot G_m} \Delta I_{V2I} \right). \quad (10)$$

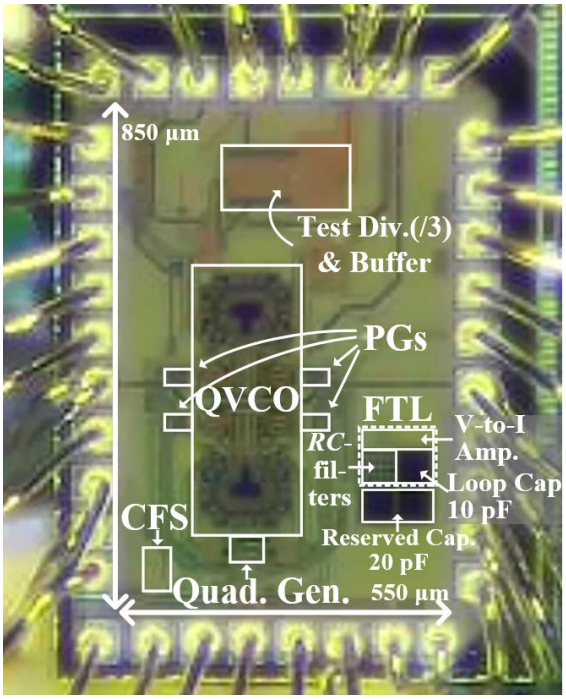
Based on the results of Monte-Carlo simulations, the 3-sigma values of $\Delta\varphi_{QVCO}$, ΔV_{SRC}, and ΔI_{V2I} are

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

approximately 0.01π, 8 mV, and 3.6 μA, respectively. Considering the worst-case values of $K_{\theta 2V}$ and G_m, i.e., 0.2 V/rad and 150 μA/V, the largest contribution to f_{SO} comes from the up/down current mismatch of the V-to-I amplifier, and it is followed by the mismatch effect of the switched *RC*-filters. When f_{VCO} and N are 29.25 GHz and 13, respectively, according to (10), the worst-case value of f_{SO} is 24.9 MHz, which is approximately 0.085% of f_{VCO}. Since f_{SO} is small compared to the lock range, which is larger than 200 MHz, it is concluded the degradation of the phase noise of the ILFM due to this mismatch effect is almost negligible. The level of the reference spur caused by this mismatch can be calculated from the equation, $\text{Spur}_{dBc} \approx 20 \log(N \cdot | f_{SO} / f_{OUT} |)$ [15]. According to this equation, the largest level of the reference spur is −39.1 dBc.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

4.5. Experimental Results



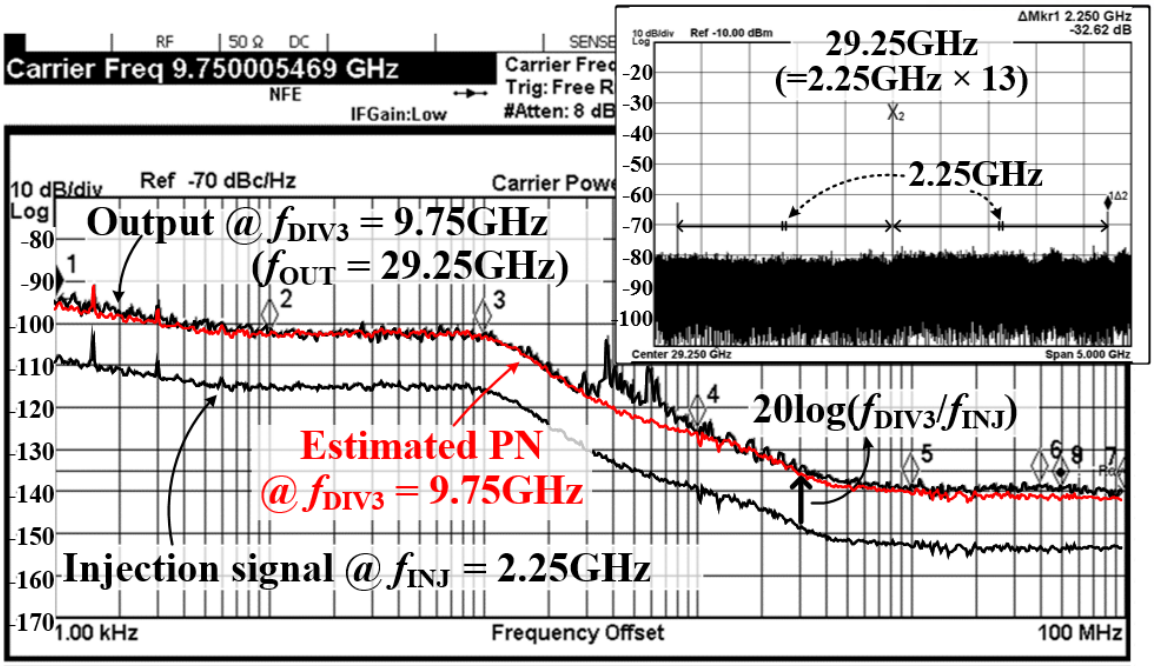
Power Consumption (mW)	
QVCO	17.5
PGs	4.0
Quad. Gen.	2.2
FTL (V-to-I Amp.)	0.6
Total	24.3

(a) (b)

Figure 4.11. (a) Die photograph. (b) Power-breakdown table.

The proposed mm-wave ILFM was fabricated in a 65-nmCMOS technology, and the active area was 0.11 mm^2, as shown in Fig. 4.11(a). According to the table in Fig. 4.11(b), the total power consumption of this paper was 24.3 mW, but the proposed ultra-low-power FTL consumed only 600µW. Using the injection clock with a frequency between 2 and 2.4 GHz, the proposed ILFM is capable of generating the output frequency from 27.4 to 30.8 GHz. Fig. 4.12 shows the spectrum and the phase noise, measured using a spectrum analyzer, Agilent PXA N9030A. To achieve sufficient output power for the accurate measurement of phase noise, f_{OUT} was reduced to f_{DIV3} by the on-chip divide-by-3 test divider. In this measurement, the frequency of the output signal (or f_{OUT}) was 29.25 GHz, when N was 13, and the injection frequency (or f_{INJ}) was 2.25 GHz. Fig. 4.12 also shows the phase noises of the output of the test divide-by-3 divider (f_{DIV3} = 9.75 GHz) and the injection signal. The injection signal was generated from a signal generator, Agilent N5183A. The difference between the levels of phase noises of the output and the injection signals is very close to the theoretical value, i.e., 20 log(f_{DIV3}/f_{INJ}) up to 100 MHz, implying the noise added by the ILFM is extremely small. From the measurement data at the output of the test divide-by-3 divider, the noise of the original output signal at f_{OUT} of 29.25 GHz can be restored to the phase noise of −129.7 dBc/Hz at 10-MHz offset and the IPN from 1 kHz to 100 MHz of −39.1 dBc. Even when the FTL was turned OFF, no noticeable differences were observed. To verify

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

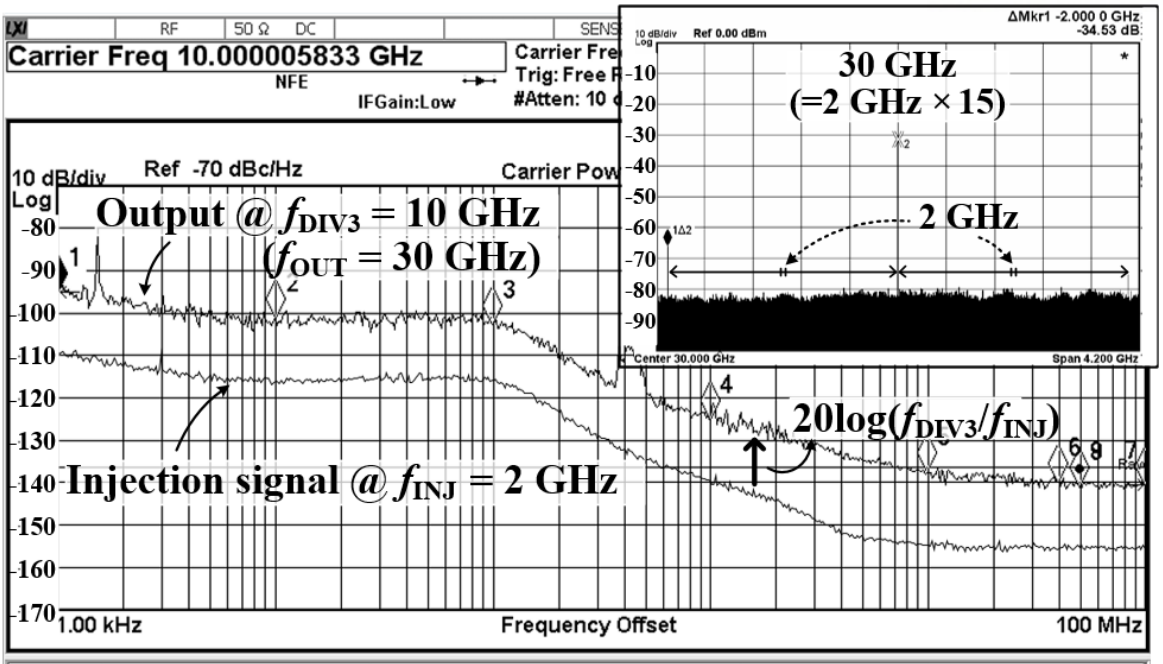


MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
	N	2	1.00 kHz	-94.10dBc/Hz			
2	N	2	10.0 kHz	-102.38dBc/Hz			
3	N	2	100 kHz	-102.67dBc/Hz			
4	N	2	1.00 MHz	-125.13dBc/Hz			
5	N	2	10.0 MHz	-139.28dBc/Hz			
6	N	2	40.0 MHz	-138.29dBc/Hz			
7	N	2	100 MHz	-139.77dBc/Hz			
8	N	2	50.0 MHz	-139.71 dBc/Hz	Integ Noise	100 MHz	85.55 fs
9	N	2	50.0 MHz	-139.71 dBc/Hz	Integ Noise	100 MHz	-48.62 dBc

Figure 4.12. Measured spectrum and phase noise of the output signal with 29.25 GHz (f_{INJ} = 2.25 GHz, N = 13) with estimated phase noise from the noise model in Section 4.4.

the validity of the noise model, presented in Section 4.4, the estimated phase noise from this noise model also was plotted together in Fig. 4.12. The data of phase noises of the injection clock and the free-running VCO were obtained from the measurements, while the data of the noises of the switched *RC*-filter and the V-to-I amplifier were from the post-layout simulations. The estimated phase noise from the noise model shows a good agreement with the measurement result. The level of the reference spur shown in Fig. 4.12 is relatively high, compared to the estimated value in the analysis of Section 4.4. This is because the minimum level of the spur that could be measured was restricted by external causes, such as the direct couplings of the injection signal to the output path. Since the strength of a high-frequency output signal decreases along the inverter chain of the test buffer, the coupling of the injection signal to the test buffer through the substrate or the power line could be a major cause. Fig. 4.13 shows the spectrum and the phase noise of the output signal with f_{OUT} of 30 GHz, when f_{INJ} was 2 GHz, and N was 15. From the phase noise measured at f_{DIV3} of 10 GHz after the on-chip divide-by-3 test divider, the 10-MHz phase noise and the IPN at f_{OUT} of 30 GHz can be estimated as −127.9 dBc/Hz and −38.6 dBc, respectively.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	2	1.00 kHz	-95.06dBc/Hz			
2	N	2	10.0 kHz	-100.94dBc/Hz			
3	N	2	100 kHz	-102.64dBc/Hz			
4	N	2	1.00 MHz	-125.12dBc/Hz			
5	N	2	10.0 MHz	-137.47dBc/Hz			
6	N	2	40.0 MHz	-139.82dBc/Hz			
7	N	2	100 MHz	-140.41dBc/Hz			
8	N	2	50.0 MHz	-140.67 dBc/Hz	Integ Noise	100 MHz	88.11 fs
9	N	2	50.0 MHz	-140.67 dBc/Hz	Integ Noise	100 MHz	-48.15 dBc

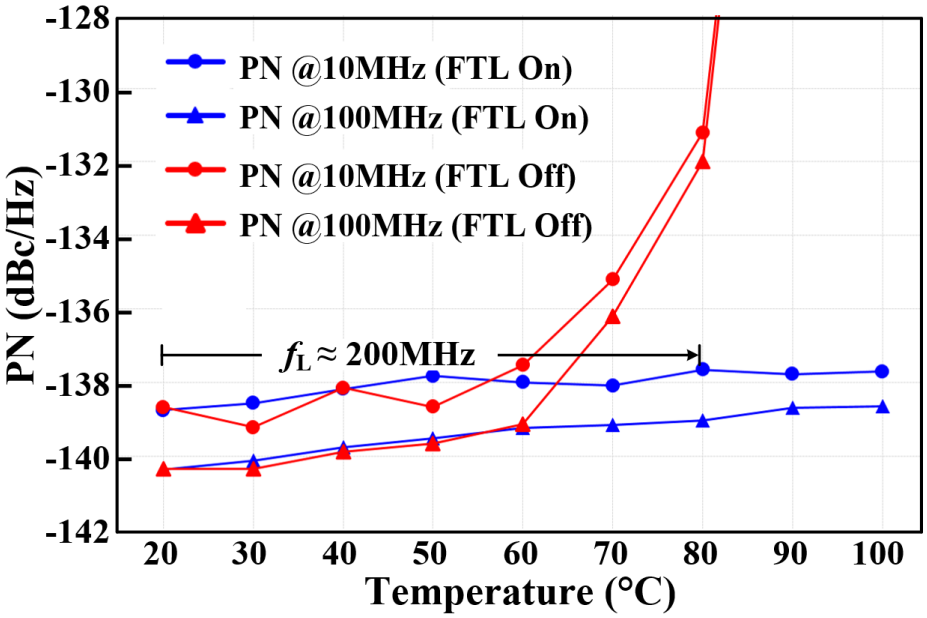
Figure 4.13. Measured spectrum and phase noise of the output signal with 30.0 GHz (f_{INJ} = 2.0 GHz, N = 15).

In Fig. 4.14(a) and (b), the variations of the phase noise were measured, when the temperature and the supply voltage were changed from 20 °C to 100 °C and from 0.9 to 1.35 V, respectively. The phase noises were also measured at the output of the divide-by-3 divider (f_{DIV3} = 9.75 GHz), to which the 29.25-GHz output signal transferred. When the FTL was turned OFF, as the temperature and the supply voltage changed, f_{VCO} deviated gradually from the target frequency. When the drift of f_{VCO} approached f_L, which was around 200 MHz, the performance of the phase noise was degraded rapidly. When the FTL was turned ON, on the other hand, f_{VCO} was adjusted continuously by the proposed FTL; thus, the degradation of phase noise was tightly regulated to less than 2 dB, irrespective of the changes of the temperature and the supply voltage. The tracking range was measured by changing f_{INJ}, until the FTL could not track the drifts of f_{VCO} and the injection lock was released. The measured tracking range was greater than 1 GHz. Fig. 4.15(a) shows the variations of spot noises at offsets of 10 and 100 MHz, measured from five different chips, while the temperature was changed from 20 °C to 100 °C. In the measurements, N was fixed at 13 with f_{INJ} and f_{DIV3} of 2.25 and 9.75 GHz, respectively. Across temperatures, the phase noises were regulated stably in all test chips, implying the proposed FTL

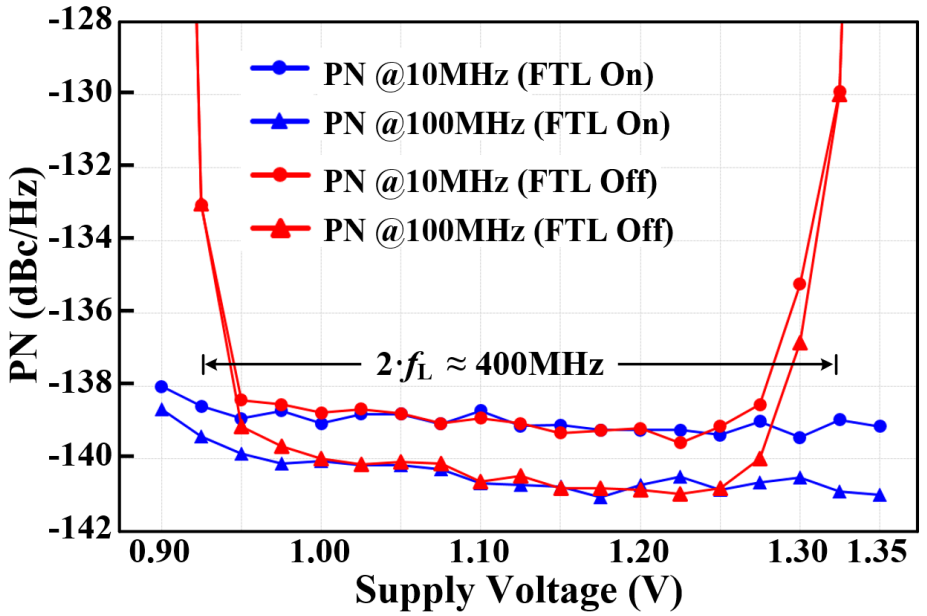
ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

operated properly in different samples. Fig. 4.15(b) shows the variation of the phase noises at the same offsets, when f_{OUT} was swept by changing f_{INJ}. To sweep f_{OUT} from 27.4 to 30.8 GHz, f_{INJ} changed from 2.10 to 2.37 GHz, respectively, while N was fixed as 13. According to Table 2 that compares the performances of this work with those of state-of-the-art mm-wave ILFMs, the ILFM in this work achieved the lowest IPN and rms jitter, irrespective of PVT-variations, although the FTL consumed only 600μW.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



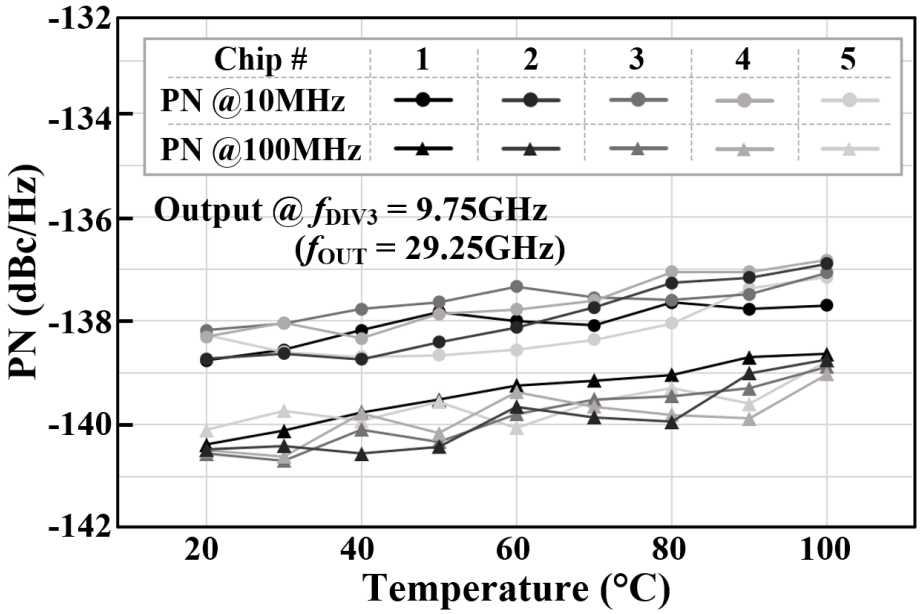
(a)



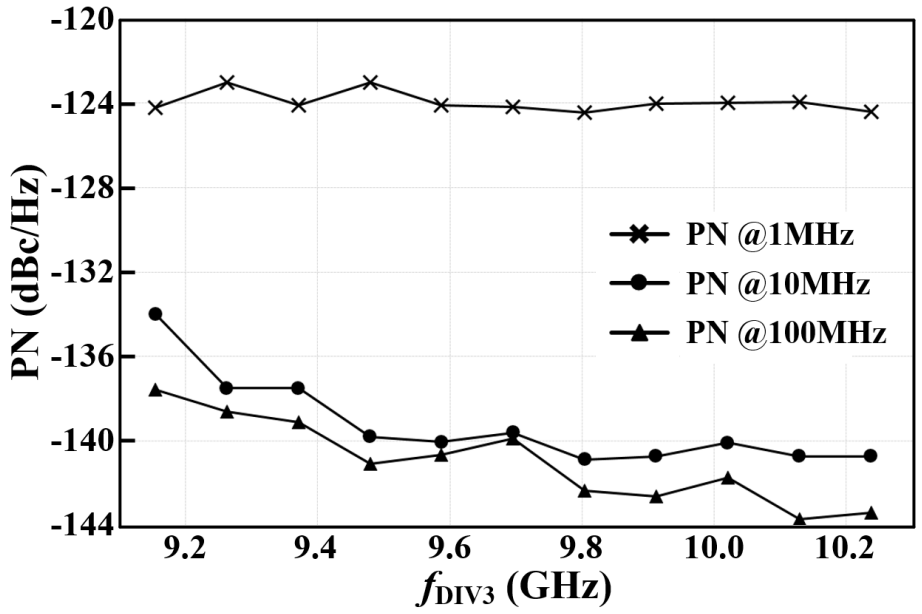
(b)

Figure 4.14. Measured phase noise at the frequency of 9.75 GHz (29.25 GHz /3) over (a) temperatures and (b) supply-voltages, when the FTL was on or off.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(a)



(b)

Figure 4.15. Measured phase noise at f_{DIV3} across (a) temperatures for five different chips and (b) output frequencies from 27.4 to 30.8 GHz (f_{INJ} changed with a fixed N of 13).

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Table 2. Performance Comparison with State-of-the-Art mm-Wave ILFMs

	This work	JSSC'15 [48]	JSSC'13 [56]	ISSCC'16 [57]
Process	65 nm CMOS	40 nm CMOS	65 nm CMOS	130 nm CMOS
Cal. method Real-time cal.	Phase-dev. averaging Yes	No calibration No	Mixer-based Yes	Envelope detecting No
Injection freq., f_{INJ}	2.0 – 2.4 GHz	2.16 GHz	17.9 – 21.7 GHz	8.8 – 10 GHz
Output freq., f_{OUT}	27.4 – 30.8 GHz	58.0 – 63.0 GHz	58.1 – 65.0 GHz	26.5 – 29.7 GHz
1MHz PN @f_{OUT}	−115.6 dBc/Hz* @29.25 GHz	−104.0 dBc/Hz @58.32 GHz	−95.7 dBc/Hz @61.56 GHz	−106.8 dBc/Hz @26.54 GHz
10MHz PN @f_{OUT}	−129.7 dBc/Hz* @29.25 GHz	−109.0 dBc/Hz @58.32 GHz	−117.2 dBc/Hz @61.56 GHz	−118.9 dBc/Hz @26.54 GHz
IPN/ $Jitter_{RMS}$ @f_{OUT} [Integ. Range] ($Jitter_{RMS}$ @f_{INJ})	−39.1 dBc*/ 86 fs @29.25 GHz [1 kHz–100 MHz] (76.8 fs @2.25 GHz)	−10.2 dBc/ 1.2 ps @58.32 GHz [1 kHz – 100 MHz] (1.09 ps @2.16 GHz)	7.5 dBc/ 8.7 ps @61.56 GHz [1 kHz – 40 MHz] (NA)	−33.8 dBc/ 174 fs @26.54 GHz [100 kHz – 100 MHz] (135.8 fs @8.85 GHz)
Tot. power/Cal. only	24.3 mW/ 600 μW	32 mW/ NA	NA**/ 65 mW	23.2 mW/ 2.4 mW
Active area	0.11 mm^2	0.07 mm^2	1.52 mm^2 ***	0.09 mm^2

* Restored from the PN measured at 9.75 GHz (or 29.25 GHz/3) through the test divide-by-3 divider

** No reported power consumption of the ILFM only (total power including 20 GHz PLL is 137 mW)

*** ILFM only

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

4.6. Discussion

In this paper, we presented a PVT-insensitive and low-phase-noise mm-wave ILFM that used the proposed ultra-low-power FTL, which was capable of calibrating real-time frequency drifts. By monitoring the instantaneous distortion between the quadrature phases of the QVCO, caused when the frequency of the VCO deviates from the target frequency, the FTL can continuously track and correct the drifts of the frequency of the VCO due to environmental variations. Therefore, it can tightly regulate the degradation of phase noise. Since the proposed FTL monitors the averages of phase deviations rather than samples the instantaneous values, it uses only 600 μW to keep calibrating the mm-wave ILFM. The ILFM generated the output signal with a frequency ranging from 27.4 to 30.8 GHz. The 10-MHz phase noise of the 29.25-GHz output signal was −129.7 dBc/Hz, and its variations across temperatures and supply voltages were less than 2 dB. The IPN integrated from1 kHz to 100 MHz and the rms jitter were −39.1 dBc and 86 fs, respectively.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Chapter 5.

A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Using a Triple-Point Background Calibrator

5.1. Motivation

Continuous increases in the data rates of either wireline or wireless communication system are requiring further improvement in the jitter performance of clock signals. To date, conventional phase-locked-loop (PLL) architectures that use an *LC*-type, voltage-controlled oscillator (*LC*-VCO) have been used the most extensively in practical applications [65] – [75]. However, the most critical problem of these *LC*-VCO-based PLLs is their large silicon areas since they use many passive components, such as an inductor in the *LC* tank and capacitors in the loop filter. This problem of conventional *LC*-VCO-based PLLs has prevented modern system-on-chips (SoCs) from efficiently using silicon in deep-sub-micron technologies. To overcome this limit, a ring-VCO-based injection-locked clock multiplier (ILCM) is now considered to be an alternative solution. (In the broad sense that the jitter of the VCO is removed periodically by the reference clock, a multiplying delay-locked loop also can be categorized as a type of ILCM). In ILCMs, the phase (or timing) of the output edges of a free-running VCO is corrected naturally by reference signals that are injected periodically [5]. This phase-realignment mechanism of an ILCM is capable of creating a much higher cutoff frequency of the noise transfer function (NTF) of the VCO compared to conventional PLLs, thereby resulting in much greater suppression of the jitter of ring VCOs [7].

Despite the superiority of ILCMs in the reduction of the jitter of ring VCOs, they have a critical problem. This problem occurs because the phase-realignment mechanism of ILCMs has no capability of frequency correction even though it does have the capability of phase correction [76]. Thus, when the free-running frequency of the VCO, f_{VCO}, drifts from the target frequency, $N \cdot f_{REF}$, (where N and f_{REF} are the target harmonic index and the frequency of the reference clock, respectively), the performances of the RMS jitter and reference spur can be degraded significantly. The impact of this problem is more severe in the degradation of the reference spur than in the degradation of the RMS jitter, so even a slight error in f_{VCO} could result in a significant increase in the reference spur, according to [26]:

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

$$\text{Ref. Spur (dBc)} \approx 20\log(N\cdot|f_{ERR}(\%)|), \quad (1)$$

where f_{ERR} is the frequency deviation of f_{VCO} from the target frequency, $N\cdot f_{REF}$. With plotting (1) with respect to f_{ERR}, Fig. 5.1 shows that the level of the reference spur increases steeply as the amount of f_{ERR} grows. When N is ten, only 0.1%-f_{ERR} of the VCO causes a reference spur of −40 dBc. Moreover, since the level of the reference spur is supposed to increase in proportion to N, it is very difficult to reduce the level of the spur sufficiently for a high N, e.g., to be less than −60 dBc.

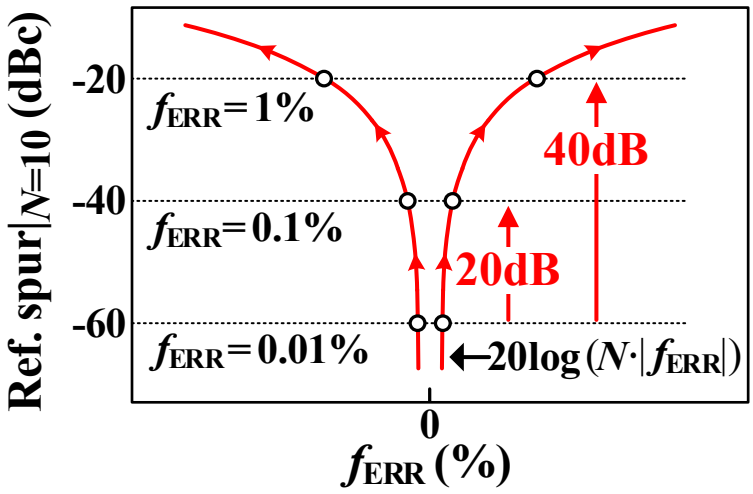


Figure 5.1 Level of reference spur with respect to f_{ERR}.

To address this problem, ILCMs must be equipped with a dedicated calibrator that can correct f_{VCO} continuously in the background. Recently, various architectures of the calibration have been developed, and, thus, many ILCMs have achieved a very low jitter and the excellent figure of merit of jitter (FoM_{JIT}) [25] – [31], [77] – [81]. Nevertheless, to date, none of them has succeeded in reducing the level of the reference spur to a level comparable to that of PLLs. This is because conventional calibrators have not considered all causes of the generation of the frequency errors of ILCMs, f_{ERR}s (Two other causes hinder the precise calibration of the frequency calibrator). Therefore, to minimize the level of the reference spur as well as the RMS jitter, a background calibrator for ILCMs should be not only precise but also versatile so that it can accurately remove all three root causes of f_{ERR}s: 1) *frequency drift* due to voltage and temperature fluctuations, 2) *phase offset* due to any systematic errors of calibrators, and 3) *slope modulation* due to the periodic injection of a reference signal. The orthogonal mechanisms of the generation of these three causes of f_{ERR} and the limits in the capability of conventional calibrators are explained in detail in Section 5.2.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

In Chapter 5, we propose a ring-VCO-based ILCM that can achieve both a low RMS jitter and low reference spur with a background triple-point frequency/phase/slope calibrator (TP-FPSC) [82]. It can remove all three causes generating f_{ERR}s accurately since the proposed TP-FPSC provides three orthogonal mechanisms of calibrations, and thus, the ILCM becomes capable of minimizing the level of the reference spur. In addition, a calibration loop of the *frequency drift* is designed to have a wide bandwidth, which helps to further suppress the flicker noise of the ring VCO and to achieve an even lower RMS jitter.

The rest of this paper is organized as follows. Section 5.2 discuss the three root causes of frequency errors and the limits of conventional calibrators. Section 5.3 presents the architecture and the mechanism of the ILCM using the proposed TP-FPSC. Section 5.4 presents the building blocks of the ILCM. Section 5.5 presents the experimental results, and Section 5.6 presents the conclusions that were made based on this work.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

5.2. Analysis on Frequency Error Generation Mechanisms of Root Causes and Limits of Conventional Calibrators

5.2.1. Three Root Causes of Frequency Errors and Limits of Conventional Calibrators

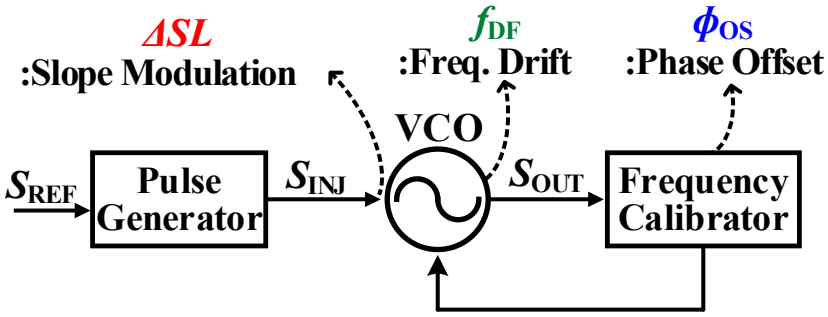


Figure 5.2. Three causes of the frequency error in ILCMs.

Fig. 5.2 shows the three root causes of f_{ERR} in an ILCM. The first root cause of f_{ERR} is the *frequency drift*, f_{DF}, that occurs when f_{VCO} deviates from $N{\cdot}f_{REF}$ due to variations in the supply or the temperature. Figs. 5.3(a) and (b) represent the effect of f_{DF} in the ILCM and how conventional calibrators, such as the one in [29], correct it. Fig. 5.3(a) shows the conceptual block diagram of an ILCM that receives the injection signal, S_{INJ}, from the reference clock, S_{REF}. While there are many other prior calibrators that can remove f_{DF} (the *frequency drift*), Fig. 5.3(a) was drawn based on the most general architectures, i.e., those that used a delay line after the VCO, as presented in [29]. In Fig. 5.3(a), $\phi_{OUT}[k]$ represents the k^{th} phase of the output signal, S_{OUT}, where $1 \le k \le N$. When $k = 1$, the injection occurs, realigning ϕ_{OUT}. Under the assumption that S_{OUT} is delayed exactly by the amount of the VCO period, T_{VCO}, at the output of the delay line, $\phi_{OUT\_D}[k]$, the phase detector (PD) of the calibrator can detect f_{DF} by comparing the phase difference between $\phi_{OUT}[k]$ and $\phi_{OUT\_D}[k]$. Fig. 5.3(b) shows that, when f_{DF} exists, the phase error of S_{OUT} accumulates over the N cycles of the VCO's signal before the rising edge of S_{OUT} is realigned by that of S_{INJ}. At the moment of the injection ($k = 1$), the phase error of $\phi_{OUT}[k]$ is cleared by the injection, while $\phi_{OUT\_D}[k]$ still retains the previous phase error of $\phi_{OUT}[k]$. Thus, by observing $\phi_{PD}[1]$, which is the phase difference between $\phi_{OUT}[1]$ and $\phi_{OUT\_D}[1]$, the information of f_{DF} can be detected.

This first cause of f_{ERR} (i.e., f_{DF}) has been addressed by many conventional calibrators in [25] – [31], [77] – [81], although each of them used a different method, e.g., delay lines [25], [29], a time-to-digital converter (TDC) [15], and replica VCOs [19], [20], [78]. However, these frequency calibrators failed to completely remove f_{DF} because they had practical issues that limited the accuracy of the calibration, such as the mismatches of the delay cells in a delay line and the input offsets of a PD [25], [29], the

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

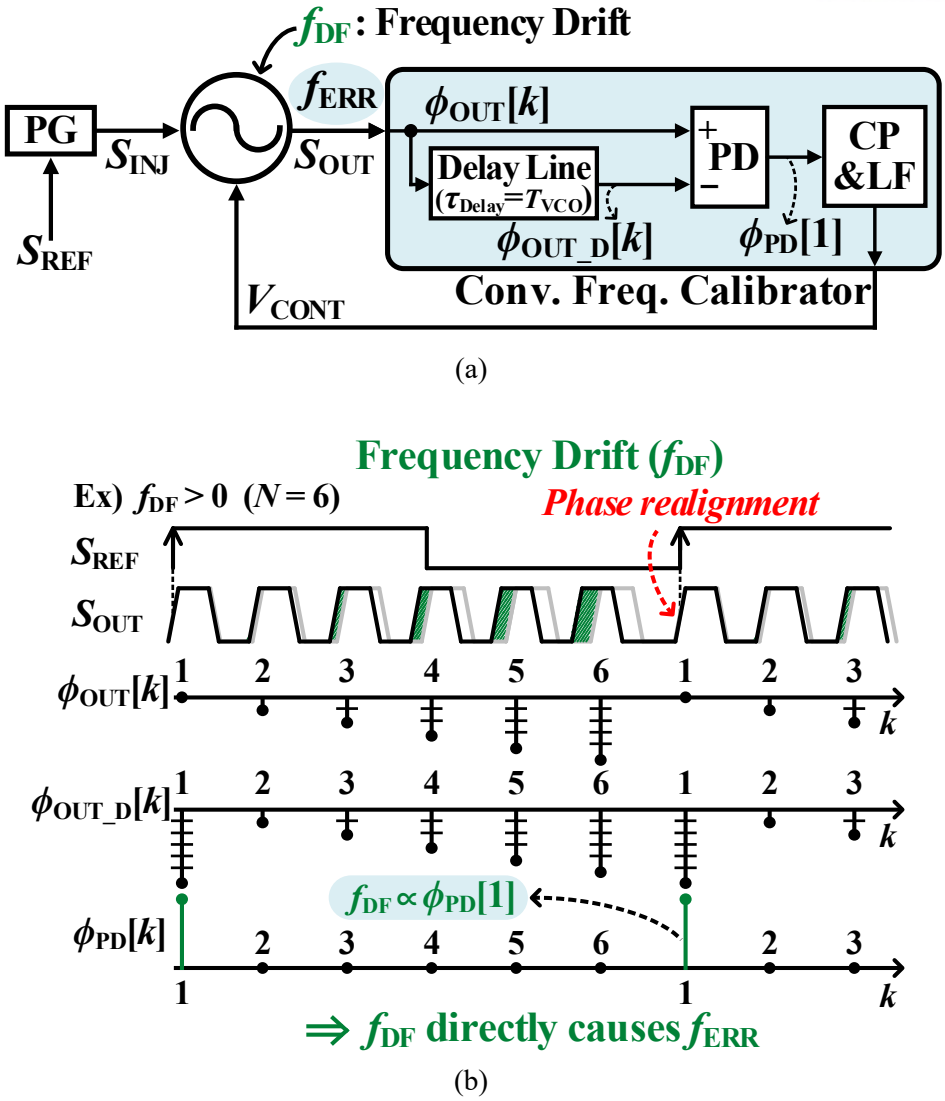
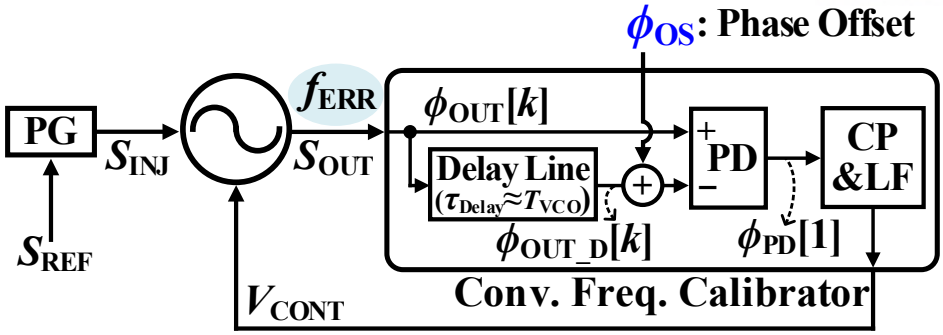


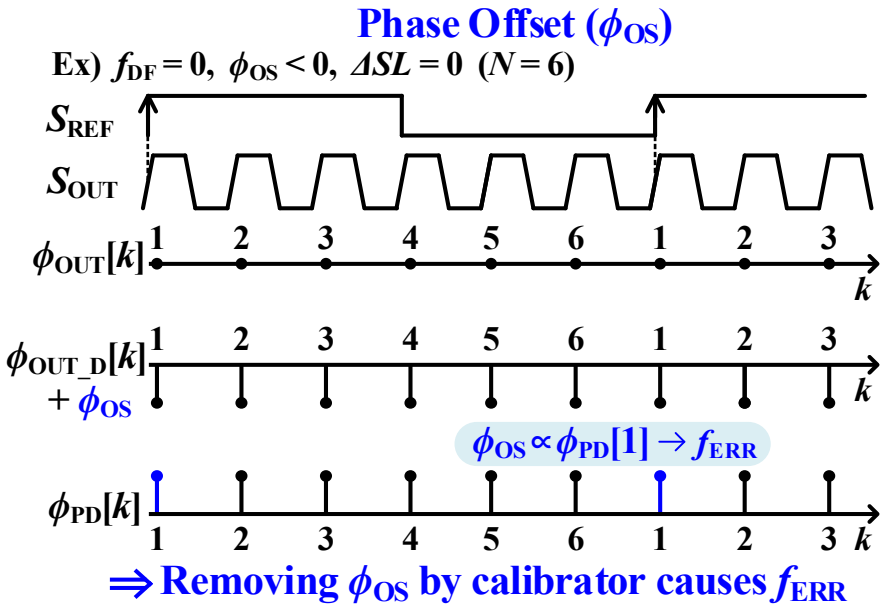
Figure 5.3. (a) First cause of f_{ERR} in ILCMs, i.e., *frequency drift*; (b) mechanism of the generation of f_{ERR} due to *frequency drift*.

limited resolution of the TDC [15], and the mismatches of replica VCOs and signal paths [19], [20], [78]. These systematic errors of the conventional frequency calibrators leave a remaining f_{ERR}, which generates the second cause, i.e., the *phase offset*, ϕ_{OS}. Figs. 5.4(a) and (b) show how ϕ_{OS} can generate f_{ERR} even when no f_{DF} exists. Specifically, in the case of using the calibrator in [29], the error in the delay time of the delay line, which is also varied due to supply and temperature variations, and the input offsets of the PD cause ϕ_{OS}. Then, as shown in Fig. 5.4(b), this ϕ_{OS} generates a constant phase error in $\phi_{PD}[k]$. In this case, the calibrator reacts as if this phase error were generated due to f_{DF}, even though it actually was caused by ϕ_{OS}. Due to this confusion, the calibrator will tune f_{VCO} to reduce the phase error, and the end result will be the generation of f_{ERR}.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

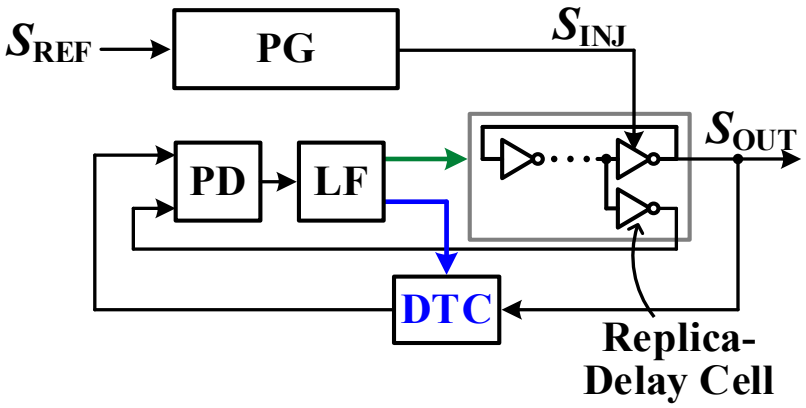


(a)



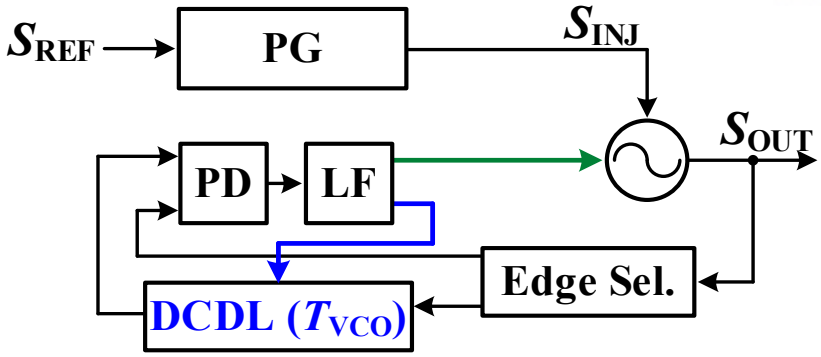
(b)

Figure 5.4. (a) Second of f_{ERR}, i.e., *phase offset,* in conventional frequency calibrators; (b) mechanisms of f_{ERR} generation due to *phase offset*.



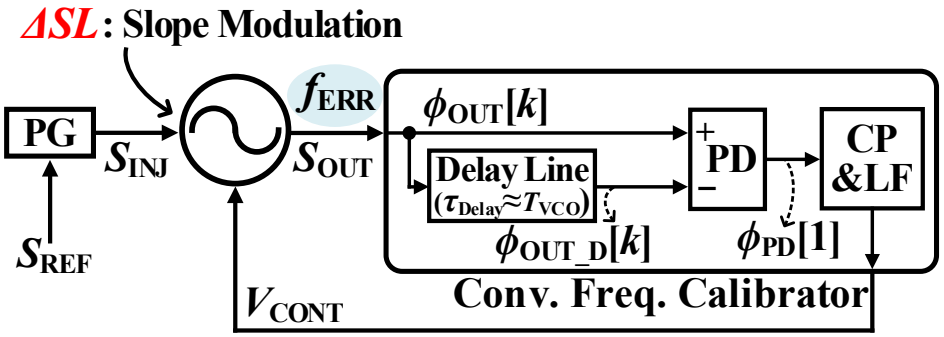
(a)

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

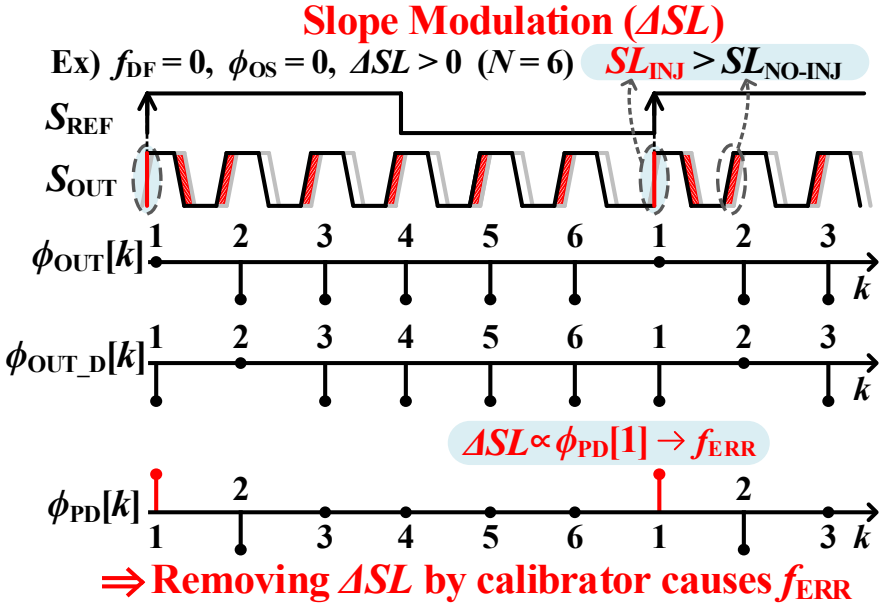


(b)

Figure 5.6. Conventional frequency calibrators for removing f_{DF} & ϕ_{OS} based on (a) DTC; and (b) DCDL.



(a)



(b)

Figure 5.5. (a) Third causes of f_{ERR}, i.e., *slope modulation,* in conventional frequency calibrators; (b) mechanisms of f_{ERR} generation due to *slope modulation*.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

More advanced ILCMs have been presented recently to remove f_{ERR} due to ϕ_{OS} as well. Fig. 5.5(a) shows the ILCM in [30] used an additional calibrating circuit to remove ϕ_{OS}, i.e., a digital-to-time converter (DTC). Fig. 5.5(b) shows the ILCM in [31] used an additional digitally-controlled delay line (DCDL) to remove ϕ_{OS} due to the input offsets of the PD and the mismatches between the two parallel signal paths. Despite the additional calibration efforts, they failed to reduce the reference spurs sufficiently e.g. less than −65 dBc. This is because, to date, none of the ILCMs has taken into consideration the third cause, i.e., the *slope modulation* of the edges of the output signal, that occurs due to the periodic injection of reference signals. Figs. 5.6(a) and (c) show how the *slope modulation* generates f_{ERR}. (We assumed that there is no f_{ERR} due to either f_{DF} or ϕ_{OS}.) When the injection of S_{INJ} is strong, the slope of the rising edges of S_{OUT}, i.e., SL_{INJ}, could be steeper than that of the original edges, i.e., $SL_{NO\text{-}INJ}$, by ΔSL. These steeper rising edges due to this *slope modulation* cause the positions of subsequent rising edges to be shifted forward, ultimately causing the phase error in $\phi_{PD}[1]$. Then, the calibrator would try again to adjust f_{VCO} to remove the error in $\phi_{PD}[1]$, which generates f_{ERR} and, eventually, prevents the ILCMs from achieving the minimum level of the reference spur.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

5.2.2. How Slope Modulation Generates Phase Error and thus Frequency Error

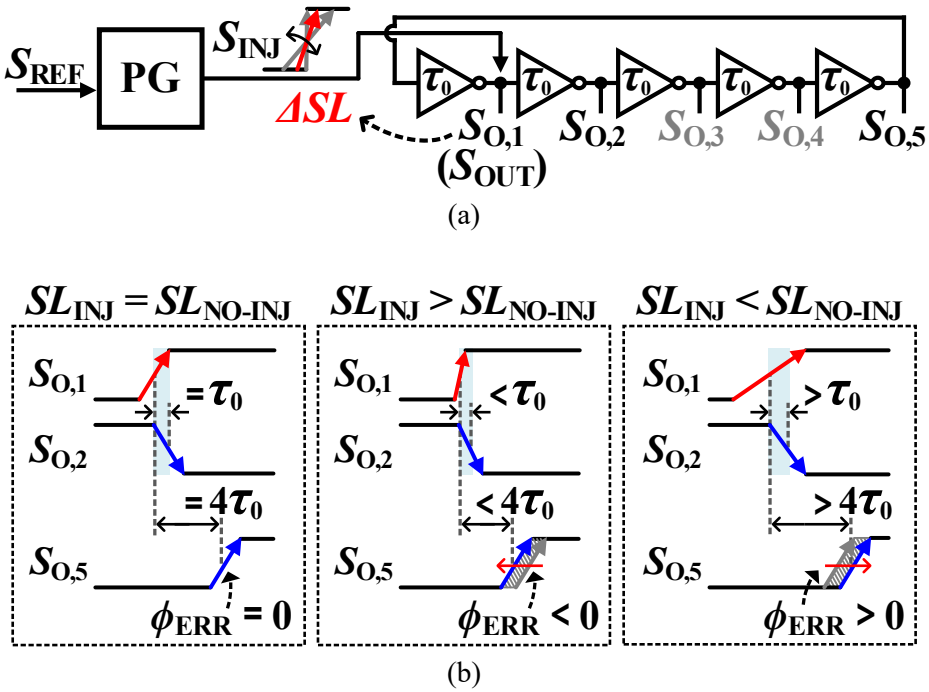
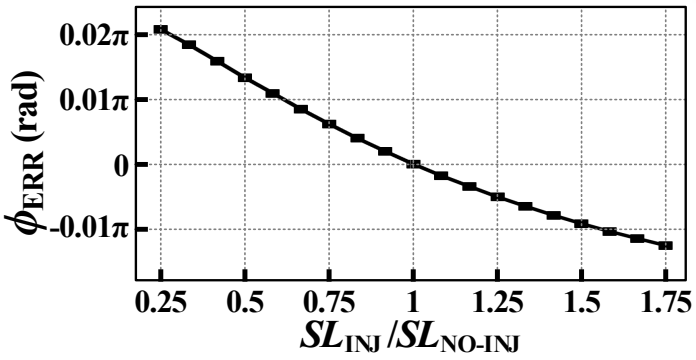


Figure 5.7. Mechanism of the *slope modulation* generating phase shift in S_{OUT} (a) five-stage ring VCO having the injection of S_{INJ}; (b) difference in slopes fades after a chain of inverters, but the phase shift remains.

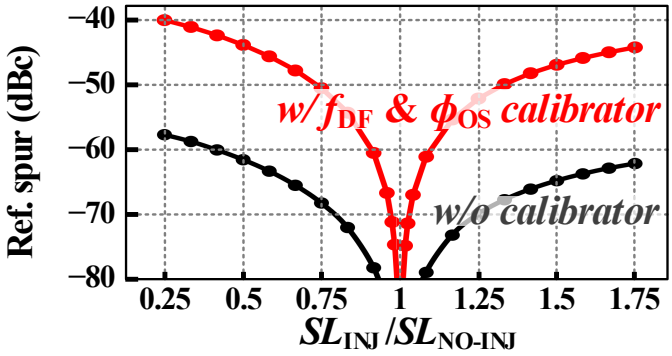
Figs. 5.7(a) and (b) show how phase error is generated by the *slope modulation* in ILCMs. Fig. 5.7(a) shows that S_{INJ} with a variable SL_{INJ} is injected to a ring VCO consisting of five delay cells, each of which has a unit delay, τ_0. Fig. 5.7(b) shows that the change in SL_{INJ} changes the propagation delay of an inverter chain [83]. When SL_{INJ} is the same as $SL_{NO\text{-}INJ}$, the total delay time after passing four delay cells is $4\tau_0$ at $S_{O,5}$, since the injection of S_{INJ} does not change the delay of the second inverter, D_2, (i.e., still τ_0). However, when SL_{INJ} is greater than $SL_{NO\text{-}INJ}$, the magnitude of the current of D_2 increases as the slope of the entering edge of $S_{O,1}$ is steeper, making the falling edge of $S_{O,2}$ fall faster. Thus, due to the reduction of the delay of D_2, the total delay time of the inverter chain becomes less than $4\tau_0$. On the contrary, when SL_{INJ} is less than $SL_{NO\text{-}INJ}$, the reduced current of D_2 makes the falling edge slower and extends the delay. As a result, the total propagation delay becomes more than $4\tau_0$. In summary, as shown in Fig. 5.7(b), even though the change in the slope of the inverters fades at $S_{O,5}$ after passing through an inverter chain, the change in the propagation delay remains as a static phase shift.

Fig. 5.8(a) shows the simulation result of the amount of the phase shift over the different ratios of SL_{INJ} to $SL_{NO\text{-}INJ}$. In this simulation, f_{DF} and ϕ_{OS} were assumed to be zero (i.e., only the effect of the *slope*

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(a)



(b)

Figure 5.8. (a) Simulated phase shifts due to the *slope modulation* assuming neither f_{DF} nor ϕ_{OS} without any calibrators; (b) simulated reference spur with a calibrator removing f_{DF} and ϕ_{OS} (red) or without any calibrators (black).

modulation was considered), and f_{REF} and f_{VCO} were 100 MHz and 2.4 GHz, respectively. According to the simulation, the absolute value of the phase shift increased almost linearly as the ratio of SL_{INJ} to $SL_{NO\text{-}INJ}$ deviated from one, and this result corresponded well with the analysis in [83]. The black dotted line in Fig. 5.8(b) shows the simulation result of the level of the reference spur when the same conditions as Fig. 4(a) were applied without the use of any calibrators. As the ratio of SL_{INJ} to $SL_{NO\text{-}INJ}$ deviated from one, the level of the reference spur increased, following a logarithmic line. In Fig. 4(b), the red dotted line represents the level of the reference spur when a conventional calibrator that can remove f_{DF} and ϕ_{OS} was used to remove ΔSL. Paradoxically, according to the simulation result, when a conventional calibrator was used, the level of the reference spur increased even more significantly. When the ratio of SL_{INJ} to $SL_{NO\text{-}INJ}$ changed from 0.99 to 0.75, the degradation in the reference spur was more than 25 dB. This result occurred because the use of a conventional frequency calibrator generated a significant f_{ERR} when the phase shift due to the *slope modulation* existed. Since the conventional calibrator tried to remove the phase shift due to the *slope modulation* by adjusting f_{VCO} (as shown in Fig. 5.6(b)), instead it generated an f_{ERR}, resulting in a significant increase in the reference spur. This result strongly

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

supported the claim that, to solve the problem of the reference spur fundamentally, ILCMs must be equipped with a more versatile calibrator that can correct the *slope modulation* as well as the *frequency drift* and the *phase offset*.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

5.3. ILCM Using the Proposed Background TP-FPSC

5.3.1. Overall Architecture of the ILCM with the Background TP-FPSC

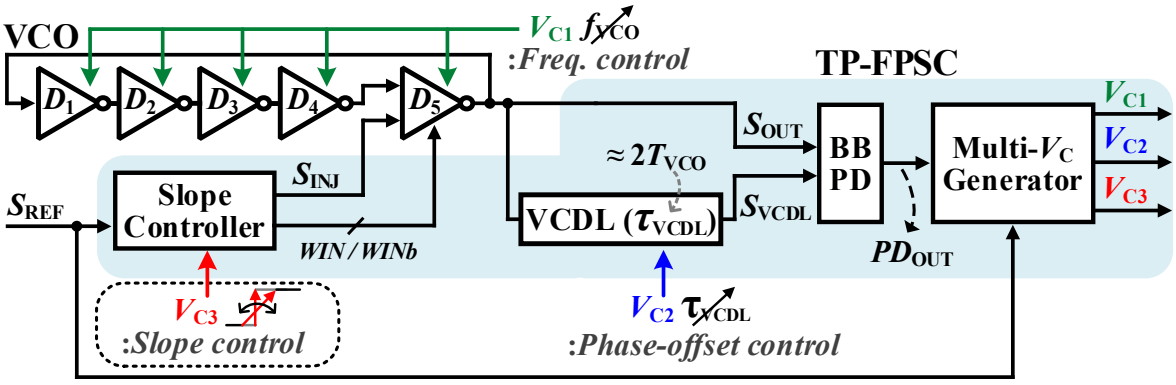


Figure 5.9. Overall architecture of the proposed ILCM with the triple-point frequency/phase/slope calibrator (TP-FPSC).

To remove the all three root causes of f_{ERR}, i.e., the *frequency drift*, the *phase offset*, and the *slope modulation*, we proposed the TP-FPSC. By including a slope controller, the TP-FPSC can keep adjusting the slope of the edges of S_{INJ} so that all edges of S_{OUT} can maintain the same slope in any conditions. Since the slope of the edges of S_{INJ} is adjusted such that the injection does not cause any phase distortions, the slope controller can address any other minor causes of phase errors that are related to the injection of S_{INJ}, such as charge injection, clock feedthrough, and substrate coupling, which cannot have been corrected by conventional calibrators.

Fig. 5.9 shows the overall architecture of the proposed ILCM, designed with a five-stage ring VCO. To ensure low reference spur as well as low RMS jitter, it is equipped with the proposed TP-FPSC (in blue background), which consists of a voltage-controlled delay line (VCDL), a bang-bang PD (BBPD), a multi-control-voltage (V_C) generator (MVG), and the slope controller. The TP-FPSC generates three independent V_Cs, each of which is delivered to a different target circuit and used for one of the three orthogonal calibration mechanisms. First, V_{C1} is used for the VCO to make f_{VCO} close to $N{\cdot}f_{REF}$, thereby removing the *frequency drift*. Second, V_{C2} is used for the VCDL, which generates S_{VCDL} by delaying S_{OUT} by τ_{VCDL}. According to V_{C2}, τ_{VCDL} is adjusted to be near $2T_{VCO}$, where T_{VCO} is the reciprocal of f_{VCO}. During this process, the *phase offset* from any systematic errors, such as the input offsets of the PD and the mismatches between the two signal paths to the PD, also can be cancelled. Third, most importantly, V_{C3} is used for the slope controller to equalize the slopes of S_{OUT}, either when S_{INJ} is injected or not, so that the *slope modulation* is eliminated.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

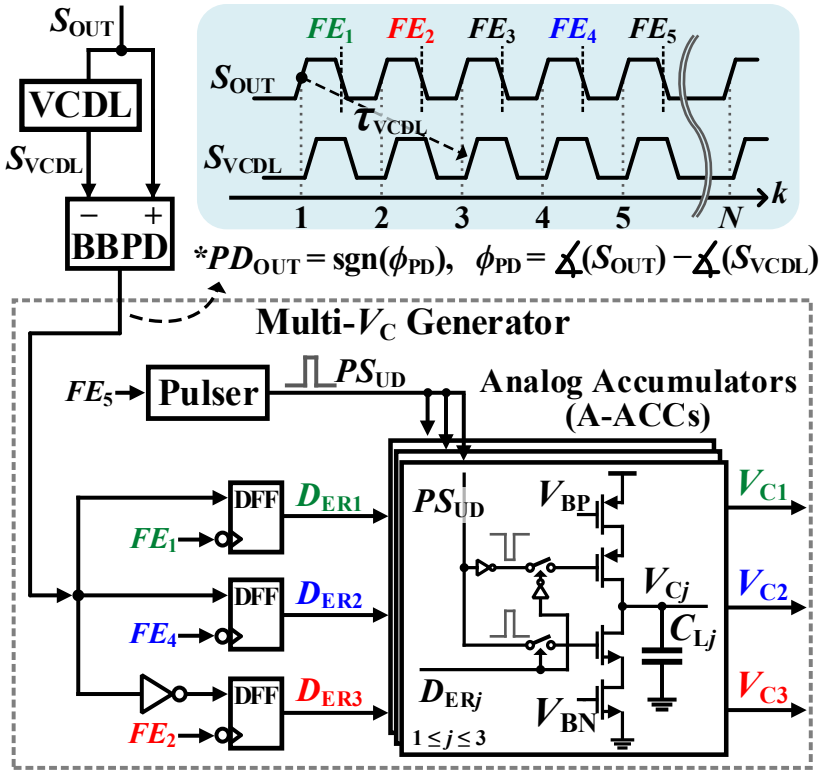
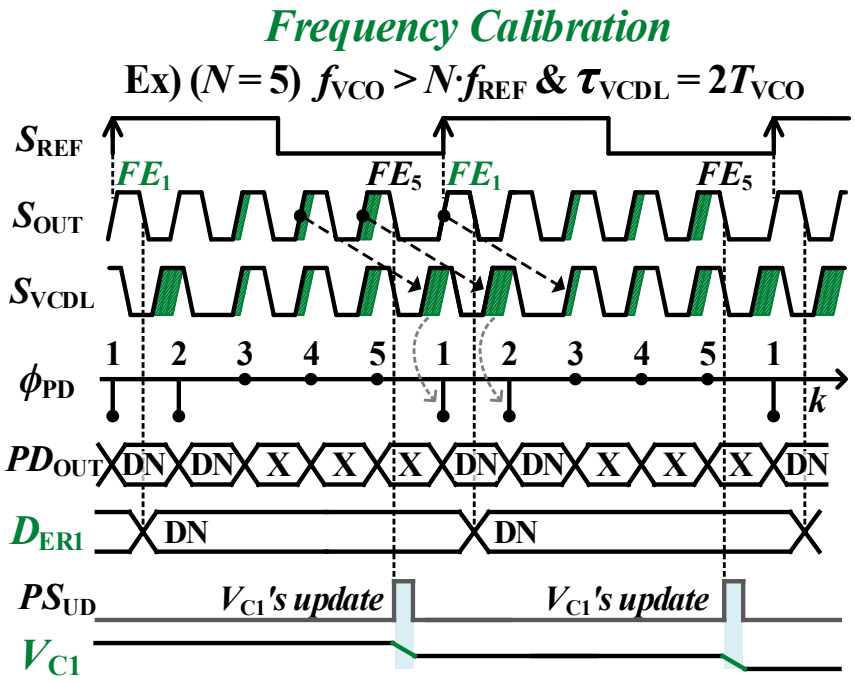


Figure 5.10. Implementation of TP-FPSC.

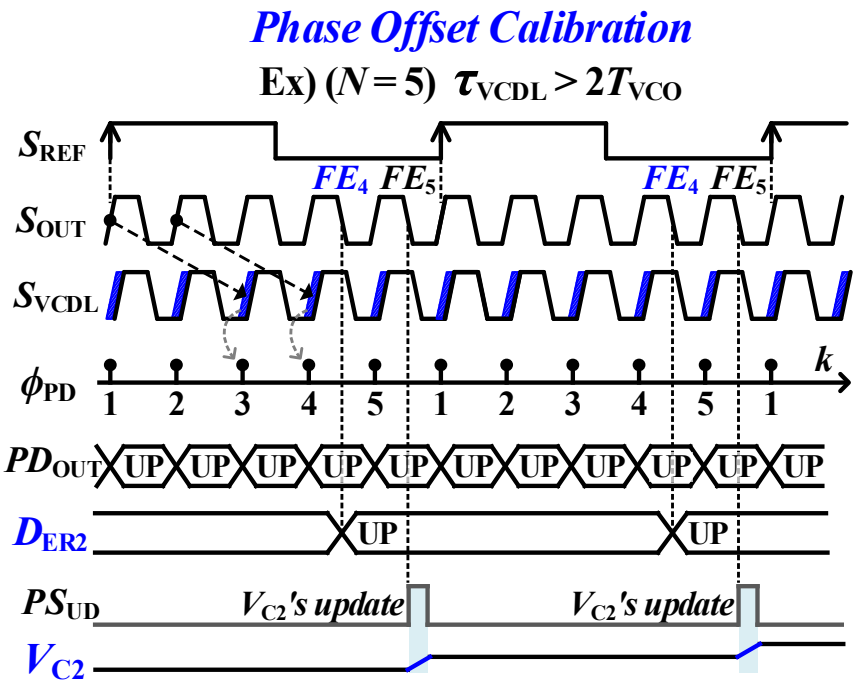
Fig. 5.10 shows that the TP-FPSC uses one bang-bang PD (BBPD) to extract all information required for the three orthogonal calibrations. The PD detects the phase difference, ϕ_{PD}, between the two input signals, i.e., S_{OUT} and S_{VCDL}. Then, it provides the MVG with its one-bit output, PD_{OUT}, having the polarity information of ϕ_{PD}. The MVG includes three D-flip-flops (DFFs) to sample PD_{OUT} from the PD sequentially at different timings, so that three sets of independent information can be extracted from the same output, i.e., PD_{OUT}. In the timing diagram in Fig. 5.10, FE_k ($1 \le k \le N$) represents the k^{th} falling edge of S_{OUT} after the injection of S_{INJ}. Following this notation, PD_{OUT} is sampled sequentially at FE_1, FE_4, and FE_2 by the three DFFs of the MVG, generating three corresponding one-bit error codes, D_{ER1}, D_{ER2}, and D_{ER3}, respectively. Each of these three error codes, D_{ERj}, enters the j^{th} analog accumulator (A-ACC) and determines whether charges will be sourced to or extracted from the loop capacitor C_{Lj}. Finally, all three V_{Cj}s are updated concurrently during a short pulse, PS_{UD}, which is created from FE_5 by the pulser. Whereas, to achieve a high resolution, typical digital accumulators require a large number of bits or a delta-sigma modulator (DSM), the proposed A-ACC easily can enhance the resolution just by decreasing the pulse width of PS_{UD}. Different from conventional charge pumps, the pulse width of PS_{UD} is fixed so that the digital information from the BBPD is accumulated in C_{Lj} in a discrete manner.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

5.3.2. Three Error Detection Mechanisms of the TP-FPSC

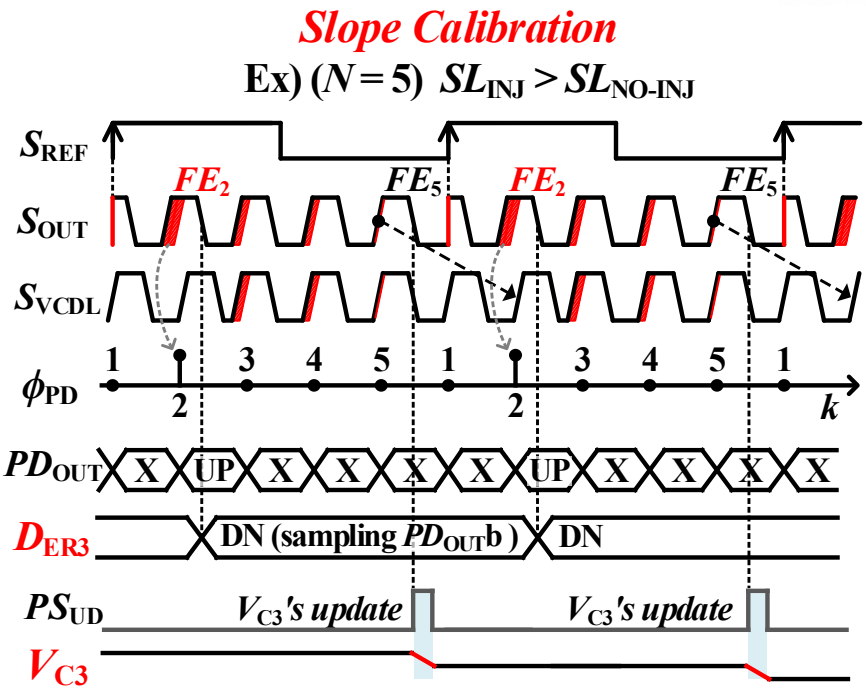


(a)



(b)

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(c)

Figure 5.11. Three causes detection mechanisms of the TP-FPSC; (a) *frequency drift*, (b) *phase offset*, and (c) *slope modulation*.

Figs. 5.11(a) – (c) show how these three causes of f_{ERR}, i.e., the *frequency drift*, the *phase offset*, and the *slope modulation*, can be detected at PD_{OUT}. For easy understanding by simplifying situations, the value of N is assumed to be five. We also assume each case of Figs. 5.11(a) – (c) includes only a single cause at a time. This latter assumption is valid, since the three causes of f_{ERR} are orthogonal one another. First, Fig. 5.11(a) shows how the *frequency drift* can be detected, when f_{VCO} is higher than $N \cdot f_{REF}$ so that f_{ERR} is positive, whereas τ_{VCDL} is $2T_{VCO}$ and SL_{INJ} is equal to $S_{NO\text{-}INJ}$. In this case, the effect of the *frequency drift* of f_{VCO} appears in ϕ_{PD}, when the first rising edges of S_{OUT} and S_{VCDL} or the second rising edges of S_{OUT} and S_{VCDL} are compared by the PD. This is because S_{VCDL} is the $2T_{VCO}$-delayed version of S_{OUT} since τ_{VCDL} is fixed at $2T_{VCO}$. In the implementation, we used FE_1 to sample PD_{OUT}, which generates D_{ER1}. Second, Fig. 5.11(b) shows the detection of the *phase offsets*, when τ_{VCDL} is larger than $2T_{VCO}$ while f_{ERR} is zero and SL_{INJ} is equal to $S_{NO\text{-}INJ}$. In this situation, since τ_{VCDL} is deviated from $2T_{VCO}$ due to any static errors of the frequency calibrator, ϕ_{PD} becomes constant for all rising edges of S_{OUT} and S_{VCDL}. In this work, we used FE_4 to sample PD_{OUT}, which generates D_{ER2}. Third, Fig. 5.11(c) shows how the *slope modulation* can be detected, when SL_{INJ} differs from $S_{NO\text{-}INJ}$. After the two foregoing calibrations are done, f_{ERR} is not completely removed due to the *slope modulation*. The effect of this *slope modulation* is detected by sampling PD_{OUT} by FE_2. PD_{OUT} sampled by FE_2 also could include a little information of the *frequency drift*. However, since the *frequency calibration* was designed to have

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

a much wider bandwidth, (which is discussed later in Section 5.3.3) the *frequency drift* is supposed to be removed earlier by V_{C1}; thus, we consider that almost all phase error at PD_{OUT} at the moment of FE_2 is due to the *slope modulation*. As mentioned at the beginning of Section 5.3.1, this mechanism also can detect any phase errors, occurring due to the injection of S_{INJ}, such as charge injection, clock feedthrough, and substrate coupling.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

5.3.3. Settling Behaviors of Three Calibrations of the TP-FPSC

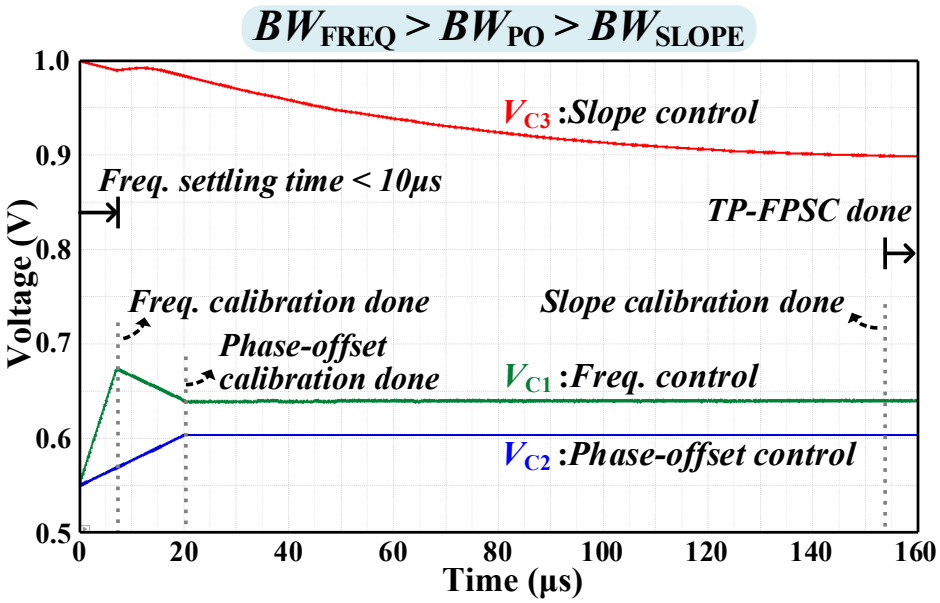


Figure 5.12. The settling behaviors of three control voltages in the TP-FPSC.

In the timing diagrams in Fig. 5.11(a) – (c), for easy explanation, we assume each of the three cause to be singled out. However, their effects would be mingled one another in real situations, and the three calibrations would proceed concurrently. Fig. 5.12 shows the simulation results of the settling of the three control voltages. To secure the stability, we designed differently each bandwidths of the three calibrating loops, resulting in different settling speeds of V_{C1}, V_{C2}, and V_{C3}. Since the *frequency calibration* has the largest loop bandwidth, V_{C1} settles the first. At this moment, S_{OUT} already can have an ultra-low jitter, but it cannot have a low reference spur yet, because the other two root causes of f_{ERR} still remain. Since the *phase-offset calibration* has the second largest bandwidth, V_{C2} settles the next. V_{C3} settles the last since the *slope calibration* has the smallest bandwidth. After the settlement of V_{C3}, finally, the ILCM can achieve both a low reference spur and a low jitter. The bandwidth of the *frequency calibration* was designed to be ten times larger than that of the *phase-offset calibration*. The bandwidth of the *slope calibration* was designed to be one tenth of that of the *phase-offset calibration*. Since the bandwidths of the three calibrating loops were designed such different, the proposed architecture can secure the stability. As shown in Fig. 5.12, the *frequency calibration* finishes in less than 10 μs so that the ILCM can start generating the accurate output frequency very shortly.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

5.4. Design of Sub-Building Blocks: Slope Controller, VCO, and VCDL

Fig. 5.13(a) shows the schematics of the slope controller. The slope controller consists of three current-starved inverters, a NAND gate, and simple inverters, and it can control the slope of S_{INJ} simply by adjusting the bias voltage, V_{C3}, of the tail transistors of the three current-starved inverters. The delay between S_{REF} and S_{INJ}, which is generated by the slope controller is very small, thereby causing just negligible impact on RMS jitter. Fig. 5. 13(b) shows the ring VCO following the slope controller consists of five-stage delay cells, each of which has a capacitor bank, C_{BANK1}, digitally controlled by $COARSE_1$ and a varactor, C_{VAR1}, continuously adjusted by V_{C1} from the TP-FPSC. Each delay cell is based on an inverter having two input ports, IN_{VCO} and $\overline{IN_{INJ}}$, either of which is activated according to control signals entering two ports, $\overline{EN_{VCO}}$ and $\overline{EN_{INJ}}$. As shown in Fig. 5.13(b), for the first delay cell of the VCO, its IN_{VCO} and $\overline{IN_{INJ}}$ ports are connected to the output of the last delay cell and S_{INJ}, respectively. However, for other four delay cells, $\overline{IN_{INJ}}$ port is fixed at '1', whereas IN_{VCO} port is connected to its previous delay cell. Therefore, these four delay cells always receive the output signals of their previous delay cells as the inputs, and, for doing this, their $\overline{EN_{VCO}}$ and $\overline{EN_{INJ}}$ ports are also fixed at '0' and '1', respectively. As shown in timing diagram of Fig. 5.13(a), the two control signals, i.e., *WIN* and *WINb*, for activating either of the two input ports of the first delay cell are generated by the slope controller using S_A and S_B. Since S_A and S_B are generated before and after S_{INJ}, respectively, they can enclose S_{INJ} safely irrespective of PVT-variations. When $WIN = 0$ and $WINb = 1$, the first delay cell receives the output of the previous delay cell; thus, the VCO is free-running. On the other hand, when $WIN = 1$ and $WINb = 0$, the delay cell receives S_{INJ}, of which the slope has been already adjusted by the slope controller to be the same as that of the output signal of the free-running VCO. Fig. 5.13(c) shows the schematics of the VCDL consisting of an inverter chain. To change the amount of delay, a capacitor bank, C_{BANK2}, at the output of each inverter is controlled by $COARSE_2$ and a varactor, C_{VAR2}, is adjusted by V_{C2}. The buffer was used to reduce the loading and coupling effects to the VCO from the VCDL.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

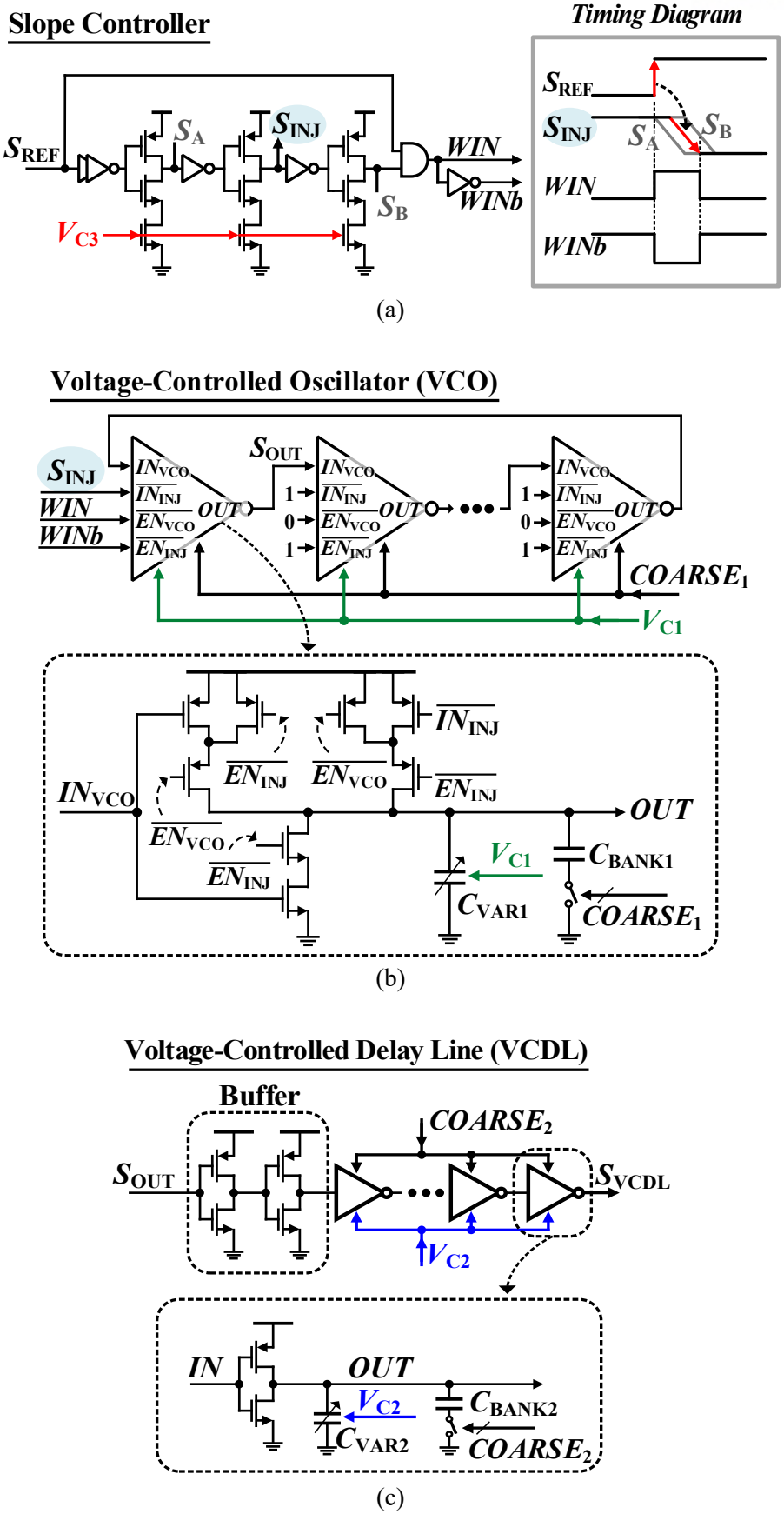
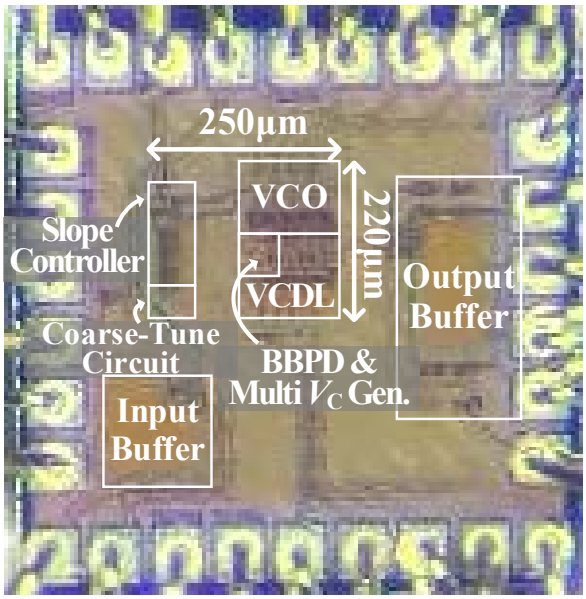


Figure 5.13. Schematics of (a) slope controller, (b) VCO, and (c) VCDL.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

5.5. Experimental Results



(a)

Power Consumption (mW)	
Ring VCO	7.5
VCDL	3.0
PG & BBPD & Multi-V_C Generator	0.5
Total	11.0

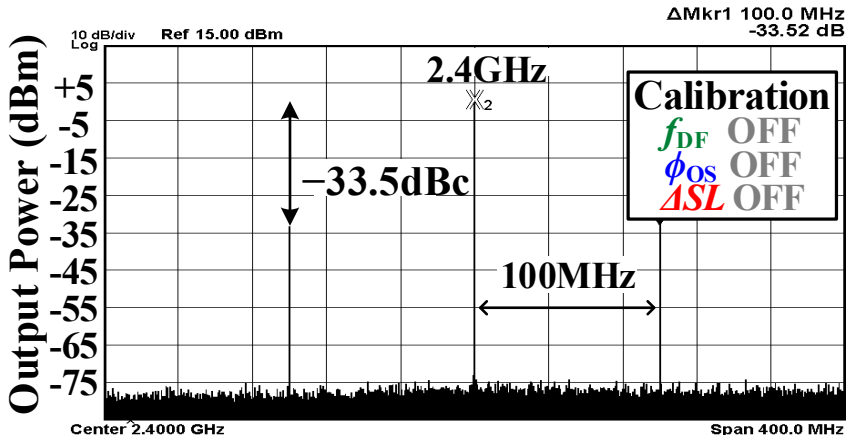
(b)

Figure 5.14. (a) Die photograph. (b) Power-breakdown table.

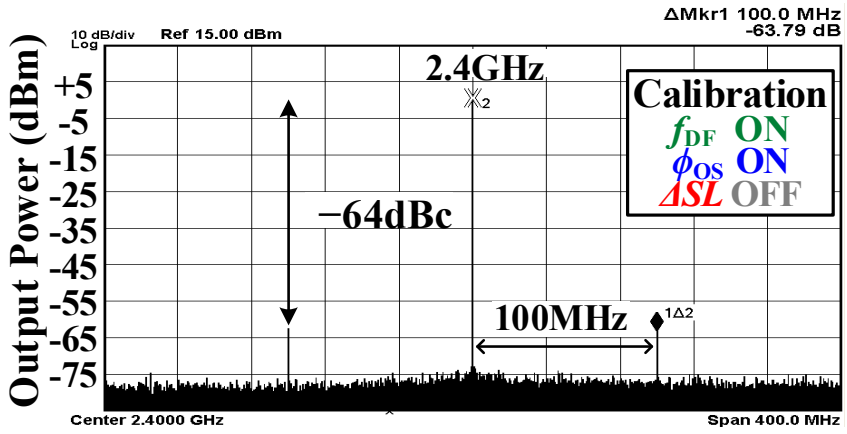
Fig. 5.14(a) shows the micrograph of this ILCM, fabricated in a 65-nm CMOS technology. The active area of the ILCM was 0.055 mm^2. Fig. 5.14(b) shows that the total power consumption was 11.0 mW from a 1.1-V supply; the ring VCO, the VCDL, and other building circuits (including the PG, the BBPD, and the MVG) consumed 7.5, 3.0, and 0.5 mW, respectively. Figs. 5.15(a) – (c) show the measured spectrums of the 2.4-GHz output signal of the ILCM (f_{REF} = 100 MHz and N = 24) for different configurations of the proposed TP-FPSC. First, Fig. 5.15(a) shows the spectrum, when all three functions of the TP-FPSC were completely turned off. (The frequency of the VCO was manually adjusted to achieve the injection locking.) In this situation, the output signal of the ILCM were prone to all three causes of the frequency error; thus, the measured level of the reference spur was high as approximately −33 dBc. Second, Fig. 5.15(b) shows the spectrum, when two functions of the TP-FPSC, i.e., *frequency calibration* and the *phase-offset calibration*, were turned on, so the level of the reference spur was decreased to −64 dBc. Finally, when all three functions including the *slope calibration* were turned on, all three root causes of the frequency error were removed, and the level of the reference spur was reduced to −72 dBc, as shown in Fig. 5.15(c). Fig. 5.15(d) shows the measured spectrum of the 2.5-GHz output signal, when all three functions of the TP-FPSC were turned on. The level of the reference spur was −72.9 dBc. Fig. 5.16 show the levels of the reference spur across different output frequencies measured from five different chips. To sweep output frequency, N changed from 22 to 25, while f_{REF} was fixed as 100 MHz. These measurement results show that the levels of the reference spurs

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

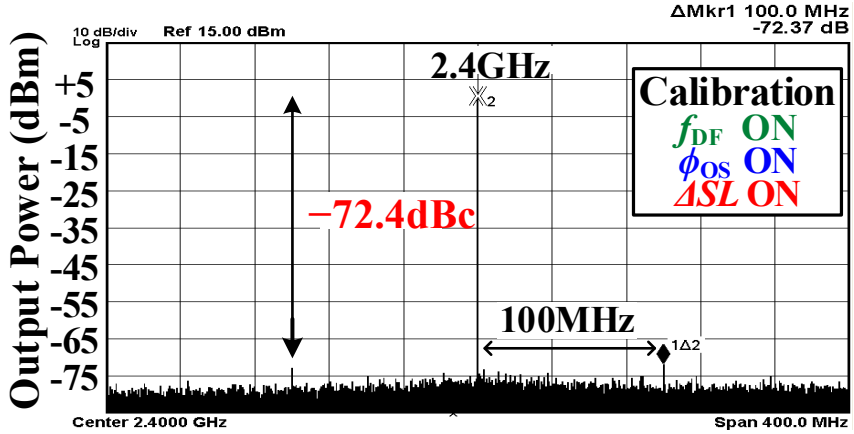
were constantly regulated to less than −70 dBc over different output frequencies and five different chips.



(a)

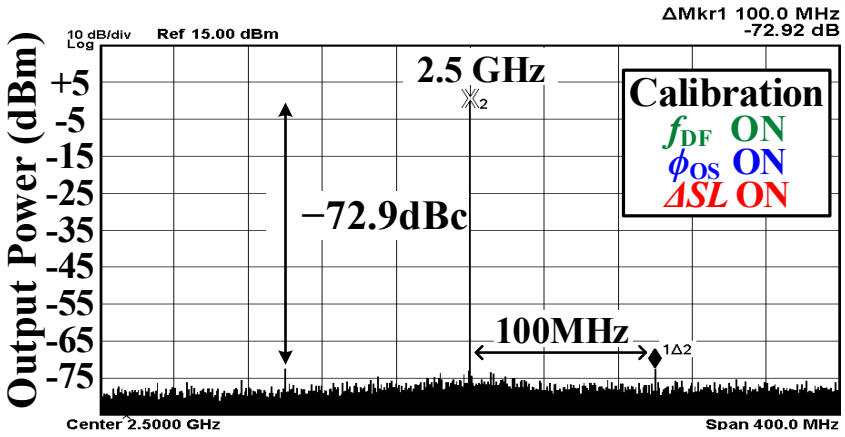


(b)



(c)

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY



(d)

Figure 5.15. Measured spectrum of the output signal with a frequency of 2.4 GHz, when (a) TP-FPSC was turned off, (b) f_{DF} and ϕ_{OS} calibrations were turned on, but ΔSL calibration was turned off, (c) TP-FPSC was fully turned on. (d) Measured spectrum of the output signal with 2.5 GHz.

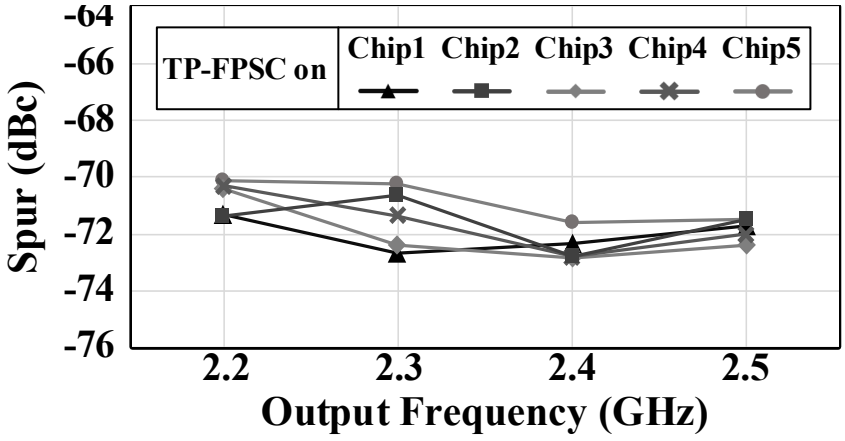
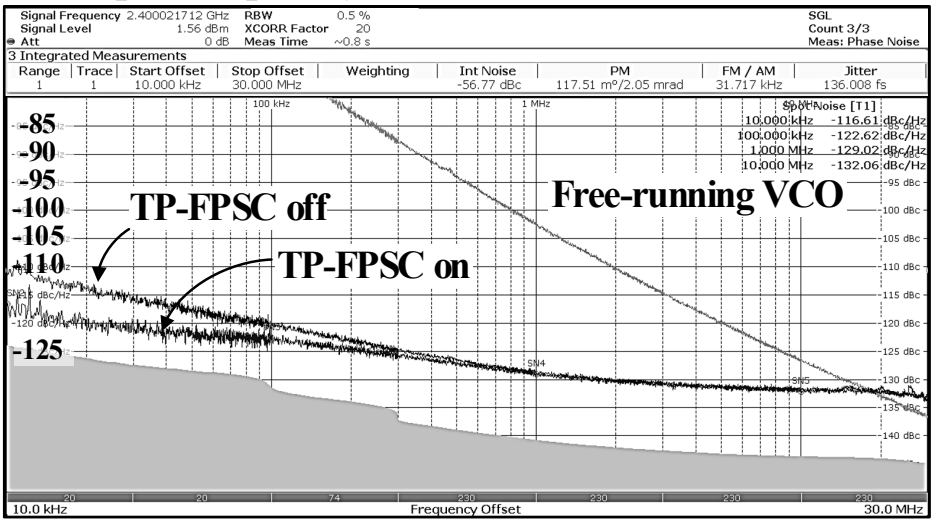


Figure 5.16. Variations of reference spurs over output frequencies in five different sample chips.

Figs. 5.17(a) and (b) show the measured phase noises of the output signal at 2.4 and 2.5 GHz, respectively, when the 100-MHz reference clock was used. Since the injection-locking mechanism had a very wide bandwidth, when the reference clock was injected, the phase noises of the ring VCO were suppressed greatly at both frequencies. When the TP-FPSC was turned on, the wide bandwidth of the *frequency calibration* provided an additional suppression to the in-band phase noise of the VCO, so that the ILCM was able to achieve an ultra-low jitter. The RMS jitters, integrated from 10 kHz to 30 MHz, were approximately 136 fs at both frequencies, i.e., 2.4 and 2.5 GHz. At both output frequencies commonly, the spot noises at 100 kHz and 1 MHz were −122 and −129 dBc/Hz, respectively. Fig. 5.18 shows that this low-jitter performance was maintained robustly across the output frequencies ranging from 2.2 to 2.5 GHz in all five different chips.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Output frequency = 2.4GHz, Jitter$_{RMS}$ = 136.0fs

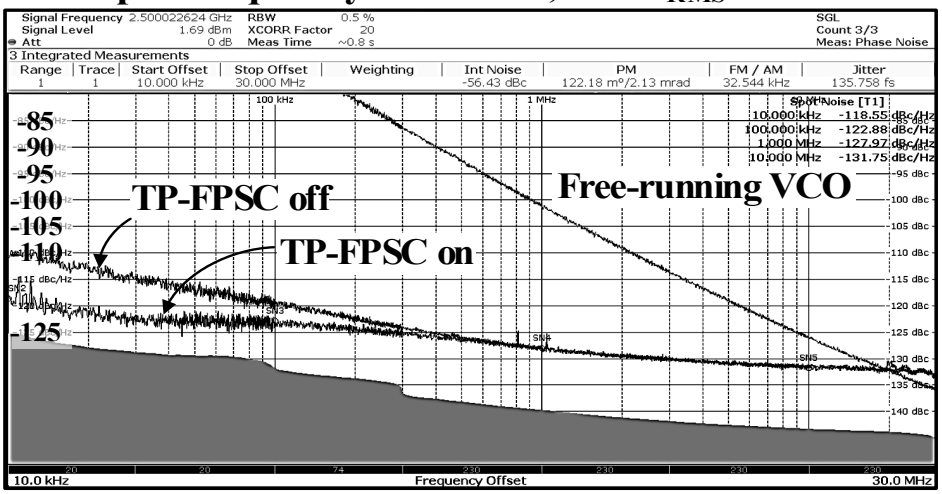


10k 100k 1M 10M 30M

Offset Frequency (Hz)

(a)

Output frequency = 2.5GHz, Jitter$_{RMS}$ = 135.8fs



10k 100k 1M 10M 30M

Offset Frequency (Hz)

(b)

Figure 5.17. Measured phase noise, when the TP-FPSC was turned on and off at (a) 2.4 GHz and; (b) 2.5 GHz.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

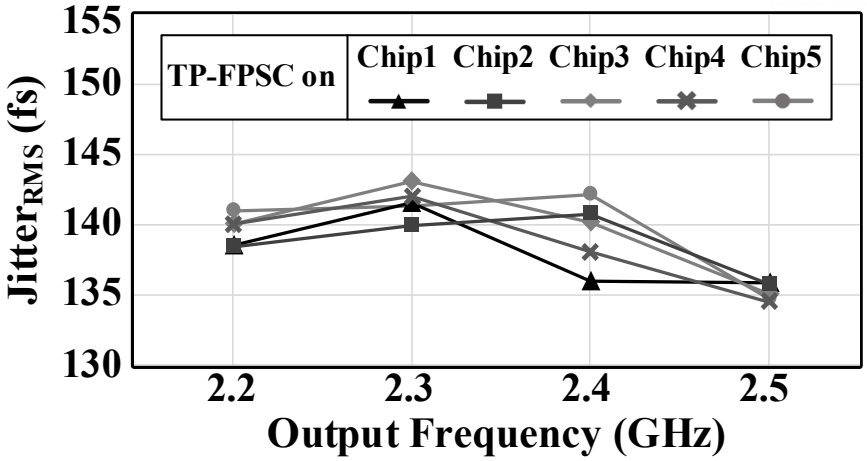


Figure 5.18. Variations of integrated RMS-jitter over output frequencies in five different sample chips.

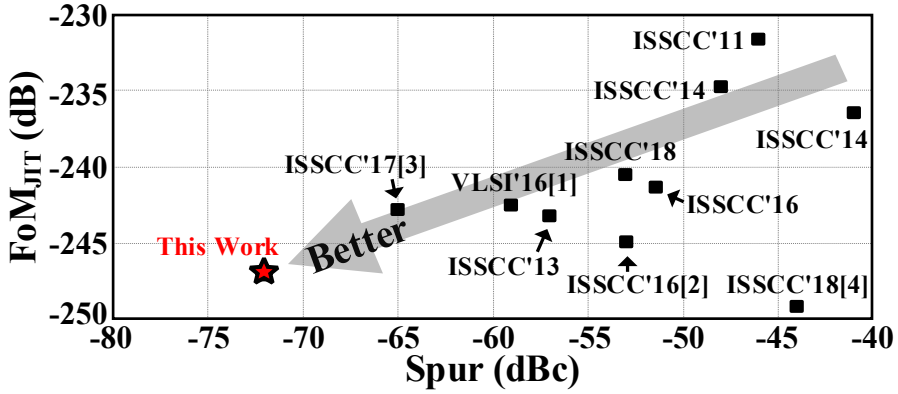


Figure 5.19. Benchmark of performances of this work and state-of-the-art ring-VCO-based ILCMs.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Table 3 Comparison with Ring-VCO-Based ILCMs

	This work	JSSC'16 [29] S. Choi	ISSCC'17 [77] H. C. Ngo	JSSC'19 [80] D. Coombs	ISSCC'17 [30] S. Kim	JSSC'19 [81] K.M. Megawer	JSSC'19 [31] S. Yang
Process (CMOS)	65 nm	65 nm	65 nm	65 nm	65 nm	65 nm	28 nm
Calibrator	Frequency/ Offset/ Slope	Frequency	Frequency	Frequency/ Offset	Frequency/ Offset	Frequency/ Offset	Frequency/ Offset
Out. freq., f_O (GHz)	2.4 (2.2 – 2.5)	1.2	0.9 (0.52 – 1.15)	5.0 (2.5 – 5.75)	2.5	4.752 (2.6 – 5.2)	3.0 (1.55 – 3.35)
Ref. freq., f_{REF} (MHz)	100	120	150	125	156.25	54	200
1MHz PN (dBc/Hz) @ f_O (GHz)	–129.0 @ 2.4	–134.4 @ 1.2	–124.0 @ 0.9	–115.9 @ 5.0	-	–113.7 @ 4.752	–118.0 @ 3.0
Ref. spur, L_{spur} (dBc)	–72	–53	N/A	–45	–65	–53	–44
Out. jitter$_{RMS}$,σ_t (fs) (Integ. Range)	140 (10k – 30MHz)	185 (10k – 40MHz)	420 (10k – 10MHz)	340 (10k – 40MHz)	198 -	370 (10k – 30MHz)	292 (10k – 40MHz)
Total jitter$_{RMS}$,σ_{tot} (fs) ($=\sqrt{(\sigma_t^2 + {*}\sigma_{spur}^2)}$)	142	459	N/A	424	204	385	556
Power, P_{DC} (mW)	11.0	9.5	3.8	5.3	13.5	6.5	1.45
Active area (mm^2)	0.055	0.06	0.028	0.09	0.064	0.16	0.0056
**FoM$_{JIT}$ (dB)	–246.7	–244.9	–241.7	–242.4	–242.8	–240.5	–249.1
***FoM$_{JIT2}$ (dB)	–246.5	–237.0	N/A	–240.2	–242.5	–240.2	–243.5
****FoM$_{REF}$ (dB)	–246.7	–244.1	–240.0	–241.2	–240.8	–243.2	–246.1

*$\sigma_{spur} = 10^{L_{spur}/20}/\sqrt{2}\pi f_o$ **FoM$_{JIT}$: $10\log_{10}(\sigma_t^2 \cdot P_{DC}(\text{mW}))$ ***FoM$_{JIT2}$: $10\log_{10}(\sigma_{tot}^2 \cdot P_{DC}(\text{mW}))$ ****FoM$_{REF}$: $10\log_{10}(\sigma_t^2 \cdot P_{DC}(\text{mW}) \cdot \frac{f_{REF}}{100\text{MHz}})$ [84]

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

In Table 3, the performance of the proposed ILCM was compared with those of state-of-the-art ring-VCO-based ILCMs equipped with calibrators that were able to correct only the *frequency drift* or both the *frequency drift* and the *phase offset* to maintain the performance of the RMS jitter and the reference spur. The comparison table shows that the ILCM in this work can achieve not only the lowest RMS jitter but also the lowest reference spur by using the proposed TP-FPSC; thus, it achieved the excellent $\mathrm{FoM_{JIT}}$. The performance of this ILCM with the TP-FPSC is more conspicuous in the $\mathrm{FoM_{JIT2}}$, in which the noise power of the reference spur (outside the integration range) is included to calculate the RMS jitter. Having a much lower reference spur than others, this work achieved the $\mathrm{FoM_{JIT2}}$ that is at least 3 dB better than other ILCMs. Table 3 shows that this work also achieved the best $\mathrm{FoM_{REF}}$ [84], in which $\mathrm{FoM_{JIT}}$ is normalized to the value of f_{REF}. The benchmarking of the state-of-the-art ring-VCO-based ILCMs in Fig. 5.19 shows that this work is the first ring-VCO-based ILCM that concurrently has the reference spur less than −70 dBc and the $\mathrm{FoM_{JIT}}$ lower than −245 dB.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

5.6. Discussion

In this work, we presented a low-jitter and ultra-low reference spur ring-VCO-based ILCM**.** Using the TP-FPSC that can remove all three major causes generating the frequency errors, i.e., the *frequency drift*, the *phase offset*, and the *slope modulation*, the ILCM in this work can achieve a very low reference spur as well as an ultra-low RMS jitter. In addition, the calibration loop of the *frequency drift* was designed to have a wide bandwidth, which helps to further suppress the flicker noise of the ring VCO. The measured reference spur and RMS jitter of the 2.4-GHz output signal were −72 dBc and 136 fs, respectively, and their variations across output frequencies for five different samples were tightly regulated by the TP-FPSC**.** Consequently, the ILCM in this work can achieve and maintain both low reference spur and low RMS-jitter, while using a small amount of power and a compact silicon area.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Chapter 6.

Conclusion

This dissertation has focused mainly on the design of a frequency calibrator for the injection-locked frequency multiplier. Conventional calibrators were introduced, and the pros and cons of each calibrators were discussed in Chapter 2.

Chapter 3 presented a low power, compact area *LC*-tank-based frequency multiplier. By using input signals with a pulsed waveform to minimize the duration of the core current flow, the proposed architecture was able to reduce power consumption dramatically. With the *LC*-tank having a resonant frequency close to the target frequency, the signal component of the target harmonic was effectively amplified while other components were suppressed. AM spurs, caused by the damping of the signal due to the tank loss, were removed using the D-to-S amplifier. The proposed frequency tripler had a low power consumption of less than 1 mW and a compact silicon area of 0.08 mm^2. It also achieved excellent phase noise performance; the deviation from the theoretical bound was less than 0.5 dB.

In Chapter 4, we presented a PVT-insensitive and low-phase-noise mm-wave ILFM that used the proposed ultra-low-power FTL, which was capable of calibrating real-time frequency drifts. By monitoring the instantaneous distortion between the quadrature phases of the QVCO, caused when the frequency of the VCO deviates from the target frequency, the FTL can continuously track and correct the drifts of the frequency of the VCO due to environmental variations. Therefore, it can tightly regulate the degradation of phase noise. Since the proposed FTL monitors the averages of phase deviations rather than samples the instantaneous values, it uses only 600 μW to keep calibrating the mm-wave ILFM. The ILFM generated the output signal with a frequency ranging from 27.4 to 30.8 GHz. The 10-MHz phase noise of the 29.25-GHz output signal was −129.7 dBc/Hz, and its variations across temperatures and supply voltages were less than 2 dB. The IPN integrated from1 kHz to 100 MHz and the rms jitter were −39.1 dBc and 86 fs, respectively.

Chapter 5 presented a low-jitter and ultra-low reference spur ring-VCO-based ILCM**.** Using the TP-FPSC that can remove all three major causes generating the frequency errors, i.e., the *frequency drift*, the *phase offset*, and the *slope modulation*, the ILCM in this work can achieve a very low reference spur as well as an ultra-low RMS jitter. In addition, the calibration loop of the *frequency drift* was designed to have a wide bandwidth, which helps to further suppress the flicker noise of the ring VCO. The

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

measured reference spur and RMS jitter of the 2.4-GHz output signal were −72 dBc and 136 fs, respectively, and their variations across output frequencies for five different samples were tightly regulated by the TP-FPSC**.** Consequently, the ILCM in this work can achieve and maintain both low reference spur and low RMS-jitter, while using a small amount of power and a compact silicon area.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

References

[1] B. M. Helal, M. Z. Straayer, G. Wei, and M. H. Perrott, "A highly digital MDLL-based clock multiplier that leverages a self-scrambling time-to-digital converter to achieve subpicosecond jitter performance," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 855–863, Apr. 2008.

[2] T. Ali, A. Hafez, R. Drost, R. Ho, and C. Yang, "A 4.6 GHz MDLL with −46 dBc reference spur and aperture position tuning," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 466–468.

[3] R. Farjad-rad *et al*., "A0.2–2GHz12mWmultiplyingDLLforlow-jitter clock synthesis in highly-integrated data-communication chips," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 56–57.

[4] A. Elshazly, R. Inti, B. Young, and P. K. Hanumolu, "A 1.5 GHz 890 µW digital MDLL with 400 fs rms integrated jitter, –55.6 dBc reference spur and 20 fs/mV supply-noise sensitivity using 1b TDC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 242–243.

[5] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004

[6] B. M. Helal, C. Hsu, K. Johnson, and M. H. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391−1400, May. 2009.

[7] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.

[8] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 1539–1553, May 2009.

[9] E. Monaco, M. Pozzoni, F. Svelto, and A. Mazzanti, "Injection-locked CMOS frequency doublers for µ-wave and mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1565–1574, Aug. 2010.

[10] S. Lee, L. Wang, and Y. Lin, "A CMOS quadrature VCO with subharmonic and injection-locked techniques," *IEEE Trans. Circuits Syst. II Exp. Briefs*, vol. 57, no. 11, pp. 843–847, Nov. 2010.

[11] J. Chien *et al*., "A pulse-position-modulation phase-noise-reduction technique for a 2-to-16GHz injection-locked ring oscillator in 20nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 52–53.

[12] Y. Huang and S. Liu, "A 2.4-GHz subharmonically injection-locked PLL with self-calibrated injection timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb. 2013.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

[13] P. Park, J. Park, H. Park, and S. Cho, "An all-digital clock generator using a fractionally injection-locked oscillator in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 336–337.

[14] S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara, and K. Masu, "An inductor-less injection-locked PLL with 1/2- and 1/4-integral subharmonic locking in 90 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig*., Jun. 2012, pp. 189–192.

[15] B. Helal, C. Hsu, K. Johnson, and M. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[16] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A 0.022 mm2 970 μW dual-loop injection-locked PLL with -243 dB FOM using synthesizable all-digital PVT calibration circuits," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 248–249.

[17] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada and A. Matsuzawa, "A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.

[18] W. Deng *et al*., "A 0.0066 mm2 780 μW fully synthesizable PLL with a current-output DAC and an interpolative phase-coupled oscillator using edge-injection technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 266–267.

[19] W. Deng *et al*., "A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, Jan. 2015.

[20] Y. Lee, M. Kim, T. Seong, and J. Choi, "A low phase noise injection-locked programmable reference clock multiplier with a two-phase PVT-calibrator for ΣΔ PLLs," *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 62, no. 3, pp. 635–644, Mar. 2015.

[21] I. Lee, Y. Chen, S. Liu, C. Jou, F. Hsueh, and H. Hsieh, "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 414–415

[22] C. Liang and K. Hsiao, "An injection-locked ring PLL with self-aligned injection window," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 90–92.

[23] S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara and K. Masu, "An inductorless injection-locked PLL with 1/2- and 1/4-integral subharmonic locking in 90 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig*., 2012, pp. 189–192.

[24] M. Kim, S. Choi and J. Choi, "A 450-fs jitter PVT-robust fractional-resolution injection-locked clock multiplier using a DLL-based calibrator with replica-delay-cells," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2015, pp. C142–C143.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

[25] M. Kim, S. Choi, T. Seong and J. Choi, “A Low-Jitter and Fractional-Resolution Injection-Locked Clock Multiplier Using a DLL-Based Real-Time PVT Calibrator With Replica-Delay Cells,” *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 401–411, Feb. 2016.

[26] Y. Lee, H. Yoon, M. Kim and J. Choi, "A PVT-Robust −59-dBc Reference Spur and 450-fs_{RMS} Jitter Injection-Locked Clock Multiplier Using a Voltage-Domain Period-Calibrating Loop,” in *Symp. VLSI Circuits Dig. Tech. Papers*, 2016, pp. C238–C239.

[27] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, “A 6.75-to-8.25GHz 2.25mW 190fs_{rms} integrated-jitter PVT-insensitive injection-locked clock multiplier using all-digital continuous frequency-tracking loop in 65nm CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2015, pp. 188–189.

[28] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, “Design and analysis of low-power high-frequency robust sub-harmonic injection-locked clock multipliers,” *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3160–3174, Dec. 2015.

[29] S. Choi, S. Yoo, Y. Lim and J. Choi, “A PVT-Robust and Low-Jitter Ring-VCO-Based Injection-Locked Clock Multiplier with a Continuous Frequency-Tracking Loop Using a Replica-Delay Cell and a Dual-Edge Phase Detector,” *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1878–1889, Aug. 2016.

[30] S. Kim, H. Ko, S. Cho, J. Lee, S. Shin, M. Choo, H. Chi, and D. Jeong, “A 2.5GHz Injection-Locked ADPLL with 197fsrms Integrated Jitter and -65dBc Reference Spur Using Time-Division Dual Calibration,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 494–495.

[31] S. Yang, J. Yin, P. Mak, and R. P. Martins, “A 0.0056-mm2 −249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs,” *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 88–98, Jan. 2019.

[32] B. R. Jackson, F. Mazzilli and C. E. Saavedra, “A frequency tripler using a subharmonic mixer and fundamental cancellation,” *IEEE Trans. Microw. Theory Techn*., vol. 57, no. 5, pp. 1083–1090, May 2009.

[33] C. Kuo, H. Chen and T. Yan, “A K-band CMOS quadrature frequency tripler using sub-harmonic mixer,” *IEEE Microw. Wireless Compon. Lett*., vol. 19, no. 12, pp. 822–824, Dec. 2009.

[34] P. Tsai, C. Liu and T. Huang, “A CMOS voltage controlled, oscillator and frequency tripler for 22–27 GHz local oscillator generation,” *IEEE Microw. Wireless Compon. Lett*., vol. 21, no. 9, pp. 492–494, Sep. 2011.

[35] Y. Lo and J. Kiang, “A 0.18μm CMOS self-mixing frequency tripler,” *IEEE Microw. Wireless Compon. Lett*., vol. 22, pp. 79–81, Feb. 2012.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

[36] T. Song, H. Oh, J. Yang, E. Yoon and S. Hong, "A 2.4 GHz sub-mW frequency source with current-reused frequency multiplier," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig.*, Jun. 2006, pp. 49–52.

[37] T. Song, H. Oh, E. Yoon and S. Hong, "A low-power 2.4 GHz current-reused receiver front-end and frequency source for wireless sensor network," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1012– 2033, May 2007.

[38] L. Couch, *Digital and Analog Communication Systems*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1997.

[39] *E-UTRA Base Station (BS) Radio Transmission and Reception*, document 3GPP TS 36.104 v14.3.0, 3rd Generation Partnership Project (3GPP), 2017. [Online].
Available: http://www.3gpp.org/ftp/Specs/archive/36_series/36.104/

[40] Verizon 5G TF. (2016). *Verizon 5th Generation Radio Access; Test Plan for Air Interface, V1.1*. [Online].
Available: http://www.5gtf.net/

[41] K. Okada *et al*., "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.

[42] L. Iotti, A. Mazzanti and F. Svelto, "Insights into phase-noise scaling in switch-coupled multi-core *LC* VCOs for E-band adaptive modulation links," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1703–1717, Jun. 2017.

[43] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66 GHz quadrature PLL in 45 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 494–495.

[44] W. Wu, R. B. Staszewski, and J. R. Long, "A 56.4-to-63.4 GHz multi-rate all-digital fractional-N PLL for FMCW radar applications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1081–1096, May 2014.

[45] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk, and P. Wambacq, "A 42 mW 230 fs-jitter sub-sampling 60 GHz PLL in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 366–367.

[46] Z. Huang, H. C. Luong, B. Chi, Z. Wang, and H. Jia, "A 70.5-to-85.5 GHz 65nm phase-locked loop with passive scaling of loop filter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 448–449.

[47] T. Siriburanon *et al*., "A low-power low-noise mm-wave subsampling PLL using dual-step-mixing ILFD and tail-coupling quadrature injection-locked oscillator for IEEE 802.11ad," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1246–1260, May 2016.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

[48] C. Jany, A. Siligaris, J. L. Gonzalez-Jimenez, P. Vincent, and P. Ferrari, "A programmable frequency multiplier-by-29 architecture for millimeter wave applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1669–1679, Jul. 2015.

[49] Z. Zong, M. Babaie, and R. B.Staszewski, "A 60 GHz frequency generator based on a 20 GHz oscillator and an implicit multiplier," *IEEEJ. Solid-State Circuits*, vol. 51, no. 5, pp. 1261–1273, May 2016.

[50] Q. Zou, K. Ma, and K. S. Yeo, "A low phase noise and wide tuning range millimeter-wave VCO using switchable coupled VCO-cores," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 554–563, Feb. 2015.

[51] *E-UTRA User Equipment Radio Transmission and Reception*, document 3GPP TS 36.101 v12.6.0, 3rd Generation Partnership Project (3GPP), 2015. [Online]. Available: http://www.3gpp.org/ftp/Specs/archive/36_series/36.101/

[52] H. Yoon *et al*., "A 0.56–2.92 GHz wideband and low phase noise quadrature LO-generator using a single *LC*-VCO for 2G–4G multistandard cellular transceivers," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 614–625, Mar. 2016.

[53] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A dual-loop injection-locked PLL with all-digital background calibration system for on-chip clock generation," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jan. 2016, pp. 238–239.

[54] S. Choi *et al*., "A 185 fs_{RMS}-integrated-jitter and−245 dB FOM PVT robust ring-VCO-based injection-locked clock multiplier with a continuous frequency-tracking loop using a replica-delay cell and a dual-edge phase detector," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 194–195.

[55] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada, and A. Matsuzawa, "A low phase noise quadrature injection locked frequency synthesizer for mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2635–2649, Nov. 2011.

[56] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, "A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1710–1720, Jul. 2013.

[57] D. Shin, S. Raman, and K.-J. Koh, "A mixed-mode injection frequency-locked loop for self-calibration of injection locking range and phase noise in 0.13μmCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 50–51.

[58] G. Mangraviti *et al*., "Design and tuning of coupled-*LC* mm-wave subharmonically injection-locked oscillators," *IEEE Trans. Microw. Theory Techn*., vol. 63, no. 7, pp. 2301–2312, Jul. 2015.

[59] W. El-Halwagy *et al*., "A 28 GHz quadrature fractional-N synthesizer for 5G mobile communication with less than 100 fs jitter in 65 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig*., Nov. 2016, pp. 118–121.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

[60] S. Yoo *et al*., "A PVT-robust −39 dBc 1 kHz-to-100 MHz integrated-phase-noise 29 GHz injection-locked frequency multiplier with a 600μW frequency-tracking loop using the averages of phase deviations for mm-band 5G transceivers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 324–325.

[61] G. R. Gangasani and P. R. Kinget, "Time-domain model for injection locking in nonharmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1648–1658, Jul. 2008.

[62] M. Izad and C. Heng, "A pulse shaping technique for spur suppression in injection-locked synthesizers," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 652–664, Mar. 2012.

[63] T. Seong, Y. Lee, and J. Choi, "Ultralow in-band phase noise injection-locked frequency multiplier design based on open-loop frequency calibration," *IEEE Trans. Circuits Syst. II, Reg. Papers*, vol. 61, no. 9, pp. 701–705, Sep. 2014.

[64] E. Monaco, G. Anzalone, G. Albasini, S. Erba, M. Bassi, and A. Mazzanti, "A 2–11 GHz 7-bit high-linearity phase rotator based on wideband injection-locking multi-phase generation for high-speed serial links in 28-nm CMOS FDSOI," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1739–1752, Jul. 2017.

[65] H. Yoon, *et al*., "A -31dBc Integrated-Phase-Noise 29GHz Fractional-N Frequency Synthesizer Supporting Multiple Frequency Bands for Backward-Compatible 5G Using a Frequency Doubler and Injection-Locked Frequency Multipliers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 366–367.

[66] D. Turker, *et al*., "A 7.4-to-14GHz PLL with 54fsrms jitter in 16nm FinFET for integrated RF-data-converter SoCs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 378–379

[67] D. Yang, *et al*., "A Calibration-Free Triple-Loop Bang-Bang PLL Achieving 131fs_{rms} Jitter and -70dBc Fractional Spurs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 266–267.

[68] X. Gao, E. A. M. Klumperink, M. Bohsali and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N^2," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec. 2009.

[69] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali and B. Nauta, "Spur Reduction Techniques for Phase-Locked Loops Exploiting A Sub-Sampling Phase Detector," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1809–1821, Sep. 2010.

[70] J. Sharma and H. Krishnaswamy, "A 2.4-GHz Reference-Sampling Phase-Locked Loop That Simultaneously Achieves Low-Noise and Low-Spur Performance," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1407–424, May. 2019.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

[71] D. Liao, F. F. Dai, B. Nauta, and E. A. M. Klumperink, "A 2.4-GHz 16-phase sub-sampling fractional-N PLL with robust soft loop switching," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 715–727, Mar. 2018.

[72] W. Chang, P. Huang and T. Lee, "A fractional-N divider-less phase-locked loop with a subsampling phase detector," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2964–2975, Dec. 2014.

[73] A. Sharkia, S. Mirabbasi and S. Shekhar, "A type-I sub-sampling PLL with a 100 × 100 μm^2 footprint and −255-dB FOM," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3553–3564, Dec. 2018.

[74] M. Talegaonkar, *et al*., "A 5GHz Digital Fractional-*N* PLL Using a 1-bit Delta–Sigma Frequency-to-Digital Converter in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2306–2320, Sep. 2017.

[75] J. Kim, *et al*., "An Ultra-Low-Jitter, mmW-Band Frequency Synthesizer Based on Digital Subsampling PLL Using Optimally Spaced Voltage Comparators," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3466–3477, Dec. 2019.

[76] Y. Lee, T. Seong, S. Yoo and J. Choi, "A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Switched-Loop Filter PLL Using a Fast Phase-Error Correction Technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1192–1202, Apr. 2018.

[77] H. C. Ngo, K. Nakata, T. Yoshioka, Y. Terashima, K. Okada and A. Matsuzawa, "A 0.42ps-Jitter -241.7dB-FOM Synthesizable Injection-Locked PLL with Noise-Isolation LDO," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 150–151.

[78] H. Yoon, S. Park and J. Choi, "A Low-Jitter Injection-Locked Multi-Frequency Generator Using Digitally Controlled Oscillators and Time-Interleaved Calibration," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1564–1574, Jun. 2019.

[79] A. Elkholy, A. Elmallah, M. G. Ahmed and P. K. Hanumolu, "A 6.75–8.25-GHz−250-dB FoM Rapid ON/OFF Fractional-N Injection-Locked Clock Multiplier," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1818–1829, Jun. 2018.

[80] A. Elkholy, D. Coombs, R. K. Nandwana, A. Elmallah and P. K. Hanumolu, "A 2.5–5.75-GHz Ring-Based Injection-Locked Clock Multiplier With Background-Calibrated Reference Frequency Doubler," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 2049–2058, Jul. 2019.

[81] K. M. Megawer, A. Elkholy, M. G. Ahmed, A. Elmallah, and P. K. Hanumolu, "Design of Crystal-Oscillator Frequency Quadrupler for Low-Jitter Clock Multipliers," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 65–74, Jan. 2019.

[82] S. Yoo, S. Choi, Y. Lee, T. Seong, Y. Lim, and J. Choi, "A 140fs_{rms}-Jitter and -72dBc-Reference-Spur Ring-VCO Based Injection-Locked Clock Multiplier Using a Background Triple-Point

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Frequency/Phase/Slope Calibrator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 490–491.

[83] D. Auvergne, J. M. Daga and M. Rezzoug, "Signal Transition Time Effect on CMOS Delay Evaluation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 47, no. 9, pp. 1362–1369, Sep. 2000.

[84] J. Zhu, R. K. Nandwana, G. Shu, A. Elkholy, S. Kim and P. K. Hanumolu, "A 0.0021 mm2 1.82 mW 2.2 GHz PLL using time-based integral control in 65nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 8–20, Jan. 2017.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

Acknowledgments

First of all, I would like to express my sincere gratitude to my advisor, Professor Jaehyouk Choi, for his invaluable guidance and wholehearted support. It was the best luck and best thing of my college life to take a lecture of Professor Jaehyouk Choi. In the lecture, his intuitive and clear explanation about the analog circuit has attracted me to the circuit design field. I was very happy when he gave me a great opportunity to join the Integrated Circuits and Systems Lab. (ICSL). He spent a lot of time teaching me and my lab members. Thanks to his enthusiasm, I learned a lot of knowledge and intuition about the analog circuits and know-how to design the circuit. He was always interested in future research, and gave me directions for further study. Without him, I could never have reached this moment of achievement.

I would also like to thank my committee members, Professor Kyuho Lee, Professor Seong-jin Kim, Professor Kyung Rok Kim, and Professor Hyun Jong Yang for being on my committee despite their busy schedule.

I would especially like to thank my beloved friends, Seojin Choi, Yongsun Lee, Younghyun Lim, Taeho Seong, and Heein Yoon (Alphabetical order of the last name). They and I were first members of the ICSL and worked together day and night to set up the laboratory and to have many tape-outs, sharing many unforgettable memories. In particular, working my teammate, Seojin Choi, I learned how to work in team and collaborate. I also want to thank Juyeop Kim, Jeonghyun Lee, Suneui Park, Jooeun Bang, Yoonseo Cho, Yongwoo Jo, Chanwoong Hwang, and Hangi Park. With them, I was able to have a happy and enjoyable time during my graduate student.

Finally, I would like to express my gratitude to my family and my girlfriend. My mother, Jeonghwa Lee, always gave me endless love and support. My father, Wonju Yoo, gave me a lot of advice as a father and an engineer. My brother, Jeayeon Yoo, who also is in doctoral program, gave me a lot of help as a family, friend and roommate. I am blessed to have my girlfriend, Eunjin Lee. She has been with me since the beginning of my master's and doctoral programs and always with me through thick and thin.

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Publications

1. Y. Lim=, J. Kim=, Y. Jo, J. Bang, **S. Yoo**, H. Park, H. Yoon and J. Choi, "A 170MHz-Lock-In-Range and -253dB-FOM_{JIT}, 12-14.5GHz Subsampling PLL with ...," *IEEE International Solid-State Circuits Conference (ISSCC)*, accepted for presentation, Feb. 2020. (= Equally-Credited Authors)

2. J. Lee, J. Bang, Y. Lim, **S. Yoo**, Y. Lee, T. Seong, and J. Choi, "A Fast-Transient and High-Accuracy, Adaptive-Sampling Digital LDO Uisng a Single VCO-Based Edge-Racing Time Quantizer," *IEEE Solid-State Circuits Letters (SSC-L)*, accepted for publication, invited from *IEEE 2019 Symp. VLSI Circuits*.

3. S. Park, J. Kim, C. Hwang, H. Park, **S. Yoo**, T. Seong, and J. Choi, "A 0.1-1.5 GHz Wide Harmonic-Locking-Free Delay-Locked Loop Using an Exponential DAC", *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 8, pp. 548-550, Aug. 2019.

4. T. Seong, Y. Lee, **S. Yoo**, and J. Choi, "A 320-fs RMS-Jitter and −75-dBc Reference-Spur Ring-DCO-Based Digital PLL Using an Optimal-Threshold TDC," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 9, pp. 2501–2512, Sep 2019.

5. S. Choi, **S. Yoo**, Y. Lee, Y. Jo, J. Lee, Y. Lim, and J. Choi, "An Ultra-Low-Jitter 22.8-GHz Ring-LC-Hybrid Injection Locked Clock Multiplier with a Multiplication Factor of 114," *IEEE Journal of Solid-State Circuits*, Apr. 2018, invited from *IEEE 2018 Symp. VLSI Circuits*.

6. **S. Yoo**, S. Choi, Y. Lee, T. Seong, Y. Lim and J. Choi, "A 140fs_{RMS}-Jitter and −72dBc-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Using a Background Triple-Point Frequency/Phase/Slope Calibrator," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2019.

7. S. Choi, **S. Yoo**, Y. Lee, Y. Jo, J. Lee, Y. Lim and J. Choi, "153 fs_{RMS}-Integrated-Jitter and 114-Multiplication Factor PVT-Robust 22.8 GHz Ring-LC-Hybrid Injection-Locked Clock Multiplier," *IEEE Symp. VLSI Circuits Dig*., Jun. 2018,

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

8. T. Seong, Y. Lee, **S. Yoo** and J. Choi, “A -242dB FOM and -75dBc-Reference-Spur Ring-DCO-Based All-Digital PLL Using a Fast Phase-Error Correction Technique and a Low-Power Optimal-Threshold TDC,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.

9. Y. Lee, T. Seong, **S. Yoo** and J. Choi, “A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Switched-Loop Filter PLL Using a Fast Phase-Error Correction Technique,” *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1192–1202, Apr 2018.

10. **S. Yoo**, S. Choi, J. Kim, H. Yoon, Y. Lee and J. Choi, “A Low-Integrated-Phase-Noise 27-30-GHz Injection-Locked Frequency Multiplier with an Ultra-Low-Power Frequency-Tracking Loop for mm-Wave-Band 5G Transceivers,” *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 375–388, Feb 2018.

11. T. Seong, Y. Lee, **S. Yoo**, and J. Choi, "A –242-dB FOM and –71-dBc Reference Spur Ring-VCO-based Ultra-Low-Jitter PLL," *IEEE Symp. VLSI Circuits Dig*., Jun. 2017.

12. **S. Yoo**, S. Choi, J. Kim, H. Yoon, Y. Lee, and J. Choi, "A PVT-Robust 29GHz Injection-Locked Frequency Multiplier with a 600uW Frequency-Tracking Loop for mm-Band 5G Transceivers," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2017.

13. S. Choi, **S. Yoo**, Y. Lim and J. Choi, “A PVT-Robust and Low-Jitter Ring-VCO-Based Injection-Locked Clock Multiplier With a Continuous Frequency-Tracking Loop Using a Replica-Delay Cell and a Dual-Edge Phase Detector,” *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1878–1889, Aug 2016.

14. S. Choi, **S. Yoo** and J. Choi, “A 185-fsrms Integrated-Jitter and -245dB FOM PVT-Robust Ring-VCO-Based Injection-Locked Clock Multiplier with a Continuous Frequency Tracking Loop Using a Replica-Delay Cell and a Dual-Edge Phase Detector,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.

15. **S. Yoo**, S. Choi, T. Seong and J. Choi, “An Ultra-Low Power and Compact LC-Tank-Based Frequency Tripler Using Pulsed Input Signals,” *IEEE Microwave and Wireless Components Letters (IEEE MWCL)*, vol. 26, no.2, pp.140–142, Feb 2016.

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

16. **S. Yoo**, J. Kim and J. Choi, “A 2-8 GHz Wideband Dually Frequency-Tuned Ring-VCO with a Scalable Kvco,” *IEEE Microwave and Wireless Components Letters (IEEE MWCL)*, vol. 23, no. 11, pp.602–604, Nov 2013.