Doctoral Dissertation

Overcoming Thermodynamic Limit of Subthreshold Swing in MOSFET: Device Structure and Unconventional Source Metal

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Abstract

Subthreshold swing is one of most important parameters in controversial metal-oxide-semiconductor (CMOS) technology, which is related on power consumption. In the metal-oxide-semiconductor field effect transistor (MOSFET), there is thermodynamic limit of subthreshold swing of 60 mV/dec at room temperature. In order to achieve the subthreshold swing, edge-over MOSFET structure is proposed, transistor channel of EO MOSFET is formed on sidewall of insulating pillar. Therefore, transistor channel length increases even though the lateral transistor channel length is maintained. Since the subthreshold swing is deteriorated by the short channel effect, relatively long channel due to existence of insulating pillar has advantage to suppress the subthreshold swing in nano-meter scale. By technology computer aided design (TCAD) modeling, electrical characteristics are demonstrated. Low drain induced barrier lowering (DIBL) of 13.7 mV/V and steep subthreshold swing of 62.6 mV/dec are estimated.

Ternary characteristics of EO ternary inverter are investigated by TCAD Mixed mode, the voltage transfer characteristics (VTC) of EO ternary inverter gives an apparent ternary voltage states. In according to structures of EO resistor and EO MOSFET, EO ternary inverter can be formed perpendicular to substrate, therefore, which allows thin lateral dimension of the inverter. Reliability of ternary operation is explained with static noise margin (SNM) and transient response. In the transient response, ternary operation is maintained at 10 MHz frequency, and a propagation delay of 1.69 ns is evaluated.

Theoretical approach to thermionic emission at Dirac semimetal source is performed. In the Dirac semimetal, since density of states are determined by linear energy dispersion near the Dirac point, thermionic emission current can be controlled by difference between Dirac point and fermi level and Schottky barrier height. As absence of direct injection of carriers from contact to Si, equation of thermionic emission is different with that of conventional up-down source/substrate structure. In case of graphene, there are singularities at negative infinity, hence the possibility of constant thermionic current exists regardless of the gate biasing of MOSFET. Meanwhile, lowest subthreshold swing of 30 mV/dec for 3 dimensional Dirac semimetal source is discussed.

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Nomenclature

CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nano Tube
CVD	Chemical Vapor Deposition
DIBL	Drain Induced Barrier Lowering
EO	Edge-Over
FED	Finite Element Method
FET	Field Effect Transistor
FinFET	Fin-shaped FET
GCA	Gradual Channel Approximation
IMT	Insulator-Metal Transition
LDOS	Local Density Of States
LPCVD	Low Pressure Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
MS	Metal Semiconductor
NCFET	Negative Capacitance FET
NEGF	Non Equilibrium Green's function
NMOSFET	N-channel MOSFET

PCFET	Phase Change FET
PMOSFET	P-channel MOSFET
SOI	Silicon On Insulator
STI	Shallow Trench Isolation
STM	Static Noise Margin
TCAD	Technology Computer Aided Design
TFET	Tunneling FET
VTC	Voltage Transfer Characteristics
WKB	Wentzel–Kramers–Brillouin

I. Overview

As improvement of controversial metal-oxide-semiconductor (CMOS) technology, subthreshold swing become important to suppress the power consumption of devices. In this doctoral thesis, approaches to overcome the subthreshold swing are discussed as structural approach and applying the Dirac semimetal source. Throughout the researches, numerical calculations are mainly performed to investigate the electrical characteristics. Theoretical works on thermionic emission current of Dirac semimetal source is studied, which show the subthreshold swing beyond thermodynamic limit.

In the chapter II, Brief reviews of solid state physics on energy band theory and semi-classical description to conventional metal-oxide-semiconductor (MOS) structure are described. In addition, metal-oxide-silicon field effect transistor (MOSFET) characteristics at subthreshold condition to derive the subthreshold swing are demonstrated.

In the chapter III, various approaches to suppress the subthreshold swing are introduced, and edge-over (EO) MOSFET structure is proposed. Due to existence of unique insulating pillar, channel of transistor is enlarged in vertical direction on the silicon (Si) substrate, hence the transistor can achieve ultimate scaling in lateral dimension. Electrical characteristics of EO MOSFET are investigated by technology computer aided design (TCAD) modeling, which show subthreshold swing of 62.6 mV/dec and drain induced barrier lowering (DIBL) of 13.7 mV/V.

In the chapter IV, edge-over ternary inverter is proposed. Voltage transfer characteristics (VTC) is evaluated by TCAD mixed mode, which show ternary voltage states due to potential distribution by existence of resistors. Transient responses show the reliable ternary operation at tens of MHz frequency, and propagation delay of 1.69 ns is estimated.

In the chapter V, thermionic emission current of graphene (2 dimensional Dirac semimetal) and arbitrary 3 dimensional Dirac semimetal are discussed as Schottky barrier height and difference between Dirac point and fermi level. Depending on the presence of direct injection of carriers from contact to Si, formalism of thermionic current is distinguished. The subthreshold swing of Dirac semimetal source MOSFET breaks the thermodynamic limit by prohibiting direct injection of carrieres. Lowest subthreshold swing of 3 dimensional Dirac semimetal case is 30 mV/dec, which is half of thermodynamic limit of 3 dimensional bulk material source case, and subthreshold swing of graphene has negative singularity.

II. Introduction to MOSFET

2.1 Band Theory

The mechanics of electrons in an atom is described by atomic orbitals with eigen energy state of electron. In the solid, there exit tremendous number of atoms and their potential from atom affects the other atomic system and their atomic orbitals overlap each other, therefore energy states are different from that of an atom. In this regard, the solid system can be described with some assumptions, which is periodicity of potential and electron states. Large-scale homogeneous system assures the periodicity of potential in the solid, also single electron state is assured by non-interactivity. With these assumptions, Bloch theorem gives the energy band structure of solid as shown in Figure 2.1(a), which is called energy band diagram. In band theory, there are usually several bands, but energy bands around the Fermi level, called valence band and conduction band, contribute to electron transport. These 2 bands are determined by Fermi level which have a 50% probability of being occupied by electron, function of Fermi-Dirac statistics describe these as [1][2]

$$f_{FD}(E) = \frac{1}{e^{(E-E_F)/k_BT} + 1} \tag{2.1}$$

Where, μ is the Fermi level, k_B is the Boltzmann constant and T is temperature. The valence band is located just below the Fermi level (or chemical potential) and is completely filled with electrons which makes the movement of carrier restricted at the absolute 0 K. Meanwhile, the conduction band is located just above the Fermi level and has no electron at the absolute 0 K, which enables electron to move freely. And there are no state for electron in the forbidden band gap (or band gap).

There are 3 main classification in band theory as shown in Figure 2.1(b): conductor, semiconductor and insulator. In case of conductor, there is a partially filled band due to the position of Fermi level located inside of energy band, hence electrons move freely in this band. However, the Fermi level of insulator is located in forbidden band gap, moreover, wide band gap suppresses the transition of electron from fully filled valence band to empty conduction band. In case of semiconductor, energy band diagram is similar with insulator, however, relatively small band gap allows the transition of electron from the valence band to the conduction band by thermally or external potential. In addition, since defects or impurities can supply the additional energy states in forbidden gap and provide additional carriers in band, Fermi level is shifted.

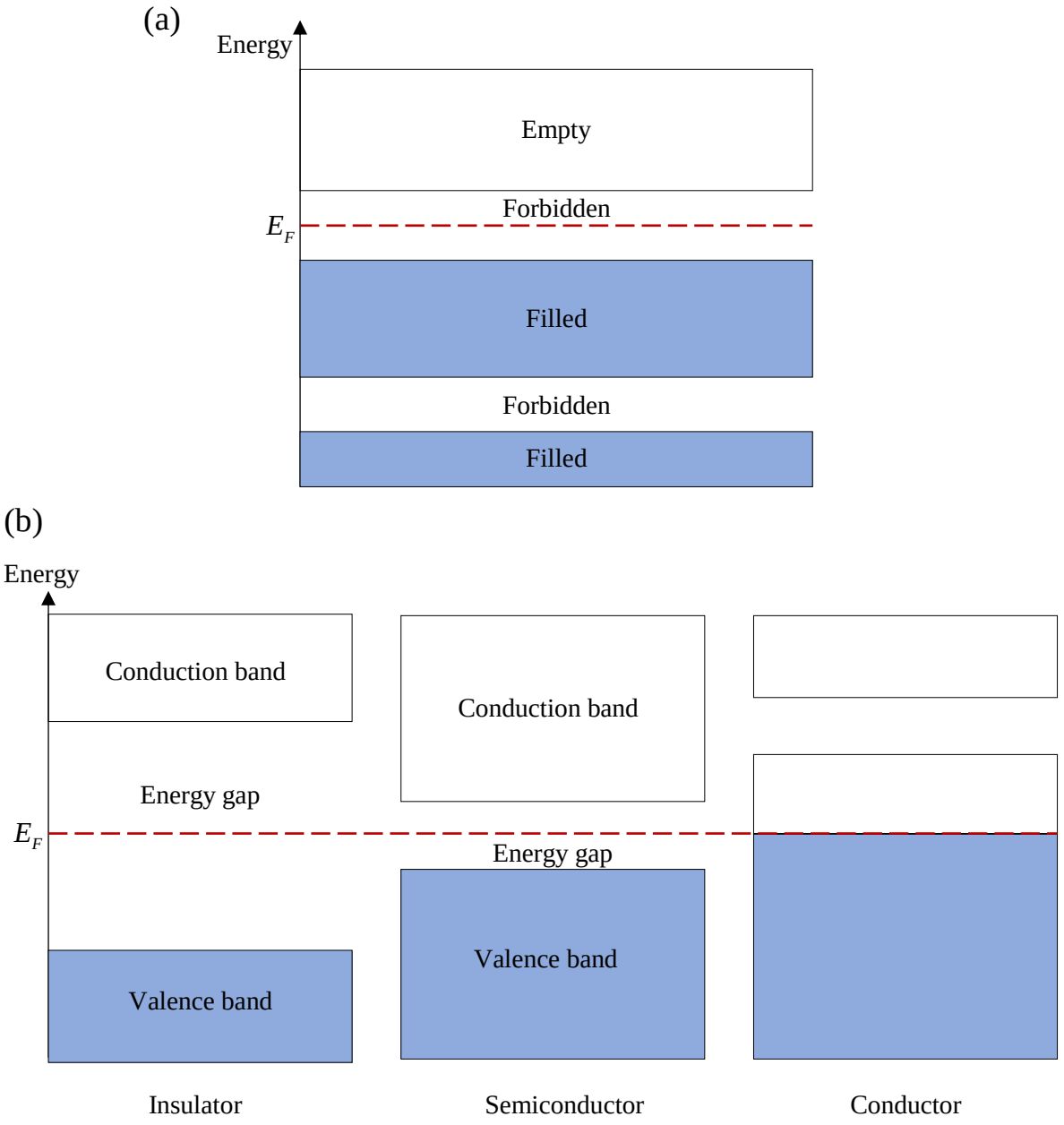

Figure 2.1 (a) Energy band diagram of semiconductor case, continuous atomic orbitals construct the energy band which is filled up to Fermi level (chemical potential). (b) Energy band diagrams of insulator, semiconductor and conductor are determined by Fermi level and shape of bands.

2.2 Silicon

Silicon (Si) is one of the abundant materials on earth (27.7% of crust is Si). From abundance of Si deposit and excellent electrical properties of Si make it possible to use them as the electronic devices, glasses and organic compounds, we live in the age of Si. In this section, material properties of Si are introduced.

2.2.1 Material properties

Bulk silicon crystal has diamond lattice structure as illustrated in Figure 2.2, 8 atoms of Si are located in lattice unit cell (called primitive cell) with lattice constant of 5.43 Å. In the bulk Si crystal, two nearest Si atom forms covalent bonding. Therefore, a Si atom forms 4 covalent bonds with 4 nearest neighbours, energy state of these 4 electrons construct the valence band by band theory. In other hands, unoccupied 4 electron states construct conduction band. As purpose of increasing the free carrier (electron or hole) concentration, specific impurity atom is doped in Si. For example, column V elements such as phosphorus (P), arsenic (As) and antimony (Sb) supply the extra electrons by substitute for Si atom, they are called donors. In other hand, column III elements such as boron (B), gallium (Ga), indium (In) and aluminium (Al) absorb electron by substitute for Si atom, hence which supply the hole, they are called acceptors. When the concentration of donors is larger than the concentration of acceptors, which is called n-type Si. The opposite case is called p-type Si.

Table 2.1 shows material properties of Si, which show prominent motilities of electron and hole to use electronic device. Also, pure Si has a band gap of 1.12 eV at room temperature, which is moderate energy for switching conduction and insulation states by external potential. However, energy band gap has temperature dependence, which is described empirically:

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta} \tag{2.2}$$

Where, $E_G(0)$ is 1.169 eV, α is 4.9×10^{-4} eV/K and β is 655 K [4]. As increase of temperature, since energy band gap narrows, electron in the valence band can be excited to conduction band easily result in narrowed band gap and additional thermal energy, it is undesirable in the device.

Table 2.1 Material properties of Silicon [3]

Lattice constant (Å)	Density (g/cm^3)	Relative permittivity	Electron mobility (cm^2/Vs)	Hole mobility (cm^2/Vs)	Electron affinity (eV)	Band gap (eV)
5.43095	2.3290	11.68~11.90	≤ 1400	≤ 450	4.05	1.12

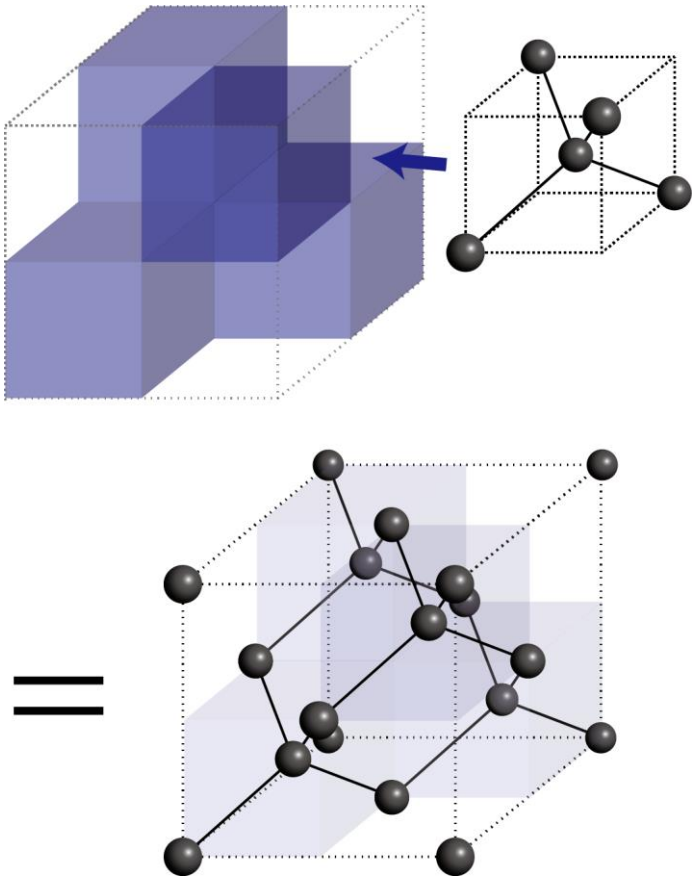

Figure 2.2 Crystal structure of Si in primitive cell, which is diamond lattice structure.

2.2.2 Carrier concentration

The number of electrons n and holes p is determined by the density of state $D(E)$ and the Fermi-Dirac statistics:

$$n = \int_{E_c}^{\infty} dE D_c(E) f_{FD}(\mathrm{E}) \tag{2.3}$$

$$p = \int_{-\infty}^{E_v} dE D_v(E)[1 - f_{FD}(\mathrm{E})] \tag{2.4}$$

Where, E_c is energy of conduction band minimum, E_v is energy of valence band maximum. 3-dimensional density of state $D(E)$ near the edge of conduction band minimum is approximately given by

$$D_c(\mathrm{E}) = \frac{m_e^{3/2}\sqrt{2}\sqrt{E - E_c}}{\pi^2\hbar^3} \tag{2.5}$$

Where, $\hbar$ is the Planck constant, g_c is the number of equivalent conduction band minimum, m_e is the effective mass of electron given by $m_e = \sqrt{m_l m_t^2}$ (m_l and m_t are the electron effective mass in the conduction band along the longitudinal and transverse directions, respectively). With (2.1) and (2.5), the electron concentration is

$$\begin{aligned} n &= \frac{m_e^{3/2}\sqrt{2}}{\pi^2\hbar^3}\int_{E_c}^{\infty} dE \frac{\sqrt{E - E_c}}{e^{(E-E_F)/k_BT} + 1} \\ &= \frac{2}{\sqrt{\pi}}\left(\frac{m_e k_b T}{2\pi\hbar^2}\right)^{3/2}\int_{E_c}^{\infty}\frac{dE}{k_b T}\frac{\sqrt{(E - E_c)/k_b T}}{e^{(E-E_F)/k_BT} + 1} \\ &= \frac{2N_c}{\sqrt{\pi}} F_{1/2}\left(\frac{E_F - E_c}{k_b T}\right) \end{aligned} \tag{2.6}$$

Where, $F_{1/2}$ is the Fermi-Dirac integral of order 1/2 and N_c is the effective density of states in conduction band:

$$N_c = 2\left(\frac{m_e k_B T}{2\pi\hbar^2}\right)^{3/2} \tag{2.7}$$

$$F_{1/2}(\eta) = \int_0^{\infty} dE \frac{\sqrt{E}}{e^{E-\eta} + 1} \tag{2.8}$$

Similarly, hole concentration and effective density of states in valence band N_v are

$$n = \frac{2N_v}{\sqrt{\pi}} F_{1/2}\left(\frac{E_v - E_F}{k_b T}\right) \tag{2.9}$$

$$N_v = 2\left(\frac{m_h k_B T}{2\pi\hbar^2}\right)^{3/2} \tag{2.10}$$

Where, m_h is the effective mass of hole in the valence band given by $m_h = (m_{lh}^{3/2} + m_{hh}^{3/2})^{2/3}$ (m_{lh} and m_{hh} are the hole effective mass in the valence band).

When the doping concentration is less than the effective density of states, it is said nondegenerate. On the other hands, when the doping concentration is more than the effective density of states, it is said degenerate. In case of nondegenerate Si, electron statistics approach to function of Maxwell-Boltzmann distribution $f_{MB} = e^{-(E-E_F)/k_B T}$, hence carrier concentrations are become

$$n = \frac{2N_c}{\sqrt{\pi}} F_{1/2}\left(\frac{E_F - E_c}{k_B T}\right) \approx N_c e^{-(E_c - E_F)/k_B T} \tag{2.11}$$

$$p \approx N_v e^{-(E_F - E_v)/k_B T} \tag{2.12}$$

There are thermal excited electrons from the valence band to the conduction band, meanwhile holes are created in the valence band. In this process, the equilibrium of carrier concentration is maintained by recombination of carriers.

Intrinsic Si

In the intrinsic Si, which is nondegenerate, Fermi level and the intrinsic Fermi level E_i of intrinsic Si is determined with (2.11) and (2.12):

$$E_F = E_i = \frac{E_c + E_v}{2} + \frac{k_B T}{2} \ln \frac{N_v}{N_c} \tag{2.13}$$

From (2.13), the intrinsic Fermi level E_i is close to the middle of band gap. In steady state, carrier concentrations are given by intrinsic concentration $n_i = n = p$, therefore $n_i^2 = np$ gives the intrinsic carrier concentration n_i:

$$n_i = N_c e^{-(E_c - E_i)/k_B T} = N_v e^{-(E_i - E_v)/k_B T} = \sqrt{N_c N_v} e^{E_G/2k_B T} \tag{2.14}$$

Carrier concentration can be expressed with intrinsic carrier concentration in nondegenerate case n_i :

$$n = n_i e^{(E_F - E_i)/k_B T} \tag{2.15}$$

$$p = n_i e^{(E_i - E_F)/k_B T} \tag{2.16}$$

These alternative equations describe carrier concentration by difference of Fermi level and intrinsic Fermi level, in other words, carrier concentrations give the Fermi level.

Extrinsic Si

For impurities doped Si, donors and acceptors are mostly ionized in relatively high temperature including room temperature, in this regard, charge neutrality condition is given by

$$n - p + N_a^- - N_d^+ \approx n - p + N_a - N_d = 0 \tag{2.17}$$

Where, N_d is the concentration of donors, and N_a is the concentration of acceptors. In case of the n-type Si, carrier concentration in the thermal equilibrium is approximately given by

$$n_{n0} \approx N_d = N_c e^{-(E_c - E_F)/k_B T} = n_i e^{(E_F - E_i)/k_B T} \tag{2.18}$$

$$p_{n0} = \frac{n_i^2}{n_{n0}} \approx \frac{n_i^2}{N_d} \tag{2.19}$$

In case of the p-type Si, carrier concentration in the thermal equilibrium is approximately given by

$$p_{p0} \approx N_a = N_v e^{-(E_F - E_v)/k_B T} = n_i e^{(E_i - E_F)/k_B T} \tag{2.20}$$

$$n_{p0} = \frac{n_i^2}{p_{n0}} \approx \frac{n_i^2}{N_a} \tag{2.21}$$

2.3 MOSFET characteristics

The metal oxide semiconductor field effect transistor (MOSFET) is the key of the microprocessors, and complementary metal oxide semiconductor (CMOS) consists logic gates with the advantage of low power consumption. In particular, subthreshold swing is one of the most important characteristics associated with the power consumption of MOSFET. In this section, MOSFET characteristics are reviewed from surface charge to subthreshold swing.

2.3.1 Space charge on MOS

Energy band diagram of MOS structure with p-type Si at equilibrium is illustrated in Figure 2.3. Where q is the elementary charge, E_0 is vacuum level energy, $q\Phi_m$ is metal work function, $q\psi_b$ is energy difference of Fermi level and intrinsic Fermi level, $q\chi_i$ and $q\chi_{Si}$ are the electron affinity of insulator and Si respectively (q is multiplied to prevent confusion from units of eV). In the case of Figure 2.3, which shows flat band condition with applied voltage equal to the difference between the work function of the metal and the Fermi level Si. In general case, difference of metal work function and Fermi energy of p-type Si $\Delta q\Phi_p$ is given by

$$\Delta q\Phi_p = q\Phi_m - (q\chi_{Si} + E_G + q\psi_b) \tag{2.22}$$

The quasi Fermi potential at insulator/Si interface $\psi(x)$ is same with the difference of intrinsic Fermi level at position x and deep inside $x = \infty$ (bulk):

$$q\psi(x) = -(E_i(x) - E_i(\infty)) \tag{2.23}$$

$\psi(x)$ is defined downward in the energy band diagram as potential energy increases. Figure 2.4 shows the energy band of p-type Si with band bending by surface space charge. Space charge condition of the region can be distinguished by the quasi Fermi potential at insulator/Si interface $\psi(0)$ [5],

$\psi(0) < 0$	Accumulation of holes
$\psi(0) = 0$	Flat band condition
$0 < \psi(0) < \psi_b$	Depletion of holes
$\psi(0) = \psi_b$	$E_F = E_i(0)$, $n_i = p_p(0) = n_p(0)$
$\psi_b < \psi(0) < 2\psi_b$	Weak inversion
$2\psi_b < \psi(0)$	Strong inversion

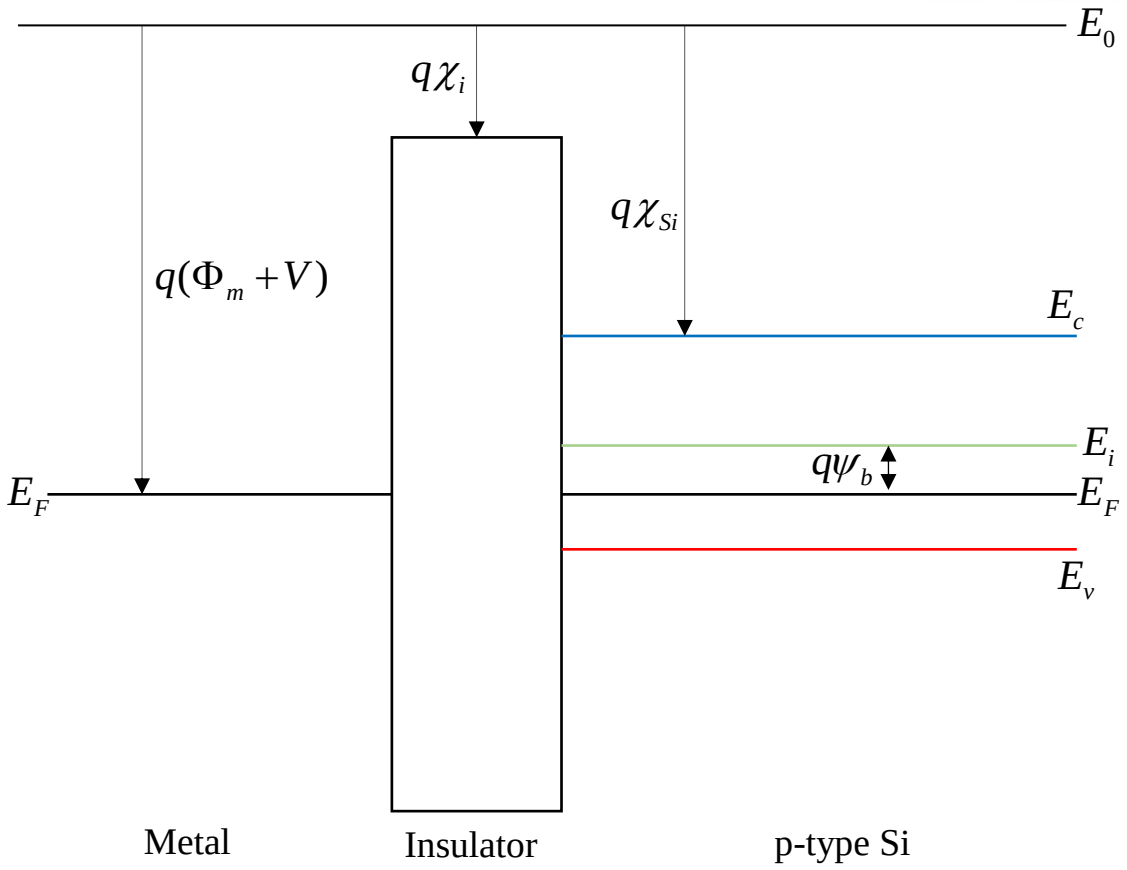

Figure 2.3 Energy band diagram of MOS structure with p-type Si at equilibrium, flat band is induced with applied voltage equal to the difference between the work function of the metal and the Fermi level Si.

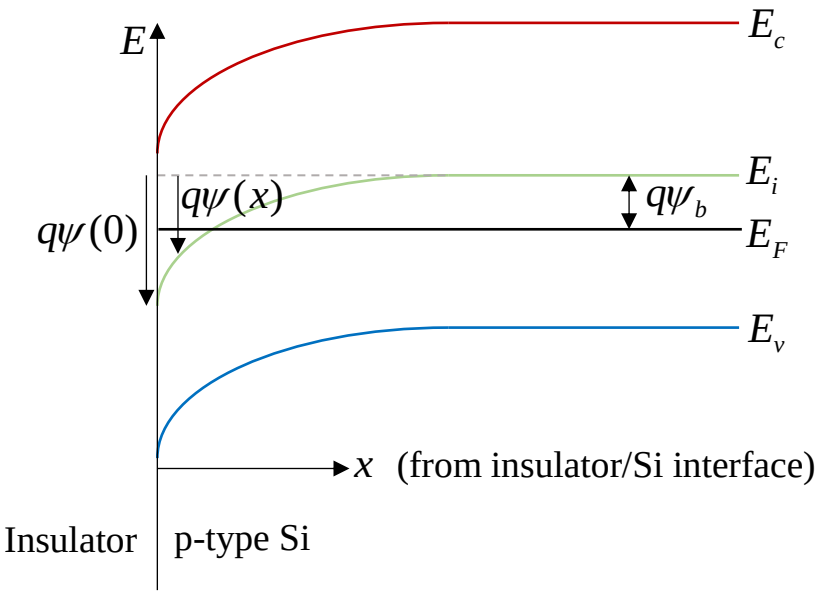

Figure 2.4. Energy band diagram of p-type Si at insulator/Si interface.

From (2.20) and (2.21), carrier concentrations can be write with quasi Fermi potential expressed as (2.23):

$$\begin{aligned} p_p(x) &= n_i e^{(E_i(x)-E_F)/k_BT} = n_i e^{q(\psi_b-\psi(x))/k_BT} = n_i e^{-q\psi_b/k_BT} e^{-q\psi(x)/k_BT} \\ &= p_{p0} e^{-q\psi(x)/k_BT} \end{aligned} \tag{2.24}$$

$$n_p(x) = n_{p0} e^{q\psi(x)/k_BT} \tag{2.25}$$

In the bulk Si which is far from insulator/Si interface, there are no net current with charge neutrality condition:

$$N_d^{+} - N_a^{-} = n_{p0} - p_{n0} \tag{2.26}$$

Hence, 1-dimensional Poisson's equation of n-type MOSFET become

$$\begin{aligned} \frac{d^2\psi}{dx^2} &= -\frac{q}{\varepsilon_{Si}}(N_d^{+} - N_a^{-} + p_p - n_p) \\ &= -\frac{q}{\varepsilon_{Si}}(n_{p0} - p_{p0} + p_p - n_p) \\ &= -\frac{q}{\varepsilon_{Si}}[p_{p0}(e^{-q\psi/k_BT} - 1) - n_{p0}(e^{q\psi/k_BT} - 1)] \\ &= -\frac{q}{\varepsilon_{Si}}[p_{p0}(e^{-a\psi} - 1) - n_{p0}(e^{a\psi} - 1)] \end{aligned} \tag{2.27}$$

Where, ε_{Si} is the relative permittivity of Si, and $a = q/k_BT$ is for simplicity of equation. To get the electric field inside of silicon, integration of Poisson's equation is [6]

$$\frac{d^2\psi}{dx^2} = \frac{d}{dx}\left(\frac{d\psi}{dx}\right) \rightarrow$$

$$\frac{d^2\psi}{dx^2}d\psi = \frac{d^2\psi}{dx^2} \times \frac{d\psi}{dx}dx = \frac{d}{dx}\left(\frac{d\psi}{dx}\right) \times \frac{d\psi}{dx}dx = \frac{d\psi}{dx}d\left(\frac{d\psi}{dx}\right) \tag{2.28}$$

$$\begin{aligned} \int_0^{\frac{d\psi}{dx}} \frac{d\psi'}{dx} d\left(\frac{d\psi'}{dx}\right) &= \frac{1}{2}\left(\frac{d\psi}{dx}\right)^2 \\ &= -\frac{q}{\varepsilon_{Si}}\int_0^{\psi} d\psi'[p_{p0}(e^{-a\psi'} - 1) - n_{p0}(e^{a\psi'} - 1)] \\ &= \frac{qp_{p0}}{\varepsilon_{Si}a}[(e^{-a\psi} + a\psi - 1) + \frac{n_{p0}}{p_{p0}}(e^{a\psi} - a\psi - 1)] \end{aligned} \tag{2.29}$$

Hence the electric field at Si surface is

$$\xi = \frac{d\psi}{dx} = \pm\sqrt{\frac{2qp_{p0}}{\varepsilon_{Si}a}[(e^{-a\psi(0)} + a\psi(0) - 1) + \frac{n_{p0}}{p_{p0}}(e^{a\psi(0)} - a\psi(0) - 1)]} \tag{2.30}$$

Where, $\psi(0)$ is called surface potential. In the expression of electric field (2.30), first bracket describes dependence on holes and ionized donors, and second bracket describes dependence on electrons and ionized acceptors. Finally, the total space charge per unit area on MOS is

$$\begin{aligned} Q_s &= -\varepsilon_{Si}\xi = \mp\sqrt{\frac{2q\varepsilon_{Si}p_{p0}}{a}[(e^{-a\psi(0)} + a\psi(0) - 1) + \frac{n_{p0}}{p_{p0}}(e^{a\psi(0)} - a\psi(0) - 1)]} \\ &= \mp\sqrt{2\varepsilon_{Si}p_{p0}k_bT[(e^{-q\psi(0)/k_bT} + \frac{q}{k_bT}\psi(0) - 1) + \frac{n_{p0}}{p_{p0}}(e^{q\psi(0)/k_bT} - \frac{q}{k_bT}\psi(0) - 1)]} \end{aligned} \tag{2.31}$$

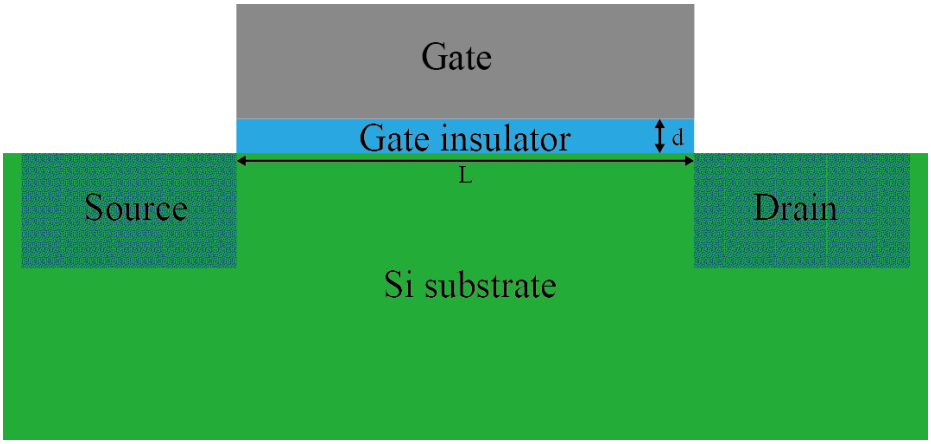

Figure 2.5 Schematic cross-sectional view of n-channel MOSFET with p-type Si substrate

2.3.2 Diffusion current and the form of subthreshold swing

Figure 2.5 shows schematic cross-sectional view of n-channel MOSFET with channel length of L and gate insulator thickness of d, source and drain are defined by n-type impurities doping on p-type Si substrate. The goal of the section is derivation of subthreshold swing $S.S$ by analytic equation, which is described by

$$S.S = \left. \frac{dV_G}{d(\log_{10} I_D)} \right|_{V_D} \tag{2.32}$$

Where, V_G and V_D are gate voltage and drain voltage respectively and I_D is drain current, the source contacts are considered grounded. Subthreshold swing is proportional to the inverse slope of channel current by gate voltage at subthreshold condition, where the diffusion current is dominant. Thus, diffusion current of MOSFET at subthreshold swing will be derived firstly, and subthreshold swing for MOSFET will be investigated secondly.

Width of Depletion layer

The range of the quasi Fermi potential is $0 < \psi < 2\psi_b = 2\frac{k_b T}{q}\ln\frac{N_a}{n_i}$ due to subthreshold condition covering the depletion of holes and weak inversion. The electric field inside of depletion layer depending on ionized acceptors and holes can be approximated with (2.20) ,(2.21) and $N_a \gg n_i$ at subthreshold condition:

$$\begin{aligned} \xi = \frac{d\psi}{dx} &= -\sqrt{\frac{2qN_a}{\varepsilon_{Si} a}\left[(e^{-a\psi} + a\psi - 1) + \frac{n_i^{\,2}}{N_a^{\,2}}(e^{a\psi} - a\psi - 1)\right]} \\ &\approx -\sqrt{\frac{2qN_a}{\varepsilon_{Si}}\psi} \end{aligned} \tag{2.33}$$

Integration of (2.33) gives

$$\int_{\psi(0)}^{\psi} \frac{d\psi'}{\sqrt{\psi'}} = 2(\sqrt{\psi} - \sqrt{\psi(0)}) = -\int_0^x dx\sqrt{\frac{2qN_a}{\varepsilon_{Si}}} = -\sqrt{\frac{2qN_a}{\varepsilon_{Si}}}x \tag{2.34}$$

$$\psi = \psi(0)\left(1 - \sqrt{\frac{qN_a}{2\varepsilon_{Si}\psi(0)}}x\right)^2 = \psi(0)\left(1 - \frac{x}{W_d}\right)^2 \tag{2.35}$$

$$W_d = \sqrt{\frac{2\varepsilon_{Si}\psi(0)}{qN_a}} \tag{2.36}$$

Where, W_d is the width of depletion layer. Integration range is from insulator/Si interface to end of the deletion layer x. The depletion layer is widened until before starting the strong inversion. Therefore, the maximum width of the depletion layer $W_{d,\max}$ is determined at the condition of the quasi Fermi potential, $\psi = 2\psi_b = 2\frac{k_bT}{q}\ln\frac{N_a}{n_i}$:

$$W_{d,\max} = \sqrt{\frac{4\varepsilon_{Si}\psi_b}{qN_a}} = \sqrt{\frac{4\varepsilon_{Si}k_bT}{q^2N_a}\ln\frac{N_a}{n_i}} \tag{2.37}$$

In addition, the total charge of ionized acceptors in the deletion layer is same with the total depletion charge density Q_d:

$$Q_d = -qN_aW_d = -\sqrt{2\varepsilon_{Si}qN_a\psi(0)} \tag{2.38}$$

Subthreshold current

In according too gradual channel approximation (GCA), the change of electric field perpendicular to the insulator/Si interface in the channel is stronger than the change of electric field along the channel except the pinch-off. Electron concentration at position x and y in channel of n-channel MOSFET, y is the position between the drain and the source along the channel (longitudinal direction), can be write with GCA:

$$n_p(x,y) = \frac{n_i^2}{N_a}e^{q(\psi(x)-V(y))/k_bT} \tag{2.39}$$

The channel potential of strong inversion at Si surface can be written as

$$\psi(0,y) = 2\psi_b + V(y) \tag{2.40}$$

Hence, the maximum depletion layer width in n-channel MOSFET is

$$W_{d,\max} = \sqrt{\frac{4\varepsilon_{Si}\psi_b + V(y)}{qN_a}} \tag{2.41}$$

Similarly, the electric field in n-channel without ionized donors is approximately given by

$$\begin{aligned}\xi(0,y) &= \sqrt{\frac{2N_a k_B T}{\varepsilon_{Si}}[(e^{-q\psi(0,y)/k_B T} + \frac{q}{k_B T}\psi(0,y) - 1) + \frac{n_i^{\,2}}{N_a^{\,2}}(e^{q\psi(0,y)/k_B T} - 1)e^{qV(y)/k_B T}]} \\ &\approx \sqrt{\frac{2N_a k_B T}{\varepsilon_{Si}}\left(\frac{q}{k_B T}\psi(0,y) + \frac{n_i^{\,2}}{N_a^{\,2}}e^{q(\psi(0,y)-V(y))/k_B T}\right)}\end{aligned} \tag{2.42}$$

Hence, total space charge density become

$$Q_s(0,y) = -\sqrt{2\varepsilon_{Si}N_a k_B T\left(\frac{q}{k_B T}\psi(0,y) + \frac{n_i^{\,2}}{N_a^{\,2}}e^{q(\psi(0,y)-V(y))/k_B T}\right)} \tag{2.43}$$

Since the voltage $V(y)$ depends only on y, it can be write as the voltage V. In the expression of total space charge density (2.43), since second term is much smaller than first term, it can be approximated

$$\begin{aligned}-Q_s &= \sqrt{2q\varepsilon_{Si}N_a\psi(0,y)}\left(1 + \frac{k_B T}{q\psi(0,y)}\frac{n_i^{\,2}}{N_a^{\,2}}e^{q(\psi(0,y)-V)/k_B T}\right)^{\frac{1}{2}} \\ &\approx \sqrt{2q\varepsilon_{Si}N_a\psi(0,y)} + \sqrt{\frac{q\varepsilon_{Si}N_a}{2\psi(0,y)}}\frac{k_B T}{q}\frac{n_i^{\,2}}{N_a^{\,2}}e^{q(\psi(0,y)-V)/k_B T} \\ &= -Q_d - Q_i\end{aligned} \tag{2.44}$$

Because the space charge is sum of the depletion charge and the inversion charge, the total inversion charge density is acquired from (2.44):

$$-Q_i = \sqrt{\frac{q\varepsilon_{Si}N_a}{2\psi(0,y)}}\frac{k_B T}{q}\frac{n_i^{\,2}}{N_a^{\,2}}e^{q(\psi(0,y)-V)/k_B T} \tag{2.45}$$

The inversion charge density is smaller than depletion charge density, hence the quasi Fermi potential is predominantly depends on the transverse electric field (by the gate voltage), which means the electric field across the channel from drain to source is negligibly small. Also, the quasi Fermi potential can be treated as function of x, $\psi(0,y) = \psi(0)$. In the same manner, the drift current can be ignored, because which is determined with the longitudinal electric field by the drain voltage, $J_{drift} \propto \xi_{DS}$.

In according to the Fick's law of diffusion, the diffusion current can be described with diffusion coefficient D_n [5][7]:

$$J_n = qD_n\frac{dn}{dy} \tag{2.46}$$

$$J_p = -qD_p \frac{dp}{dy} \tag{2.47}$$

$$D_n = \frac{k_B T}{q} \mu_n \tag{2.48}$$

$$D_n = \frac{k_B T}{q} \mu_p \tag{2.49}$$

Where, μ_n and μ_p are motilities of electron and hole, n and p are the density of electron and hole. The diffusion current with lateral channel width W (W is the direction perpendicular to $x-y$ plane) can be acquired by integration from Si surface to bulk Si:

$$I_{sub}(y) = qW\mu_n^* \int_0^\infty dx \cdot n(x, V(y)) \frac{dV}{dy} \mu_n \tag{2.50}$$

Where, μ_n^* is effective electron mobility with the averaged electric field from the gate and the drain. Integration of the diffusion current by longitudinal direction gives

$$\begin{aligned} I_{sub} &= \int_0^L \frac{dy}{L} I_{DS}(y) \\ &= q\mu_n^* \frac{W}{L} \int_0^{V_{DS}} dV \int_0^\infty dx n(x,V) \\ &= q\mu_n^* \frac{W}{L} \int_0^{V_{DS}} dV(-Q_i(V)) \end{aligned} \tag{2.51}$$

In according to the current continuity condition, the current needs to be independent of the direction y. The diffusion current is determined by the total inversion charge density (2.45), the final form of the diffusion current at subthreshold condition is

$$\begin{aligned} I_{sub} &= q\mu_n^* \frac{W}{L} \int_0^{V_{DS}} dV \sqrt{\frac{q\varepsilon_{Si} N_a}{2\psi(0,y)}} \frac{k_B T}{q} \frac{n_i^2}{N_a^2} e^{q(\psi(0)-V)/k_B T} \\ &= q\mu_n^* \frac{W}{L} \sqrt{\frac{q\varepsilon_{Si} N_a}{2\psi(0,y)}} \left(\frac{k_B T}{q}\right)^2 \frac{n_i^2}{N_a^2} e^{q\psi(0)/k_B T} (1 - e^{-qV_{DS}/k_B T}) \end{aligned} \tag{2.52}$$

Finally, it is the subthreshold current. However, there are no direct relation between the gate voltage and the quasi Fermi potential at Si surface. Subthreshold swing can be rewrite:

$$S.S = \left.\frac{dV_G}{d(\log_{10} I_D)}\right|_{V_D} = \frac{dV_G}{d\psi(0)} \left.\frac{d\psi(0)}{d(\log_{10} I_D)}\right|_{V_D} \tag{2.53}$$

The electrostatic potential across the insulator from metal/insulator interface to insulator/Si interface is

$$V_G - V_{fb} = V_i + \psi(0) = \frac{\sqrt{2q\varepsilon_{Si}N_a\psi(0)}}{C_i} + \psi(0) \tag{2.54}$$

Where, $V_i = C_i Q_d$ is potential drop across the insulator and $C_i = \varepsilon_i d$ is the capacitance of the insulator.

$$\frac{dV_G}{d\psi(0)} = \frac{1}{C_i}\sqrt{\frac{q\varepsilon_{Si}N_a}{2\psi(0)}} + 1 = \frac{C_d}{C_i} + 1 \tag{2.55}$$

$$C_d = \frac{\varepsilon_{Si}}{W_d} = \sqrt{\frac{q\varepsilon_{Si}N_a}{2\psi(0)}} \tag{2.56}$$

Where, C_d is the capacitance of depletion layer. Subthreshold swing is evaluated by

$$S.S = \left.\frac{dV_G}{d(\log_{10} I_D)}\right|_{V_D} = \frac{dV_G}{d\psi(0)}\left.\frac{d\psi(0)}{d(\log_{10} I_D)}\right|_{V_D} = \ln(10)\frac{dV_G}{d\psi(0)}\left.\frac{d\psi(0)}{d(\ln I_D)}\right|_{V_D} = \left(1 + \frac{C_d}{C_i}\right)\frac{k_B T}{q}\ln(10) \tag{2.57}$$

Subthreshold swing depends on the capacitance of the insulator and the depletion layer. There are several ways to suppressing the subthreshold swing. The first way is to increase the capacitance of the insulator, but there is physical limitation to reduce the thickness of the insulator and increasing the relative permittivity of the insulator has the limitation of the material diversity. The second way is achieving the negative capacitance of the insulator using by ferroelectric material. The third way is reducing the capacitance of depletion layer by novel structures or materials. The details of suppressing the subthreshold swing is discussed in the next chapter.

III. Edge-over MOSFET

The MOSFET structure is the heart of the logic circuits, and most of electrical computations are performed with MOSFET based computing systems. Hence the MOSFET is one of most important transistor structure. This chapter describes the current challenges of nano-meter scale MOSFETs and propose the solution on structural approach with novel structure called Edge-over MOSFET.

3.1 Introduction

Over the past decades, size of field effect transistors (FETs) has been reduced from micro-meter scale to nano-meter scale due to significant improvements in complementary metal oxide semiconductor (CMOS) technology. As the scale down of the device, short channel effect which is parasitic effect in micro-meter scale has become the predominant of device operation in nano-meter scale. Therefore, suppressing the short channel effect in nano-meter scale has become an important in current CMOS technology.

3.1.1 Drain induced barrier lowering

In particular, drain induced barrier lowering (DIBL) which is one of most important short channel effects deteriorates the device's operating characteristics. As can be seen in the Figure 3.1(a)(b), DIBL affects the height of barrier in short channel as increase of source drain bias V_{ds}, however the barrier height of long channel devices is not effected by increase of V_{ds}, only the potential near the drain is reduced. The increase in DIBL raises the issue of stability of device operation, but the most concern is increase of device power consumption. Due to the dense CMOS integrated circuits consisted by devices in nano-meter scale, power consumption of device has reached a considerable level, therefore suppressing power consumption is one of most important problems facing the CMOS industry in present. In practice, DIBL of MOSFET is evaluated in transfer characteristics (I_{ds} vs. V_{gs}, source drain current vs. gate voltage) as

$$DIBL = -\frac{V_t^h - V_t^l}{V_{ds}^h - V_{ds}^l} \tag{3.1}$$

Where, V_{ds}^l is low source drain voltage, V_{ds}^h is high source drain voltage, V_t^l is threshold voltage at V_{ds}^l and V_t^h is threshold voltage at V_{ds}^h. In general, low source drain voltage is 0.05V or 0.1V.

3.1.2 Subthreshold Swing

The increase of subthreshold swing causes similar problems with DIBL such as shifting of threshold voltage and increasing power consumption. In the previous section of 2.3.2, we discussed the form of subthreshold swing, in practice, subthreshold swing determined by

$$S.S = \frac{dV_{gs}}{d(\log_{10} I_{ds})}\bigg|_{V_{ds}} \tag{3.2}$$

Where, I_{ds} is source drain current. Subthreshold swing evaluates the gate controllability at subthreshold condition (in case of conventional planar MOSFET, dominant transport mechanism at subthreshold condition is diffusion as mentioned in the section of 2.3.2), which is the inverse change of drain source current by the change of gate source voltage as shown Figure 3.1(c). As increase as subthreshold swing, threshold voltage V_t also deceases, as a result, off-state current is increases, which means power consumption of the device is also increases. In summary, DIBL and subthreshold swing are significant indicator of transistor on operational characteristics and power consumption. Thermodynamic limit of subthreshold swing for conventional MOSFET structure is only depend on temperature, which is

$$S.S^* = \frac{k_B T}{q}\ln 10 \tag{3.3}$$

At room temperature, the thermodynamic limit of subthreshold swing is ~60 mV/dec, which is hard to achieve with nano-meter scale planar MOSFET, because the portion of the channel region with competing the gate source voltage and the source drain voltage increases. Also, analytic approach to subthreshold swing is unmatched with the real electric characteristics due to the failure of GCA in the short channel. In the next section, attempts to suppress the subthreshold swing are introduced.

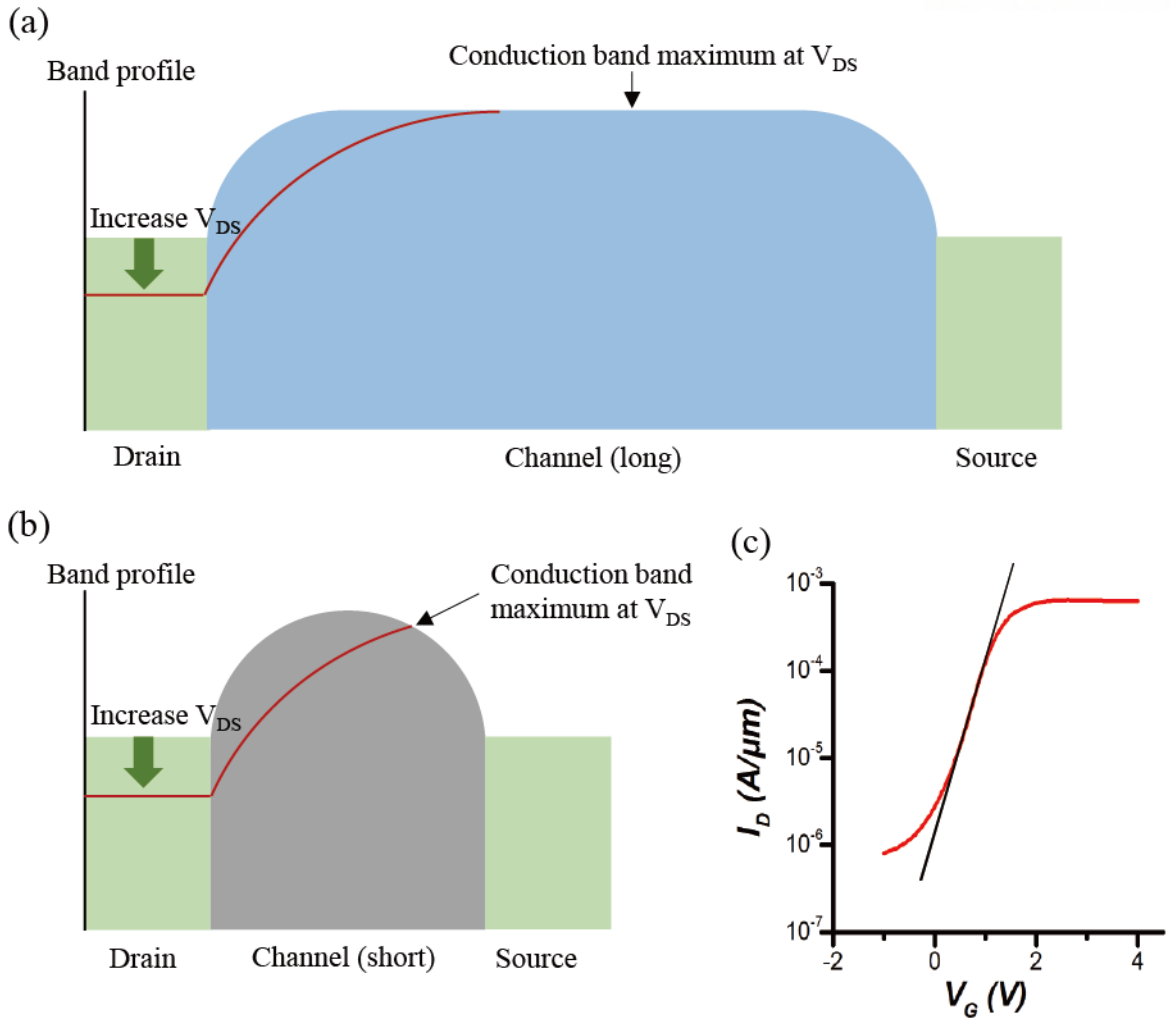

Figure 3.1 (a) Energy band profile of long channel case by change of drain source voltage, (b) Energy band profile of short channel case by change of drain source voltage and (3) subthreshold swing in transfer characteristics of MOSFET.

3.2 Suppressing subthreshold swing on transistor

3.2.1 Suppressing subthreshold swing and drain induced barrier lowering in conventional CMOS technology

Over the last decades, novel device structures are suggested to suppress the subthreshold swing and some structures have showing subthreshold swing close to thermodynamic limit even at nano-meter scale. One of the most favourable condition to suppress subthreshold swing is the process require to be in CMOS technology or easy to implement. In this regard, some structures in CMOS technology ars suggested, they are MOSFET with silicon on insulator (SOI) structure (Figure 3.2(a)) and Fin-shaped FET called FinFET (or tri-gate FET, Figure 3.2(b)) [8 - 23]. In the SOI MOSFET, the channel of device is mostly depleted with structural confined with existence of buried oxide, hence subthreshold swing is suppressed. Similarly, since the channel of FinFET is confined in physically with 3 dimensional wrapped structure and electrostatically with 3 dimensional gate biasing, FinFETs have a fully depleted channel. In addition, the gate-all-around MOSFET can be possible due to the improvement of fabrication technology which is shown as Figure 3.2(c), in the gate-all-around MOSFET, extrema channel controllability can be achieved due to the transistor channel confined in all the transverse direction [24].

Current trends in FinFET

Since, Intel produces first commercialized FinFET with 22 nm process technology, which showed subthreshold swing of ~70 mV/dec and low DIBL of ~50 mV/V, FinFET is most commercialized structure in present [10-14]. In recent, Taiwan Semiconductor Manufacturing Company (TSMC) report the improved performance of FinFET with 7 nm CMOS technology, which showed steep subthreshold swing of ~65 mV/dec and DIBL of ~35 mV/V [23]. Nevertheless, multi-dimensional structure of FinFET is challenge and complex to fabricate, compared with the conventional planar MOSFET [25]. In this reason, there is effort to overcoming the complex fabrication process through the extreme ultraviolet lithography process (EUV) [22]. However, there is still no guarantee that FinFET will be successful to achieve steep subthreshold swing and low DIBL in a few nano-meter device channel length.

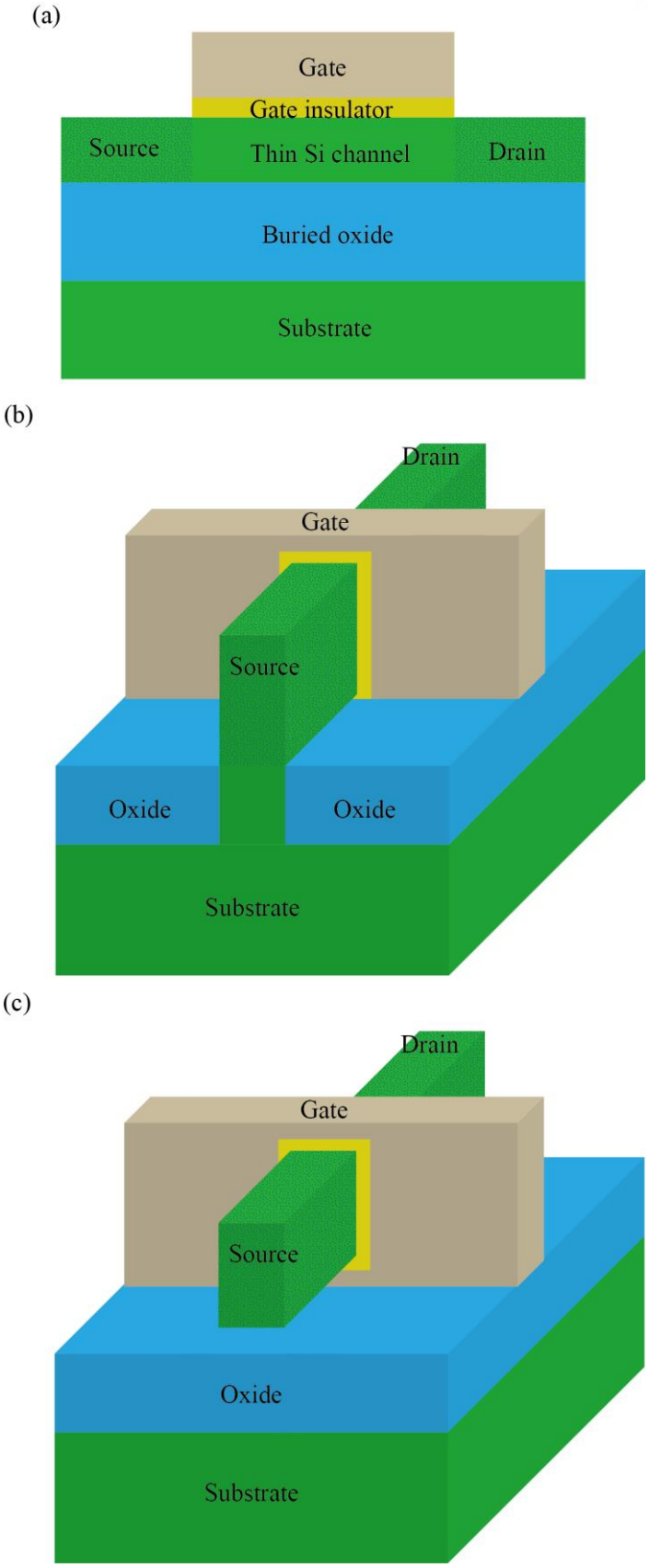

Figure 3.2 (a) Schematic cross-sectional view of SOI MOSFET, (b) schematic view of FinFET, and (c) gate-all-around MOSFET.

3.2.2 Suppressing subthreshold swing on various approaches

There are several novel structures beyond the CMOS fabrication, and some transistors overcome the thermodynamic limit of subthreshold swing. Transistors which overcome the subthreshold swing are negative capacitance FET (NCFET) with ferroelectric material, tunnelling FET (TFET), phase change FET (PCFET) with insulator-metal transition material (IMT) and graphene Dirac source FET. In this subsection, NCFET, TFET, and PCFET are introduced, however, graphene Dirac source FET is treated at relevant chapter V [26 - 32].

Negative capacitance FET (NCFET)

NCFET has the unique gate insulting layer which consisted with ferroelectric material and insulator or ferroelectric insulator as shown in Figure 3.3. The reason of using ferroelectric material is described with analytic equation of the subthreshold swing:

$$S.S = \frac{k_B T}{q}\left(1+\frac{C_s}{C_g}\right)\ln(10) \tag{3.4}$$

$$C_s = C_{in} + C_d \tag{3.5}$$

$$C_g = \left(C_i^{-1} + C_{FE}^{-1}\right)^{-1} \tag{3.6}$$

Where, C_s is the capacitance of substrate, C_{in} is the capacitance of inversion layer, C_g is the capacitance between gate and substrate, and C_{FE} is the capacitance of ferroelectric material. In the previous section, inversion charge is neglected due to dominance of depletion charge at subthreshold condition, however, the case of NCFET can't be neglect the capacitance of inversion layer due to the rapid transition from the subthreshold to strong inversion. In according to considering negative capacitance of ferroelectric material near the threshold voltage, C_s / C_g term can be negative when the capacitance of insulator is larger than the negative capacitance of ferroelectric layer, $C_i > -C_{FE} > 0$. Hence $1+C_s / C_g$ term is lower than 1, which means that the subthreshold swing of the transistor overcomes the thermodynamic limit (in the thermodynamic limit, $1+C_s / C_g$ term is 1). However, it is not possible to improve the subthreshold swing indefinitely. As the term $1+C_s / C_g$ approaches to singularity of subthreshold swing when $1+C_s / C_g = 0$, electrical characteristics such as transfer characteristics show the hysteresis which is the disadvantage of the transistor [26 - 29].

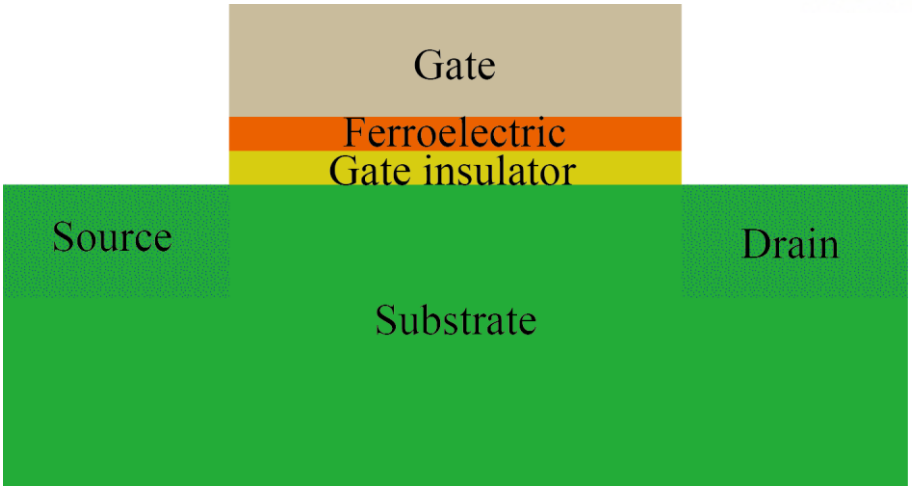

Figure 3.3 schematic cross-sectional view of NCFET.

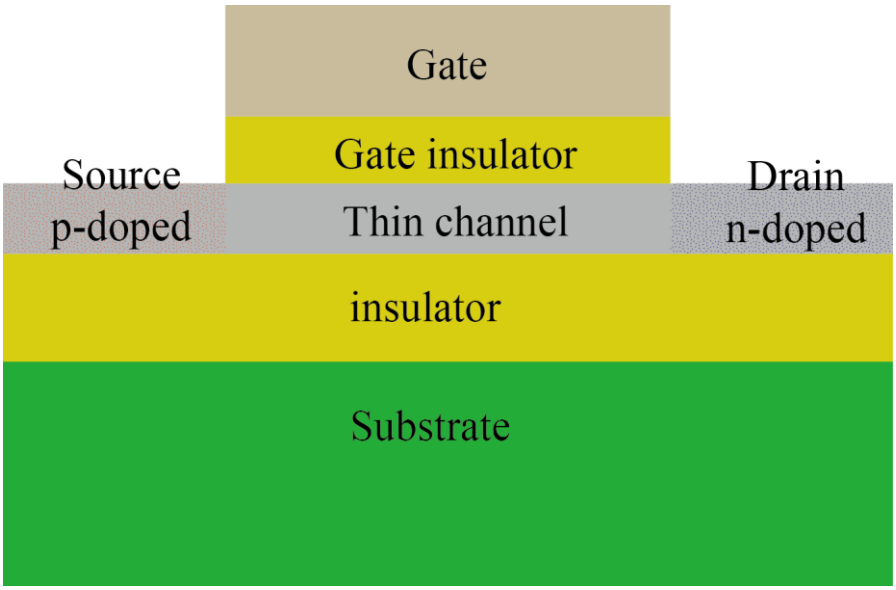

Figure 3.4 schematic cross-sectional view of TFET, which looks similar with SOI MOSFET, however transport mechanism of the transistor is differed with MOSFET.

Tunnelling FET (TFET)

Figure 3.4 shows cross-sectional view of TFET, which structure is similar with the SOI MOSFET, however, the different impurities doping on source and drain differs the transport mechanism with MOSFET [30]. In the MOSFET, carrier transport is mainly induced by thermionic emission. Meanwhile, in case of TFET, transport between source and drain by thermionic emission is prohibited by the band gap. Hence, the only possible transport is the quantum tunnelling between the valence band and the conduction band, which is called band-to-band tunnelling. As the change of gate bias, there are 3 operating states which are illustrated in Figure 3.5. In the On-state as shown in Figure 3.5(a), the potential of the transistor channel is increased with gate bias, hence the conduction band of p-doped drain and channel are aligned to maximize the band-to-band tunnelling with short distance. In the Off-state as shown in Figure 3.5(b), band-to-band tunnelling distance is maximized from the source to the drain, therefore transport is blocked mostly. In addition, there is ambipolar-state, which is allowed by band-to-band tunnelling between the transistor channel and the drain due to the negative gate biasing as illustrated in Figure 3.5(c). Since the main transport is the quantum tunnelling in all the operational states, the TFET can overcome the thermodynamic limit of subthreshold swing, which is mainly determined by the diffusion current due to the thermionic emission came from tail of Fermi-Dirac statistics. However, the OFF-state current of the TFET is hard to transistor engineering and binary logic due to the ambipolar characteristics, also relative low ON-stated current due to quantum tunnelling is also problem.

Phase change FET (PCFET)

PCFET has an additional unique structure on source or gate insulator consisting of insulator to metal transition material (IMT). Figure 3.6 shows the phase change of IMT between the insulator and the metal by the voltage, in other words, localized electron can be changed to free electron by voltage, and also free electron can be change to localized electron by voltage. The structures of PCFET is illustrated in Figure 3.7, there are 2 main parts of the MOSFET and the IMT source, which occupying relatively large dimension compared to MOSFET. In the operational characteristics, sudden phase change of IMT in subthreshold region break the thermodynamic limit of subthreshold swing, however critical hysteresis is reported due to the IMT's hysteric phase change, moreover, extremely low ON/OFF ratio is another disadvantage of PCFET [31].

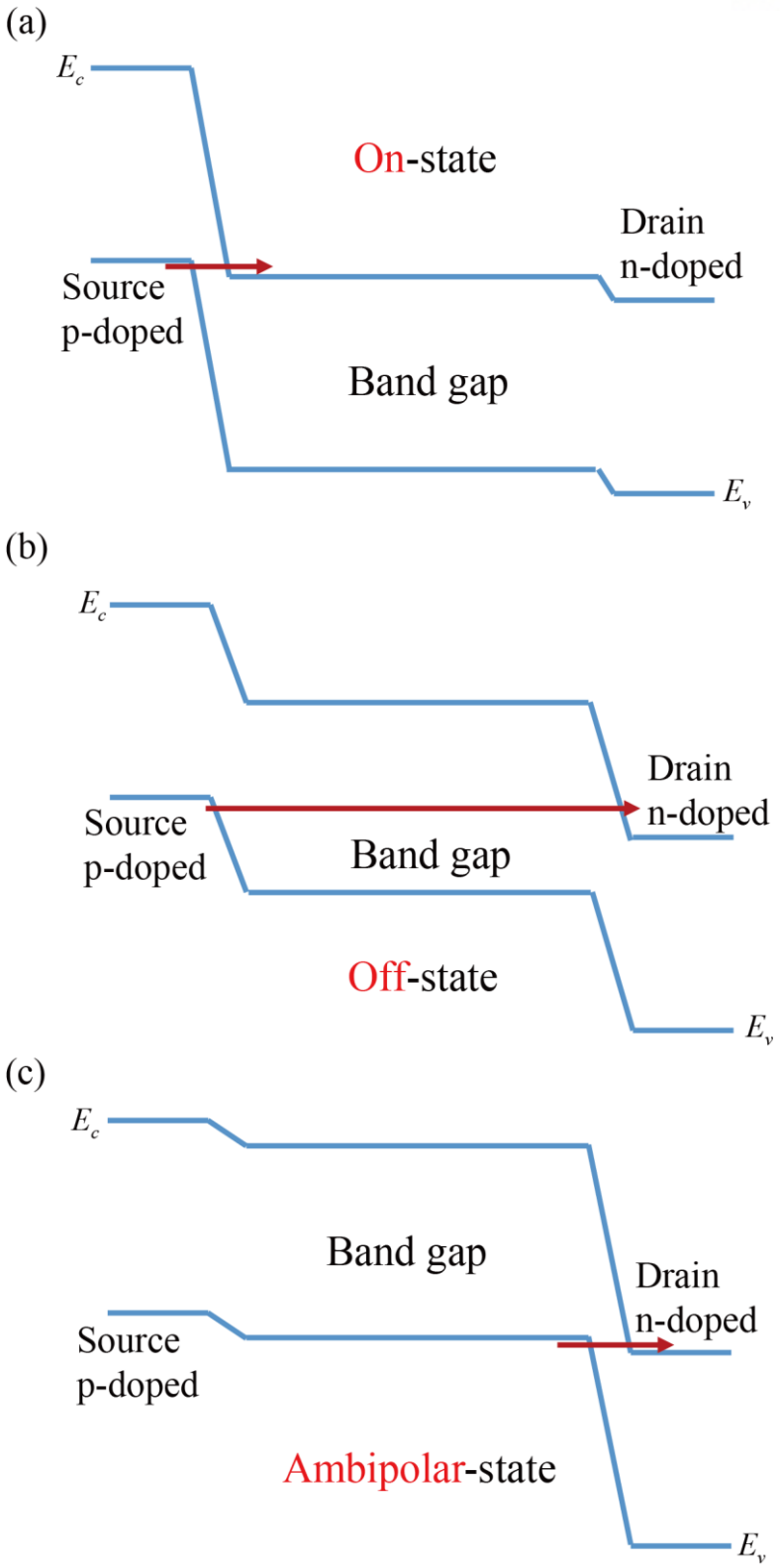

Figure 3.5 Band diagram of TFET at the operational state of (a) On-state, (b) Off-state, and (c) ambipolar-state.

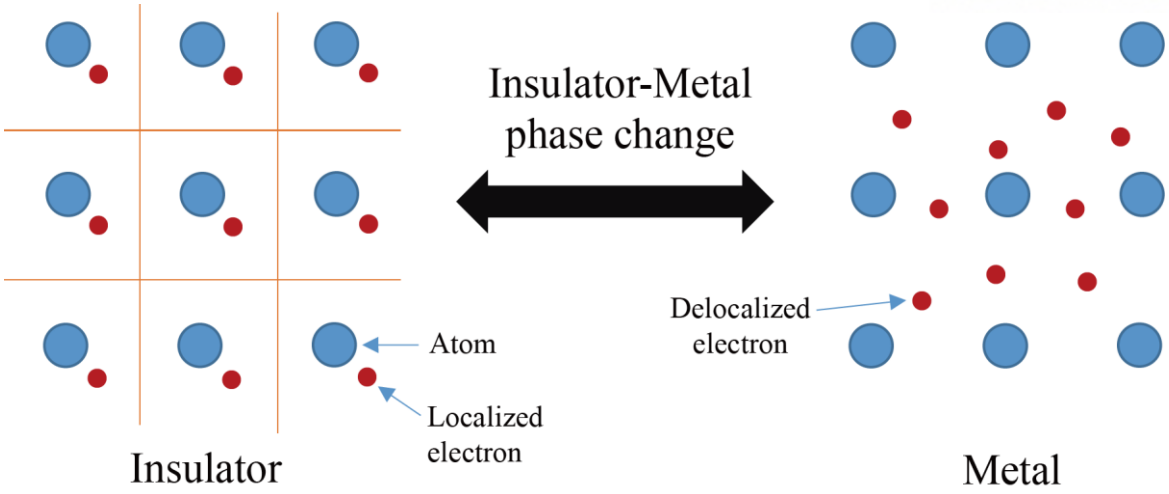

Figure 3.6 Schematic of insulator-metal phase change in IMT, which has the characteristics about localized electron-delocalized electron (free electron) phase change.

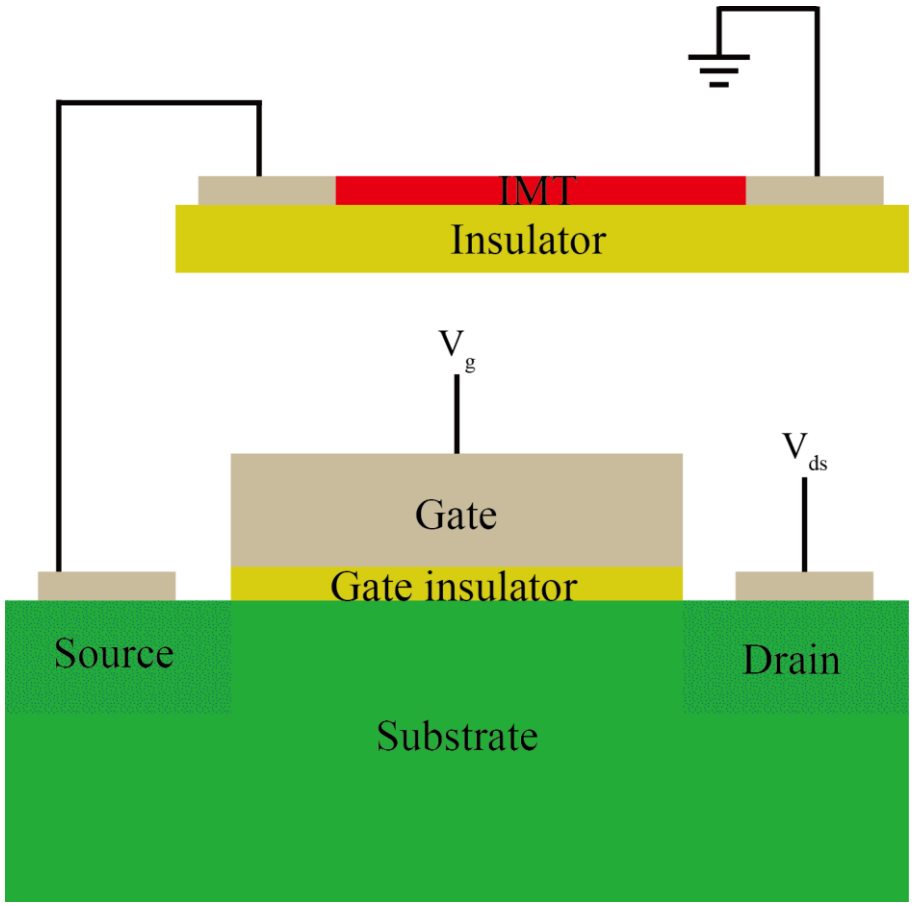

Figure 3.7 Schematic cross-sectional view of PCFET, which consists by MOSFET and IMT source.

3.3 Edge-over MOSFET

Because the channel length of MOSFET is the predominant variable of DIBL, the scaled down of transistor to nano-meter scale is causing the increase of DIBL, and conversely increasing the length of transistor channel diminish the DIBL. Furthermore, if the transistor channel can be enlarged in same lateral transistor pitch, DIBL will be suppressed by longer the effective channel length. Hence, the transistor channel in vertical direction is the prime candidate to constructing dense integrated circuit with longer effective channel. So far, constructing vertical MOSFET with noticeable improvement of subthreshold swing is reported in experimentally [33][34]. In line with this approach, we propose a novel MOSFET structure which showed subthreshold swing near the theoretical thermodynamic limit and remarkably low DIBL at nano-meter scale lateral channel length, the name is edge-over MOSFET (EO MOSFET). In the EO MOSFET, the transistor channel is elongated to vertical direction due to the existence of a unique insulating pillar as shown in Figure 3.9(a). The height of insulating pillar determines the effective channel length mainly by forming over the edge of insulating pillar. Thin undoped poly-Si is intended to improve the gate channel controllability by fully depleted channel and easy to edge over the channel.

3.3.1 TCAD methodology

Technology computer aided design (TCAD) is a computer simulation of CMOS technology, including the device process and operational characteristics of the device. Based on finite element method, TCAD solve the partial differential equation such as transport equations, hence electrical characteristics and structural properties are obtained. To investigate the electrical properties, we use the commercial TCAD package of the SILVACO. Schematic of the TCAD modeling process in case of EO MOSFET is illustrated in Figure 3.8.

Included physical models in TCAD modeling

In our device modeling, the physical models included in SILVACO TCAD were chosen to imitate the operation of real devices [35], adopted models are described briefly:

1. Parallel electric field dependence model: which describes the carrier velocity saturation with parallel electric field.
2. Direct quantum tunneling model: which describes the tunnuling on thin insulating layer in several nano-meter.
3. Uchida's low field model: which describes the mobility in thin channel SOI MOSFET in range of

2.4 ~ 8 nm.

4. Shockley-Read-Hall recombination model: which is recombination due to phonon transitions caused by the presence of a traps or defects in forbidden band gap.
5. Auger electron-hole recombination model: which is recombination about transition of particles, however underlying physics is unclear in present. Only the qualitative interpretation is given.
6. Klaassen band-to-band tunneling model: which describes the tunneling between the valence band and the conduction band by energy band bending due to high electric field, in this model, the tunneling parameters specified by Klaassen are used.

Especially, since the transistor has an ultra-thin channel of 2nm, quantum models of confinement or correction must be included. The Uchida's low mobility model is based on experimental data of thin SOI MOSFETs that reflects the fluctuation of quantum confinement in order to non-uniform channel thickness of 2.4 ~ 8 nm [36]. Therefore, Uchida's low mobility model was adopted to take quantum confinement in thin transistor channel. In order to validate the TCAD models, the calculated curves were compared with experimentally measured curves for a junctionless MOSFET. The structure has an undoped thin poly-Si channel, which is channel length of 0.4 μm and channel thickness of 10 nm, and SiO_2 gate insulator thickness of 8.5 nm. The TCAD models in modeling of a junctionless MOSFET are same with TCAD models of EO MOSFET and planar MOSFET. As shown as Figure 3.10, the calculated curve and the actual measurement curve (Figure.3 in [37]) are close and similar [37]. In TCAD modeling of junctionless MOSFET, carrier mobility, defect state density, and Klaassen band to band tunneling parameters are calibrated with measured data.

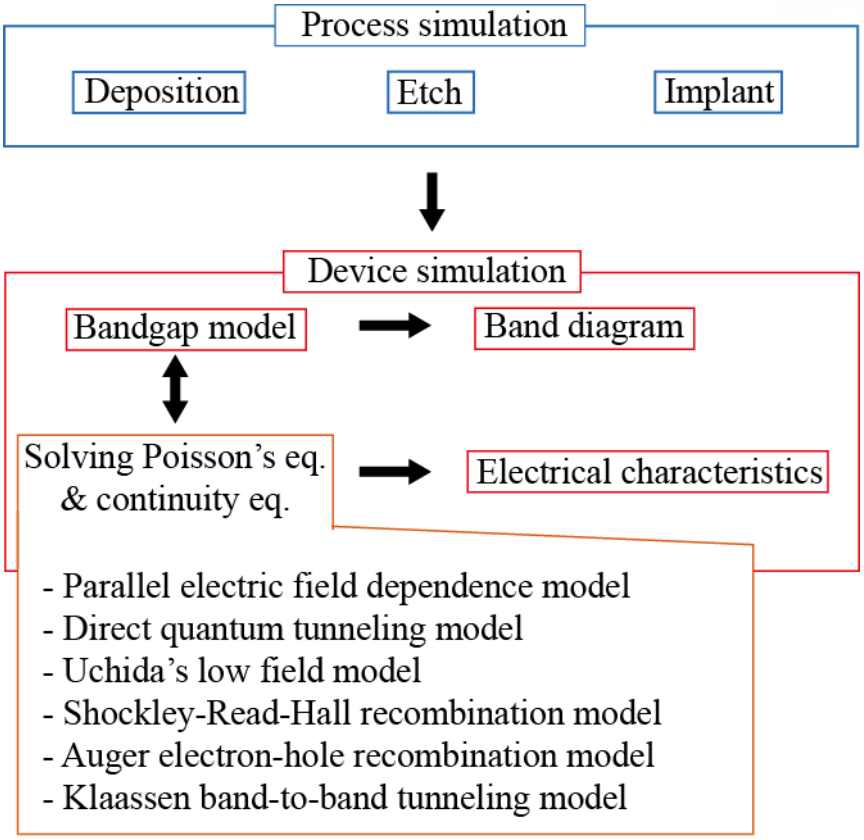

Figure 3.8 TCAD modeling process of the EO MOSFET, device simulation is performed on the structural results of the process simulation.

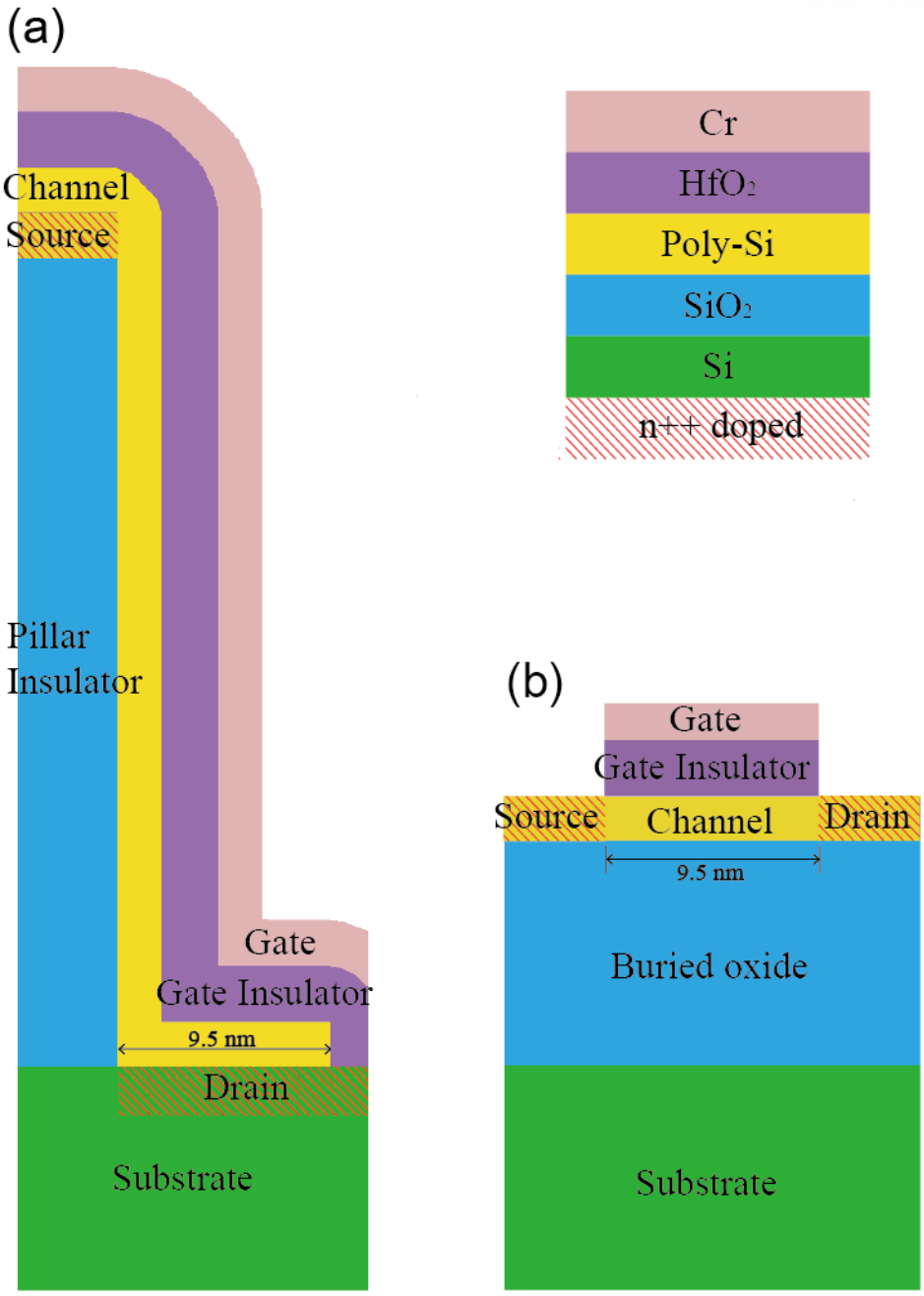

Figure 3.9 Schematic cross-sectional view for (a) of EO NMOSFET and (b) planar NMOSFET [39].

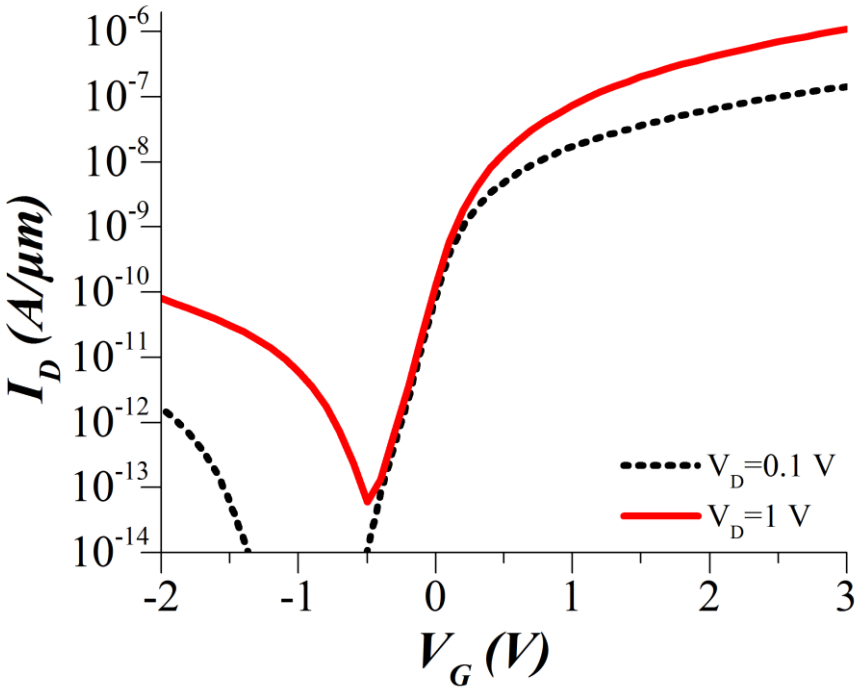

Figure 3.10 The calculated transfer characteristics of junctionless MOSFET, which is similar with the actual measurement (Figure.3 in [3-22]) [3-24 Figure.S1].

3.3.2 Method and fabrication procedure

TCAD was performed to investigate the operational characteristics of the proposed EO MOSFET, the channel band profile, the transfer characteristics, the output characteristics and carrier concentration were obtained. For comparison, another TCAD modeling was performed for a planar SOI MOSFET in same condition, the structural difference was came from insulating pillar (for example, height of device and length of effective channel) as shown in Figure 3.9(b).

The cross-sectional layer structure of the EO MOSFET is shown in Figure 3.9 (a), which is constructed by a fabrication process simulator, the fabrication procedure is briefly demonstrated as follows and illustrated in Figure 3.11. First step, a silicon oxide (SiO_2) is deposited on a Si substrate and 2 nm thick undoped poly-Si is deposited on the SiO_2 successively (Figure 3.11.i), in this step, the height of insulating pillar is determined by thickness of SiO_2 layer. Secondly, poly Si and SiO_2 are sequentially etched to form insulating pillars, and the etching process is performed on the same patterned photoresist layer (Figure 3.11.ii). Thirdly, implantation of phosphorus (NMOSFET) concentration of $\sim 10^{19}$ cm^{-3} or boron (PMOSFET) concertation of $\sim 7\times 10^{19}$ cm^{-3} is performed on poly-Si layer and Si substrate to define drain and source contact, in this step, insulating pillar define the source contact well region in self-aligned fashion and also take a role of precise positioned implantation mask (Figure 3.11.iii). Fourthly, undoped poly-Si is deposited into entire structure and etched to form the transistor channel with thickness of 2 nm (Figure 3.11,iv). Finally, HfO_2 is deposited with thickness of 2.5 nm for making gate insulator layer (Figure 3.11.v) and Cr (NMOSFET) or Ru (PMOSFET) is deposited on HfO_2 to form gate electrode (Figure 3.11.vi). In the fabrication process of EO MOSFET, defining regions of the transistor channel, gate insulator and gate electrode are constructed over sidewall due to insulating pillar with self-aligned source and drain contact. Based on this, EO-MOSFET can be considered topologically similar with planar MOSFET structure, which is regarded as 90 degrees rotation of entire transistor respect to Si substrate. In the TCAD modeling, the transistor channel size in lateral dimension is 9.5 nm as shown in Figure 3.9(a) with room temperature for both EO MOSFET and planar MOSFET. In order to induce large electric field perpendicular to gate electrode in the transistor channel, the thin transistor channel and the thin gate insulator are implemented, hence the gate bias control the channel potential effectively and DIBL is diminished [9][10].

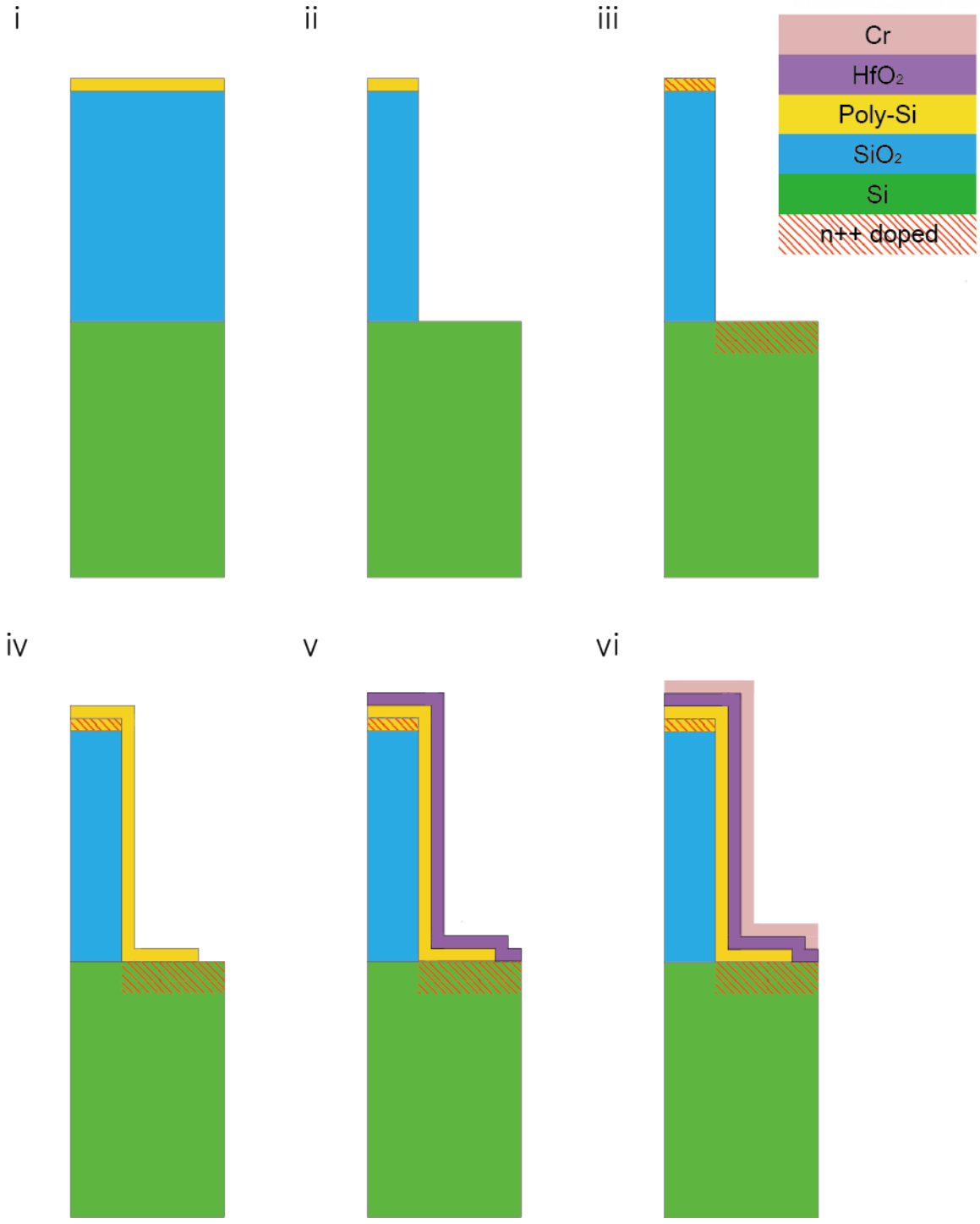

Figure 3.11 Fabrication process sequence of EO NMOSFET (Sequence is from ‘i’ to ‘vi’ in Roman numeral).

3.3.3 Electrical characteristics

Transfer characteristics and output characteristics

Output characteristics (vs. V_{ds}, source drain current vs. drain voltage) of the EO MOSFET with pillar height of 36 nm and planar MOSFET for gate overdrive voltages ($V_g - V_t$) are shown in Figure 3.12(a). The pillar height of EO MOSFET is set to 36 nm. As the drain bias is increased to 0.7V, the drain current of EO MOSFET saturates, but the drain current of planar MOSFET increases continuously due to short transistor channel. Transfer characteristics of EO MOSFET and Planar MOSFET are shown in Figure 3.12(b). In the transfer characteristics, difference of OFF-state current which defined to be the drain current at zero gate bias is obvious, the OFF-state current of EO MOSFET is much smaller than that of Planar MOSET in all drain biases. In specifically, when the drain bias is 0.5V, the OFF-state current of EO n-channel MOSFET (NMOSFET) is ~2.08×10^{-4} μA/μm and the OFF-state current of planar NMOSFET is ~0.119 μA/μm, hence planar NMOSFET has ~570 times larger OFF-state current than EO NMOSFET. However, the difference of OFF-state current is tend to decrease with large drain bias, because the OFF-state current of EO MOSFET shows the little upward trend in OFF-state. The reason for this upward trend in OFF-state current of EO MOSFET is explained in energy band diagram part. When the drain bias is 0.7V, the OFF-state current of EO NMOSFET and Planar NMOSFET are ~1.34×10^{-3} μA/μm and ~0.286 μA/μm respectively, therefore Planar MOSFET has ~213 times larger OFF-state current than that of EO NMOSFET. In the case of PMOSFET, similar trends are observed. Since the difference in OFF state current represents the difference of transistor power consumption, EO MOSFET outperform the planar MOSFET in relevant operation. In according to definition of DIBL, shift of the threshold voltage depending on the drain bias is DIBL. In case of EO NMOSFET, Very small DIBL is evaluated ~13.7 mV/V due to threshold voltage of 0.237 V and 0.228 V at the drain bias of 0.05 V and 0.7 V respectively. Also, the DIBL of EO PMOSFET is evaluated ~22.1 mV/V due to threshold voltage of -0.245 V and -0.231 V at the drain bias of -0.05V and -0.7V respectively. On the other hand, in case of planar NMOSFET, since the noticeable shift of threshold voltage is estimated from 0.119 V at the drain bias of 0.05 V to -0.06 V at the drain bias of 0.7V, resulting in the DIBL of ~275 mV/V. Similarly, the DIBL of planar PMOSFET is ~263.3 mV/V. All the DIBL of planar MOSFET is much larger than that of EO MOSFET, therefore DIBL of EO MOSFET is remarkably better than that of Planar MOSFET. As mentioned, the FinFET of TSMC by 7nm CMOS technology show the DIBL of ~35 mV/V, which is even large than the DIBL of EO MOSFET [23]. From transfer characteristics of Figure 3.12(b), the subthreshold swing is estimated as Table 3.1, which show the subthreshold swing for EO NMOSFET 62.2~63.6 mV/dec as drain bias increases from 0.05 V to 0.7 V. Likewise, the subthreshold swing for EO PMOSFET is 61.9~65.5 mV/dec in the drain bias from -0.05V to -0.7V. Meanwhile, in case of planar MOSFET, subthreshold swing in relevant drain bias range of EO

MOSFET is estimated to be 110.6~131.0 mV/dec for NMOSFET and 105.1~124.3 mV/dec for PMOSFET. It is remarkable that the subthreshold swing for ~62.6 mV/dec at the drain bias of 0.5V is close to the thermodynamic limit at room temperature.

Table 3.1 Subthreshold swing for EO MOSFET and Planar MOSFET, the height of insulating pillar is 36 nm in case of EO MOSFET [39].

$\lvert V_{ds} \rvert$ (V)	Subthreshold Swing (mV/dec)			
	EO MOSFET		Planar MOSFET	
	n-channel	p-channel	n-channel	p-channel
0.05	62.2	61.9	105.1	110.6
0.30	62.2	62.3	109.9	114.7
0.50	62.6	63.5	116.3	121.8
0.70	63.6	65.5	124.3	131.0

Transfer characteristics with change in insulating pillar height

As varying the height of insulating pillar, the transfer characteristics change of EO MOSFET at the drain bias of 0.5 V is shown in Figure 3.13. Since the height of insulating pillar is related with the effective channel length, it is reasonable that the subthreshold swing tends to be steep as the insulating pillar increases. In the case of minimum insulating pillar height (12 nm), the subthreshold swing is estimated to 69.9 mV/dec for NMOSFET and 75.2 mV/dec for PMOSFET, which is the maximum subthreshold swing in cases of Figure 3.13.

Transfer characteristics with change in temperature

Figure 3.14 shows the transfer characteristics of EO NMOSFET depending on temperature variation from 300 K (room temperature) to 400 K. As the temperature increases, since the channel carriers gain additional thermal energy, the channel current is increased in all bias. Likewise, the subthreshold swing changes to 67.6, 72.7, 77.9 and 83.0 mV / dec at temperatures 325, 350, 375 and 400K, respectively. In

according to relation between thermodynamic limit of the subthreshold swing and the temperature, $S.S \propto T$ from (3.3), the subthreshold swing for each temperature is also close to thermodynamic limit.

Transfer characteristics with change in the gate insulator thickness

The change in transfer characteristics with different gate insulator thickness from 2.5 nm to 10.0 nm is shown in Figure 3.15. Because the thickness of gate insulator determines the amount of potential drop in the gate insulator, hence the surface potential (or the effective electric field in the channel) is also related with the gate insulator thickness. In this manner, thicker gate insulator reduces the effective electric field in the channel, leading to the degradation of channel controllability. As increase of gate insulator thickness from 5.0 nm to 10.0 nm, the subthreshold swings are estimated 64.3, 68.3 and 73.9 mV/dec, respectively, which did not deviate significantly from the thermodynamic limit.

Transfer characteristics with grain boundaries in poly-Si channel

In our TCAD modeling, poly-Si is used for transistor channel, which properties are determined with the synthesis quality of poly-Si. In the view of material properties, the operational characteristics of EO MOSFET can be affected by the grain boundaries of the poly-Si. Therefore, additional TCAD modeling with existence of grain boundaries in poly-Si channel was performed, in this modeling, grain boundary is assumed to be amorphous Si in consideration of the poly-Si synthesis process. Figure 3.16 shows the transfer characteristics for existence of grain boundaries at drain bias of 0.5 V. As the number of grain boundaries increases, there is little deviation in transfer characteristics under subthreshold condition. All the TCAD modelings except this grain boundary case are performed without grain boundaries in transistor channel, because showing operational feasibility of EO MOSFET is the main goal of the research. Furthermore, low pressure chemical vapor deposition (LPCVD) can deposit the poly-Si which having grain size over 100 nm, hence there is rare possibilities for EO MOSFET with the tens of nano-meter transistor channel containing the grain boundaries. In conclusion, for the purpose of the research to showing operational characteristics especially on DIBL and subthreshold swing, the inclusion of grain boundaries is seems to be lowly relevant.

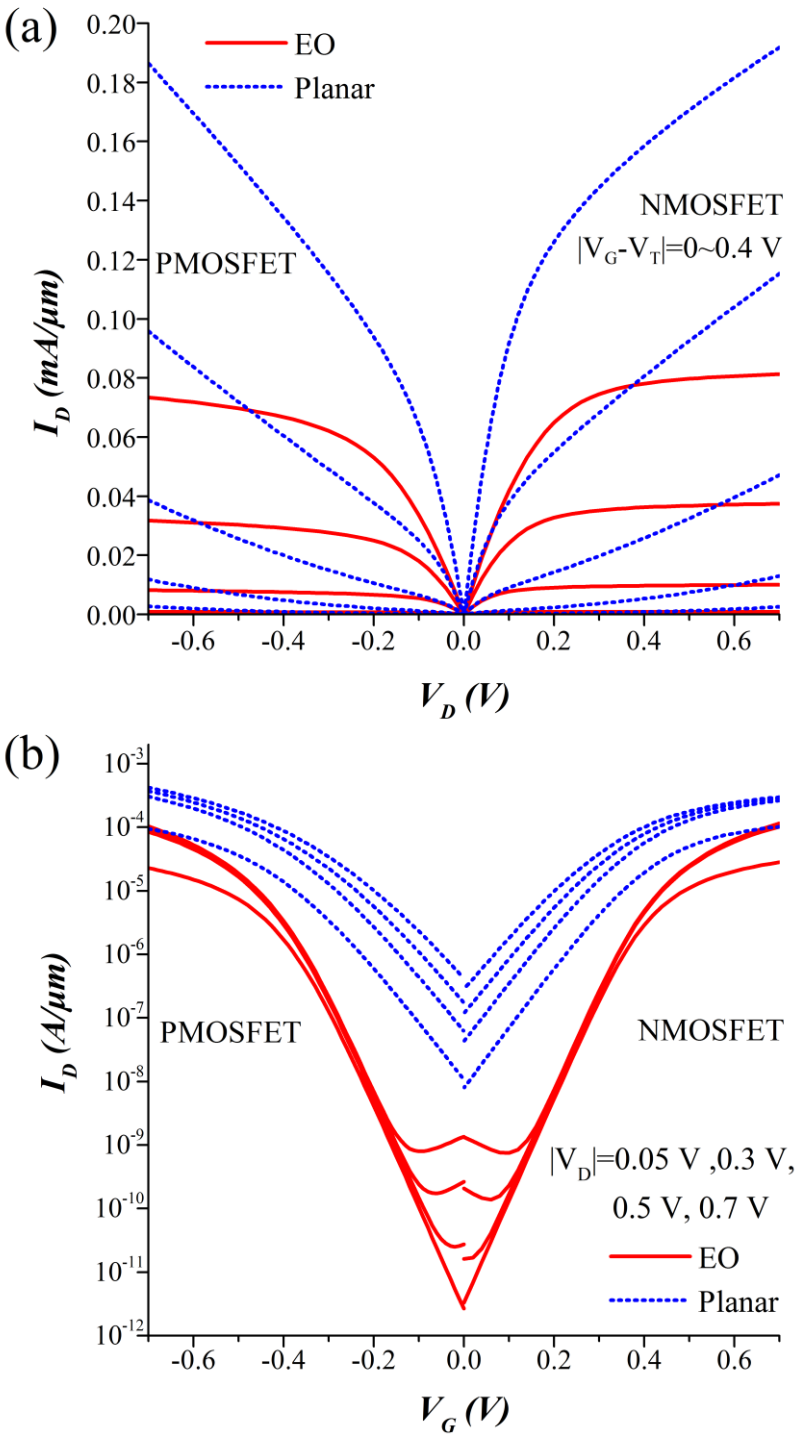

Figure 3.12. (a) The calculated output characteristics of EO MOSEET and planar MOSFET for the gate overdrive from 0 to 0.4 V. (b) The calculated transfer characteristics of EO MOSFET and Planar MOSFET for the drain bias from 0.05 V to 0.7V. In case of EO MOSFET, the height of insulating pillar is 36 nm. [39]

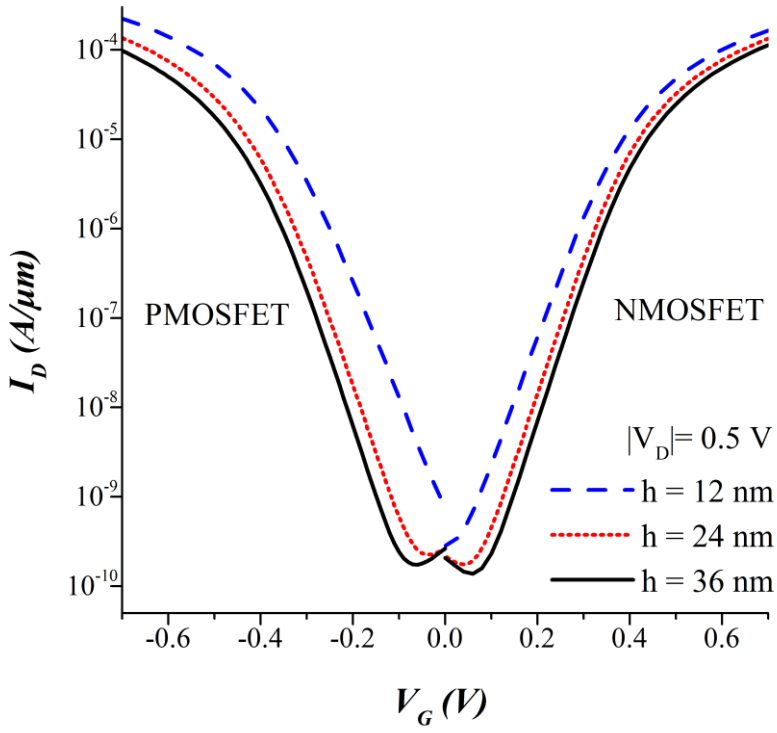

Figure 3.13. Transfer characteristics calculated with insulating pillar height of 12, 24 and 36 nm at drain bias of 0.5 V [39].

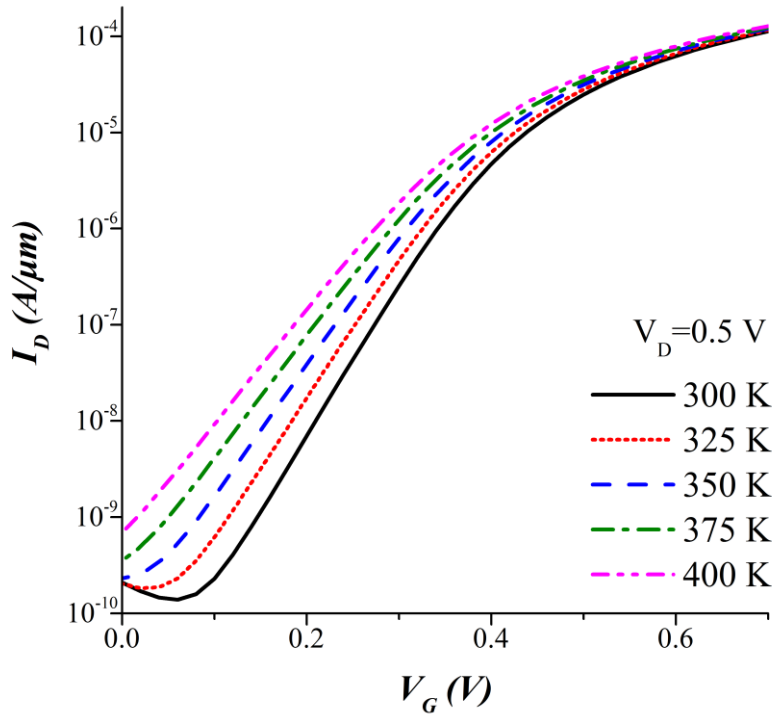

Figure 3.14. Transfer characteristics calculated with temperatures from 300 K to 400 K at drain bias of 0.5 V [39].

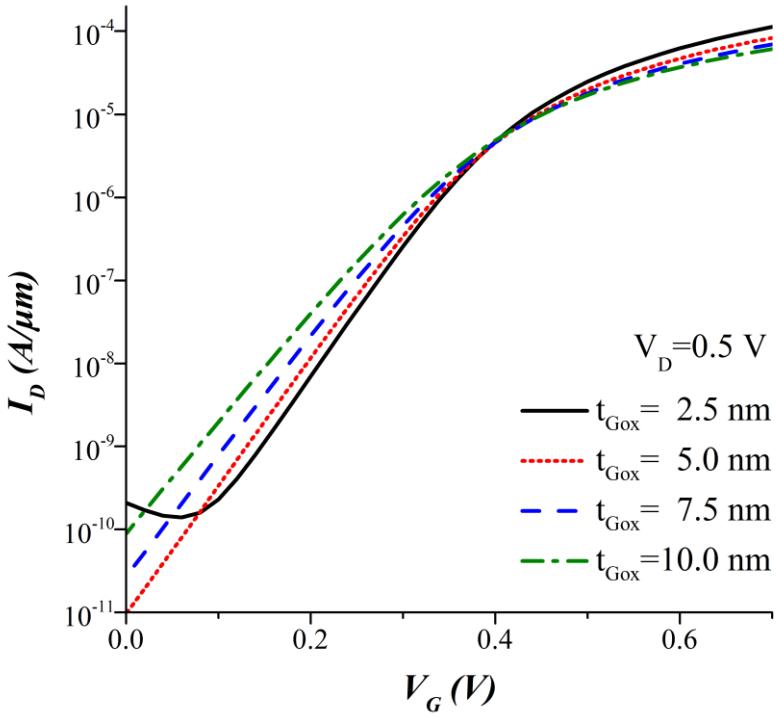

Figure 3.15. Transfer characteristics calculated with varying the thickness of gate insulator from 2.5 nm to 10.0 nm at drain bias of 0.5 V [39].

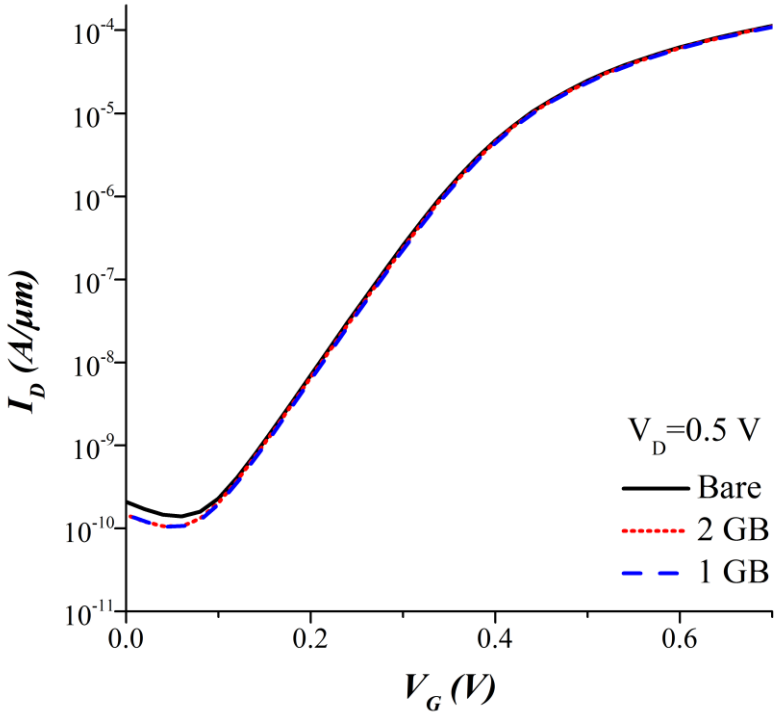

Figure 3.16. Transfer characteristics calculated with the grain boundaries in the transistor channel at drain bias of 0.5 V.

3.3.4 Energy band and carrier concentration

Energy band

The OFF-state energy band profiles along the transistor channel of EO MOSFET and planar MOSFET are shown in Figure 3.17(a) for NMOSFET at the drain bias of 0.5 V and Figure 3.17(b) for PMOSFET at the drain bias of -0.5 V. The conduction band maximum along the channel is ~0.419 for EO NMOSFET and ~0.268 for planar MOSFET, which referenced from the grounded electrode. Apparently, the difference of DIBL between the EO NMOSFET and planar NMOSFET makes the large difference on the conduction band maximum along the channel, similarly, there are large difference on the valance band minimum along the channel between EO PMOSFET and planar PMOSFET. The main carrier type of OFF-state current can be expected by energy band profiles, which is looks different between the two devices. In case of EO NMOSFET, the electron transport on thermionic emission from the source to the drain is easily blocked by the large conduction band maximum in the transistor channel, also, carrier transport on direct tunneling between the source and the drain is prevented by the relative long effective channel length. Meanwhile, since the valance band barrier become thinner as drain bias increases, some holes near the drain electrode may be quantum tunneled into the valence band. In the case of planar MOSET, the low conduction band maximum and the relative short channel length is favourable to thermionic emission and direct tunneling between the source and drain [38]. Also, the OFF-state current of planar MOSFET is much larger than that of EO MOSFET as shown in Figure 3.12(b). Hence, in the OFF-state for the planar MOSFET, the electron transport by the thermionic emission and the electron tunneling is enough to overwhelm the hole tunneling transport.

Carrier concentration

Figure 3.18 shows the electron and hole concentration of ON-state (the gate bias is 0.7 V) and OFF-state with the drain bias of 0.5 V. In the OFF-state, almostly the intrinsic electrons are existed, meanwhile the holes are induced by the hole tunnelling as described before. On other hands, in the On-state, only the intrinsic holes are existed, meanwhile the electrons are induced mostly by electrostatic potential. Hence, the EO MOSFET has the fully depleted channel, which is the evidence for the steep subthreshold swing. In summary, the relatively longer transistor channel at the same lateral channel length and the thin fully depleted channel make the steep subthreshold swing for EO MOSFET.

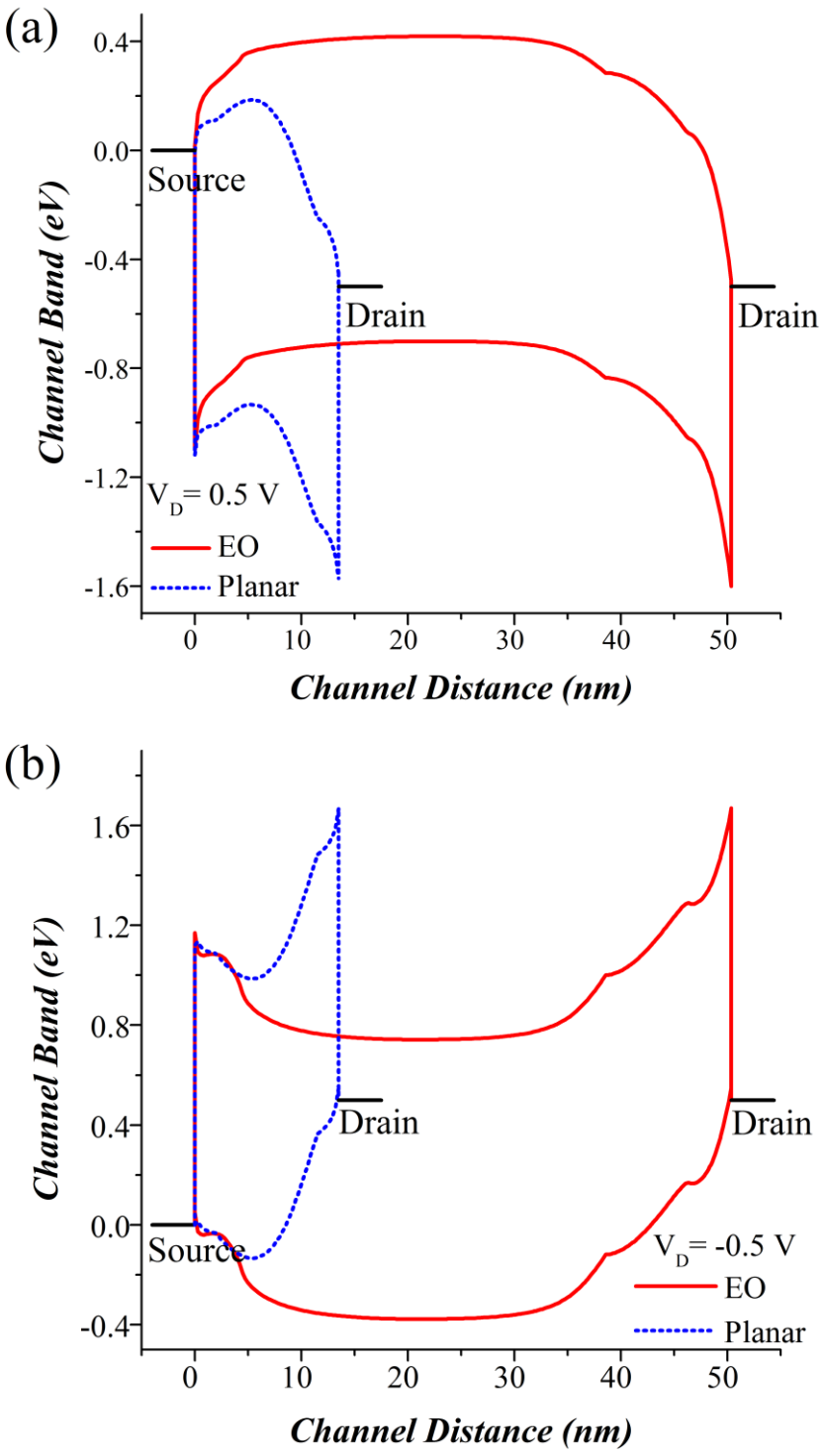

Figure 3.17. The channel energy band diagram of EO MOSFET and planar MOSFET in the case of (a) NMOSFET and (b) PMOSFET [39].

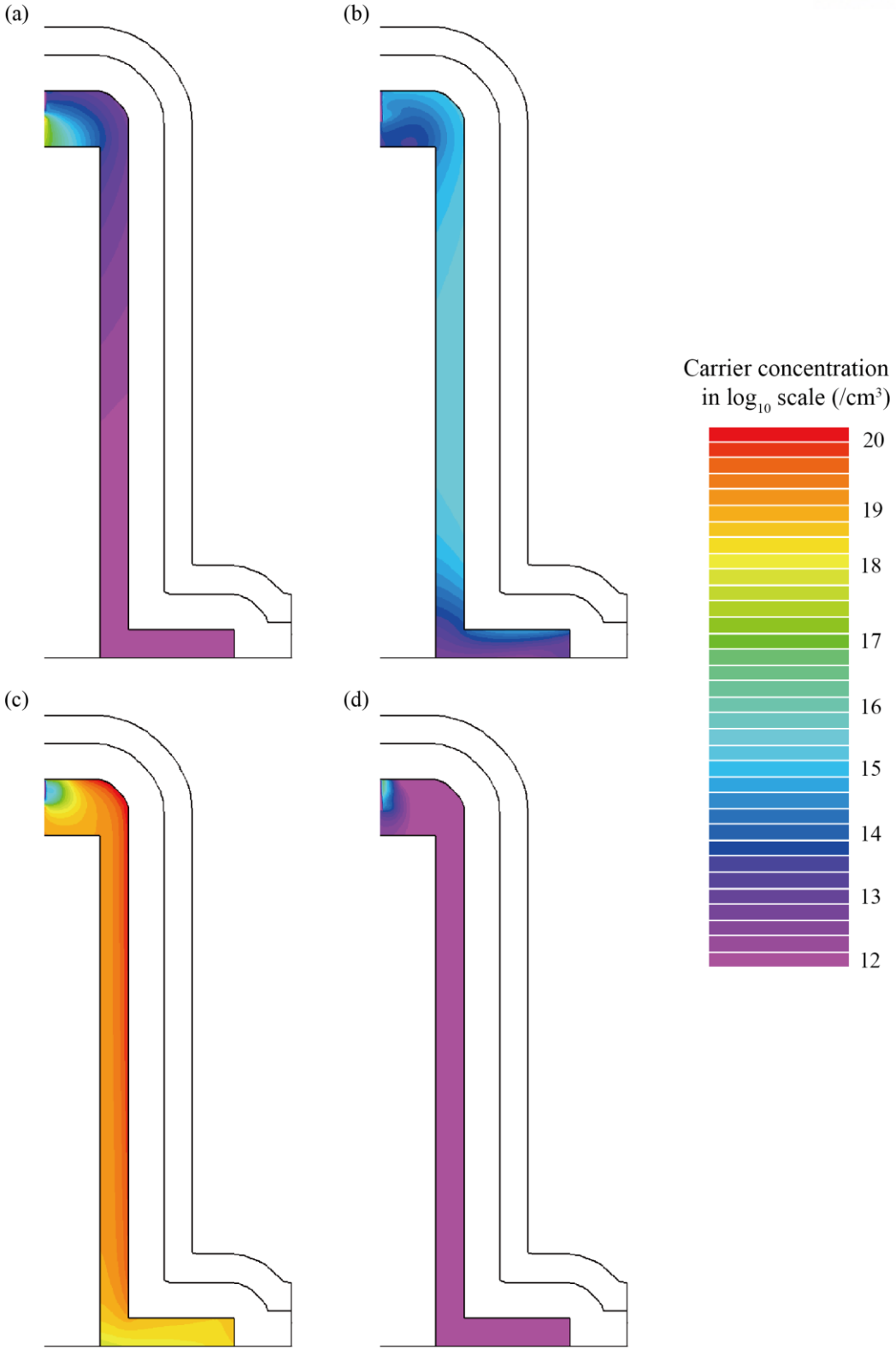

Figure 3.18. Schematics show (a) electron concentration at OFF-state, (b) Hole concentration at OFF state, (c) electron concentration at ON-state and (d) hole concentration at ON-state, all the cases are calculated at drain bias 0.5 V. Carrier concentrations are express in $\log_{10}$ scale.

3.3.5 Conclusion

The EO MOSFET is proposed, which structure is composed by a MOSFET with an insulating pillar, and its operational characteristics of EO MOSFET were investigated with TCAD modeling. Since the existence of insulating pillar elongate the transistor channel to perpendicular for Si substrate which formed over the sidewall of the insulator pillar, the effective channel length is enlarged without changing the transistor lateral pitch. In the same manner, extreme scaling on lateral pitch can be possible due to the part of transistor channel in vertically formed on sidewall of insulator pillar. From the TCAD modeling, the EO MOSFET shows the very low DIBL due to the long effective channel length in fully depleted. In same reason, the subthreshold swing of EO MOSFET is close to thermodynamic limit at temperatures from 300 K to 400 K, and it is improved on the insulator pillar height increases. In summary, the EO MOSFET with lateral channel size of 9.5 nm and the insulator pillar height of 36 nm in drain bias of 0.5 V shows the subthreshold swing of ~62.6 mV/dec and the low DIBL of ~13.7 mV/V. The fabrication process of EO MOSFET can be included in the present Si CMOS technology and provide the way to the ultimate scaling on lateral dimension of several nm size while diminishing the degradation of DIBL and subthreshold swing.

IV. Edge-over Ternary Inverter

The CMOS inverter is the most elementary part of logic circuit, it is called 'not logic gate'. Typically, CMOS composed with PMOSFET and NMOSET in pair, Figure 4.1(a) shows the cross-sectional view of CMOS with planar MOSETs, and its circuit diagram is illustrated in Figure 4.1(b). Conventionally, most of the computational system constructed with binary logic which is about the state '0' and '1', however there were continuous efforts to constructing multi valued logic and multi valued logic systems in last decades. In this chapter, the ternary inverter which composed with EO MOSFETs and two resistors on integrated circuit is described with the operational characteristics which obtained from TCAD mixed mode.

4.1 Introduction

The improvement of the fabrication technology and the efficient layout of integrated circuit makes higher information processing density in the CMOS technology. As the drastic scaled down of MOSFET, power consumption of the transistor was involved with parasitic leakage current, as mentioned in previous chapter, one of the most concerned leakage currents is the subthreshold current induced by increases of DIBL and the subthreshold slope. In order to suppress the subthreshold swing, there are several efforts which described at the chapter III. Meanwhile, other attempts are existing for achieving higher information processing density by constructing multi-valued logic system beyond binary logic system.

4.1.1 Ternary logic circuit

The theory which describes the complexity of the logic circuit has two main perspectives [4-1]. The first point of view is based on the assumption that the cost of logic circuit (which determined by the total number of gates and inputs) and the complexity of logic circuit are independent of different multivalued logic, hence the complexity reduction ΔC from n-valued to m-valued is [40]

$$\Delta C = \frac{\log n}{\log m} \tag{4.1}$$

In this point of view, the complexity reduction of binary system to ternary system is ~ 63.1%. The second point of view assumes that the complexity of the logic circuit is proportional to the multivalued capacity [40]:

$$\Delta C = \frac{m \log n}{n \log m} \tag{4.2}$$

In according to the second point of view, the complexity reduction of binary system to ternary system is ~94.6 %. In addition, the lowest complexity to binary logic circuit is the ternary logic circuit case in the second point of view. In summary, both perspectives explained the reduction of complexity from binary logic circuit to ternary logic circuit. Since the number of logic cells and the complexity of interconnects are reduced with the ternary logic circuit, the power consumption of entire system decrease [40 - 44].

For the past few decades, study on the ternary logic operation and the ternary logic system were progressed widely. There are mainly two approaches to constructing ternary characteristics, the first approach is making ternary transistor using by novel device materials or unique transistor characteristics, the second approach is constructing ternary circuit using by additional electronic components [41 - 48]. In the carbon nanotube (CNT) FET, ternary logic cells are constructed by the geometric dependence (diameter and the chirality) of threshold slope [41]. Since the shift of the effective workfunction by metal strip on graphene make additional current state, complementary ternary graphene FET can be constructed [42]. Tungsten diselenide (WSe_2)/graphene hetero-junction device shows the ternary characteristics with photo-induced current [43]. Quantum dot gate FET exhibits ternary characteristics due to the quantum tunneling of carrier from channel to quantum dots [44]. In the MOSFET, since the engineering of band-to-band tunneling at OFF state, which is undesirable in usual CMOS technology, provides the ternary state in CMOS inverter [45]. Nevertheless, challenging fabrication or limit of the device operation frequency are remained [42 - 45]. In the case of ternary circuit using by additional electronic components with conventional transistor, the ternary CMOS requires additional dimension compared to the binary CMOS, hence the higher information density in area is not guaranteed [40][46 - 48].

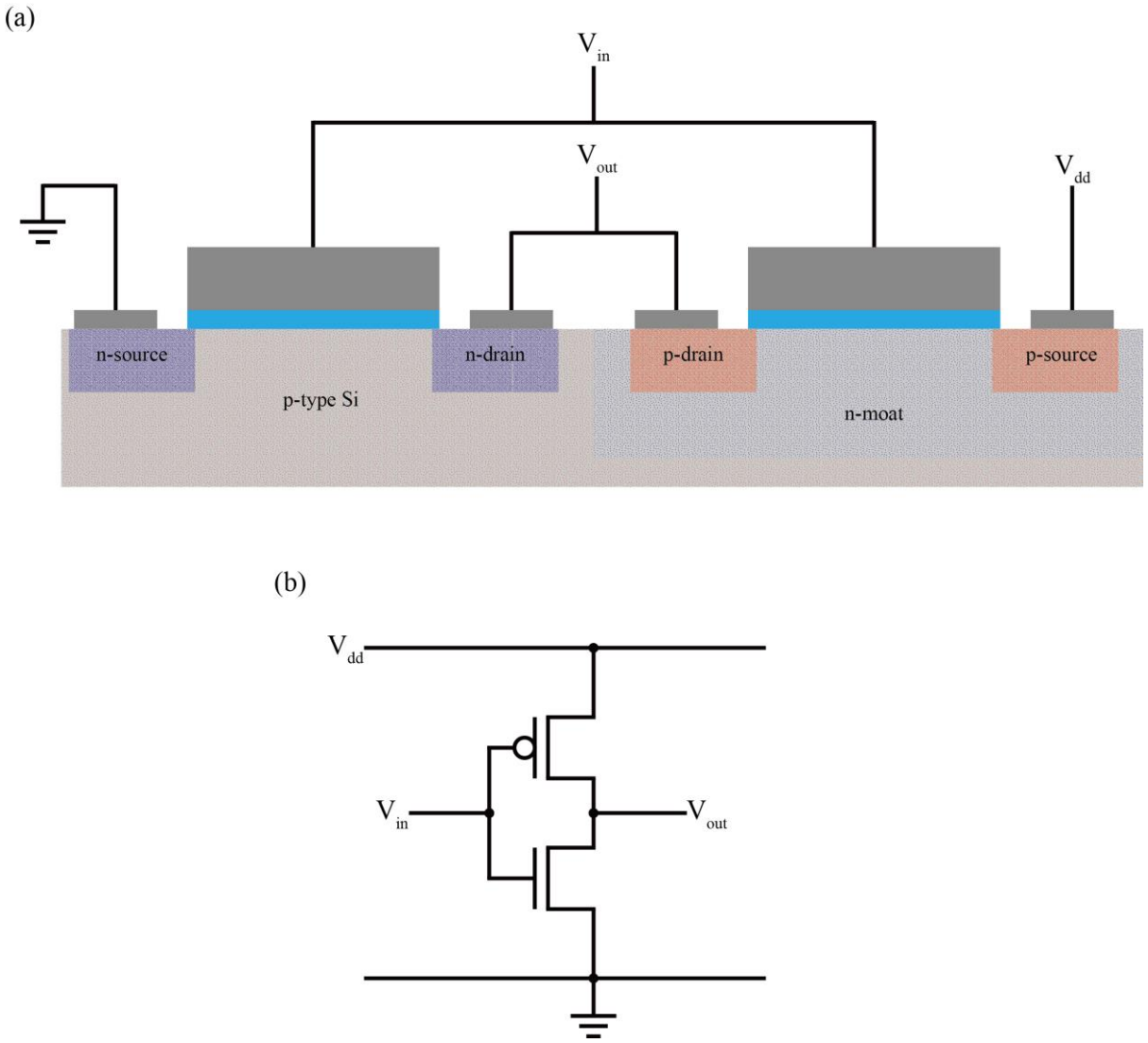

Figure 4.1 (a) Schematic cross-sectional view of a conventional binary CMOS inverter with planar MOSFETs, and (b) Circuit diagram of relevant CMOS inverter, CMOS consists of NMOSFET and PMOSFET.

4.2 Edge-over Ternary Inverter

As mentioned in previous section, since the ternary CMOS inverter with additional electronic components occupy the relatively large dimension, which has the disadvantage to achieve higher information density. However, if the electronic components can be located in the vertical direction such as EO MOSFET, the disadvantage of large area occupancy can be ignored. In this regard, we propose the EO Ternary Inverter which composed by unique EO resistor and EO MOSFET. EO resistor is designed to enlarge in perpendicular direction to the substrate, hence the resistor is formed over the sidewall of insulating pillar, top of the insulating pillar, and over the trench isolation as illustrated in Figure 4.5.

4.2.1 TCAD mixed mode methodology for EO ternary inverter

Operational characteristics of EO ternary inverter are investigated by TCAD mixed mode, which is the circuit simulator similar with simulation program with integrated circuit emphasis (SPICE), the different aspect between mixed-mode and SPICE is that TCAD modeling can be applied to the circuit simulation in mixed-mode. In other words, physical device simulation is performed in TCAD mixed mode for significant device such as EO MOSFETs in our case, and the rest of circuit is simulated with conventional compact circuit model used as compact models in SPICE [3-20]. However, differences of device simulation between TCAD and TCAD mixed-mode exist due to the computational limitation, which arouse by massive physical device simulation with complex device structure.

In the TCAD mixed-mode for EO ternary inverter, 2 device simulations are required for the electrical characteristics of NMOSFPET and PMOSFET, which structures was constructed by TCAD modeling. In the simulation, EO MOSFET has insulating pillar height of 36 nm, polysilicon channel thickness of 5 nm, HfO2 gate insulator thickness of 2.5 nm. The rest of systems are two resistors R_1 and R_2, V_{dd} voltage supply and ground as illustrated in Figure 4.2. Load capacitance is determined by gate capacitance of EO MOSFETs in C-V curves for transistor width of 1 μm as shown in Figure 4.3, capacitance of EO NMOSFET and PMOSFET are ~ 4 fF. In the device simulation in TCAD mixed-mode, following physical models are included: Shockley-Read-Hall recombination model, Auger electron-hole recombination model, parallel electric field dependence model, Klaassen band-to-band tunneling model, and Uchida's low field model [3-20]. As mentioned in the chapter III, Uchida's low field model is included for quantum confinement effect in thin poly-Si channel thickness of 5 nm.

4.2.2 Edge-over Ternary Inverter

In the EO MOSEFET describe in Chapter III, insulating pillar extends the transistor channel in a direction perpendicular to the substrate. Likewise, EO resistor is enlarged with insulating pillar as shown in Figure 4.4.(a), hence the EO resistor is formed on the upper surface of insulating pillar, the lower part is formed on the shallow trench isolation (STI) surface and vertical part is formed on the sidewall of the insulating pillar. Figure 4.4.(b)(c) shows top view of EO resistor as the position variation of resistor end, four different cases show the possibility of circuit configuration regardless of the location of the interconnection between devices.

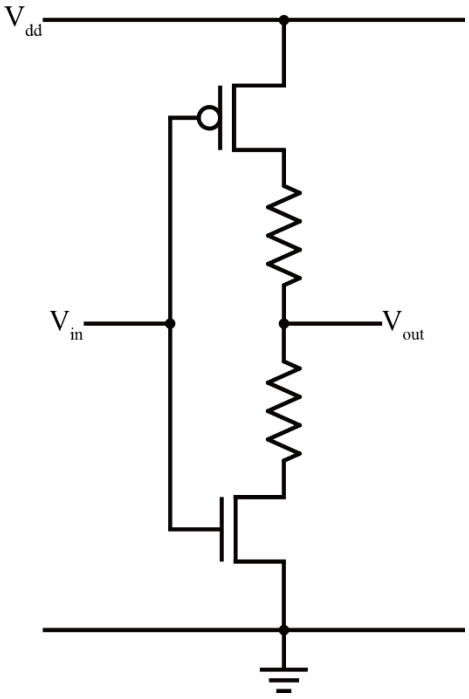

Figure 4.2 Circuit diagram of ternary inverter consisted by two resistors, NMOSFET and PMOSFET.

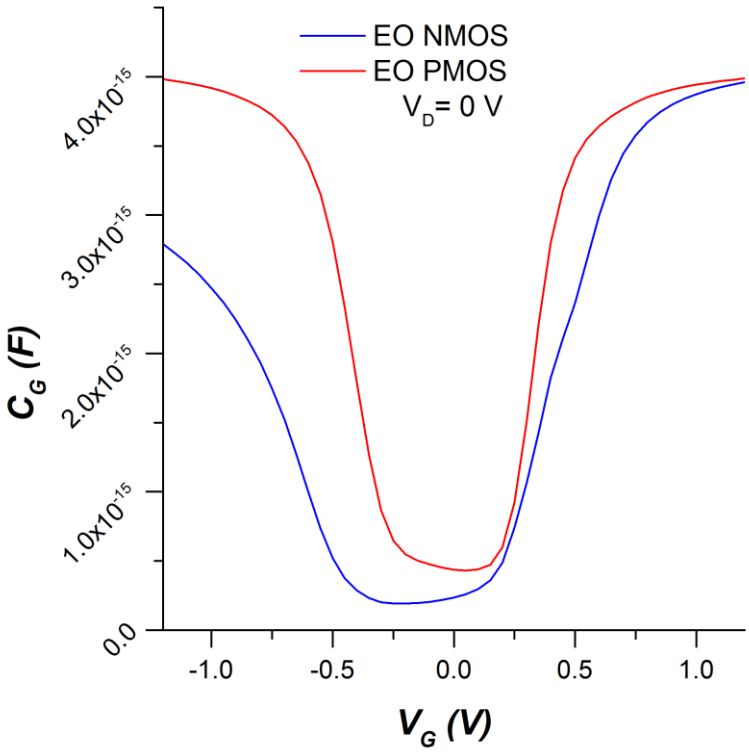

Figure 4.3 Gate capacitance of EO MOSFETs at drain bias of 0 V, blue is for NMOSFET and red is for PMOSFET.

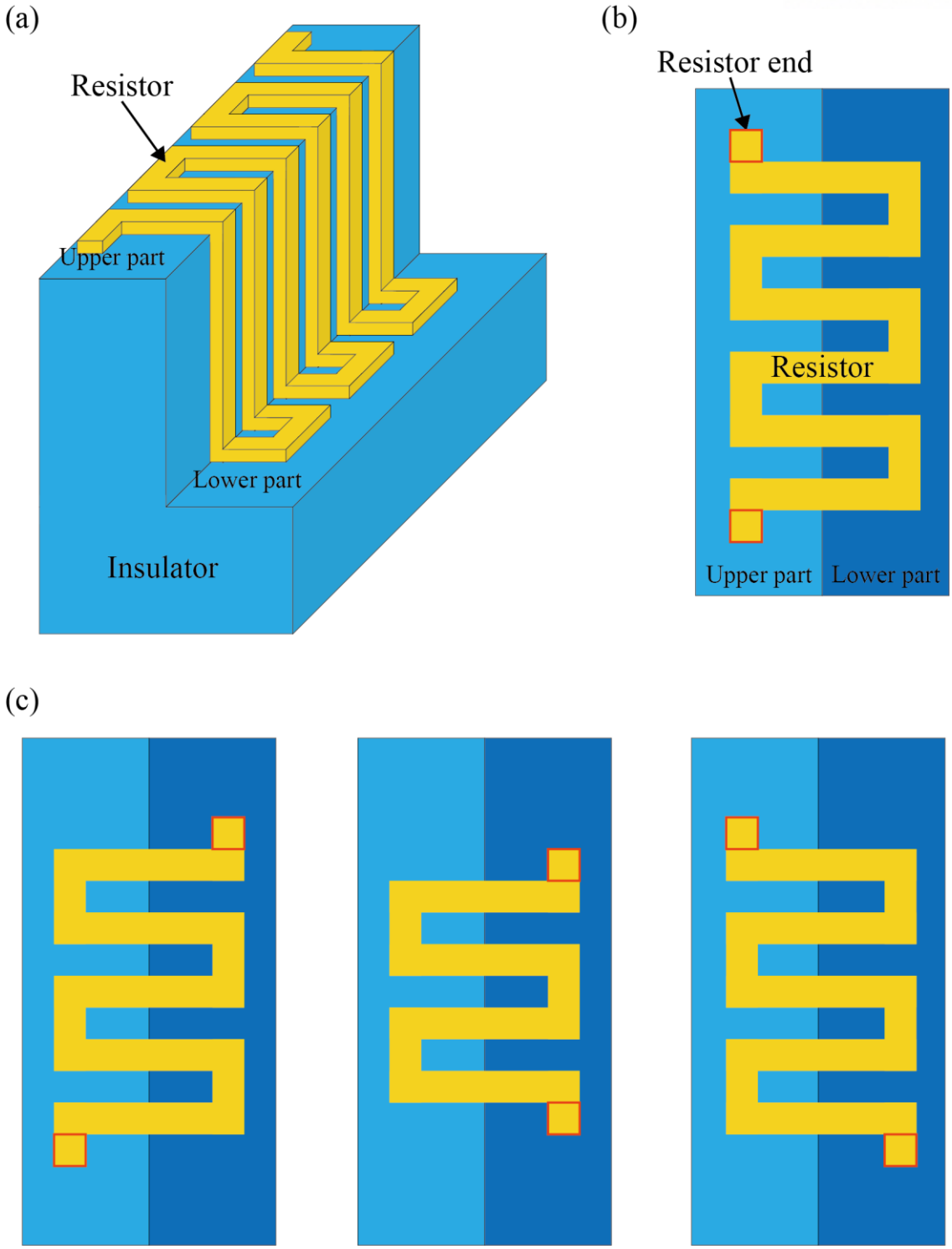

Figure 4.4 (a) 3-dimensional view of EO resistor in an insulating pillar step structure, which is not necessarily located on same material. Top view of EO resistor with resistor end (red square) illustrate (b) the same structure of (a), and (c) the cases of EO resistor end variation.

4.2.3 Procedure of EO ternary inverter structure

Figure 4.5 shows the sequential fabrication process of EO ternary inverter composed by EO CMOS and EO resistors, brief explanations of fabrication process for EO ternary inverter follows the sequence of Figure 4.5:

Firstly, STI of SiO_2 on Si substrate which separates the NMOSFET and PMOSFET is constructed, hence the leakage current between NMOSFET and PMOSFET can be diminished (Figure 4.5.i).

Secondly, a SiO2 layer is deposited on Si substrate and STI, height of insulating pillar is determined by thickness of SiO2 layer in this step, and 5nm poly-Si thin film is deposited on SiO2 sequentially (Figure 4.5.ii).

Thirdly, poly-Si and SiO2 layer is etched successively with same pattern for define pillar region, hence edges of poly-Si and insulating pillar are matched as self-aligned fashion (Figure 4.5.iii).

Fourthly, Phosphorus concentration of $\sim 10^{19}$ cm^{-3} and boron concentration of $\sim 7 \cdot 10^{19}$ cm^{-3} are implanted on the patterned region to make drain and source of NMOSFET and PMOSFET, respectively (Figure 4.5.iv). In this step, the doped regions on the substrate are defined by the STI and the insulating pillars.

Fifthly, poly-Si on the insulating pillar is etched in pattern to separate each device element region (Figure 4.5.v), hence the inaccuracy of poly-Si doping patterned on topside of insulating pillar is revised.

Sixthly, patterned 5nm thick Poly-Si is deposited to define channel of MOSFETs and resistors (Figure 4.5.vi).

Seventhly, poly-Si for the EO resistor is implanted with phosphorus and boron to activate resistance (Figure 4.5.vii).

Eighthly, HfO2 layer is deposited on all the region which becomes gate insulator and protective layer of resistor (Figure 4.5.viii).

Finally, Cr and Ru gate electrodes are formed on HfO2 layer for NMOSFET and PMOSFET, respectively (Figure 4.5.ix).

In our structure, EO structure enlarges the channel and resistor in perpendicular direction to substrate which decreases the lateral dimension of MOSFETs and resistors, thus high density integrated circuits can be possible. Moreover, Self-aligned design allows to define the source and drain regions feasibly.

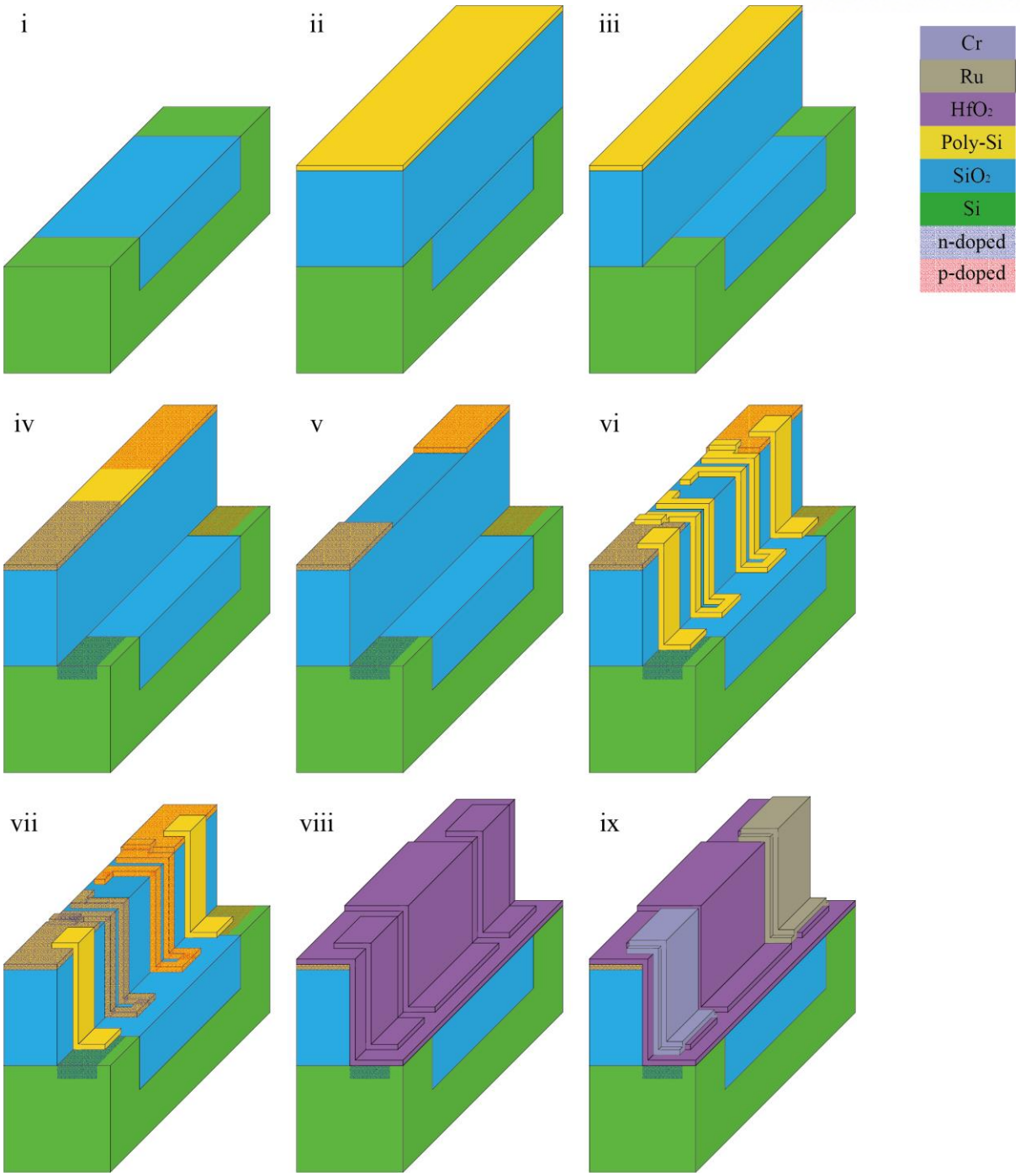

Figure 4.5 Sequential process of the ternary CMOS inverter, which composed by EO MOSFETs and EO resistors.

4.2.4 Electrical characteristics

V_{in}-V_{out} curves of ternary inverter

V_{in}-V_{out} curves (or voltage transfer characteristics, VTC) of EO inverter which transistor width of 1.0 μm are investigated with the resistance change of 50, 100, and 200 kΩ as shown in Figure 4.6. As the resistance of resistor increases, ternary characteristic become apparent, which is induced by change of potential distribution. In according to the circuit configuration as shown in Figure 4.2, gate bias of CMOS is determined by difference of input voltage V_{in} and V_{dd} voltage supplier, $V_{in} - V_{dd} = V_{Gp}$ for PMOSFET and difference of input voltage and ground, $V_{in} - V_{ground} = V_{in} = V_{Gn}$ for NMOSFET, hence the gate bias of the transistor is same with binary inverter. However, potential across the inverter is different with binary inverter as existence of resistors, which is given by ohm's law:

$$V_{dd} = I(R_p + R + R + R_n) = V_p + V_R + V_R + V_n \tag{4.3}$$

Where, R_p and R_n is resistance of EO MOSFETs, and R is resistance of a resistor, and potential of PMOSFET, a resistor and NMOSFET are V_p, V_R and V_n, respectively. In according to series resistance of inverter, current across inverter I is same in CMOS and resistors. When the input voltage approach to 0 or V_{dd}, total resistance of the inverter is dominated by resistance of OFF-state transistor. In the intermediate input voltage around $\sim V_{dd}/2$, since NMOSFET and PMOSFET are on-state, total resistance of inverter is dominated by resistance of resistors. As a result, the ternary state of the inverter appeared due to the presence of resistors, and the resistance ratio of resistors determines the voltage of intermediate state.

Figure 4.7 shows the V_{in}-V_{out} curves of EO inverter as transistor width of 0.2, 0.5 and 1.0 μm with the resistor resistance of 200 kΩ. As decrease of transistor channel width, the ternary characteristic is diminished due to transistor resistance, which has relation:

$$\text{Resistance} \propto \frac{L_r}{A_r} \tag{4.4}$$

Where, L_r is the length, and A_r is the cross-sectional area. As the relation of (4.4), width of transistor is proportional to the cross sectional area, therefore the increase of width is inverse proportional to transistor resistance. In this regard, since the transistor width is related with potential distribution on inverter, the resistance of resistors also needs to be changed to achieve ternary state. For example, narrow transistor width requires higher resistance of resistors to achieve the stable ternary state, inversely, wide transistor width requires lower resistance of resistors.

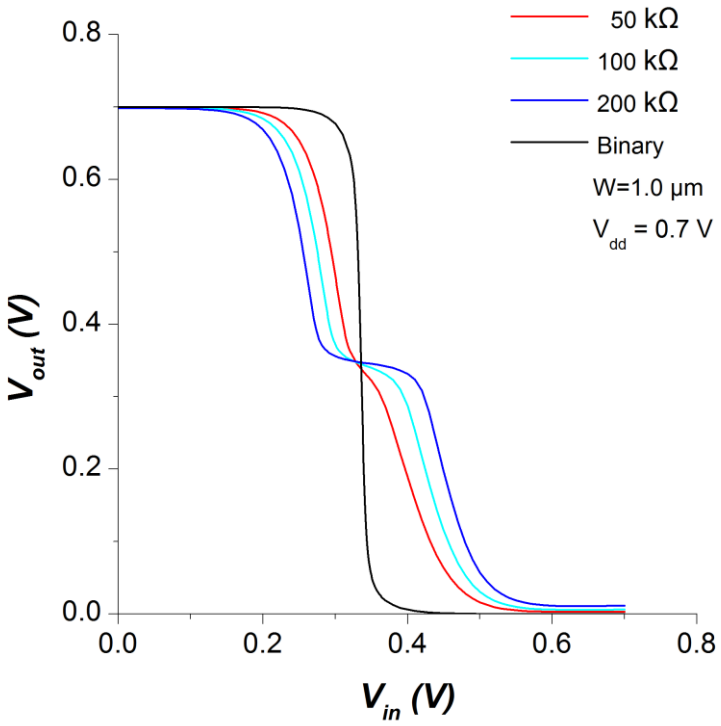

Figure 4.6 V_{in}-V_{out} curves for EO inverter as changing resistor's resistance from 0 to 200 kΩ clearly shows ternary characteristics.

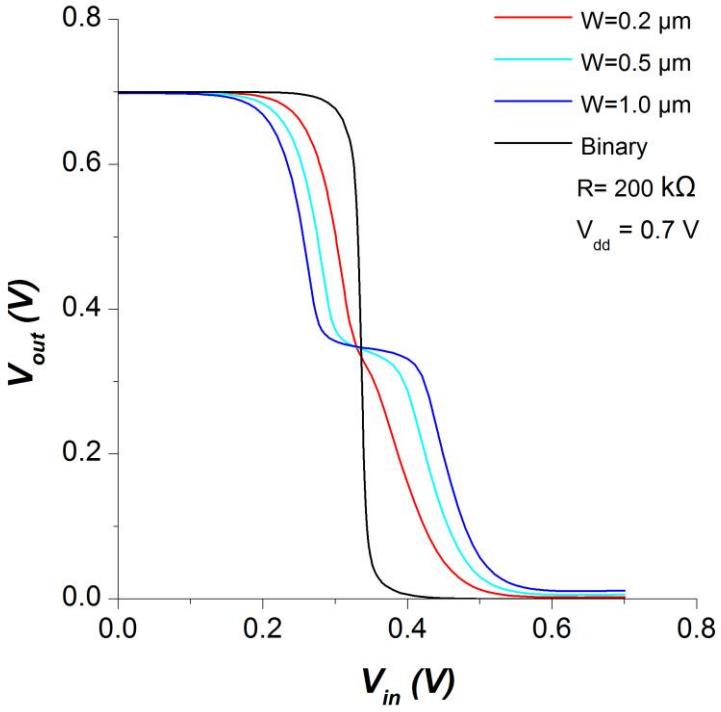

Figure 4.7 V_{in}-V_{out} curves of EO inverter as change of transistor width from 0.2 to 1.0 μm, the ternary characteristics.

Static noise margin (SNM)

In the logic circuits, static noise margin (SNM) evaluates the noise tolerance, which is generally important in combinational cells. One of most well-known SNM evaluation is determined by diagonal distance of maximum possible inscribe square in butterfly curves [4-10]. In the ternary inverter, there are 2 more VTC crossed regions due to the third state, therefore SNM of the third state can be evaluate by sum of two SNM around the third state. In this regard, ideal SNM of ternary inverter $SNM_{ternary}^{ideal}$ can be expressed by

$$SNM_{ternary}^{ideal} = \frac{\sqrt{2}V_{dd}}{3} \tag{4.5}$$

Figure 4.8 shows butterfly curves for different transistor width of 0.2, 0.5, and 1.0 μm with 200 kΩ resistors at drain bias of 0.7 V. As increase of the transistor width from 0.2 μm to 1.0 μm, SNM for V_{dd} and 0 is decreased from 290 mV to 220 mV, they are in considerable range compare to ideal SNM of ~ 330 mV. However, 0.2 μm transistor width case which shows best SNM for V_{dd} and 0 in Figure 4.8 is nearly binary characteristics in V_{in}-V_{out}, and there is no noise tolerance in the intermediate state. As mentioned before, since third state can be induced by the potential distribution of the inverter by adjusting the resistance of resistors, hence a narrow width transistor can be achieved the ternary characteristics by increasing the resistance of resistors. Meanwhile, SNM of the third state for transistor width of 0.5 and 1.0 μm are 49 mV and 115 mV, respectively, which is relatively low compared with SNM for V_{dd} and 0, but it can be improved by resistors.

Figure 4.9 shows the butterfly curves with V_{dd} changing from 0.5 V to 1.1 V, which inverter is consisted with 200 kΩ resistors and transistors width of 1.0 μm. As increase of V_{dd}, SNM for V_{dd} and 0 is decrease from 229 mV to 193 mV, while SNM of third state is enlarged from 115 mV to 623 mV, however, V_{dd} of 0.5 V shows binary characteristics in V_{in}-V_{out}. The range changing of third state by V_{dd} in Figure 4.9 is explained by the range of near threshold operation of transistors. In other words, when the transistor operates only in subthreshold condition around $V_{dd}/2$, the high resistance of the transistor dominates the total resistance across the inverter, hence there may be only binary characteristics or small range of intermediate state. In this respect, the threshold voltage engineering is required for the target V_{dd}. At another point, shifting the threshold voltage by changing V_{dd} may be possible in accordance with DIBL and subthreshold swing, however the nature of EO MOSFET for low DIBL and steep subthreshold diminishes the shift of threshold voltage.

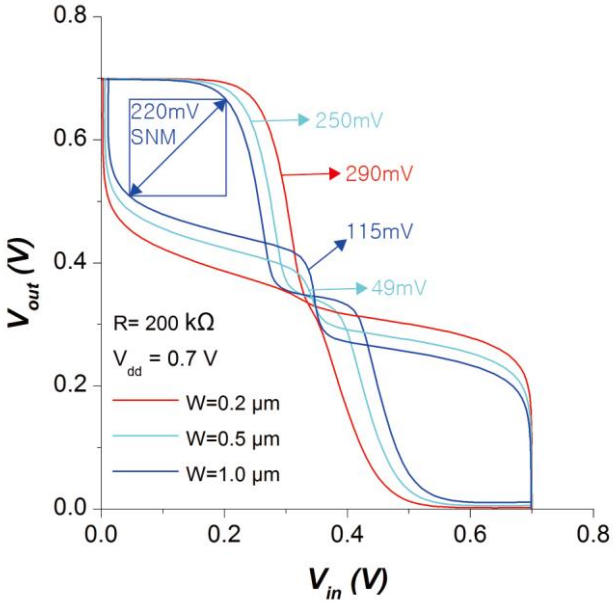

Figure 4.8 Butterfly curves for different transistor width of 0.2, 0.5, and 1.0 μm with 200 kΩ resistors at drain bias of 0.7 V. Static noise margin (SNM) is determined by diagonal distance of maximum possible inscribe square to butterfly curves.

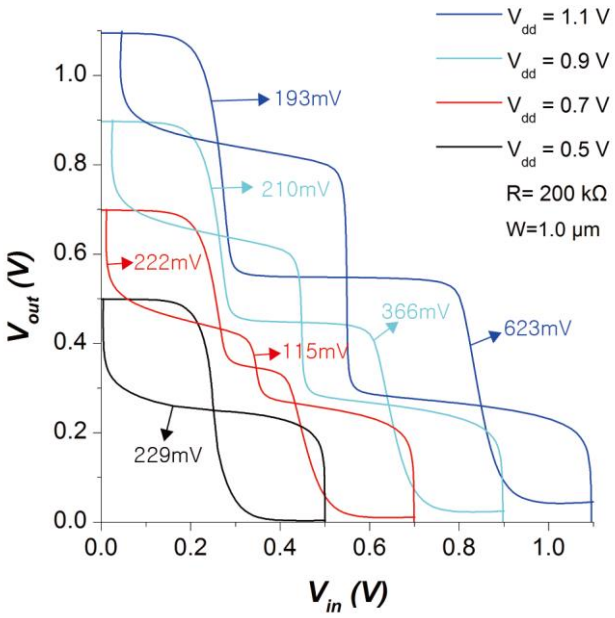

Figure 4.9 Butterfly curves for different V_{dd} from 0.5 V to 1.1 V with 200 kΩ resistors and transistor width of 1.0 μm.

Resistors and transistor width mismatching

In the fabrication of EO ternary inverter, there are possibilities of mismatching on resistors and transistor width. In this manner, operational characteristics are investigated for variation tolerance on extremely mismatched cases for resistors and transistor width.

Figure 4.10(a) shows V_{in}-V_{out} curves of EO ternary inverter with transistor width of 1.0 μm at V_{dd} of 0.7 V in mismatched resistances of resistors. As increase of resistor resistance on PMOSFET side, voltage level of the third state also increased in same manner of changing potential distribution across the inverter. However, butterfly curves of the worst combination of resistor mismatching has low SNM, especially, the third state of 160kΩ-240kΩ and 240kΩ-160kΩ mismatching case is unreliable by due to intermixing with other state as shown in Figure 4.10(b).

Figure 4.11(a) shows V_{in}-V_{out} curves of EO ternary inverter with resistor resistance of 200kΩ and V_{dd} of 0.9 V for the mismatched transistor width ratio of 1:5, 1:1, and 5:1. Since the resistance of transistor depends on width of the transistor, the range of third level is shifted due to mismatched transistors width. Therefore, the range of third level is shifted to thinner width transistor which has large resistance on near threshold region. In the case, the SNM of 3 states also changed by transistor width mismatching for the same reason by transistor resistance dependence on transistor width, in particular, SNM of V_{dd} and 0 is deteriorated from 288 mV to 241 mV while SNM of the third state is improved from 168 mV to 276 mV, however, the symmetry of the V_{in}-V_{out} curve is degraded.

Transient response

Transient response of ternary EO inverter is investigated for operational characteristics in the time domain, which is related with the reliability of the device operation and dynamic power consumption. Figure 4.12(a) shows transient responses of ternary inverter with 200kΩ resistors and transistor width of 1.0 μm at V_{dd} of 0.9 V and the sinusoidal input voltage of 0.9V with frequency of 10 Mhz. The ternary states are obviously quantized with a sinusoidal input voltage, and the influence of propagation delay is not predominant at frequency of 10 Mhz operation. In the case, to evaluate the propagation delay, transient response for square voltage input of 0.9V at frequency of 100 Mhz shows propagation delay of 1.69 ns, which is not adequate to Ghz operation of logic circuits. Nevertheless, there is the possibility of Ghz operation to EO ternary inverter through EO MOSFET optimization such as capacitance suppression with redefinition of source and drain, and improving mobility to reduced transistor resistance.

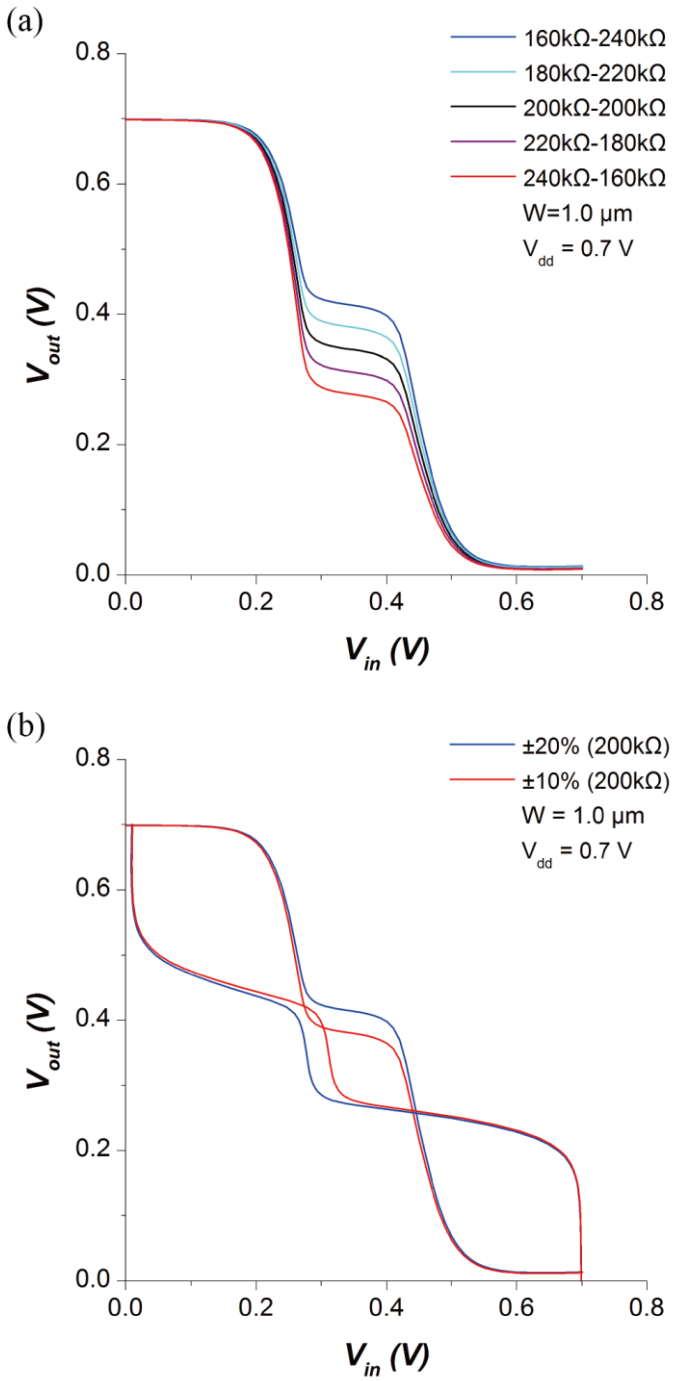

Figure 4.10 (a) V_{in}-V_{out} curves with mismatched resistor resistances, and (b) Butterfly curves of the worst mismatched resistor resistances with ±20 % (160kΩ-240kΩ and 240kΩ-160kΩ) and ±10 % (180kΩ-220kΩ and 220kΩ-180kΩ) are illustrated in the ternary EO inverter with transistor width of 1.0 μm and V_{dd} of 0.7 V.

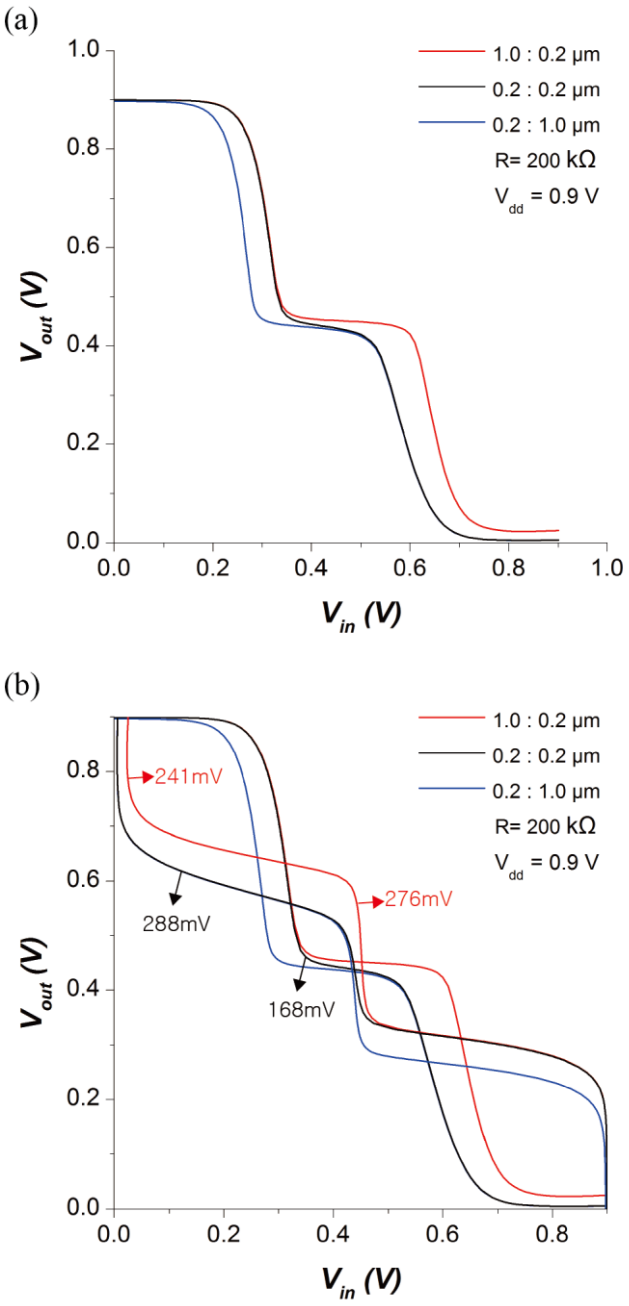

Figure 4.11 (a) V_{in}-V_{out} curves with mismatched transistor width, and (b) Butterfly curves of mismatched transistor width are illustrated in the ternary EO inverter with resistor resistance of 200kΩ and V_{dd} of 0.9 V.

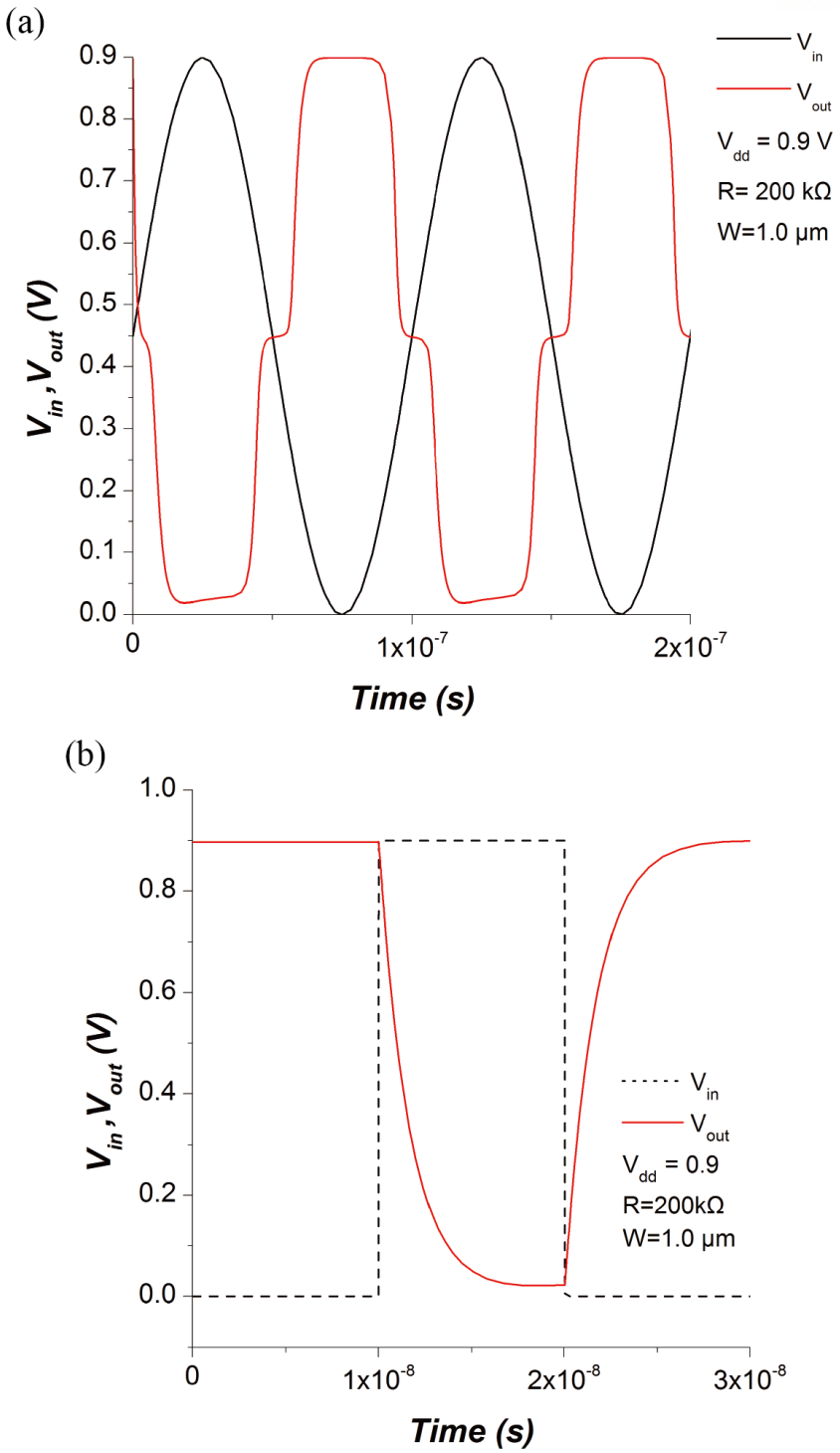

Figure 4.12 Transient responses of ternary inverter with 200kΩ resistors and transistor width of 1.0 μm at V_{dd} of 0.9 V are investigated on (a) the sinusoidal V_{in} and (b) the square V_{in}.

4.2.5 Conclusion

The EO ternary inverter structure is proposed, which structure constructed through insulating pillar with EO resistors and EO NMOSFET and EO PMOSFET, ternary characteristics of EO ternary inverter were demonstrated by TCAD mixed mode. The presence of insulating pillar, EO resistors and EO MOSFETs formed through sidewall of insulating pillar, hence the integrated circuit of EO ternary inverter can be possible to reduce lateral dimension extremely for achieve high information density on structural perspective. Moreover, since ternary logic reduce the complexity of system, there is another possibility to achieve high information density. Examine the ternary characteristics on the resistor resistance and the transistor width show dependence of transistor width and resistance of resistor to the ternary states and its noise tolerance. In addition, the ternary characteristics on changing V_{dd} also investigated, which show the necessity of threshold engineering to achieve adequate V_{dd}. Transient response shows the time domain ternary operation of the case, the EO ternary inverter is reliable at tens of Mhz frequency operation, and propagation delay is estimated of 1.69 ns. Hence, there is possibility of ternary EO inverter to Ghz operation by improving the carrier mobility and the structural optimization of EO MOSFET.

V. Dirac source effect on subthreshold swing

Since the first theoretical approach to graphene was investigated in 1947 [50], Dirac semi metal which is described by massless Dirac equation, predicted firstly in graphene in 1984 [85]. Unique linear energy dispersion relation near the Dirac point gives unique density of states proportional to energy. Despite these special characteristics being predicted, it took a lot of time to get to the physical manufacture of graphene due to challenging process to get graphene. In 2004, first experimental characteristics of graphene was reported [51], thenceforth 3-dimensional Dirac semimetal was reported in recent [52 - 55]. In this chapter, thermionic emission of Dirac semimetal source is demonstrated by doping types and Dirac point, and Dirac semimetal source on MOSFET is discussed in perspective of subthreshold swing.

5.1 Graphene

With the advent of the mechanical process of graphene, called the Scotch tape method, there have been many attempts to investigate graphene properties, but this has been limited because mass production of graphene by the scotch tape method is not possible [50]. Subsequently, chemical vapor deposition (CVD) graphene was developed to enable mass production of graphene, but the quality and uniformity of graphene were not guaranteed [56-58]. Nevertheless, there are several reports to supporting Dirac fermion on graphene [59 - 64].

5.1.1 Graphene Hamiltonian

Graphene is consisted by Carbon atom (C) in well-known honey-comb lattice structure as shown in Figure 5.1. In the graphene and graphite, carbon atom has sp^2 hybridization states make σ-bonds with adjacent 3 carbon atom as covalently and remained single p-orbital makes π-bond [65]. Distance between carbon atoms a_0 in graphene is 1.42 Å [66]. Figure 5.2(a) shows translational vector to adjacent C atoms $\vec{\delta}$,

$$\vec{\delta}_1 = a_0(-1,0),\ \vec{\delta}_2 = a_0\left(\frac{1}{2},\frac{\sqrt{3}}{2}\right),\ \vec{\delta}_3 = a_0\left(\frac{1}{2},-\frac{\sqrt{3}}{2}\right) \tag{5.1}$$

From the translational vectors, we can construct the primitive cell of graphene with basis vector $\vec{a}_1$ and $\vec{a}_2$ as shown in Figure 5.2(b).

$$\vec{a}_1 = \vec{\delta}_2 - \vec{\delta}_1 = a_0\left(\frac{3}{2}, \frac{\sqrt{3}}{2}\right), \quad \vec{a}_2 = \vec{\delta}_3 - \vec{\delta}_1 = a_0\left(\frac{3}{2}, -\frac{\sqrt{3}}{2}\right) \tag{5.2}$$

For a convenient quantum mechanical approach to graphene Hamiltonian, reciprocal lattice vectors are constructed by k-space approach (or Fourier transform from real space to momentum space)

$$\vec{a}_i \cdot \vec{b}_j = 2\pi\delta_{ij}, \tag{5.3}$$

Where, δ_{ij} is Kronecker delta and $\vec{b}_i$ is the reciprocal lattice vector of $\vec{a}_i$. Therefore, graphene reciprocal vectors $\vec{b}_1$ and $\vec{b}_2$ are

$$\vec{b}_1 = \frac{2\pi}{a_0}\left(\frac{1}{3}, \frac{\sqrt{3}}{3}\right), \quad \vec{b}_2 = \frac{2\pi}{a_0}\left(\frac{1}{3}, -\frac{\sqrt{3}}{3}\right) \tag{5.4}$$

From the reciprocal vectors $\vec{b}_1$ and $\vec{b}_2$, the first Brillouin zone of graphene in momentum space can be constructed as shown in Figure 5.3. In the primitive cell of graphene, there has two different atom sites as shown in Figure 5.2(b), hence, annihilation operator at first C site $\vec{R}$ is $\alpha_{\vec{R}}$ and annihilation operator to second C site $\vec{R}+\vec{\delta}$ is $\beta_{\vec{R}+\vec{\delta}}$, likewise, creation operator $\alpha_{\vec{R}}^{\dagger}$ and $\beta_{\vec{R}+\vec{\delta}}^{\dagger}$ are determined. In according to tight binding model, Hamiltonian is considered with nearest neighbors in real space, which can be described by [50]

$$H = -t\sum_{\vec{R}}\sum_{\vec{\delta}}(\alpha_{\vec{R}}^{\dagger}\beta_{\vec{R}+\vec{\delta}} + \beta_{\vec{R}+\vec{\delta}}^{\dagger}\alpha_{\vec{R}}) \tag{5.5}$$

Where, t is graphene hopping energy determined by π-bond Hamiltonian, which is ~2.7 eV [67]. In the k-space, annihilation and creation operators are transformed as

$$\alpha_{\vec{R}} = \frac{1}{\sqrt{N}}\sum_{\vec{k}}\alpha_{\vec{k}}e^{i\vec{k}\cdot\vec{R}}, \beta_{\vec{R}+\vec{\delta}} = \frac{1}{\sqrt{N}}\sum_{\vec{k}}\beta_{\vec{k}}e^{i\vec{k}\cdot(\vec{R}+\vec{\delta})} \tag{5.6}$$

Where, N is the number of primitive cells in graphene. In this regard, Hamiltonian of graphene at k-space is

$$\begin{aligned} H &= -\frac{t}{N}\sum_{\vec{R}}\sum_{\vec{\delta}}\sum_{\vec{k}}\sum_{\vec{k}'}(\alpha_{\vec{k}}^{\dagger}\beta_{\vec{k}'}e^{i\vec{R}\cdot(\vec{k}'-\vec{k})}e^{i\vec{k}'\cdot\vec{\delta}} + \beta_{\vec{k}'}^{\dagger}\alpha_{\vec{k}}e^{i\vec{R}\cdot(\vec{k}-\vec{k}')}e^{-i\vec{k}'\cdot\vec{\delta}}) \\ &= = -t\sum_{\vec{\delta}}\sum_{\vec{k}}(\alpha_{\vec{k}}^{\dagger}\beta_{\vec{k}}e^{i\vec{k}\cdot\vec{\delta}} + \beta_{\vec{k}}^{\dagger}\alpha_{\vec{k}}e^{-i\vec{k}\cdot\vec{\delta}}) = \sum_{\vec{k}}\Psi H(\vec{k})\Psi^{\dagger} \end{aligned} \tag{5.7}$$

$$\frac{1}{N}\sum_{\vec{R}} e^{i\vec{R}\cdot(\vec{k}-\vec{k}')} = \delta_{\vec{k},\vec{k}'} \tag{5.8}$$

Where,

$$\Psi = \begin{pmatrix} \alpha_{\vec{k}} \\ \beta_{\vec{k}} \end{pmatrix}, \quad \Psi^{\dagger} = \begin{pmatrix} \alpha_{\vec{k}}^{\dagger} & \beta_{\vec{k}}^{\dagger} \end{pmatrix} \tag{5.9}$$

$$H(\vec{k}) = \begin{pmatrix} 0 & -t\sum_{\vec{k}} e^{i\vec{k}\cdot\vec{\delta}} \\ -t\sum_{\vec{k}} e^{-i\vec{k}\cdot\vec{\delta}} & 0 \end{pmatrix}, \tag{5.10}$$

Hamiltonian matrix in k-space (or Bloch Hamiltonian) gives the eigenvalues, which is the energy of graphene:

$$\begin{aligned} E(\vec{k}) &= \pm t\sqrt{\sum_{\vec{k}} e^{i\vec{k}\cdot\vec{\delta}} \sum_{\vec{k}} e^{-i\vec{k}\cdot\vec{\delta}}} \\ &= \pm t\sqrt{e^{-ik_x a_0}\left(1+2e^{-i\frac{3k_x a_0}{2}}\cos\left(\frac{\sqrt{3}k_y a_0}{2}\right)\right)e^{ik_x a_0}\left(1+2e^{i\frac{3k_x a_0}{2}}\cos\left(\frac{\sqrt{3}k_y a_0}{2}\right)\right)} \\ &= \pm t\sqrt{1+4\cos\left(\frac{\sqrt{3}k_x a_0}{2}\right)\cos\left(\frac{\sqrt{3}k_y a_0}{2}\right)+4\cos^2\left(\frac{\sqrt{3}k_y a_0}{2}\right)} \end{aligned} \tag{5.11}$$

Figure 5.4 shows the graphical expression of (5.11), which has zero bandgap at Dirac point. Near the Dirac point $\vec{D}$, which location is corners of the first Brillouin zone, Bloch Hamiltonian is approximated with relative vector to the Dirac point $\vec{q} = \vec{k} - \vec{D}$ [68],

$$\sum_{\vec{k}} e^{i(\vec{D}+\vec{q})\cdot\vec{\delta}} = e^{-ia_0 D_x} e^{-ia_0 q_x}\left[1-2e^{i\frac{3a_0}{2}q_x}\cos\left(\frac{\pi}{3}+\frac{3a_0}{2}q_y\right)\right] \approx \left(-\frac{3}{2}\right)a_0 e^{\frac{2\pi i}{3}}(iq_x+q_y) \tag{5.12}$$

$$\begin{aligned} E(\vec{D}+\vec{q}) &= \pm t\sqrt{\left(-\frac{3}{2}\right)a_0 e^{\frac{2\pi i}{3}}(iq_x+q_y)\left(-\frac{3}{2}\right)e^{-\frac{2\pi i}{3}}(-iq_x+q_y)} \\ &= \pm\frac{3ta_0}{2}\sqrt{{q_x}^2+{q_y}^2} = \frac{3ta_0}{2}|\vec{q}| = \pm\hbar v_F|\vec{q}| \end{aligned} \tag{5.13}$$

$$v_F = \frac{3ta_0}{2\hbar} \tag{5.14}$$

Where, $\hbar$ is the Plank constant and v_F is the fermi velocity in graphene, which is extraordinarily high velocity $v_F \sim c/300$ (c is the velocity of light). Hence, graphene follows the linear energy dispersion relation with fermi velocity and massless mechanics near the Dirac point. In this regard, electrons near the Dirac point are called Dirac fermion and are described by massless Dirac equation with the Pauli vector $\vec{\sigma}$ [50][68],

$$H(\vec{D}+\vec{q}) = \pm\hbar v_F \begin{pmatrix} 0 & q_x - iq_y \\ q_x + iq_y & 0 \end{pmatrix} = \pm\hbar v_F \vec{\sigma}\cdot\vec{q}\,, \tag{5.15}$$

5.1.2 Graphene density of states near the Dirac point

Graphene density of states is described by 2-dimensional geometry and linear energy dispersion near the Dirac point. Thus, feature of graphene density of states is unique compare to 3D bulk materials and 2D materials, which are described by parabolic energy dispersion relation. The number of electron states $D(q)$ can be counted in k-space as

$$D(q)dq = \frac{1}{A} g_{valley} g_{spin} \frac{2\pi q dq}{(2\pi/L)(2\pi/W)}\,, \tag{5.16}$$

Where, A is area of graphene sheet, which determined by length L and width W, and g_{valley} is the degeneracy of valley, and g_{spin} is the electron spin degeneracy. In the graphene, degeneracy of valley and electron is 2, $g_{valley} = 2$, $g_{spin} = 2$. Density of states in k-space is converted to energy space by linear energy dispersion relation.

$$D(E)dE = \frac{2|E|dE}{\pi(\hbar v_F)^2}\,, \tag{5.17}$$

Hence, graphene density of states near the Dirac point is determined by linear relationship with energy, as illustrated in Figure 5.5. In the density of states, fermi level of n-type graphene (n-graphene) is located above the Dirac point, meanwhile fermi level of p-type graphene (p-graphene) is located below the Dirac point.

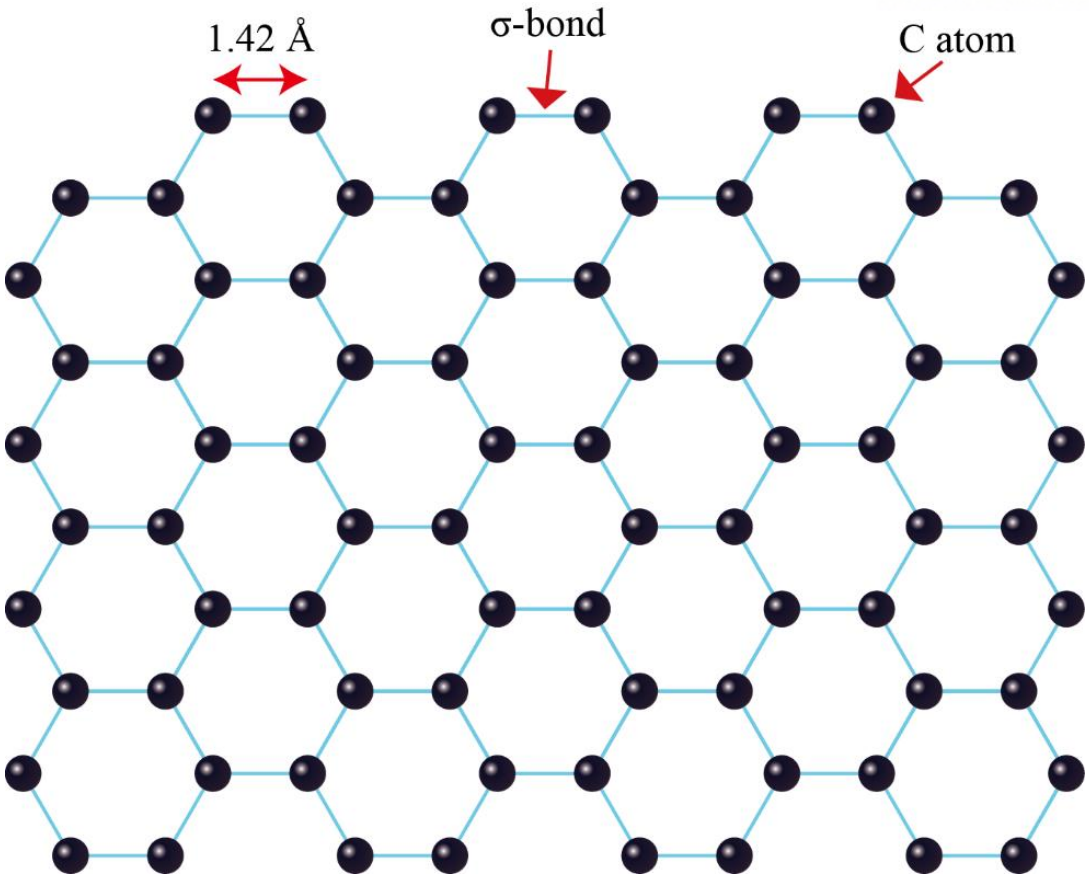

Figure 5.1 Honeycomb lattice structure of monolayer graphene, C-C bonding distance (σ-bond) is 1.42 Å.

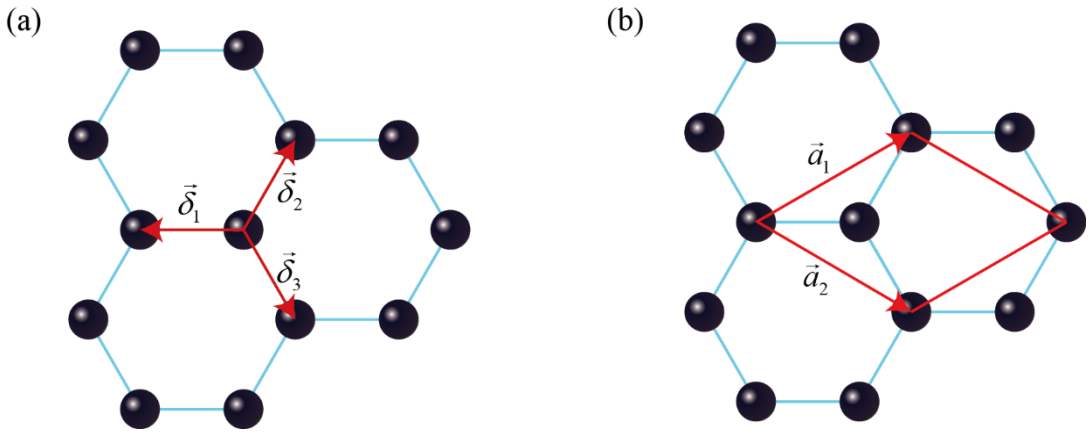

Figure 5.2 (a) Translational vectors to adjacent neighbor C atoms in graphene. (b) Primitive unit cell of graphene, which is marked by red rhombus.

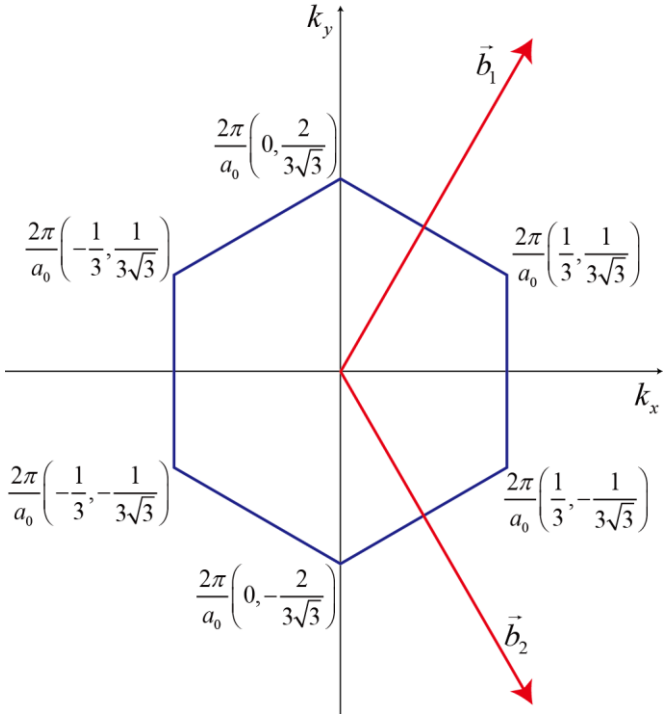

Figure 5.3 the first Brillouin zone of graphene in k-space with reciprocal vectors and hexagonal corners of the first Brillouin zone.

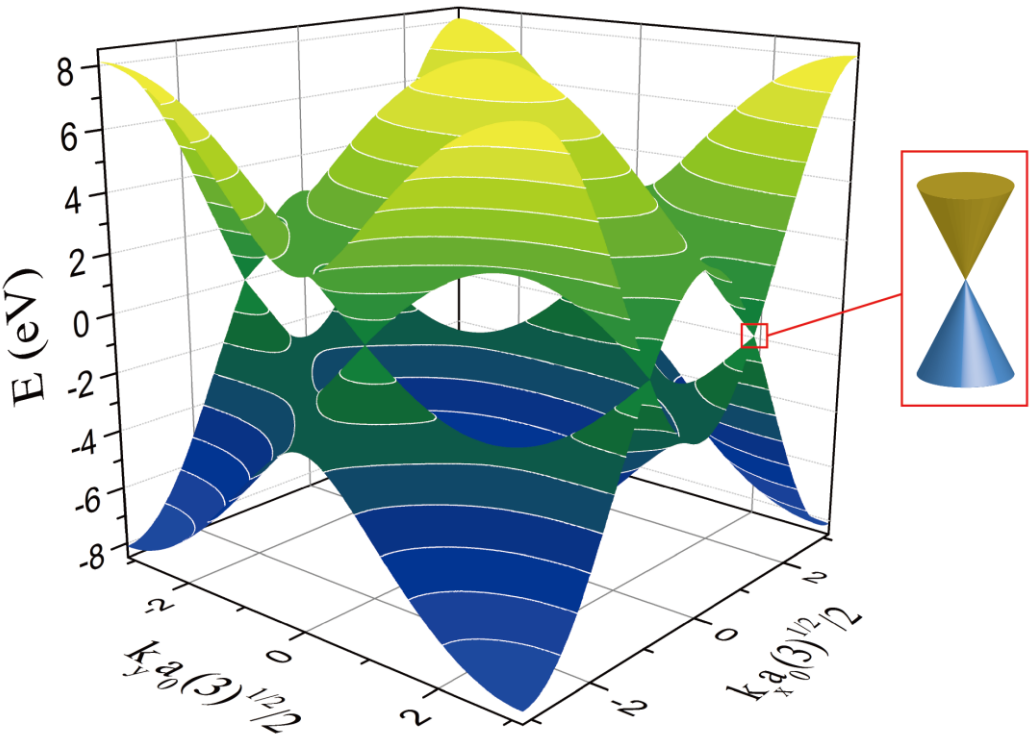

Figure 5.4. Graphene energy given in k-space, red inner box is energy near the Dirac point.

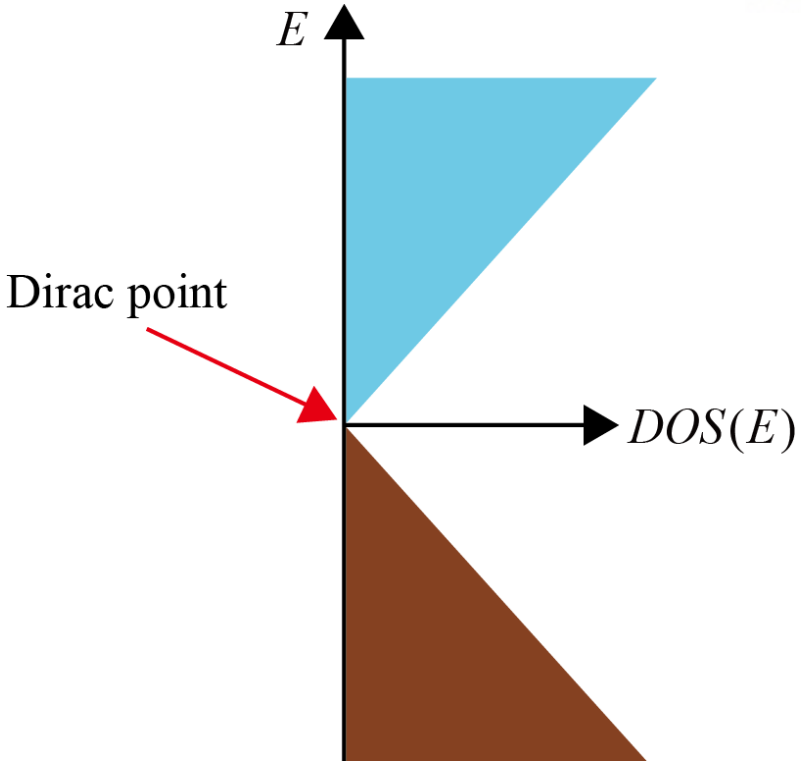

Figure 5.5 Density of states in graphene near the Dirac point, which has linearly dependent on energy.

5.2 Thermionic emission at Graphene/Si interface

In general, thermionic emission on metal/semiconductor (MS) contact was described by Richardson's law, while neglecting some details such as quantum mechanical reflections and inter-valley scattering, nevertheless, Richardson's laws explains MS contact fairly well [69][70].

$$J_{Ri} = A_{Ri}^{*} T^2 e^{-q(\phi_b - E_F)/k_B T}\left(1 - e^{-qV/k_B T}\right) \tag{5.18}$$

$$A_{Ri}^{*} = \frac{qm^{*}k_B^{2}}{2\pi^2\hbar^3} \tag{5.19}$$

Where, A^{*} is the effective Richardson constant, m^{*} is the electron effective mass, and ϕ_b is Schottky barrier height on MS contact, which is determined by difference between metal work function Φ_m and electron affinity of Si χ_{Si}, $\phi_b = \Phi_m - \chi_{Si}$, and direction of voltage is same with Figure 5.6. In according to graphene linear energy dispersion near the Dirac point, electron effective mass is vanished, which is determined by perspective of solid-state physics [71],

$$m_{ij}^{*} = \hbar^2\left(\frac{\partial^2 E}{\partial k_i \partial k_j}\right)^{-1} \tag{5.20}$$

In order to describing thermionic emission of Dirac fermion system with zero electron effective mass, there is newly thermionic emission model excluding effective mass of electron by neglecting the substrate effect [72],

$$J_{Shi} = A_{Shi}^{*} T^3 e^{-q(\phi_b - E_F)/k_B T}\left(1 - e^{-qV/k_B T}\right) \tag{5.21}$$

$$A_{Shi}^{*} = \frac{qk_B^{3}}{\pi\hbar^3 v_F^{2}} \tag{5.22}$$

Obviously, this model describe the linear energy dispersion characteristics of graphene with massless Dirac fermion, moreover, neglecting density of states of Si can be justified by number of carriers in graphene, which is extremely lower than substrate due to difference between 2-dimension of graphene and 3-dimension of Si. However, this model only considers fermi level of graphene located at the Dirac point, in other words, it represents only the intrinsic graphene.

5.2.1 Thermionic emission at Graphene/Si interface across the graphene layer

Figure 5.6 shows graphene/Si diode with voltage V, with electrons injected into Si across the graphene layer (source). In the same approach as in (5.21), there are two different energy components that are vertical electron energy to the graphene layer E_x and parallel electron energy along the graphene layer E_p [72]. Unlike the linear energy dispersion along the graphene layer, electron across the graphene layer in perpendicular direction is considered with conventional parabolic energy dispersion [72]. In this manner, the number of electrons across the graphene layer to Si between infinitesimal energy differences $E_x \sim E_x + dE_x$ and $E \sim E + dE$ is [72]

$$\begin{aligned} N(E,E_x)dE_x dE &= \frac{2|E_p|dE_p}{\pi(\hbar v_F)^2} f_{FD}(E)\frac{v_x dk_x}{2} \\ &= \frac{|E_p|}{\pi\hbar^3 {v_F}^2}\frac{dE_p dE_x}{e^{(E-E_F)/k_BT}+1} \end{aligned} \tag{5.23}$$

However, the Dirac point is not consider in (5.23). Figure 5.7 shows the energy band diagram of n-graphene/Si interface and density of states of graphene (DOS). Where, vacuum energy level and Si conduction band energy are E_0 and E_c, respectively. Schottky barrier height $q\phi_b$ is determined by difference between graphene fermi level and electron affinity of Si, $q\phi_b = E_F - q\chi_{Si}$, and energy difference between the Dirac point $q\Phi_{gr}$ and fermi level of graphene E_F is $E_D = E_F - q\Phi_{gr}$. Hence, E_D is negative in n-type graphene, on the other hand, E_D is positive in p-type graphene. Therefore, (5.23) can be represented with the Dirac point:

$$N(E,E_x)dE_x = \frac{dE_x}{\pi\hbar^3 {v_F}^2}\int_{E_x}^{\infty} dE\,\frac{|E-E_x-E_D|}{e^{(E-E_F)/k_BT}+1} \tag{5.24}$$

Thermionic emission current density across the graphene layer is determined by the vertical electron energy E_x above Schottky barrier height $q\phi_b$, for simplicity, quantum reflection and inter-valley scattering is neglected, hence transmission probability is assumed as 1:

$$J_{\perp} = \frac{q}{\pi\hbar^3 {v_F}^2}\int_{q\phi_b}^{\infty} dE_x \int_{E_x}^{\infty} dE\,\frac{|E-E_x-E_D|}{e^{(E-E_F)/k_BT}+1}\left(1-\frac{1}{e^{(E-E_{F,S})/k_BT}+1}\right) \tag{5.25}$$

Where, $E_{F,\mathrm{S}}$ is the fermi level of Si, which is related with voltage bias, when the graphene fermi level is reference point, $E_{F,\mathrm{S}} = E_F - V$, and subscript $\perp$ means the carriers are injected directly.

Figure 5.8 shows three different energy band conditions for thermionic emission at graphene/Si interface, when the carrier is dominantly transported in the conduction band, these conditions are distinguished by n-graphene/Si and p-graphene/Si. Thermionic emission from n-graphene to Si is approximated at $q\phi_b > 3k_BT$, hence the Fermi-Dirac statistics become Maxwell-Boltzmann statistics, which is the case of Figure 5.8.i:

$$\begin{aligned} J_{\perp,n-Gr\to Si} &= \frac{q}{\pi\hbar^3 {v_F}^2}\int_{q\phi_b}^{\infty} dE_x \int_{E_x}^{\infty} dE \frac{E-E_x-E_D}{e^{(E-E_F)/k_BT}} \\ &= \frac{qk_BT}{\pi\hbar^3 {v_F}^2}(k_BT-E_D)\int_{q\phi_b}^{\infty} dE_x e^{-(E_x-E_F)/k_BT} \\ &= \frac{q(k_BT)^2}{\pi\hbar^3 {v_F}^2}(k_BT-E_D)e^{-(q\phi_b-E_F)/k_BT} \end{aligned} \tag{5.26}$$

Total thermionic current across n-graphene/Si interface is

$$J_{\perp,n-Gr/Si} = \frac{q(k_BT)^2}{\pi\hbar^3 {v_F}^2}(k_BT-E_D)e^{-(q\phi_b-E_F)/k_BT}(1-e^{-qV/k_BT}) \tag{5.27}$$

When the fermi level and Dirac point are same, $E_D = 0$, (5.27) is identical with (5.21). In according to derived representation, condition of $E_D = k_BT$ gives the zero thermionic emission current. However, since $k_BT > E_D$ is always true in n-graphene case, thermionic emission current always exists in n-type graphene case.

Similarly, thermionic current density across the p-graphene layer to Si is (the case of Figure 5.8.ii and Figure 5.8.iii)

$$\begin{aligned} J_{\perp,p-Gr\to Si} &= \frac{q}{\pi\hbar^3 {v_F}^2}\int_{q\phi_b}^{\infty} dE_x \left(\int_{E_x}^{E_x+E_D} dE \frac{E_x+E_D-E}{e^{(E-E_F)/k_BT}} + \int_{E_x+E_D}^{\infty} dE \frac{E-E_x-E_D}{e^{(E-E_F)/k_BT}} \right) \\ &= \frac{q}{\pi\hbar^3 {v_F}^2}\int_{q\phi_b}^{\infty} dE_x \left[(k_bT)^2 \left(e^{-E_D/k_BT} - 1 + \frac{E_D}{k_BT} \right) e^{-(E_x-E_F)/k_BT} \right. \\ &\qquad \left. + (k_BT)^2 e^{-(E_x+E_D-E_F)/k_BT} \right] \\ &= \frac{q(k_BT)^2}{\pi\hbar^3 {v_F}^2}\left(2e^{-E_D/k_BT} - 1 + \frac{E_D}{k_BT} \right)\int_{q\phi_b}^{\infty} dE_x e^{-(E_x-E_F)/k_BT} \\ &= \frac{q(k_BT)^3}{\pi\hbar^3 {v_F}^2}\left(2e^{-E_D/k_BT} - 1 + \frac{E_D}{k_BT} \right) e^{-(q\phi_b-E_F)/k_BT} \end{aligned} \tag{5.28}$$

Therefore, total thermionic current density across p-graphene/Si interface is

$$J_{\perp,p-Gr/Si} = \frac{q(k_BT)^3}{\pi\hbar^3 {v_F}^2}\left(2e^{-E_D/k_BT} - 1 + \frac{E_D}{k_BT}\right)e^{-(q\phi_b - E_F)/k_BT}(1 - e^{-qV/k_BT}) \tag{5.29}$$

Once more, (5.29) is identical with (5.21), when the fermi level and Dirac point are same, $E_D = 0$. As a results, representations of thermionic emission current are differed by the difference between Dirac point and fermi level of graphene, in particular, the representations for thermionic emission of n-type graphene and p-type graphene are different.

In the MOSFET, the Schottky barrier height changes with the surface potential of the Si, in other words, gate voltage changes the Schottky barrier height at a constant source drain voltage. In this sense, subthreshold swing is revisited

$$S.S = \left.\frac{dV_G}{d(\log_{10} J)}\right|_V = \ln(10)\frac{\partial V_G}{\partial \phi_b}\left.\frac{\partial \phi_b}{\partial \ln J}\right|_V = -\frac{\ln(10)}{\eta}\left.\frac{\partial \phi_b}{\partial \ln J}\right|_V \tag{5.30}$$

$$\frac{1}{\eta} = -\frac{dV_G}{d\phi_b} \geq 1 \tag{5.31}$$

Where η is Schottky barrier height change by gate voltage, the best case of Schottky barrier height change is 1. In this regard, subthreshold swings of the n-graphene/Si and p-graphene/Si are

$$S.S_{\perp,p-Gr/Si} = S.S_{\perp,n-Gr/Si} = \frac{1}{\eta}\frac{k_BT}{q}\ln(10) \tag{5.32}$$

Hence, subthreshold swing of thermionic emission across the graphene monolayer are limited at $\frac{k_BT}{q}\ln(10)$, which is thermodynamic limit of subthreshold swing for 3 dimensional bulk material source with parabolic energy dispersion.

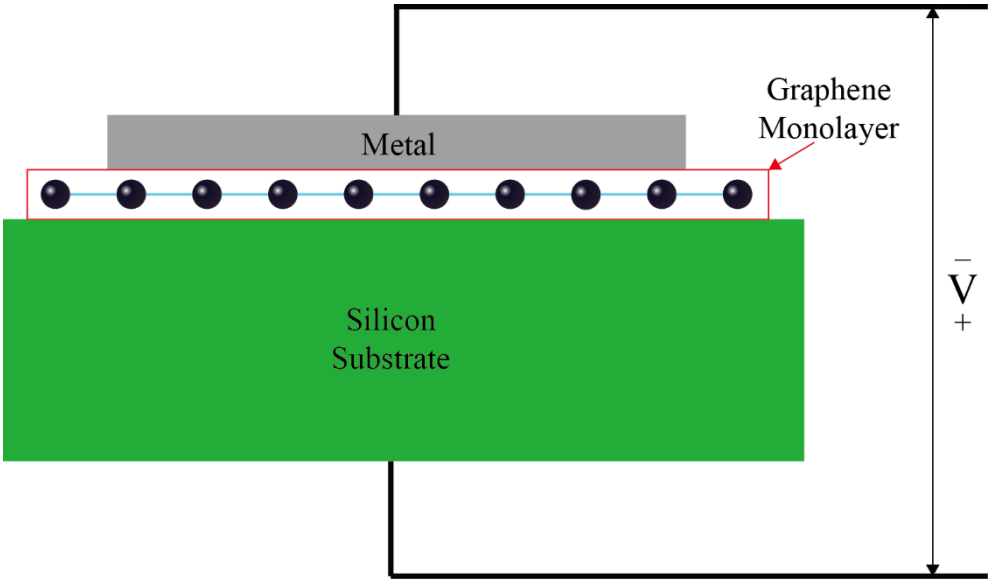

Figure 5.6 Cross-sectional view of graphene/Si contact diode, electrons are injected into silicon across the graphene layer.

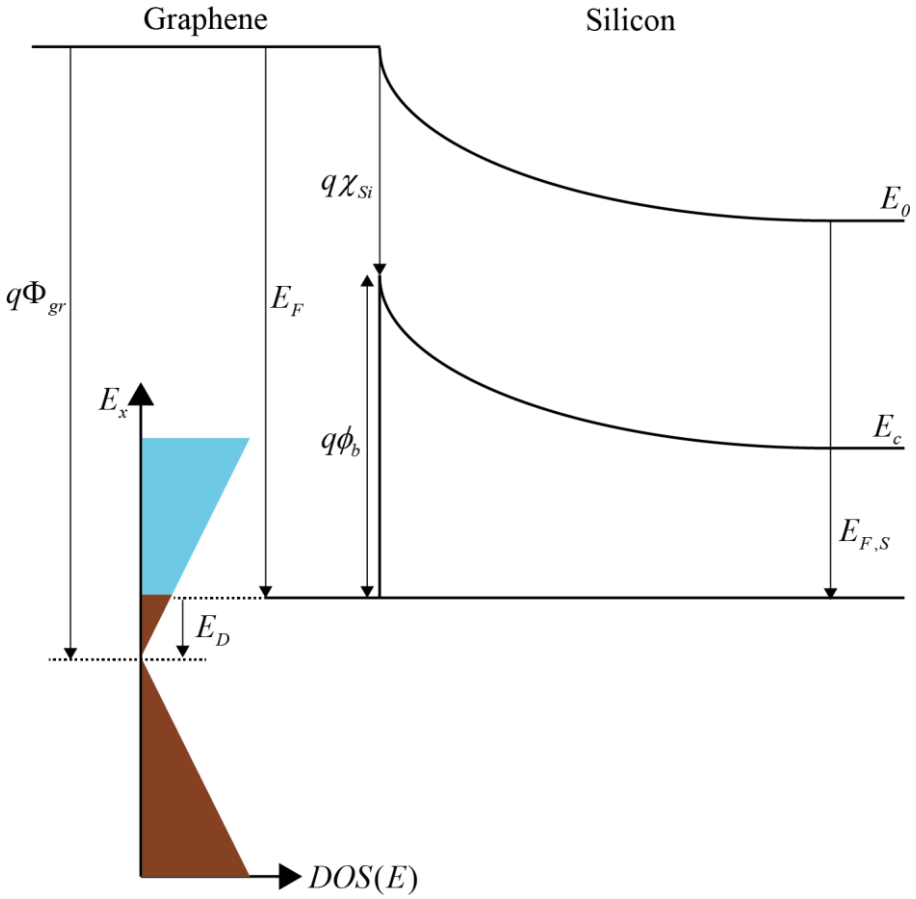

Figure 5.7 Energy band diagram of n-graphene/Si interface, n-type graphene density of state is aligned with fermi level.

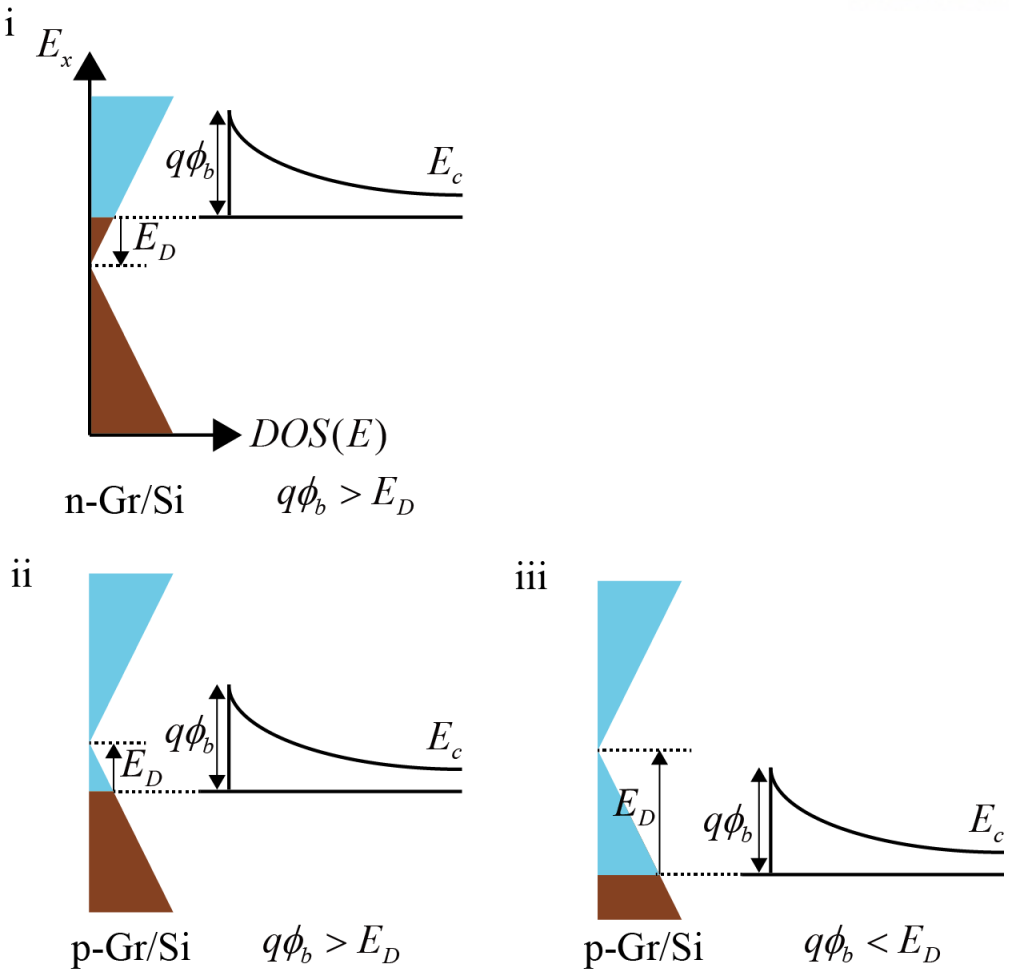

Figure 5.8 Different energy band conditions of Graphene/Si interface by the carrier type of graphene and energy aligning of graphene fermi level, Dirac point, and Schottky barrier height.

5.2.2 Thermionic emission at Graphene/Si interface without direct injection of carrier

In recent, Dirac source CNT FET breaks the thermodynamic limit of subthreshold swing. In the case, graphene source doesn't transfer the perpendicular energy from source to CNT channel due to the unique structure, in other words, there are no direct injection from graphene to Si [32]. Similarly, Graphene/Si diode can be constructed as illustrated in Figure 5.9.

Analytic approach

Since the additional insulator layer forbids the direct electron injection by perpendicular energy across the graphene layer and the number of carrier in graphene is much smaller than Si, current density can be described by Landauer–Büttiker formula [32][73 - 75]:

$$J = \frac{q}{\tau}\int_{-\infty}^{\infty} dE T(E) D(E)\left(\frac{1}{e^{(E-E_F)/k_BT}+1} - \frac{1}{e^{(E-E_{F,S})/k_BT}+1}\right) \tag{5.33}$$

Where, τ is the time scale of carrier injection from the voltage supplier, therefore $1/\tau$ is the carrier injection rate from the voltage supplier [75]. Thermionic current density using the Landauer–Büttiker formalism at n-graphene/Si interface gives

$$\begin{aligned} J_{\|,n-Gr/Si} &= \frac{2q}{\pi(\hbar v_F)^2\tau}\int_{q\phi_b}^{\infty} dE\left|E-E_D\right|\left(\frac{1}{e^{(E-E_F)/k_BT}+1} - \frac{1}{e^{(E-E_{F,S})/k_BT}+1}\right) \\ &\approx \frac{2q}{\pi(\hbar v_F)^2\tau}\int_{q\phi_b}^{\infty} dE\left|E-E_D\right|\left(e^{(E-E_F)/k_BT} - e^{(E-E_{F,S})/k_BT}\right) \\ &= \frac{2q}{\pi(\hbar v_F)^2\tau}\int_{q\phi_b}^{\infty} (E-E_D)\left(e^{(E-E_F)/k_BT} - e^{(E-E_{F,S})/k_BT}\right) dE \\ &= \frac{2qk_BT}{\pi(\hbar v_F)^2\tau}(q\phi_b - E_D + k_BT)e^{-(q\phi_b-E_F)/k_BT}(1-e^{-qV/k_BT}) \end{aligned} \tag{5.34}$$

Where, subscript $\|$ means the carriers in graphene are injected by depletion field of Si without direct injection.

Similarly, thermionic current density at p-graphene/Si interface is derived.

$$
\begin{aligned}
J_{\|,p-Gr/Si} &= \frac{2q}{\pi(\hbar v_F)^2\tau}\int_{q\phi_b}^{\infty} dE\,|E-E_D|\left(e^{(E-E_F)/k_BT}-e^{(E-E_{F,S})/k_BT}\right) \\
&= \frac{2q}{\pi(\hbar v_F)^2\tau}\left[\int_{q\phi_b}^{E_D}(E_D-E)\left(e^{(E-E_F)/k_BT}-e^{(E-E_{F,S})/k_BT}\right)dE\right. \\
&\qquad \left. +\int_{E_D}^{\infty}(E-E_D)\left(e^{(E-E_F)/k_BT}-e^{(E-E_{F,S})/k_BT}\right)dE\right] \qquad (5.35) \\
&= \frac{2qk_BT}{\pi(\hbar v_F)^2\tau}[2k_BTe^{-(E_D-E_F)/k_BT} \\
&\qquad +(E_D-q\phi_b-k_BT)e^{-(q\phi_b-E_F)/k_BT}](1-e^{-qV/k_BT})
\end{aligned}
$$

Obviously, the thermionic current density of p-graphene/Si interface has term which depends on Schottky barrier height linearly. Subthreshold swings of n-graphene/Si and p-graphene/Si are

$$S.S_{\|,n-Gr/Si} = \frac{1}{\eta}\ln(10)\frac{k_BT}{q}\left(1+\frac{k_BT}{q\phi_b-E_D}\right) \qquad (5.36)$$

$$S.S_{\|,p-Gr/Si} = \frac{1}{\eta}\ln(10)\frac{k_BT}{q}\left(1-\frac{k_BT}{E_D-q\phi_b}\right) \qquad (5.37)$$

In case of n-graphene/Si, $q\phi_b - E_D$ is always positive value, hence, subthreshold swing follows the thermodynamic limit. On the other hand, in case of p-graphene/Si, $E_D - q\phi_b$ term can be positive or negative either as illustrated in Figure 5.8.ii and Figure 5.8.iii. In particular, the subthreshold swing of p-graphene/Si under condition of $E_D > q\phi_b$ (Figure 5.8.iii) can break the thermodynamic limit like Dirac source CNT FET [32]. Figure 5.10 shows the subthreshold swing of the p-graphene source MOSFET by varying the difference between Dirac point and graphene fermi level E_D, and varying the Schottky barrier height $q\phi_b$, at perfect Schottky barrier change on gate voltage $\eta = 1$. In the Figure 5.10, subthreshold swing diverges at the $E_D = q\phi_b$, and subthreshold swing is suppressed below the thermodynamic limit as approach to $E_D = q\phi_b$ when $E_D > q\phi_b$. Therefore, the conditions for E_D and $q\phi_b$, which overcome the thermodynamic limit of subthreshold swing, always exist regardless of Schottky barrier height change on gate voltage η when the subthreshold current is dominated by thermionic emission. In addition, abnormal negative subthreshold swing also appeared near the $E_D = q\phi_b$, the negative subthreshold swing means that thermionic emission current is suppressed when the transistor is turned on. Also, subthreshold current become constant near the singularities of subthreshold swing, therefore there is a possibility that the tunneling current prevails under subthreshold conditions, but this task is not covered in this research. Figure 5.11 shows schematic of thermionic

emission in energy band diagram for conventional source substrate interface, n-graphene/Si interface, and p-graphene/Si interface. Density of states for conventional source and n-graphene is increases as higher energy. Meanwhile, the density of states for p-graphene decreases until the electron energy reaches the Dirac point, especially, when the Schottky barrier height is located near the Dirac point, thermionic emission is suppressed effectively due to the shape of density of states and Fermi-Dirac statistics.

Simple numerical approach

In order to investigate the numerical explanation of the case, surface potential of MOS structure with Schottky contact is given by solving Poisson's equation which is performed by FlexPDE package, and thermionic current density is calculated by MATLAB. Image force lowering to Schottky barrier height is included in depletion and inversion conditions, which describes the change of Schottky barrier height as maximum channel electric field near the metal/Si interface [5].

$$\Delta q\phi_b = \sqrt{\frac{q\xi_{\max}}{4\pi\varepsilon_{Si}}} \tag{5.38}$$

Where, $\xi_{\max}$ is the maximum electric field at Si surface. As a result, modified Schottky barrier height is

$$q\phi_b^* = q\phi_b - \Delta q\phi_b \tag{5.39}$$

In addition, tunneling current between graphene and Si is numerically calculated with Wentzel–Kramers–Brillouin (WKB) approximation.

$$\begin{aligned} J_{||,tunneling} = {} & \frac{2q}{\pi(\hbar v_F)^2\tau}\int_{q(\phi_b-\psi_{bi}-V)}^{E_D} dE\left|E-E_D\right|T(E) \\ & \times\left(\frac{1}{e^{(E-E_F)/k_BT}+1}-\frac{1}{e^{(E-E_{F,S})/k_BT}+1}\right) \end{aligned} \tag{5.40}$$

$$T(E) = \exp\left(\frac{2\sqrt{2m^*}}{\hbar}\int_{x1(E)}^{x2(E)} dx\sqrt{q\psi(x)-E}\right) \tag{5.41}$$

Where, $T(E)$ is tunneling probability of WKB approximation, $x1(E)$ and $x2(E)$ are the real space location of the energy band by electron energy, $q\psi(x)$ is energy band at position x. Simplified Schottky barrier shape is adjusted by image force lowering as shown in Figure 5.12, hence the tunneling current is underestimated by simplified shape of Schottky barrier. Nevertheless, since thermionic

emission depends on maximum Schottky barrier height regardless of shape of barrier, the characteristics of thermionic emission are properly evaluated with simplified image force lowering. Work functions of gate metal and electron affinity of Si are set to same value of 4.05 eV. MOSFET is assumed fully depleted channel as like SOI MOSFET, and undoped intrinsic Si channel and gate insulator of SiO_2 is used. Figure 5.13 shows numerically calculated transfer characteristics at drain bias of 0.5 V consisting of thermionic current density and tunneling current density at intrinsic Schottky barrier height 0.3 eV with varying the difference between Dirac point and graphene fermi level E_D 0~0.6 eV. In the subthreshold condition, thermionic emission predominate transport, meanwhile, tunneling current dominate the transport after threshold. In condition of $E_D > q\phi_b$, minimum subthreshold swings are evaluated as 40 and 48 mV/dec for E_D=0.4 eV and E_D=0.6 eV, respectively, which corresponds to the analytic result as discussed previously.

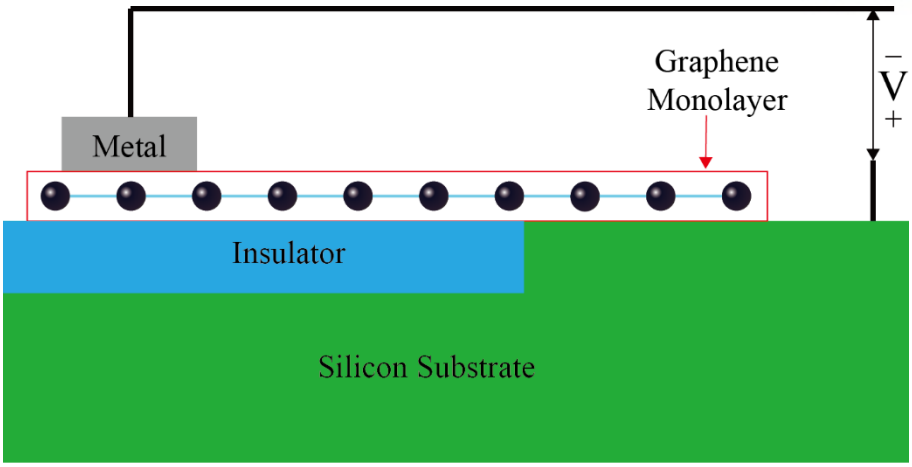

Figure 5.9 Cross-sectional view of graphene/Si contact diode to prohibit the direct injection from graphene to Si.

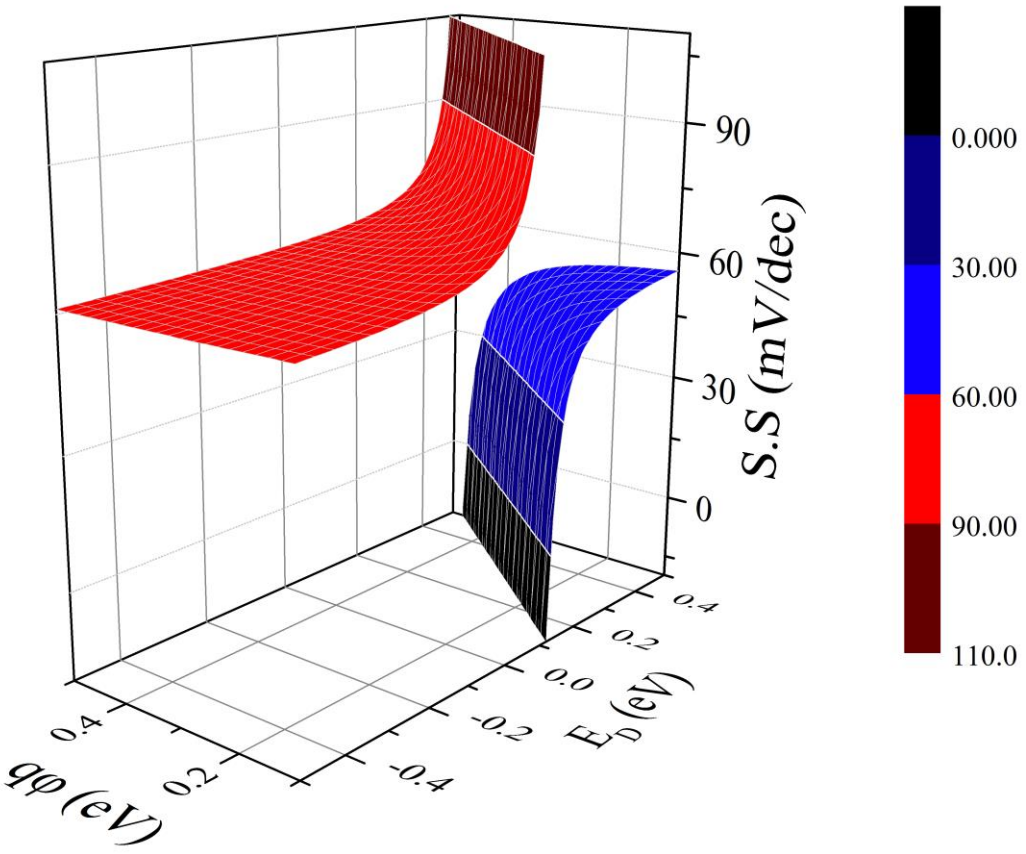

Figure 5.10 Subthreshold swing of the p-graphene source MOSFET at perfect Schottky barrier change on gate voltage $\eta = 1$ as varying Schottky barrier height and the difference between Dirac point and graphene fermi level.

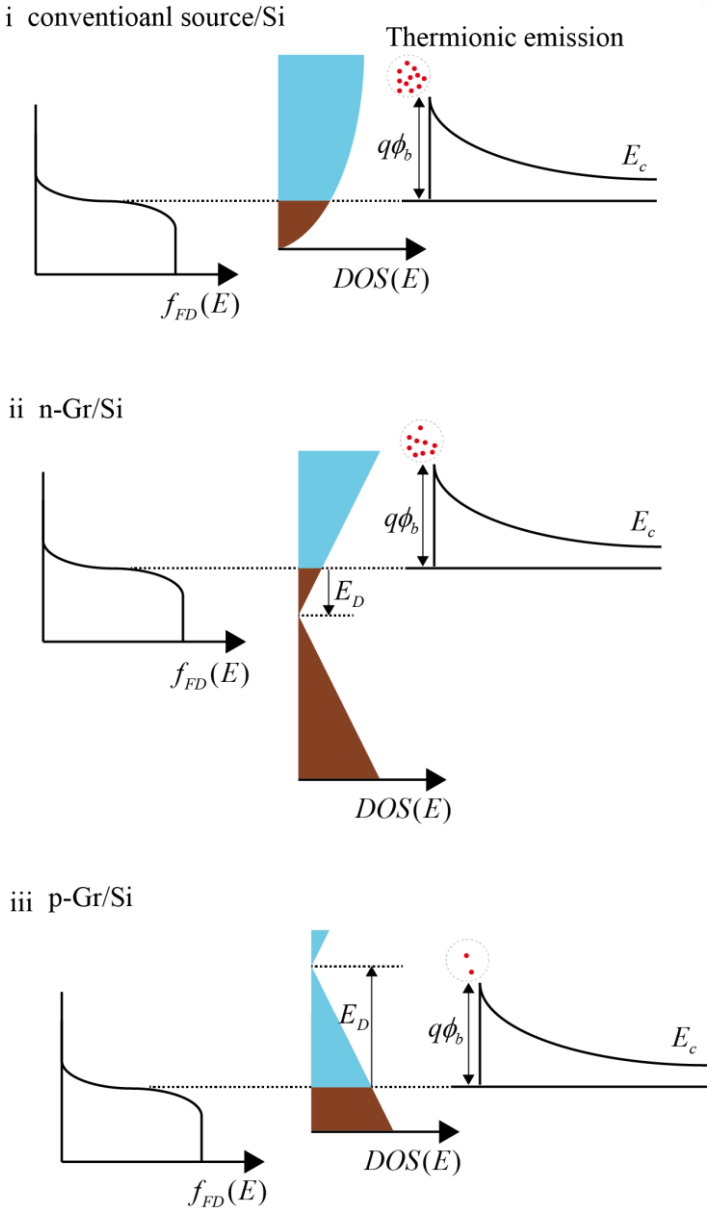

Figure 5.11 Energy band diagram with Fermi-Dirac statistics and density of states for conventional source, n-graphene, and p-graphene, the number of carriers for thermionic emission (red dot, inside of gray dot circle) depend on Schottky barrier height and difference between Dirac point and fermi level.

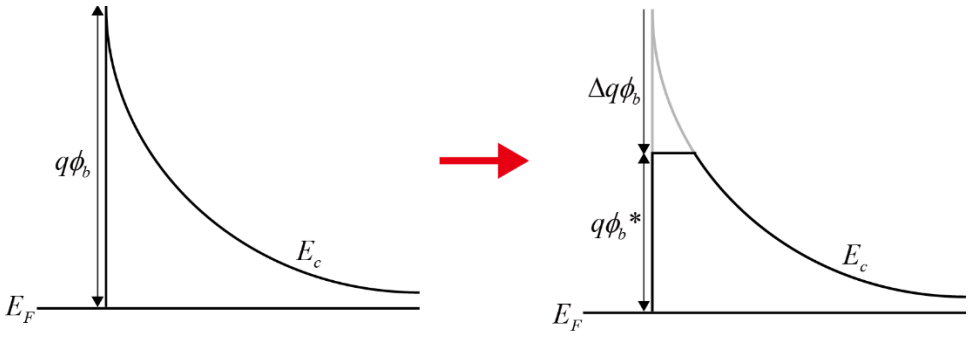

Figure 5.12 Simplified image force lowering in Schottky barrier.

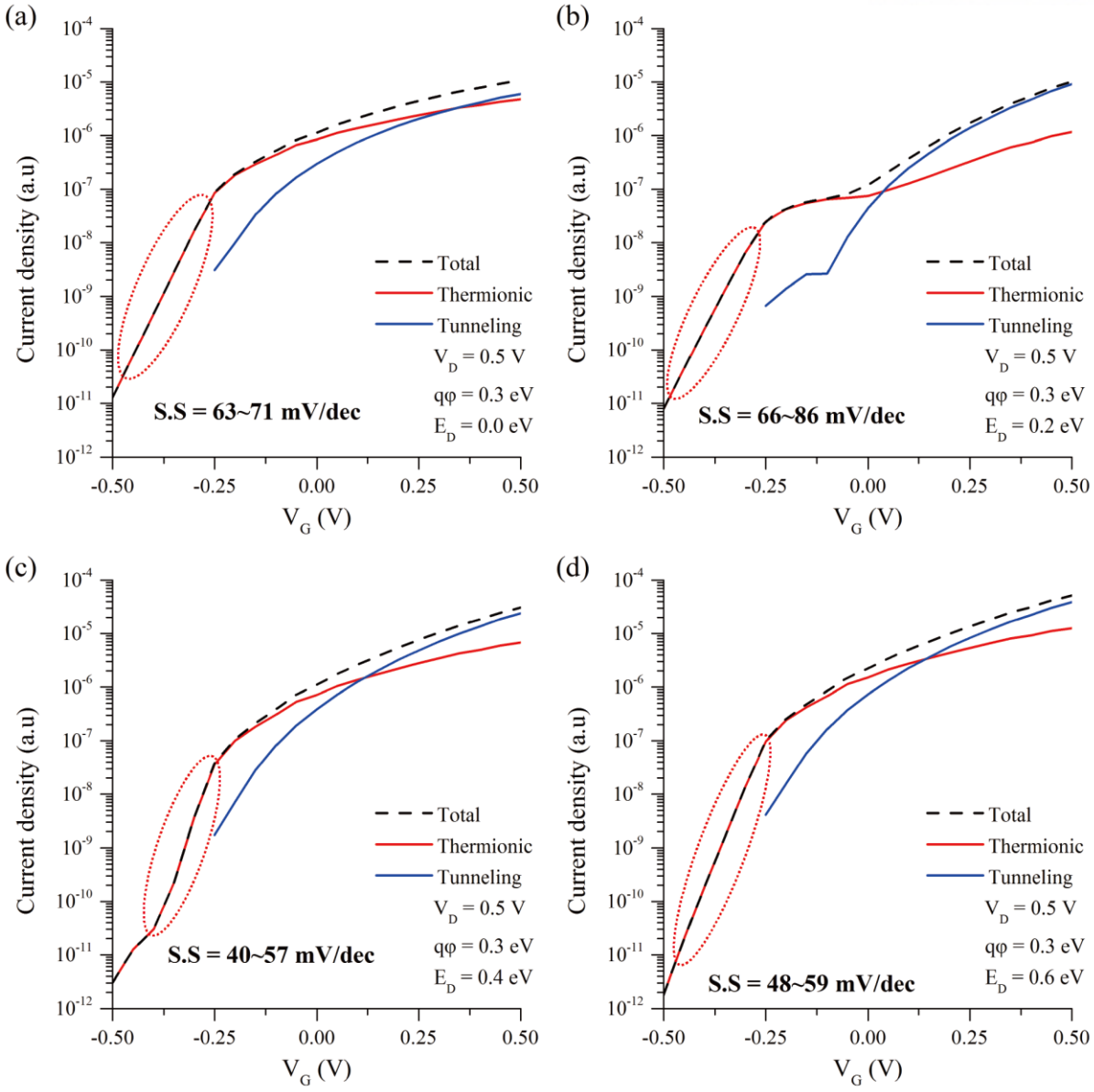

Figure 5.13 Numerically calculated transfer characteristics of graphene source MOSFET consisting of thermionic emission current and tunneling current at intrinsic Schottky barrier height of 0.3 eV with varying the difference between Dirac point and graphene fermi level (a) E_D = 0.0 eV, (b) E_D = 0.2 eV, (c) E_D = 0.4 eV, and (d) E_D = 0.6 eV.

5.3 Thermionic emission at 3 dimensional Dirac semimetal/Si interface without direct injection of carrier

In this section, thermionic emission current density for arbitrary 3 dimensional Dirac semimetal/Si interface is investigated analytically and numerically. In this case, it is forbidden to inject carriers directly into the Si substrate from the voltage supplier, as in the case of graphene in section 5.2.2. Figure 5.15 shows cross-sectional schematic of 3 dimensional Dirac Semimetal source and Si with the insulator to block carrier injection directly from Dirac Semimetal to Si.

Analytic approach

When k-space is isotropic, density of states of 3 dimensional Dirac semimetal with linear energy dispersion is

$$D(q)dq = \frac{1}{V} g_{valley} g_{spin} \frac{4\pi q^2 dq}{(2\pi / L)^3} \tag{5.42}$$

$$D(E)dE = g \frac{E^2}{2\pi^2 (\hbar v_F)^3} dE \tag{5.43}$$

Where, $g = g_{valley} g_{spin}$ is total degeneracy of the 3 dimensional Dirac semimetal. Density of states for arbitrary 3 dimensional Dirac semimetal is illustrated in Figure 5.15, which depends on energy squared. If the carrier density near the Dirac point is much lower than that of Si and thermally excited electron predominate the transport at Dirac-semimetal/Si interface, thermionic current density of the case can be demonstrated by Landauer–Büttiker formalism.

$$\begin{aligned} J &= g \frac{q}{2\pi^2 (\hbar v_F)^3 \tau} \int_{q\phi_b}^{\infty} dE (E - E_D)^2 \left(\frac{1}{e^{(E-E_F)/k_B T} + 1} - \frac{1}{e^{(E-E_{F,S})/k_B T} + 1} \right) \\ &\approx g \frac{q}{2\pi^2 (\hbar v_F)^3 \tau} \int_{q\phi_b}^{\infty} dE (E - E_D)^2 \left(e^{-(E-E_F)/k_B T} - e^{-(E-E_{F,S})/k_B T} \right) \\ &= g \frac{q k_B T}{2\pi^2 (\hbar v_F)^3 \tau} [(q\phi_b - E_D + k_B T)^2 + (k_B T)^2] e^{-(q\phi_b - E_F)/k_B T} (1 - e^{-qV/k_B T}) \end{aligned} \tag{5.44}$$

Considering (5.30) and (5.44), subthreshold swing of the case is

$$SS = \frac{1}{\eta} \frac{k_B T \ln 10}{q} \left(1 + \frac{2(q\phi_b - E_D + k_B T) k_B T}{(q\phi_b - E_D)^2} \right) \tag{5.45}$$

(5.45) has a global minimum at $q\phi_b - E_D = -2k_BT$, which gives the lowest limit of subthreshold swing such as thermodynamic limit for 3 dimensional bulk source MOSFET, which is exactly half of thermodynamic limit:

$$SS^* = \frac{k_BT \ln 10}{2q} \approx 30 \text{ mV/dec} \tag{5.46}$$

Figure 5.16 shows subthreshold swing of the 3 dimensional Dirac semimetal/Si MOSFET by Schottky barrier height $q\phi_b$ and the difference between Dirac point and graphene fermi level E_D at perfect Schottky barrier change on gate voltage $\eta = 1$. There are singularities at $q\phi_b = E_D$, near the singularities, subthreshold slope suddenly decreases when $E_D > q\phi_b$. In this condition, subthreshold swing can break the thermodynamic limit with proper Schottky barrier change on gate voltage η, as in case of p-graphene/Si interface. In case of $\eta = 1$, minimum subthreshold swing is evaluated ~ 30 mV/dec. As compare to graphene case, lowest subthreshold swing is given by theoretically such as thermodynamic limit of conventional 3 dimensional bulk source with parabolic energy dispersion. Since the density of states of 3 dimensional Dirac semimetal increases as energy squared, the range of the difference between fermi level and Dirac point for suppressing thermionic emission is effectively wider than that of graphene.

Simple numerical approach

Numerical approach is carried out in same methodology as graphene case. Energy band profiles are calculated by FlexPDE. Current densities for thermionic emission and tunneling are simulated on MATLAB. Schottky barrier height is adjusted by image force lowering with simplified adjustment as shown in Figure 5.12.

The current density of tunneling across the Schottky barrier height is evaluated with density of states for 3 dimensional Dirac semimetal, which is uniquely determined regardless of doping types unlike the graphene case:

$$J_{||,tunneling} = g\frac{q}{2\pi^2(\hbar v_F)^3\tau}\int_{q(\phi_b-\psi_{bi}-V)}^{E_D} dE(E-E_D)^2T(E) \times\left(\frac{1}{e^{(E-E_F)/k_BT}+1} - \frac{1}{e^{(E_x-E_{F,S})/k_BT}+1}\right) \tag{5.47}$$

Figure 5.17(a),(b),(c), and (d) show numerically calculated transfer characteristics of 3 dimensional Dirac semimetal source MOSFET consisting of thermionic current and tunneling current at intrinsic Schottky barrier height $q\phi_b$ of 0.3 eV with varying the difference between Dirac point and graphene fermi level E_D from 0 to 0.6 eV. Obviously, thermionic emission current overwhelms the tunneling current under all conditions calculated with all gate biases. In case of E_D = 0.4 eV and E_D = 0.6 eV, minimum subthreshold swings are evaluated as 30 mV/dec and 41 mV/dec, especially, 30 mV/dec is lowest subthreshold slope as expected in analytic approach.

5.4 Conclusion

In Dirac semimetal source, there are 2 types of thermionic current density due to direct injection from source to Si. In conventional graphene/Si structure, carrier has the vertical electron energy across the graphene layer. Meanwhile, by prohibiting the direct injection of carrier, thermally excited electrons, which induced by thermal energy or depletion field of Si, dominate thermionic emission. The difference between graphene fermi level and Dirac point affects the thermionic current density. In particular, subthreshold swing without direct injection of carriers depends on Schottky barrier height and the difference between fermi level and Dirac point, hence subthreshold swing can break the thermodynamic limit when Schottky barrier is lower than the difference between fermi level and Dirac point. Simple numerical calculations also confirms subthreshold swing below the thermodynamic limits. In addition, thermionic emission current density for arbitrary 3 dimensional Dirac semimetal/Si without direct injection of carriers also investigated, which also has the dependence on Schokttky barrier and the difference between fermi level and Dirac point. Subthreshold swing of 3 dimensional Dirac semimetal can break the thermodynamic limit when Schottky barrier is lower than the difference between fermi level and Dirac point like graphene, and lowest limit of 30 mV/dec is evaluated theoretically. In addition, numerical simulation confirms subthreshold swing and the effect of energy squared density of states on subthreshold swing.

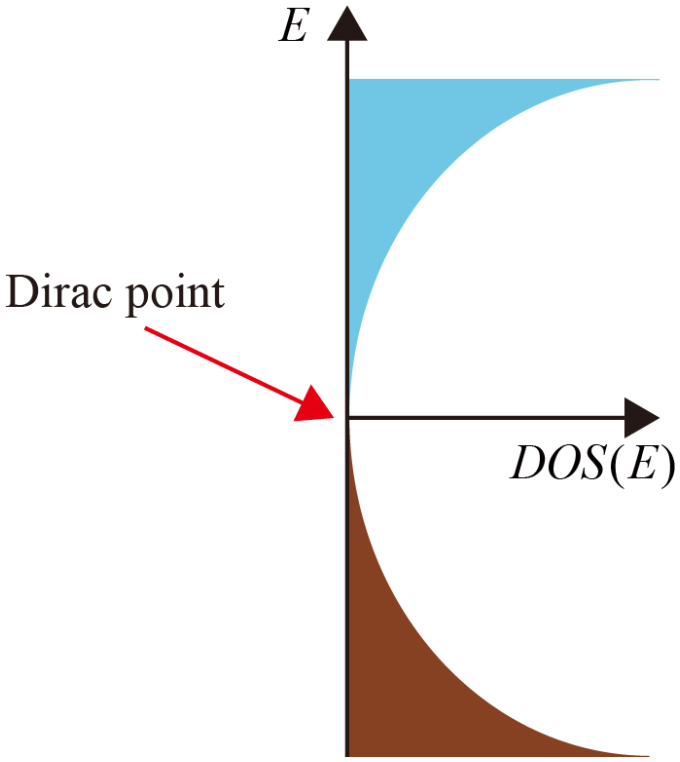

Figure 5.14 Density of states for arbitrary 3 dimensional Dirac semimetal near the Dirac point, which depends on energy squared.

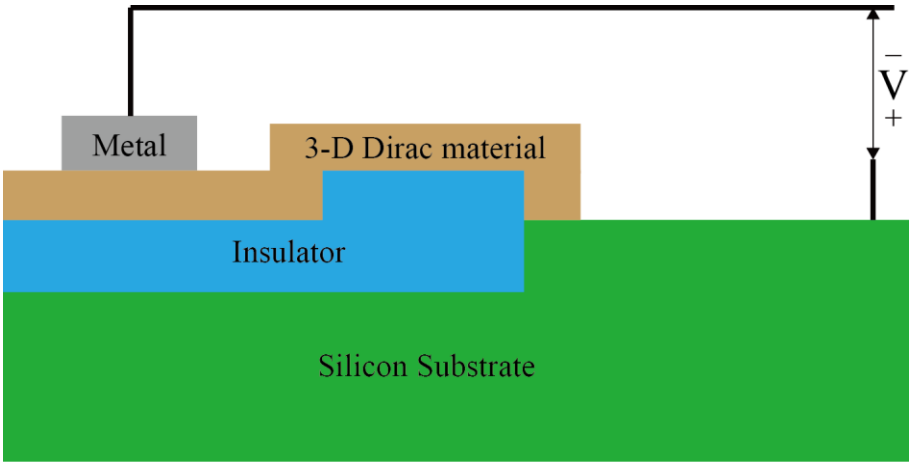

Figure 5.15 Cross-sectional schematic of 3 dimensional Dirac semimetal and Si diode.

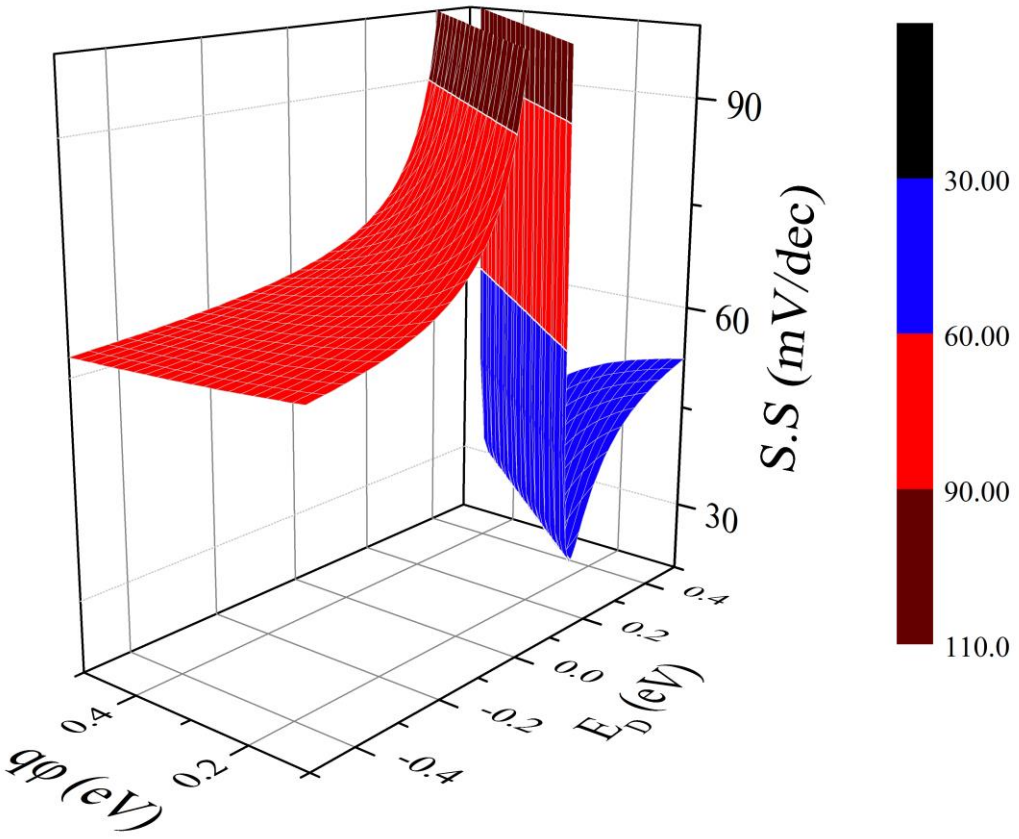

Figure 5.16 Subthreshold swing of the 3 dimensional Dirac semimetal source MOSFET at perfect Schottky barrier change on gate voltage $\eta = 1$ as varying Schottky barrier height and the difference between Dirac point and graphene fermi level.

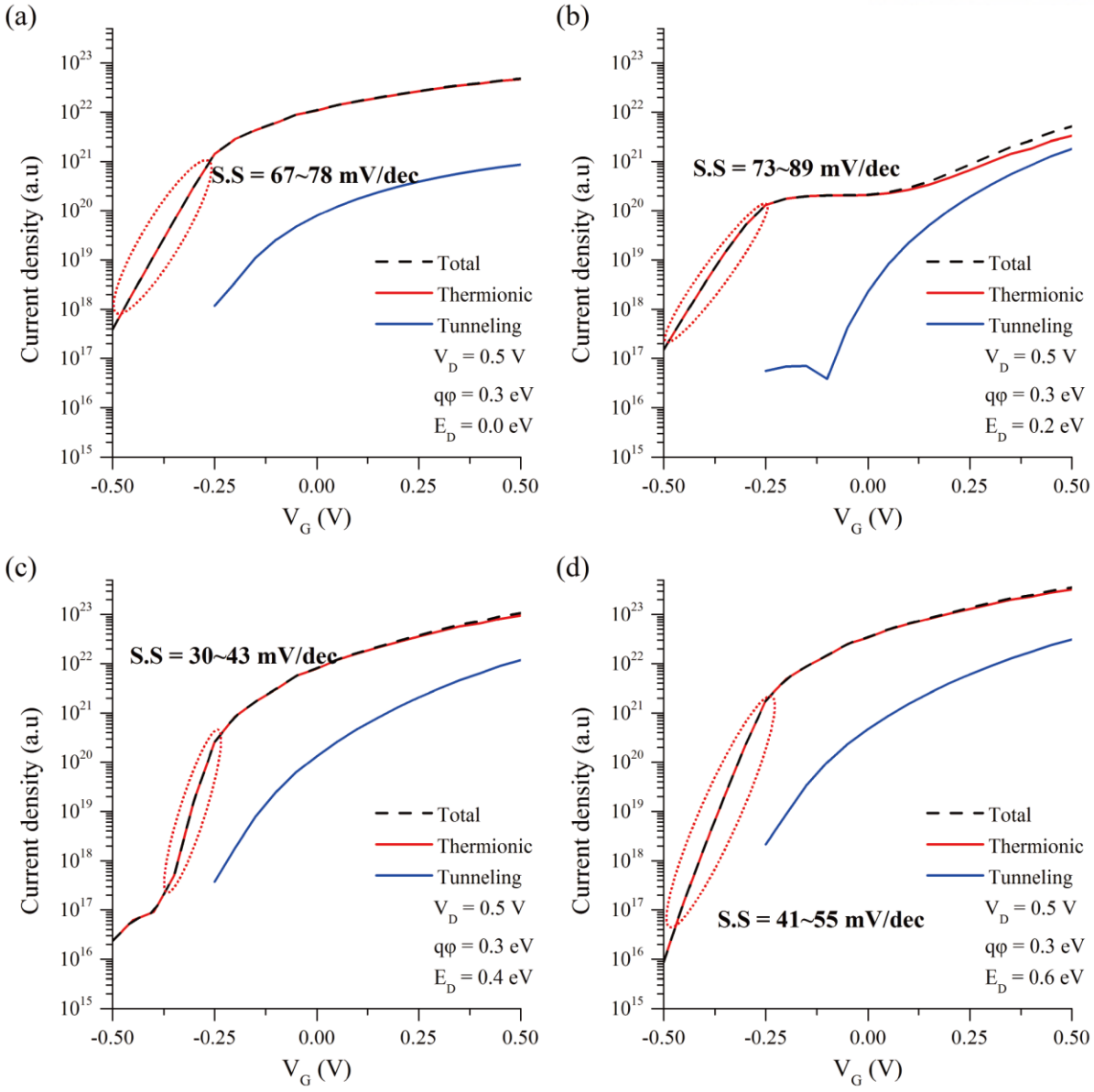

Figure 5.17 Numerically calculated transfer characteristics of 3 dimensional Dirac semimetal source MOSFET consisting of thermionic current and tunneling current at intrinsic Schottky barrier height of 0.3 eV with varying the difference between Dirac point and graphene fermi level (a) E_D = 0.0 eV, (b) E_D = 0.2 eV, (c) E_D = 0.4 eV, and (d) E_D = 0.6 eV.

Appendix A. Non Equilibrium Green's function

As the device shrinks from the micrometer scale to the nanometer scale, conventional device physics based prediction show inaccurate results because the quantum effects neglected in the semi-classical approach become significant or not enough for non-equilibrium thermodynamics. Especially, quantum transport has become important due to quantum confinement on channel of FinFET and gate-all-around FET [76][77]. One of the effective ways to solve this problem, NEGF is one of the successful ways of handling quantum approaches.

A.1 Non Equilibrium Green's function (NEGF)

In 1964, Keldysh pioneered the NEGF method for treat the thermodynamic non equilibrium system such as electrons in strong electric field which is established by analogue technique of Feynman diagram [78]. Since the first formulation of Keldysh's NEGF, other perspectives are appeared such as many-body perturbation theory (MBPT) and Datta's one-electron Schrödinger equation approach. In this work, Datta's NEGF perspective is adopted which is one of most widely used in Nano-electronics [78][79].

A.1.1 Formalism of Non Equilibrium Green's function (NEGF)

Isolated contact system

Start with time-independent Schrodinger equation, the isolated system without any external potential is described with wave function Ψ

$$E\Psi = H\Psi \tag{A.1}$$

E is the energy of the system and H is the Hamiltonian of the system. When the system is connected to arbitrary source, extraction of electron from the system and injection to the system can be occurred, then Schrodinger equation becomes

$$(E - H + i0^{+})\Psi = S \tag{A.2}$$

$i0^{+}\Psi$ is electron extraction from the system to source and S is reinjection from source to the system, therefore chemical potential of the system is maintained with relation of $i0^{+}\Psi = S$. If there are another system B which coupling to original system A, then the coupling between system A and system B is described by coupling Hamiltonian τ. Schrodinger equations can be expressed in the form

of matrix:

$$\begin{pmatrix} E_A - H_A + i0^+ & -\tau^\dagger \\ -\tau & E - H \end{pmatrix} \begin{pmatrix} \Psi_A + \theta \\ \Psi \end{pmatrix} = \begin{pmatrix} S_A \\ 0 \end{pmatrix} \tag{A.3}$$

Where H_A is the Hamiltonian of system A, H is the Hamiltonian of system B and θ is scattered wave function in system A, which is due to coupling with system B when the extraction and reinjection are occurred on system A. Solving the matrix with (5.3) give

$$(E_A - H_A + i0)\theta = \tau^\dagger \Psi \tag{A.4}$$

$$\theta = \frac{\tau^\dagger \Psi}{E_A - H_A + i0} \tag{A.5}$$

$$\begin{aligned} \tau\psi_A &= (E - H)\Psi - \tau\theta \\ &= (E - H)\Psi - \tau \frac{1}{E_A - H_A + i0} \tau^\dagger \Psi \end{aligned} \tag{A.6}$$

Let's define,

$$S = \tau\Psi_A \tag{A.7}$$

$$\Sigma = \tau \frac{1}{E_A - H_A + i0} \tau^\dagger \tag{A.8}$$

Now, Schrödinger equation of channel with a single contact become

$$(E - H - \Sigma)\Psi = S \tag{A.9}$$

In the device, this description is equivalent with contact (system A) and channel (system B). From (A.9), outflow of the channel is determined by self-energy Σ and wave function of the channel, as shown in (A.8), self-energy is described by coupling with energy and Hamiltonian of contact A (In theoretical physics, the energy change that occurs in the environment is called self-energy). However, the inflow of channel is independent with the channel and they only depend on the coupling from the contact. Hence, description of (A.2) is maintained in (A.9). Finally, define the Green's function for isolated contact by rearrange the Schrödinger equation:

$$\Psi = \frac{S}{E - H - \Sigma} = GS \tag{A.10}$$

$$G = (E - H - \Sigma)^{-1} \tag{A.11}$$

Hamiltonian of the channel give complex eigen energy and eigen function due to self-energy of the channel. Hence, broadened the density of state and eigen state with finite time is induced, it is described in latter section [79].

Local density of states (LDOS)

Local density of state (LDOS) with eigen energy in the channel is expressed in generally,

$$D(\vec{r};E) = \sum_n |\psi_n(\vec{r})|^2 \, \delta(E - \varepsilon_n) \tag{A.12}$$

Where ε_n is eigen energy of state n, $\vec{r}$ is position in the channel and δ is Dirac-delta function. In general, LDOS is diagonal element of spectral function A, matrix element of spectral function A is

$$A(\vec{r},\vec{r}';E) = 2\pi \sum_n \psi_n(\vec{r})\psi_n^*(\vec{r}')\delta(E - \varepsilon_n) \tag{A.13}$$

Unitary transformation on spectral function A from an energy space to a real space is

$$Tr_{\vec{r},\mathrm{n}} = \psi_n(\vec{r}) \tag{A.14}$$

$$Tr_{\vec{r},\mathrm{n}}^{-1} = Tr_{\vec{r},\mathrm{n}}^{\dagger} = Tr_{\vec{r},\mathrm{n}}^{*} = \psi_n^*(\vec{r}) \tag{A.15}$$

$$A(\vec{r},\vec{r}';E) = 2\pi \sum_n \sum_m Tr_{\vec{r},\mathrm{n}} \delta(E - \varepsilon_n) Tr_{\vec{r}',m}^{\dagger} \tag{A.16}$$

Where $Tr_{\vec{r},\mathrm{n}}$ is unitary transformation matrix between eigenstates n and real space $\vec{r}$. Hence, spectral function in eigen state $A(E)$ is

$$A(E) = 2\pi\delta(E - H) \tag{A.17}$$

In the mathematics, one of alternative form of Dirac delta function is

$$\begin{aligned} \delta(a-b) &= \lim_{c\to 0^+} \frac{2c}{(a-b)^2 + c^2} \\ &= i\left[\frac{1}{a-b+i0^+} - \frac{1}{a-b-i0^+}\right] \end{aligned} \tag{A.18}$$

Therefore, spectral function in energy can be expressed as

$$A(E) = 2\pi\delta(E-H) = i\left[\frac{1}{E+i0^{+}-H} - \frac{1}{E-i0^{+}-H}\right] = i(G-G^{\dagger}) \tag{A.19}$$

Imaginary part of green's function affect the shape of LDOS [79].

Physical meaning of Green's function

In the previous sections, Green's function is derived in the view of quantum physics, however physical interpretation is not clear. To get the insight on Green's function, let's try the Fourier transform to Green' function [79].

$$\begin{aligned} G(t) &= \int_{-\infty}^{\infty}\frac{dE}{2\pi\hbar}e^{iEt/\hbar}G(E) \\ &= \int_{-\infty}^{\infty}\frac{dE}{2\pi\hbar}e^{iEt/\hbar}\begin{pmatrix} 1/(E-\varepsilon_1+i0^{+}) & 0 & \cdots \\ 0 & 1/(E-\varepsilon_2+i0^{+}) & \cdots \\ \cdots & \cdots & \cdots \end{pmatrix} \\ &= -\frac{i}{\hbar}\Theta(t)e^{-0^{+}t/\hbar}\begin{pmatrix} e^{-i\varepsilon_1 t/\hbar} & 0 & \cdots \\ 0 & e^{-i\varepsilon_2 t/\hbar} & \cdots \\ \cdots & \cdots & \cdots \end{pmatrix} \end{aligned} \tag{A.20}$$

$$G(t) = G^{\dagger *}(t) \tag{A.21}$$

Where $\Theta(t)$ is Heaviside step function. Hence, Green's function $G(t)$ is always zero when time is negative $t<0$, it could be called retarded Green's function. Similarly, $G^{\dagger}$ is called advanced Green's function. In addition, retarded Green's function satisfied the differential relation as

$$\left(i\hbar\frac{\partial}{\partial t}-H\right)G(t) = \delta(\mathrm{t})\frac{G(t)}{\Theta(t)} = \delta(\mathrm{t})G(t) \tag{A.22}$$

$$\left(i\hbar\frac{\partial}{\partial t}-H\right)\Psi(t) = 0 \tag{A.23}$$

Therefore, there are suggestion of retarded Green's function regrading as the impulse response at $t=0$, but advanced Green's function has no physical meaning which is only the mathematical solution [79].

Carrier concentration

From the quantum physics, quantum probability density (or probability amplitude) is related with the square modulus of the wave function $\Psi\Psi^{\dagger}$. In the NEGF formalism according to (A.10), then quantum probability density $\Psi\Psi^{\dagger}$ give

$$SS^{\dagger} = \Sigma^{in} = -i\Sigma^{<} \tag{A.24}$$

$$\begin{aligned} \Psi\Psi^{\dagger} &= GSS^{\dagger}G^{\dagger} = G\Sigma^{in}G^{\dagger} \\ &= G^{n} = -iG^{<} \end{aligned} \tag{A.25}$$

$$G^{n} = G\Sigma^{in}G^{\dagger} \tag{A.26}$$

Therefore, electron correlation function G^{n} related with the electron density in the system and Σ_{in} is inflow self-energy related with density of carrier inflow from the contact, they are easily change the notation to Keldysh's lessor Green's function $G^{<}$ and lessor self-energy $\Sigma^{<}$ [78]. Similarly, hole correlation function G^{p}, which showed hole density in the system, and total local density of state (LDOS) called the spectral function A are

$$G^{p} = G\sum^{out} G^{\dagger} \tag{A.27}$$

$$A = G^{n} + G^{p} = G(\Sigma^{in} + \Sigma^{out})G^{\dagger} \tag{A.28}$$

Then, how can we determined self-energies of inflow $\sum^{in}$ and outflow $\sum^{out}$ (in fact, they are different with self-energy)? Before using the NEGF, only the self-energy of source Σ_{S} and drain Σ_{D} can be obtained by solution of Hamiltonian for source and drain analytically or numerically. In the latter part of the section, self-energies of inflow and outflow are defined.

Total self-energy is

$$\Sigma = \Sigma_{S} + \Sigma_{D} + \Sigma_{sc} \tag{A.29}$$

Where Σ_{sc} is self-energy of carrier scattering in the channel. Self-energies of source and drain are given by Hamiltonian of source and drain, respectively, as mentioned, however self-energy of scattering is determined by NEGF method self-consistently, which is discussed in latter section. From the total self-energy, we can get the level broadening function Γ, which is

$$\Gamma = i(\Sigma + \Sigma^{\dagger}) = \Sigma^{in} + \Sigma^{out} \tag{A.30}$$

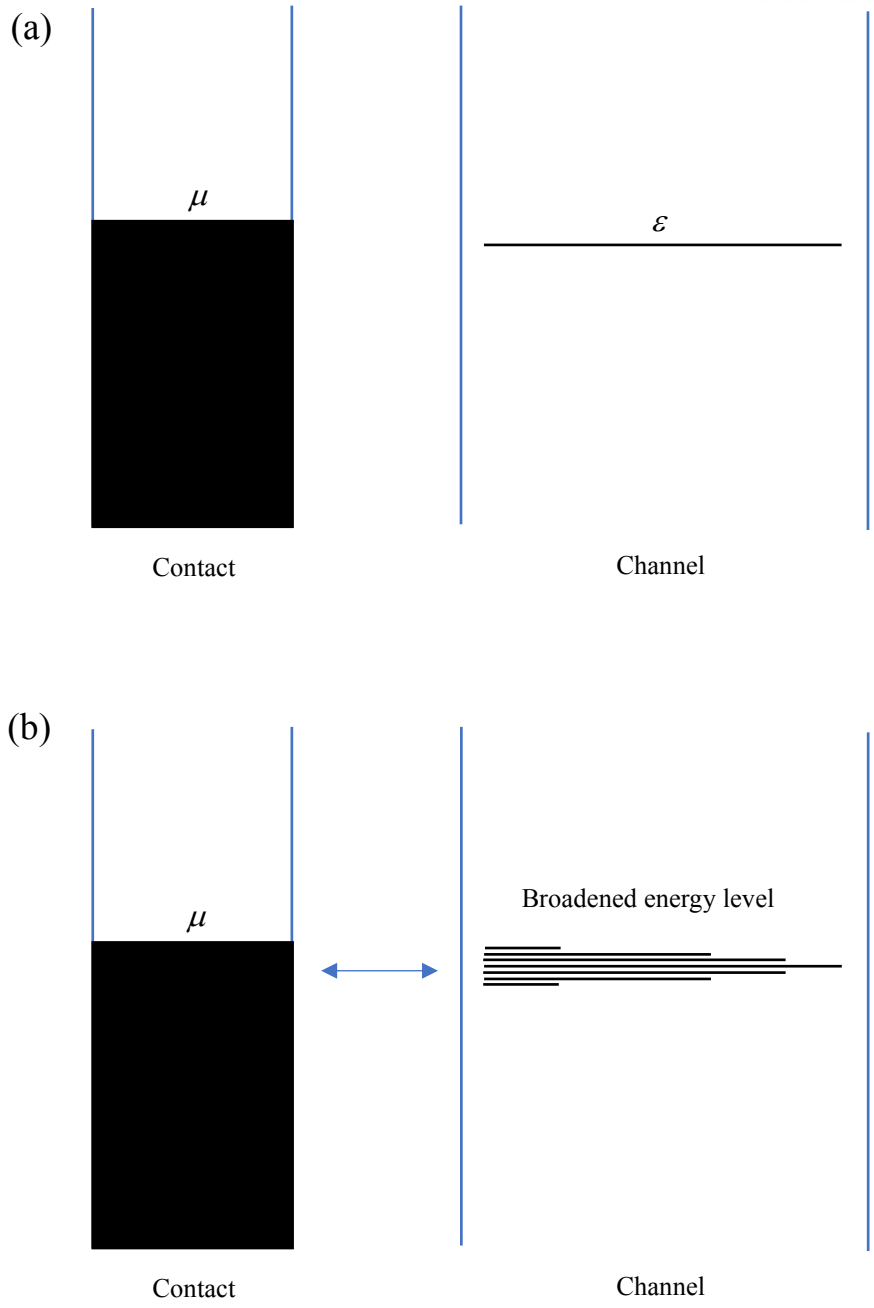

Figure A.1 (a) energy diagram of single level channel and (b) energy diagram of broadened energy level channel due to coupling of contact.

In the (A.28) with (A.29), imaginary part of self-energy describe the LDOS with Green's function, in this reason, which is called broadening function. For the connection of LDOS in (A.19) and (A.28), let's rewrite the representation with (A.11)

$$\Sigma - \Sigma^{\dagger} = (G^{\dagger})^{-1} - G^{-1} \tag{A.31}$$

$$\begin{aligned} G\Gamma G^{\dagger} &= iG(\Sigma - \Sigma^{\dagger})G^{\dagger} = iG((G^{\dagger})^{-1} - G^{-1})G^{\dagger} \\ &= iG^{\dagger}((G^{\dagger})^{-1} - G^{-1})\mathrm{G} = i(G - G^{\dagger}) = \mathrm{A} \end{aligned} \tag{A.32}$$

Figure A.1(a) shows the simple schematic of energy level with single level state in channel when the coupling occurred with energy state in the channel and the contact, energy state in channel is broadened by the contact shown in figure A.1(b).

Inflow and outflow self-energy of source and drain are defined with energy broadening function and Fermi-Dirac statistics (which have convenience for recognize the properties respectively, and they are broadening function, not the self-energy):

$$\Sigma_S^{in} = \Gamma_S f_{FD}(E - \mu_S) \tag{A.33}$$

$$\Sigma_D^{in} = \Gamma_D f_{FD}(E - \mu_D) \tag{A.34}$$

$$\Sigma_S^{out} = \Gamma_S[1 - f_{FD}(E - \mu_S)] \tag{A.35}$$

$$\Sigma_D^{out} = \Gamma_D[1 - f_{FD}(E - \mu_D)] \tag{A.36}$$

$$f_{FD} = \frac{1}{e^{(E-\mu)/k_B T} + 1} \tag{A.37}$$

Where, μ is the chemical potential of the contact, k_B is the Boltzmann constant, T is temperature, and f_{FD} is function of the Fermi-Dirac statistics. Finally, inflow total self-energy and outflow total self-energy are

$$\Sigma^{in} = \Sigma_S^{in} + \Sigma_D^{in} \tag{A.38}$$

$$\Sigma^{out} = \Sigma_S^{out} + \Sigma_D^{out} \tag{A.39}$$

Going back to the spectral function A, there is an alternative representation that distinguishes the

LDOS from source A_S and drain A_D with (A.38) and (A.39):

$$A_S = G\Gamma_S G^\dagger \tag{A.40}$$

$$A_D = G\Gamma_D G^\dagger \tag{A.41}$$

$$A = A_S + A_D \tag{A.42}$$

Connection between spectral function A and electron correlation function G^n and hole correlation function G^p can be expressed as

$$\begin{aligned} G^n &= G\Sigma^{in}G^\dagger = G(\Sigma_S^{in} + \Sigma_D^{in})G^\dagger \\ &= G\Gamma_S G^\dagger f_{FD}(E-\mu_S) + G\Gamma_D G^\dagger f_{FD}(E-\mu_D) \\ &= A_S f_{FD}(E-\mu_S) + A_D f_{FD}(E-\mu_D) \end{aligned} \tag{A.43}$$

$$G^p = A_S[1-f_{FD}(E-\mu_S)] + A_D[1-f_{FD}(E-\mu_D)] \tag{A.44}$$

The total electron density n and the total hole density p is determined by

$$\begin{aligned} n &= \int_{-\infty}^{\infty} \frac{dE}{2\pi} G^n(E) \\ &= \int_{-\infty}^{\infty} \frac{dE}{2\pi} [A_S(E) f_{FD}(E-\mu_S) + A_D(E) f_{FD}(E-\mu_D)] \end{aligned} \tag{A.45}$$

$$\begin{aligned} p &= \int_{-\infty}^{\infty} \frac{dE}{2\pi} G^p(E) \\ &= \int_{-\infty}^{\infty} \frac{dE}{2\pi} [A_S(E)(1-f_{FD}(E-\mu_S)) + A_D(E)(1-f_{FD}(E-\mu_D))] \end{aligned} \tag{A.46}$$

Now, we can solve the Poisson's equation from electron density n and hole density p in self-consistently.

A.1.2 Transmission and electric current with NEGF

In the previous section, formalism of NEGF is started with time independent Schrödinger equation on device with a single contact. In this section, I will discuss about current and transmission with NEGF, electric current is determined with

$$I = \frac{d}{dt}(\psi\psi^{\dagger}) \tag{A.47}$$

Therefore, time dependent Schrödinger equation is required to derive the electric current. Time dependent Schrödinger equation for inflow and outflow in matrix form is given by (which is same case with previous section, only difference is indexing 'i' to S)

$$i\hbar\frac{d}{dt}\psi = H\psi + \Sigma\psi + S_i \tag{A.48}$$

$$-i\hbar\frac{d}{dt}\psi^{\dagger} = H\psi^{\dagger} + \psi^{\dagger}\Sigma^{\dagger} + S_i^{\dagger} \tag{A.49}$$

The electric current between channel and contact at terminal 'i' in matrix form is

$$\begin{aligned}
I_i(E) &= trace\left(\frac{d}{dt}(\psi\psi^{\dagger})\right) = trace\left(\frac{d\psi}{dt}\psi^{\dagger} + \psi\frac{d\psi^{\dagger}}{dt}\right) \\
&= trace\left(\frac{H\psi\psi^{\dagger} + \Sigma\psi\psi^{\dagger} + S_i\psi^{\dagger}}{i\hbar} - \frac{\psi H\psi^{\dagger} + \psi\psi^{\dagger}\Sigma^{\dagger} + \psi S_i^{\dagger}}{i\hbar}\right) \\
&= trace\left(\frac{S_i\psi^{\dagger} - \psi S_i^{\dagger}}{i\hbar} - \frac{\psi\psi^{\dagger}\Sigma^{\dagger} - \Sigma\psi\psi^{\dagger}}{i\hbar}\right) \\
&= trace\left(\frac{S_iS_i^{\dagger}G^{\dagger} - GS_iS_i^{\dagger}}{i\hbar} - \frac{G^n\Sigma^{\dagger} - \Sigma G^n}{i\hbar}\right) \\
&= trace\left(\Sigma_i i\frac{G - G^{\dagger}}{\hbar} - i\frac{\Sigma_i - \Sigma_i^{\dagger}}{\hbar}G^n\right) \\
&= trace\left(\Sigma_i A - \Gamma_i G^n\right) \\
&= trace\left(\Gamma_i A\right) f_{FD}(E - \mu_i) - trace\left(\Gamma_i G^n\right)
\end{aligned} \tag{A.50}$$

In this expression, inflow electric current is $trace\left(\Gamma_i A\right) f_{FD}(E-\mu_i)$ and outflow electric current is $trace\left(\Gamma_i G^n\right)$ as shown Figure A.2. The net electric current in contact 'i' determined by Landauer formalism is [73][80]

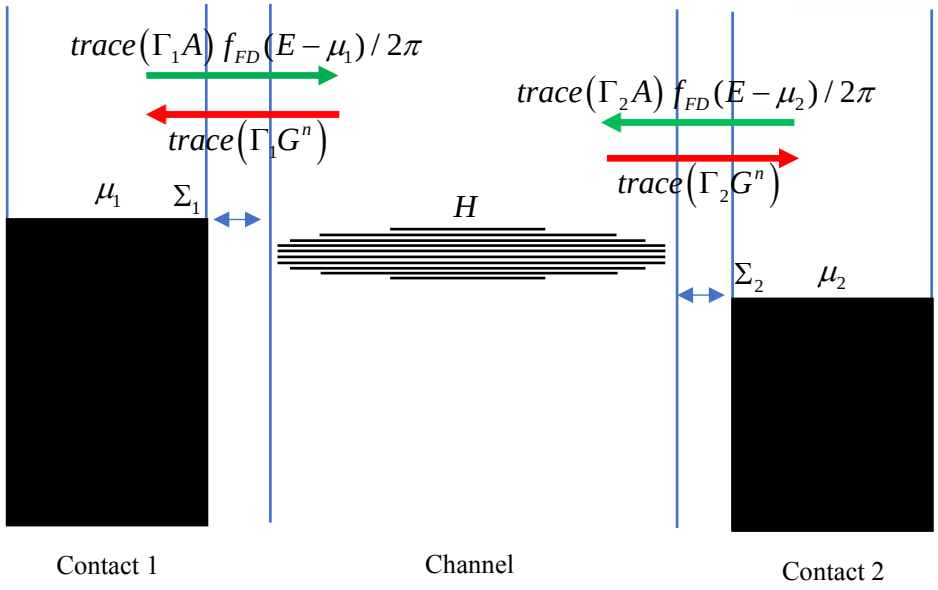

Figure A.2 Schematic shows Inflow and outflow between contact and channel, the coupling between channel and contact is demonstrated by self-energy.

$$I_i = -\frac{q}{\hbar}\int_{-\infty}^{\infty}\frac{dE}{2\pi}T_i(E) \tag{A.51}$$

$$T_i(E) = \left[trace\left(\Gamma_i A\right) f_{FD}(E-\mu_i) - trace\left(\Gamma_i G^n\right)\right] \tag{A.52}$$

Where, T_i is transmission probability of contact 'i'. However, it is not the conventional form of transmission probability. If there are two contact on channel, for example source and drain, then I_S and $-I_D$ are must be equal (considering direction shown in Figure A.2). Transmission probability in the case become

$$\begin{aligned} T_S(E) &= trace\left(\Gamma_S A\right) f_{FD}(E-\mu_S) - trace\left(\Gamma_S G^n\right) \\ &= trace\left(\Gamma_S (A_S + A_D) f_{FD}(E-\mu_S)\right) \\ &\quad - trace\left(\Gamma_S [A_S f_{FD}(E-\mu_S) + A_D f_{FD}(E-\mu_D)]\right) \\ &= trace\left(\Gamma_S A_D\right)\left(f_{FD}(E-\mu_S) - f_{FD}(E-\mu_D)\right) \\ &= -T_D(E) \\ &= trace\left(\Gamma_D A_S\right)[f_{FD}(E-\mu_S) - f_{FD}(E-\mu_D)] \end{aligned} \tag{A.53}$$

As a result, transmission probability is expressed as conventional form in the source and drain contact case, then the net electric current in this case become

$$I = -\frac{q}{\hbar}\int_{-\infty}^{\infty}\frac{dE}{2\pi}T(E)[f_{FD}(E-\mu_S) - f_{FD}(E-\mu_D)] \tag{A.54}$$

$$\begin{aligned} T(E) &= trace\left(\Gamma_D A_S\right) = trace\left(\Gamma_S A_D\right) \\ &= trace\left(\Gamma_S G \Gamma_D G^{\dagger}\right) = trace\left(\Gamma_D G \Gamma_S G^{\dagger}\right) \end{aligned} \tag{A.55}$$

Where, $T(E)$ is transmission function. The net electric current is described by transmission function and difference of Fermi-Dirac function in source and drain.

A.1.3 Electron-Phonon scattering formalism in NEGF

General electron-phonon scattering formalism in NEGF

In according to self-consistent Born approximation, the self-energy of scattering is described by the phonon propagator and carrier correlation function as [81][82]

$$\Sigma_{sc}^{in}(x_1,x_2) = D^n(x_1,x_2)G^n(x_1,x_2) \tag{A.56}$$

$$\Sigma_{sc}^{out}(x_1,x_2) = D^p(x_1,x_2)G^p(x_1,x_2) \tag{A.57}$$

Where x_1 and x_2 are space-time $(\vec{r}_1,t_1)$ and $(\vec{r}_2,t_2)$. The phonon propagators D^n and D^p are consists of the electron-phonon scattering Hamiltonian by angle bracket, the phonon propagator and electron-phonon Hamiltonian are [81][82]

$$H_{ph}(x) = \sum_{\vec{q}} M_{\vec{q}} a_{\vec{q}} (b_{\vec{q}} e^{-i\omega_{\vec{q}}t + i\vec{q}\cdot\vec{r}} + b_{\vec{q}}^{\dagger} e^{-i\omega_{\vec{q}}t + i\vec{q}\cdot\vec{r}}) \tag{A.58}$$

$$a_{\vec{q}} = \sqrt{\frac{\hbar}{2\omega_{\vec{q}}\rho V}} \tag{A.59}$$

$$D^n(x_1,x_2) = \left\langle H_{eph}(x_1)H_{eph}(x_2)\right\rangle \tag{A.60}$$

$$D^p(x_1,x_2) = \left\langle H_{eph}(x_2)H_{eph}(x_1)\right\rangle \tag{A.61}$$

Where $b_{\vec{q}}$ and $b_{\vec{q}}^{\dagger}$ are phonon annihilation and creation operator on phonon wave vector $\vec{q}$, $M_{\vec{q}}$ is electron-phonon deformation potential matrix element on $\vec{q}$, $a_{\vec{q}}$ is the half-amplitude of single phonon in the channel volume V, ρ is mass/volume density of system and $\omega_{\vec{q}}$ is the angular frequency on $\vec{q}$. Properties of annihilation and creation operator give

$$\left\langle b_{\vec{q}}^{\dagger} b_{\vec{q}'}\right\rangle = n_{\vec{q}}\delta(\vec{q}-\vec{q}') \tag{A.62}$$

$$\left\langle b_{\vec{q}} b_{\vec{q}}^{\dagger}\right\rangle = (n_{\vec{q}}+1)\delta(\vec{q}-\vec{q}') \tag{A.63}$$

Where $n_{\vec{q}}$ is occupation number for wave vector $\vec{q}$. In this case, $n_{\vec{q}}$ is the function of Bose-Einstein statistics considering that phonon is boson. Therefore, phonon propagator become

$$\begin{aligned} D^n(x_1,x_2) &= \left\langle H_{eph}(x_1)H_{eph}(x_2)\right\rangle \\ &= \left\langle \sum_{\vec{q},\vec{q}'} M_{\vec{q}}M_{\vec{q}'}a_{\vec{q}}a_{\vec{q}'}(b_{\vec{q}}e^{-i\omega_{\vec{q}}t_1+i\vec{q}\cdot\vec{r}_1}+b_{\vec{q}}^{\dagger}e^{-i\omega_{\vec{q}}t_1+i\vec{q}\cdot\vec{r}_1}) \right. \\ &\qquad \left. \times(b_{\vec{q}'}e^{-i\omega_{\vec{q}'}t_2+i\vec{q}'\cdot\vec{r}_2}+b_{\vec{q}'}^{\dagger}e^{-i\omega_{\vec{q}'}t_2+i\vec{q}'\cdot\vec{r}_2})\right\rangle \\ &= \sum_{\vec{q}}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2[(n_{\vec{q}}+1)e^{i\omega_{\vec{q}}(t_2-t_1)+i\vec{q}\cdot(\vec{r}_1-\vec{r}_2)}+n_{\vec{q}}e^{i\omega_{\vec{q}}(t_1-t_2)+i\vec{q}\cdot(\vec{r}_2-\vec{r}_1)}] \end{aligned} \tag{A.64}$$

$$n_{\vec{q}} = \frac{1}{e^{\hbar\omega_{\vec{q}}/k_BT}-1} \tag{A.65}$$

Fourier transform of the scattering self-energy from time interval t_2-t_1 to energy E in steady state give

$$\begin{aligned} \Sigma_{sc}^{in}(\vec{r}_1,\vec{r}_2,E) &= \int\frac{d(t_2-t_1)}{2\pi}e^{iE(t_2-t_1)}\Sigma_{sc}^{in}(t_1,t_2) \\ &= \sum_{\vec{q}}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i\vec{q}\cdot(\vec{r}_1-\vec{r}_2)}(n_{\vec{q}}+1)G^n(\vec{r}_1,\vec{r}_2,E+\hbar\omega_{\vec{q}}) \\ &\quad +\sum_{\vec{q}}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{-i\vec{q}\cdot(\vec{r}_1-\vec{r}_2)}n_{\vec{q}}G^n(\vec{r}_1,\vec{r}_2,E-\hbar\omega_{\vec{q}}) \end{aligned} \tag{A.66}$$

$$\begin{aligned} \Sigma_{sc}^{out}(\vec{r}_1,\vec{r}_2,E) &= \sum_{\vec{q}}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{-i\vec{q}\cdot(\vec{r}_1-\vec{r}_2)}(n_{\vec{q}}+1)G^p(\vec{r}_1,\vec{r}_2,E-\hbar\omega_{\vec{q}}) \\ &\quad +\sum_{\vec{q}}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i\vec{q}\cdot(\vec{r}_1-\vec{r}_2)}n_{\vec{q}}G^p(\vec{r}_1,\vec{r}_2,E+\hbar\omega_{\vec{q}}) \end{aligned} \tag{A.67}$$

$$D(r_1,r_2,E) = \sum_{\vec{q}}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i\vec{q}\cdot(\vec{r}_1-\vec{r}_2)} \tag{A.68}$$

Where, D is the electron-phonon scattering operator. However, confinement is different as the system. For example, Fin-FET is confined in all directions (x, y, z), but planar FET is confined in device length and width directions (x, y). Let's investigate the case of unconfined transverse direction with plane wave function on wave vector $\vec{k}$ (N is for normalization, it is the number of grid for the NEGF simulation) [83]:

$$\psi_{\vec{k}} = \frac{e^{i\vec{k}\cdot\vec{r}}}{\sqrt{N}}, \qquad \left(\psi_{\vec{k}_t} = \frac{e^{i\vec{k}_t\cdot\vec{r}_t}}{\sqrt{N}}\right) \tag{A.69}$$

$$G^n(\vec{r}_1,\vec{r}_2,E) = \frac{1}{N}\sum_{\vec{k}_{1t}',\vec{k}_{2t}'} e^{i(\vec{k}_{1t}'\cdot\vec{r}_{1t}-\vec{k}_{2t}'\cdot\vec{r}_{2t})}G^n(\vec{r}_{1l},\vec{r}_{2l},\vec{k}_{1t}',\vec{k}_{2t}',E) \tag{A.70}$$

$$\begin{aligned}\Sigma_{sc}^{in}(\vec{r}_{1l},\vec{r}_{2l},\vec{k}_{1t},\vec{k}_{2t},E) &= \frac{1}{N}\sum_{\vec{r}_{1t},\vec{r}_{2t}} e^{i(\vec{k}_{1t}\cdot\vec{r}_{1t}-\vec{k}_{2t}\cdot\vec{r}_{2t})}\Sigma_{sc}^{in}(\vec{r}_1,\vec{r}_2,E) \\ &= \frac{1}{N^2}\sum_{\vec{r}_{1t},\vec{r}_{2t}} e^{i(\vec{k}_{1t}\cdot\vec{r}_{1t}-\vec{k}_{2t}\cdot\vec{r}_{2t})} \\ &\quad\times\sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i(\vec{q}_l\cdot(\vec{r}_{1l}-\vec{r}_{2l})+\vec{q}_t\cdot(\vec{r}_{1t}-\vec{r}_{2t}))}(n_{\vec{q}}+1) \\ &\quad\times\sum_{\vec{k}_{1t}',\vec{k}_{2t}'} e^{i(\vec{k}_{1t}'\cdot\vec{r}_{1t}-\vec{k}_{2t}'\cdot\vec{r}_{2t})}G^n(\vec{r}_{1l},\vec{r}_{2l},\vec{k}_{1t}',\vec{k}_{2t}',E+\hbar\omega_{\vec{q}})+. \\ &= \frac{1}{N^2}\sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i\vec{q}_l\cdot(\vec{r}_{1l}-\vec{r}_{2l})}(n_{\vec{q}}+1) \\ &\quad\times\sum_{\vec{k}_{1t}',\vec{k}_{2t}'} G^n(\vec{r}_{1l},\vec{r}_{2l},\vec{k}_{1t}',\vec{k}_{2t}',E+\hbar\omega_{\vec{q}}) \\ &\quad\times\delta(\vec{k}_{1t}'-\vec{k}_{1t}+\vec{q}_t)\delta(\vec{k}_{2t}'-\vec{k}_{2t}+\vec{q}_t)+...\end{aligned} \tag{A.71}$$

As a result, the scattering self-energy of inflow and outflow in unconfined transverse direction $\vec{k}$ (= $\vec{k}_t$) is

$$\begin{aligned}\Sigma_{sc}^{in}(\vec{r}_1,\vec{r}_2,\vec{k},E) &= \sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i\vec{q}_l\cdot(\vec{r}_1-\vec{r}_2)}(n_{\vec{q}}+1)G^n(\vec{r}_1,\vec{r}_2,\vec{k}+\vec{q}_t,E+\hbar\omega_{\vec{q}}) \\ &\quad+\sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{-i\vec{q}_l\cdot(\vec{r}_1-\vec{r}_2)}n_{\vec{q}}G^n(\vec{r}_1,\vec{r}_2,\vec{k}-\vec{q}_t,E-\hbar\omega_{\vec{q}})\end{aligned} \tag{A.72}$$

$$\begin{aligned}\Sigma_{sc}^{out}(\vec{r}_1,\vec{r}_2,\vec{k},E) &= \sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i\vec{q}_l\cdot(\vec{r}_1-\vec{r}_2)}(n_{\vec{q}}+1)G^p(\vec{r}_1,\vec{r}_2,\vec{k}-\vec{q}_t,E-\hbar\omega_{\vec{q}}) \\ &\quad+\sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{-i\vec{q}_l\cdot(\vec{r}_1-\vec{r}_2)}n_{\vec{q}}G^p(\vec{r}_1,\vec{r}_2,\vec{k}+\vec{q}_t,E+\hbar\omega_{\vec{q}})\end{aligned} \tag{A.73}$$

Acoustic phonon scattering in NEGF

Now, let's consider the acoustic phonon scattering (or elastic phonon scattering) in non-polar crystal system. In general, amount of phonon energy $\hbar\omega_{ph}$ is little compare to thermal energy k_BT in room temperature, $\hbar\omega_{ph} \ll k_BT$ (also, $\vec{k} \gg \vec{q}$). Then approximation on the function of Bose-Einstein statistics is

$$n_{\vec{q}} \approx \frac{1}{\hbar\omega_{\vec{q}}/k_BT+(\hbar\omega_{\vec{q}}/k_BT)^2/2+...} \approx \frac{k_BT}{\hbar\omega_{\vec{q}}} \approx n_{\vec{q}}+1 \tag{A.74}$$

First linear term of the approximation of electron-phonon deformation potential matrix element gives

$\left|M_{\vec{q}}\right|^2 = D_a{}^2 q^2$ and $\omega_{\vec{q}} = v_a q$, where v_a is speed of sound (or speed of the acoustic phonon propagation) [81]. Therefore, scattering self-energy of the acoustic phonon interaction is

$$\begin{aligned}\Sigma_{ac}^{in}(\vec{r}_1,\vec{r}_2,\vec{k},E) &\approx \sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{i\vec{q}_l\cdot(\vec{r}_1-\vec{r}_2)}\frac{k_B T}{\hbar\omega_{\vec{q}}}G^n(\vec{r}_1,\vec{r}_2,\vec{k},E) \\ &\quad+\sum_{\vec{q}_l,\vec{q}_t}\left|M_{\vec{q}}\right|^2 a_{\vec{q}}{}^2 e^{-i\vec{q}_l\cdot(\vec{r}_1-\vec{r}_2)}\frac{k_B T}{\hbar\omega_{\vec{q}}}G^n(\vec{r}_1,\vec{r}_2,\vec{k},E) \\ &= \frac{D_a{}^2 k_B T}{\rho v_a{}^2}\sum_{\vec{q}_l,\vec{q}_t}G^n(\vec{r}_1,\vec{r}_2,\vec{k},E)\delta(\vec{r}_1-\vec{r}_2)\end{aligned} \tag{A.75}$$

$$\Sigma_{ac}^{out}(\vec{r}_1,\vec{r}_2,\vec{k},E) = \frac{D_a{}^2 k_B T}{\rho v_a{}^2}\sum_{\vec{q}_l,\vec{q}_t}G^p(\vec{r}_1,\vec{r}_2,\vec{k},E)\delta(\vec{r}_1-\vec{r}_2) \tag{A.76}$$

$$D_{ac} = \frac{D_a{}^2 k_B T}{\rho v_a{}^2}\frac{1}{a_x a_y a_z} \tag{A.77}$$

D_{ac} is the coupling constant of the acoustic phonon scattering. Green's function is self-consistently determined with the scattering self-energy. Additionally, the scattering self-energy can be developed for the NEGF calculation with grid size a_x, a_y and a_z in the direction x, y and z respectively [83].

$$\Sigma_{ac}^{in}(\vec{r}_1,\vec{r}_2,\vec{k},E) = D_{ac}\frac{N_u}{V}\sum_{\vec{q}_t}G^n(\vec{r}_1,\vec{r}_2,\vec{k},E)\delta(\vec{r}_1-\vec{r}_2) \tag{A.78}$$

$$\Sigma_{ac}^{in}(\vec{r}_1,\vec{r}_1,\vec{k},E) = D_{ac}\frac{N_u N_c}{V}G^n(\vec{r}_1,\vec{r}_1,\vec{k},E) = D_{ac}\frac{1}{a_x a_y a_z}G^n(\vec{r}_1,\vec{r}_1,\vec{k},E) \tag{A.79}$$

$$\Sigma_{ac}^{out}(\vec{r}_1,\vec{r}_1,\vec{k},E) = D_{ac}\frac{1}{a_x a_y a_z}G^p(\vec{r}_1,\vec{r}_1,\vec{k},E) \tag{A.80}$$

Where, N_u is the number of grid for unconfined dimension and N_c is the number of grid for confined dimension.

A.2 NEGF approach to 1 dimensional channel MOSFET

For test the NEGF formalism, 1 dimensional channel MOSFET is investigated briefly with real space approach. In NEGF calculation, Hamiltonian of 1 dimensional Si channel is regarded as 1 dimensional chain for simplicity. In addition, acoustic phonon scattering on Si is included.

A.2.1 Self-consistent NEGF calculation with Poisson's equation

Figure A.3 shows the flow chart of self-consistent loop of NEGF and Poisson equation, carrier densities given by NEGF and electrostatic potential is evaluated by Poisson equation. In this study, self-consistent loop is performed until the carrier density is saturated.

For constructing self-consistent loop of NEGF and Poisson equation, approximation of Poisson equation for finite element method (FED) with square unit grid is demonstrated by

$$U_{n,m} = \left(\frac{U_{n+1,m} + U_{n-1,m}}{a_x^{\,2}} + \frac{U_{n,m+1} + U_{n,m-1}}{a_y^{\,2}} - \frac{q\rho_{n,m}}{\varepsilon_{n,m}} \right) \left(\frac{2}{a_x^{\,2}} + \frac{2}{a_y^{\,2}} \right)^{-1} \tag{A.81}$$

$$\rho_{x,y} = N_{a,x,y} - N_{d,x,y} + n_{x,y} - p_{x,y} \tag{A.82}$$

Indexes of n and m represent the position on grid along x and y axes, a_x and a_y are the distances between the grid points along the x and y axes, respectively.

In according to tight binding model, Bloch equation for 1 dimensional channel give the simplified energy band [79][84]

$$E\Psi_n = -t\Psi_{n-1} + (E_{c,n} + U_n + 2t)\Psi_n - t\Psi_{n+1} \tag{A.83}$$

$$t = \frac{\hbar^2}{2m^* a^2} \tag{A.84}$$

Where, t is the hopping energy to nearest neighbor, a is the grid spacing, m^* is effective mass of carrier, and $E_{c,n}$ is the conduction band energy correction at position n. 1 dimensional infinitely long periodic structure gives the energy dispersion [84]

$$E = E_c + U + 2t(1 - \cos ka) \tag{A.85}$$

In the boundary of the channel (n=1 or N), since self-energy gives the outgoing waves at boundaries as defined in the previous section (or self-energy can be evaluated by solving surface green's function

of source and drain self-consistently), Bloch equation become [79]

$$\begin{aligned} E\Psi_1 &= -t\Psi_0 + (E_{c,1} + U_1 + 2t)\Psi_1 - t\Psi_2 \\ &= -te^{ik_1 a} + (E_{c,1} + U_1 + 2t)\Psi_1 - t\Psi_2 \end{aligned} \tag{A.86}$$

$$\Psi_0 = e^{ik_1 a}\Psi_1 \tag{A.87}$$

$$\begin{aligned} E\Psi_N &= -t\Psi_{N-1} + (E_{c,N} + U_N + 2t)\Psi_N - t\Psi_{N+1} \\ &= -t\Psi_{N-1} + (E_{c,N} + U_N + 2t)\Psi_N - te^{-ik_N a} \end{aligned} \tag{A.88}$$

$$\Psi_{N+1} = e^{-ik_N a}\Psi_N \tag{A.89}$$

Therefore, self-energies are

$$\Sigma_1 = -te^{ik_1 a} \tag{A.90}$$

$$\Sigma_N = -te^{-ik_N a} \tag{A.91}$$

A.2.2 NEGF calculation for 1 dimensional channel MOSFET

Figure A.4 shows the cross-sectional schematic of 1 dimensional channel MOSFET structure for NEGF calculation, SiO_2 of 2.5 nm for gate insulator is used, and thickness of thin Si channel is 0.5 nm. n-doped Si having a impurity concentration of 10^{19} cm^{-3} is used for source and drain, the transistor channel is undoped Si, work function of gate metal and electron affinity of Si are 4.05 eV. Grid spacing along the channel is same with distance between Si atoms of 2.35 Å. Deformation potential is assumed to be 8.93 eV, and the sound velocity of Si is 90.4 m/s [81].

Figure A.5 shows the carrier density of the 1 dimensional channel MOSFET at transistor channel (distance from source contact) with drain bias of 0.5 V and the gate biases of (a) 0 V (OFF-state) and (b) 0.5 V (ON-state). Due to extremely thin thickness of Si and 1 dimensional chain model, confinement effect on source and drain is occurred even though highly doped impurity doping of 10^{19} cm^{-3}, hence the induced carrier is much lower than impurity doping.

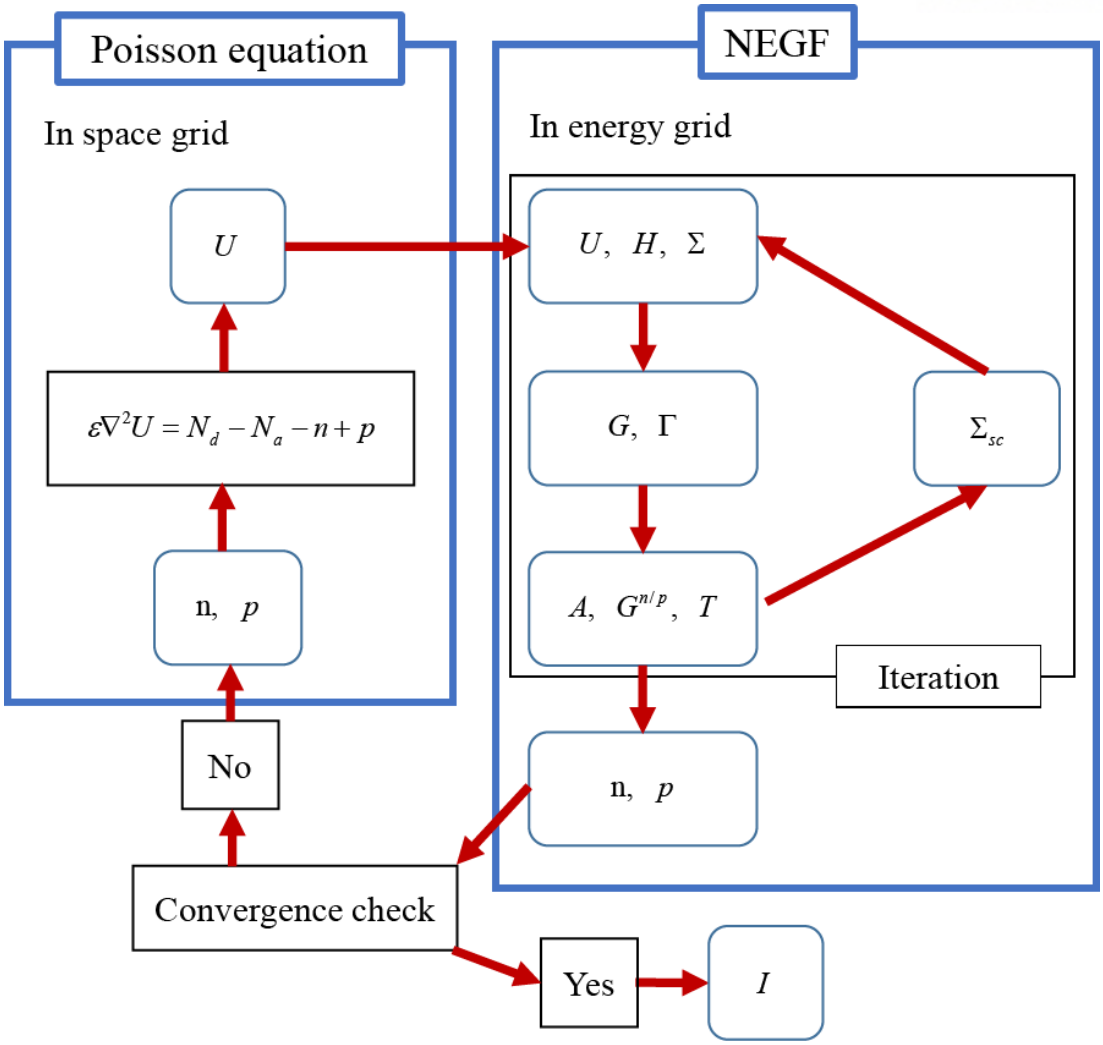

Figure A.3 Flowchart of solving NEGF and Poisson equation in self-consistently, NEGF gives the carrier density, and Poisson equation gives the electrostatic potential self-consistently.

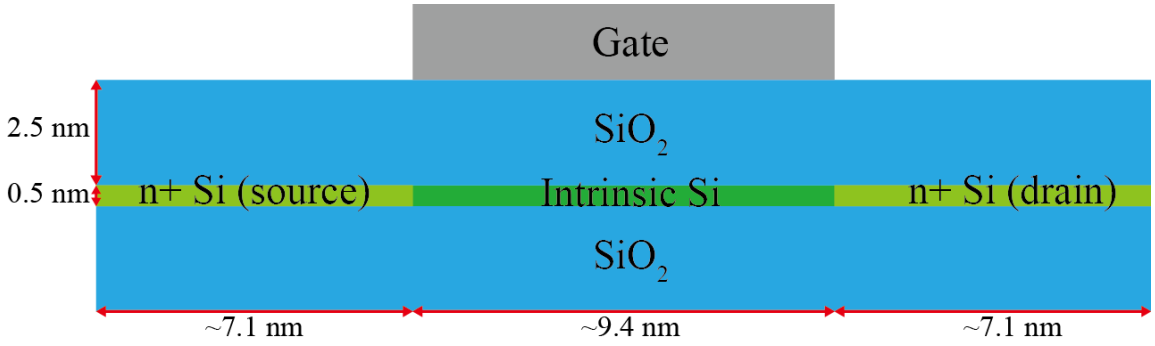

Figure A.4 Cross-sectional schematic of 1 dimensional channel MOSFET for numerical NEGF calculation, n-doped Si are used for source and drain, intrinsic Si is used for channel length of ~9.4 nm.

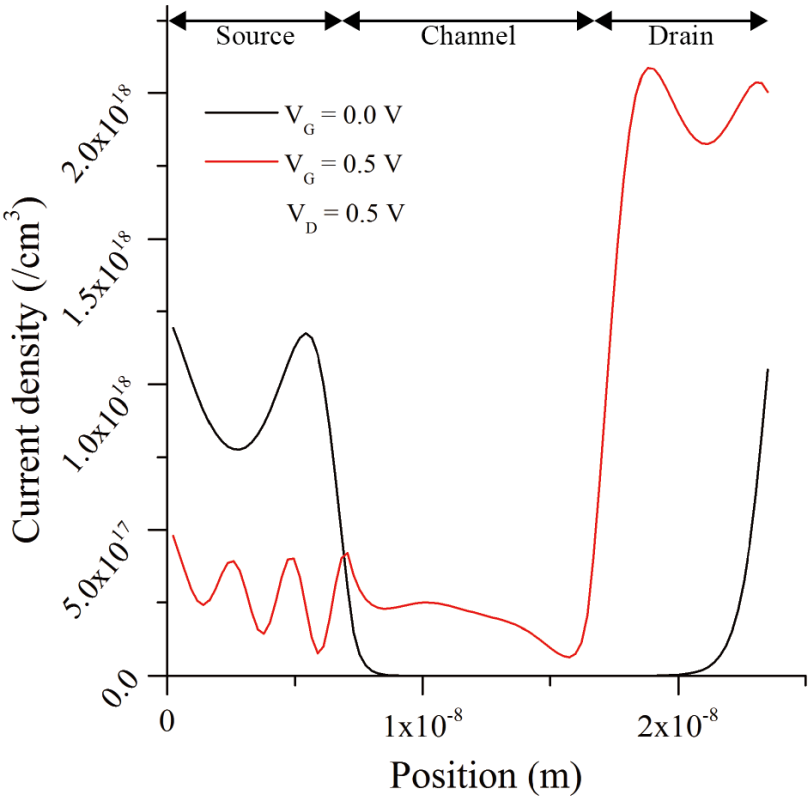

Figure A.5 Carrier density of the 1 dimensional channel MOSFET at position (distance from source contact) with the drain bias of 0.5 V and the gate biases of (a) 0 V and (b) 0.5 V.

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