Doctoral Thesis

LOW-JITTER AND LOW-SPUR RING-OSCILLATOR-BASED PHASE-LOCKED LOOPS

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Approved by

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Abstract

In recent years, ring-oscillator based clock generators have drawn a lot of attention due to the merits of high area efficiency, potentially wide tuning range, and multi-phase generation. However, the key challenge is how to suppress the poor jitter of ring oscillators. There have been many efforts to develop a ring-oscillator-based clock generator targeting very low-jitter performance. However, it remains difficult for conventional architectures to achieve both low RMS jitter and low levels of reference spurs concurrently while having a high multiplication factor. In this dissertation, a time-domain analysis is presented that provides an intuitive understanding of RMS jitter calculation of the clock generators from their phase-error correction mechanisms. Based on this analysis, we propose new designs of a ring-oscillator-based PLL that addresses the challenges of prior-art ring-based architectures.

This dissertation introduces a ring-oscillator-based PLL with the proposed fast phase-error correction (FPEC) technique, which emulates the phase-realignment mechanism of an injection-locked clock multiplier (ILCM). With the FPEC technique, the phase error of the voltage-controlled oscillator (VCO) is quickly removed, achieving ultra-low jitter. In addition, in the transfer function of the proposed architecture, an intrinsic integrator is involved since it is naturally based on a PLL topology. The proposed PLL can thus have low levels of reference spurs while maintaining high stability even for a large multiplication factor.

Furthermore, it presents another design of a digital PLL embodying the FPEC technique (or FPEC DPLL). To overcome the problem of a conventional TDC, a low-power optimally-spaced (OS) TDC capable of effectively minimizing the quantization error is presented. In the proposed FPEC DPLL, background digital controllers continuously calibrate the decision thresholds and the gain of the error correction by the loop to be optimal, thus dramatically reducing the quantization error. Since the proposed architecture is implemented in a digital fashion, the variables defining the characteristics of the loop can be easily estimated and calibrated by digital calibrators. As a result, the performances of an ultra-low jitter and the figure-of-merit can be achieved.

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1. Introduction

1.1. Motivations

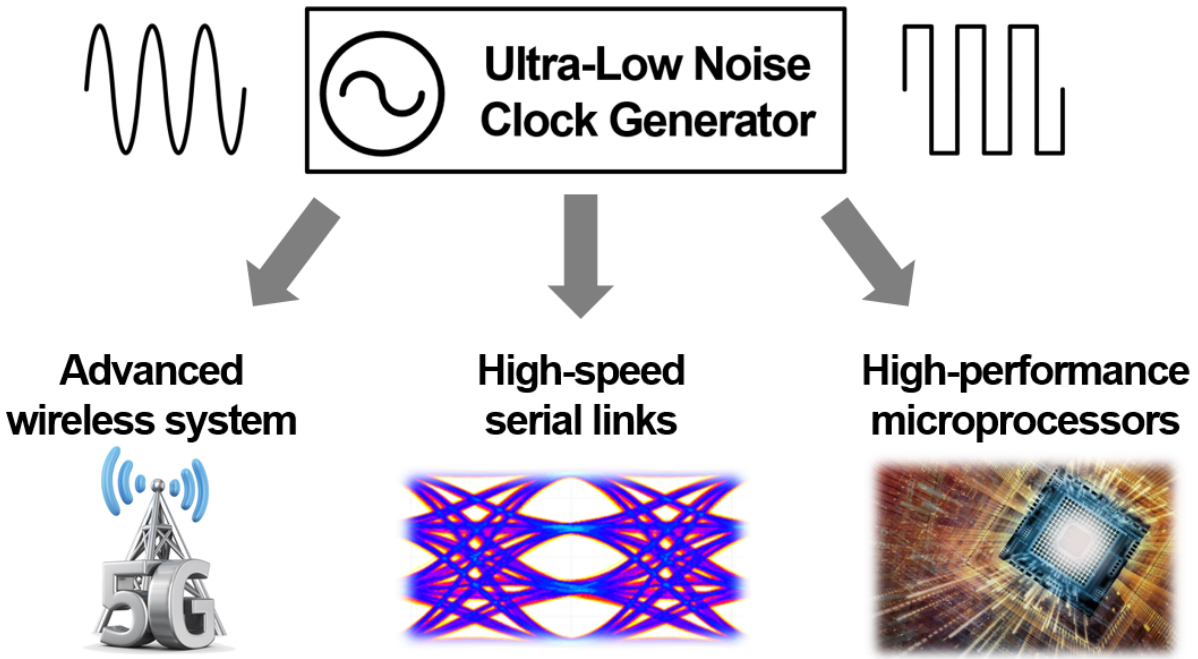
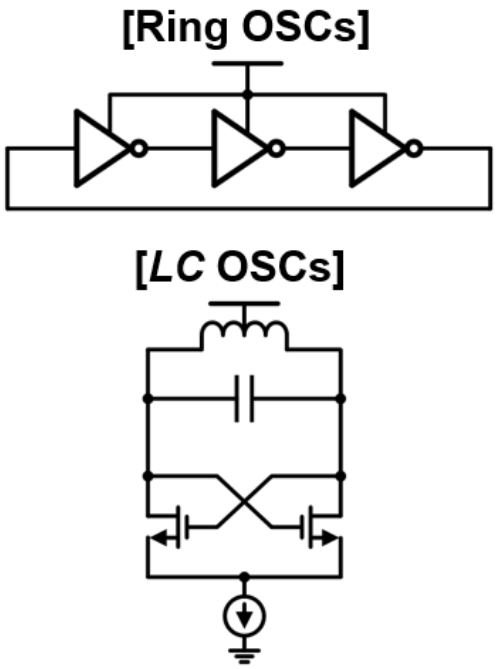


Figure 1-1. Demand on ultra-low-jitter clock generation.

Since the phase-locked loop (PLL) architecture was researched in the 1940s, various clock generation architectures have been proposed and developed. However, as high-performance applications are emerging such as advanced wireless communications, high-speed interconnections, and high-performance microprocessors (Figure 1-1) there remains strong demand for a new architecture that can provide ultra-low-jitter clock signals.

Oscillators (OSCs), key components of clock-generation systems, physically generate high-frequency signals, and they are mainly classified into two categories according to the mechanism of the frequency generation: ring OSC and *LC* OSC (Figure 1-2). A ring OSC has the following advantages over its counterpart: small area since it does not require any area-hungry inductor; a very wide frequency tuning range; a natural capability of generating multi-phases; and the low impact of frequency pulling.



	Ring	*LC*
Area	☺	☹
Tuning range	☺	☹
Freq. pulling	☺	☹
Multi phases	☺	☹
Phase noise	☹	☺

Figure 1-2. Comparison between ring OSCs and *LC* OSCs.

Nevertheless, most low-jitter clock generators have been designed with *LC* OSCs. This is primarily because the jitter (or phase noise) performance of *LC* OSCs is much superior due to their frequency selection mechanism of the *LC* tank having a high Q-factor. On the other hand, the frequency of ring OSCs is defined by the delays of delay cells, which entails an increase in thermal noise [1].

In order to effectively suppress the jitter of ring OSC while exploiting their merits, many attempts have been made to develop ring-OSC-based clock generators targeting very low-jitter performance [2]–[25], comparable to that of *LC*-OSC-based architectures. Among many efforts, an injection-locked clock multiplier (ILCM) and a switched-loop-filter (SLF) PLL are considered as two promising solutions. An ILCM can dramatically remove the ring oscillator's jitter thanks to its intrinsic phase-realignment mechanism. However, since an ILCM is based on phase correction rather than frequency correction, large reference spurs are induced and the multiplication factor, *N*, is limited. With the extended noise reduction bandwidth, SLF PLLs also can achieve low-jitter performance. In an SLF PLL, with an intrinsic integrator present in its loop transfer function and the use of an SLF, a low reference spur is also achievable. However, the limit is their jitter performance is still inferior to that of ILCMs.

1.2. Thesis organization

As described in Chapter 1.1, the two popular architectures (an ILCM and a SLF PLL) for the design of ring-OSC-based clock generators still have limitations. This dissertation discusses detailed analysis of conventional ring-OSC-based clock generators and presents new architectures addressing the design challenges of the conventional ones.

This dissertation consists of five chapters.

- Chapter 1 provides an introduction of demand on ultra-low-jitter clock generators, the merits of ring OSCs, reviews of conventional ring-oscillator, and presents the motivation of this dissertation.

- Chapter 2 details the design challenges on ring-OSC-based clock generators and analyzes the limitations of conventional architectures.

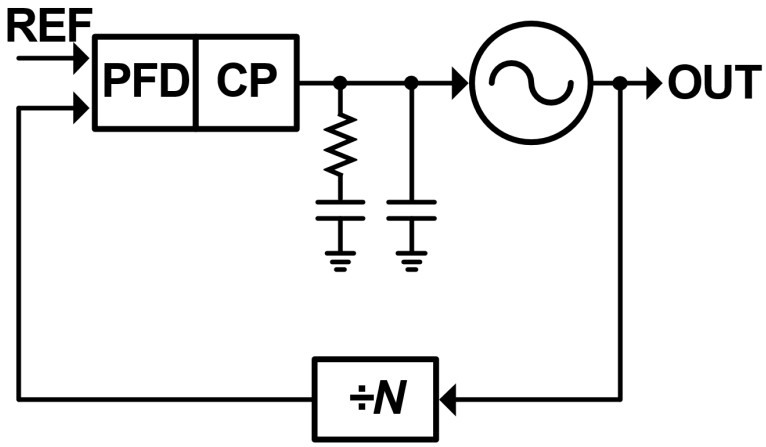
- Chapter 3 demonstrates the proposed fast-phase-error correction (FPEC) technique addressing the issues of conventional ring-OSC-based, and presents a prototype ring-OSC-based PLL using the FPEC technique that solves those challenges with the previous works.

- Chapter 4 presents a design of a digital PLL embodying the FPEC technique (or FPEC DPLL). In the proposed FPEC DPLL, a low-power optimally-spaced (OS) TDC that can effectively minimize the quantization error is presented.

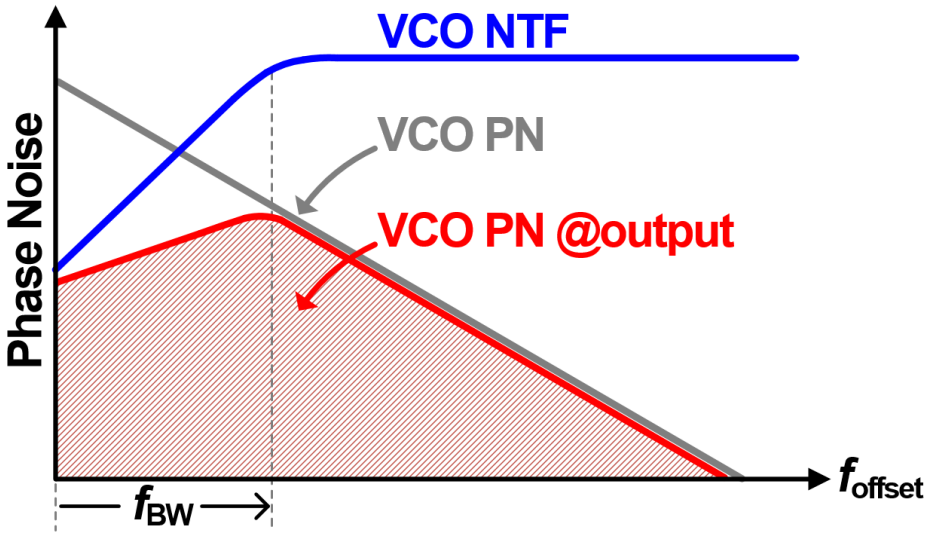
- Chapter 5 concludes the dissertation.

2. Problems and Limits of Prior Ring-Oscillator-Based Clock Generators

2.1. Traditional Charge-Pump-Based Type-II PLL



(a)



(b)

Figure 2-1. (a) A traditional charge-pump Type-II PLL (b) characteristics of VCO noise transfer function (NTF).

A traditional charge-pump Type-II PLL, shown in Figure 2-1(a), is the most popular clock-generation architecture for many practical applications due to high system stability and relatively good jitter and spur performance. Despite its popularity, Gardner's limit restricts its loop bandwidth to less than 10% of the reference frequency (f_{REF}) [26]. In general, the noise transfer function (NTF) of a voltage-controlled oscillator (VCO) has a high-pass response with respect to the loop bandwidth, as shown in Figure. 2-1 (b). To reduce the jitter of a VCO, the loop bandwidth (f_{BW}) must, therefore, be extended as much as possible. From this point of view, it is obvious that a Type-II PLL is not a desirable architecture for ring-based clock generators.

To overcome the limitation of Type-II PLLs, injection-locked clock multipliers (ILCMs) [2]–[17] and switched-loop (SLF) filter PLLs [18]–[25] are considered as two promising solutions. Since the loop bandwidth in these architectures can be largely extended without the restriction of Gardner's limit, achieving an ultra-low noise signal is feasible even when a ring VCO is used. Chapters 2.2 and Chapter 2.3 analyze these two architectures in detail.

2.2. Injection-Locked Clock Multipliers

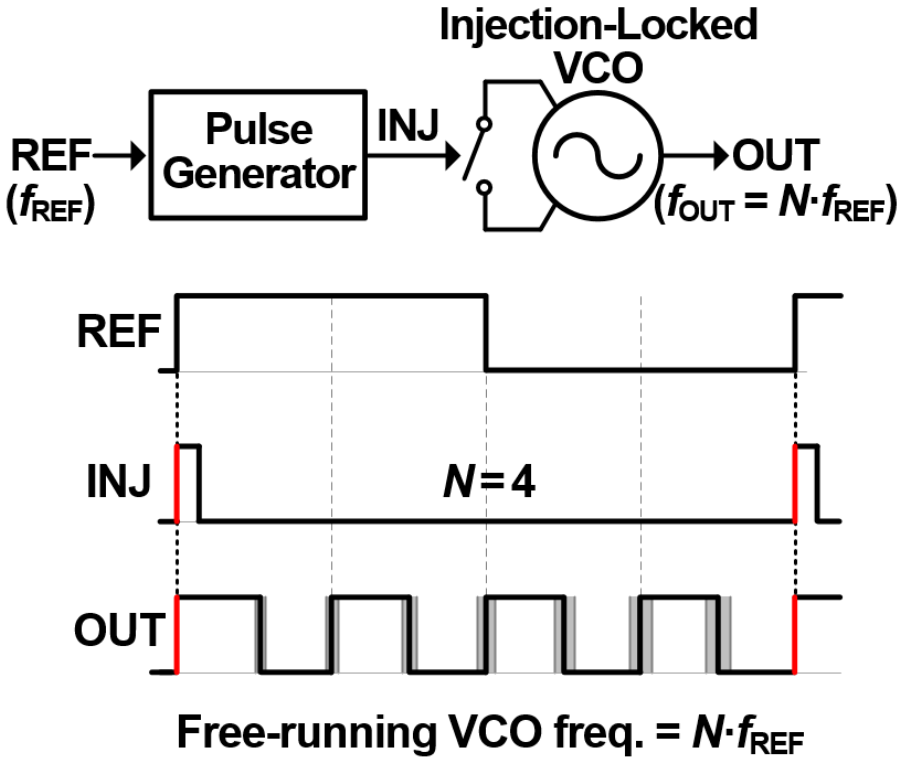


Figure 2-2. Basic block diagram of an ILCM with waveforms.

A block diagram and operating mechanism of an ILCM is shown in Figure 2-2. In an ILCM, narrow pulses generated from the clean reference clock are physically injected into the VCO. As long as the free-running VCO frequency (f_{VCO}) approximates the target one ($N \cdot f_{REF}$), it achieves a lock and its instantaneous phase variation is realigned by the injection. In this mechanism, the phase rather than the frequency of the VCO is directly corrected. Therefore, the accumulated jitter of the VCO is removed instantaneously with a very wide bandwidth of the VCO noise reduction, achieving an ultra-low jitter performance despite the use of a ring VCO.

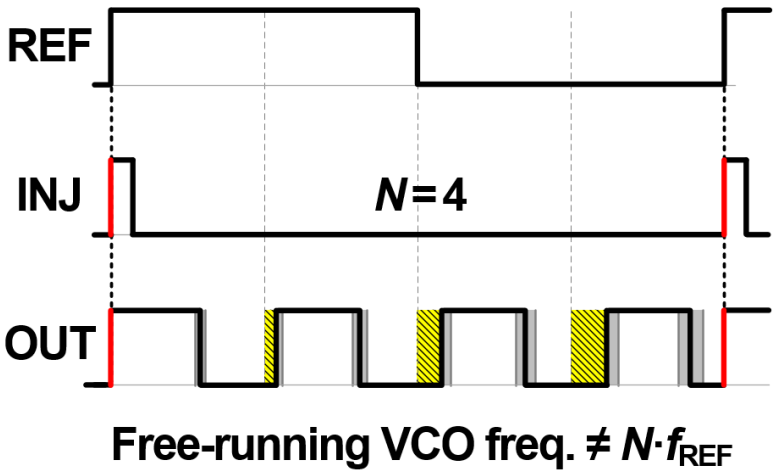


Figure 2-3. Timing diagram of an ILCM when periodic phase shifts are present due to nonzero frequency deviation.

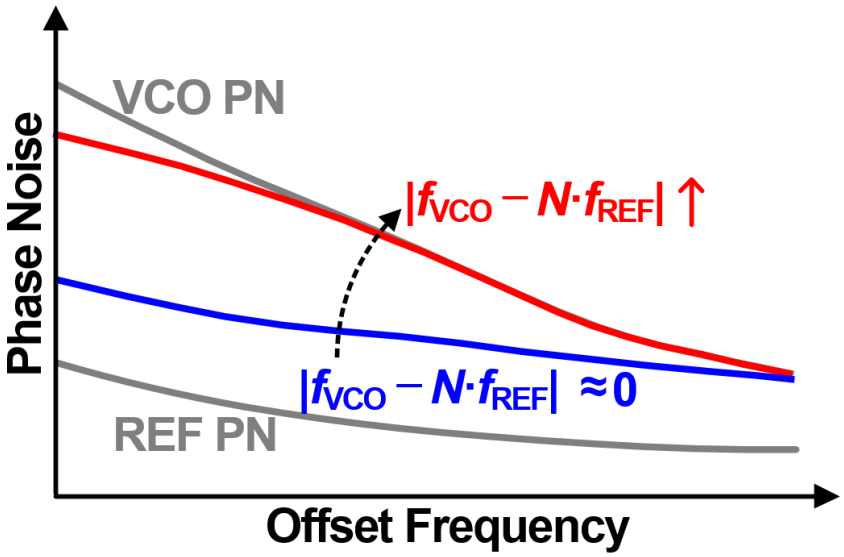


Figure 2-4. Degradation of phase noise in ILCMs due to frequency deviation.

However, the ILCM has a critical problem. Since the mechanism of the phase-error correction in an ILCM does not involve an integrator in its loop, the deviation of f_{VCO} from $N \cdot f_{REF}$ cannot be eliminated. This leads to periodic phase shifts at the frequency of f_{REF}, as shown in Figure 2-3, thereby significantly increasing the level of reference spurs at the output of an ILCM. For example, when N is 10, just 1% of the frequency deviation causes approximately –20 dBc-reference spur. Another critical problem of an ILCM is the vulnerability of noise performance against PVT variations. In other words, the aforementioned excellent noise performance is valid only when f_{VCO} is sufficiently close to $N \cdot f_{REF}$. The

noise performance is therefore degraded severely when drifts in f_{VCO} occur due to variations in process, voltage, and temperature (PVT), as shown in Figure 2-4. Even worse, it is difficult to achieve a high-multiplication factor of N in ILCMs since their system stability degrades as N increases.

2.3. Switched-Loop-Filter PLLs

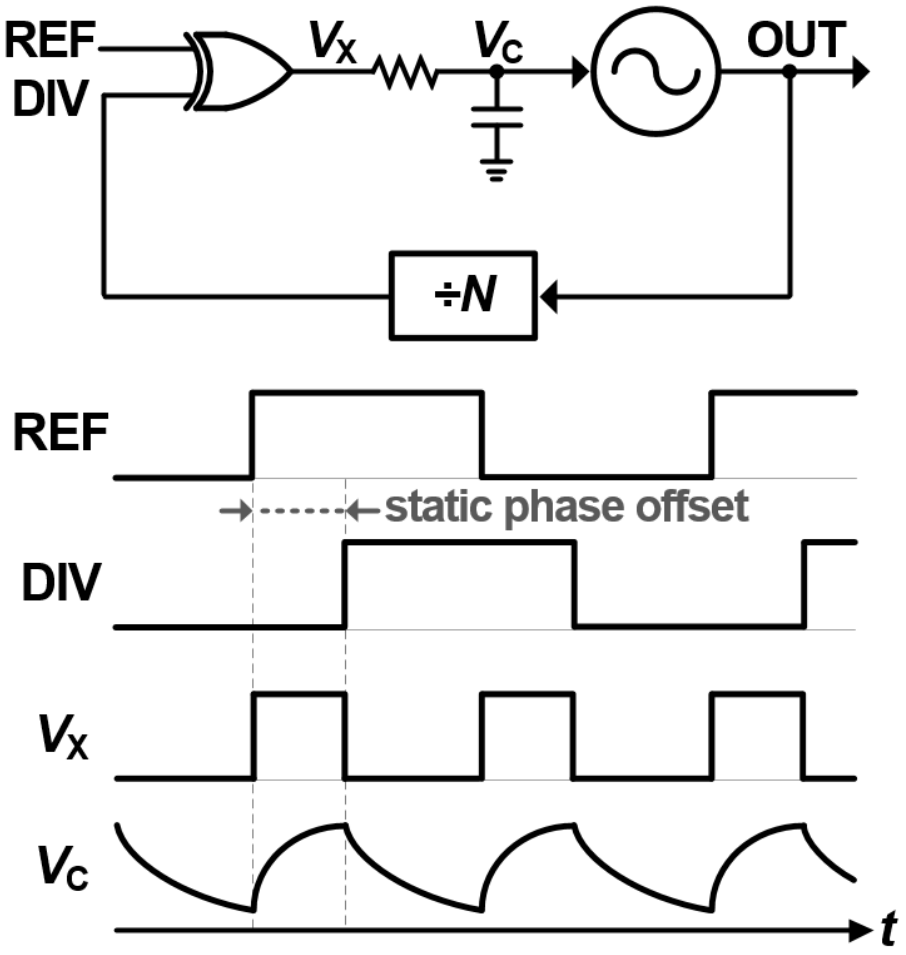


Figure 2-5. A traditional XOR-PD-based Type-I PLL

Another emerging architecture is the switched-loop-filter (SLF) PLL, which makes available the extended loop bandwidth. Before discussing the SLF-PLL architecture, it is necessary to first review a conventional Type-I PLL. Figure 2-5 shows an architecture of a traditional Type-I PLL using an XOR-type phase detector (PD). Since the Type-I PLL is not confined by Gardner's limit, the bandwidth can increase much further than a Type-II PLL. However, the use of an XOR-type PD and a continuous RC filter is supposed to cause a large fluctuation in the VCO's control voltage, V_C, which leads to a significant increase in reference spurs. To address this problem, the bandwidth must be forced to be narrow, which negates its merit of the wide bandwidth.

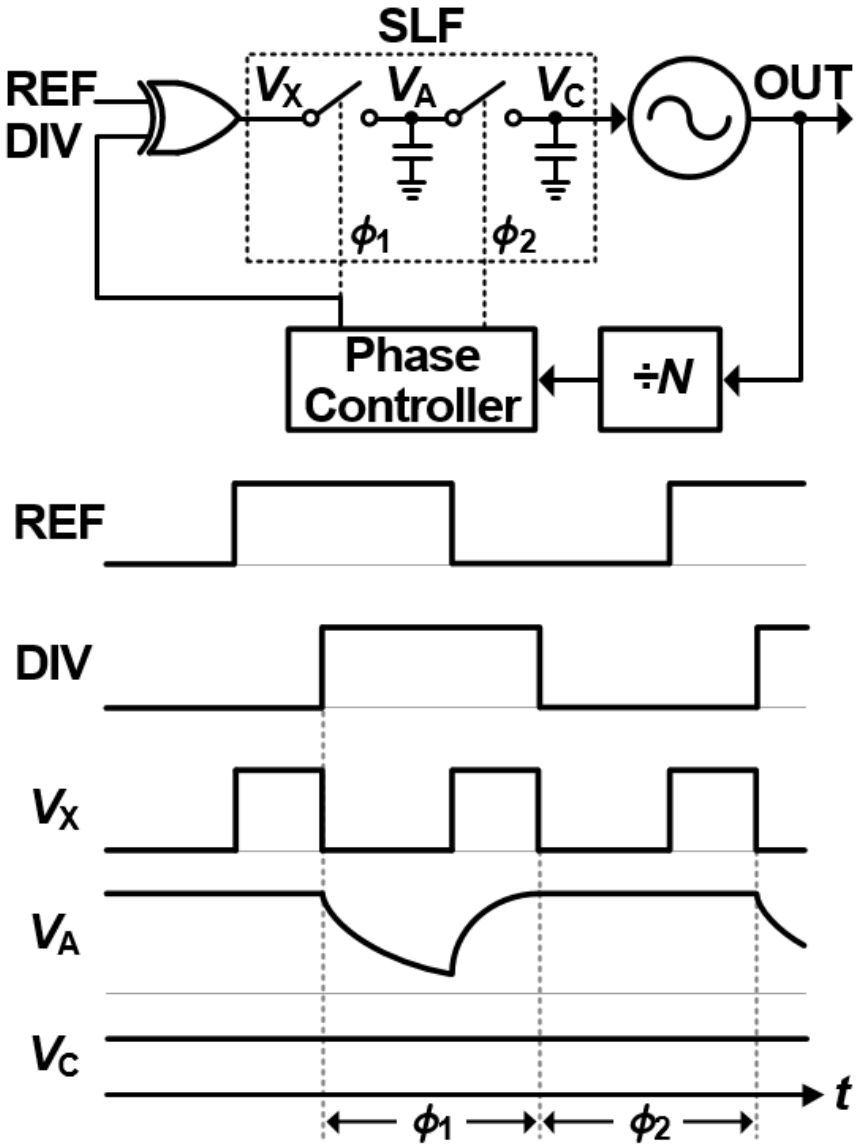


Figure 2-6. A switched-loop-filter (SLF) PLL.

To overcome this issue of a conventional Type-I PLL, an SLF PLL has been proposed [18]–[25], in which the continuous time loop filter is replaced by the SLF in order not to transfer the fluctuation of V_C to the VCO. Since the moment of capturing the phase error (i.e., ϕ_1) is separated from the moment of updating the frequency of the VCO (i.e., ϕ_2) the control voltage can be isolated from the fluctuation of the voltage of the loop filter, as shown in Figure 2-6, thus achieving a wide bandwidth of the PLL without the problem of reference spurs. Note that, unlike an ILCM, an SLF PLL includes an intrinsic

integrator in the transfer functions of its loop since it is naturally based on a PLL topology. The frequency deviation of f_{VCO} from $N \cdot f_{REF}$ can thus be corrected naturally, which frees the SLF PLL from the periodic phase shifts as in an ILCM and achieves a very low level of reference spur. In an SLF PLL, although the VCO's jitter can be effectively suppressed without the reference-spur problem, its overall jitter performance is still inferior to that of an ILCM. The crucial difference between them is their jitter reduction mechanisms, which will be detailed in Chapter 3.

3. Proposed Ring-VCO-Based Switched-Loop-Filter PLL Using a Fast Phase-Error Correction Technique

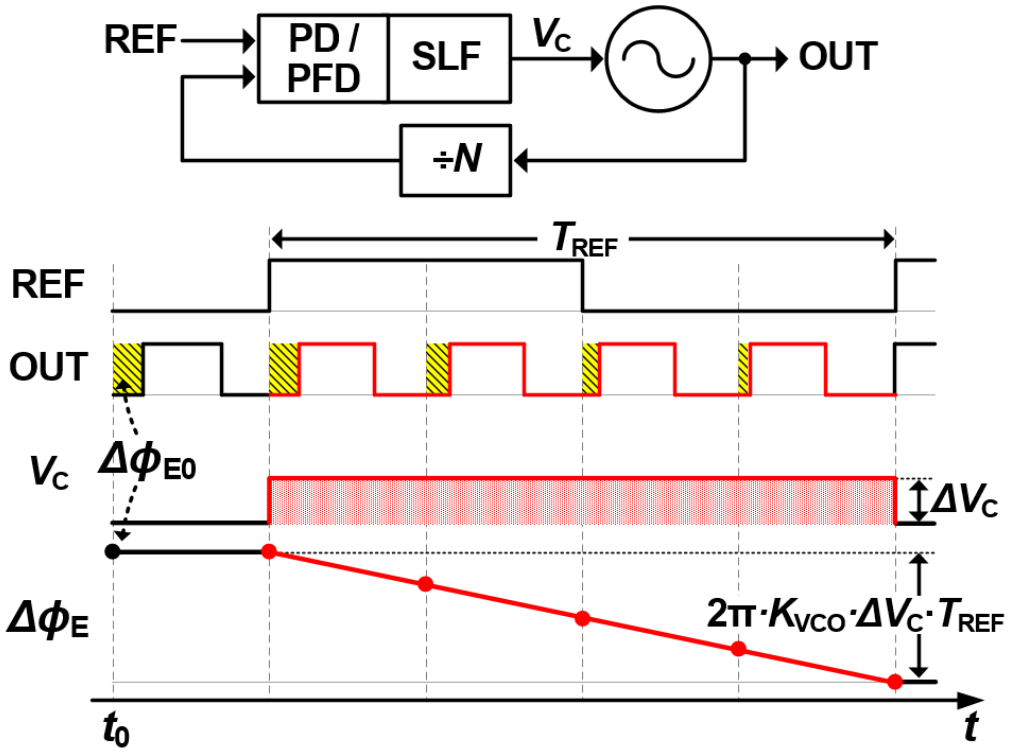
3.1. Motivations and Overview

The ILCM and SLF PLL are considered as promising solutions to the design of a ring-oscillator-based clock generator. However, as briefly described in Chapter 2, the difficulty in achieving both low RMS jitter and low levels of reference spurs while simultaneously maintaining a high multiplication factor remains a problem, which will be detailed in the following chapter.

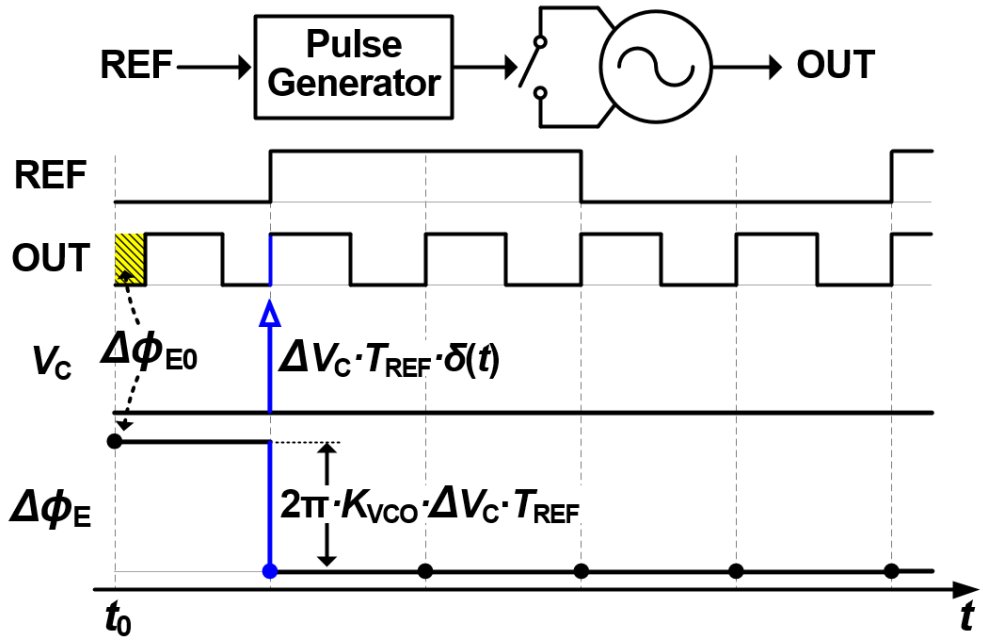
Chapter 3 presents a ring-oscillator-based SLF PLL capable of achieving good performances of RMS jitter and reference spurs despite the high multiplication factor. The key feature of this architecture is the proposed fast phase-error correction (FPEC) technique [27], [28] which is implemented in its loop filter. Emulating the phase-realignment mechanism of an ILCM, the phase error of the voltage-controlled oscillator (VCO) can be quickly removed, thus achieving ultra-low jitter. In addition, since the proposed architecture is based on PLL topology, it intrinsically has an integrator in its transfer function; the proposed PLL can thus achieve low reference spur while maintaining high stability even for a large multiplication factor. We also present a selective frequency-tuning (SFT) technique in the implementation of the VCO, which allows the proposed PLL to have much lower reference spur.

In Chapter 3.2, conventional SLF PLLs and ILCMs are analyzed in terms of the mechanisms of phase-error correction. Chapter 3.3 presents the proposed FPEC technique, and Chapter 3.4 presents its implementation. Chapter 3.5 details the operation of the FPEC technique. Measurement results are presented in Chapter 3.6, and conclusions are drawn in Chapter 3.7.

3.2. Phase-Error Correction Mechanisms of ILCMs and SLF PLLs



(a)



(b)

Figure 3-1. Processes of phase-error correction. (a) A conventional SLF PLL; (b) an ILCM.

To understand the jitter reduction difference between an SLF PLL and an ILCM, we need first to analyze the way in which each of them corrects the phase error, $\Delta\phi_E$, described by Figure 3-1(a) and (b), respectively. For the sake of simplicity, we focus on the correction of the initial phase error, $\Delta\phi_{E0}$, during a reference period, T_{REF}, and the following conditions are assumed: first, that the two architectures operate in a steady state, f_{VCO} being equal to the target frequency; second, that the effect of intrinsic noises from the building blocks is neglected, i.e.: no excess phase error occurs except $\Delta\phi_{E0}$ during T_{REF}; third, that $\Delta\phi_{E0}$ is eliminated during T_{REF}, i.e.: the realigning factor, β, [2] is 1.

Figure 3-1(a) shows the process of phase-error correction of a conventional SLF PLL. After detecting $\Delta\phi_{E0}$, the PD generates the change in V_C, ΔV_C. This changed voltage is maintained constantly over T_{REF} and causes a corresponding change in f_{VCO}. Then, due to the inherent function of the integrator in the VCO, $\Delta\phi_{E0}$ is gradually removed over the T_{REF}. During T_{REF}, the phase error is corrected by the amount of $2\pi \cdot K_{VCO} \cdot \Delta V_C \cdot T_{REF}$, and given that β is assumed to be 1 this is equivalent to $\Delta\phi_{E0}$.

In contrast to the SLF PLL, an ILCM directly realigns the VCO's phase by injecting narrow pulses into the VCO, as shown in Figure 3-1(b). Consequently, $\Delta\phi_{E0}$ is instantaneously removed at the time of injection. Since this process is performed without the use of the integrator of the VCO, there is no change in f_{VCO}. For this reason, the change in V_C is not physically involved in the phase-error correction. However, to continue with the analysis of a SLF PLL (Figure 3-1(a)), the change in V_C of an ILCM can be conceptually represented using a Dirac-delta function, $\delta(t)$, as shown in Figure 3-1(b). This assumption allows us to conceptualize the ILCM's phase-error correction as though the VCO has an integrating function and is affected by the change in control voltage. Note that the phase error is corrected by the same amount as in the case of an SLF in Figure 3-1(a), i.e: $2\pi \cdot K_{VCO} \cdot \Delta V_C \cdot T_{REF}$, by the assumption of β.

From these observations, we may now proceed to theoretically estimate the RMS jitter of each architecture. Since our objective is to compare the suppression of the VCO's jitter to the phase-error correction mechanism of an ILCM and an SLF PLL, it is sufficient to account for only the thermal noise of the VCO; the flicker noise of the VCO is thus disregarded. For a similar reason, we do not consider noise from other sources, such as the reference clock and loop building blocks. For a fair comparison of RMS jitter, we assume a VCO with the same noise profile is used in both architectures. Figures 3-2(a) and (b) depict how the RMS jitter, σ_{RMS}, is determined in an SLF PLL and an ILCM, respectively. To provide an intuitive understanding in the illustration, N is set to 8, unlike Figures 3-1(a) and (b) where N is 4. Here, $J_{OUT}(t)$ denotes the instantaneous jitter at the output that changes according to the time (see Appendix A).

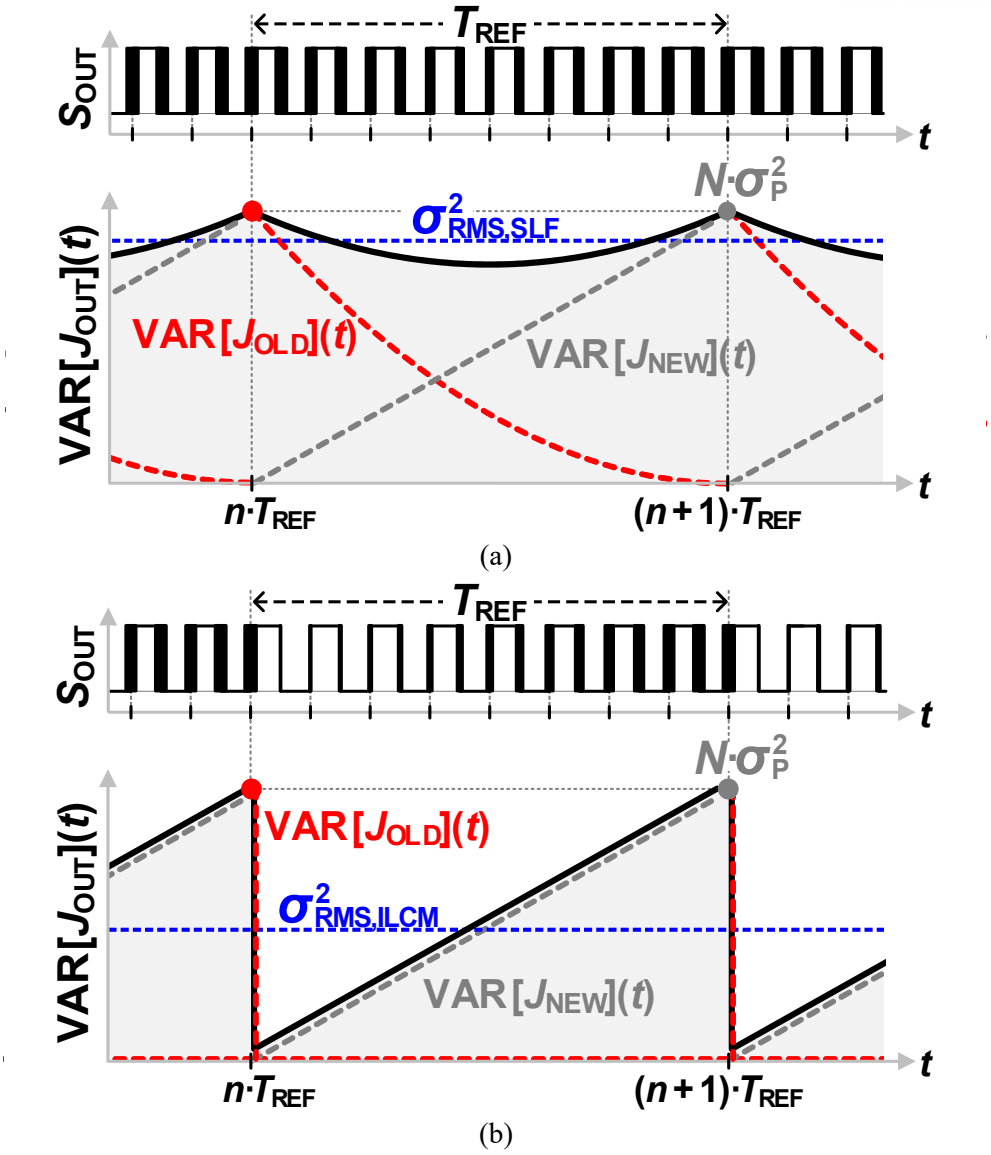


Figure 3-2. Timing diagram illustrating how σ_{RMS} is determined differently according to phase-error correction mechanisms (a) in (a) an SLF PLL; (b) an ILCM.

In Figures 3-2(a) and (b), VAR[J_{OUT}](t) represents the variance of $J_{OUT}(t)$ (black solid line), a superposition of the variances of $J_{OLD}(t)$ and $J_{NEW}(t)$, which are as follows. $J_{OLD}(t)$ is the jitter that accumulated during the previous cycle of T_{REF} by the intrinsic noise of the VCO and is corrected according to the process of the phase-error correction during the current cycle. VAR[J_{OLD}](t) (dashed red line) denotes J_{OLD}'s variance over time. $J_{NEW}(t)$ is the jitter newly occurring due to VCO noise and accumulates during the current cycle of T_{REF}. Because an identical noise profile of the VCO is assumed to be used in the two architectures, the variance of this jitter component, VAR[J_{NEW}](t) (dashed grey line) of the two architectures, increases linearly and reaches the same value of $N{\cdot}\sigma^2_P$ at the end of the

current T_{REF} [29]–[31], where σ_P denotes the period jitter of the free-running VCO. Then, since VAR[J_{NEW}](t) is the same in the two architectures, the difference in VAR[J_{OUT}](t) of an SLF PLL and an ILCM comes from VAR[J_{OLD}](t). In an SLF PLL, $\Delta\phi_E$ decreases linearly over time, as described in Figure 3-1(a). Thus, the VAR[J_{OLD}](t) of an SLF PLL at the n-th reference period (i.e.: $n \cdot T_{REF} \leq t < (n + 1) \cdot T_{REF}$) corresponds to $N \cdot \sigma^2_P \cdot (1 - (t - n \cdot T_{REF})/T_{REF})^2$, as shown in Figure 3-2(a). In contrast, in an ILCM, $\Delta\phi_E$ is instantaneously eliminated at the beginning of a T_{REF}, as shown in Figure 3-1 (b); thus, no $J_{OLD}(t)$ remains during the current T_{REF}, as shown in Figure 3-2 (b). Due to the difference in VAR[J_{NEW}](t), the area under VAR[J_{OUT}](t) is much smaller in an ILCM than an SLF PLL. Here, we can quantify the RMS jitter, σ_{RMS}, as follows:

$$\sigma_{RMS} = \sqrt{\frac{1}{T_{REF}} \cdot \int_0^{T_{REF}} VAR[J_{OUT}](t)dt} \tag{3.1}$$

As shown in Figures 3-2(a) and (b), an ILCM can achieve a much lower σ_{RMS} than an SLF PLL.

3.3. Concept of the Proposed Fast Phase-Error-Correction (FPEC) Technique

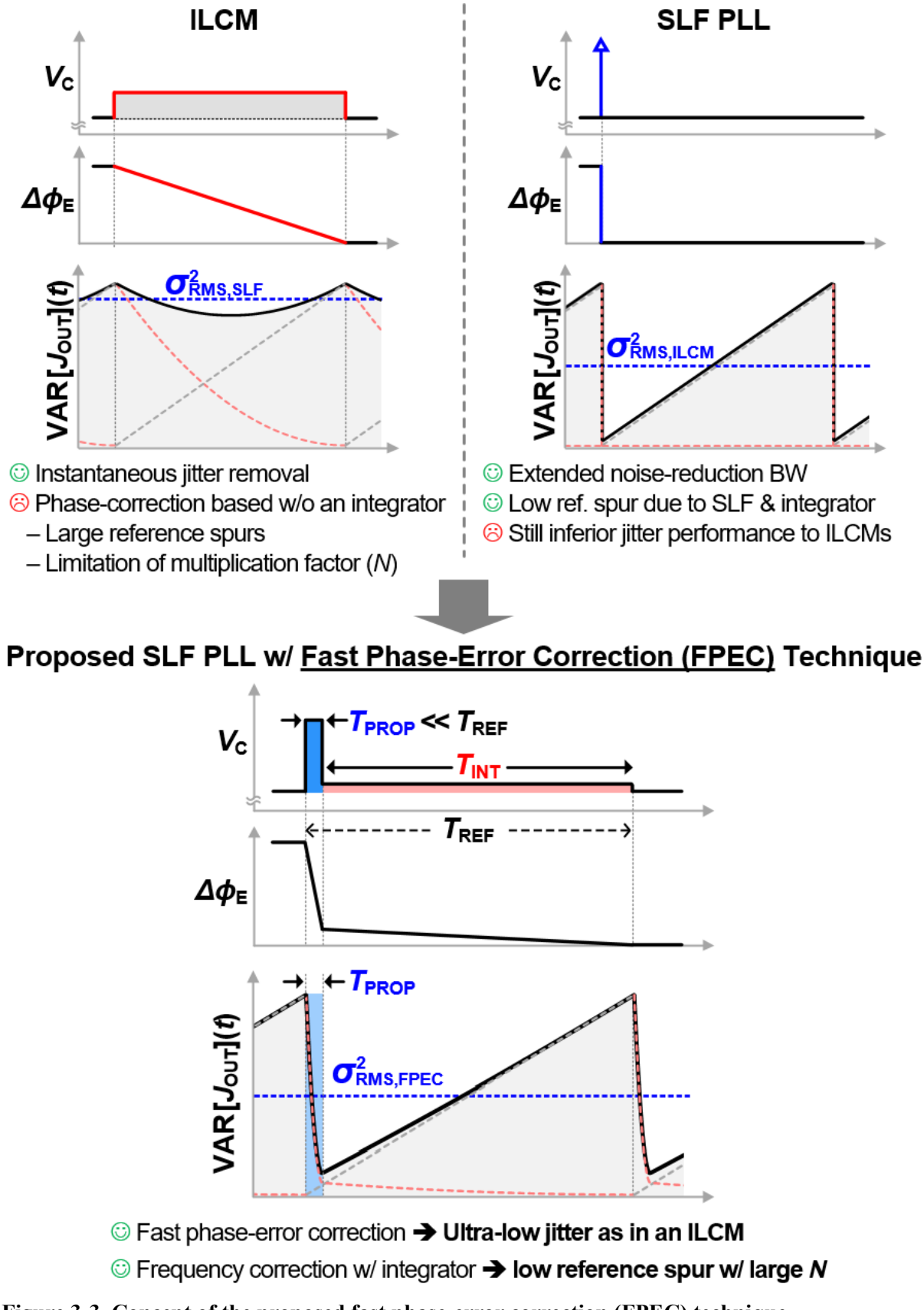


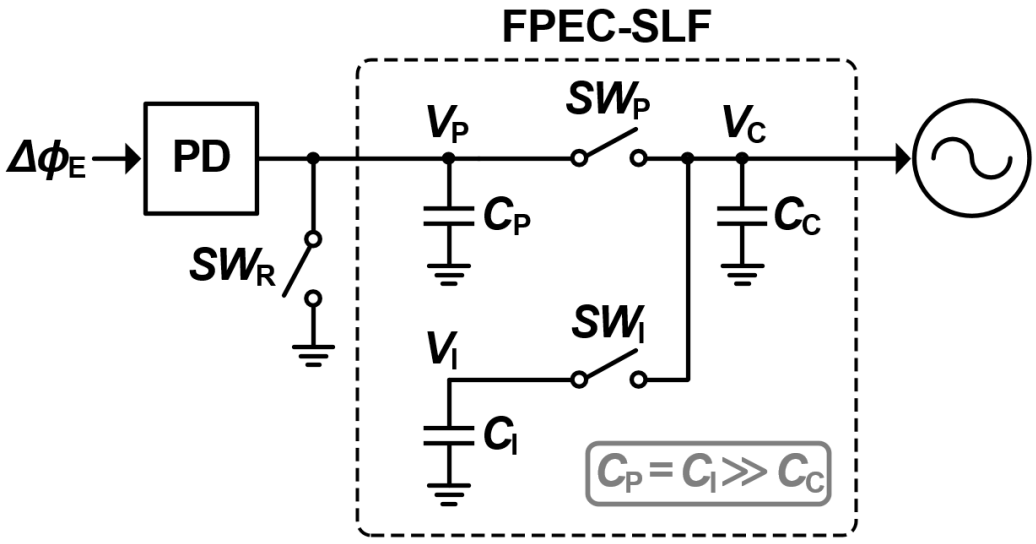
Figure 3-3. Concept of the proposed fast phase-error correction (FPEC) technique.

In Chapter 3.2, we saw that the cause of low-jitter performance in the ILCM is fast phase-error correction by the instantaneous phase-realignment mechanism. Based on this observation, we propose an SLF PLL with a fast phase-error correction (FPEC) technique that emulates the phase-realignment mechanism of an ILCM, as shown in Figure 3-3 [27], [28]. In the proposed FPEC technique, the speed of phase-error correction is intended to be increased by boosting the magnitude of ΔV_C in a short time. As shown in Figure 3-3, the FPEC process is divided into two phases: 1) the proportional period, T_{PROP}; and 2) the integral period, T_{INT}. During the short period of T_{PROP}, the loop gain remains very high so that the magnitude of change in V_C becomes large like an impulse to rapidly remove most of the detected phase error. If the duration of T_{PROP} with a high loop gain is designed to be too large the phase error could be overcorrected, thereby degrading loop stability and jitter performance. To avoid this overcorrection, the loop gain is switched to be small during the long period of T_{INT} so that the phase error remainder is slowly removed while maintaining loop stability. Hence, the proposed SLF PLL with the FPEC technique can achieve ultra-low jitter without the stability issue. Note that V_C's shape of the conventional charge pump-based Type-II PLL resembles that of the proposed SLF PLL in Figure 3-3. However, it is very difficult for the conventional charge pump-based Type-II PLL to suppress the VCO's jitter as much as the proposed SLF PLL can due to a stringent tradeoff between the reference spur and jitter concerning the loop bandwidth [32]. In other words, a wide loop bandwidth, which is desirable to reduce jitter, causes a large reference spurs in the conventional charge pump-based Type-II PLL.

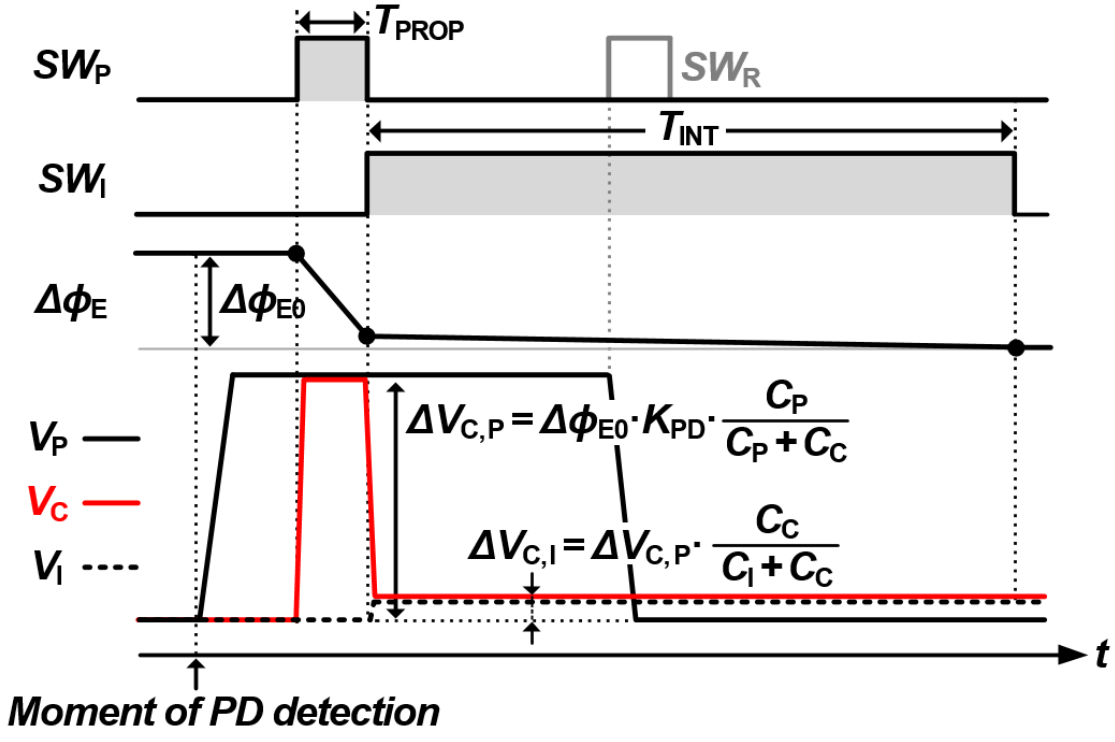
One might argue that the FPEC technique could result the reference spur problem since the process of error correction resembles that of an ILCM. As mentioned in Chapter 2.2, the reason behind a large reference spur in an ILCM is due to the absence of an integrator; the absence of an integrator to eliminate the frequency deviation of f_{VCO} occasions periodic phase shifts at the VCO's output, resulting in large reference spurs. Unlike an ILCM, the proposed architecture has an integrator of the VCO in the transfer function, so the frequency deviation of f_{VCO} can be completely removed. Since the phase error due to any drifts in f_{VCO} remains zero for N cycles of the VCO signal, the proposed SLF PLL can achieve a low reference spur, despite a large value of N.

3.4. Implementation of the SLF PLL using the FPEC Technique

3.4.1. Switched-loop filter (SLF) Implementing the FPEC Technique



(a)



(b)

Figure 3-4. (a) Conceptual diagram of the proposed SLF with the FPEC technique; (b) operational principle of the FPEC SLF.

Figures 3-4(a) and (b) show a conceptual diagram and operational principle of the proposed SLF with the FPEC. Note that Figure 3-4(b) shows the initial state of the operation, not in a steady state. The key functional components of the FPEC-SLF are three capacitors (C_P, C_I, and C_C) and three switches (SW_R, SW_P, and SW_I). The capacitances of C_P and C_I are the same, while that of C_C is much smaller than the other two capacitors. According to the signal-controlling switches, the three capacitors are connected with or disconnected from each other.

The detailed operation of the FPEC-SLF is as follows: first, before starting the phase-error correction, all three switches are open; then, at the moment of PD detection, C_P is charged with the corresponding amount of charges of $\Delta\phi_{E0}$. Since the gain of the PD, K_{PD}, is designed very high, V_P exhibits a large change even for a small phase error. During T_{PROP}, where SW_P and SW_I are turned on and off, respectively, V_P is connected to V_C. Since C_C is much smaller than C_P, V_C instantaneously increases almost up to the value of V_P. In the meantime, $\Delta\phi_E$ rapidly drops. Calculating the change of V_C in T_{PROP}, i.e.: $\Delta V_{C,P}$, associated with loop parameters, this operation can be represented as:

$$\Delta V_{C,P} = \Delta\phi_{E0} \cdot K_{PD} \cdot \frac{C_P}{C_P + C_C}. \tag{3.2}$$

During T_{INT}, where SW_P and SW_I are turned off and on, respectively, V_C connects with from V_P to V_I. In this phase, the charge on C_I that holds the frequency information of the VCO is updated by the charge from C_C having the new information. Since C_I is significantly greater than C_C, the loop gain during T_{INT} becomes very small, which ensures the stable operation of the loop. Due to charge sharing between C_C and C_I during T_{INT}, V_C experiences a change by the amount of $\Delta V_{C,P} \cdot C_P/(C_I + C_C)$ in the opposite direction of the change of $\Delta V_{C,P}$. Then, the net change of V_C in T_{INT} with respect to its initial value, $\Delta V_{C,I}$, can be calculated as:

$$\Delta V_{C,I} = \Delta V_{C,P} \cdot \frac{C_C}{C_I + C_C}. \tag{3.3}$$

In the middle of T_{INT}, V_P is initialized by turning on SW_R to prepare the next phase-error-correction cycle. Associating (3.2) and (3.3) with loop parameters, we can represent the amount of the phase-error correction, $\Delta\phi_{CORR}$, as:

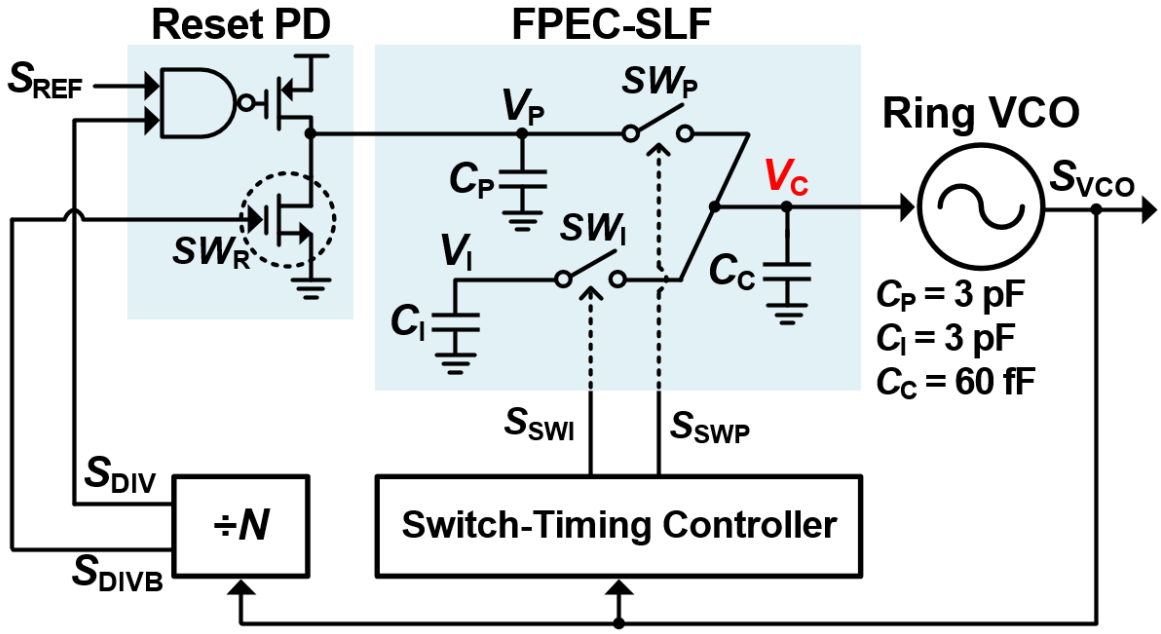
$$\begin{aligned} \Delta\phi_{CORR} &= 2\pi \cdot K_{VCO} \cdot \int_0^{T_{REF}} \Delta V_C(t) \cdot dt \\ &= 2\pi \cdot K_{VCO} \cdot (\Delta V_{C,P} \cdot T_{PROP} + \Delta V_{C,I} \cdot T_{INT}). \end{aligned} \tag{3.3}$$

Then, β can be obtained as:

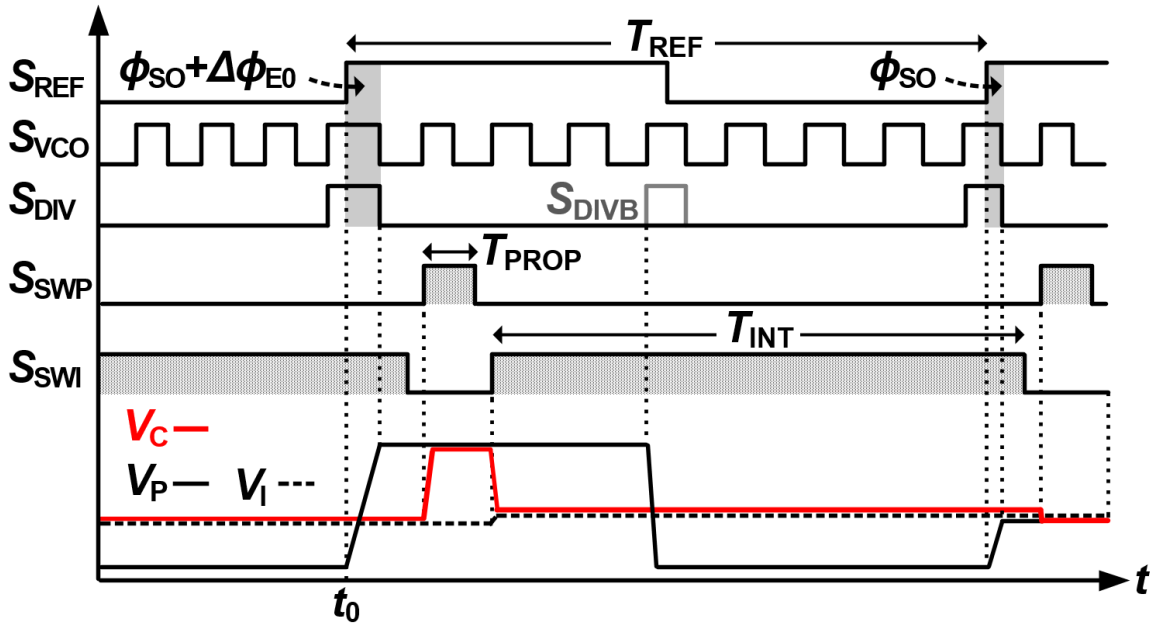
$$\beta = \frac{\Delta\phi_{\mathrm{CORR}}}{\Delta\phi_{\mathrm{E0}}} = 2\pi \cdot K_{\mathrm{VCO}} \cdot K_{\mathrm{PD}} \cdot \frac{C_{\mathrm{P}}}{C_{\mathrm{P}} + C_{\mathrm{C}}} \cdot T_{\mathrm{PROP}} \cdot \left(1 + \frac{C_{\mathrm{C}}}{C_{\mathrm{I}} + C_{\mathrm{C}}} \cdot \frac{T_{\mathrm{INT}}}{T_{\mathrm{PROP}}}\right), \tag{3.4}$$

where the units of K_{PD} and K_{VCO} are [V/rad] and [Hz/V], respectively (1 rad here is $T_{\mathrm{VCO}}/2\pi$, where T_{VCO} is $1/f_{\mathrm{VCO}}$). To achieve the minimum RMS jitter, a value of β close to 1 is desirable. By doing so, the detected phase error can be almost completely corrected during the current cycle of T_{REF}, so that it is not transferred to the next T_{REF}. In the following chapter, we will discuss how these parameters were designed.

3.4.2. Overall Architecture and Operation of the SLF PLL with the FPEC Technique



(a)



(b)

Figure 3-5. (a) Overall architecture of the proposed SLF PLL with the FPEC technique, (b) timing diagram.

Figure 3-5(a) shows the overall architecture of the proposed SLF PLL with the FPEC technique, which consists of the reset PD (R-PD), the FPEC-SLF, the switch-timing controller, a ring VCO, and a frequency divider. In the FPEC-SLF, C_P, and C_I were designed to 3 pF, and C_C to 60 fF. The parameters by which these components were selected will be discussed in Chapter 3.5. Using the output of the ring VCO, the switch-timing controller generates the switching signals, S_{SWP} and S_{SWI}, which dynamically control the switches of SW_P and SW_I, to implement the FPEC operation. To minimize leakage current flowing through the gate, SW_P and SW_I are designed using thick-oxide NMOS transistors. The switch initializing the charges in C_P (SW_R in Figure 3-4(a)), implemented using an NMOS transistor in the R-PD, is controlled by S_{DIVB}. The output signal of the PLL has a frequency of approximately 3 GHz from 47-MHz reference clock (the multiplication factor of N is 64).

Figure 3-5 (b) shows a steady-state timing diagram of the proposed PLL. At $t = t_0$, the R-PD detects the phase error of $\phi_{SO}+\Delta\phi_{E0,}$ where ϕ_{SO} and $\Delta\phi_{E0}$ respectively are the static offset of the loop and the initial phase error to be corrected. As can be seen in the configuration of the FPEC-SLF, this proposed PLL is based on a Type-I topology, so it has a finite ϕ_{SO} in steady state. During T_{PROP}, SW_P is enabled by S_{SWP} and a large change in V_C occurs, which rapidly reduces $\Delta\phi_{E0}$. In the subsequent period of T_{INT}, SW_I is closed by S_{SWI}, which makes C_C and C_I share charges. During this period, the remaining part of $\Delta\phi_{E0}$ is removed slowly, while f_{VCO} is adjusted.

To lower the RMS jitter, a smaller value of T_{PROP} is desirable since it makes the error-correction process of the proposed PLL approximate that of an ILCM. To estimate a theoretical value of RMS jitter with respect to T_{PROP}/T_{REF}, behavioral simulations using Simulink® were performed. For simplicity in

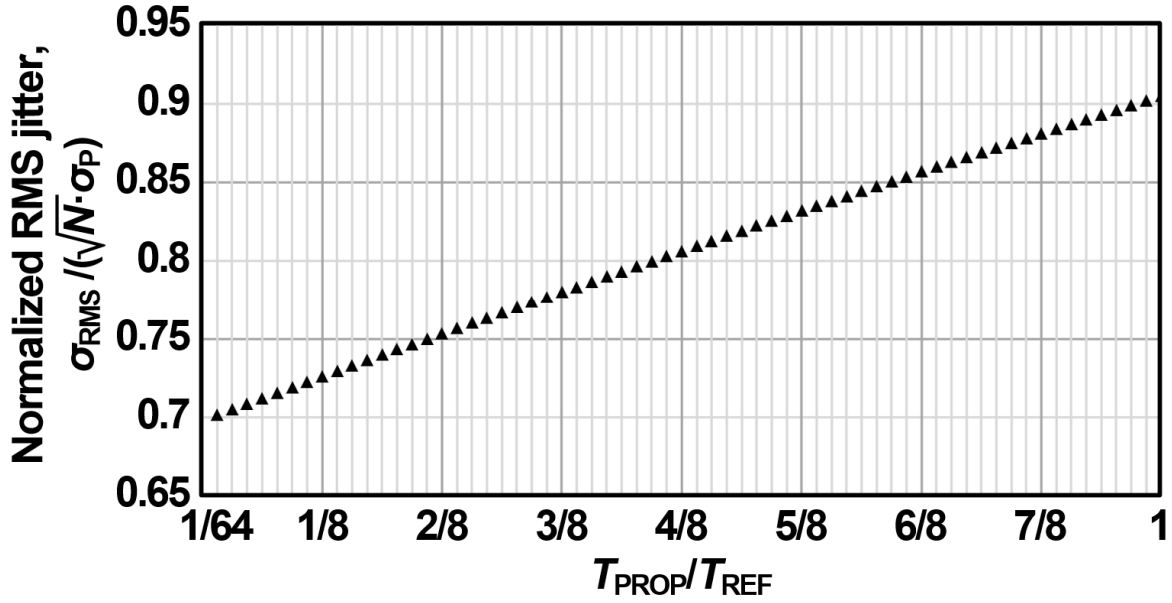


Figure 3-6. Normalized RMS jitter in accordance with T_{PROP}/T_{REF}.

analysis, we set the simulation environment such that β is 1 and the phase-error correction is performed only during T_{PROP}. As shown in Figure 3-6, the RMS jitter normalized to $\sqrt{N}\sigma_P$, $\sigma_{RMS}/(\sqrt{N}\sigma_P)$, decreases in proportion to T_{PROP}/T_{REF}. However, if T_{PROP}/T_{REF} is minimized, the PD gain, K_{PD}, should be significantly increased to meet β of one in the shorter duration of T_{PROP}. In such a large K_{PD}, the PD operates like a bang-bang PD, which narrows the capture range of the PLL. Considering this tradeoff, we set T_{PROP}/T_{REF} to 1/8. In this work, in order to set β close to 1, the values of K_{PD} and K_{VCO} were set to be approximately 0.4 V/rad (or 7.6 GV/s) and 150 MHz/V.

In the FPEC-SLF, clock feedthrough perturbing V_C occurs as SW_P and SW_I toggle. In this case, if V_C controls all delay cells at once, as shown in Figure 3-7, the perturbation of V_C coincides with one or more transition edges of the outputs of multiple delay cells. This could cause a huge fluctuation of f_{VCO}, thereby significantly increasing reference spurs. This situation is described by the timing diagram of Figure 3-7, where the falling edges of S_{D1} and S_{D3} are affected by transitions of S_{SWP} and S_{SWI}. To resolve this issue, we also present a selective frequency-tuning (SFT) ring VCO, as shown in Figure 3-8. The SFT VCO is composed of five-stage inverter-based delay cells, D_0 – D_4, where only D_4 is controlled using an NMOS transistor, M_C. The two-cascaded NMOS switches, M_1 and M_3, which are controlled

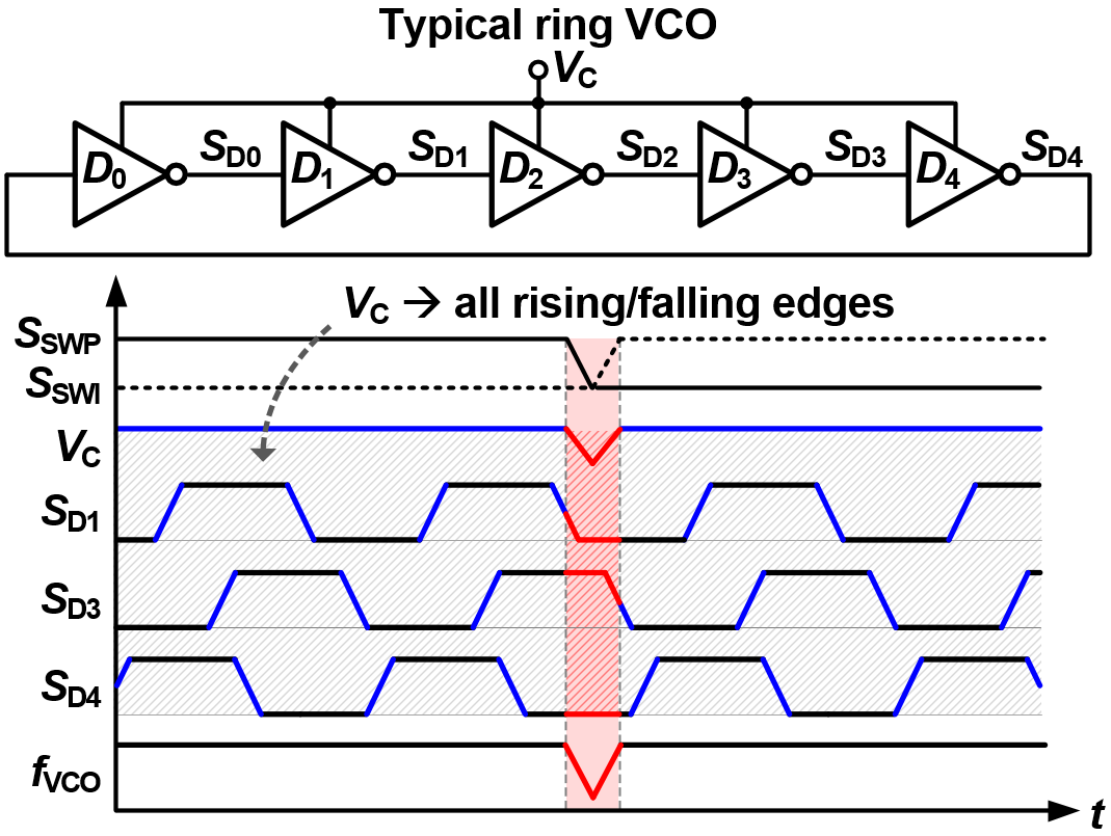


Figure 3-7. A typical ring VCO.

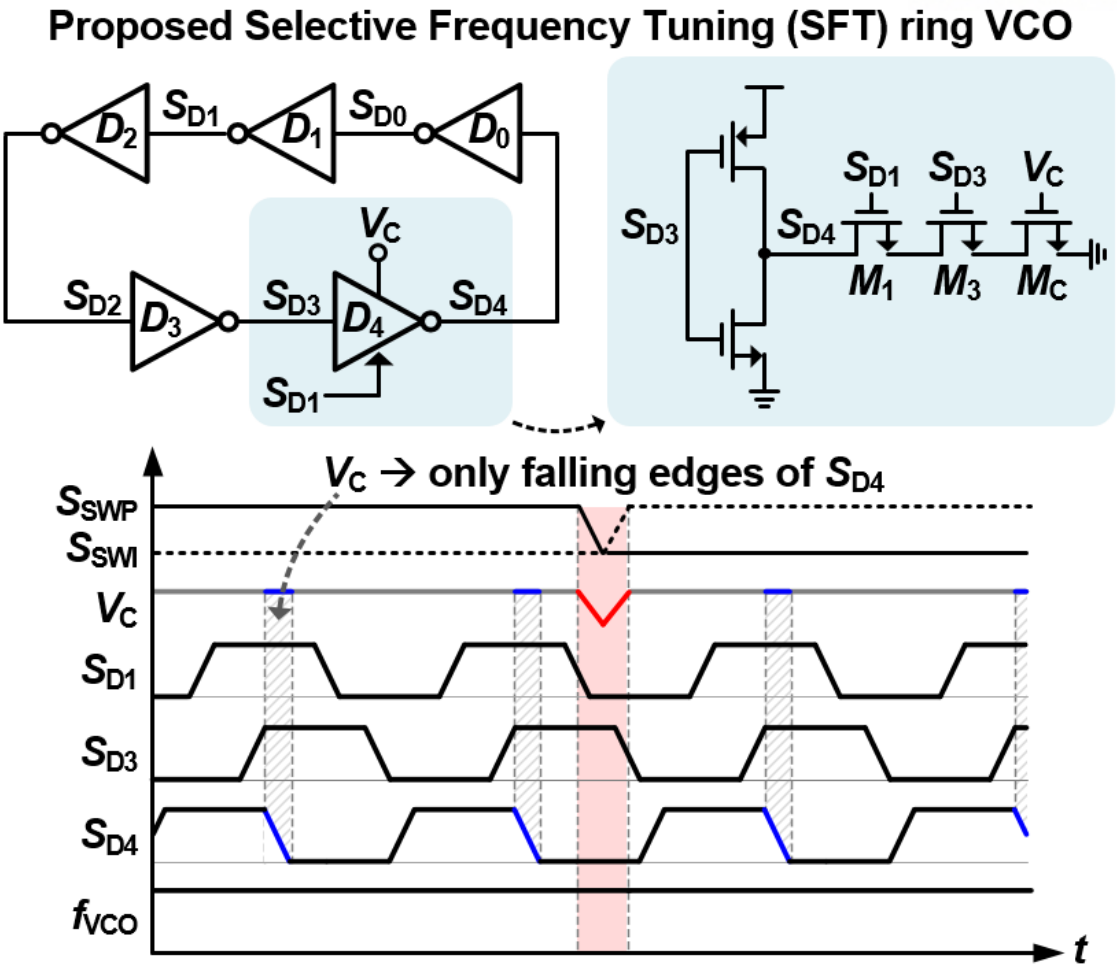


Figure 3-8. Proposed selective frequency-tuning (SFT) ring VCO.

by S_{D1} and S_{D3}, respectively, are placed before M_C. In this implementation, among the transition edges of the delay cells, only the falling ones of S_{D4} are selectively affected by V_C. Note that V_C is constant at those moments, which ensures all the transition edges of the delay cells to be isolated from the perturbations of V_C. Since the moments V_C affecting the falling edges of S_{D4} occur at the period of the VCO, the SFT technique of the proposed VCO causes no additional spurs. Compared to the topology of a typical VCO, the number of delay cells controlled by V_C is small, so K_{VCO} is also smaller (150 MHz/V). Nevertheless, the SFT technique is useful for minimizing the level of reference spur.

3.5. Analysis on the Proposed FPEC Technique

3.5.1. Effect of Noise Reduction According to FPEC Strength and Design Considerations

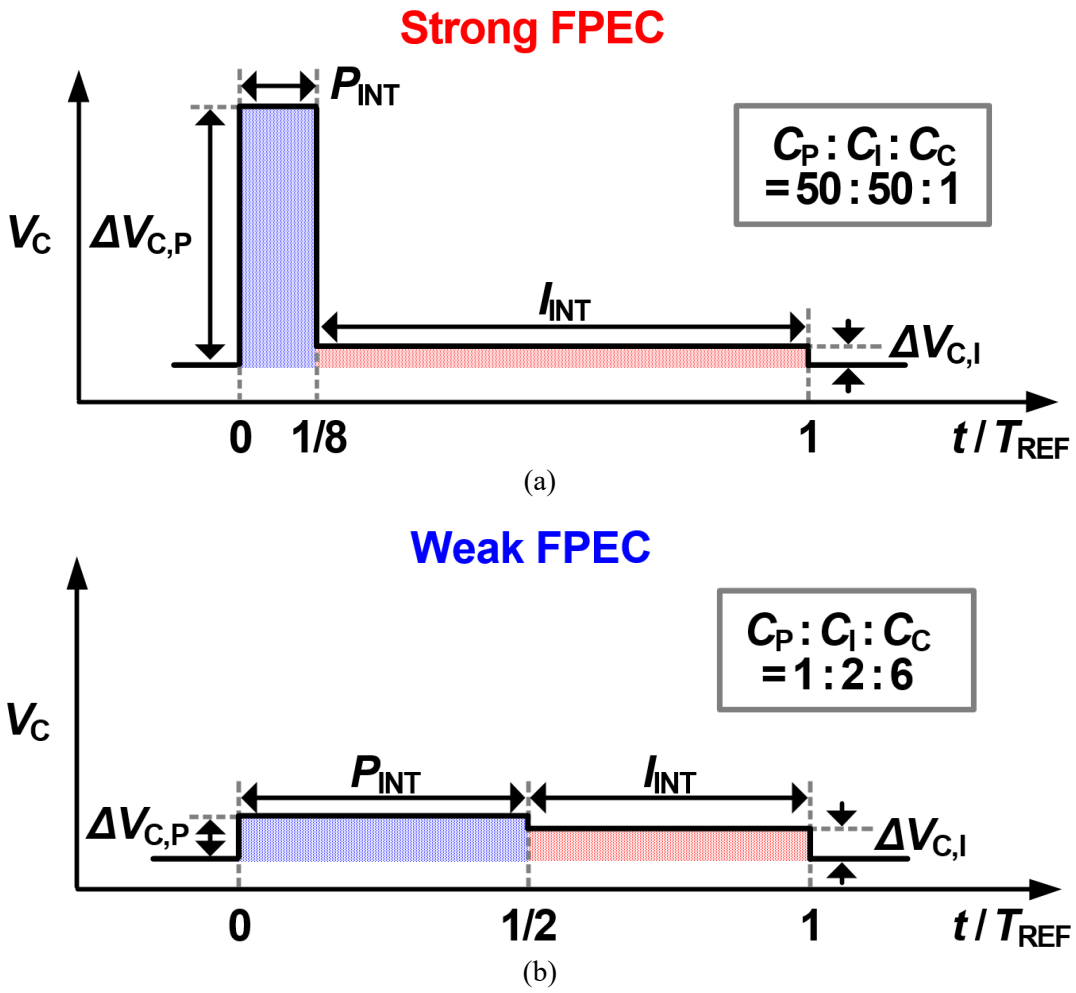


Figure 3-9. Phase noises of the FPEC DPLL in case (a) FPEC is strong; (b) weaker FPEC.

To further investigate the effects of noise reduction of the proposed FPEC technique, we performed simulations by changing the strength of the FPEC, described by Figure 3-9(a). The ratio of C_P : C_I : C_C is 50 : 50 : 1, and the ratio of T_{PROP} : T_{INT} is 1 : 7, which yields a gain ratio of T_{PROP} to T_{INT} of 1 to 7. Figure 3-9(b) describes a case in which the strength of an FPEC is far weaker than that of Figure 3-9(a). The ratio of C_P : C_I : C_C is 1 : 2 : 6 and that of T_{PROP} : T_{INT} is 1 : 1, which yields a gain ratio of T_{PROP} to T_{INT} of 4 to 3. In this case, V_C has a nearly constant shape over T_{REF}, which makes the process of phase-error correction similar to that of a conventional SLF PLL. The value of β is set to be the same in Figures 3-9(a) and (b), so the total sum of the areas of T_{PROP} and T_{INT} is the same in both cases.

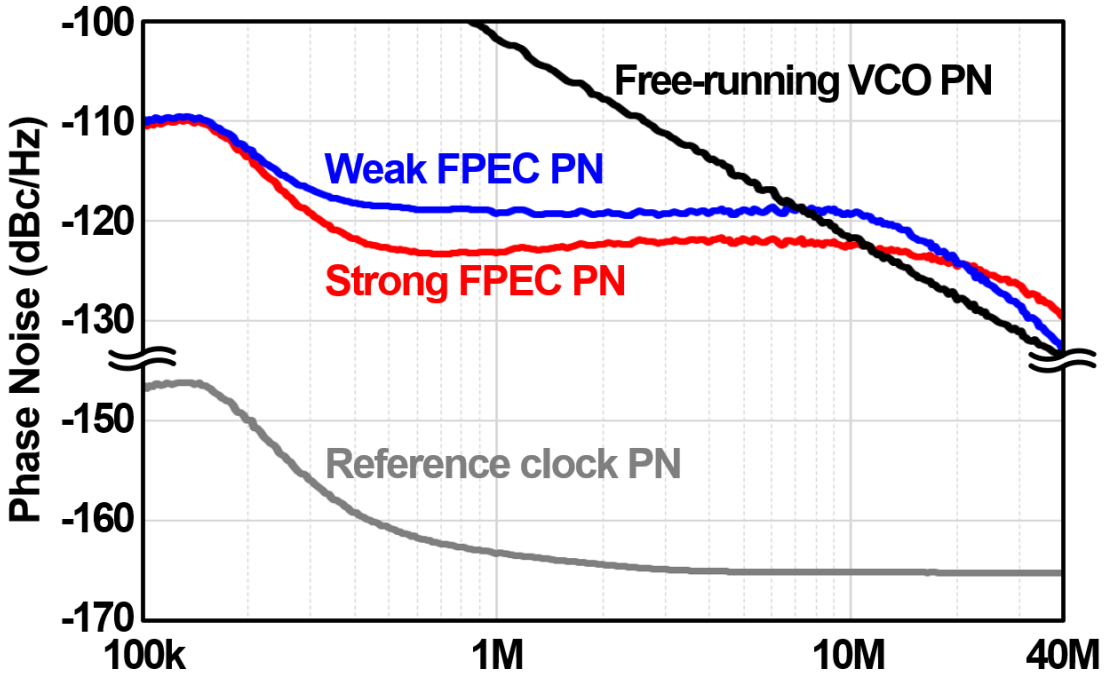


Figure 3-10. Simulated phase noise plots in different FPEC strengths.

To compare the effect of the difference in the FPEC strength, we performed simulations to obtain the phase noise of the output for the two cases of Figures 3-9(a) and (b), as shown in Figure 3-10. The noise profiles of the free-running VCO and the reference clock were obtained from post-layout simulation and the measurement, respectively. As shown in Figure 3-10, the case of the strong FPEC achieves a wider loop bandwidth than that with a weak one, since the stronger FPEC allows the PLL to more quickly remove the phase error (or jitter) of the VCO than its weaker counterpart. Note that the in-band phase noise at frequencies below 200 kHz is saturated by that of the reference clock. At the frequency offset above 8 MHz, phase noises of the FPEC PLLs are slightly higher than that of the free-running VCO. This is because $J_{OUT}(t)$ abruptly changes by the FPEC operation that increases the magnitudes of high-frequency components in the power spectral density (PSD) of $J_{OUT}(t)$ [33]. This effect becomes more noticeable as the FPEC strength increases; thus, the phase noise around 40 MHz of the strong FPEC PLL is higher than that of the weak one. Despite the higher phase noise, the strong FPEC PLL can nevertheless achieve much lower RMS jitter because the noise contribution at those offset frequencies is low.

The values of C_P, C_I, and C_C not only determine the FPEC strength but also affect the noise contribution of the FPEC SLF and the reset PD to the overall in-band phase noise. Their values were therefore carefully chosen based on the following design considerations. In order to maximize the FPEC strength, C_C should be much smaller than C_P and C_I. On the contrary, a lager C_C is better for minimizing

the kT/C noise from SW_P and SW_I. In consideration of this tradeoff in capacitor sizes, C_C was therefore set to 60 fF.

Another noise consideration comes from the reset PD. The intrinsic thermal noise of the reset PD is delivered to V_P whenever it charges C_P, rendering a larger C_P desirable for its ability to reduce this noise. Unlike C_C, increasing C_P is also beneficial to strengthen the magnitude of the FEPC. However, a large C_P occupies too much area. The value of C_P was thus designed to be 3 pF.

From these values of C_C and C_P, using the noise data from the post-layout simulations, the levels of the output in-band phase noise from the reset PD and the FPEC SLF are respectively less than –152 dBc/Hz and –140 dBc/Hz, which are far lower than the overall phase noise. In order to minimize the effect of clock feedthrough or charge injection in the FPEC SLF, C_I was designed to be identical to C_P (just as SW_I was to SW_P). Therefore, the ratio of C_P : C_I : C_C becomes 50 : 50 : 1, by which an FPEC with a sufficient strength, as shown in Figure 3-9(a), can be achieved.

3.5.2. Transient Behavior of the FPEC-SLF PLL for Frequency Acquisition

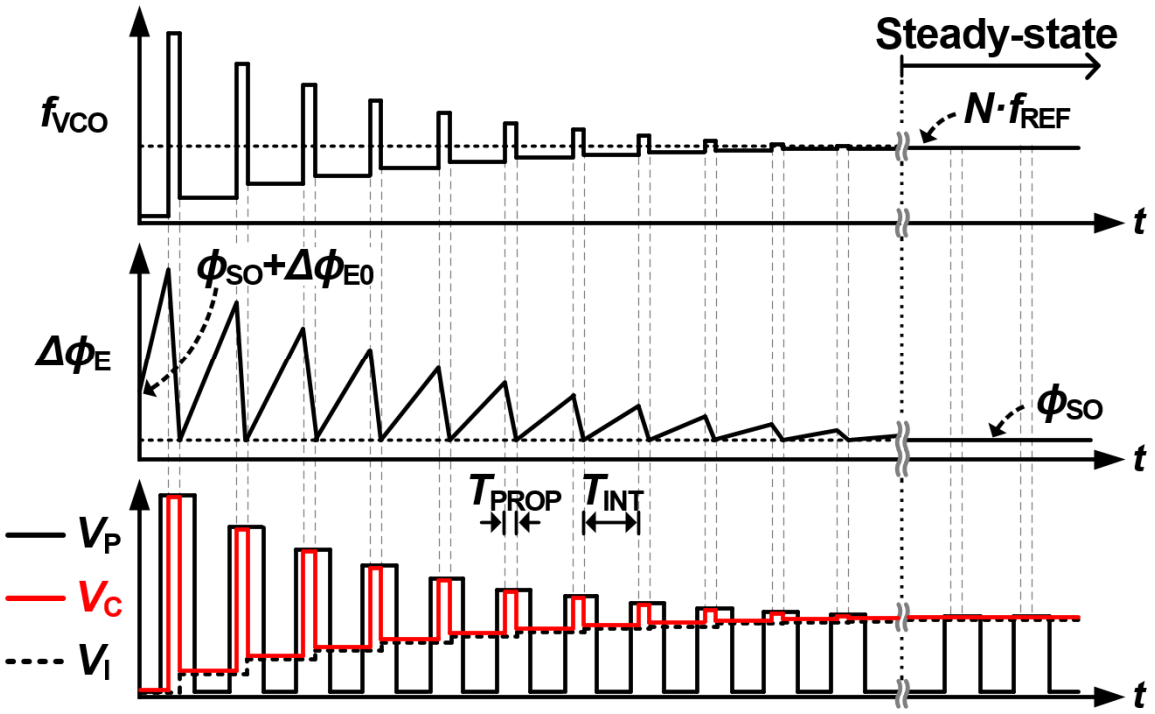


Figure 3-11. Transient behavior when initial $f_{VCO} < N \cdot f_{REF}$.

Figure 3-11 shows a transient behavior of the proposed PLL that achieves a lock when the initial f_{VCO} is much smaller than $N \cdot f_{REF}$. At the beginning of the operation, $\Delta\phi_E$ is set to have $\Delta\phi_{E0}$ and ϕ_{SO}. Due to the large initial deviation of f_{VCO} from $N \cdot f_{REF}$, $\Delta\phi_E$ steeply evolves as the PLL begins the operation. During the following T_{PROP}, $\Delta\phi_E$ quickly drops, where the loop gain is high, which leads to a large increase in V_C. As the operation of the loop switches into T_{INT}, charge sharing between C_C and C_I causes V_C to decrease and V_I to increase. In this period, since f_{VCO} remains smaller than $N \cdot f_{REF}$, $\Delta\phi_E$ increases again. Note that the values of V_C and V_I exceed their initial values, as does f_{VCO}. As the process iterates, f_{VCO} approaches $N \cdot f_{REF}$, and the increase of $\Delta\phi_E$ in T_{INT} becomes more gradual. When f_{VCO} finally meets $N \cdot f_{REF}$, the PLL achieves a lock, V_P, V_C, and V_I settle, and the average of $\Delta\phi_E$ equals that of ϕ_{SO}. With the high gain of the reset PD deployed in this work, ϕ_{SO} was less than 100 ps in a steady state. Since ϕ_{SO} is maintained at such a small value, the proposed architecture resembles a Type-II PLL and can in fact be designed as a Type-II architecture.

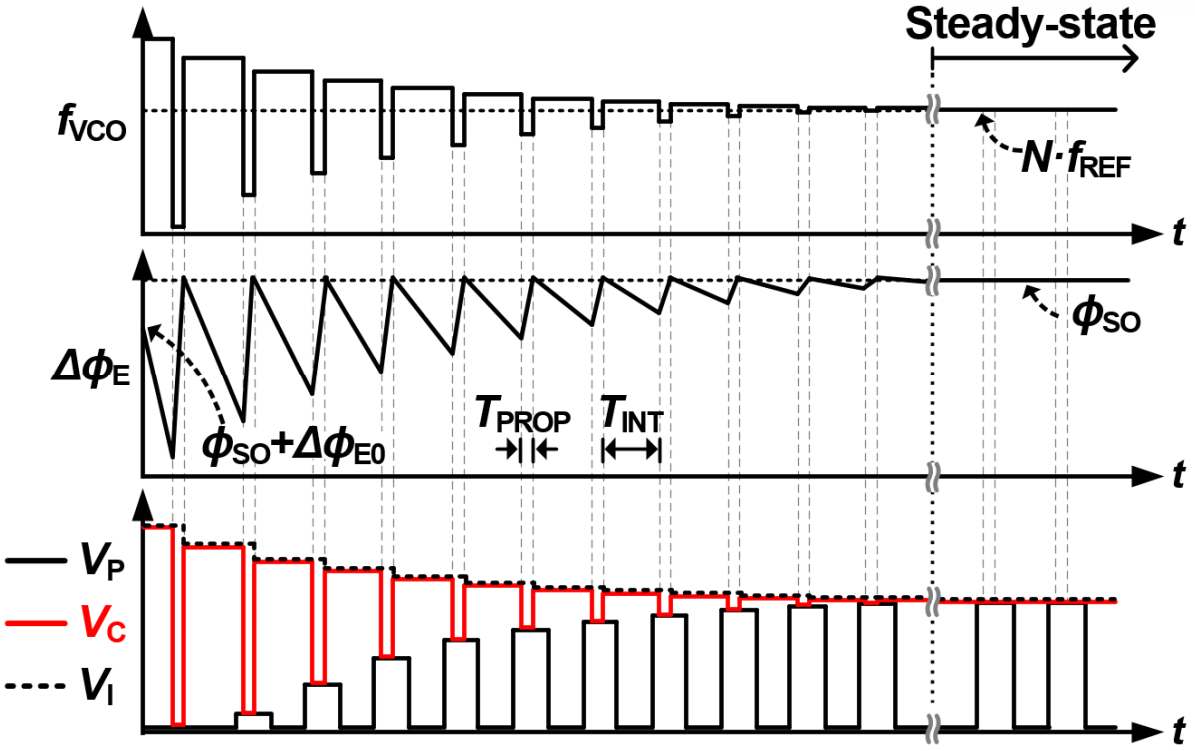


Figure 3-12. Transient behavior when initial $f_{VCO} > N \cdot f_{REF}$.

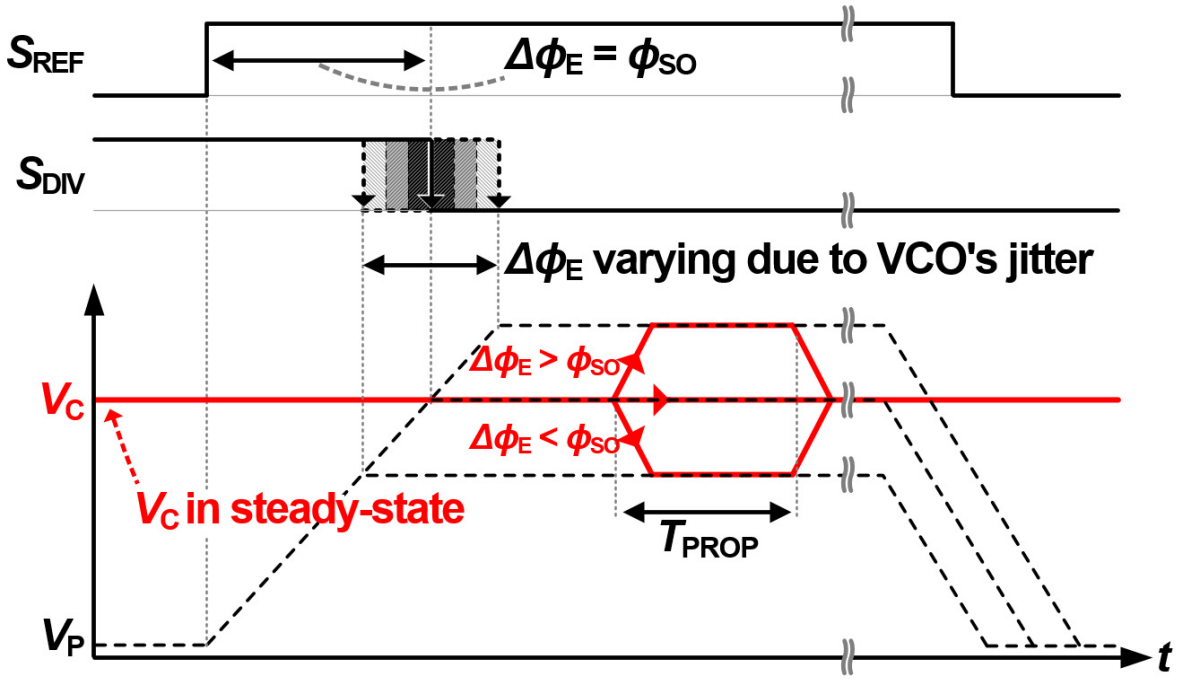
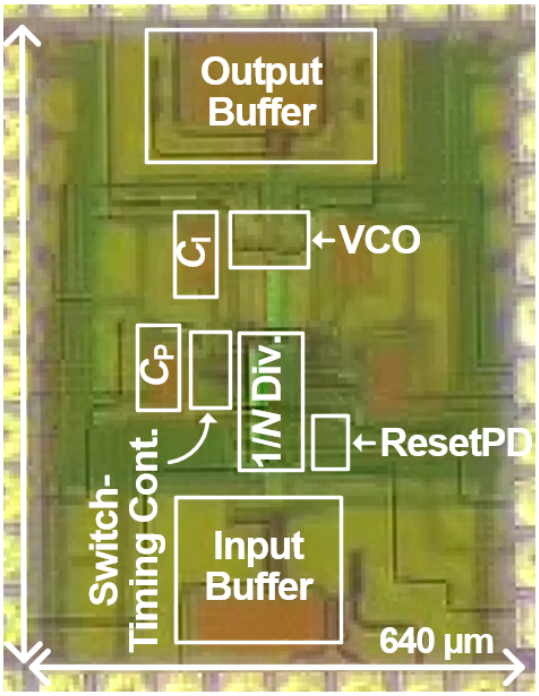


Figure 3-13. Illustration of how V_P and V_C change to correct $\Delta\phi_E$ in steady state.

Figure 3-12 describes the transient behavior that follows when f_{VCO} far exceeds $N \cdot f_{REF}$. At the beginning of the operation, since $\Delta\phi_E$ is much smaller than ϕ_{SO}, there is no overlap between the pulses of S_{REF} and S_{DIV}, and the PD does not increase V_P at all, unlike Figure 3-11. Therefore, when V_C is connected to V_P during T_{PROP}, V_C drops significantly. This large drop of V_C leads to a fast slow-down in f_{VCO}, thereby quickly correcting $\Delta\phi_E$. Through the following iterative process of loop operation, the PLL achieves a lock.

In steady state, $\Delta\phi_{E,}$ defined by the time difference between the rising edge of S_{REF} and the falling edge of $S_{DIV,}$ varies randomly according to the jitter of the VCO. Figure 13 illustrates how V_P and V_C interacts in steady state to correct the variation in $\Delta\phi_{E.}$ When $\Delta\phi_E$ is perturbed to be larger than ϕ_{SO}, V_P proportionally increases over the steady-state value of V_C. As a result, V_C instantaneously increases during T_{PROP} and the variation in $\Delta\phi_E$ is promptly corrected. Similarly, when $\Delta\phi_E$ is less than ϕ_{SO}, V_P is increased less than the steady-state value of V_C, such that V_C drops to quickly correct $\Delta\phi_E$.

3.6. Measurement Results



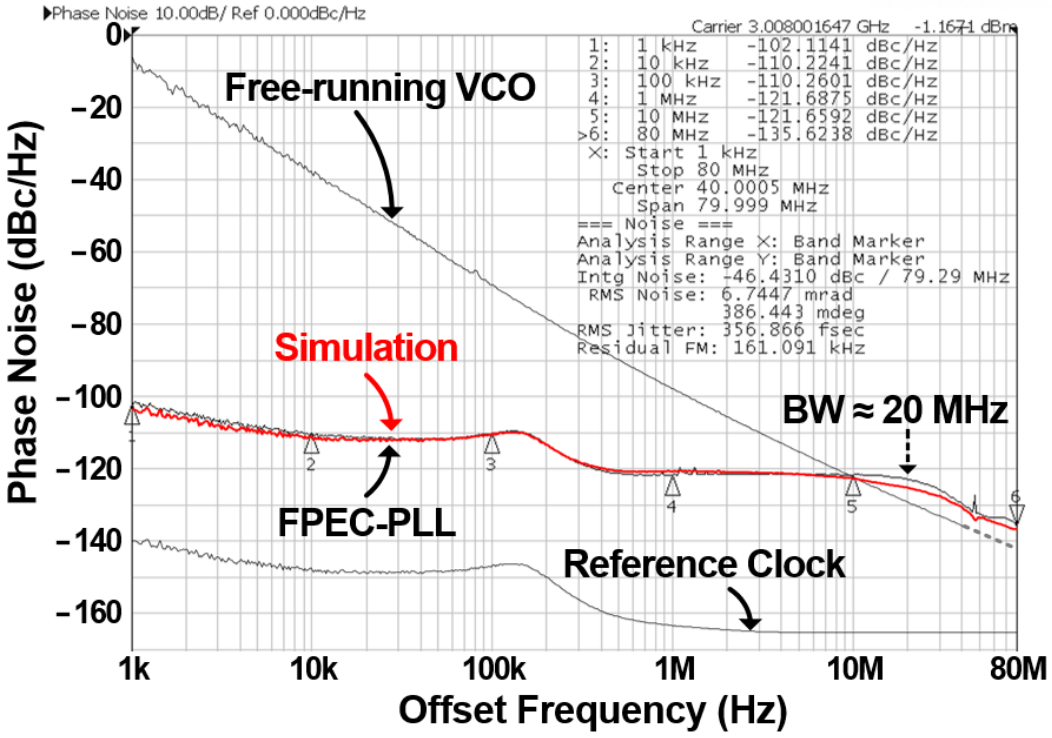
(a)

Power Consumption (mW)	
VCO	4.12
1/*N* Divider	0.24
Reset PD	0.14
Switch-Timing Controller	0.08
Total	4.58

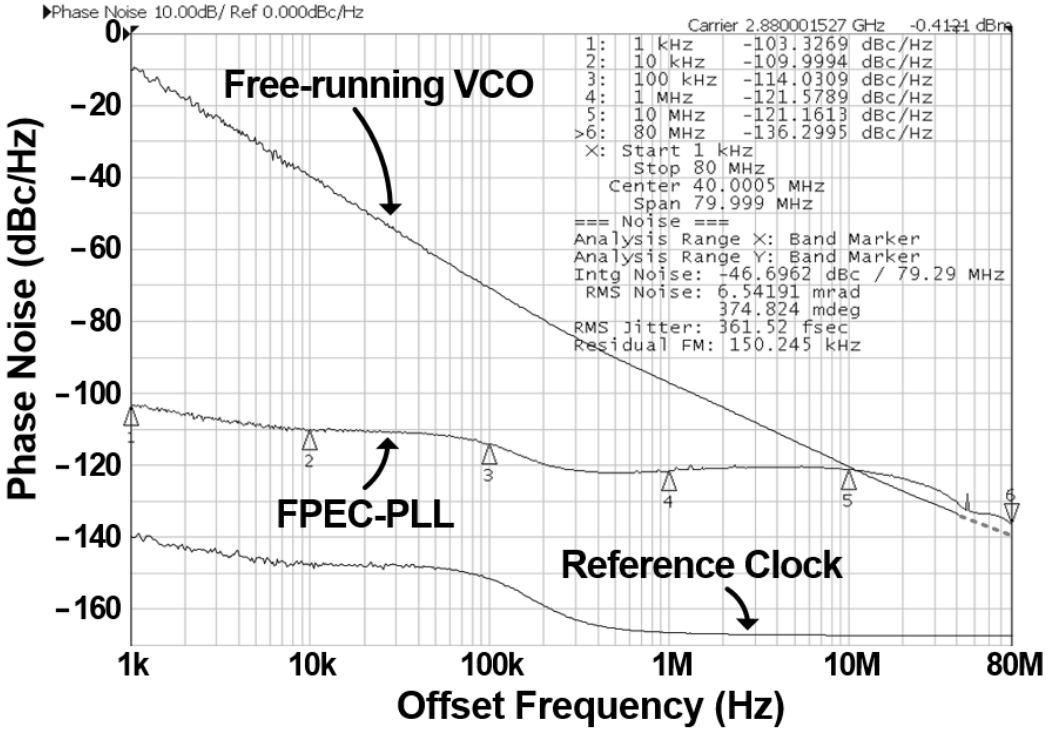
(b)

Figure 3-14. (a) Die micrograph; (b) power-breakdown table.

Figure 3-14(a) shows the micrograph of the proposed PLL. It was fabricated in a 65-nm CMOS technology and occupies an active area of 0.047 mm^2. The total power consumption was approximately 4.6 mW as shown in Figure 3-14(b). The nominal supply voltage was 1.2 V, but the circuits relevant to drive SW_P and SW_I (thick-oxide NMOSs) used a 2.2-V supply. The VCO consumed 4.12 mW and other circuits of the loop consumed 0.46 mW. Figure 3-15(a) shows the measured phase noise of 3.008-GHz output signal, when a 47-MHz reference clock was used. As shown in Figure 3-15(a), a very wide bandwidth of more than 20 MHz, (i.e.: comparable to $f_{REF}/2$) dramatically suppresses the jitter of the ring VCO. Before turning on the loop, the 1-MHz noise of the free-running VCO was −98.2 dBc/Hz. However, after turning on the loop and as the FPEC operation started, the same spot noise was reduced to −121.6 dBc/Hz. The phase noise of the PLL at the frequency offset above 10 MHz is 3 dB higher than that of the free-running VCO. This is because the FPEC operation emulates the phase realignment mechanism of an ILCM, as detailed in Chapter 3.4.1. The gap between the two phase-noise plots around an offset frequency of 20 MHz is slightly larger than 3 dB. This is because the noise from the reference



(a)



(b)

Figure 3-15. Measured phase noise (a) at 3.008 GHz; (b) at 2.880 GHz.

clock was introduced (since N is considerably large as 64, the elevation of the noise of the reference clock by $20 \cdot \log N$ is considerable). The RMS jitter integrated from 1 kHz to 80 MHz was 357 fs. Figure

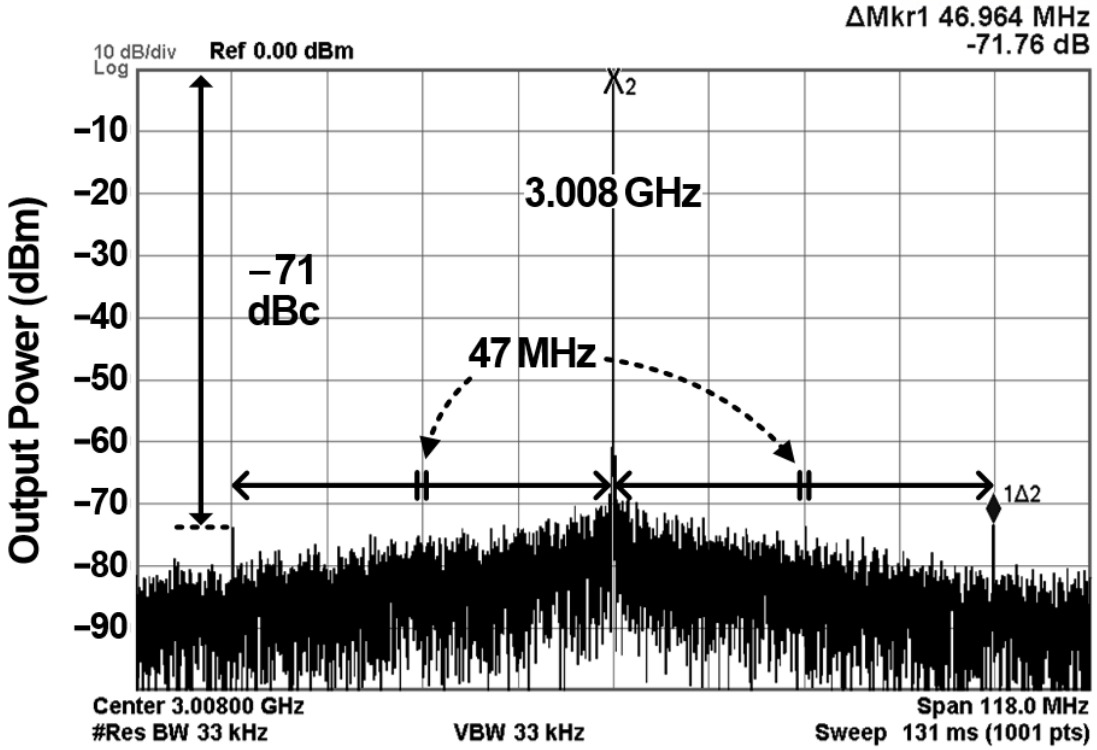


Figure 3-16. Measured spectrum at 3.008 GHz.

Table 3-I. Performance comparison with some of state-of-the-art ring-VCO-based clock generators.

	This work	JSSC'16 [6] S. Choi	ISSCC'17 [15] D. Coombs	ISSSC'16 [13] H. Kim	JSSC'16 [21] L. Kong	ISSCC'16 [25] K-Y. J. Shen
Process (CMOS)	65 nm	65 nm	65 nm	65 nm	65 nm	14 nm
Architecture	SLF-PLL w/ FPEC	ILCM	ILCM	MDLL	SLF-PLL	SLF-PLL
Out. freq., f_O (GHz)	3.008	1.2	5.0 (2.5 – 5.75)	2.4	2.4 (2.0 – 3.0)	4.0 (0.4 – 5.0)
Ref. freq. (MHz)	47	120	125	75	22.6	100
Mult. Factor (N)	64	10	40 (20 – 46)	32	106 (88 – 133)	40 (4 – 125)
1MHz PN (dBc/Hz) @ f_O (GHz)	−121.6 @ 3.008	–134.4 @ 1.2	–116.0 @ 5.0	–115.0 @ 2.4	–113.8 @ 2.4	–112.0 @ 4.0
Integ. jitter,σ_t (fs) (Integ. range)	357 (1k − 80MHz)	185 (10k – 40MHz)	340 (1k − 40MHz)	699 (10k – 40MHz)	970 (10k – 200MHz)	1264 (100k – 1GHz)
Ref. spur (dBc)	–71	–53	–45	–51	–65	N/A
Power, P_{DC} (mW)	4.6	9.5	5.3	1.51	4.0	2.6
Active area (mm^2)	0.047	0.06	0.09	0.024	0.015	0.021
*FOM_{JIT} (dB)	–242.3	–244.9	-242.4	–241.3	–234.1	–233.9

*FOM_{JIT}: $10\log_{10}(\sigma_t^2 \cdot P_{DC}(\text{mW}))$ (dB)

3-15(b) shows another measured phase noise when the output frequency was 2.880 GHz from a 45-MHz reference clock. The 1-MHz phase noise and σ_{RMS} were respectively −121.5 dBc/Hz and 362 fs.

Figure 3-16 shows the output spectrum. The level of the reference spur at the 47-MHz offset was −71 dBc when the output frequency was 3.008 GHz.

Table 3-I compares the performance of the proposed PLL with that of some of state-of-the-art ring-VCO-based clock generators. This work achieved excellent performances of RMS jitter and the figure-of-merit of jitter (FOM_{JIT}), almost comparable to those of ILCMs and an MDLL, while having a much lower reference spur and a larger N. Compared to conventional SLF PLLs, this work achieved lower RMS jitter, thereby achieving much better FOM_{JIT}.

Figure 3-17 compares the performances of the proposed architecture, in terms of FOM_{JIT} and the level of a reference spur, with those of the state-of-the-art ring-VCO-based clock generators, where N is four or more. Figure 3-17 clearly shows the proposed PLL achieved the outstanding performances of jitter and reference spur simultaneously.

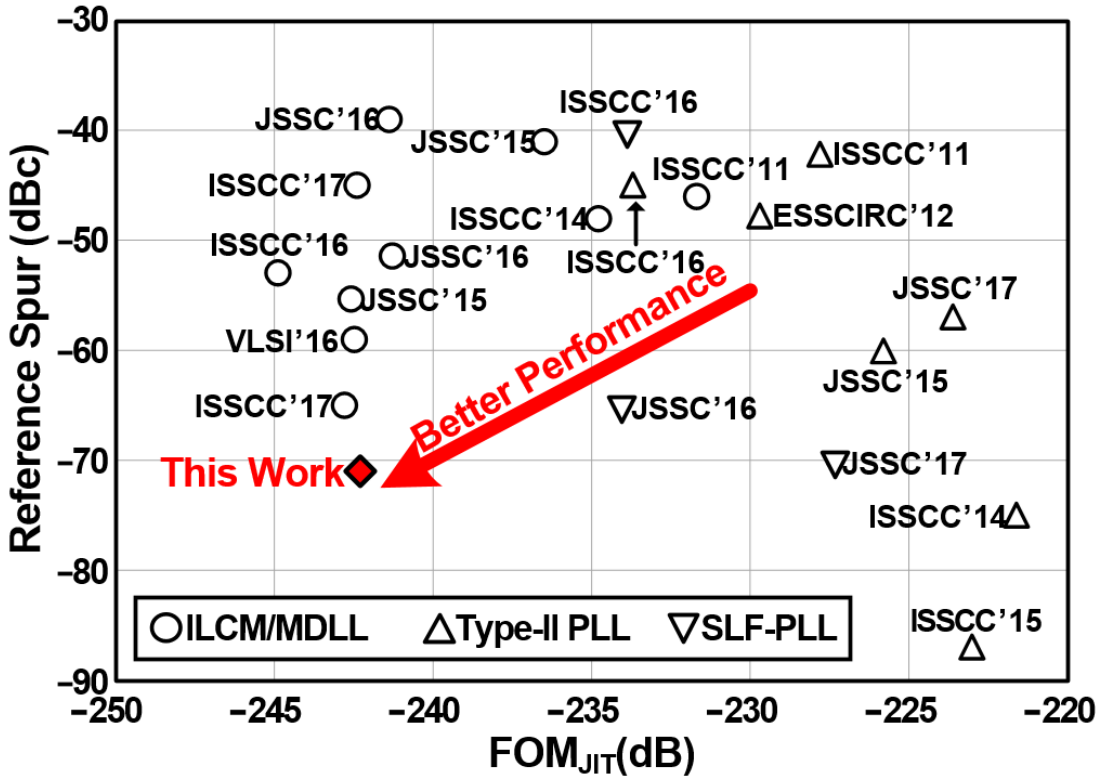


Figure 3-17. Performance comparison with some of state-of-the-art ring-VCO-based clock generators ($N \geq 4$).

3.7. Discussion

In this work, we have demonstrated a PLL using the proposed FPEC technique. Despite the use of a ring VCO, this prototype PLL achieved an ultra-low jitter while maintaining low reference spur. The key feature of the FPEC technique is to emulate the mechanism of the phase realignment in an ILCM, thereby removing the VCO's jitter dramatically during a short period. As a result, the proposed PLL achieved low RMS jitter of the output signal comparable to that of an ILCM. Since the proposed architecture has an intrinsic integrator in its transfer function, it was also able to achieve a low reference spur despite a large multiplication of N.

This work also presented the SFT technique that isolates a VCO from the effect of the clock feedthrough which occurs due to the switching operations in the FPEC SLF. As a result, the proposed ring-VCO-based SLF PLL with the FPEC technique achieved ultra-low jitter, low reference spur and large N concurrently.

4. Proposed Ring-DCO-Based Digital PLL Using a FPEC Technique and an Optimally-Spaced TDC

4.1. Motivations and Overview

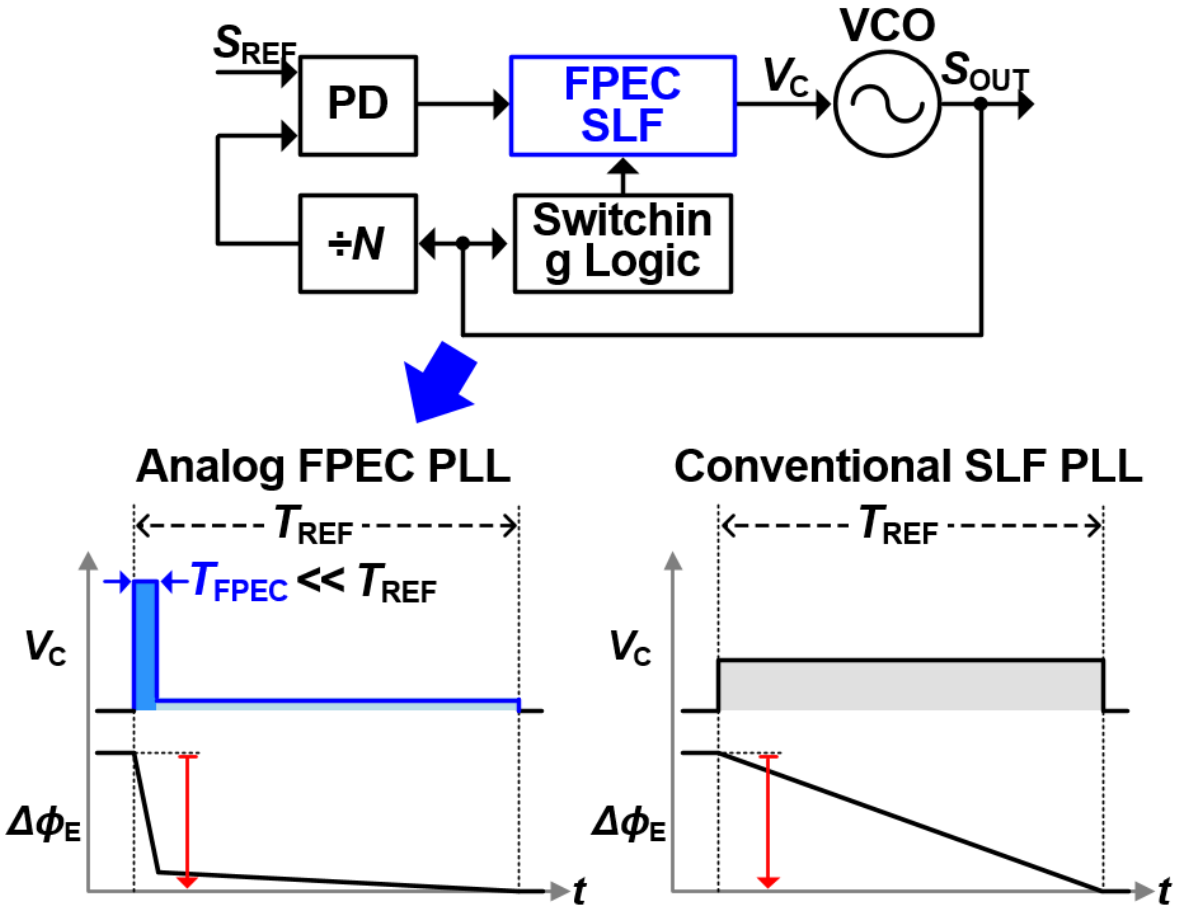


Figure 4-1. Analog FPEC PLL using an SLF.

In order to solve the design challenges of conventional ring-oscillator-based ILCMs and SLF PLLs, which were limited in their ability to concurrently have good performances of the RMS jitter and reference spur with a large N, we proposed an SLF PLL with the FPEC technique [27], [28], as described in Chapter 3. This PLL with the FPEC technique (or the FPEC PLL) emulates the phase-realignment mechanism of an ILCM. As shown in Figure 4-1, after detecting a phase error, an SLF with the FPEC technique generates a significant increase or decrease in the control voltage of a VCO during a short period of time (during T_{FPEC}). This mechanism allows the FPEC PLL to correct phase errors more quickly than conventional SLF PLLs, thereby achieving low RMS jitter comparable to that of ILCMs. Because the transfer function of the FPEC PLL naturally involves an intrinsic integrator, a low level of reference spur even for a large N is also achievable. However, based on the analog implementation, the

FPEC PLL presented in Chapter 3 [27], [28] has trouble in sustaining an optimal loop gain, and the loop parameters could easily vary by the change of the output frequency or PVT variations. For instance, in the analog FPEC PLL of Chapter 3, according to post-layout simulation, the value of K_{VCO} varies across the tuning range of V_C by approximately ±30% from the target value of 150 MHz/V. By PVT variations and/or the change of the output frequency, V_C could settle to an arbitrary value, and this results in the deviation of the β of the loop from 1, thereby increasing RMS jitter. To avoid this, β was initially calibrated by controlling K_{PD} in the analog FPEC PLL in Chapter 3 (the PD was designed to have six-bit switchable PMOSs to change K_{PD}).

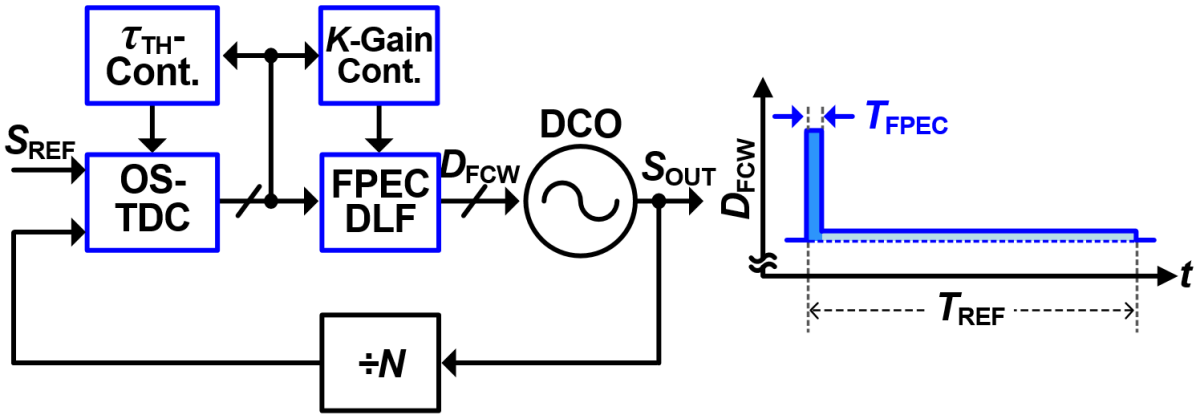


Figure 4-2. Proposed FPEC digital PLL (FPEC DPLL) and the optimally-spaced (OS) TDC.

To address this limitation of analog implementation and for a complete design, implementing the FPEC technique in a digital PLL (DPLL) can be a solution. By doing so, the variation of loop characteristics can be tracked and calibrated in the background by a simple digital algorithm. However, simply porting the FPEC technique into a DPLL in a conventional way is insufficient to achieve ultra-low jitter of the analog FPEC PLL. This is because a typical time-to-digital converter (TDC) used in conventional DPLLs provides less precise information regarding the oscillator's jitter than a PD in analog PLLs. Thus, in a DPLL, to fully exploit the FPEC technique, the TDC quantization error must be minimized. The relationship between the error and the FPEC technique is discussed in Chapter 4-2, along with the explanation on the capability of the jitter reduction in the FPEC DPLL over conventional DPLLs.

In Chapter 4, this work presents an FPEC DPPL that concurrently achieves an ultra-low jitter and a low reference spur. As shown in Figure 4-2, a DPLL with the FPEC technique can be implemented by increasing or decreasing the frequency-control word, D_{FCW}, of the digital loop filter (DLF) shortly during T_{FPEC}. This work also presents a low-power optimally-spaced (OS) TDC capable of minimizing the quantization error, τ_Q effectively [34], [35], thereby overcoming the problem of a conventional TDC.

In the design of a TDC, the conventional approach to minimize τ_Q has been to reduce the spacing between the decision thresholds (DTs). In this approach, however, the number of DTs inevitably increases to cover the dynamic range of a TDC with the minimized steps of DTs [36]. Instead of this approach, the proposed OS TDC uses a small number of DTs. In the proposed FPEC DPLL, the DTs and the gain of the error correction by the loop are continuously calibrated to be the optimal values calculated from the Lloyd-Max algorithm (LMA) [37]. Thus, τ_Q can be reduced dramatically, even with a small number of DTs and low power consumption. Since the proposed architecture is implemented in a digital fashion, the variables that define the loop characteristics can be easily estimated and corrected by digital calibrators in the background. As a result, the performances of an ultra-low jitter and the figure-of-merit (FOM) can be achieved.

Chapter 4 is organized as follows. Chapter 4.2 describes the capability of the proposed DPLL with an FPEC technique and effect of τ_Q. Chapter 4.3 presents an analysis of the proposed OS TDC. Chapter 4.4 presents the operation principle and the implementation of the proposed DPLL. Experimental results are presented in Chapter 4.5, and conclusions are drawn in Chapter 4.6.

4.2. Capability of the proposed DPLL with a FPEC Technique and Effect of Quantization Error (τ_Q)

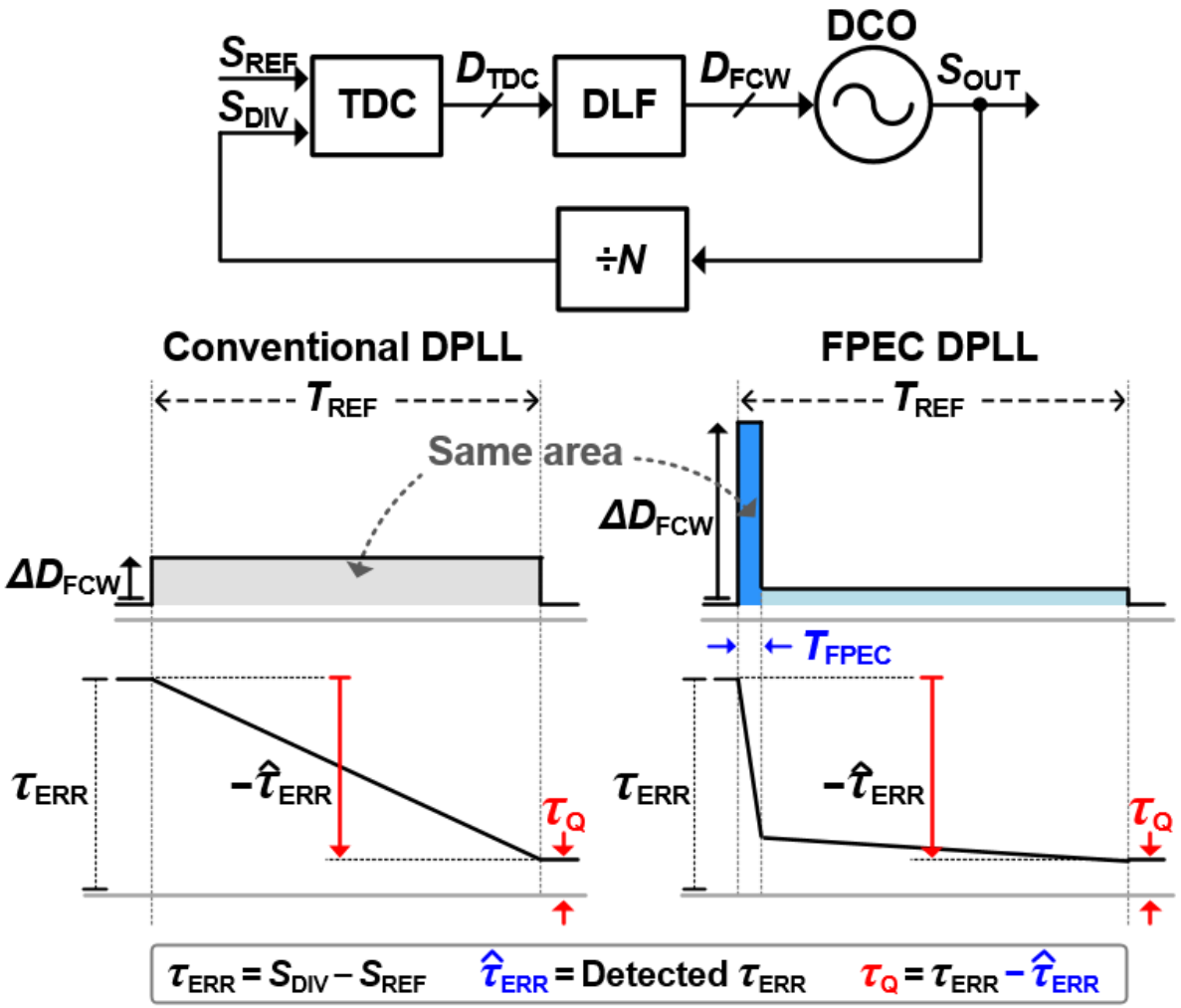


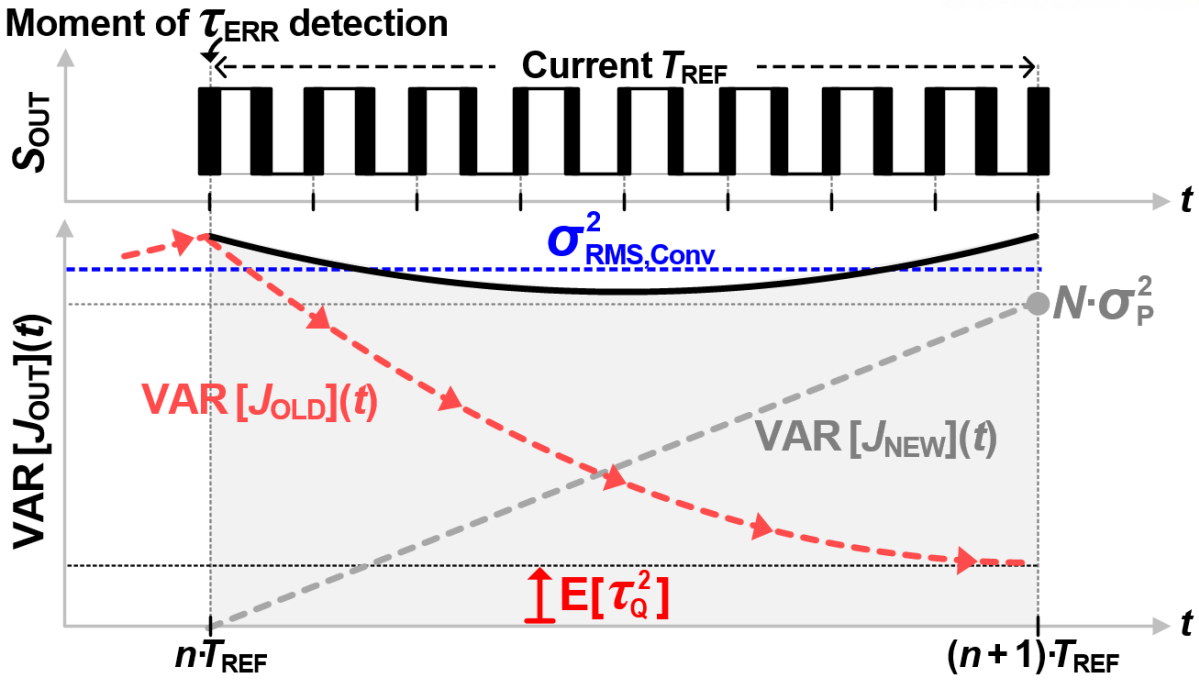
Figure 4-3. Comparison of the phase (or timing) error correction between conventional DPLLs and the proposed FPEC DPLL.

Figure 4-3 compares the process of correction in phase (or timing) error between conventional DPLLs and the proposed FPEC DPLL. The top of Figure 4-3 shows an architecture of a typical DPLL consisting of a TDC, a DLF, a digitally-controlled oscillator (DCO), and a divider. The notations S_{REF}, S_{DIV}, and S_{OUT} represent the signals from the reference clock, the divider, and the DCO, respectively. When the TDC detects a timing error between S_{REF} and S_{DIV}, which is denoted by τ_{ERR}, it generates a corresponding digital code, D_{TDC}. In Figure 4-3, $\hat{\tau}_{ERR}$ denotes a digitized version of τ_{ERR} that the TDC recognizes. As

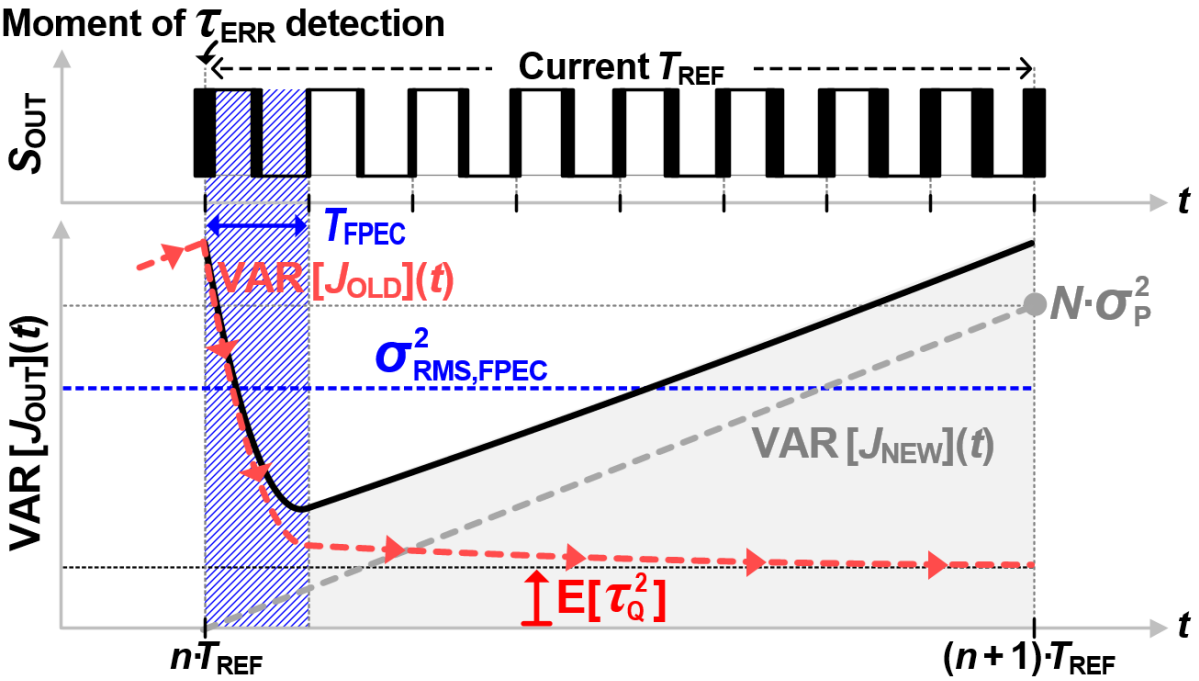
D_{TDC} is delivered to the following DLF, D_{TDC} is processed and D_{FCW} is adjusted to correct the detected timing error. Even though the same D_{TDC} is generated in both the conventional and proposed architectures, the change of D_{FCW} (or ΔD_{FCW}) is very different. This difference in ΔD_{FCW} makes a huge difference in reduction of the timing error between the two architectures. In a conventional DPLL, the DLF maintains ΔD_{FCW} constantly over T_{REF}; thus, $\hat{\tau}_{ERR}$ is linearly removed. On the other hand, in the FPEC DPLL, the DLF sets its gain to be very high during a short period of T_{FPEC}, thereby making ΔD_{FCW} experience a huge change momentarily during T_{FPEC}. Thus, $\hat{\tau}_{ERR}$ is quickly removed during the short duration. For the remaining time of T_{REF}, the loop gain is reduced to ensure loop stability. In Figure 4-3, $\hat{\tau}_{ERR}$ is assumed to be completely removed within one T_{REF}; thus, the colored area in ΔD_{FCW} is the same in both cases. Note that, even though the detected τ_{ERR} is supposed to be corrected by the amount of $\hat{\tau}_{ERR}$, τ_Q remains in both architectures, since the TDC has difficulty to recognize it due to the limited resolution. As described in Chapter 3, the faster the error correction, the lower the RMS jitter, σ_{RMS}. We may thus intuit that the proposed FPEC DPLL is able to achieve far lower σ_{RMS} than conventional DPLLs.

Figures 4-4(a) and (b) represent the way in which σ_{RMS} is determined in conventional DPLLs and the FPEC DPLL, respectively. To analyze only the PLL's capability to suppress the jitter of the DCO, all noise sources except for the DCO are ignored. For a fair comparison, it is assumed that the identical TDC and DCO are used in the two architectures. Notations (e.g.: σ_P, $J_{OUT}(t)$, $J_{OLD}(t)$, and $J_{NEW}(t)$) and methodology for estimating σ_{RMS} are the same as those used in Chapter 3. Then, as shown in Figure 4-4(a) and (b), we can conclude that the fast error-correction process allows the FPEC DPLL to achieve much lower σ_{RMS} than conventional DPLLs.

As described in the above analysis, with the FPEC technique, the FPEC DPLL can achieve much lower σ_{RMS} jitter than conventional DPLLs. The FPEC DPLL, however, has a problem in that the minimum achievable σ_{RMS} is still considerably higher than that of an analog FPEC PLL. Due to the nature of digitization, the resolution of typical TDCs is finite, which differs from analog PDs. For this reason, the timing error that the TDC captures is $\hat{\tau}_{ERR}$ not τ_{ERR} and τ_Q always remains at the end of the T_{REF} in the error-correction process of the FPEC DPLL (and also of typical DPLLs). As shown in Figures 4-4(a) and (b), since τ_Q is present, VAR[J_{OLD}](t) cannot be eliminated during the current cycle of T_{REF}. At the end point of every cycle of the T_{REF}, VAR[J_{OLD}](t) is thus reduced to a non-zero value of E[τ_Q^2], which is defined by the average of the squared τ_Q, and this degrades σ_{RMS}. Therefore, to fully exploit the FPEC technique, the quantization error of TDCs (or E[τ_Q^2]) must be minimized.



(a)



(b)

Figure 4-4. Conceptual illustration of how σ_{RMS} is determined according to error-correction mechanisms: (a) in a conventional DPLL; (b) in the FPEC DPLL.

4.3. Proposed Optimally-Spaced (OS) TDC

4.3.1. Limits of BBPDs and Introduction of the Proposed OS TDC

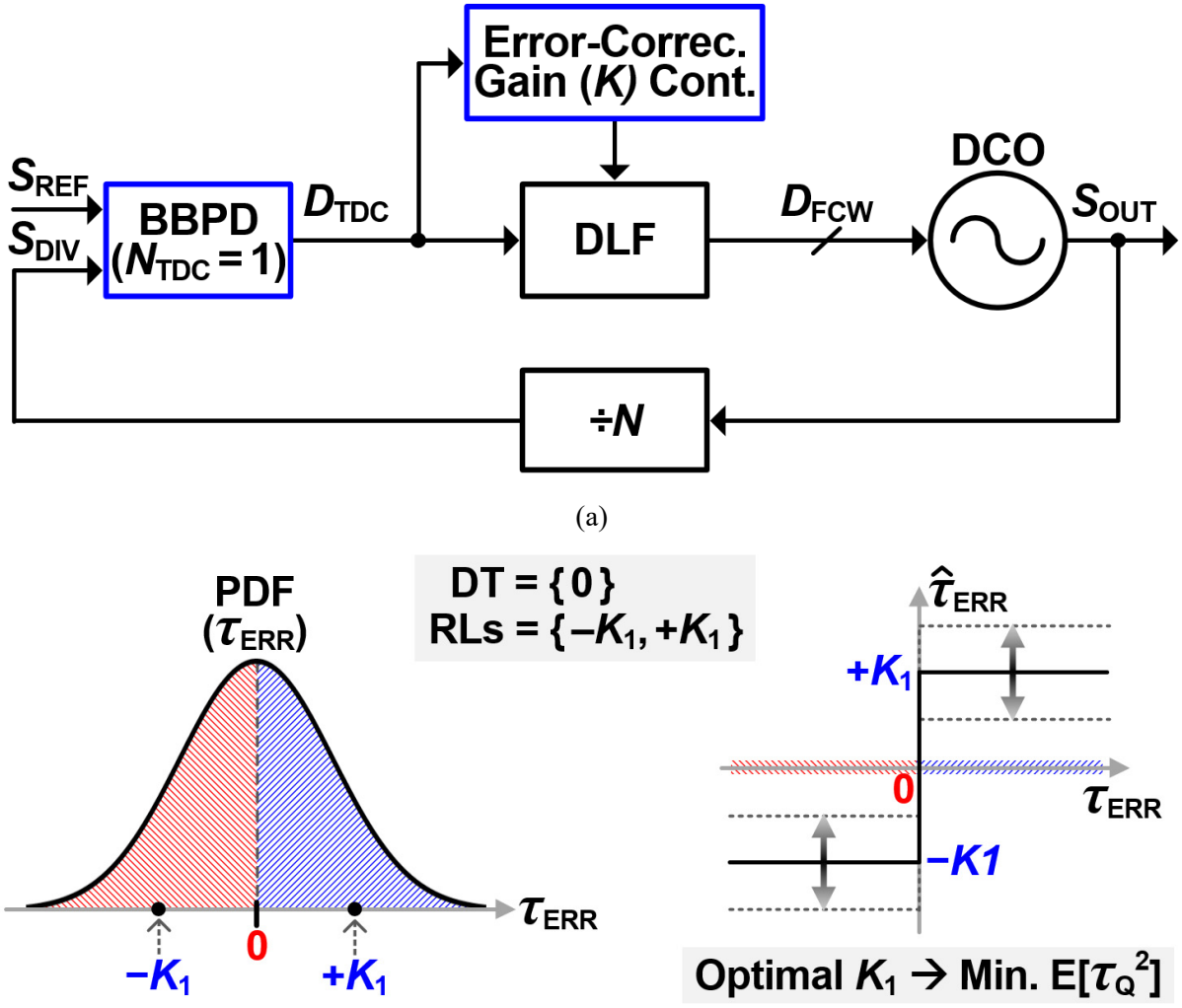


Figure 4-5. Conventional BBPD-based DPLL using the gain correction technique: (a) block diagram; (b) representative levels and decision thresholds for given PDF of τ_{ERR}.

It seems that reducing the spacing between DTs to a level at which the quantity of jitter is easily distinguished (e.g., sub-100-fs level) is fairly straightforward. However, achieving such a fine resolution in a typical CMOS process, which is necessary in order to minimize τ_Q in a typical multi-bit TDC, is very difficult. Even if the implementation were possible, it would require a lot of power because the number of DTs significantly increases to sufficiently cover a wide dynamic range [36]. Figure 4-5(a) shows another approach to reduce τ_Q, where a bang-bang PD (BBPD) and an error-correction gain (K)

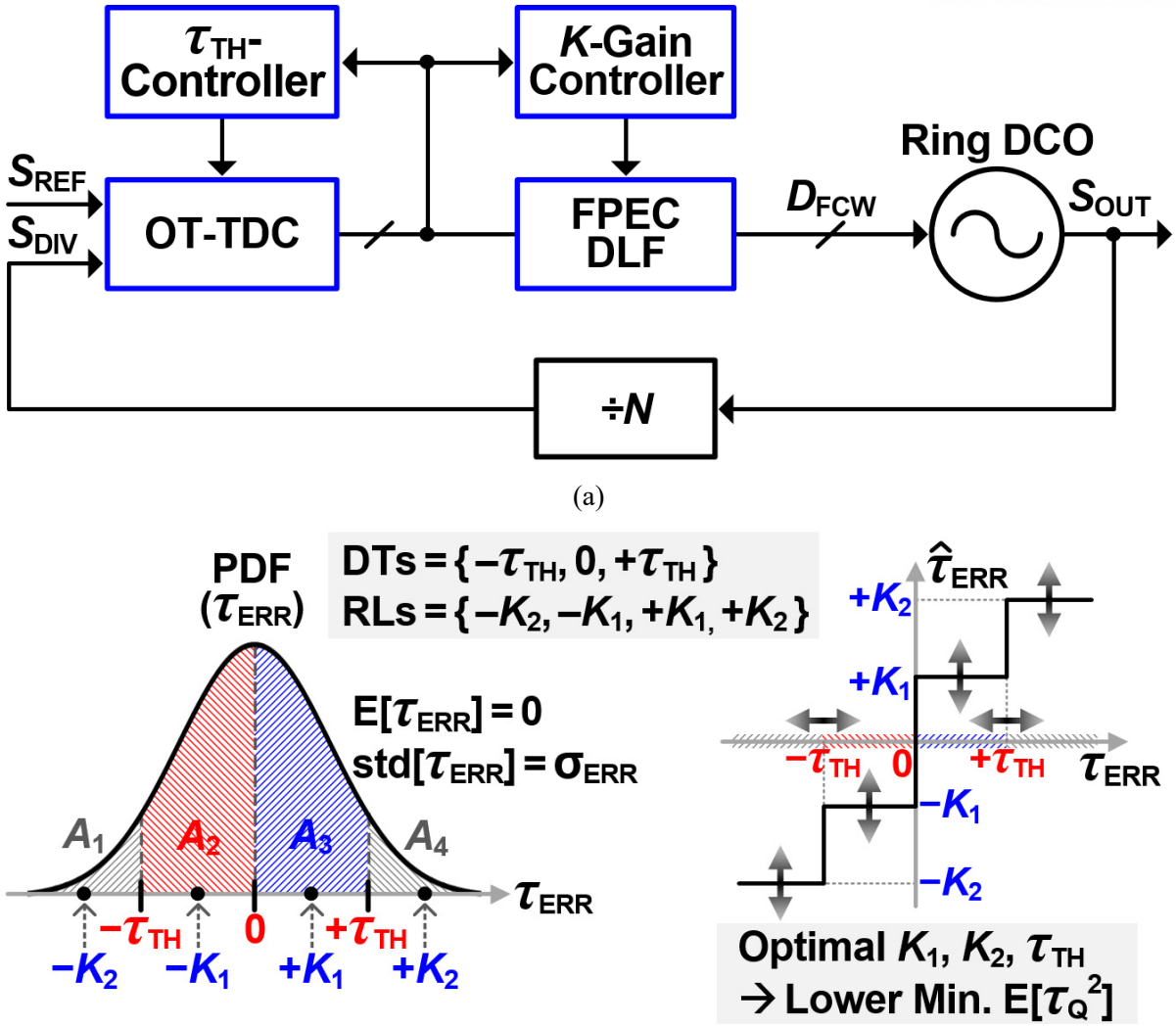


Figure 4-6. Proposed FPEC DPLL using the optimally spaced (OS) TDC: (a) block diagram; (b) representative levels and decision thresholds for given PDF of τ_{ERR}.

controller are used [36], [38]–[41]. In this approach, the use of a BBPD offers advantages of a lower power consumption and a lower design complexity. However, this method has a critical problem that a BBPD has a limit to acquire precise information of τ_{ERR}. For further analysis about this, let us first investigate how the BBPD-based DPLL recognizes and estimates τ_{ERR}. Figure 4-5 (b) depicts the probability density function (PDF) of τ_{ERR} with a DT and two representative levels (RLs) [36]. In Figure 4-5 (b), DTs function as a set of time thresholds for TDC and are distinct from τ_{ERR}, and the RLs function as a set of the amounts of the error correction proceeded by the DPLL. Since the BBPD provides only the polarity information of τ_{ERR}, it has only one DT as zero. Consequently, the number of RLs is only two, which means the error correction can be performed by the amount of either $+K_1$ or $-K_1$, where K_1 denotes the DPLL error-correction gain. In this case, if the value of K_1 is set too small, the DPLL corrects

the error insufficiently, whereas it corrects the error excessively if the value is set too large. Therefore, when K_1 is optimally set so too is the error correction of the DPLL, minimizing $E[\tau_Q^2]$. The minimum value of $E[\tau_Q^2]$ is still considerably large, however, since the number of DTs and RLs in the BBPD-based DPLL is insufficient to precisely detect and correct τ_Q. In order to overcome this limitation due to the nature of a BBPD, we present the optimally-spaced (OS) TDC having multiple DTs and RLS.

A block diagram of the proposed DPLL with the OS TDC is shown in Figure 4-6(a). The DTs and RLs of the OS TDC are drawn with the PDF of $\tau_{ERR,}$ as shown in Figure 4-6 (b). The number of DTs of the OS TDC, N_{TDC}, is designed as three, and the set of the DTs is $\{-\tau_{TH}, 0, +\tau_{TH}\}$, in which τ_{TH} denotes a reference timing to distinguish τ_{ERR}. Since N_{TDC} is three, there are four RLs and their set can be represented as $\{-K_2, -K_1, +K_1, +K_2\}$. Here, K_2 denotes another value of the error-correction gain of which magnitude is larger than K_1. In the OS TDC, the key feature is that its DTs and RLs are optimized in the background (how they are adjusted to what values will be detailed in the following chapter) using two digital calibrators of the τ_{TH} controller and the K-gain controller. Then, the proposed FPEC DPLL with the proposed OS TDC can significantly lower $E[\tau_Q^2]$, thereby achieving far lower σ_{RMS} than conventional BBPD-based DPLLs.

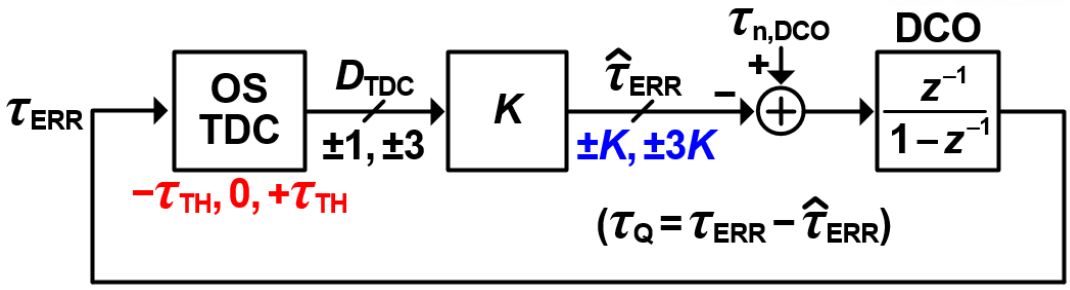
4.3.2. Optimization of Decision Thresholds and Representative Levels of OS TDC

Let us now focus on determining the optimum values of the DTs and the RLs of the OS TDC. Because multiple variables of $\tau_{TH,}$ K_1, and K_2, are free to vary, optimizing these values is more challenging than one-dimensional optimization. To simplify the procedure, we assume that the distances between the RLs remain the same. From this assumption, we can represent the sets of DTs and the RLs as $\{-\tau_{TH}, 0, +\tau_{TH}\}$ and $\{-3K, -K, +K, +3K\}$, respectively, in which K is an error-correction gain of the PLL. Of course, the minimum achievable σ_{RMS} of this case would be higher than that of the case in which K_1 and K_2 vary independently. However, the difference of σ_{RMS} between the two cases is negligible (validation for this will be followed at the end of this chapter). As shown in Figure 4-6 (b), when we assume only thermal noise is present in the DCO, the PDF of τ_{ERR} forms a white Gaussian having the standard deviation of σ_{ERR}. For the given information of τ_{ERR}'s PDF, the objective is then to figure out the optimal values of K and τ_{TH}, which minimizes $E[\tau_Q^2]$.

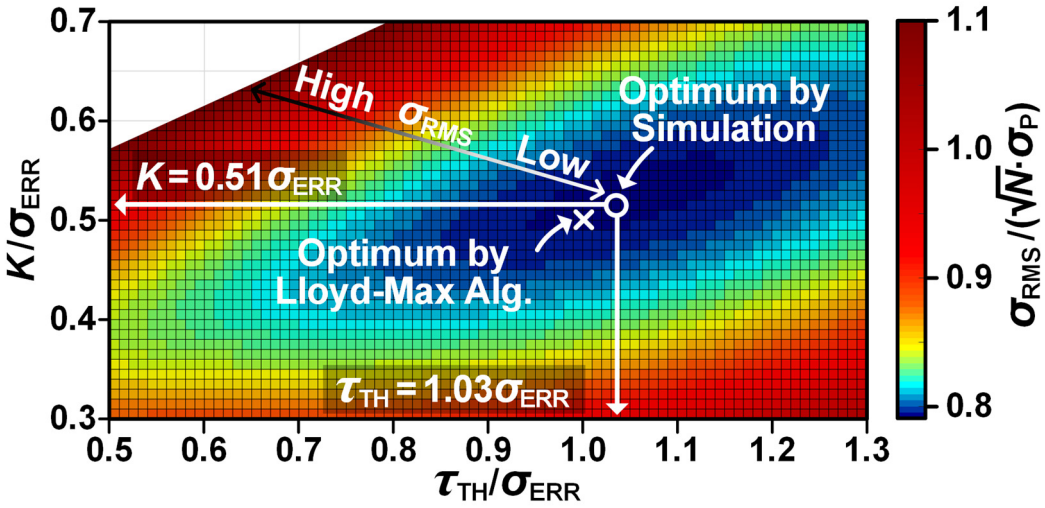
We found that the Lloyd-Max algorithm (LMA) [37] can provide proper solution to this problem. Originally, this algorithm was developed to find general solution of DTs and RLs that can minimize the variance of the quantization error for any given PDFs. According to this algorithm, the optimal values of K and τ_{TH} and are calculated to be $0.5\sigma_{ERR}$ and σ_{ERR}, respectively. The reason behind such a simple form of the solutions is because of the assumption that τ_{ERR} follows Gaussian. When choosing the values K and τ_{TH} as $0.5\sigma_{ERR}$ and σ_{ERR}, respectively, the probabilities of $P(\tau_{ERR}<-\tau_{TH})$, $P(-\tau_{TH}<\tau_{ERR}<+\tau_{TH})$, and $P(\tau_{ERR}>+\tau_{TH})$ are equal to 0.16, 0.68, and 0.16, respectively, and these values are used for the calibration of τ_{TH} (how they are calibrated will be elaborated in the following chapter).

To validate whether the solutions obtained from LMA offers the minimum σ_{RMS}, we performed simulations based on the behavioral model, as shown in Figure 4-7(a). The noise profile of the DCO, $\tau_{n,DCO}$, which is used in the behavioral model, is obtained from the post-layout simulation. Figure 4-7 (b) shows σ_{RMS} with respect to the values of K and τ_{TH} and; the dark blue color implies a lower σ_{RMS}, and the dark red color does a higher σ_{RMS}, as shown in the jet colormap. According to the results of the simulation, when K and τ_{TH} are respectively $0.51\sigma_{ERR}$ and $1.03\sigma_{ERR}$, the minimum σ_{RMS} is achieved and they agree well with the solution obtained by theoretical calculation from the LMA.

If we can independently adjust each of K_1 and K_2 without the aforementioned assumption that the distances between RLs are equal, the optimal values of K_1, K_2, and τ_{TH} obtained from the LMA slightly changes to $0.46\sigma_{ERR}$, $1.51\sigma_{ERR}$, and $0.98\sigma_{ERR}$, respectively. With these values, σ_{RMS} can be further lowered compared to the case in which τ_{TH} and K are σ_{ERR} and $0.5\sigma_{ERR}$, respectively, but the improvement is less than 1%. Note that controlling K_1 and K_2 independently offers a very slight reduction of σ_{RMS}, but increases the dimension of the optimization, thereby making analysis and implementation



(a)



(b)

Figure 4-7. (a) Behavioral model of the proposed PLL with the OS TDC; (b) simulated σ_{RMS} across τ_{TH} and K.

significantly difficult, which justifies the assumption that the distances between RLs are equal.

In order to know the minimum achievable σ_{RMS} with respect to N_{TDC}, we also performed another simulation. For each N_{TDC}, we obtained the optimal values of τ_{TH} and K with the results of the LMA and used them in each run of simulations. When N_{TDC} is three, σ_{RMS} is 34% lower than that of a BBPD-based DPLL with optimized error-correction gain. As N_{TDC} increases, σ_{RMS} decreases gradually since the quantization process becomes more accurate, reducing $E[\tau_Q^2]$. When N_{TDC} exceeds three, however, the decrease in σ_{RMS} becomes noticeably slower. Increasing N_{TDC} to five and seven results in the reduction of σ_{RMS} by only 4% and 2%, respectively. Therefore, to reduce design complexity and power consumption, N_{TDC} was chosen as three in this work.

In order for the analysis derived in Figures 4-7(a) and (b) to be valid, the PDF of τ_{ERR} in steady state must be Gaussian since the optimal values of τ_{TH}s and K are derived based on the assumption of Gaussian PDF. Reference [38] demonstrates that in a BBPD-based PLL when the loop gain is optimized such that the DPLL generates a minimum jitter, a phenomenon known as "*stochastic resonance*" (SR) occurs, and the input of the BBPD has a Gaussian distribution. The SR phenomenon also occurs in the proposed DPLL; when τ_{TH}s and K are adjusted to values making the DPLL's jitter minimum, τ_{ERR} has a Gaussian distribution. To verify this, we performed simulations to observe the distributions of τ_{ERR} with different values of τ_{TH} and K. To examine the fitness of the distribution of τ_{ERR} to that of Gaussian

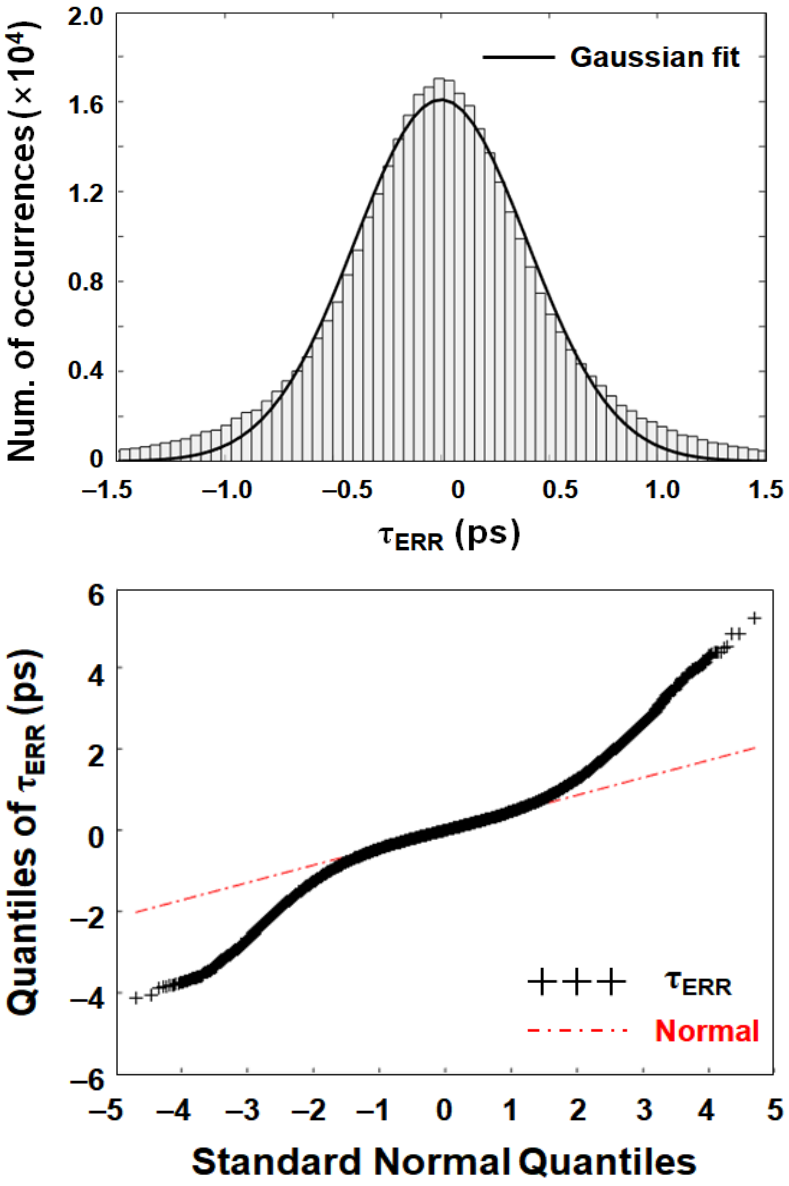


Figure 4-8. Histogram with curve fitted Gaussian PDF and normal Q-Q plot of τ_{ERR}, when $K = K_{OPT}/3$ and $\tau_{TH} = \tau_{TH,OPT}/3$.

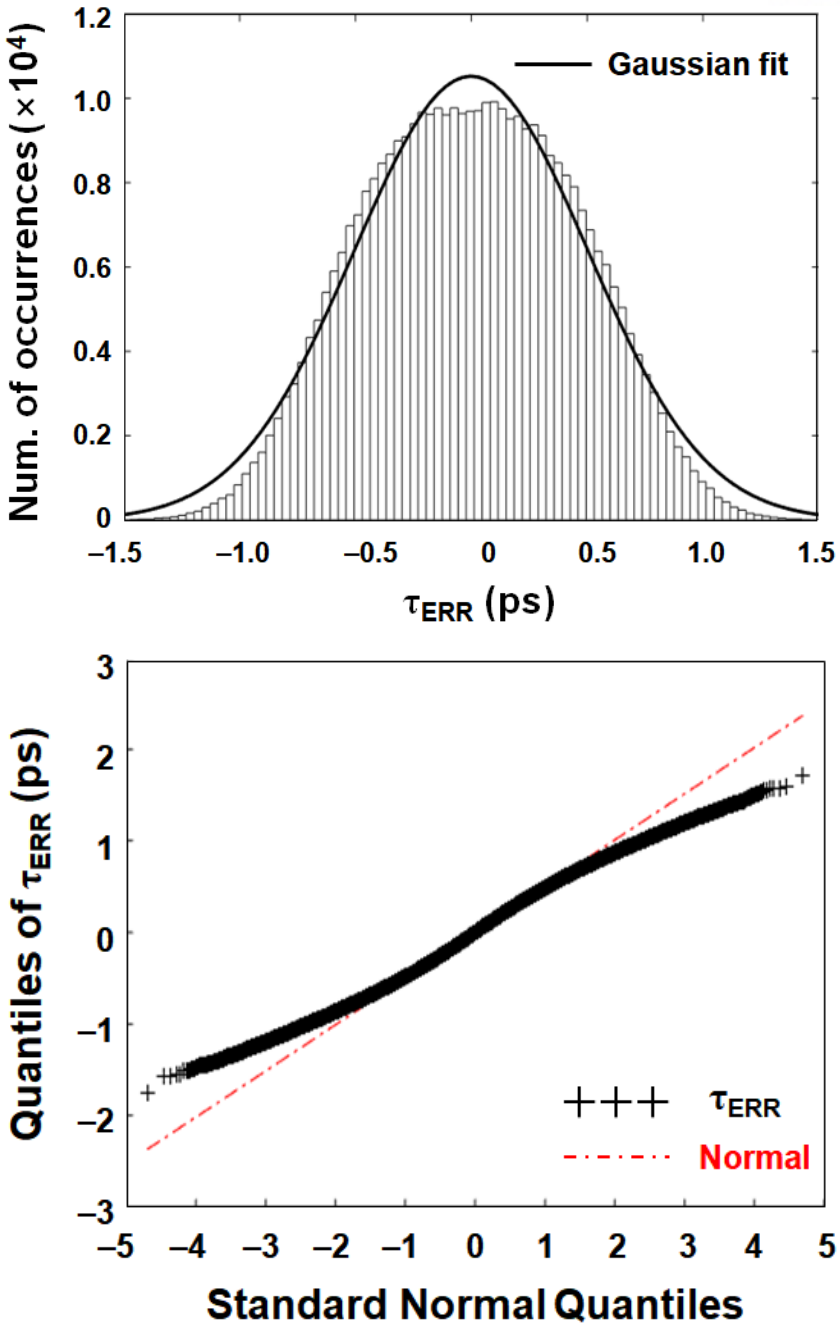


Figure 4-9. Histogram with curve fitted Gaussian PDF and normal Q-Q plot of τ_{ERR}, when K = $3 \cdot K_{OPT}$ and $\tau_{TH} = 3 \cdot \tau_{TH,OPT}$.

distribution, we performed simulations and obtained the histogram and normal quantile-quantile (Q-Q) plots of τ_{ERR} as shown in Figures 4-8 to 4-10. Here, the optimal values of τ_{TH} and K corresponds to $\tau_{TH,OPT}$ (=$0.5\sigma_{ERR}$) and K_{OPT} (= σ_{ERR}), respectively. When both τ_{TH} and K are one-third of the optimal values (Figure 4-8) or three times the optimal values (Figure 4-9), the distribution of τ_{ERR} deviates from the Gaussian. However, when τ_{TH} and K are the optimal values (Figure 4-10)), the distribution of τ_{ERR} is well-matched with a Gaussian one. Thus, the assumption of the Gaussian PDF in τ_{ERR} is valid.

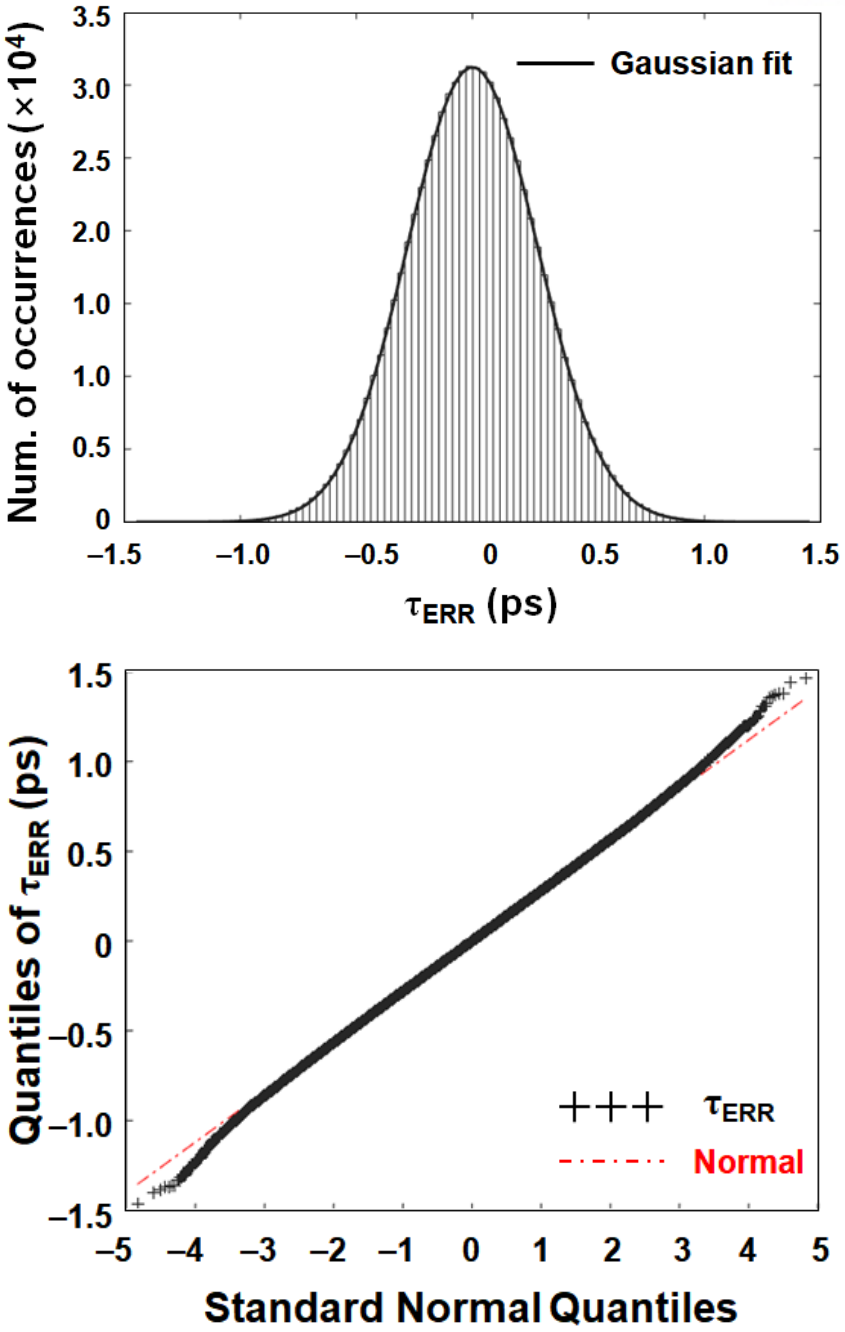


Figure 4-10. Histogram with curve fitted Gaussian PDF and normal Q-Q plot of τERR, when K = K_{OPT} and $\tau_{TH} = \tau_{TH,OPT}$.

In the foregoing analysis from Figures 4-4 to 4-10, it has been assumed that only thermal noise is present in the DCO and that the resultant distribution of τ_{ERR} is Gaussian. However, in practice, the contribution of flicker noise needs to be taken into account as well. Reference [38] also demonstrates that in a circumstance of the SR, timing errors detected by the PD follow a Gaussian distribution even when the superposition of white thermal noise and colored flicker noise is considered in the DCO. As

in [38], for noise analysis of any PLL systems considering the DCO (or VCO) noise, it is generally noted that flicker noise, like thermal noise, follows the Gaussian distribution, even though it is colored rather than white. Similarly in this work, the effect of flicker noise does not compromise the validity of the aforementioned analysis.

4.4. Design and Implementation of the FPEC DPLL Using the OS TDC

4.4.1. Implementation of the FPEC DPLL

Figure 4-11 shows the overall architecture of the proposed FPEC DPLL that includes the OS TDC, the FPEC DLF, a ring DCO, the τ_{TH}-controller, and the K-gain controller. The OS TDC detects a timing error between S_{REF} and S_{DIV} and generates a digital code of D_{TDC}. The following FPEC DLF processes D_{TDC} and controls the DCO through an integral (I-) path and a proportional (P-) path. To avoid the phenomenon of jitter peaking, the I-path gain should be far smaller than that of the P-path. The gain ratio of the P-path to the I-path is thus designed to be 19:1.

In addition, to minimize the degradation of RMS jitter due to latency in the FPEC DLF, the digital codes of the P- and I-paths (D_P and D_I, respectively) are separately applied to the DCO [36]. The FPEC operation is carried out by boosting the P-path gain during a short period time of T_{FPEC}, in accordance with S_{FPEC} generated from the FPEC DLF logic. As analyzed in Chapter 3.4.2, as the duration of T_{FPEC} shortens, the more the phase-realignment mechanism of the PLL resembles that of an ILCM, which offers a lower value of RMS jitter. In the proposed FPEC DPLL, the duration of T_{FPEC} was chosen as one-eighth that of T_{REF}. The OS TDC consists of three pairs of a digital-time converter (DTC) and a D-flip-flop (DFF).

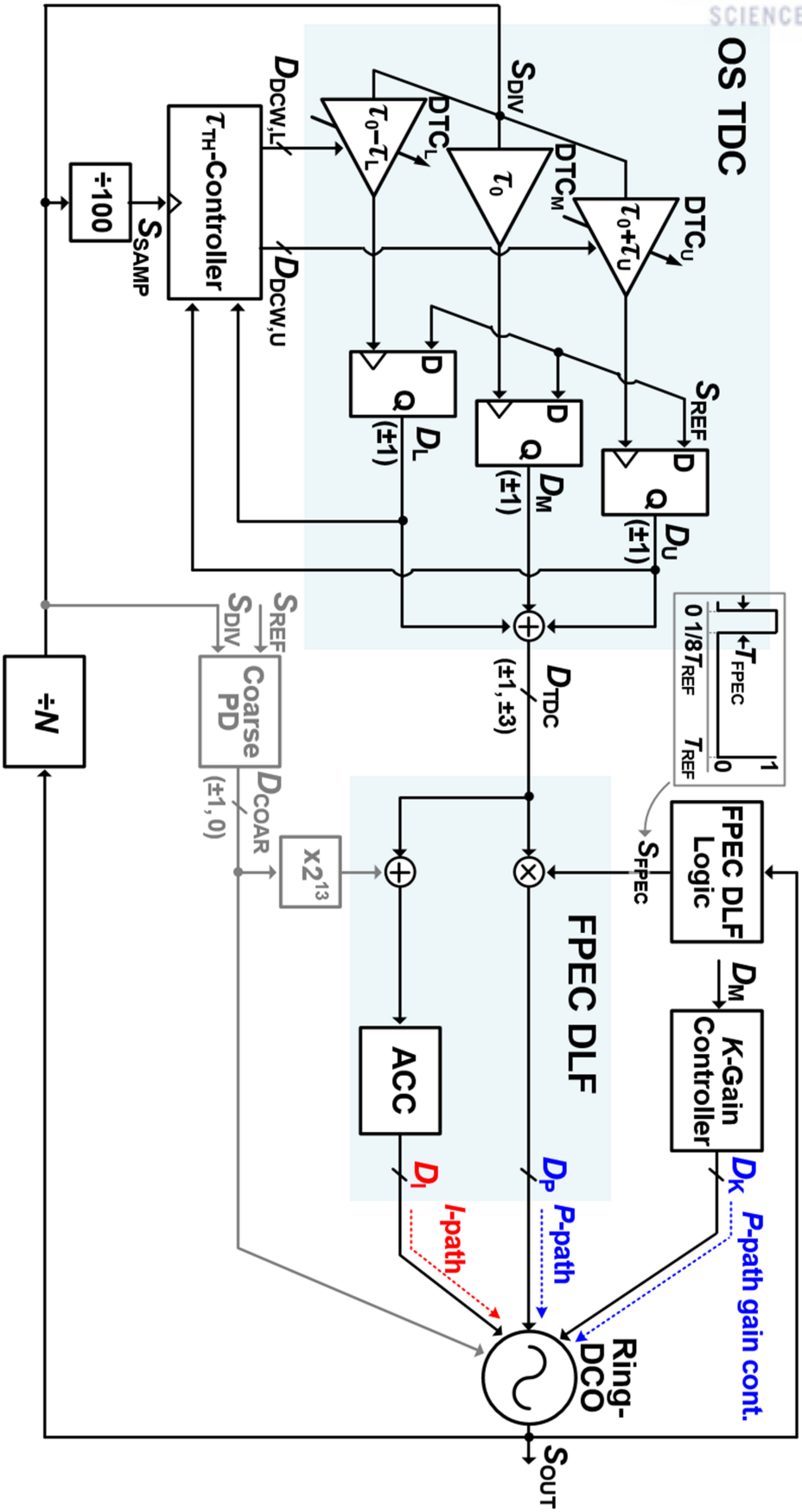


Figure 4-11. Overall architecture of the proposed FPEC DPLL.

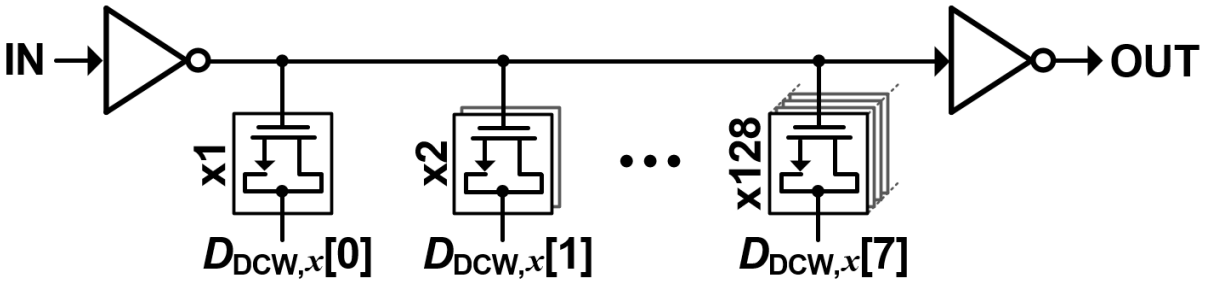


Figure 4-12. Architecture of 8-bit DTC used in the proposed OS TDC.

Figure 4-12 depicts that each DTC consists of two series inverters and 8-bit binary-weighted capacitors. Through the delay control word of DTC_x (x is either U or L), $D_{DCW,x}[7:0]$, the effective load capacitance is changed, and the delay of each DTC is correspondingly adjusted. The capacitance of each bit of the capacitors is determined by the number of identical unit MOS capacitors to improve the linearity. According to the simulation, the maximum differential non-linearity (DNL) of the DTC is 0.04 LSB. In the beginning of the loop operation, upper, middle, and lower DTCs (DTC_U, DTC_M, and DTC_L) are supposed to generate an identical delay of τ_0, as their D_{DCW}s ($D_{DCW,U}$, $D_{DCW,M}$, and $D_{DCW,L}$) are given as the same digital code of '10000000.' As the loop operation begins, τ_{TH}, $D_{DCW,U}$ and $D_{DCW,L}$ are adjusted continuously, while $D_{DCW,M}$ is fixed to the initial digital code. As a result, DTC_U and DTC_L generate positive and negative delays, respectively, relative to the delay generated by DTC_M.

Note that the DTs are determined by these relative delays of DTC_U and DTC_L (i.e., $+\tau_{TH}$ and $-\tau_{TH}$). Ideally, it is not necessary to control $D_{DCW,U}$ and $D_{DCW,L}$ independently to achieve symmetric DTs. However, in practice, local mismatches between the DTCs occur, which causes unpredictable offsets. To address this problem, the τ_{TH}-controller adjusts the positive DT, τ_U, and the negative DT, τ_L independently through $D_{DCW,U}$ and $D_{DCW,L}$. The K-gain controller calibrates the error-correction gain, K. It provides the DCO a digital code of D_K, by which the weighting of D_P is determined. In order to speed up the frequency-acquisition time, the proposed PLL employs an auxiliary coarse PD activated only when the magnitude of τ_{ERR} is significant. For a very large value of τ_{ERR}, its output, D_{COAR}, turns into +1 or –1 from 0, amplified by 2^{13} times, and fed to the I-path's accumulator.

4.4.2. Principle and Implementation of Calibration of τ_U, τ_L, and K

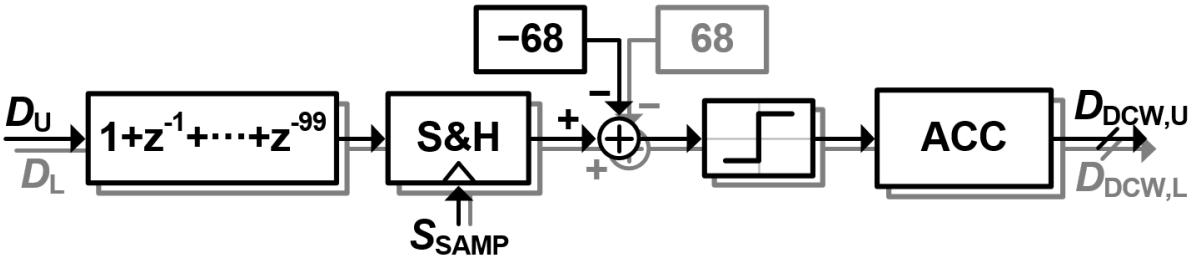


Figure 4-13. Implementations of τ_{TH}-controller.

To achieve the minimum $E[\tau_Q^2]$, the values of τ_U, τ_L, and K are continuously controlled by the τ_{TH}-controller and the K-gain in background. Figure 4- 13 shows the implementation of the τ_{TH}-controller. By comparing the average values of D_U and D_L with the target values, τ_{TH}-controller estimates the deviations of the current values of τ_U and τ_L from the optimal values. After this comparison, it adjusts $D_{DCW,U}$ and $D_{DCW,L}$ to correct the detected deviations. The estimation of the deviation of D_U or D_L, and thus that of τ_U or τ_L, is proceeded by using a 100-tap finite impulse response (FIR) filter and a sample and hold (S&H) circuit. Note that the FIR filter is designed such that all the coefficients are 1. Its output thus corresponds to the sum of 100 consecutive values of D_U or D_L. The S&H circuit samples the FIR filter output at every rising edge of S_{SAMP} having a period of $100T_{REF}$; the output of the S&H circuit thus implies the average of D_U or D_L, (i.e., $E[D_U]$ or $E[D_L]$). As mentioned in Chapter 4.3.1, the PDF of τ_{ERR} in Figure 4-6 (b) can be divided into four areas (i.e., from A_1 to A_4) according to the three DTs (i.e., $-\tau_{TH}$, 0, and $+\tau_{TH}$). Using these, we can calculate the target average values of D_U and D_L, $E[D_U]_{TARG}$ and $E[D_L]_{TARG}$, respectively, as:

$$\begin{aligned} E[D_U]_{TARG} &= (+1)\cdot P(\tau_{ERR} > \tau_U) + (-1)\cdot P(\tau_{ERR} < \tau_U) \\ &= A_4 - (A_3 + A_2 + A_1) \\ &= 0.16 - (0.68 + 0.16) = -0.68 \end{aligned} \tag{4.1}$$

and

$$\begin{aligned} E[D_L]_{TARG} &= (+1)\cdot P(\tau_{ERR} > -\tau_L) + (-1)\cdot P(\tau_{ERR} < -\tau_L) \\ &= (A_2 + A_3 + A_4) - A_1 \\ &= (0.34 + 0.34 + 0.16) - 0.16 = 0.68. \end{aligned} \tag{4.2}$$

The deviation of τ_U can thus be estimated by comparing the S&H circuit output with -68 according to (4.1), whereas that of τ_L can be estimated by comparing the S&H circuit output with 68 according to (4.2). Finally, the polarity information of these deviations is added to the following accumulators, and $D_{DCW,U}$ and $D_{DCW,L}$ are adjusted to calibrate τ_U and τ_L, respectively.

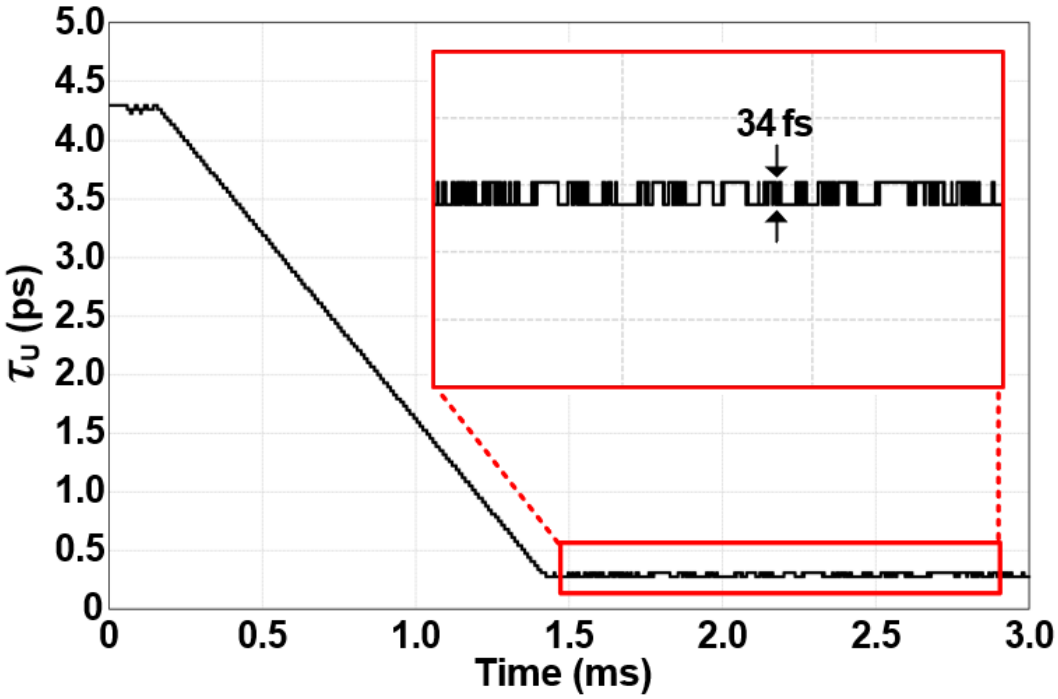


Figure 4-14. Transient behavior of time threshold of the upper path (τ_U) of the OS TDC.

Even in a steady state, the values of τ_U and τ_L are slightly toggled, since τ_{TH}-controller continuously operate in the background. However, as the bandwidth of the τ_{TH}-calibrator is set far narrower than that the PLL loop bandwidth, the fluctuations in τ_U and τ_L have a small influence on the performance of the proposed DPLL. To verify this, we performed transient simulations of the time threshold of the upper path (τ_U in Figure 4-11) of the OS TDC with respect to the middle path. As shown in Figure 4-14, in the steady state, τ_U was toggled by an amount corresponding to only 1-LSB control word of the DTC, which is 34 fs (the way in which the resolution was chosen will be detailed in Chapter 4.4.3). This effect of the continuous calibration corresponds to only 1%-degradation of RMS jitter, when it is compared to the case in which τ_{TH}s (as well as K) are fixed at an optimal value.

Figure 4-15 shows a block diagram of the K-gain controller, which is composed of an accumulator and a logic investigating an autocorrelation. If K is set too large, the amount of the error correction

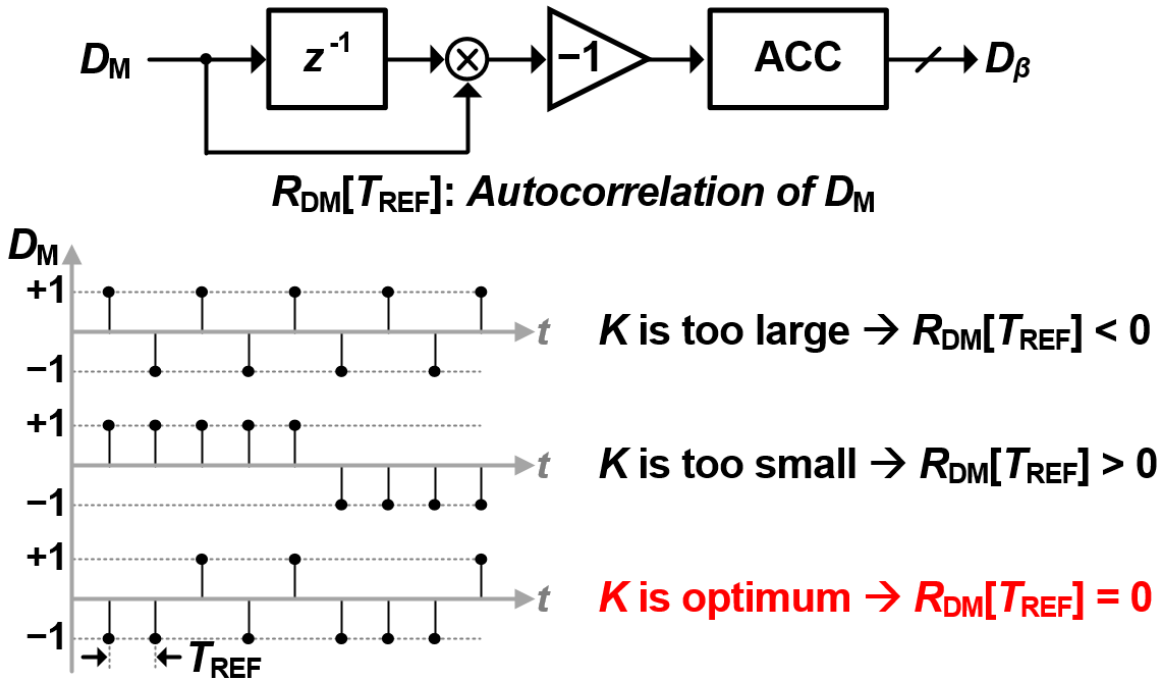


Figure 4-15. Implementations of *K*-gain controller.

becomes excessive, which makes D_M toggle frequently. In this case, the autocorrelation of D_M with respect to T_{REF}, $R_{DM}[T_{REF}]$ becomes negative. In contrast, if K is set too small, the amount of the error correction becomes insufficient, and D_M shows a pattern of repeating +1s or –1s over several T_{REF}s, which results in $R_{DM}[T_{REF}] > 0$. Thus, from these observations, the K-gain controller adjusts D_K to achieve the condition of $R_{DM}[T_{REF}] = 0$, and in this condition, K becomes the optimum [36], [38]–[41].

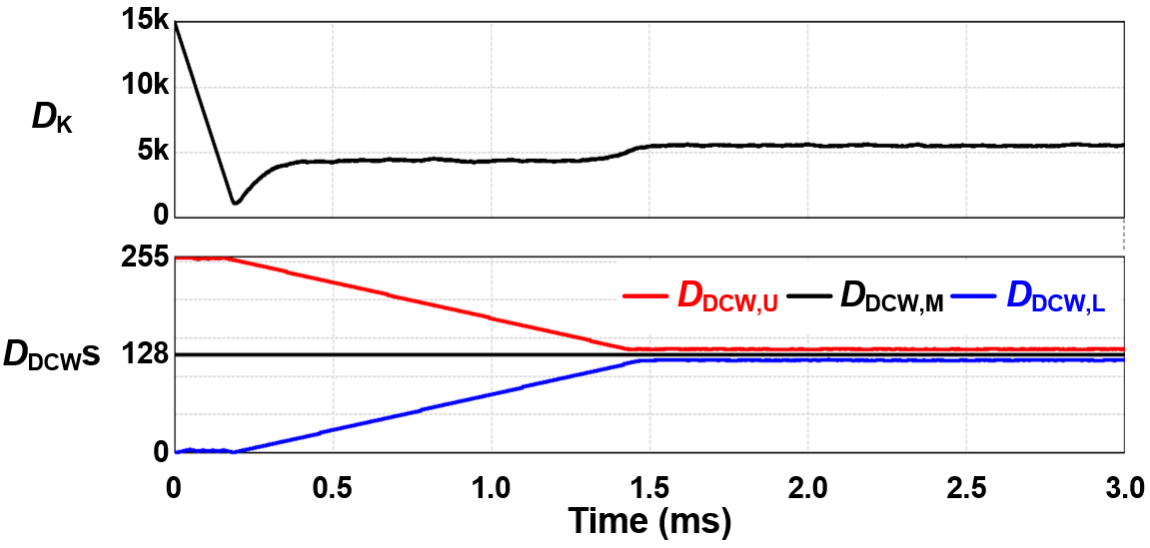


Figure 4-16. Settling behavior of D_K and D_{DCW}s.

In the convergence process, the two digital calibrators are not totally independent, but they actually affect each other. However, because we designed the *K*-gain calibrator to have far wider than that of the τ_{TH}-calibrator, their convergence can be guaranteed with no stability issue. We performed transient simulations to verify their stable operations, as shown in Figure 4-16. In this simulation, to evaluate the worst-case (or the longest) settling time, all initial values of digital codes were set to start from their extreme corners, i.e., the maximum or the minimum values in their ranges. That is, D_K and $D_{DCW,U}$ started from their maximum values, while $D_{DCW,L}$ and D_I from their minimum. As shown in Figure 4-16, since the *K*-gain calibrator has a much wider bandwidth than τ_{TH} calibrator, the value of D_K changed much faster initially and tracked the changes in the values of D_{DCW}s. Finally, the two loops, and thus the values, of D_K and D_{DCW}s were settled within 1.5 ms.

4.4.3. Design and Implementation of DTCs of the OS TDC

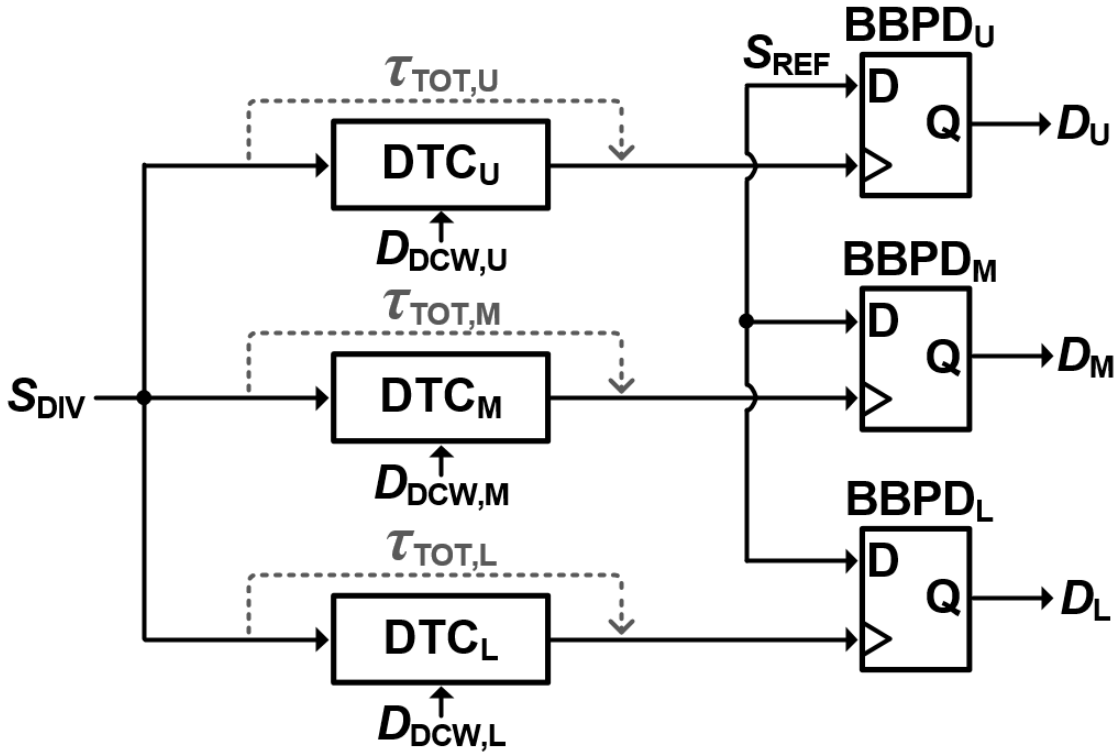
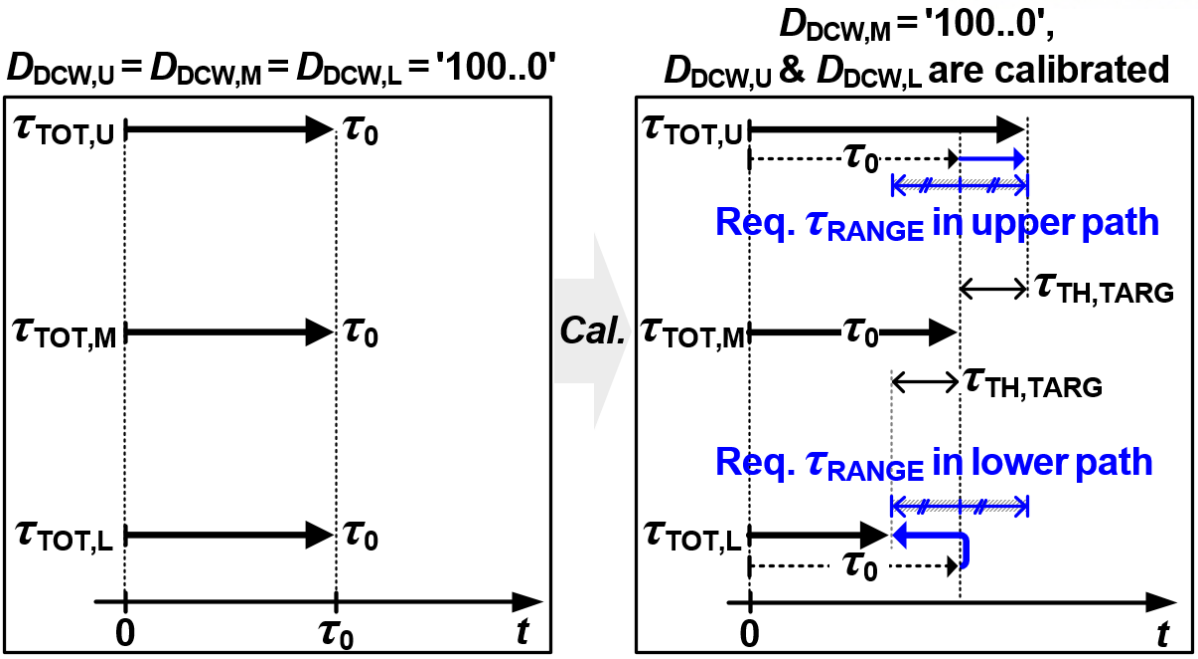


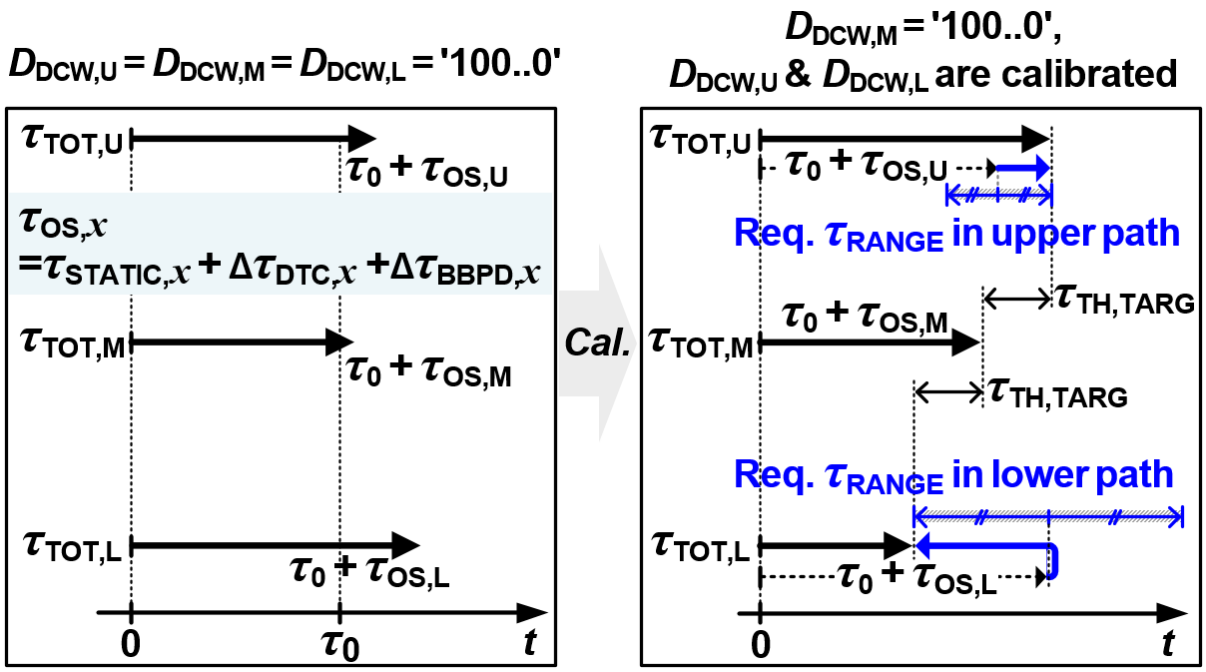
Figure 4-17. Implementation of the OS TDC.

Figure 4-17 shows the block diagram of the OS TDC, consisting of three identical pairs of the DTC and the BBPD. The relative delay difference between the three paths determines the DTs of the OS TDC. In Figure 4-17, $\tau_{TOT,x}$ (x can be U, M, or L) denotes the total delay of each path, and it is adjusted by changing the effective load capacitance of DTC$_x$ in accordance with $D_{DCW,x}$. In the ideal case where no mismatches are present in the three paths, all $\tau_{TOT,x}$s are identical to τ_0, when all $D_{DCW,x}$s are given as the median value of '100…0' (see Figure 4-18(a)). In this case, to make the relative delays between the three paths equal to the target threshold (or $\tau_{TH,TARG}$), we need to adjust $\tau_{TOT,U}$ and $\tau_{TOT,L}$ to $\tau_0 + \tau_{TH,TARG}$ and $\tau_0 - \tau_{TH,TARG}$, respectively, while fixing $\tau_{TOT,M}$ to τ_0. The dynamic range of DTCs, τ_{RANGE}, is required to cover the range of more than $2\tau_{TH,TARG}$.

In practice, however, due to local mismatches between the DTCs, random time offsets are present in $\tau_{TOT,x}$s. Figure 4-18 (b) shows this case where $\tau_{TOT,x}$s differ from τ_0 due to a time offset of each path, $\tau_{OS,x}$, which is the sum of $\tau_{STATIC,x}$, $\Delta\tau_{DTC,x}$ and $\Delta\tau_{BBPD,x}$ even when all D_{DCW}s are provided as the median value. Here, $\tau_{STATIC,x}$ denotes a static delay that occurs due to asymmetric clock and power routings in the layout. $\Delta\tau_{DTC,x}$ and $\Delta\tau_{BBPD,x}$ represent randomly given delays due to local process variations of DTC$_x$ and BBPD$_x$, respectively. Since $\Delta\tau_{DTC,x}$ and $\Delta\tau_{BBPD,x}$ are random variables, they are unpredictable, but



(a)



(b)

Figure 4-18. Required DTC range in (a) the ideal case; (b) the real situation, where local mismatches are present.

the standard deviation is identical in all three paths and can be obtained through Monte Carlo simulations. In consideration with the effect of $\tau_{OS,x}$, the required τ_{RANGE} for each path differs from the

ideal case in Figure 4-18(a). As shown in the case of Figure 4-18 (b), when $\tau_{OS,x}$ is taken into account, we can see that the required τ_{RANGE} is different for the upper path ($< 2\tau_{TH,TARG}$) and the lower path ($> 2\tau_{TH,TARG}$).

To ensure that the OS TDC's DTs are adjusted to the target values, we must design τ_{RANGE} of the upper and lower paths so that the following conditions are satisfied:

$$\tau_0 + \tau_{OS,U} - \frac{1}{2}\tau_{RANGE} \le \tau_0 + \tau_{OS,M} + \tau_{TH,TARG} \le \tau_0 + \tau_{OS,U} + \frac{1}{2}\tau_{RANGE} \quad (4.3)$$

$$\tau_0 + \tau_{OS,L} - \frac{1}{2}\tau_{RANGE} \le \tau_0 + \tau_{OS,M} - \tau_{TH,TARG} \le \tau_0 + \tau_{OS,L} + \frac{1}{2}\tau_{RANGE}, \quad (4.4)$$

Since the three DTCs are designed to be identical, τ_{RANGE} of each path must comply with (4.3) and (4.4) even in the worst case (i.e., $\tau_{OS,U}$ and $\tau_{OS,L}$ are much smaller and larger than τ_0). From the post-layout simulations, $\tau_{STATIC,U} - \tau_{STATIC,M}$ and $\tau_{STATIC,L} - \tau_{STATIC,M}$ were obtained as –1.65 and –1.60 ps, respectively. The standard deviation of $\Delta\tau_{BBPD,x}$, $\sigma_{\Delta\tau_{BBPD}}$ was calculated to be 230 fs from Monte Carlo simulations. The magnitude of τ_{RANGE} and the standard deviation of $\Delta\tau_{DTC,x}$, $\sigma_{\Delta\tau_{DTC}}$, and they are correlated with each other since $\sigma_{\Delta\tau_{DTC}}$ increases in proportion to τ_{RANGE}; they therefore need to be considered together when calculating (4.3) and (4.4).

To obtain the value of the minimum required τ_{RANGE}, we performed an iterative method. First, a DTC was designed without consideration of (4.3) and (4.4). Second, according to Monte Carlo simulations based on a given DTC design that gives a specific value of τ_{RANGE}, $\sigma_{\Delta\tau_{DTC}}$was obtained. Third, a random sample of $\Delta\tau_{DTC,x}$ and of $\Delta\tau_{BBPD,x}$ were generated from given $\sigma_{\Delta\tau_{DTC}}$ and $\sigma_{\Delta\tau_{BBPD}}$, and a number of simulations (100k runs) were performed to check whether the conditions of (4.3) and (4.4) were met. Our goal was to achieve the success rate of the calibration at least 99.7%. When it was failed, we modified the DTC to increase τ_{RANGE} and restarted the above process. As τ_{RANGE} increases, so does $\sigma_{\Delta\tau_{DTC}}$, but the rate of increase is much faster in the calibration success rate. Finally, we designed τ_{RANGE} to be 8.6 ps because it provided a 99.7% success rate. The number of bits of the DTC was 8, so the resolution is 34 fs.

4.4.4. Implementation of the Ring DCO

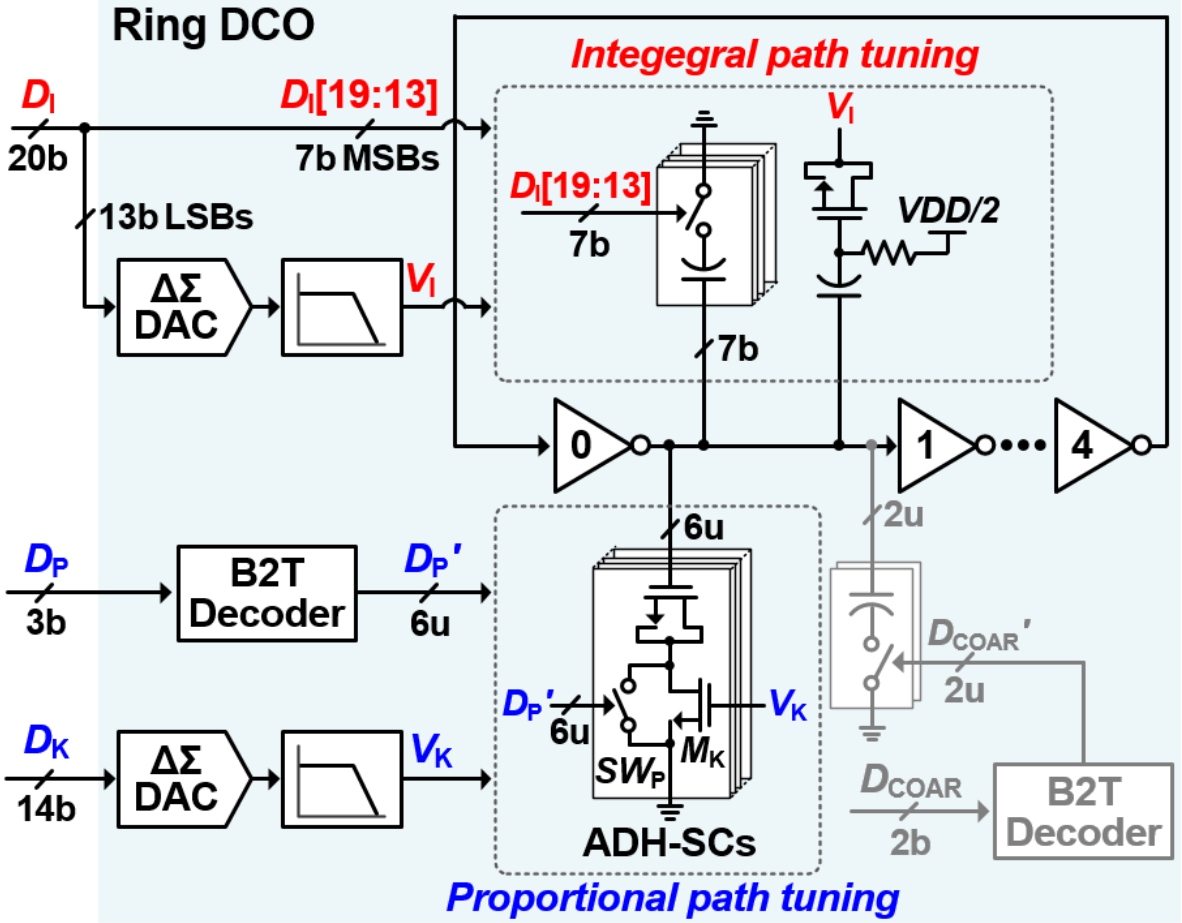


Figure 4-19. Ring DCO schematic.

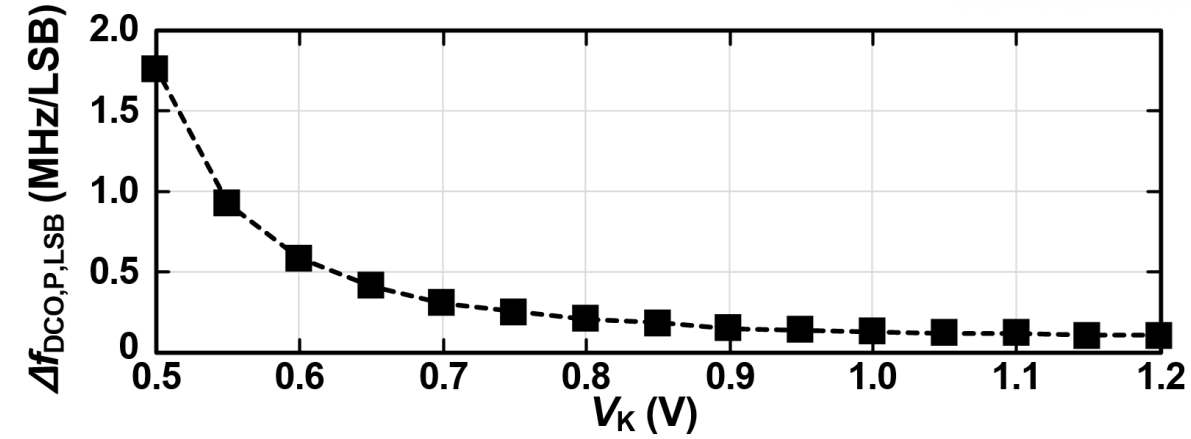
The implementation of the ring DCO in this work is based on five-stage inverters, as shown in Figure 4-19. For the signals of D_P and D_I, the effective load capacitance of the output of each stage is determined, which allows the DPLL to adjust the DCO's frequency, f_{DCO}. The 7 MSBs of D_I, D_I[19:13], control a bank of 7-bit binary-weighted capacitors that provide a tuning range from 2.30 to 2.55 GHz. The 13 LSBs of D_I, D_I[12:0], are converted to V_I through a delta-sigma digital-to-analog converter (ΔΣDAC) and an RC filter. With NMOS varactors controlled by V_I, f_{DCO} can be adjusted to a resolution of 1.5 kHz/LSB within 10 MHz. The ΔΣDAC is composed of a MASH 1-1 ΔΣ-modulator of which clocking frequency is 75 MHz (i.e., f_{REF}) and a 5-bit resistor DAC (RDAC). The subsequent low-pass filter consists of two cascaded RC networks having the same resistance and capacitance, which are 32

kΩ and 2.54 pF, respectively, to configure a 2nd-order RC low-pass filter. Since the capacitors are designed to be large, the low-pass filter's thermal noise itself is sufficiently suppressed and its impact on the overall jitter performance becomes negligible.

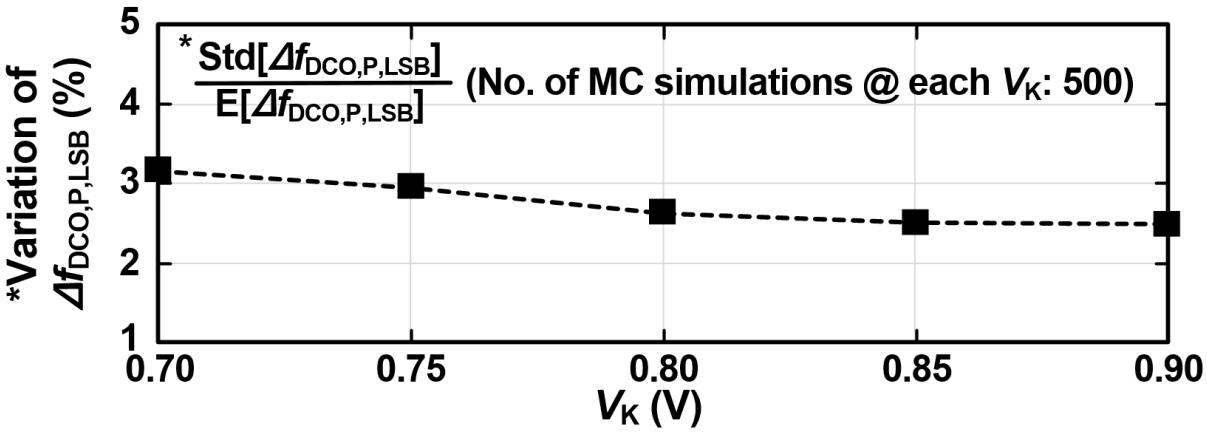
To apply the change in D_P to the DCO quickly and adjust its weighting through D_K accurately, the *P*-path tuning and the *K*-gain control are performed through analog-digital-hybrid switched capacitors (ADH-SCs), as shown in Figure 4-19. The unit cell of ADH-SCs is composed of an NMOS capacitor, a switch, SW_P, and a resistively-degenerating NMOS, M_K. The ADH-SCs were implemented with identical six-unit cells rather than binary-sized cells to minimize the mismatch effect on nonlinearities in tuning characteristics. For the *P*-path tuning, the 3-bit binary code of D_P is decoded into a 6-bit thermometer code of D_P', by the binary-to-thermometer (B2T) decoder. By D_P', SW_Ps in the ADH-SCs are turned on and off. In this operation, since D_P' immediately changes ADH-SCs' capacitance, the loop can remove τ_{ERR} right after updating D_P' with minimal delay. The *K*-gain can be controlled through M_Ks that determine the weighting of D_P'. Their gates are connected with V_K that is converted from D_K. When V_K is set low, M_K forms a high impedance underneath the NMOS capacitor. In this case, the amount of capacitance effectively changing in the unit cell of the ADH-SCs, ΔC, increases, which means the *K*-gain becomes large. In contrast, when V_K is set high, the impedance due to M_K becomes small, thereby making ΔC and the *K*-gain small. As a result, with the ADH-SCs, it is possible to quickly remove τ_{ERR} with minimal latency while precisely controlling *K*-gain. The pair of ΔΣDAC and the low-pass filter are designed identically to those used in *I*-path. The quantization noise from the ΔΣDAC on this path could cause the deviation of *K* from the optimal value. According to calculation, the value of *K* is deviated by 0.12% from the optimal value, by which the RMS jitter of the DPLL is degraded by less than 0.1%.

To ensure that the ADH-SCs operate robustly, the following two points must be ensured in their tuning characteristics. Firstly, according to the change in V_K, the variation of f_{DCO} corresponding to the change in one LSB of D_P, $\Delta f_{DCO,P,LSB}$, must be monotonous. As shown in the simulation results in Figure 4-20(a), $\Delta f_{DCO,P,LSB}$ exhibits a monotonous decrease as V_K changes from 0.5 to 1.2 V. The rate of change in $\Delta f_{DCO,P,LSB}$ is inversely proportional to V_K, but this is not problematic because V_K can be adjusted to a sufficiently high resolution by the ΔΣDAC. Secondly, for a given value of V_K, each SW_P in the ADH-SCs in Figure 4-19 should have the same amount effect on $\Delta f_{DCO,P,LSB}$ when it is turned on and off. Otherwise, nonlinearities in the *P*-path tuning increase, which could degrade jitter performance.

In order to quantify this effect of the nonlinearities, we performed Monte Carlo simulations on $\Delta f_{DCO,P,LSB}$ of the ADH-SCs. Figure 4-20(b) shows the simulation results of the variations in $\Delta f_{DCO,P,LSB}$



(a)

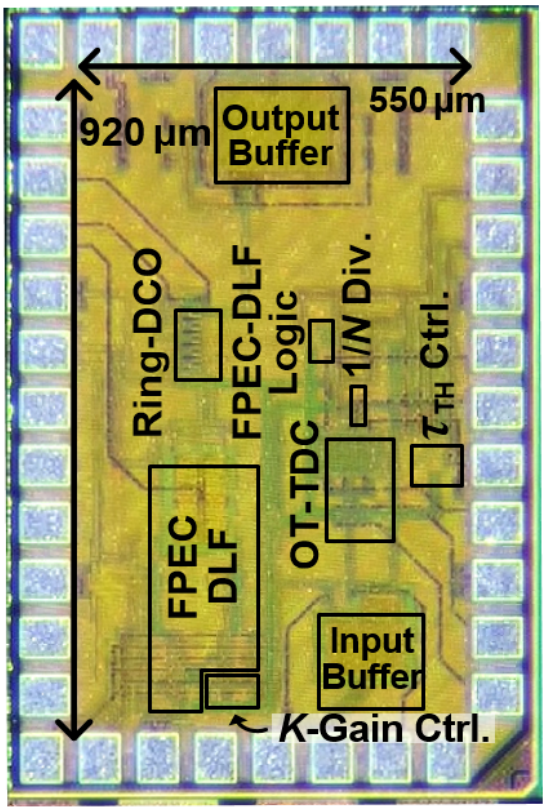


(b)

Figure 4-20. (a) Change of f_{DCO} by the one LSB of D_P, $\Delta f_{DCO,P,LSB}$, across V_K; (b) change of $\Delta f_{DCO,P,LSB}$ across V_K.

for V_K between 0.7 and 0.9 V. As we can see, the magnitude of the variation at V_K of 0.7 V has a larger value than the others. At this value of V_K, the ratio of the standard deviation of $\Delta f_{DCO,P,LSB}$, Std[$\Delta f_{DCO,P,LSB}$], to its average value, E[$\Delta f_{DCO,P,LSB}$], was 3.2%. We then performed a number of behavioral simulations (120 k runs) using the model of Figure 4-7(a). In each run, we considered the effect of mismatches on the *P*-path tuning based on the aforementioned value of variations in $\Delta f_{DCO,P,LSB}$, and evaluated RMS jitter. The simulation results showed that the difference between the three-sigma value of the RMS jitter and the nominal value is less than 1%, which implies the potential nonlinearities present in the ADH-SCs has a negligible effect on the RMS jitter. For the coarse tuning that is enabled when a large τ_{ERR} occurs, the B2T decoder converts D_{COAR} into a 2-bit thermometer code of D_{COAR}' by which the two unary-weighted capacitors are controlled. According to 1-LSB change in D_{COAR}, f_{DCO} changes by 32 MHz.

4.5. Measurement Results



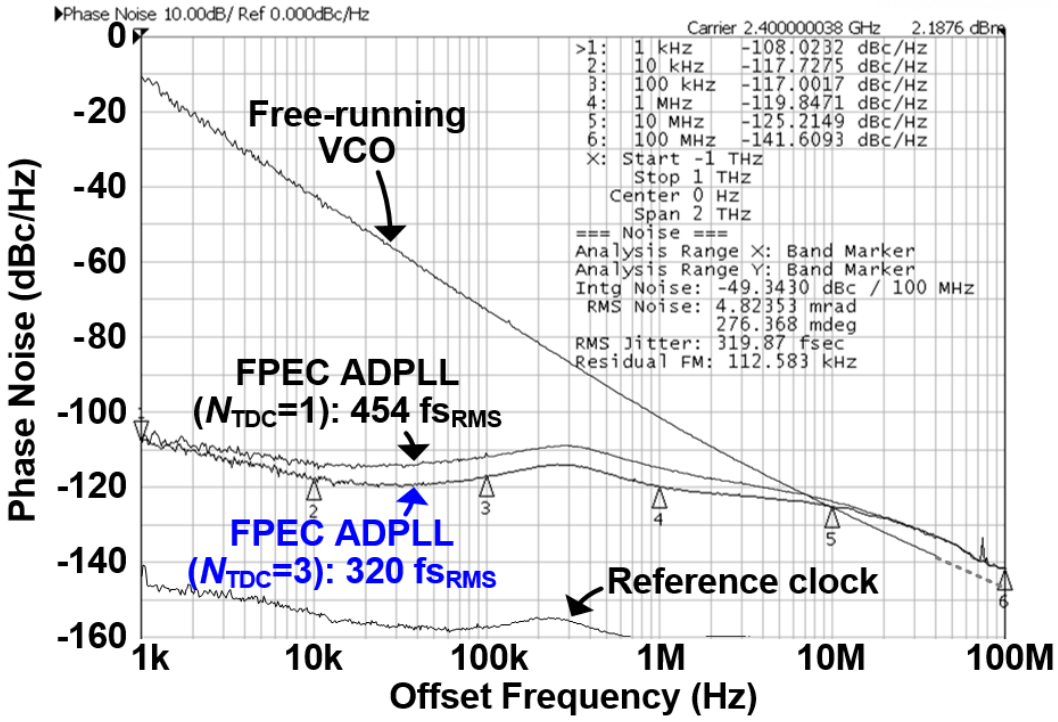
Power Consumption (mW)	
DCO	5.16
Divider	0.30
FPEC DLF + *K*-Gain Controller + FPEC-DLF Logic	0.47
OT-TDC + τ_{TH}-controller	0.07
Total	6.00

(a) (b)

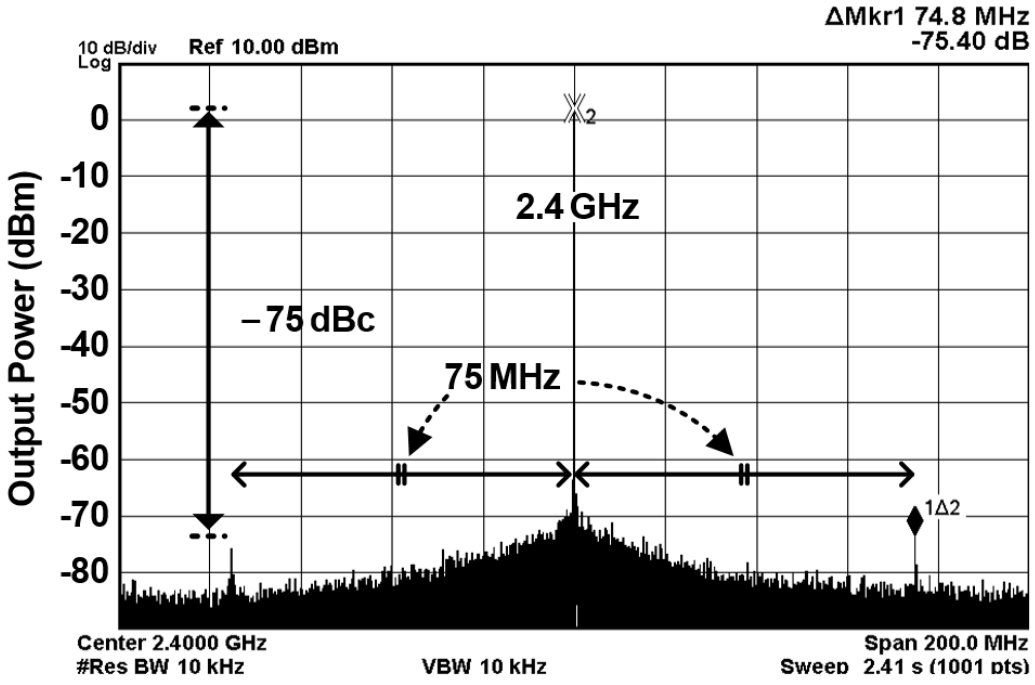
Figure 4-21. (a) Die micrograph; (b) power-breakdown table

The proposed DPLL fabricated in 65-nm CMOS technology occupies an active area of 0.055 mm^2, as shown in Figure 4-21(a). The total power consumption was 6.0mW from a supply voltage of 1.2 V, as shown in Figure 4-21(b). We used Keysight E5052B (signal source analyzer) and Keysight N9030A (spectrum analyzer) to measure phase noises and spectrums, respectively. The performance of the ring DCO in the proposed DPLL is susceptible to supply noise since it is implemented with a single-ended topology. To measure the proposed DPLL's performances while minimizing the effect of supply noise, we thus used a power supply of Keysight E3631A, which has a very low-noise performance.

Figures 4-22(a) and (b) show the measured phase noise and spectrum of the output signal with the frequency of 2.4 GHz (f_{REF} = 75 MHz), respectively. We can see that a very wide bandwidth (almost 20 MHz) was achieved by using the FPEC technique, as shown in Figure 4-22 (a); thus, low phase noise



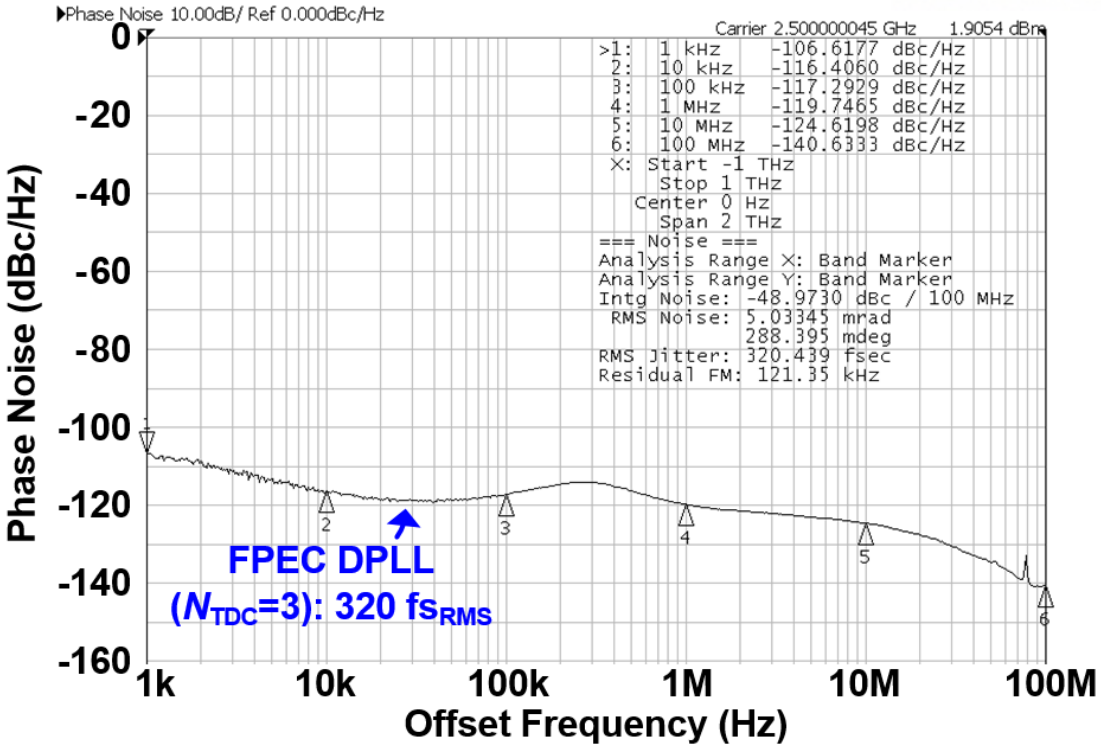
(a)



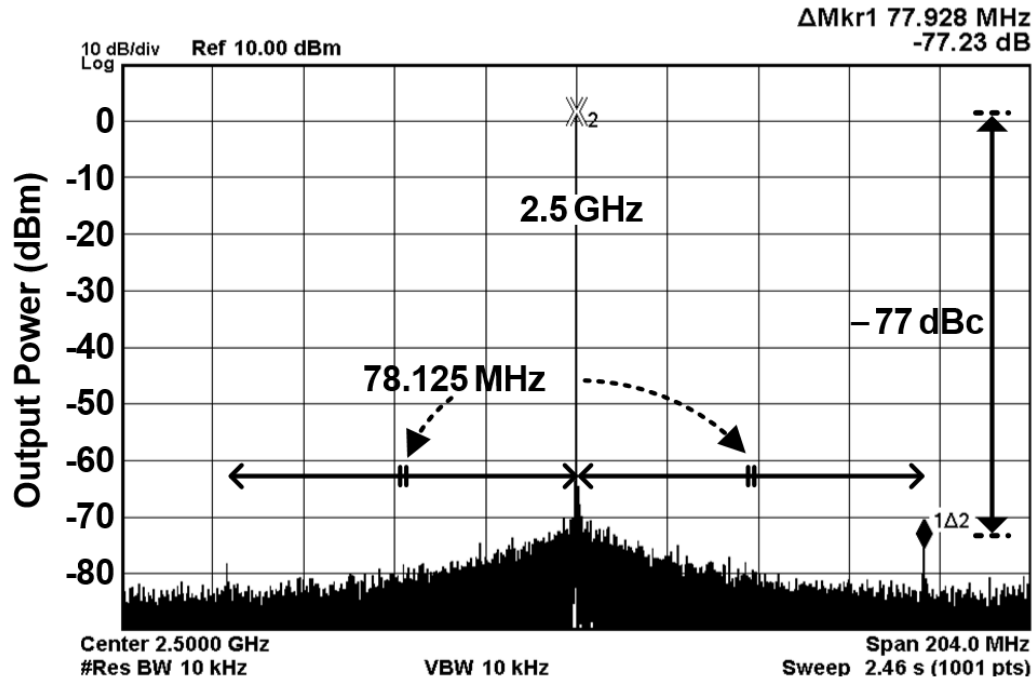
(b)

Figure 4-22. Measured (a) phase noise and (b) spectrum of the output signal with the frequency of 2.4 GHz (f_{REF} = 75 MHz).

and RMS jitter were achieved. According to N_{TDC}, the proposed FPEC DPLL exhibits very different noise performances. When the FPEC DPLL operated in a mode with N_{TDC} set to one, in which only the



(a)



(b)

Figure 4-23. Measured (a) phase noise and (b) spectrum of the output signal with the frequency of 2.5GHz (f_{REF} = 78.125 MHz).

middle DTC and DFF in the OS TDC are enabled, the RMS jitter and the 100-kHz phase noise and were 454 fs and –112 dBc/Hz, respectively. On the other hand, with N_{TDC} set to three where the OS

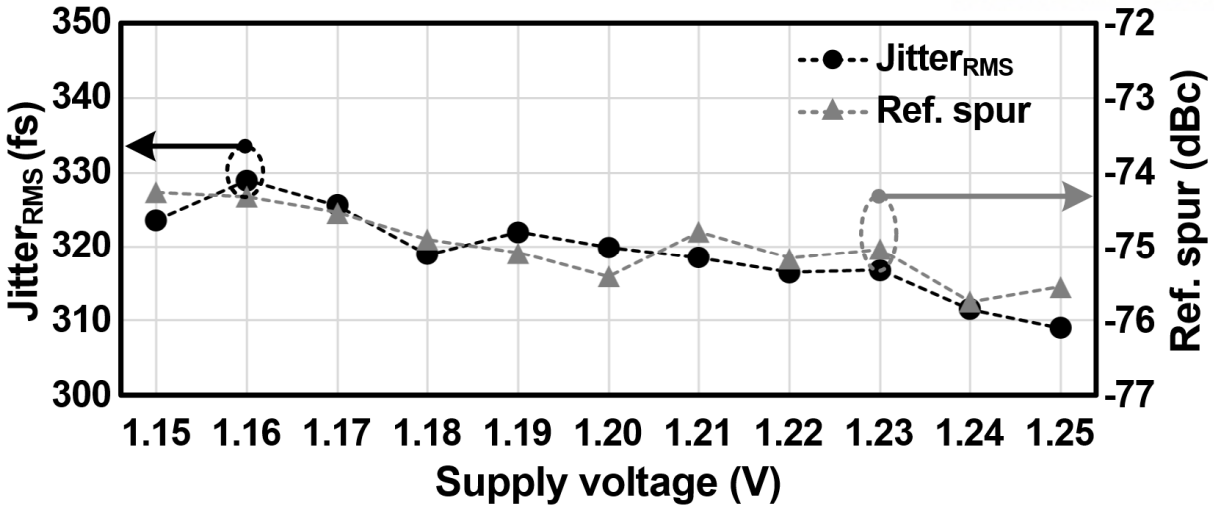


Figure 4-24. Jitter$_{RMS}$ and level of reference spur across when the supply voltage changes from 1.15 to 1.25V.

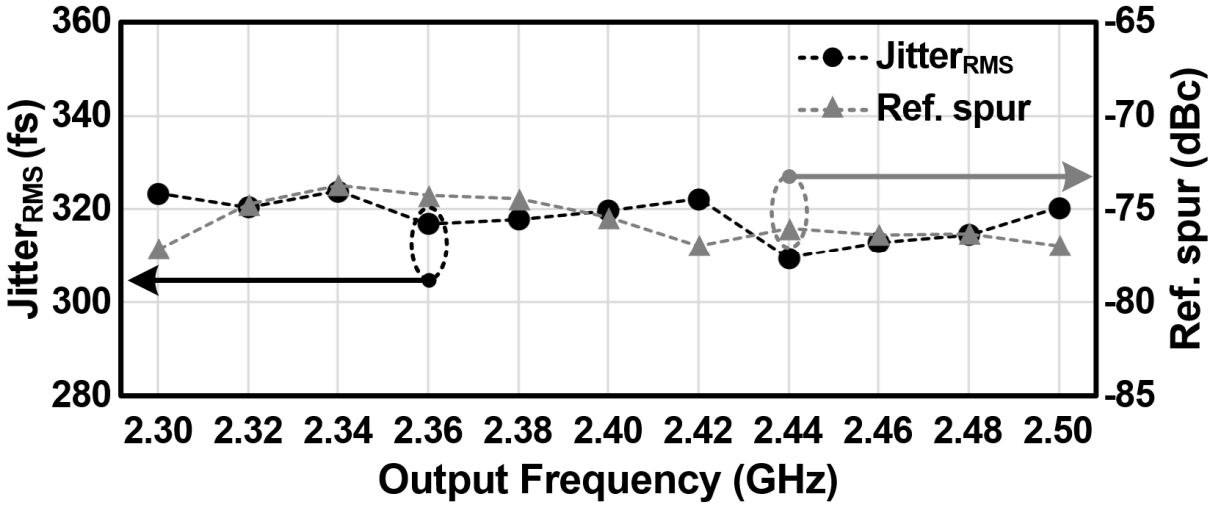


Figure 4-25. Jitter$_{RMS}$ and level of reference spur when f_{OUT} changes from 2.30 to 2.50 GHz with a different f_{REF}.

TDC is completely functional, the RMS jitter and the phase noise at the same offset were significantly improved to 320 fs and –117 dBc, respectively. From these, we can say that the proposed DPLL can effectively reduce the quantization error present in the loop by using the OS TDC, thereby achieving low RMS jitter. The measured spectrum of the proposed FPEC DPLL is at 2.4 GHz is shown in Figure 4-22(b). The reference spur of the proposed DPLL at the 75 MHz was –75 dBc. The phase noise and spectrum were measured at another output frequency of 2.5 GHz, as shown in Figures 4-23(a) and (b), respectively. The RMS jitter and the phase noise at the 1-MHz offset were 321 fs and –119 dBc/Hz, respectively. At the 78.125-MHz offset, the level of the reference spur was measured as –77 dBc.

When τ_{TH}s and K are calibrated to the proper values in the proposed FPEC DPLL, the output of the OS TDC, as well as the detected τ_{ERR}, show a random pattern. In this case, the phase of the DCO does not experience any periodic disturbances, so the proposed DPLL is expected to achieve a very low reference spur (far lower than the measured ones) systematically. It is thus suspected that the effects of nonidealities, such as coupling with the reference clock buffer operating at f_{REF} through substrate or power lines, are limiting factors preventing further reference spurs from further decreasing.

We measured the RMS jitter and the level of reference spur across supply voltage to check how robust the performances of the digital calibrators are. As shown in Figure 4-24, the variations in reference spur and RMS jitter were restricted to less than 2 dB and 40 fs, respectively, over the variations in supply voltage changing from 1.15 to1.25V. Figure 4-25 shows the changes of the level of reference spur and RMS jitter across the output frequency, f_{OUT}. The degradations of reference spur and RMS jitter were restricted to less than 5 dB and 40 fs, respectively, over the variations in f_{OUT} from 2.3 to 2.5GHz. The measurement results of Figures 4-24 and 4-25 imply that the digital calibrators operating continuously in the background maintain the OS TDC's time thresholds and the loop's error-correction gain to be optimum despite the variations in the supply voltage and f_{OUT}.

Table 4-I shows the performance comparison with recent ring-oscillator-based clock generators. The proposed FPEC DPLL achieves excellent performances of RMS jitter, $\mathrm{FOM_{JIT}}$, and $\mathrm{FOM_{JIT,N}}$, in which the effect of N is considered in the calculation of $\mathrm{FOM_{JIT}}$. Also, the level of reference spurs of this work is lower than the other architectures in Table 4-I. Table 4-II shows the performance comparison with prior-art DPLLs [43]–[47]. As shown in Table 4-II, superior performances of RMS jitter, $\mathrm{FOM_{JIT}}$, and $\mathrm{FOM_{JIT,N}}$ than other ring-oscillator-based DPLLs [43]–[45] were achieved in the proposed FPEC DPLL, and these three performances are comparable to those of LC-oscillator-based DPLLs [46], [47].

Figure 4-26(a) shows the performance comparison with prior ring-oscillator-based clock generators in terms of the level of reference spur and $\mathrm{FOM_{JIT}}$. We can see that the proposed FPEC DPLL achieves excellent performances of RMS jitter and level of reference spur concurrently. Compared to the state-of-the-art DPLLs in Figure 4-26(b), the proposed FPEC DPLL achieves superior $\mathrm{FOM_{JIT}}$.

Table 4-I. Comparison with some of state-of-the-art ring-oscillator-based integer-N clock generators ($N > 15$).

Reference	This Work	JSSC'18 [28]	JSSC'16 [21]	TCAS-I'18 [20]	ISSCC'18 [17]	VLSI'18 [36]
Technology	65nm	65nm	65nm	14nm	65nm	7nm
Architecture	FPEC DPLL	Analog FPEC PLL	SLF PLL	SLF PLL	ILCM	IL PLL
Loop BW calibration	Y	N	N	Y	N	N
f_{OUT} (GHz)	2.4	3.008	2.4 (2.0 – 3.0)	4.0 (0.8 – 4.0)	4.752 (2.6 – 5.2)	4.0 (0.48 – 4)
f_{REF} (MHz)	75	47	22.6	100	54	250 (30 – 250)
Multi. factor (N)	32	64	106 (88 – 133)	40 (8 – 125)	88 (48 – 96)	16
Area (mm^2)	0.055	0.047	0.015	0.021	0.16	0.018
1MHz PN (dBc/Hz) @f_{OUT} (GHz)	–119.8 @ 2.4	–121.6 @ 3.008	–113.8 @ 2.4	–112 @ 4.0	–113.7 @ 4.752	–118.8 @ 4.0
$Jitter_{RMS}$ (fs)	320 (1k – 100M)	357 (1k – 80M)	970 (1k – 200M)	1588 (100k – 1G)	366 (10k – 30M)	427 (100k – 1G)
Reference spur (dBc)	–75	–71	–65	N/A	–53	–61
Power (mW)	6.0	4.6	4.0	2.6	6.5	6.3
FOM_{JIT} (dB)*	–242.1	–242.3	–234.1	–231.9	–240.6	–239.4
$FOM_{JIT,N}$ (dB)**	–257.1	–260.4	–254.4	–247.9	–260.0	–251.4

Table 4-II. Comparison with state-of-the-art DPLLs.

Reference	This Work	JSSC'18 [43]	ISSCC'16 [44]	JSSC'16 [45]	JSSC'17 [46]	JSSC'11 [47]
Technology	65nm	28nm	40nm	65nm	40nm	65nm
DPLL Architecture	FPEC & OT TDC Int-*N*	BBPD Int-*N*	BBPD Int-*N*	DTC & TA-TDC Frac-*N*	DTC & ΔΣ-TDC Frac-*N*	DTC & BBPD Frac-*N*
DCO Type	Ring	Ring	Ring	Ring	*LC*	*LC*
f_{OUT} (GHz)	2.4 (2.3 – 2.55)	2.4 (0.8 – 3.2)	3.2 (N/A)	5.2 (2.0 – 5.5)	2.05 (1.73 – 3.38)	3.61 (2.92 – 4.05)
f_{REF} (MHz)	75	50	200	50	50	40
Multi. factor (*N*)	32	48	16	104	41	90.25
Area (mm^2)	0.055	0.049	0.022	0.084	0.50	0.22
1MHz PN (dBc/Hz) @f_{OUT} (GHz)	–119.8	–104.0	–104.0	–97.0 (Int-*N*) –96.5 (Frac-*N*)	–116.3 (Int-*N*) –116.3 (Frac-*N*)	–110.7 (Frac-*N*)
$Jitter_{RMS}$ (fs)	320 (1k – 100M)	2520 (100k – 100M)	3540 (10k – 300M)	1730 (Int-*N*) 1750 (Frac-*N*) (10k – 100M)	350 (Int-*N*) 420 (Frac-*N*) (1k – 30M)	420 (Frac-*N*) (3k – 30M)
Reference spur (dBc)	–75	N/A	N/A	–44	N/A	–72
Power (mW)	6.0	5.0	2.9	4.0	10.7	4.5
FOM_{JIT} (dB)*	–242.1	–225.0	–224.4	–229.2	–238.8	–241.0
$FOM_{JIT,N}$ (dB)**	–257.1	–241.8	–236.4	–249.4	–254.9	–260.6

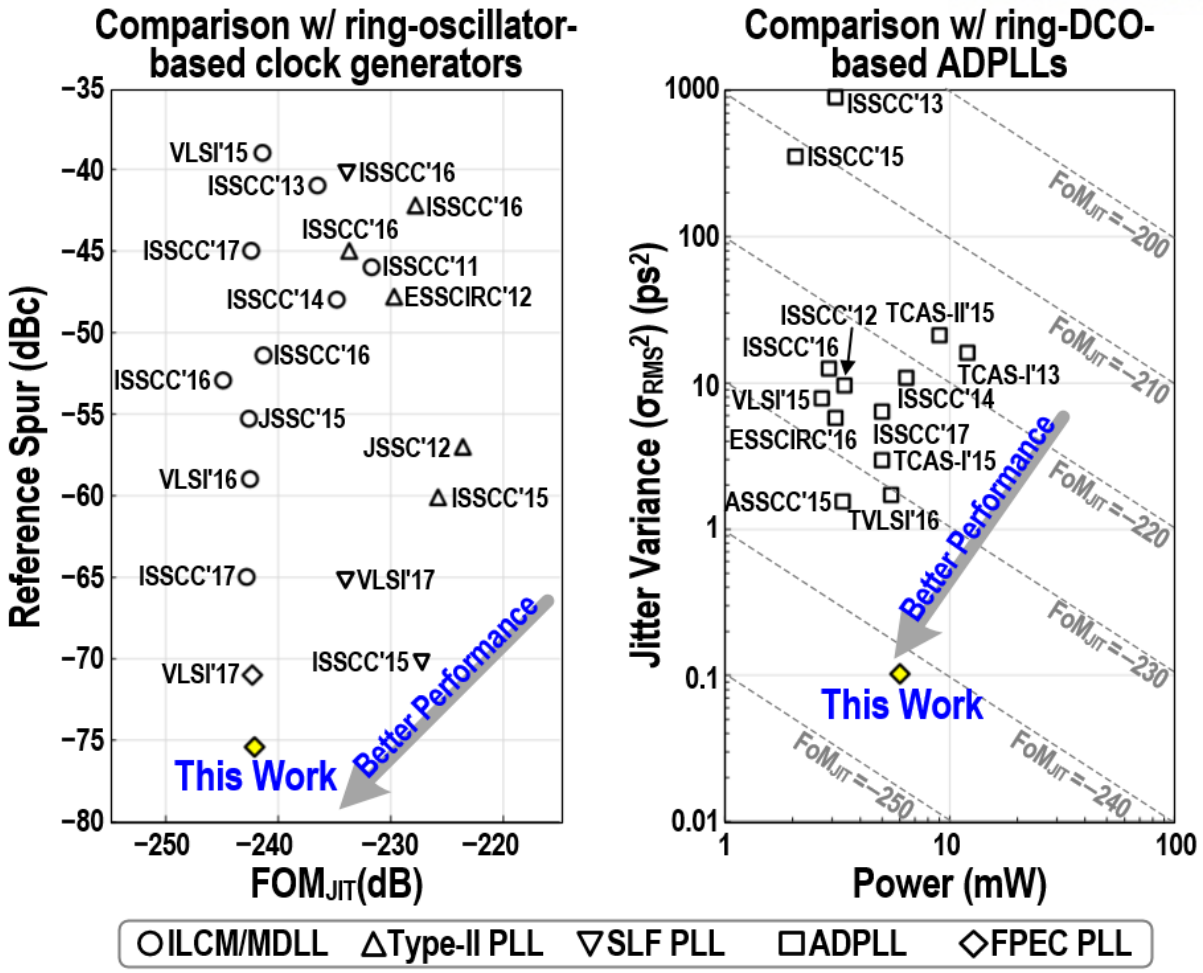


Figure 4-26. (a) Comparison with ring-oscillator-based clock generators. (b) Comparison with ring-DCO-based DPLLs.

4.6. Discussion

In this work, a new ring-DCO-based DPLL capable of concurrently achieving low RMS jitter and low levels of reference spurs is presented. The use of the FPEC technique emulating an ILCM allows the proposed DPLL to suppress the ring DCO's jitter significantly. An OS TDC is presented that lowers the quantization error effectively with low power consumption and maximizes the efficacy of the FPEC technique. Using the results of the Lloyd-Max algorithm, the digital calibrators optimize the TDC's time thresholds and the loop's error-correction gain; thus, even with a small number of N_{TDC} and a small amount of power, the quantization error present in a loop can be dramatically reduced. Digital calibration is performed continuously in the background, so the optimal performances of the DPLL can be maintained. As a result, the proposed FPEC DPLL with the OS TDC achieved ultra-low RMS jitter (320 fs) and low levels of reference spurs (< -75 dBc).

5. Conclusions

Despite the advantage of a high area-efficiency in silicon integration, the poor performance of jitter (or phase noise) has prevented the ring oscillator from replacing its *LC*-counterpart in the design of high-performance clock generators. There have been many efforts to develop a ring-oscillator-based clock generator capable of suppressing the oscillator's jitter. However, conventional architectures are still limited by the difficulty in achieving both low RMS jitter and low levels of reference spurs simultaneously while having a high multiplication factor.

In this dissertation, the problems and limits of prior ring-oscillator-based clock generators have been detailed with a time-domain analysis that provides an intuitive understanding of RMS jitter calculation of the clock generators from their phase-error correction mechanisms. Based on this analysis, new designs of a ring-oscillator-based PLL that can address the challenges of prior arts are proposed.

First, a ring-oscillator-based switched-loop-filter (SLF) PLL with the proposed fast phase-error correction (FPEC) technique is presented. The FPEC technique was developed based on the observation that an injection-locked clock multiplier (ILCM) has superior RMS-jitter performance than the other architectures, which was investigated through the time-domain analysis. With the FPEC technique that emulates the mechanism of phase realignment of an ILCM, the phase error of the voltage-controlled oscillator (VCO) can be removed quickly, so ultra-low jitter is achievable. In addition, since the SLF PLL with the FPEC technique is naturally based on a PLL topology, it has an intrinsic integrator in its transfer function; thus, the proposed PLL can achieve low reference spur while maintaining high stability even for a large multiplication factor. The prototype was fabricated with a 65-nm CMOS process. The measured RMS-jitter, FOM, and reference spur were 378 fs, −242 dB, and −71 dBc, respectively.

Second, another design of a digital PLL with the FPEC technique (or FPEC DPLL) is presented. The limit of the analog SLF PLL with the FPEC technique is that its loop characteristics are easily changed by PVT variations and/or the change of the output frequency. Unlike that architecture, the FPEC DPLL is implemented in a digital fashion, so the variables that define the loop characteristics can be easily estimated and corrected.

To overcome the problem of a conventional TDC, a low-power optimally-spaced (OS) TDC that is able to minimize the quantization error effectively is also presented. In the proposed FPEC DPLL, the decision thresholds and the loop's error-correction gain are calibrated to be optimal in the background; the quantization error can thus be minimized dramatically. As a result, the performances of an ultra-low jitter and an excellent figure-of-merit can be achieved. The proposed architecture was fabricated with a

65-nm CMOS process. The measured RMS-jitter, FOM, and reference spur were 320 fs, −242 dB, and −75 dBc, respectively.

Appendix A

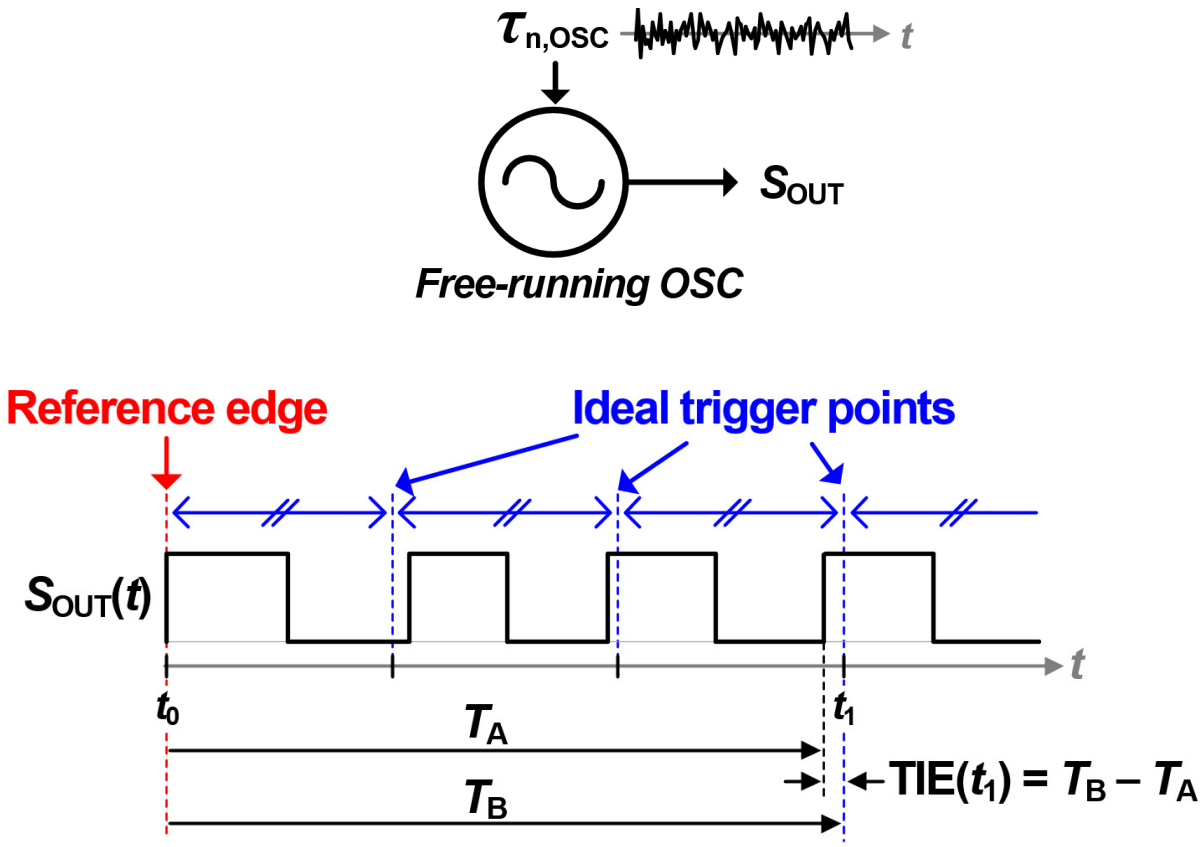


Figure A-1. Measurement of jitter using TIE.

To quantify the jitter present in the output signal of a clock generator, we used the notation of $J_{OUT}(t)$. The type of J_{OUT} is a time interval error (TIE), one of the most widely used methods of measuring jitter. The TIE denotes the timing difference between the measured signal edges and ideal trigger points. As shown in Figure A-1, when we consider a case of a free-running oscillator whose output is affected by the thermal white noise of an oscillator, $\tau_{n,OSC}$, the edges of the output signal, S_{OUT}, deviate from the ideal trigger points. Then, measuring TIE at t_1, it can be obtained as $T_B - T_A$.

Figure A-2 plots the TIE over time, (or $J_{OUT}(t)$) in the case of a free-running oscillator of Figure A-1. Due to $\tau_{n,OSC}$, J_{OUT} fluctuates arbitrarily. Every time we perform this simulation with different random seeds for $\tau_{n.OSC}$, J_{OUT} evolves differently, as shown in Figure A-3.

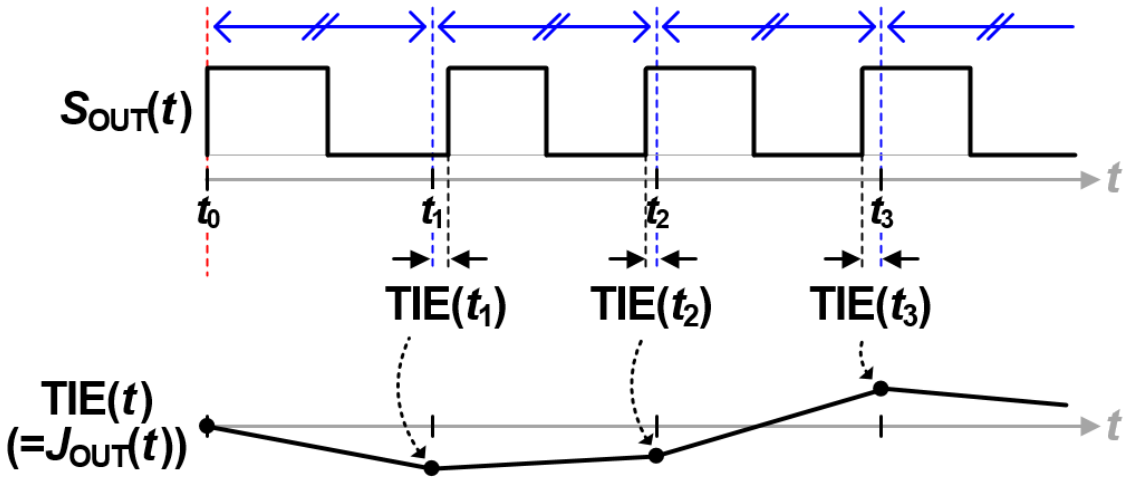


Figure A-2. Plot of TIE(=J_{OUT}) over time.

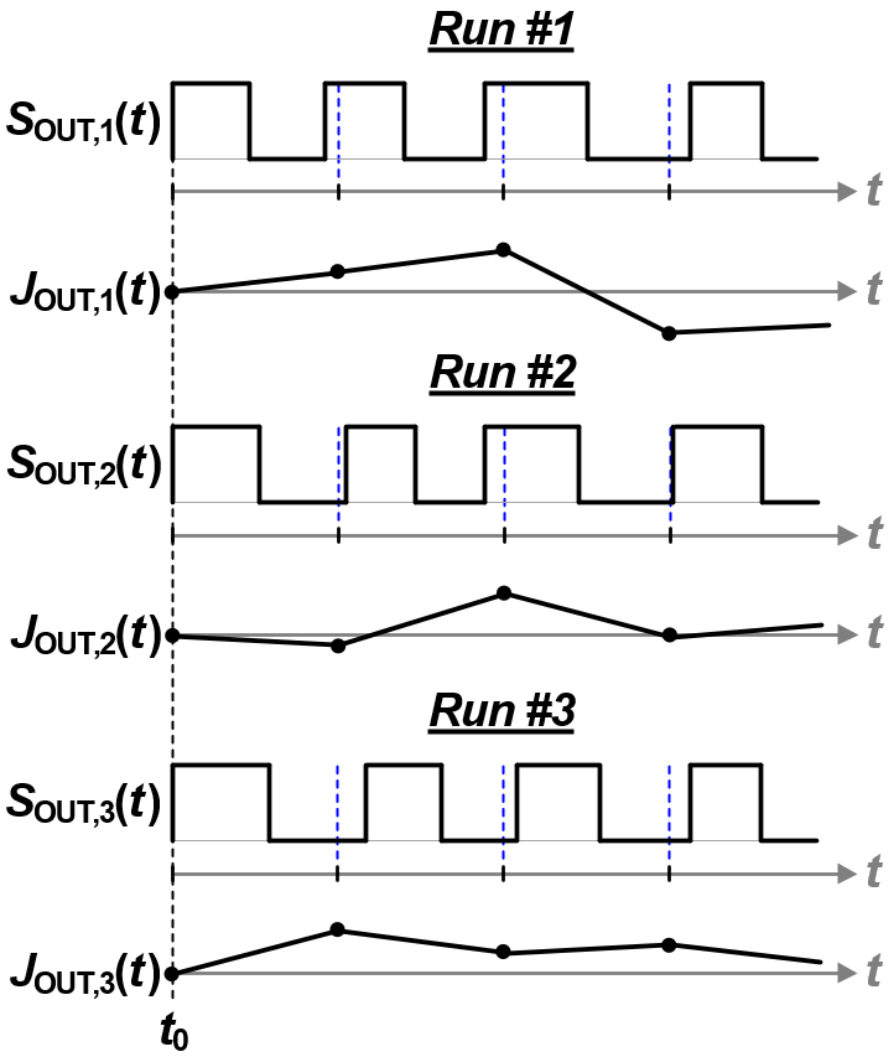


Figure A-3. Evolution of $J_{OUT}(t)$ that varies with each run of the simulation.

Basically, J_{OUT} at a certain t is unpredictable, but we can define its statistical characteristics. To do that, we performed a number of simulations of Figure A-1 and were able to acquire the distribution of J_{OUT} over time as shown in Figure A-4. The distribution of J_{OUT} exhibits a spreading shape with increasing time since the jitter introduced by $\tau_{n,OSC}$ "*accumulates*" over time [30]. Thus, we can see that quantifying the standard deviation of J_{OUT} at t, STDEV[J_{OUT}](t), causes it to increase over time. If we then plot the variance of the output jitter at t, VAR[J_{OUT}](t), it increases linearly over time, as shown in Figure A-5.

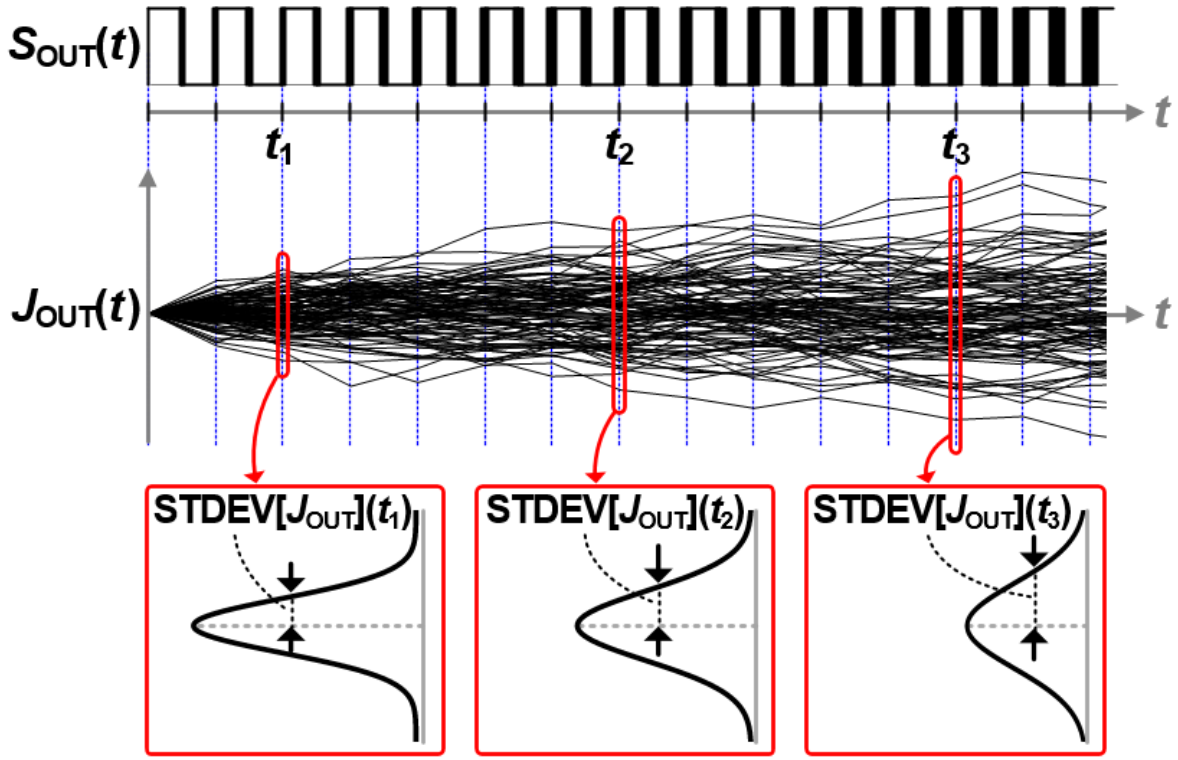


Figure A-4. Distribution of J_{OUT} over time in the case when an oscillator is free-running.

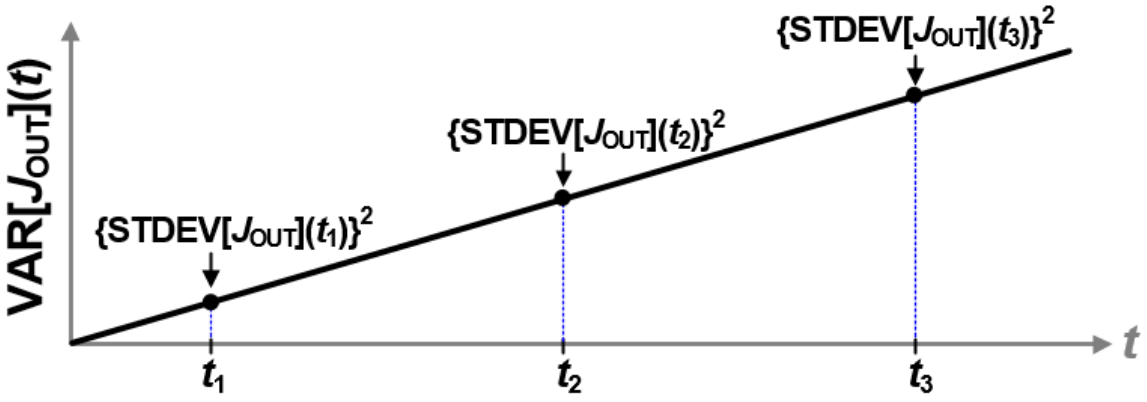
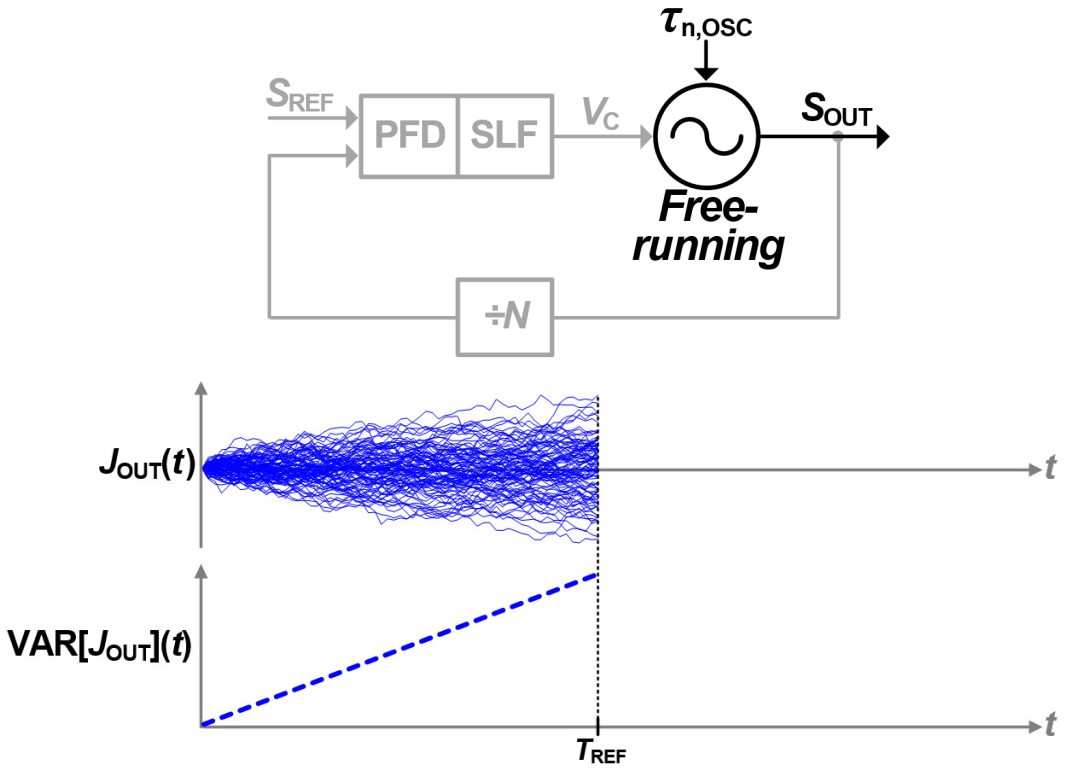
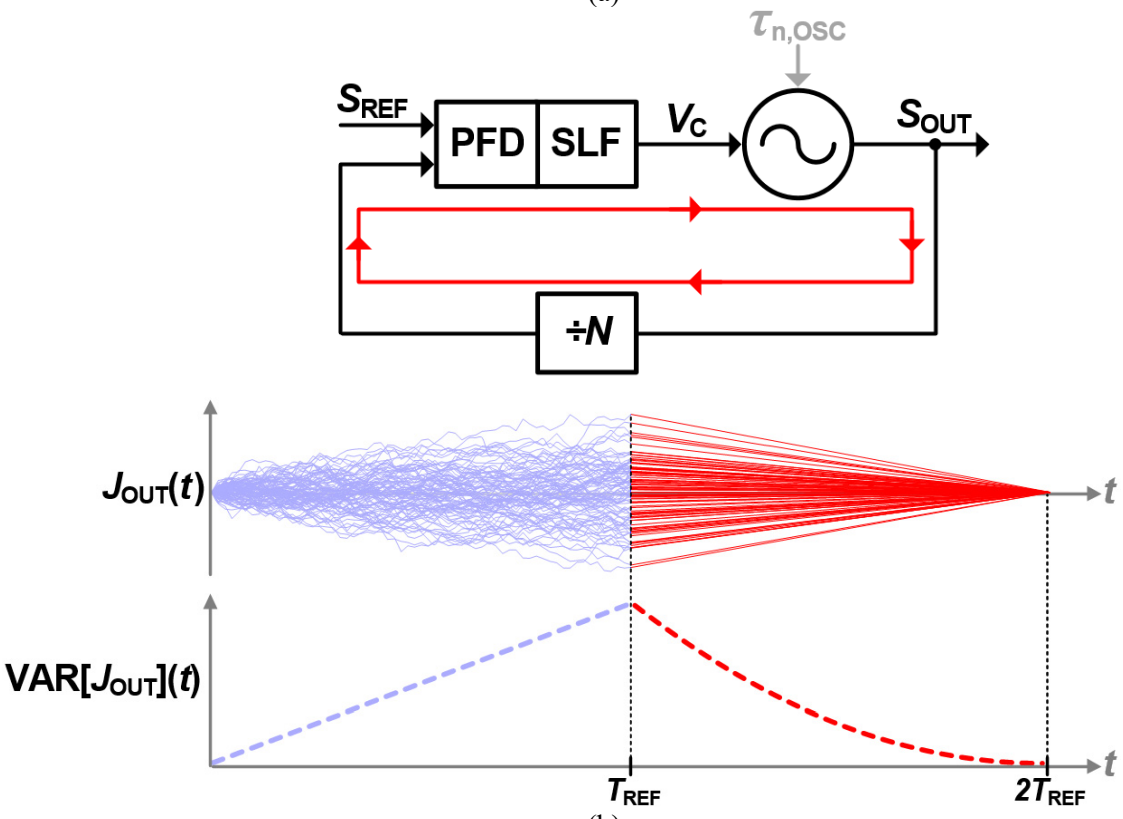


Figure A-5. Plot of VAR[J_{OUT}](t) over time of Figure A-4.



(a)



(b)

Figure A-6. J_{OUT} and VAR[J_{OUT}](t) in SLF PLL: (a) when the loop does not operate and the effect of τ_n,OSC is considered; and (b) when the loop starts to operate and τ_n is neglected.

Based on the observations in Figure A-4 and A-5, we now continue the analysis for J_{OUT} and VAR[J_{OUT}](t) when an oscillator is under the process of phase-error correction. Let us consider for the sake of simplicity an ideal case of an SLF PLL as shown in Figures A-6(a) and (b): during $0 \le t < T_{REF}$, only the generation of the oscillator's jitter due to $\tau_{n,OSC}$ without the effect of the phase-error correction is considered; and during $T_{REF} \le t < 2T_{REF}$, only the error-correction process without newly generated jitter is considered. Since there is no phase-error correction, VAR[J_{OUT}](t) increases during $0 \le t < T_{REF}$. At $t = T_{REF}$, the loop detects the phase error and starts to correct it. Then, during $T_{REF} \le t < 2T_{REF}$, $J_{OUT}(t)$ and VAR[J_{OUT}](t) respectively decrease linearly and quadratically (the phase error detected at $t = T_{REF}$ is assumed to be completely corrected, i.e., $\beta = 1$).

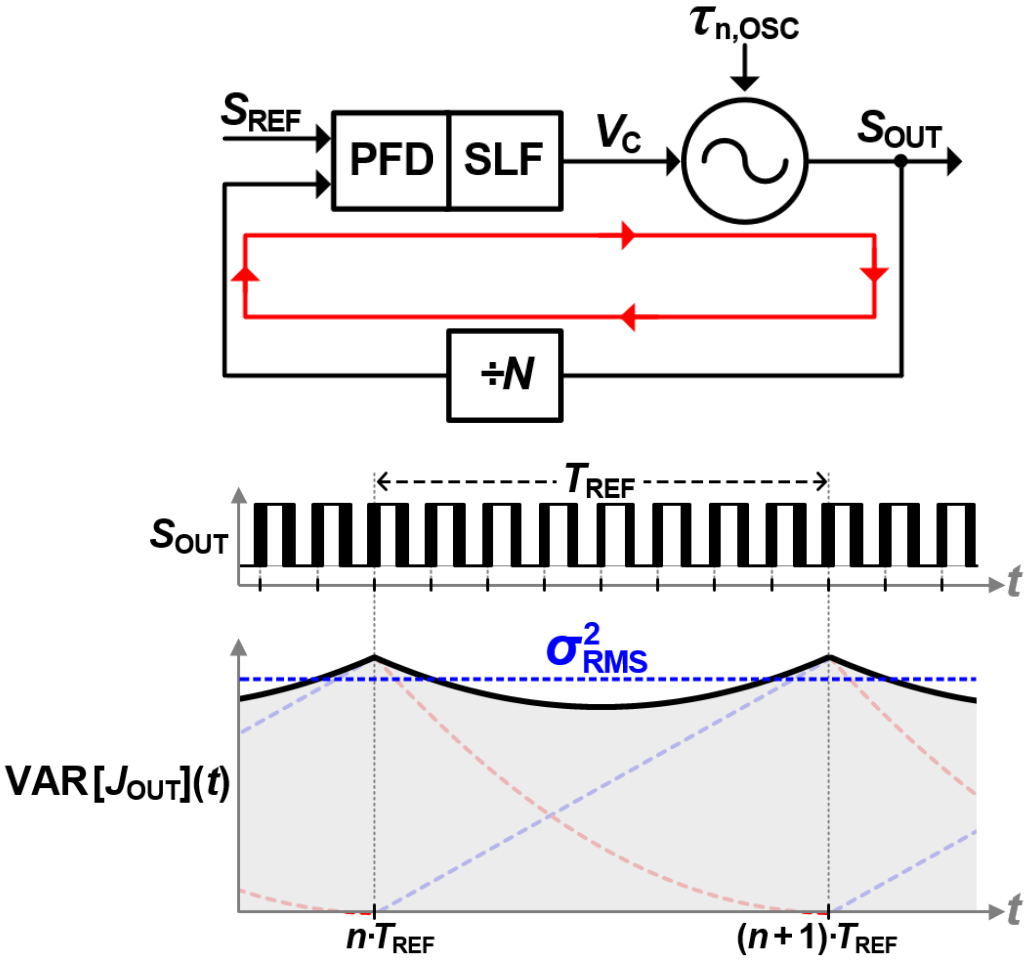
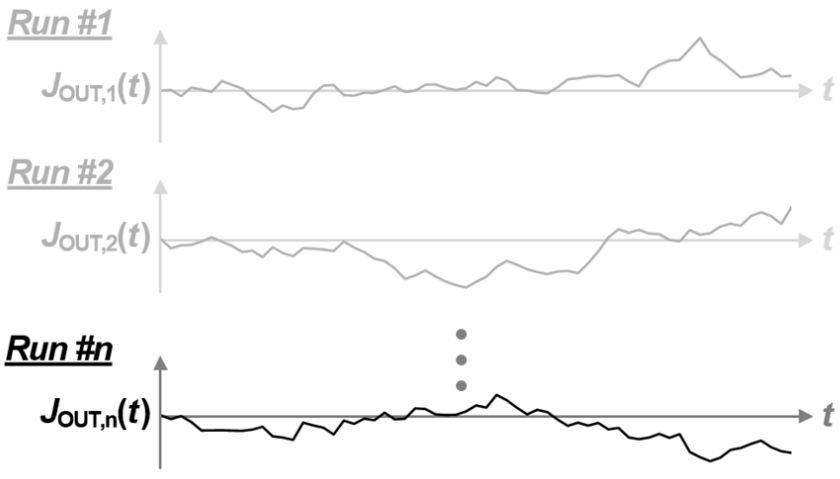


Figure A-7. VAR[J_{OUT}](t) of an SLF PLL in steady state.

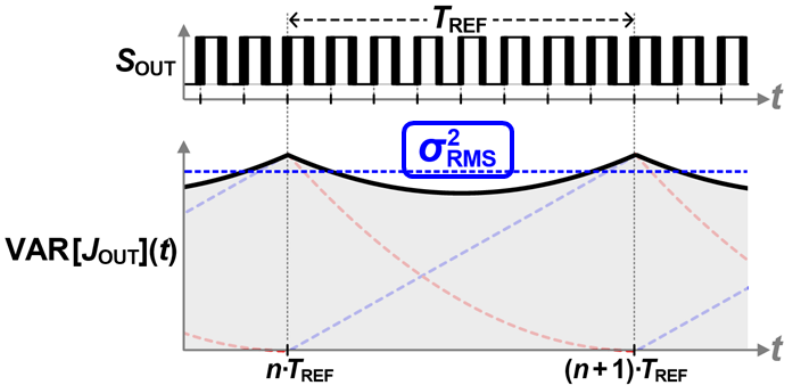
When we concurrently consider the effects of $\tau_{n,OSC}$ and error correction of Figures A-6(a) and (b), respectively, in a steady state, VAR[J_{OUT}](t) can be represented as shown in Figure A-7. In this case, VAR[J_{OUT}](t) is determined by superimposing the variances of 1) the jitter, newly generated by the VCO during the current T_{REF} (blue dotted line); and 2) the jitter, generated in the previous T_{REF} and removed during the current T_{REF} (red dotted line).

In the case of the calculation of RMS jitter, σ_{RMS}, we can calculate it by literally taking the RMS of $J_{OUT,}$ as shown in Figure A-8. Alternatively, since J_{OUT} has the property of a cyclostationary process with a period of T_{REF}, σ_{RMS} can be obtained by calculating the area under the VAR[J_{OUT}](t), as shown in Figure A-9.



$$\sigma_{\mathrm{RMS}} = \sqrt{\lim_{T\to\infty}\frac{1}{T}\cdot\int_0^T {J_{\mathrm{OUT},n}}^2(t)dt}$$

Figure A-8. Calculation of RMS jitter.



$$\sigma_{\mathrm{RMS}} = \sqrt{\lim_{T\to\infty}\frac{1}{T}\cdot\int_0^T {J_{\mathrm{OUT},n}}^2(t)dt} = \sqrt{\frac{1}{T_{\mathrm{REF}}}\cdot\int_0^{T_{\mathrm{REF}}}\mathrm{VAR}[J_{\mathrm{OUT}}](t)dt}$$

($\because J_{OUT}$ is Cyclostationary)

Figure A-9. An alternative way to calculate RMS jitter.

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