Master's Thesis

FULLY INTEGRATED HIGH-FREQUENCY CLOCK GENERATION AND SYNCHRONIZATION TECHINIQUES

Suneui Park

Department of Electrical Engineering

Graduate School of UNIST

2020

FULLY INTEGRATED HIGH-FREQUENCY CLOCK GENERATION AND SYNCHRONIZATION TECHINIQUES

Suneui Park

Department of Electrical Engineering

Graduate School of UNIST

FULLY INTEGRATED HIGH-FREQUENCY CLOCK GENERATION AND SYNCHRONIZATION TECHINIQUES

A thesis
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

Suneui Park

12/03/2019

Approved by

Advisor
Kyuho Lee

FULLY INTEGRATED HIGH-FREQUENCY CLOCK GENERATION AND SYNCHRONIZATION TECHINIQUES

Suneui Park

This certifies that the thesis of Suneui Park is approved.

12/03/2019

signature

Advisor: Professor Kyuho Lee

signature

Thesis Committee Member: Professor Seongjin Kim

signature

Thesis Committee Member: Professor Jaehyouk Choi

ABSTRACT

This thesis presents clock generation and synchronization techniques for RF wireless communication. First, it deals with voltage-controlled oscillators (VCOs) for local oscillators (LO) in transceivers, and secondly delay-locked loops for synchronization. For the high-performance LO, VCO is one of the key blocks. *LC* VCOs and ring VCOs are commonly-used types. Their characteristics are varied for different frequency bands. In this thesis, two types of VCOs, *LC* VCO and ring VCO, are presented with specific applications. For the multi-clock generator which could be used for carrier aggregation or frequency hopping, ring-type digitally controlled oscillator (DCO) was designed covering 900-1200 MHz with -165 dB FOM. For the multi-band frequency synthesizer which could be used for 5G communication with backward compatibility, three *LC* VCOs are designed which frequency range of 25-30 GHz for 5G, 5.2-6.0 GHz for LTE, 2.7-4.2 GHz for 2G-3G communication, respectively. For the clock synchronization in RF communications, a delay-locked loop (DLL) using a digital-to-analog converter (DAC) based band-selecting circuit (BSC) was presented to achieve a wide harmonic-locking-free frequency range. The BSC used the proposed exponential digital-to-analog converter (EDAC) to generate a collection of initial control voltages which follow a sequence of geometric with satisfying the condition for preventing harmonic locking problem. Therefore, the BSC can cover a much wider frequency range which is free from harmonic locking problem compared to initial band selection techniques using conventional, linear DAC (LDAC) that have a set of control voltages of arithmetic sequence. In this thesis, the DLL was implemented in a 65-nm CMOS process, and it had a measured frequency range from 100 to 1500 MHz which range is free from harmonic locking. The measure rms jitter and 1-MHz phase noise at 1000 MHz were 1.99 ps and –128 dBc/Hz, respectively. The DLL consumes 5.5 mW and its active area was 0.052 mm2.

CONTENTS

FIGURES

TABLES

TECHNICAL TERMS AND ABBREVIATIONS

VCO	Voltage-controlled oscillator
PLL	Phase-locked loop
CP	Charge pump
LF	Loop filter
DCO	Digitally-controlled oscillator
SDR	Software defined radios
VCDL	Voltage controlled delay line
DAC	Digital-to-analog converter
MUX	Multiplexer
DLF	Digital loop filter
TDC	Time-to-digital converter
PFD	Phase-frequency detector
DLL	Delay-locked loop
FTR	Frequency tuning range
EDAC	Exponential DAC

I. Introduction

For RF transceivers in wireless communications, clock generation and synchronization are essential techniques. For a local oscillator which generates carrier frequency of communications, voltage-controlled oscillators (VCOs) are main blocks for generating the appropriate frequency bands. In this thesis, *LC* VCOs were designed for frequency synthesizers which covers multi-frequency bands of 2G−4G, LTE, and 5G [1]. In that work, GHz-range analog charge-pump (CP) based phase-locked loop (PLL)'s output was multiplied to mmW frequency band. Since *LC* VCO's Q-factor is higher in GHz-range compared to mmW frequency range, achieving ultra-low phase noise of the PLL is easier in GHz-range frequency bands. In addition, ring type VCOs were designed for multi-clock generators [2]. Reference [2] presents time-interleaved all-digital calibrator with injection locking techniques. In that work, ring type digitally-controlled oscillators (DCOs) are real-time calibrated by time-interleaved fashion with MUX, TDC, DLF, and a replica-ring VCO. Since calibration bandwidth of time-interleaved calibrator is narrow, injection locked technique is applied to ring DCOs due to its large locking bandwidth. Therefore, poor ring DCOs' phase noise could be suppressed enough. For this reason, ring-type VCO is often used with injection locking techniques. Additionally, since in that work, fractional injection technique is applied, mismatches between inverter cells in DCO are critical. Therefore, layout is carefully operated.

DLLs are broadly used for synchronizing remote-located building circuits in RF transceiver modules. Some applications such as software defined radios (SDR) should cover a broad frequency spectrum. Therefore, the ability to synchronize a wide range of input frequencies, f_{IN}, is very significant issue. Though, the concern is, as the frequency spectrum of f_{IN} increases, the DLL becomes more susceptible to harmonic locking, which happens when the DLL is locked to any of harmonic tones of f_{IN} instead of the fundamental tone of f_{IN} [3], [4]. Hence, in order to prevent harmonic locking and confirm reliable operation over a broad range of fINs, a DLL should be designed with adequate measures. A simple approach is to restart the DLL's locking process whenever the DLL's output is locked to harmonic tones [4]. However, this approach degrades the power and area efficiency and increases lock time. Another approach is to use a band-selection method that initially selects a suitable range of the delay of a voltage-controlled delay line (VCDL), T_{VCDL}, of a DLL for each target f_{IN}. However, conventional band-selecting mechanisms in [5] and [6] segmented a range of f_{IN} into evenly divided frequency bands. Then, they needed a large bit number of DAC and band-selection delay cells which have large digitally controllability. In this thesis, we present a DLL with a technique of band selection that enables the DLL to achieve a very wide harmonic locking-free range with using only small bit number of a DAC. As a key block in the DLL, we propose the exponential DAC (EDAC), which provides exponential steps

instead of linear steps. The EDAC makes the DLL have a set of initial frequency bands to reduce the necessary bit number of a DAC drastically for covering the same range of f_{IN} avoiding harmonic locking.

This thesis is organized as follows: Section II presents background information of VCOs, especially in ring VCO and *LC* VCO, and DLLs. Section III provides the specific applications of each VCO. In Section IV, a DLL with proposed EDAC is presented and the conclusion is presented in Section V.

II. High-frequency clock generation

2.1 Voltage controlled oscillators (VCOs): *LC* VCOs and Ring VCOs

There are various types of the VCOs. *LC* VCOs and Ring oVCOs are used for VCO in PLL for high frequency generation, and crystal oscillator and relaxation oscillator are used for reference clock generator for PLL. In the following subparts of 2.1.1 and 2.1.4, we will focus on the characteristics of the *LC* VCO and the ring VCO. Figure 1 is the feedback model of the VCO. For the oscillation, VCOs should satisfy the Barkhausen criterion which says that total loop gain of the feedback oscillator should be larger than unity and phase shift should be 360°. For the evaluation of the VCO performance, oscillation frequency (ω), frequency tuning range (FTR), phase noise, dissipated power (P_{diss}) are the general criteria. Therefore, Figure of merit of the VCO can be represented as,

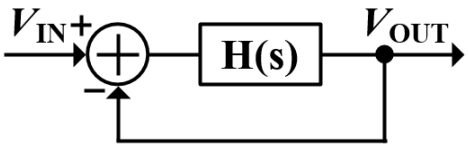
$$\text{FOM}_{\text{VCO}} = -L\{\Delta\omega\} + 20\log_{10}\frac{\omega}{\Delta\omega} - 10\log_{10}\frac{P_{\text{diss}}}{1\text{mW}}, \tag{1}$$

where $L\{\Delta\omega\}$ is the spot noise of the VCO at the offset frequency of $\Delta\omega$. For some applications, in which frequency tuning range is important, VCO FOM can be transformed to FOMT:

$$\text{FOMT}_{\text{OSC}} = -L\{\Delta\omega\} + 20\log_{10}\frac{\omega}{\Delta\omega} - 10\log_{10}\frac{P_{\text{diss}}}{1\text{mW}} + 20\log_{10}\frac{\text{FTR}}{10}. \tag{2}$$

According to the specific type of the VCO, FOM have a theoretical limit value since the power consumption has a trade-off relationship with the phase noise of the VCO.

Table. 1 shows the characteristics of the *LC* VCO and the ring VCO for comparison. Ring VCO is often used when its application needs area efficiency. Since the ring VCO is designed without oscillator, its area is very small. Compared to ring VCO, *LC* VCO needs large passive devices of inductor and capacitor to make oscillator, which makes *LC* VCO's size large. Although *LC* tank occupies large are, *LC* oscillators are widely used for the applications which needs excellent performance of the phase noise. Since *LC* resonance tank acts like a band-pass filter with its large Q-factor, its phase noise filtering effect is excellent. Therefore, it can achieve low phase noise compared to the ring VCO. However, as increasing the frequency tuning range of the *LC* VCO, its Q-factor decreases extremely, which extremely degrades the phase noise performance. Even so, since the ring VCO's maximum achievable frequency is limited to minimum delay of the inverter cells, *LC* VCO is more appropriate architecture for the extremely high frequency generation.



$$|H(s)| \geq 1$$
$$\angle H(s) = 180^\circ$$

Figure 1. Feedback model of the oscillator.

Table 1. Comparison between *LC* VCO and Ring VCO.

	***LC* VCO**	**Ring VCO**
Advantages	• Low phase noise • High frequency generation	• Wide tuning range • Small area (Integrativity)
Disadvantages	• Large area • Narrow tuning range	• Poor phase noise

2.2. *LC* VCOs for a low-phase noise phase-locked loop (PLL)

2.2.1. Voltage controlled oscillators (VCOs): Ring VCOs and *LC* VCOs

LC VCOs are the mostly used VCO for RF communication for its excellent phase noise performance. Figure 2(a), (b) show two types of the basic architectures of the *LC* VCOs. Figure 2(a) is a single-switch pair oscillator and Figure 2(b) is a double-switch pair oscillator. Especially, Figure 2(a) is a NMOS-type single-switch pair oscillator among two types of single-switch pair oscillator, NMOS-type and PMOS type. Since the mobility of the electron is higher compared to the hole, NMOS-type is more widely used. Those switch pairs of cross-coupled transistors provide negative resistance to the tank. Realistically, *LC* devices have series parasitic resistance, then, we can transform the series parasitic resistance to the parallel resistance as shown in Figure 3. As a result, energy stored in the tank is dissipated at this parasitic resistance. For the continuous oscillation, those dissipated energy compensated with generated energy from negative resistance from cross-coupled transistor pair. From the issue, start-up condition of the *LC* VCO for Figure 2(a) can be represented as,

$$\frac{2}{g_{\mathrm{mn}}} \geq R_{\mathrm{P}}. \tag{4}$$

In the same manner, for Figure 2(b), VCO's start-up condition can be represented as,

$$\frac{2}{g_{\mathrm{mn}}} + \frac{2}{g_{\mathrm{mP}}} \geq R_{\mathrm{P}}, \tag{5}$$

where $L_P \approx L_{\mathrm{TANK}}{}^2 \cdot \omega^2 / R_S$, $C_P \approx C_{\mathrm{TANK}}$, $R_S \approx Q_O{}^2 R_S$, and $2/g_m$ is the absolute value of the negative resistance from the cross-coupled transistors of the *LC* VCO From Equation (4), (5), the start-up condition is relaxed for double-switch pair oscillator since the NMOS and PMOS share the same current path and their negative resistance is added. Therefore, for the power efficient design, double-switch pair oscillator is a good choice. Output voltage swing of Figure 2(a) can be represented as,

$$V_{\mathrm{OUT}} = \frac{2}{\pi} I_{\mathrm{SS}} R_{\mathrm{P}}, \tag{6}$$

where fundamental harmonic of the load current is $2 \cdot I_{\mathrm{SS}}/\pi$ since the current flows M1 and M2 commutatively with square wave. As increasing I_{SS}, V_{OUT} also increased until V_{OUT} reaches to $2V_{\mathrm{DD}}$ which is the maximum output voltage peak-to-peak swing, V_{MAX}. Output voltage swing of Figure 2(b) can be represented as,

$$V_{OUT}=\frac{4}{\pi}I_{SS}R_P, \tag{7}$$

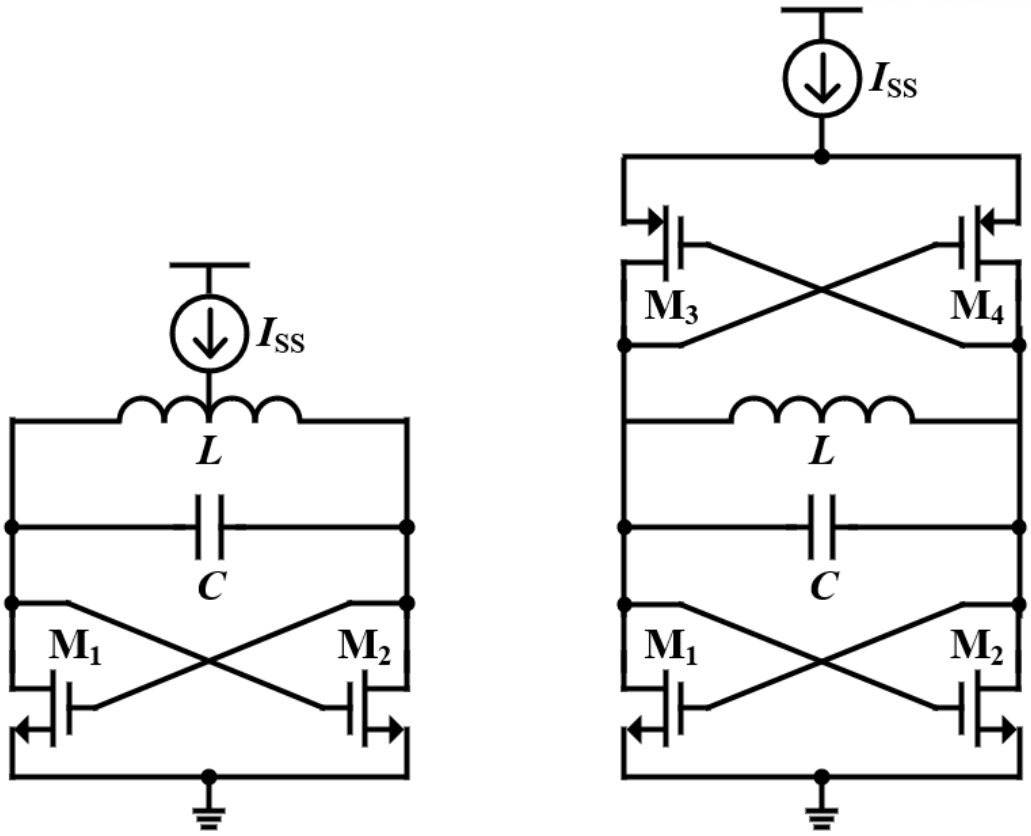
where fundamental harmonic of the load current is $4\cdot I_{SS}/\pi$. As increasing I_{SS}, V_{OUT} also increased until V_{OUT} reaches to V_{DD} which is the V_{MAX}. In the region where the output swing depends on the current, double-switch pair oscillator have larger output swing, however, after the voltage swing is limited to the supply voltage, single-switch pair oscillator can achieve more larger output swing of $2V_{DD}$. In result, double-switch pair oscillator is proper for the power efficient architecture and single-switch pair oscillator is proper for the low phase noise oscillator with large signal power. For the simple intuition to the phase noise of the *LC* VCO, Leeson's equation is well-known approach which assumes VCO as a LTI system. Then, phase noise of the VCO can be represented as [7],

$$L(\Delta\omega)=10\cdot\log_{10}\{\frac{1}{2}\cdot\frac{\frac{\overline{v_n^2}}{\Delta f}}{\frac{V_{OUT}^2}{2}}\cdot(\frac{\omega}{2Q_O\Delta\omega})^2\}, \tag{8}$$

where Q_O is the quality factor of the VCO. Therefore, to achieve low phase noise, output voltage swing should be larger, and quality factor of the VCO should be higher. Quality factor of the *LC* VCO is,

$$Q(\omega)=Q_C\|Q_L=\frac{1}{C_PR_P\omega}\|L_PR\omega, \tag{9}$$

where Q_C is the quality factor of the capacitor and Q_L is the quality factor of the inductor. As shown in the Equation (9), Q-factor of the tank follows the lower factor between Q_C and Q_L. As the frequency increases, Q-factor of the capacitor decreases and Q-factor of the inductor increases. Therefore, usually, inductor's Q-factor is dominant for GHz-range VCO and capacitor's Q-factor is dominant for tens of GHz-range VCO.



(a) (b)

Figure 2. Basic architecture of the *LC* VCO: (a) single-switch pair oscillator. (b) double-switch pair oscillator.

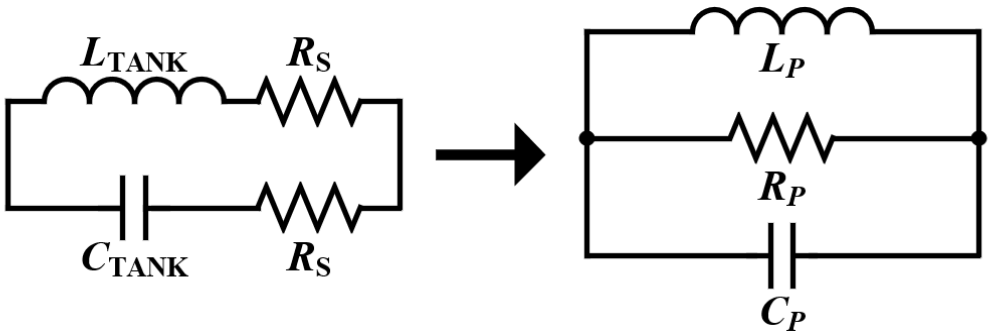


Figure 3. Realistic model of the *LC* tank.

Phase locking loop (PLL) is the most commonly used architecture for clock generation by locking the output clock's phase to the input reference clock's phase. Figure 1 shows the basic architecture of the PLL which consists of a phase-frequency detector (PFD), a charge-pump (CP), a loop-filter (LF), a voltage-controlled oscillator (VCO), and a frequency divider (/*N*). The PFD detects phase and frequency difference between the input clock, f_{IN}, and the output clock, f_{OUT}. A CP converts the phase difference to current with a gain of $I_{CP}/2\pi$, and this current flows into the loop filter which converts current to frequency-tuning voltage of the VCO, V_{TUNE}, with a gain of LF(s). The output frequency can be represented as,

$$\omega_{OUT}=\omega_0+V_{TUNE}\cdot K_{VCO}, \tag{11}$$

where K_{VCO} is the voltage to frequency gain of the VCO in rad/s/V. Relationship between input and output frequency can be represented as,

$$f_{OUT}=N\cdot f_{IN}, \tag{12}$$

where N is the division number from output to input frequency. Therefore, by changing the division number, various output frequencies can be obtained. In addition, ideally, input phase and the output phase are same, however, realistically, there exists phase offset between input and the output clock's phase since PLL have many nonlinear effects in each block.

Figure 5 shows the linear model of the PLL for each block's phase noise transform function [8]. From the input to the output, open loop gain can be represented as,

$$\mathrm{OLG(s)}=\frac{\Phi_{OUT}}{\Phi_{IN}}=\frac{I_{CP}}{2\pi}\mathrm{LF(s)}\frac{K_{VCO}}{\mathrm{s}}, \tag{13}$$

where I_{CP} is the charge pump current, LF(s) is the loop filter impedance, where LF(s) is $\{(R_1+1/C_1\mathrm{s})\|(1/C_2\mathrm{s})\}$ when PLL is a third-order with second-order loop filter. Closed loop gain from Φ_{IN}, $i_{n,CP}$, $v_{n,LF}$, or $\Phi_{n,VCO}$ to Φ_{OUT} can be represented as,

$$\mathrm{CLG\ (s)}=\frac{\Phi_{OUT}}{\Phi_{IN}}=\frac{\mathrm{OLG(s)}}{1+N\cdot\mathrm{OLG(s)}}, \tag{14}$$

$$\frac{\Phi_{OUT}}{i_{n,CP/PFD}}\mathrm{(s)}=\frac{\mathrm{OLG(s)}}{1+N\cdot\mathrm{OLG(s)}}\cdot\frac{2\pi}{I_{CP}}, \tag{15}$$

$$\frac{\Phi_{OUT}}{v_{n,LF}}\mathrm{(s)}=\frac{\mathrm{OLG(s)}}{1+N\cdot\mathrm{OLG(s)}}\cdot\frac{2\pi}{I_{CP}\cdot\mathrm{LF(s)}}, \tag{16}$$

$$\frac{\Phi_{OUT}}{\Phi_{n,VCO}}(s) = \frac{1}{1+N\cdot OLG(s)}. \quad (17)$$

From above equations, through the PLL system, input reference clock's phase noise and the PFD, and the CP noise are characterized as low-pass filter, LF noise is band-pass filtered, and the VCO's phase noise is high-pass filtered as shown in Figure 6(b) when the flicker noise of the VCO is neglected. Since each noise source have different characteristics, PLL bandwidth should be carefully designed for the optimal point. If a VCO have low free-running phase noise, PLL bandwidth could be extended to suppress the other loop building blocks' phase noise, to achieve ultra-low jitter performance of the PLL. Therefore, phase noise performance of the VCO is one of the main factors which determine the overall phase noise performance of the PLL.

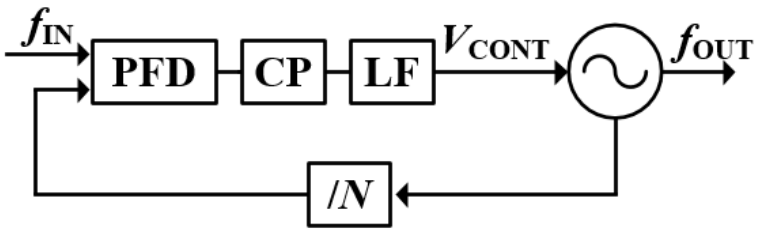


Figure 4. Basic architecture of the PLL.

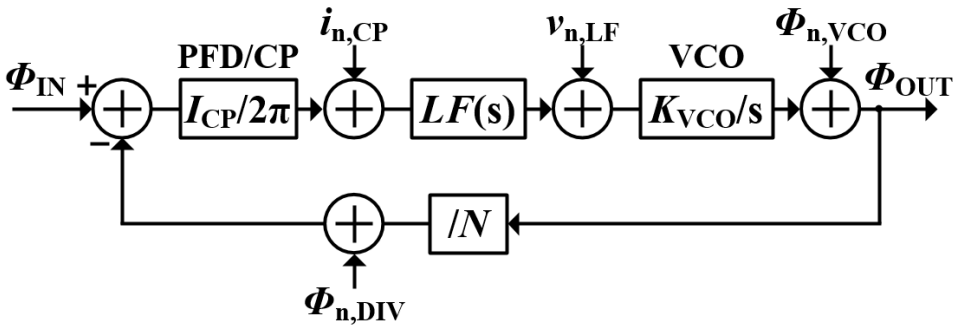


Figure 5. Linear model of the PLL.

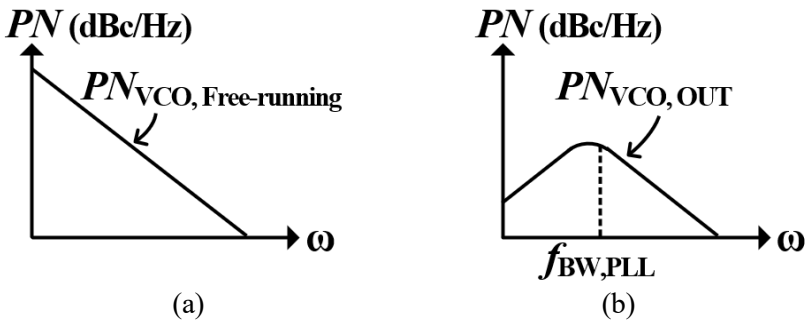


Figure 6. Phase noise of VCO at (a) $\Phi_{n,VCO}$. (b) Φ_{OUT}.

2.2.2. Design of *LC* VCOs

LC VCOs are used for frequency synthesizers which covers multi-frequency bands from 2G-5G in [1]. In that work, GHz-range analog CP PLL output multiplied to the mmW frequency band. Since *LC* oscillator of GHz-range has higher Q-factor compared to that of tens of GHz-range, achieving ultra-low phase noise of the PLL is easier in GHz-range frequency bands. Therefore, in [1], to generate tens of GHz-range low-jitter clock for 5G communications, GHz-range low-jitter PLL output is multiplied to mmW frequency band with low added jitter calibrator for mmW band.

LC oscillators are used for frequency synthesizers which covers multi-frequency bands from 2G to 5G in [1]. In that work, GHz-range analog CP PLL's output signal was multiplied to the mmW frequency band. Since the *LC* VCO of GHz-range has higher Q-factor compared to that of tens of GHz-range, achieving ultra-low phase noise of the PLL is easier in GHz-range frequency bands. Therefore, in [1], to generate tens of GHz-range low-jitter clock for 5G communications, GHz-range low-jitter PLL output is multiplied to mmW frequency band with low added jitter calibrator for mmW band.

Figure 7 shows the design of the NMOS single-switch pair *LC* VCO with 7-bit capacitor bank and 2-bit varactor bank for a GHz-range *LC* VCO. It consists of a *LC* tank, 7-bit capacitor bank (C_{BANK}), 2-bit varactor (C_{VAR}), and cross-coupled transistors (M_1, M_2). Capacitor bank is used for frequency channel switching, and varactor is used for real time frequency calibration by the PLL. Cover range of the capacitor bank decides frequency tuning range of the *LC* VCO and the varactor should be designed to cover frequency drift due to real-time VT variations. To achieve wide tuning range, capacitor bank should have large capacitance and large bit number, which results the degradation of the Q-factor of the *LC* tank. Therefore, there is a trade-off between the frequency tuning range and the Q-factor of the *LC* tank.

Figure 8(a) shows the design of the 7-bit capacitor bank. It consists of seven binary-sized capacitors, MOSFET transistors as switching devices for each bit, and biasing resistors. The size of switch transistors should be also binary sized since its R_{ON} resistance affects directly to the capacitors' Q-factor. Since the Q-factor of the capacitor bank can be calculated as the parallel of each capacitor and weighted with each capacitor size, it can be represented as,

$$\frac{1}{Q_{TOT}} = \frac{C}{Q_C} + \frac{2C}{Q_{2C}} + \cdots + \frac{2^N C}{Q_{2^N C}}. \tag{10}$$

Therefore, achieving high Q-factor of the most significant bit (MSB) capacitor is important. Bias

resistors help switching activity. To make switch MOSFET's drain voltage 0 when it is ON state, and 1 when it is OFF state, it makes the switch fully ON or OFF. Figure 8(b) shows a varactor design. Since varactor's capacitance depends on the DC bias voltage, it usually separates its bias voltage from the output DC voltage of the oscillator using DC block capacitor. DC block capacitance should be large enough compared to varactor capacitance, and V_{TUNE} is controlled by the PLL. Usually, MOSCAP is used as a varactor, and thick device is used to relive varactor leakage problem and to endure large voltage swing across the device. Figure 9(a) shows the frequency configuration according to V_{TUNE}, therefore, K_{VCO} configuration looks like a Figure 9(b). This non-linear configuration of the K_{VCO} can raise a serious problem in PLL design since PLL bandwidth is varied by K_{VCO} value. To solve this problem, offset-bias scheme with a 2-bit varactor was used as shown in Figure 10. To make two varactors have different bias voltages, V_{BIAS1}, and V_{BIAS2}, K_{VCO} of the total varactor capacitance is nearly maintained even though each varactor's K_{VCO} is significantly varied.

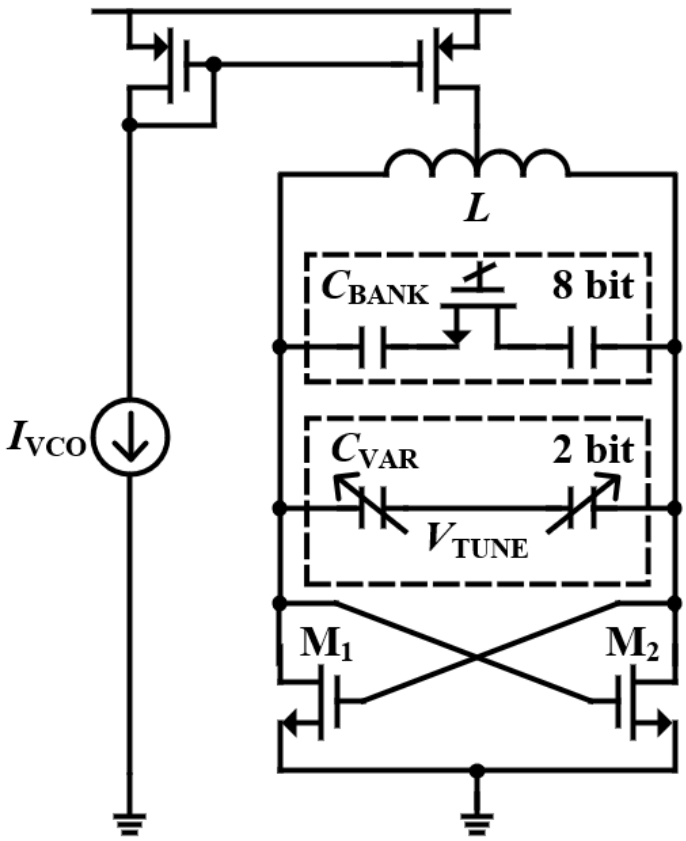
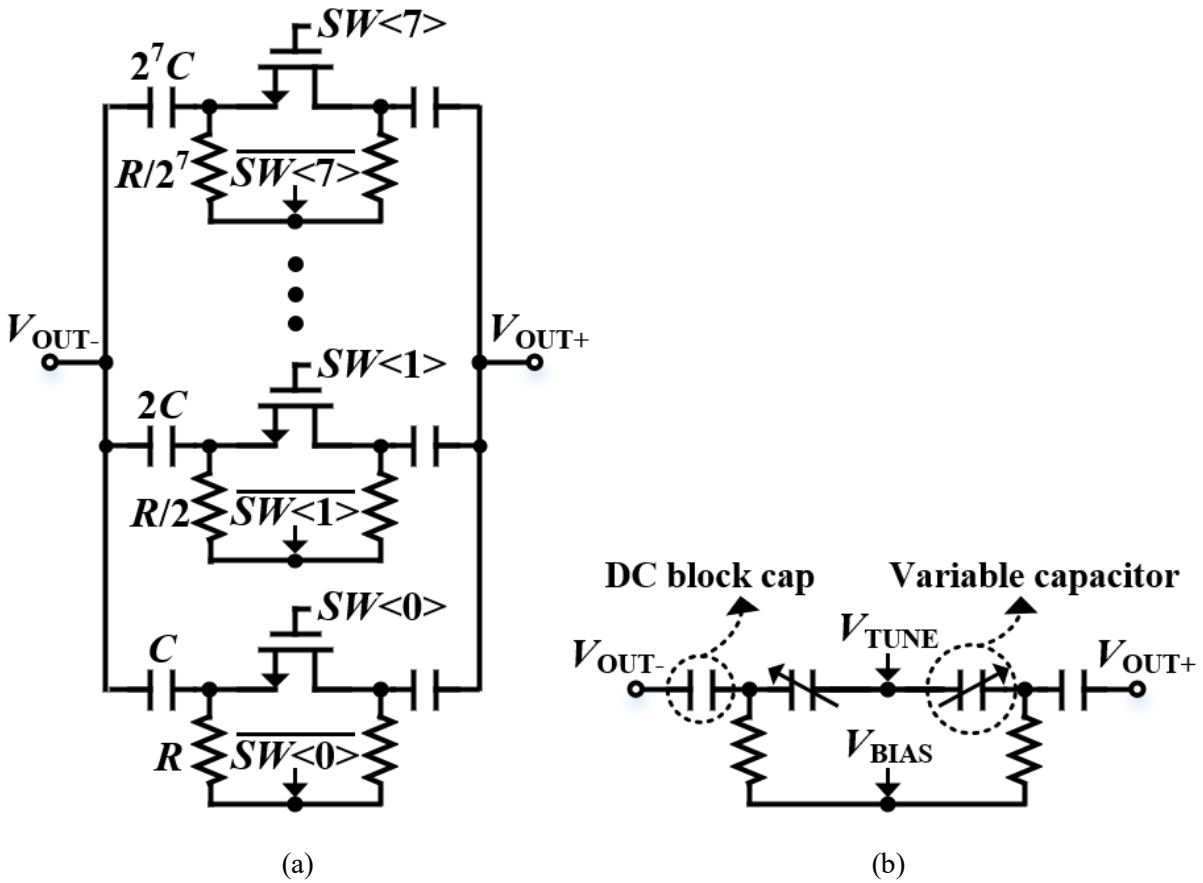
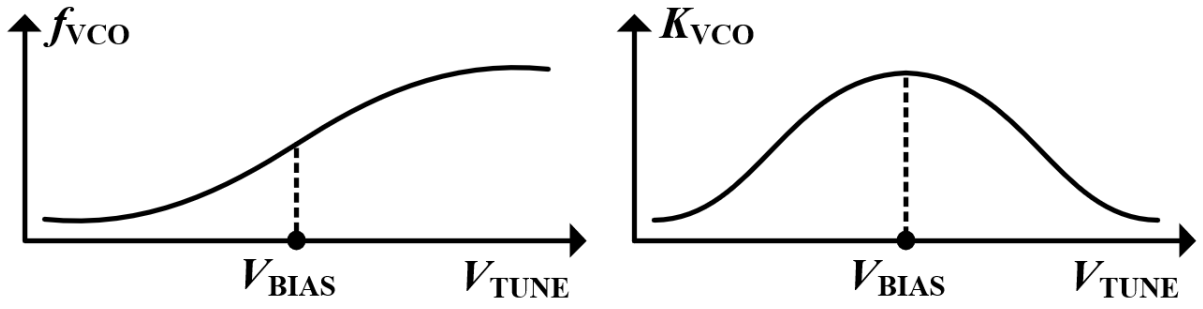


Figure 7. *LC* VCO with 8-bit capacitor bank and 2-bit varactor.



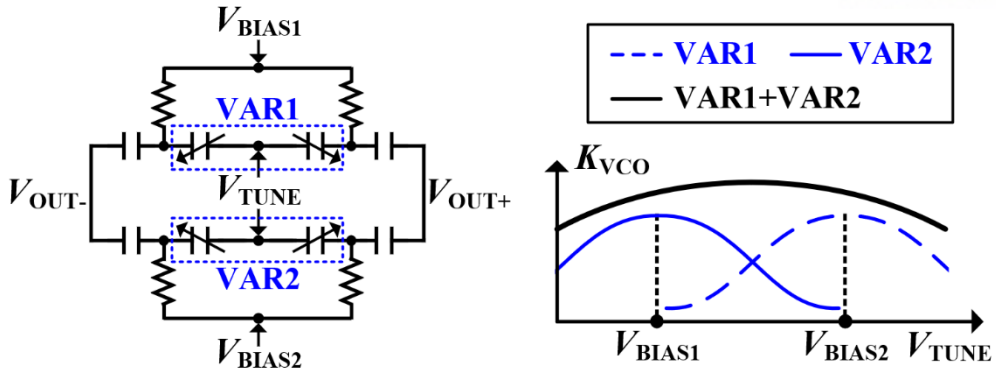
(a) (b)

Figure 8. (a) 8-bit capacitor bank design; (b) varactor design of the *LC* VCO.



(a) (b)

Figure 9. (a) Frequency configuration of a single varactor according to control voltage, V_{TUNE}. (b) K_{VCO} configuration of a single varactor according to V_{TUNE}.



(a) (b)

Figure 10. Offset-bias scheme with 2-bit varactor bank; (a) schematics. (b) K_{VCO} configuration.

2.2.3. Simulation results

In [1], since it targeted multiple frequency band to cover 2G-4G, LTE, and 5G communication's frequency band, it needs three different VCOs. First, GHz-range VCO operates with analog CP PLL. Since PLL's bandwidth is not that large, VCO's phase noise performance is critical. Therefore, one-turn inductor was used for high-Q factor, and 8-bit NMOS-type single-switch pair *LC* VCO was designed in a 65nm CMOS technology for low-phase noise application, and 2-bit varactor with offset-bias scheme was used to reduce the K_{VCO} variation effect. Output phase noise of the GHz-range *LC* VCO is shown in Figure 11 when the output frequency of the PLL was 3.897 GHz. As illustrated in section 2.2.1, the VCO was high-pass filtered by the PLL loop, and it covered from 2.7 to 4.2 GHz. In simulation result, the *LC* VCO consumed 6.0 mW, and 1MHz offset spot noise was −105 dBc/Hz, therefore, FOM of -189 was achieved. Figure 12 shows the simulation results of the nearly constant K_{VCO} of GHz-range VCO which used offset-bias scheme. Then, the PLL using the *LC* VCO could achieve robustness over VT variations.

As the operation frequency of the *LC* VCO is higher, the *LC* VCO's phase noise performance is degraded and its size is reduced dramatically. Then, even though a *LC* VCO is usually used with a PLL, injection locking techniques is a good choice for a *LC* VCO of extremely high frequency. Then, in [1], LTE band VCO and mmW band VCO was used with injection locking techniques. Since injection locking technique has wide noise shaping bandwidth, two VCOs could use multiple turned inductors to increase area efficiency. For the LTE frequency band, *LC* VCO covers the frequency range of 5.2-6.0 GHz, and for the mmW frequency band, *LC* VCO covers the range of 25.0-30.0 GHz. Additionally,

CMOS double-switch pair type *LC* VCO was used for both LTE and mmW frequency band to increase power efficiency. The simulation results of the phase noise of free-running VCO and shaped noise after injection locked are plotted in Figure 13 for LTE band, and plotted in Figure 14 for mmW band. They consumed 4.6 mW, and 5.2 mW, respectively.

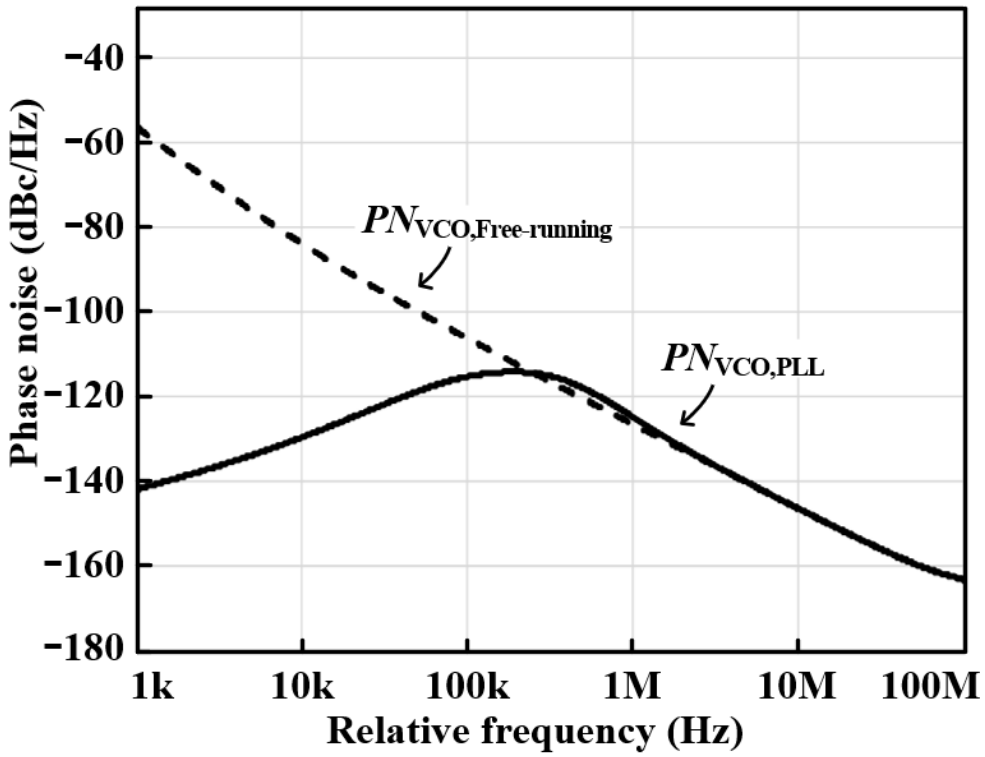


Figure 11. Free-running phase noise of the *LC* VCO and the shaped phase noise by PLL at 3.897 GHz.

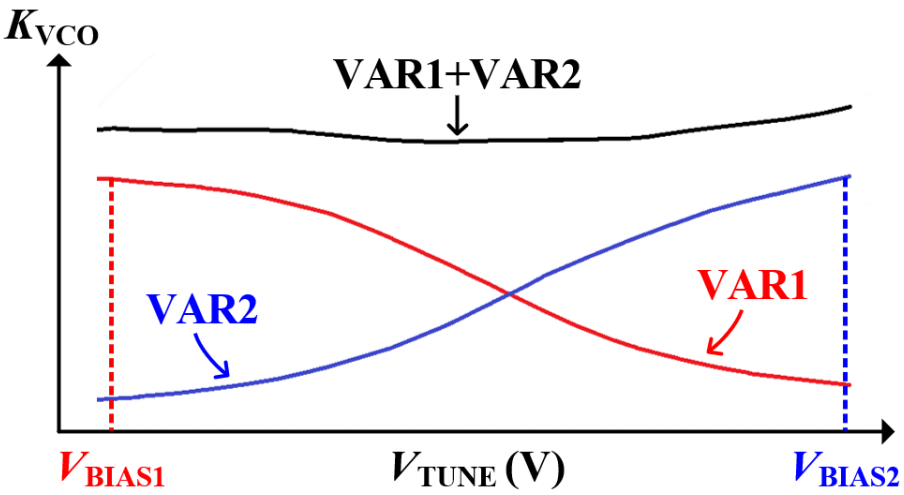


Figure 12. Simulation results of the K_{VCO} of the GHz-range *LC* VCO by using offset-bias scheme with two varactors.

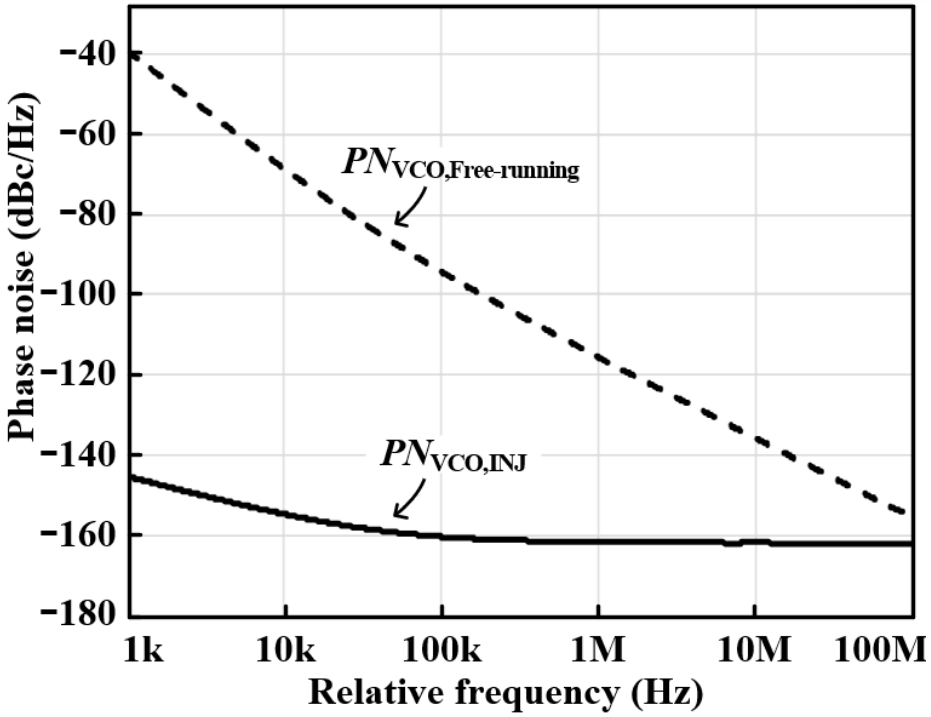


Figure 13. Free-running phase noise of the *LC* VCO and the shaped phase noise by injection locking at 5.845 GHz.

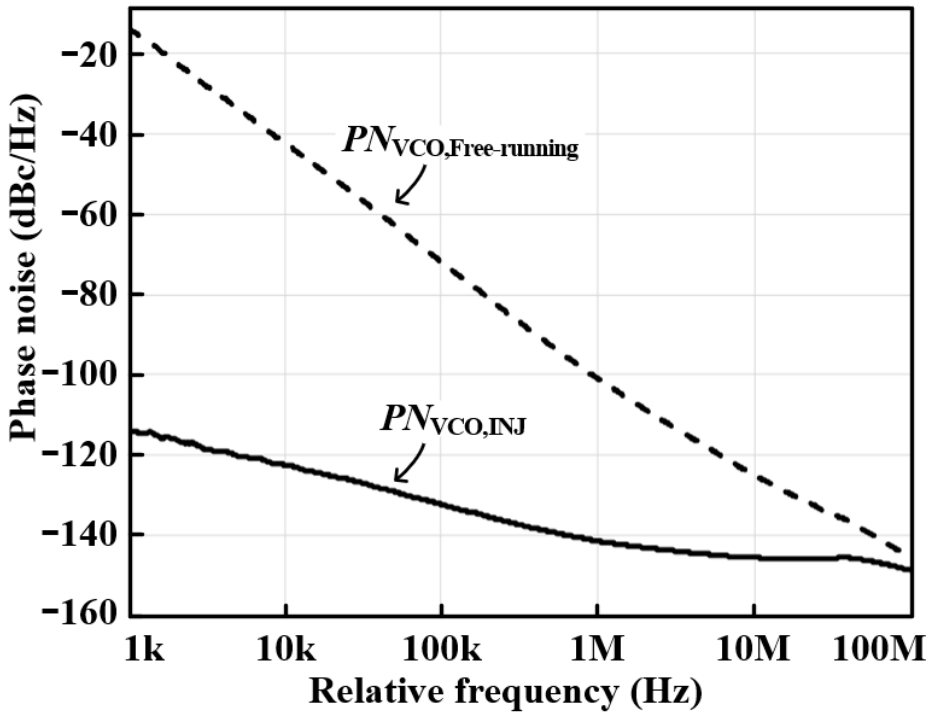


Figure 14. Free-running phase noise of the *LC* VCO and the shaped phase noise by injection locking at 29.228 GHz.

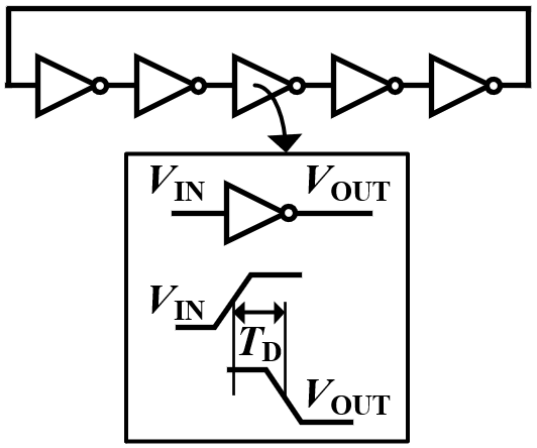
2.3. Ring VCOs for an injection-locking multi-clock generator

2.3.1. Basics of ring VCOs for a PLL

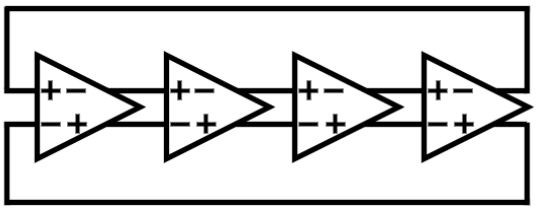
Ring VCOs are actively studied for its utility in terms of size, area, and tuning range. Especially, ring VCOs are noted for its area efficiency since it has no inductor which is very large component in *LC* VCOs. However, the ring VCO has poor phase noise performance compared to the *LC* VCO, then, increasing FOM is challenging. Figure 15(a) shows the basic architecture of the ring VCO with single ended five inverter delay cells. In this architecture, ring VCO's frequency can be represented as,

$$\omega_{\mathrm{OSC}} = \frac{1}{2 \cdot N \cdot T_{\mathrm{D}}}, \tag{3}$$

where N is the number of stages of the ring VCO and T_{D} is the transition time of a delay cell. For the single ended ring VCO, the number of the stages should be odd number to make dc phase shift 180°. If we want to make ring VCO with even number, we can use differential type of ring VCO as shown in Figure 15(b).



(a)



(b)

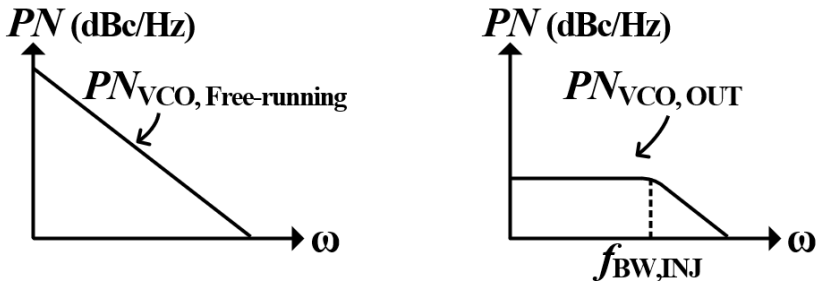
Figure 15. Basic architecture of the ring VCO with (a) single ended five inverter delay cells. (b) differential ended four delay cells.

To align the phase of a VCO to the reference clock, injection locking techniques are widely used. Injection pulse from the reference clock is injected to the VCO to makes the VCO's output frequency locked to $N{\cdot}f_{REF}$ when free-running frequency of the VCO is close to the Nth harmonic of the reference frequency. By realigning the phase of the VCO to the reference clock, the phase noise accumulation of the VCO could be greatly suppressed and the achievable bandwidth of the locked system is much larger compared to a PLL. Figure 16 shows the phase noise configuration of the injection-locked VCO. The transfer functions of the VCO and the reference clock can be represented as [9],

$$\frac{\Phi_{OUT}}{\Phi_{n,VCO}} = 1 - \frac{\beta e^{-j\omega T_{REF}/2}}{1+(\beta-1)e^{-j\omega T_{REF}}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}, \tag{18}$$

$$\frac{\Phi_{OUT}}{\Phi_{n,REF}} = \frac{N\cdot\beta e^{-j\omega T_{REF}/2}}{1+(\beta-1)e^{-j\omega T_{REF}}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}. \tag{19}$$

From above equations, through the injection-locking techniques, the input reference clock's phase noise just scaled with N factor, and VCO's phase noise high-pass filtered according to the β factor, which is the phase realignment factor. Then, when the flicker noise of the VCO is neglected, phase noise of the VCO at the output is shown in Figure 16(b), where the free-running VCO's phase noise is shown in Figure 16(a).



(a) (b)

Figure 16. Phase noise of VCO at (a) $\Phi_{n,VCO}$. (b) Φ_{OUT}.

2.3.2. Design of ring DCOs for a PLL

Ring digitally controlled oscillators (DCOs) are used for multi-clock generators in [2]. Reference [2] presents time-interleaved all-digital calibrator with injection locking techniques. For multiple output clock generation, multiple VCOs are required, therefore, area-efficient ring-type VCOs are adopted. Also, to increase the area efficiency, calibration circuits are operated digitally, then, DCOs are used. Since ring DCOs have poor phase noise performance, injection locking technique is applied to achieve ultra-low phase noise. In this work, ring DCOs are real-time calibrated by time interleaved fashion with MUX, TDC, DLF, and replica-ring VCO. Since calibration bandwidth of the time-interleaved calibrator is narrow, injection locked technique is applied to ring DCOs due to its large locking bandwidth. Therefore, poor ring DCOs' phase noise could be suppressed enough.

Figure 17 shows the design of the ring DCO with 8-bit capacitor bank which consisted of 5 single-ended inverter cells. Since the ring VCO's frequency depends on the load capacitance and the load currents, to control the T_D of the inverter cell, capacitor bank was designed as Figure 18. In Figure 18, load capacitance is controlled by the 8-bit digital code, *SW*<7:0>. Switches for each binary sized capacitor should be also binary sized. This makes each capacitor's series R_{ON} as binary values, then, this increases linearity of the capacitor banks. Controlling capacitance for manipulate the frequency of the VCO can be burden for high frequency generation, however, it can avoid the flicker noise and headroom issue of an architecture using digitally controlled current sources. In [2], for real-time calibration of the ring DCOs, one replica-DCO was used for detecting the phase error of each DCOs, mismatches between DCOs are critical. Additionally, since the fractional injection technique is applied in that work, mismatches between inverter cells in DCO are also critical. To prevent this issue, layout is carefully operated such that metal line path between each cells and loadings are carefully matched.

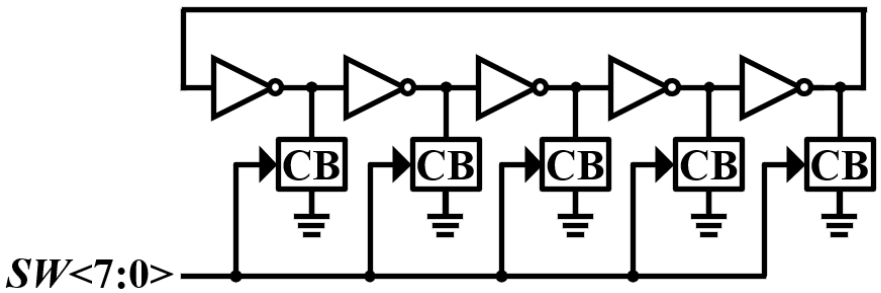


Figure 17. Ring VCO with 8-bit capacitor bank (CB).

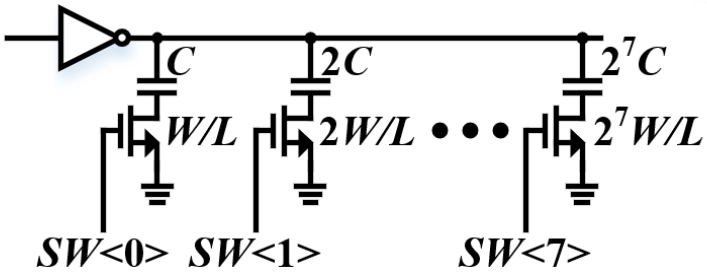


Figure 18. A single inverter cell with 8-bit capacitor bank.

2.3.3. Simulation results

Ring DCOs of the Figure 17 was designed in 65 nm CMOS technology for the architecture of [2]. The target frequency of the DCOs were from 900 to 1200 MHz. Figure 19 shows the simulation result of the phase noise performance of the ring DCO at the output frequency of 960 MHz. In simulation result, a DCO consumes 2.7mW, 1MHz offset spot noise is -110 dBc/Hz, therefore, FOM of -165 was achieved. Injection locking technique is applied to the ring DCO, and the result is also plotted in the Figure 19. Since the injection locking bandwidth is approximately 40 MHz, phase noise performance follows the clean reference clock at the in-band region. At the out-of-band, the VCO's phase noise follows the free-running VCO's phase noise. Figure 20 shows the simulation result of the frequency according to capacitor bank. It is perfectly monotonous, however, there is inevitable nonlinearity. It caused from the fact that VCO's frequency is not proportional to capacitance, but inversely proportional. Additionally, since the frequency step per 1-bit is narrow enough, excellent phase noise performance was achieved through the injection locking techniques. Output frequency range is from 822 to 1236 MHz which covers target output range enough which is from 900 to 1200 MHz.

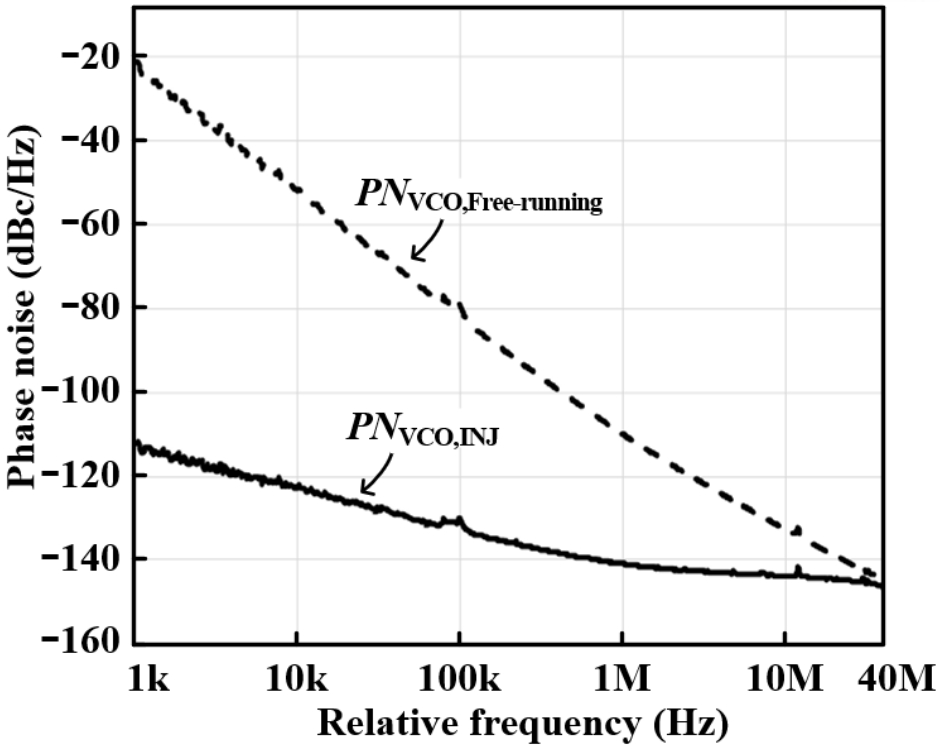


Figure 19. Free-running phase noise of the ring VCO and the shaped phase noise after injection locking at 960 MHz.

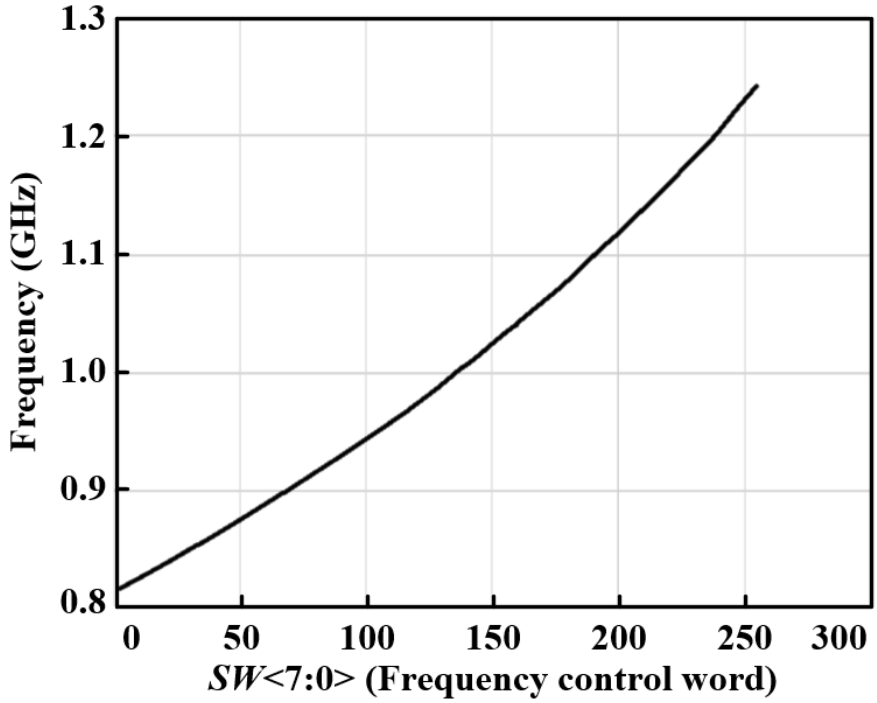


Figure 20. Frequency configuration according to capacitor bank's frequency control word, *SW*<7:0>.

III. High-frequency clock synchronization

3.1. Delay-locked loops (DLLs)

Figure 21 shows the block diagram of a conventional DLL architecture. It consists of a phase detector (PD), a CP/LF, a voltage-controlled delay line (VCDL), and a coarse frequency selection (CFS) circuit for initial frequency band selection. When the DLL is locked, the total delay of the VCDL is equal to reference period, T_{REF}. By using each delay cell's edges, it could be used for a synchronization circuit or a clock multiplier with edge combiner.

Comparing to PLLs, DLLs have several advantages in terms of stability and loop bandwidth [10]. In the PLL, a VCO acts like an accumulator while jitter accumulated, which generates an origin pole. Since LF has an origin pole also, PLL stability issue is critical. However, VCDL has no origin pole, then, DLL becomes an one-pole system. Since the stability issue is relaxed, the bandwidth can be extended, which results fast settling time. In addition, since there is no cycle-to-cycle jitter accumulation in delay cells, output jitter follows the jitter of the clean reference clock.

Harmonic-locking problem is a main issue in DLL. Since the PD detects only the phase difference between the output signal of the VCDL and the reference clock signal, not the frequency difference, VCDL output frequency can be locked to harmonic frequency of the reference frequency such as $2f_{REF}$ or $1/2f_{REF}$. To prevent the harmonic-locking, CFS commonly used for initial frequency band selection.

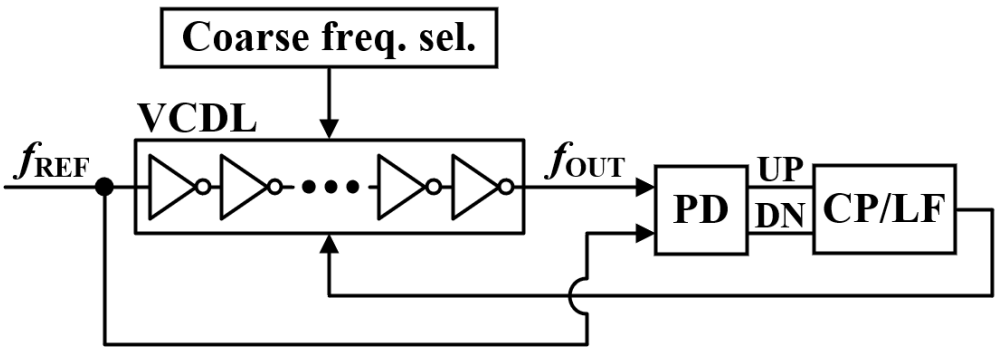


Figure 21. Block diagram of a conventional DLL architecture.

3.2. Architecture of wide harmonic-locking-free DLL

Figure 22 shows the overall structure of a band selecting circuit (BSC) consisting of an exponential digital-to-analog converter (EDAC), a low-dropout regulator (LDO), and a binary-searching engine (BS). The BSC rapidly calibrates the VCDL's total delay, T_{VCDL}, to a proper frequency band which can avoid the harmonic-locking problem according to the target f_{IN} before the DLL's fine tuning begins its locking mechanism to avoid harmonic locking. While the BSC is operated, the BS compares the amount of T_{VCDL} with T_{IN}, i.e., $1/f_{IN}$. During the initial band calibration with BS, the BS uses a bang-bang phase detector (PD) (BBPD) to compare the timing of the VCDL's output signal with the DLL's input signal. The digital code $k<3:0>$ is updated sequentially from the MSB to the LSB based on the BBPD's output polarity. The following DAC converts $k<3:0>$ to the analog voltage, V_k, and the LDO supplies the VCDL's power by setting the supply voltage of the VCDL, V_{COAR}, at V_k. After the $k<3:0>$ value is specified according to the binary-searching result, the VCDL's total delay is close to the input reference clock's period, T_{IN}. To consider enough timing margin, the decision time for each bit of $k<3:0>$ consumes $3T_{IN}$. Total binary searching time for band selection is $12T_{IN}$. If the BSC uses a typical linear DAC (LDAC), a collection of Vk values is consisted of uniformly spaced voltages. Nevertheless, since the proposed EDAC can produce a collection of Vks following an exponential curve that covers a far wider voltage range for a certain bit number. The VCDL was composed of 8-stage, differential type delay cells that provide fairly linear frequency-tuning properties for its supply voltage, V_{COAR} [7]. Therefore, it can also generate a collection of frequency bands approximated as an exponential function of k.

As the initial frequency band selected by the BSC, EN_{FINE} is set to be 1, and the PD begins to detect the phase error information of the output signal of the VCDL, S_{OUT}, comparing to the input reference signal, S_{IN}. Using this detected information, the following CP updates the fine-tuning voltage, V_{FINE}, which is the voltage level of the C_L, and makes T_{VCDL} be same with T_{IN}. In Figure 22, S_{MID} is the signal at the middle of the VCDL chain, i.e., the output of the 4th stage among the 8-stages, which is expected to have an inverted phase with S_{OUT} when the delay of the VCDL locked to T_{IN}. To ensure that harmonic locking is avoided by the use of the initial band-selection technique, as was done in this thesis, the condition for each of the initial values of T_{VCDL}, i.e., T_{INIT}, should meet the following condition [4]:

$$0.5T_{IN} < T_{INIT} < 1.5T_{IN}. \tag{20}$$

The above condition can be transformed to the frequency domain as

$$0.66\,f_{IN} < f_{INIT} < 2\,f_{IN}. \tag{21}$$

Further from (2), $f_{INIT}[k]$ is the discrete expression of $1/T_{INIT}$. When the LDAC's bit number is N_{DAC}, k can be one of the numbers from 0 to 2^{NDAC}-1. Fulfilling the Equation (2) is sufficient to avoid harmonic locking. Nonetheless, for the practical design, enough overlaps between $f_{INIT}[k]$s are needed, as the value of $f_{INIT}[k]$ could be varied significantly by the initial PVT variations. Getting an implementation margin of more than fifty percent on both sides, (2) can be transformed to

$$f_{IN} < f_{INIT}[k] < 1.2\, f_{IN}. \tag{22}$$

According to (3), $f_{INIT}[k+1]$ should be less than $1.2f_{INIT}[k]$ for each k in order to avoid harmonic locking problem all over the range of f_{IN}s. Then, when using a typical LDAC, the kth frequency band, $f_{INIT,LDAC}$[k], can be expressed as

$$f_{INIT,LDAC}\,[k] = (1 + 0.2k)\, f_{INIT,LDAC}\,[0]. \tag{23}$$

However, if the EDAC is used, the kth frequency band, $f_{INIT,EDAC}[k]$, can be expressed as

$$f_{INIT,EDAC}[k] = (1.2)k\, f_{INIT,EDAC}[0], \tag{24}$$

where $f_{INIT,LDAC}[k]$ and $f_{INIT,EDAC}[k]$ in (23) and (24), respectively, are the same in that both can fulfill the Equation (22). Nonetheless, there exists the essential difference that $f_{INIT,EDAC}[k]$ is a sequence of geometric, while $f_{INIT,LDAC}[k]$ is a sequence of arithmetic. Therefore, a much smaller range of k is needed for $f_{INIT,EDAC}[k]$ for covering the same range of f_{IN}, which means that EDAC absolutely have a less value of NDAC compared to a LDAC. For instance, LDAC requires N_{DAC} value of 6 to cover one-decade range of f_{IN}, while EDAC only requires 4. For covering two decades of input frequency range, LDAC requires as many as 9, while EDAC only needs 5. Consequentially, as the target frequency range for f_{IN} increases, the advantage of the EDAC becomes more evident. It's because the EDAC efficiently scales the size of the steps between the frequency bands which means it has a narrow step for low-frequency bands, but it has a wide step for high-frequency bands of f_{IN}. Thanks to the band selection mechanism using the EDAC, the proposed DLL achieved a wide harmonic locking-free range with less DAC numbers, which means it consumed small power and silicon area for the design compared to the counterpart of using LDAC.

Figure 23 shows the simulated results of the timing diagram of the proposed DLL using Cadence Virtuoso when the target frequency is 500 MHz. T_{VCDL} is the delay of the VCDL, V_{FINE} is the finely tuned control voltage for VCDL, and k is the EDAC output code. During the coarse tune, the binary search engine operates to make the delay of the DLL, T_{VCDL}, be near of the target frequency which satisfies the condition of (22) in the thiesis. Binary searching starts from k <3:0>= 1000_2 and comparing

the rising edge of the reference signal and the output signal of the DLL, S_{OUT}, to detect which one is fast. By changing the EDAC code from MSB to LSB, binary searching can be done within 4 times of the coarse calibration. Each detection consumes $3 \cdot T_{REF}$ to ensure sufficient timing margin, and a setup time consumes $1 \cdot T_{REF}$ for conversion from coarse tuning to fine tuning mode. In results, the coarse tuning is done within $13 \cdot T_{REF}$ (=$(4 \cdot 3+1) \cdot T_{REF}$). Therefore, coarse tuning can be done within 130 ns in the worst case when the reference frequency is 100 MHz. If we make a DLL with a linear DAC, to cover 100-1500MHz with the condition of (23), we need 7-bit DAC. Then, if we use the same binary search logic, coarse tuning time increases to $22 \cdot T_{REF}$ (=$(3 \cdot 7+1) \cdot T_{REF}$). Therefore, coarse tuning time increases 220 ns in the worst case when the reference frequency is 100 MHz which is 170% longer than the worst case coarse-tuning time of the proposed DLL with EDAC with the condition of (24). Figure 24 shows that the fine loop settles before 500 ns (=$250 \cdot T_{REF}$).

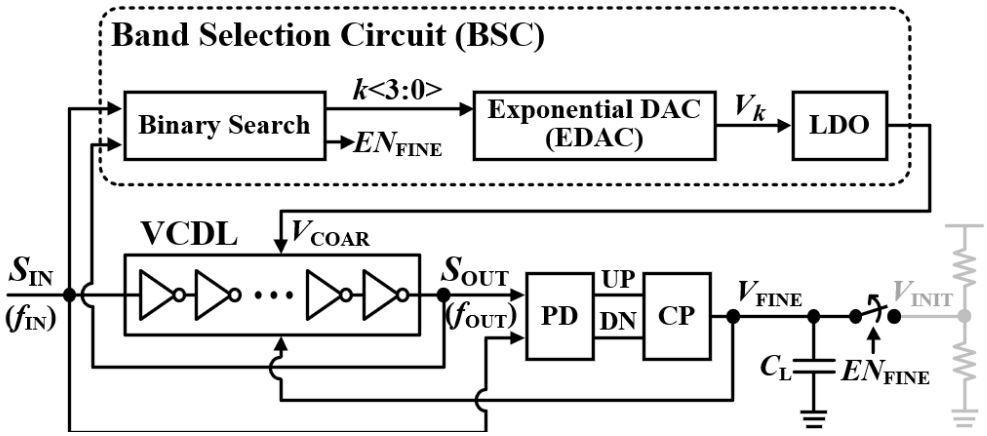


Figure 22. Overall structure of the proposed DLL.

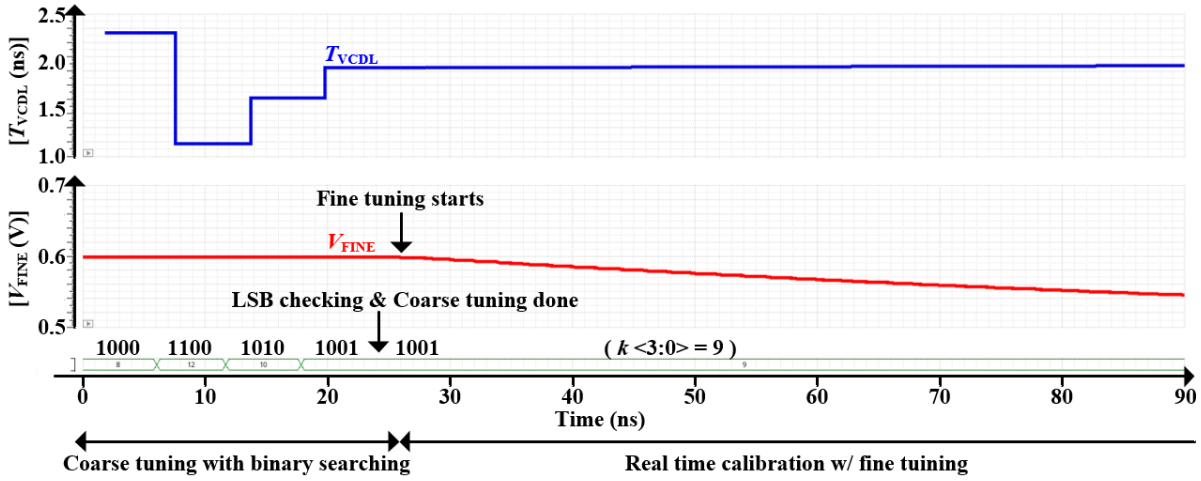


Figure 23. Timing diagram for coarse tuning of the proposed DLL.

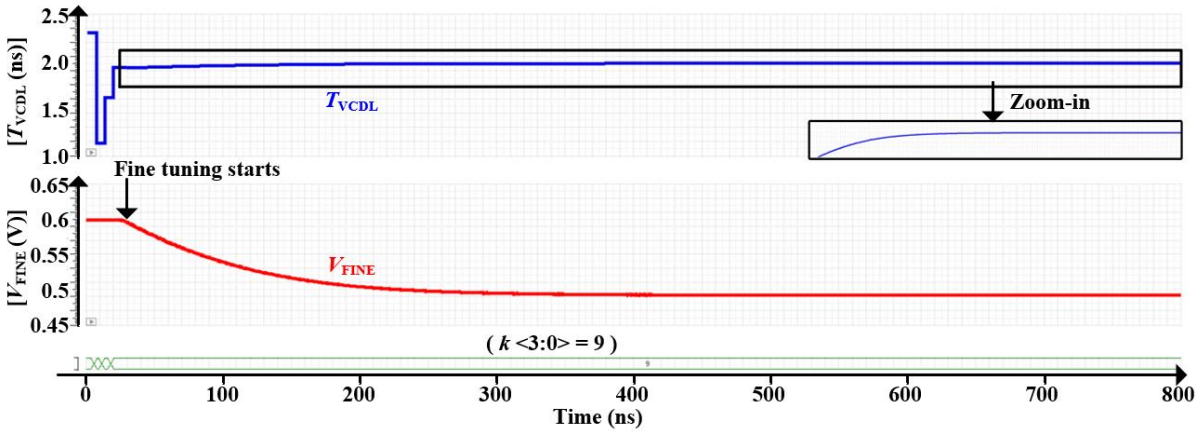


Figure 24. Timing diagram for fine tuning of the proposed DLL.

3.3. Design of core building blocks

3.3.1. The exponential digital-to-analog converter (DAC)

Figure 25 shows the schematics of the proposed EDAC consisting of resistors having one of three resistances, i.e., $R1$, $R2$, and $R3$, and a multiplexer (MUX) selecting one of $V[k]$s and outputs it as V_k. In this thesis, to make the range of f_{IN} more than a decade, the number of N_{DAC} was designed to 4, thus, k ranges from 0 to 15. The left side of Figure 25 shows that a set of resistors is positioned vertically between V_{HIGH} and V_{LOW}, where V_{HIGH} is the highest and V_{LOW} is the lowest reference voltage. The string of resistors is consisted of 15 series $R1$-resistors from the highest-voltage side and a $R2$-resistor at the lowest-voltage side. Then, resistors which value is $R3$ are attached along the resistor string to each of the 14 nodes between $R1$-resistors. The voltage between the last $R1$-resistor and the $R2$-resistor is $V[0]$, and V_{HIGH} is $V[15]$. The core idea of the EDAC design is to make the R3 value be equal to $R2 \cdot (1 + R2/R1)$. Thereby, all equivalent resistances looking down through any of the nodes of the resistor string, R_{EQ}s, become the same value with $R2$, and this is the key mechanism of the proposed EDAC that yields a geometric sequence. The right side of Figure 25 describes the procedures of proving. It uses the method of recurrence and eventually drives the general equation of $V[k]$ following the sequence of geometric:

$$V[k] - V_{LOW} = (V_{HIGH} - V_{LOW}) \times (1 + R_1/R_2)^{k-15}. \quad (25)$$

Then, by making the ratio of $R2$ to $R1$ 1 to 5, a geometric ratio of 1.2 can be attained to satisfy the Equation (24).

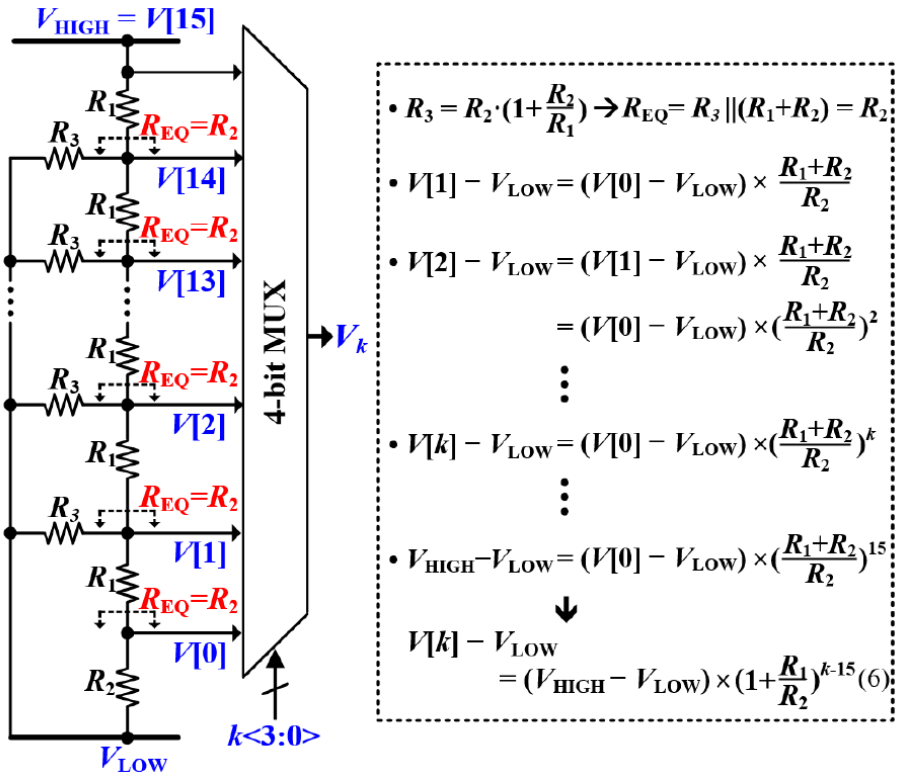


Figure 25. Schematics of the proposed EDAC and generation process of $V[k]$s which follows the sequence of geometric.

3.3.2. High-speed PD

The low power and high-speed PD was implemented as shown in the above side of Figure 26. When the PD is used, not PFD, the DLL can operate immediately without any additional initial state setting after the coarse tuning is done since the phase difference between REF and OUT is always less than π. The below side of Figure 26 shows the operating timing diagram of the proposed PD. EN generates windows to properly detect the phase difference. Delay τ is a dead-zone to switch CP fully when PD generates very narrow pulses.

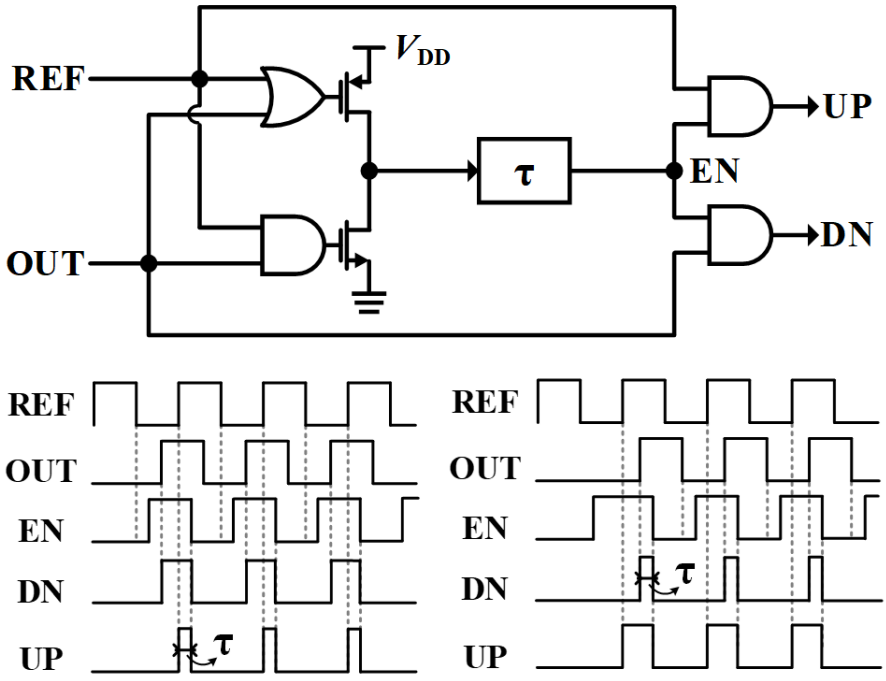


Figure 26. Schematics and conceptual timing diagram of the high-speed PD.

4.4. Measurement results

The proposed DLL was fabricated in a 65nm CMOS process. As shown in Figure 27, the total active area was 0.052mm2 and the EDAC occupied only 0.004mm2. The DLL consumes 5.5mW at f_{IN} of 1.0 GHz. In Figure 28, the measured curve of $f_{INIT,EDAC}[k]$ according to k, which ranges from 0 to 15. For this measured curve, DLL operated BSC only. For each k, input signal, S_{IN}, was tuned manually till the phase difference between S_{OUT} and S_{MID} became 180°. As shown in Figure 28, where the frequency of $f_{INIT,EDAC}[k]$ ranges from 100 to 1500 MHz, the measured curve was closely fit to the graph of $(1.2)^k f_{INIT,EDAC}[0]$. This can be possible due to frequency of the delay cells of the VCDL was linearly tuned in terms of V_{COAR} which was from the output of the EDAC. Even though there occurred the slight deviation of the measured curve from the fitting curve, the DLL can safely avoid harmonic locking problem in the input frequency range of 100 to 1500 MHz thanks to enough margin of (22). Figure 28 shows the frequency range of f_{IN} can be reached above 1500 MHz, however, the delay range of the VCDL limited the range. Corner simulations for the frequency range are operated. When the corner condition is FF, 0°C, the frequency range of $f_{INIT,EDAC}[k]$s changed to 140-2000 MHz. When the corner condition is SS, 120°C, that range changed to 80 – 1200 MHz. Although there exists some variations, it caused no problem since the harmonic-locking-free ranges of $f_{INIT,EDAC}[k]$s had enough overlaps. Figure 29(a)-(d) shows the measured waveforms of SOUT and SMID where fIN was 0.3, 0.5, 1.0, 1.5 GHz, respectively. Since the SMID was the middle stage of the delay cells and the DLL was locked to SIN, the phase of the S_{MID} had difference of 180° from the phase of the S_{OUT} in all measured output. Figure 30(a) shows the rms jitter of S_{OUT} was 1.99 ps when f_{IN} was 1000 MHz. In Figure 30(b), the 1-MHz phase noise of S_{OUT} was −128 dBc/Hz. The difference of phase noise performance between the input signal and the output signal was generated from the additional noise of the delay cells of the VCDL and the CP. Table. 2 shows that the proposed DLL achieved the widest harmonic-locking-free frequency range of 175% with the use of a 4-bit EDAC to set the initial frequency band. In [5], the DLL used a DAC with 10-bit. In the case of the DLL in [6], the digital code range was able to cover only four-bit linear DAC. In this case, if [6] used the EDAC, it can be covered with only 3-bit DAC with low power. The DLL in [12] achieved a lower jitter, however, it consumes large power and area, and it covered a different frequency range.

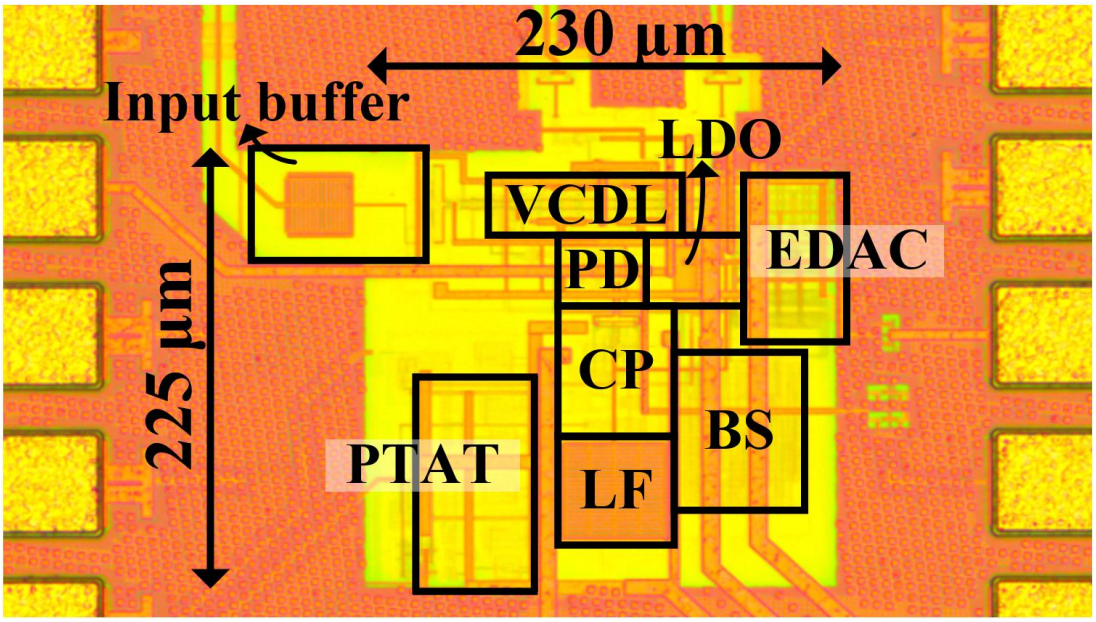


Figure 27. Die photograph.

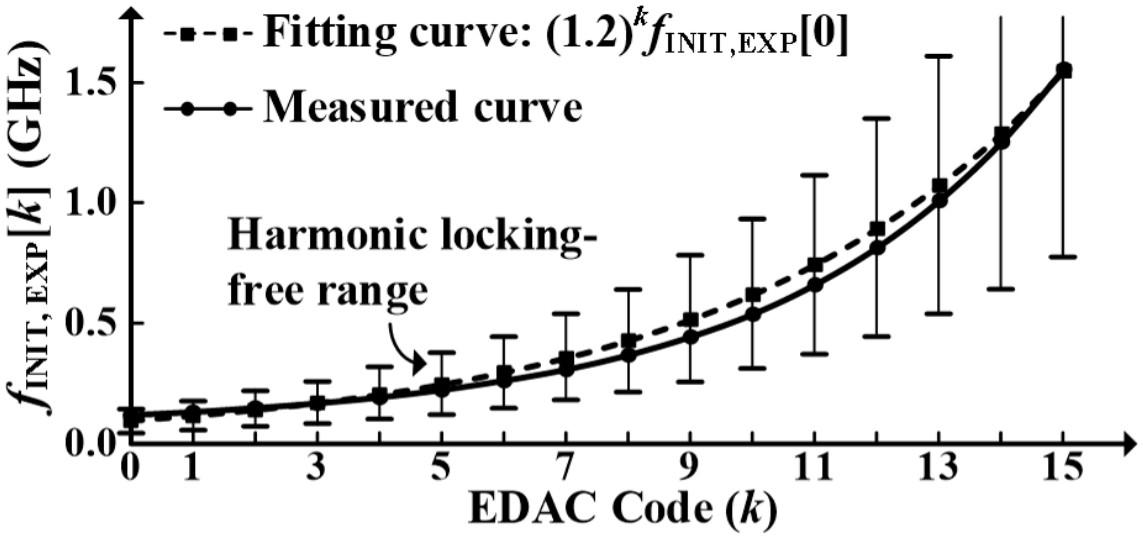
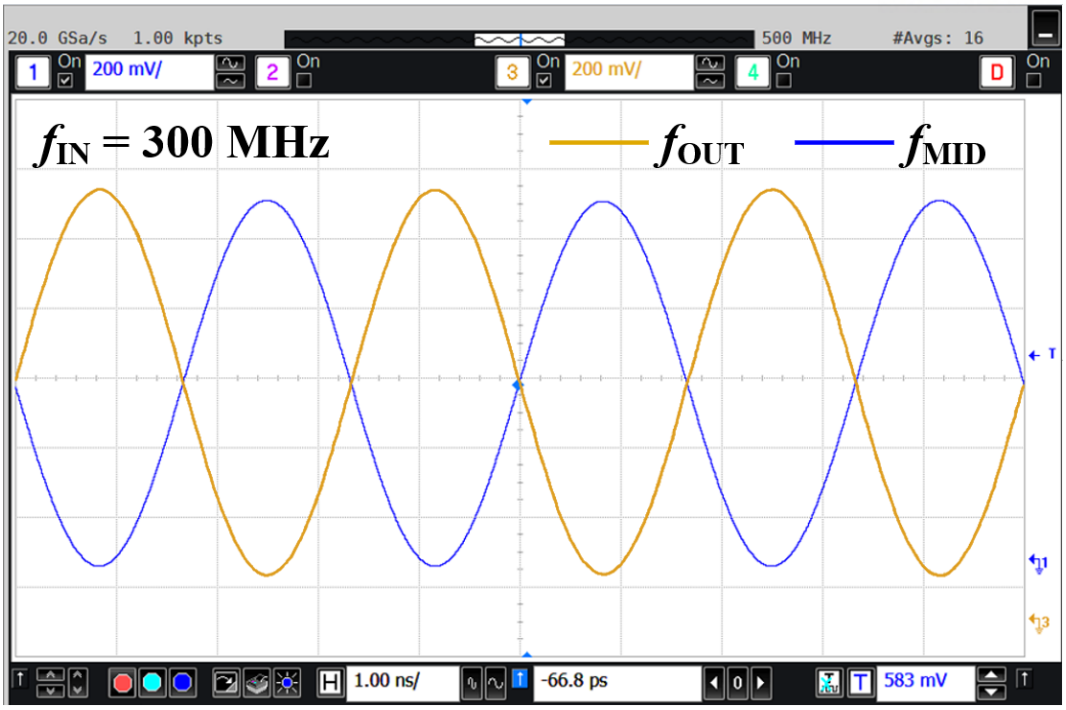
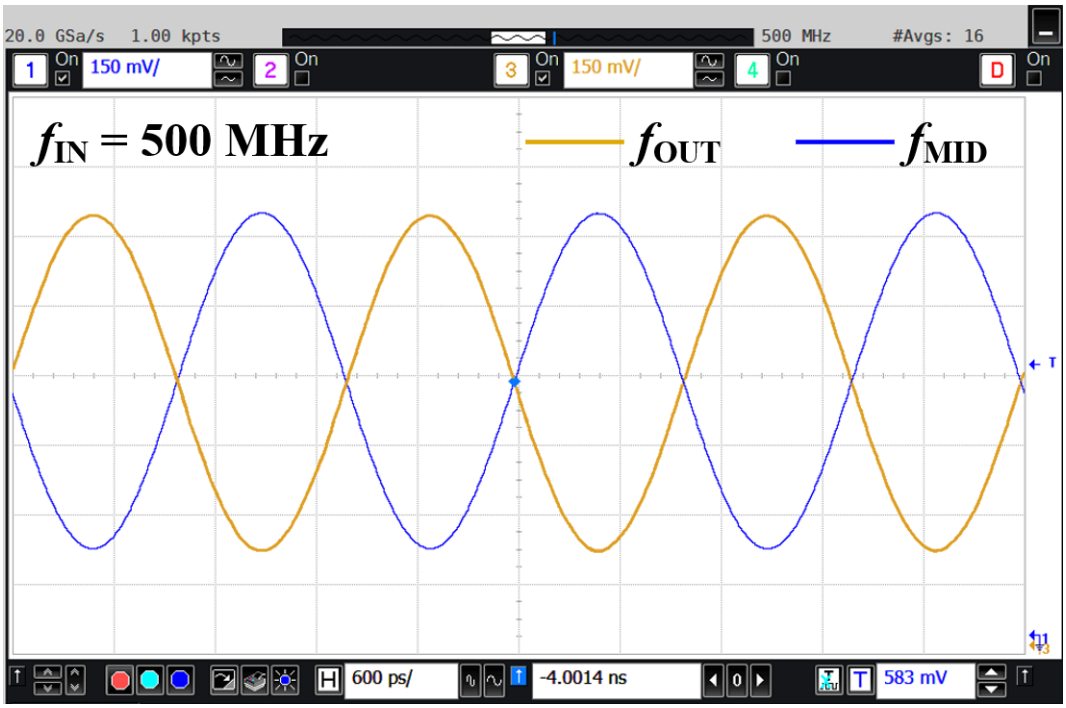


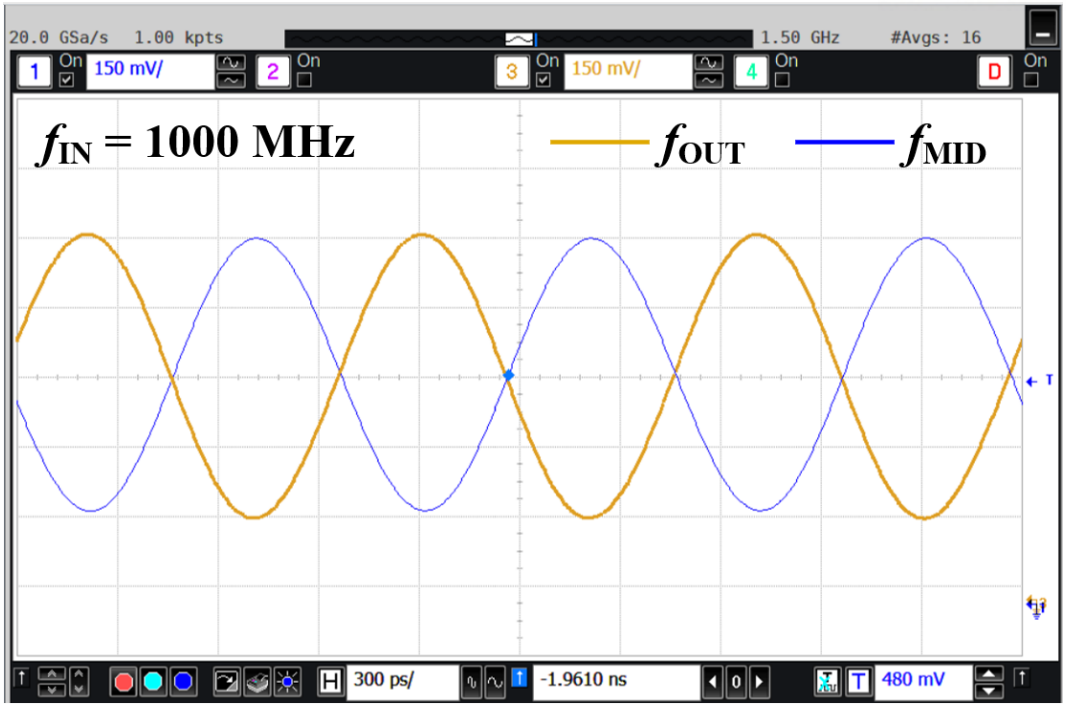
Figure 28. Measured $f_{INIT,EDAC}$[k]s with a fitting curve.



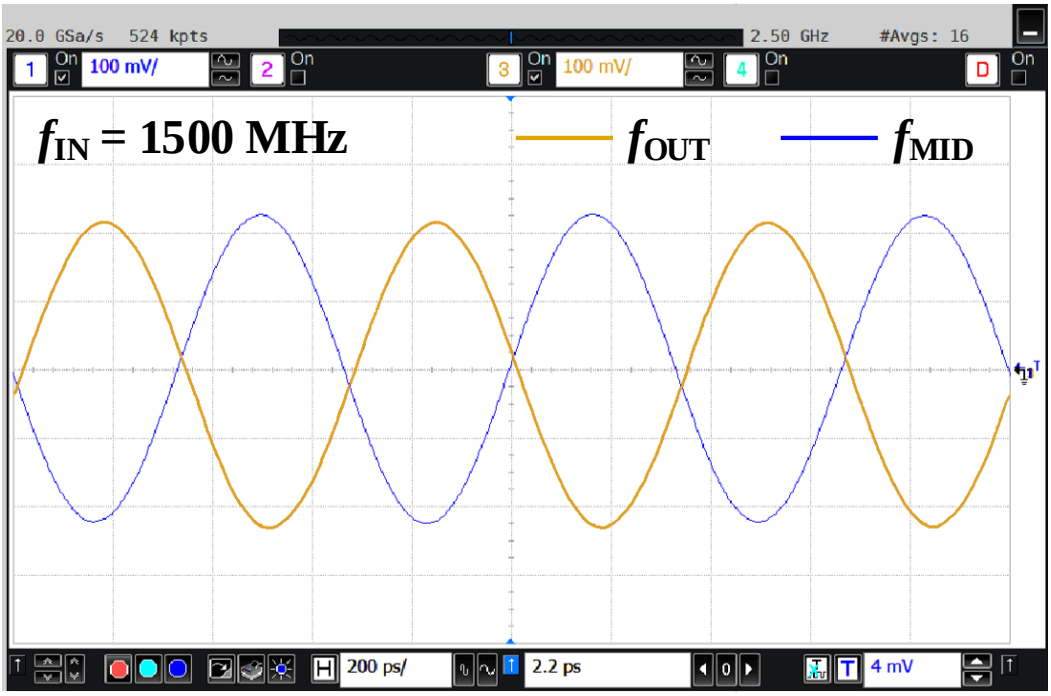
(a)



(b)



(c)



(d)

Figure 29. Measured waveforms of S_{MID} and S_{OUT} at f_{IN} of (a) 300 MHz. (b) 500 MHz. (c) 1000MHz. (d) 1500 MHz.

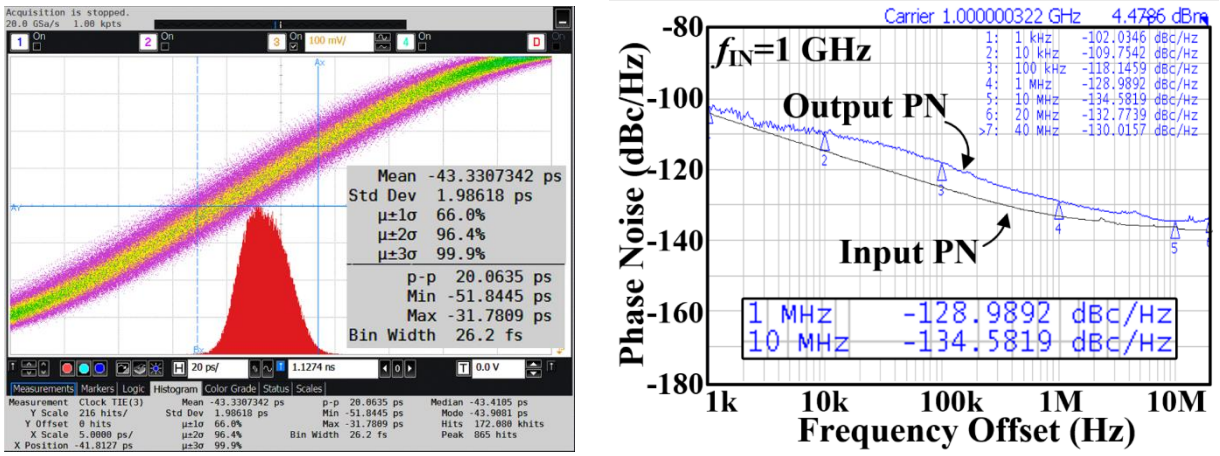


Figure 30. (a) Measured jitter. (b)Measured phase noise of the DLL at f_{IN} of 1000 MHz.

Table 2. Performance comparison of DLL with wide harmonic-locking-free range.

	This work	[3]	[5]	[6]	[12]
Process	65nm	180nm	130nm	130nm	180nm
Frequency range, f_{TR}	100-1500MHz (175%)	85-550MHz (146%)	15-600MHz (190%)	80-450MHz (140%)	900-2900MHz (105%)
Anti-harmonic lock method	Initial band selection	Harmonic-lock detector	Initial band selection	Initial band selection	Divider & switch logics
DAC bit #	4	NA	10	4*	NA
1-MHz PN @f_{OUT}	–128dBc/Hz @1.0GHz	NA	NA	NA	–116dBc/Hz @2.16GHz
JIT_{RMS}/JIT_{PP} @f_{OUT}	1.99/ 20.1ps @1.0GHz	3.8/ 25.6ps @550MHz	9.00/ NA @600MHz	2.32/ 10.0ps @180MHz	1.61/ 12.9ps @2.16GHz
P_{DC}	5.5mW	4.2mW	NA	26.0mW	19.8mW
Area	0.052mm^2	0.258mm^2	0.376mm^2	0.08mm^2	0.07mm^2

* 16 thermal codes for band selection, which can be covered by a four-bit DAC

IV. Conclusions

In this thesis, we designed *LC* VCOs which frequency range of 25-30 GHz for 5G communication band, 5.2-6.0 GHz for LTE, 2.7-4.2 GHz for 2G-4G, respectively. For GHz-frequency band which frequency is relatively low, the *LC* VCO designed with focusing on phase noise performance, and the other two VCOs focused on area and power efficiency, since GHz-band VCO was used in analog CP PLL architecture and the other two VCOs were used with injection locking techniques. Also, we designed ring DCOs for multi-clock generator of [2]. Multiple same ring DCOs were used for multiple clock generation, and a replica ring DCO was used for calibration. Its frequency range was covered from 900 to 1200 MHz with -165 dB FOM. Even though ring DCO have poor phase noise, after injection locked, it can have extremely low jitter. Additionally, we presented a DLL with a wide harmonic-locking-free range. As the proposed EDAC provides a set of control voltages, which follows a geometric sequence, it can cover a very wide range of frequencies for a given number of bit. In the measurement results, the DLL with the EDAC was accurately operated over input frequencies from 100 to 1500 MHz with avoiding any harmonic-locking issues. When fIN was 1000 MHz, the rms jitter of the output signal and the total power consumption was 1.99 ps and 5.5 mW, respectively.

REFERENCES

[1] H. Yoon, *et al*., "A -31dBc integrated-phase-noise 29GHz fractional-N frequency synthesizer supporting multiple frequency bands for backward-compatible 5G using a frequency doubler and injection-locked frequency multipliers," *ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 366–367.

[2] H. Yoon, *et al*., "A Low-Jitter Injection-Locked Multi-Frequency Generator Using Digitally Controlled Oscillators and Time-Interleaved Calibration," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1564–1574, June 2019.

[3] C.-T. Lu, *et al*., "A 0.6V low-power wide-range delay-locked loop in 0.18um CMOS," *IEEE Microw. Wireless Compon. Lett*., vol. 19, no. 10, pp. 662–664, Oct. 2009.

[4] Y.-H. Moon, *et al*., "A 2.2-mW 20–135 MHz false-lock-free DLL for display interface in 0.15 um CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 8, pp. 554–558, Aug. 2014.

[5] S. Hoyos, *et al*., "A 15 MHz to 600 MHz, 20 mW, 0.38 mm2 split-control, fast coarse locking digital DLL in 0.13 um CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*., vol. 20, no. 3, pp. 564–568, Mar. 2012.

[6] D. Zhang, *et al*., "A multiphase DLL with a novel fast-locking fine-code time-to-digital converter," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*., vol. 23, no. 11, pp. 2680–2684, Nov. 2015.

[7] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Pro*. IEEE, vol.54, no. 2, pp.3219–330, Feb. 1966.

[8] D. Banergee, *PLL Performance, Simulation, and Design*, 4th ed., Sirirajmedj Com., 2006.

[9] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits,* vol. 39, p. 1415–1424, Sep. 2004.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGrawHill, 2002.

[11] S. Yoo, *et al*., "A 2–8 GHz wideband dually frequency-tuned ring-VCO with a scalable K_{VCO}," *IEEE Microw. Wireless Compon. Lett*., vol. 23, no. 11, pp. 602–604, Nov. 2013.

[12] Q. Du, *et al*., "A low-phase noise, anti-harmonic programmable DLL frequency multiplier with period error compensation for spur reduction," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1205–1209, Nov. 2006.

ACKNOWLEDGEMENTS

First of all, I sincerely appreciated my advisor, Professor Jaehyouk Choi for all his guidance and support. I am deeply grateful that he has always been my counselor for my research and overall life.

I feel gratitude to my committee members, Professor Kyuho Lee and Professor Seong-Jin Kim for serving the committee members and providing valuable comments.

I am also truly thankful to all members of ICSL. They have always helped and encouraged me.

Finally, I'm also grateful to my parents for their unconditional love and care.