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Doctoral Thesis

Ballistic Carrier Transport Through Graphene
: Out-of-Plane and In-Plane Aspects

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2020

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A dissertation
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Hoon Hahn Yoon

12/18/2019

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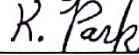
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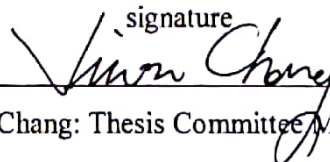
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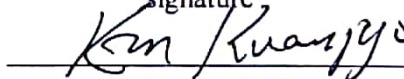
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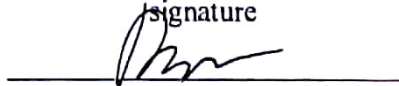
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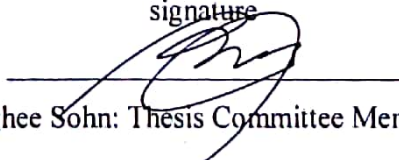
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Abstract

The outstanding properties of graphene have enabled to reveal the exotic carrier transport behavior approaching to the relativistic quantum mechanics, act as the excellent diffusion barrier protecting the junction interface from the material intermixing by atomic diffusion, serve as the effective interlayer modulating the electronic states, and offer the promising solid-state platform allowing the quantum optics of the Dirac Fermion. In this dissertation, the ballistic carrier transport through graphene in two different aspects will be covered. Understanding of vertical transport across graphene-combined hetero-junction and lateral transport in the graphene channel is the main agenda. The sensitive manipulation of electronic states at/across the interface and the controllable distribution of electric potential on the surface can lead to an extraordinary physical phenomenon and conductance switching. Based on that, it is eventually proposed that how the brand-new type graphene-based device can be evolved or what kind of method can be adapted to improve the actual performance of the graphene-based devices significantly regardless of property or quality of graphene.

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Nomenclature

0D	Zero-Dimensional
1D	One-Dimensional
2D	Two-Dimensional
2DEG	Two-Dimensional Electron Gas
3D	Three-Dimensional
Al	Aluminium
Au	Gold
ALD	Atomic Layer deposition
BCT	Ballistic Carrier Transport
BEEM	Ballistic Electron Emission Microscopy
BFTEM	Bright-Field Transmission Electron Microscopy
BOE	Buffered Oxide Etch
CMOS	Complementary Metal-Oxide-Semiconductor
CNL	Charge Neutrality Level
CVD	Chemical Vapor Deposition
DFT	Density Functional Theory
DI	Deionized
FLP	Fermi-Level Pinning Effect
FEEM	Finite Element Electrostatic Modeling
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GS	Graphene Superlattice
HRTEM	High-Resolution Transmission Electron Microscopy
IFL	Image Force Lowering

IPA	Isopropyl Alcohol
IPE	Internal Photo-Emission
I-V	Current-Voltage
Ni	Nickel
PCB	Printed Circuit Board
PCM	Parallel Conduction Model
PMMA	Poly Methyl Meth-Acrylate
Pt	Platinum
RIE	Reactive Ion Etching
RE	Recombinatoin
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscopy
Si	Silicon
SiO₂	Silicon Dioxide
STM	Scanning Tunneling Microscopy
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
Ti	Titanium
TU	Tunneling
UV	Ultraviolet
VGf	Vertical Gradient Freeze

Chapter 1. Introduction

1.1 Motivation

Physics contributes to human lives by understanding basic rules in nature and identifying profound scientific truth. I was particularly interested in condensed matter physics, which deals with physical properties of diverse systems, has infinite potential in wide applications, and establishes the links to real-world from microscopic world. I also felt interest in semiconductor device physics, which gives insights into assembling technological methodologies by encompassing all kinds of study with great creativity.

In the fields of condensed matter physics and semiconductor device physics, modern scientists have witnessed the marvelous revolution employing various low-dimensional materials [1, 2] and novel quantum materials [3, 4]. There have been huge academic interests and enormous research activities regarding the remarkable physical, mechanical, electrical, and optical properties of zero-dimensional (0D) nanocrystals/quantum dots [5, 6], one-dimensional (1D) nanowires/nanotubes [7, 8], two-dimensional (2D) Van der Waals materials [9], superconductors [10], and topological insulators [11]. I have been convinced that the discovery of new material or the development of advanced technology brings innovation research. This is literally state-of-the-art modern alchemy, which explores both fundamental physics and applied science, needs to follow up the cutting-edge nanotechnology, and boosts the infinite potential in next-generation device applications by considering the upcoming industry, and has a great impact on the human lives in the future.

Beyond the conventional device technologies, the technical realization of electronic, photonic, optoelectronic, and spintronic devices by controlling quantum transport is a long-cherished desire of all condensed matter physicists around the world [12, 13]. I could have learned through the doctoral study that the most significant physical phenomena in determining functionality and efficiency of devices occur at the interface where the contact boundaries between the different materials meet. When we recall the famous and inspirational quote, “God made the bulk; surfaces were invented by the devil.” from Wolfgang Ernst Pauli [14], atoms inside the bulk are surrounded by other atoms and remain in their original states, while atoms on the surface are influenced by the external environment and interact with other atoms. Indeed, many scientific breakthroughs have been achieved by surface/interface engineering. The role of electronic states are crucial greatly tuning the energy barrier formation, carrier transport mechanism at/across the interface or on the surface, and device operation characteristics. Likewise, I find the fact that we can predict the use of materials and improve device performance with desired physical properties is remarkably interesting to me.

1.2 Overview

In this dissertation, the two different aspects of ballistic carrier transport through the graphene are studied. The first aspect is the *out-of-plane* ballistic carrier transport across the graphene inserted at the metal/semiconductor interface or the graphene contacted with the semiconductor substrate. The second aspect is the *in-plane* ballistic carrier transport in the graphene under the periodic potentials, so-called the graphene superlattice.

1.2.1 Ballistic Carrier Transport

The number of valence electrons (outer shell electrons) determine the atomic elements. Under an electric field, the valence electrons in metal, the electrons in the conduction band of semiconductor, and holes in the valence band of semiconductor are well known to travel freely. These flow of charged particles carry an electric current following the Ohm's law [15].

In general, charged particles in real solids undergo a lot of intrinsic scattering processes [15-17], originated from electronic Coulomb interaction, phonon, surface roughness, impurity, defect, grain boundary etc. This is why carrier transport in solids is known to be quite diffusive, causing the suppressed response of charge carriers to an external field and the energy dissipation inevitably.

However, in some emerging materials with a certain physical regime, the charged particles can move like billiard balls without the effective scattering processes. This is what we call the *ballistic carrier transport* [18-25]. In the ballistic regime, the kinetic energy is far higher than the lattice potential energy or the mean free path of charge carriers is long enough exceeding the dimension of channel. The energetic carrier acquiring a very powerful kinetic energy is called as the *hot carrier*. The established techniques such as scanning tunneling microscopy (STM) [26-28], ballistic electron emission microscopy [29-31], and internal photoemission spectroscopy (BEEM) [32-34] utilizes the ballistic carrier transport or the hot carrier injection.

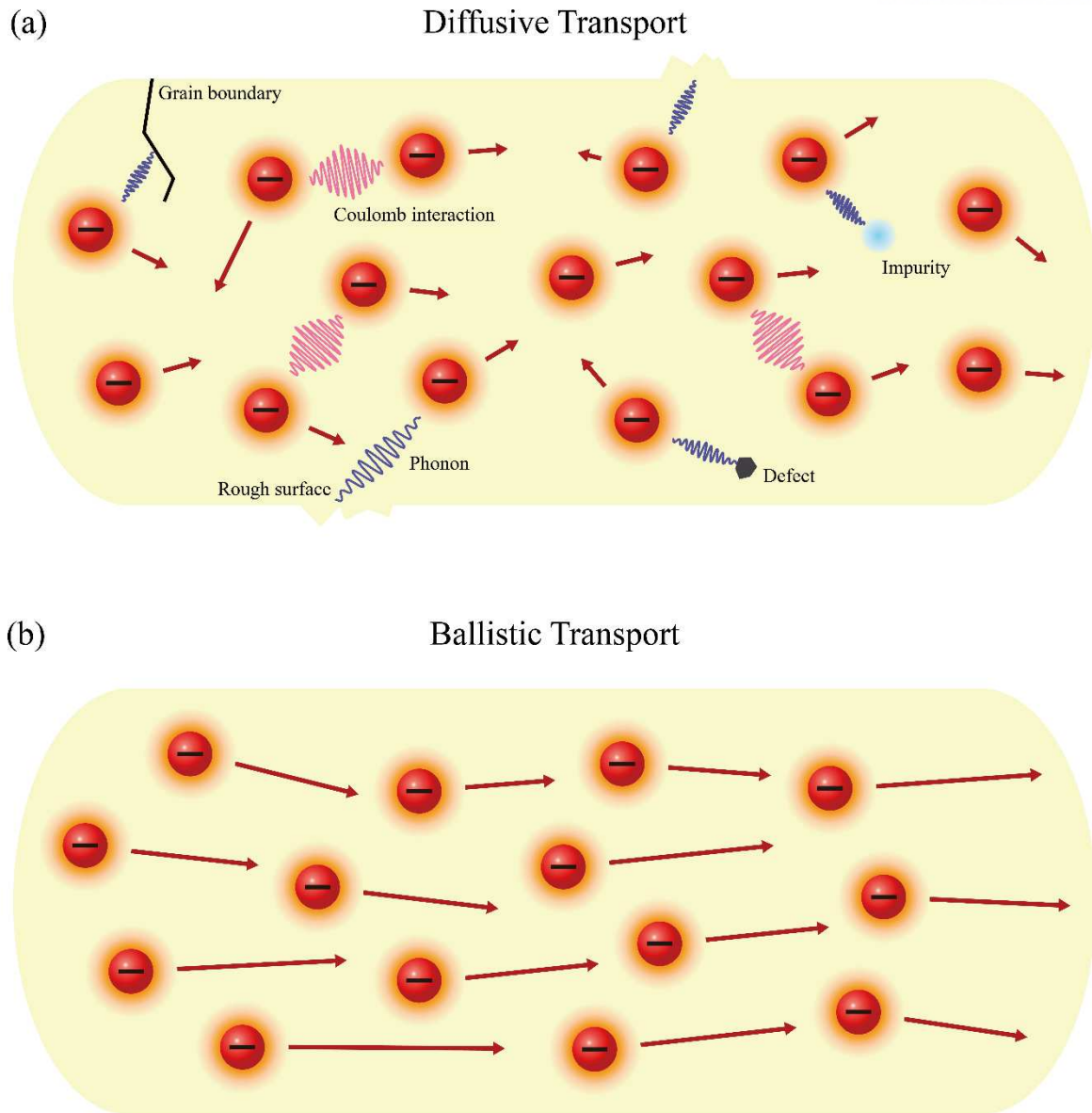


Figure 1. Schematic illustration of comparison between the diffusive (a) and the ballistic (b) transport in solid.

1.2.2 *Out-of-plane* Ballistic Carrier Transport through Graphene

Here, the idea of using graphene as the diffusion barrier or the interlayer is employed to form atomically abrupt Schottky contacts and to obtain the homogeneous energy barrier. The Fermi-level pinning effect at the interface of metal/graphene/semiconductor junction is investigated in-depth by modulating the dependence of energy barrier on the metal work-function, the metal-graphene interaction, and the semiconductor surface state. Thanks to an experience of building the IPE system independently, the energy barrier on the prevailing area was able to be determined without the disruption of charge carrier flow through the low-barrier patches. In the aid of IPE and graphene interlayer, strong Fermi-level pinning effect and unusual negative Fermi-level pinning effect were observed. The parallel conduction model and the finite element electrostatic model were adopted to explain the results theoretically.

Besides, it is clarified how downscaling of electrical contacts or hole carriers supplied from the p-doped graphene layer can affect effective energy barrier and transport mechanism. The forward-bias current measured on the graphene/semiconductor junction is considered to be compromised due to the recombination process regarding the hole carriers injected from p-doped graphene. The temperature-dependent current ratio of recombination to thermionic emission implies the possibility of utilizing the low-temperature operating rectifier.

In addition to that, the effective energy barriers of Schottky junction are found to be reduced with decreasing the lateral size scaling of metal electrode, which is attributed to the thermionic emission and tunneling of charge carriers around the junction edge.

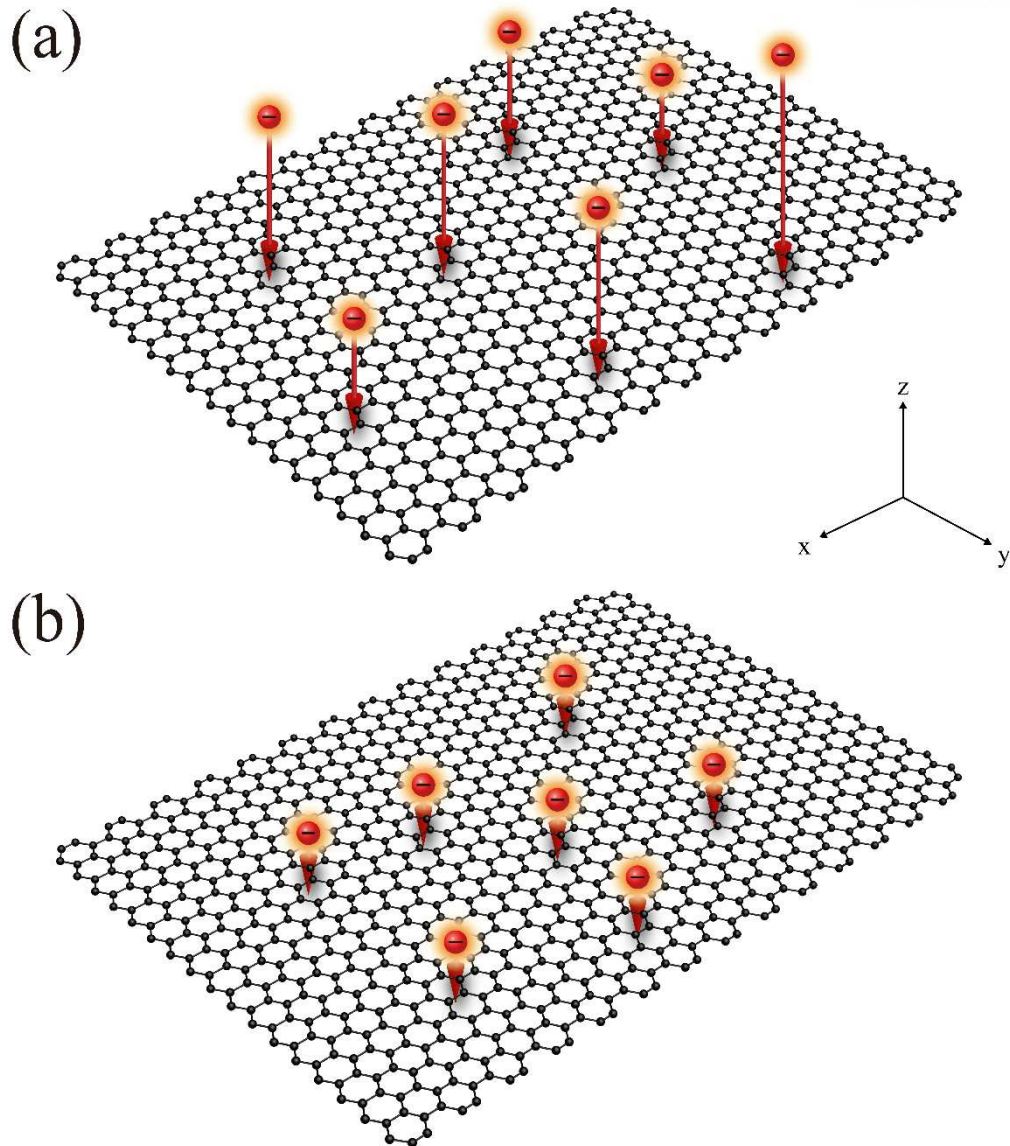


Figure 2. Schematic illustration of the out-of-plane ballistic carrier transport through graphene. (a) Hot carrier injection into graphene. (b) Direct carrier transport from graphene.

1.2.3 *In-plane* Ballistic Carrier Transport through Graphene

Creating a practically available off-state of graphene transistor to overcome the absence of its band-gap, the useful concepts in photon physics are introduced to electron physics. It is demonstrated that the Kronig-Penney type periodic potentials can be installed to realize the single-channel multi-drain graphene device, where the charge carriers can be guided to a desired direction on purpose. The angular spread and propagating direction of electron wave packets in the graphene is found to be manipulated just by tuning the magnitude of bias voltage applied on the superlattice potential or the length of the superlattice period.

In appendix, the square/triangular superlattices partially patterned on the graphene, the artificial randomized defects induced by metal adatom deposition on the graphene, and the Aharonov-Bohm interferometer are also introduced. The modulation of carrier transport properties can give insight into another way to minimize the off-state current.

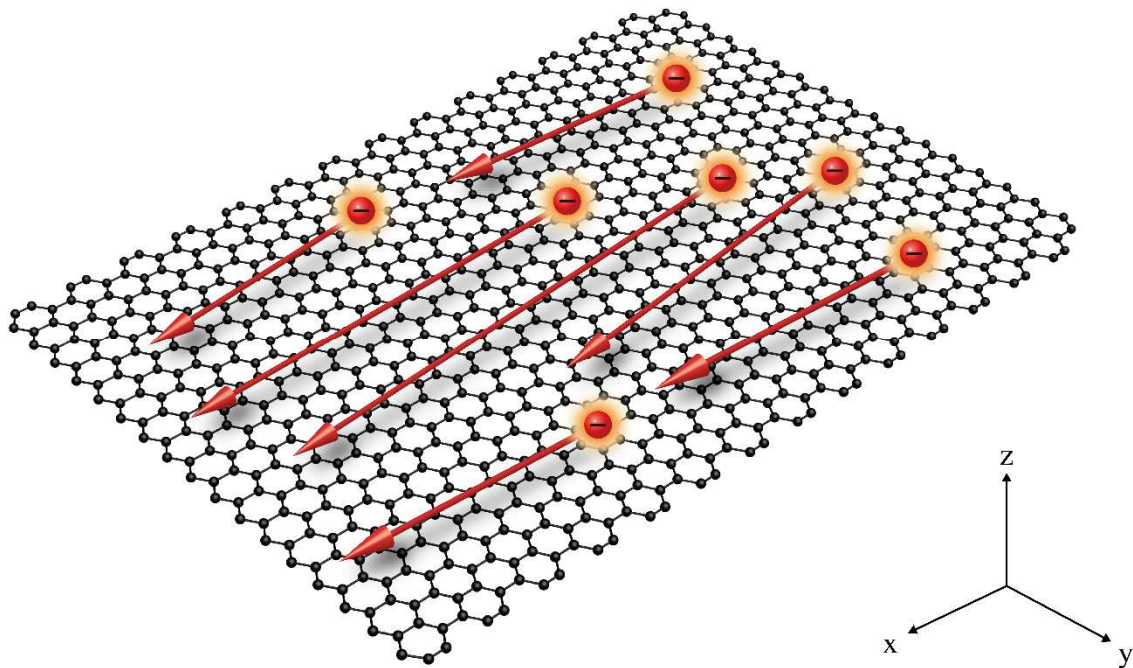


Figure 3. Schematic illustration of the in-plane ballistic carrier transport through graphene.

1.3 Graphene

1.3.1. Research Trend in Graphene

Graphene [35-43], the most well-noted 2D Van der Waals material, has provided a unique opportunity corresponding to the innovation research. In cooperation between the academia and the industry [44], a worldwide movement has taken place continuously to extend the technology boundaries by utilizing the graphene. A new class of graphene-based electronic [45-48], photonic/optoelectronic [49-52], spintronic [53-56], transparent/flexible [57-62] devices have been explored widely. The relativistic quantum phenomena and ballistic carrier transport in the 2D graphene system makes possible to develop electron quantum optics [63-67] relying on the Klein tunneling [68-72], which incorporates the essential components of photon physics such as focusing [73-77], angle-dependent transmission [78-82], collimation [83-87] (through periodic potentials [88-92], *i.e.*, superlattice [93-97]), reflection [98-102], interference [103-107] (including the Aharonov-Bohm oscillation [108-112]), localization [113-117], confinement [118-122]. An important role of graphene in practical use has been also reported to integrate into semiconductor devices rather than to compete with well-developed Si-based CMOS technology [123].

However, it has been pointed out that there are several disadvantages of graphene for real device applications. The major limitation comes from zero band-gap and lattice imperfection. Although there had been research activities to open the band-gap of graphene [124-129], heal the structural defects in the graphene [130-135], and control the current flow using local/tunable gate applied on the graphene transistor [136-142], establishing a completely tunable and reliable way for graphene-based electronics have remained as a challenging task. Besides, other comparable 2D Van der Waals materials [143-146] have appeared at the contest stage to challenge the limits of graphene.

Accordingly, the aim of research for graphene has been expanded and diversified in order to increase the utility of graphene, which can be categorized as metal adatom on the graphene [147-150], graphene Schottky diode [151-154], graphene barrister [155-158], electrical contact between graphene and other materials [159-162], charge transfer induced doping of graphene [163-166], charge transport through graphene hetero-junction [167-170], vertically stacked Van der Waals hetero-junctions consisting of graphene [171-174], and graphene diffusion barrier or interlayer inserted at metal-semiconductor interfaces [175-178], etc.

1.3.2 Massless Dirac Fermion in Graphene

It is known that the four valence electrons of a carbon atom denote one $2s^1$ -orbital and three $2p^3$ -orbitals (Figure 4a). The mechanical and electrical properties of graphene relies on its atomic orbital of carbon. The orbital hybridization composed of three sp^2 -orbitals (Figure 4b, left) forms the σ -bonds and builds up the trigonal planar geometry (Figure 4c). This lead to the mechanical robustness and material flexibility [179-182]. The remaining unaffected p_z -orbital (Figure 4b, right) is vertically aligned to the plane. As a result, its overlapping produces the π -bands (Figure 4c), which is responsible for gapless band structure, linear energy dispersion, helicity, zero effective mass, high carrier mobility, bipolar nature, and electrically-tunable carrier type/concentration [15-23].

The distinct feature of graphene allows electron near the Dirac points to propagate along the graphene sheet like a massless relativistic particle. The electron has an effective speed comparable to the light called as the Fermi velocity $v_F \equiv \frac{\sqrt{3}\gamma a}{2\hbar} \cong 10^6$ m/s, where $\gamma \cong 2.8$ eV is the hopping energy between nearest neighbors, $a \cong 2.46$ Å is lattice constant, and \hbar is the plank constant.

$$E = s\gamma \sqrt{1 + 4\cos^2\left(\frac{k_y a}{2}\right) + 4\cos\left(\frac{k_y a}{2}\right)\left(\frac{\sqrt{3}k_x a}{2}\right)} \quad (1)$$

Equation 1 shows the energy dispersion relation derived from the tight-binding model [183-185] in consideration of the first-nearest-neighbor interaction, where s is the band index due to the helicity (1 for the conduction band and -1 for the valence band), k_x and k_y are the components of Bloch wave-vector.

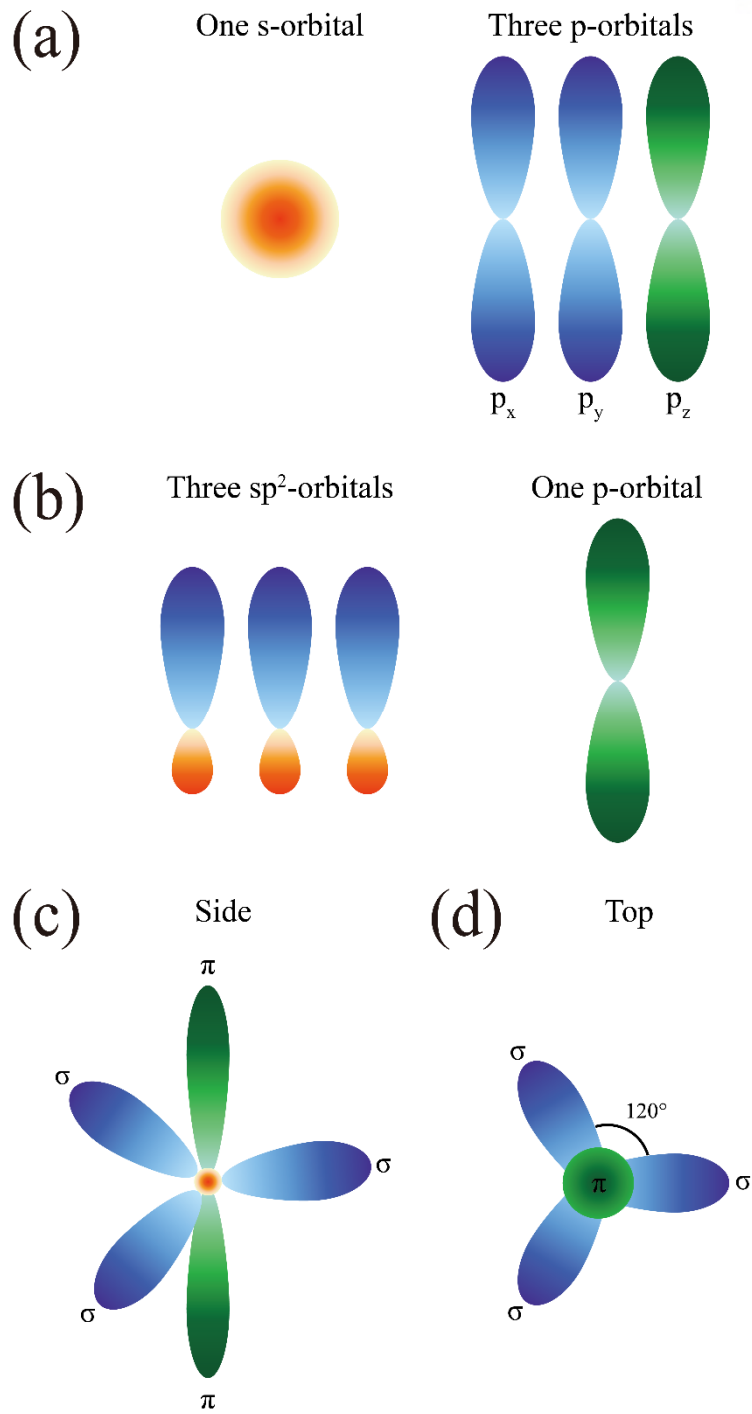


Figure 4. Orbital configuration and the bonding of the graphene. (a) Orbitals of a carbon atom. (b) Hybridized sp^2 -orbitals and remained p-orbital. (c) Orbitals of the graphene showing the σ bonds and π bands in trigonal planar geometry

As shown in Figure 5, the lattice structure consists of triangular two equivalent sublattices. In real space, the length $a_0 = \frac{a}{\sqrt{3}}$ between carbon atoms is approximately 1.42 Å and the unit cell is defined by the primitive lattice vectors $\vec{a}_1 = \sqrt{3}a_0\hat{x}$ and $\vec{a}_2 = \frac{\sqrt{3}}{2}a_0(\hat{x} + \sqrt{3}\hat{y})$. The area of unit cell is $\frac{3\sqrt{3}}{2}a_0^2$. The vectors connecting to the other sublattice are expressed as $\vec{\delta}_1 = \frac{a_0}{2}(\sqrt{3}\hat{x} + \hat{y})$, $\vec{\delta}_2 = \frac{a_0}{2}(-\sqrt{3}\hat{x} + \hat{y})$, and $\vec{\delta}_3 = -a_0\hat{y}$. In reciprocal space, the reciprocal lattice vectors $\vec{b}_1 = \frac{2\pi}{\sqrt{3}a_0}\left(\hat{x} - \frac{1}{\sqrt{3}}\hat{y}\right)$ and $\vec{b}_2 = \frac{4\pi}{3a_0}\hat{y}$ can be derived from $\vec{a}_i\vec{b}_j = 2\pi\delta_{ij}$. The reciprocal lattice constant is $b = \frac{4\pi}{\sqrt{3}a} = \frac{4\pi}{3a_0}$ and the reciprocal lattice spacing is $b_0 = \frac{4\pi}{3a} = \frac{4\pi}{3\sqrt{3}a_0}$.

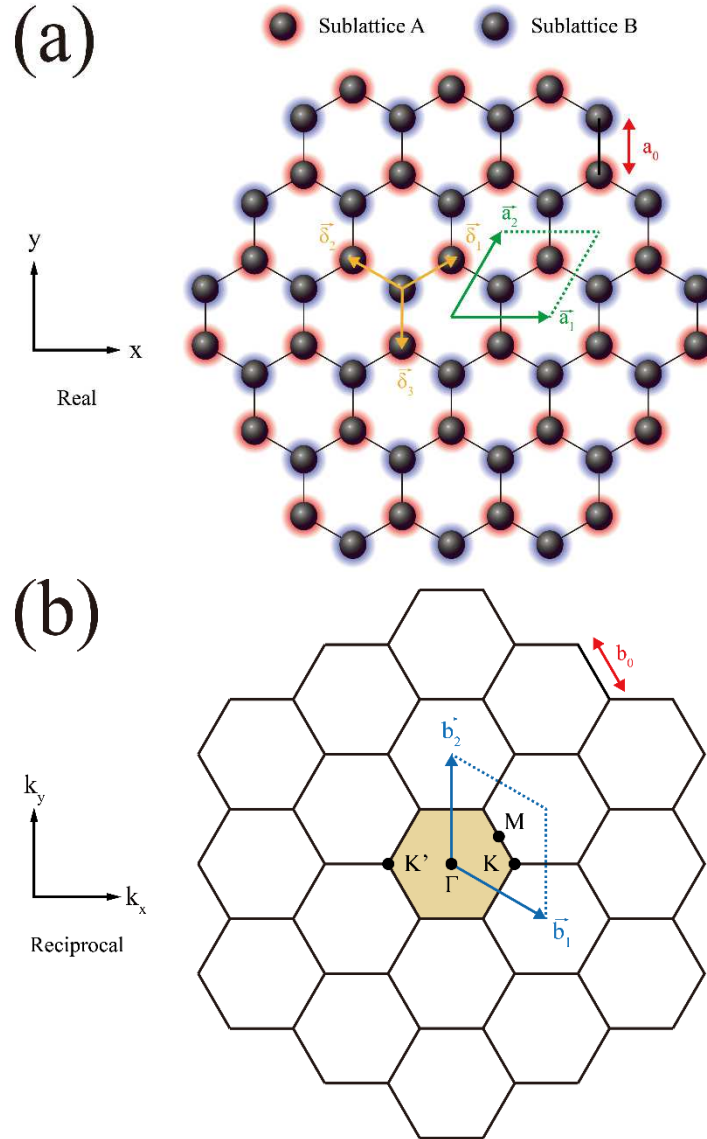


Figure 5. Graphene lattice structure in real (a) and reciprocal (b) spaces, where a_0 is the bond length, \vec{a}_1 and \vec{a}_2 is the primitive lattice vectors, $\vec{\delta}_1$, $\vec{\delta}_2$, and $\vec{\delta}_3$ are the connecting vectors to the each carbon atom, b_0 is the reciprocal lattice spacing, \vec{b}_1 and \vec{b}_2 is the reciprocal lattice vectors. The yellow hexagon signify the first Brillouin zone, where Γ represents the center, \mathbf{K}' and \mathbf{K} represent the inequivalent corner, and \mathbf{M} represents the middle of the zone edge.

As a consequence of triangular two equivalent sublattices in hexagonal honeycomb lattice (A and B two carbon atom basis Bravais lattice), the electronic states in the graphene are given by the Dirac equation (Equation 2) [186] with coupling between the momentum and the pseudo-spin [15-23], where $\hat{\boldsymbol{\sigma}}$ is the Pauli matrix consisting of $\sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$ and $\sigma_y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}$, $\boldsymbol{\psi}(\mathbf{r})$ is the wave-function, \mathbf{r} is the real space vector, and E is the total energy. This coupling of momentum and pseudo-spin can be depicted as shown in Figure 6. The corresponding wave-function (Equation 3) is bispinor associated with pseudo-spin degree of freedom, where s is the band index (1 for the conduction band and -1 for the valence band), \mathbf{k} is the Bloch wave-vector and $\theta = \tan^{-1}\left(\frac{k_y}{k_x}\right)$ is the tangential angle between the k_x and the k_y . The associated Hamiltonian equations are expressed as Equation 4 for the kinetic energy and Equation 5 for the total energy, where U is the potential energy.

$$-i\hbar v_F \hat{\boldsymbol{\sigma}} \cdot \nabla \boldsymbol{\psi}(\mathbf{r}) = E \boldsymbol{\psi}(\mathbf{r}) \quad (2)$$

$$\boldsymbol{\psi}(\mathbf{r}) = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 \\ s e^{i\theta} \end{pmatrix} e^{i\mathbf{k} \cdot \mathbf{r}} \quad (3)$$

$$\hat{H}_{kinetic} = \hbar v_F \mathbf{k} \cdot \hat{\boldsymbol{\sigma}} = \hbar v_F \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} \quad (4)$$

$$\hat{H}_{total} = \hbar v_F \mathbf{k} \cdot \hat{\boldsymbol{\sigma}} + U = \hbar v_F \begin{pmatrix} \frac{U}{\hbar v_F} & k_x - ik_y \\ k_x + ik_y & \frac{U}{\hbar v_F} \end{pmatrix} \quad (5)$$

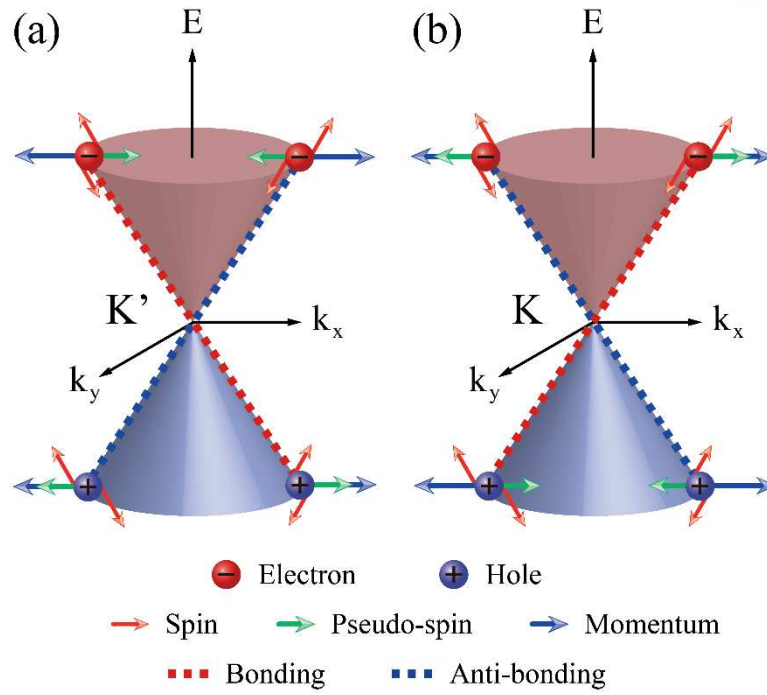


Figure 6. Gapless band structures of the graphene describing the linear energy dispersion and the helicity at K' (a) and K (b) points in the Brillouin zone.

1.4 Metal/Semiconductor Junction

A diode is one of the basic electrical component allowing charge current to move in primarily one direction (one-way electrical valve) and is the most representative electronic device application in the modern semiconductor industry. The two-terminal switching characteristic of diode shows an asymmetric conductance which is generally called as the rectifying behavior. In an ideal diode, it has infinity resistance (like a perfect insulator) in the reverse bias and zero resistance (like a perfect conductor) in the forward bias. In a common diode, when the applied bias voltage exceeds a certain threshold voltage, it reaches to a turn-on state and begins to conduct a charge current. A conventional diode was made of semiconductor-semiconductor junction formed with two different doping types (p-n junction). The most used diode in modern times is the Schottky contact (or Schottky barrier), which is formed by contact of metal and semiconductor.

1.4.1 Energy Barrier Formation

The working principle of Schottky contact strongly depends on its energy barrier height (Schottky barrier height) and interfacial environment [15], showing either the rectifying or Ohmic behaviors. The combination of metal electrode and semiconductor substrate creates the different energy barrier heights and interfacial environments. Therefore, the fundamental understanding of Schottky barrier formation has great importance regarding the carrier transport across the Schottky contact [187-190].

First of all, we will deal with the formation of Schottky barrier without considering the interfacial environment. Before making contact of metal and semiconductor, each Fermi-level (the energy level of an electron with the occupation probability of 50% at thermodynamic equilibrium, the most of electrons that actually contribute to conduction are distributed near this energy level) in metal and semiconductor is different. And then, after the junction is formed, both the Fermi-levels line up. If the interfacial environment is excluded, the primary things we have to consider are the work-function [191-194] (the energy level difference between the vacuum level and the Fermi level) and the electron affinity [194, 195] (the energy level difference between the vacuum level and the conduction band edge in semiconductor).

As shown in Figure 7 and Figure 8, the mobile charge carriers (electrons for n-type semiconductor and holes for p-type semiconductor) are enforced to diffuse from the semiconductor into the metal. The ionized impurities (donor for n-type semiconductor and acceptor for p-type semiconductor) are left to build up the depletion region on near the surface. Accordingly, the semiconductor Fermi-level moves (lowered for n-type semiconductor and raised for p-type semiconductor) relative to the metal one. The semiconductor band is bent in a parabolic shape to match the Fermi-level at the surface with that in the bulk. In thermal equilibrium at zero bias voltage, the bent semiconductor band in the depletion region is equivalent to the electric field preventing the charge carriers in semiconductor from diffusing into the metal. The curvature and direction of semiconductor band determines the type of contact (rectifying Schottky contact or non-rectifying Ohmic contact).

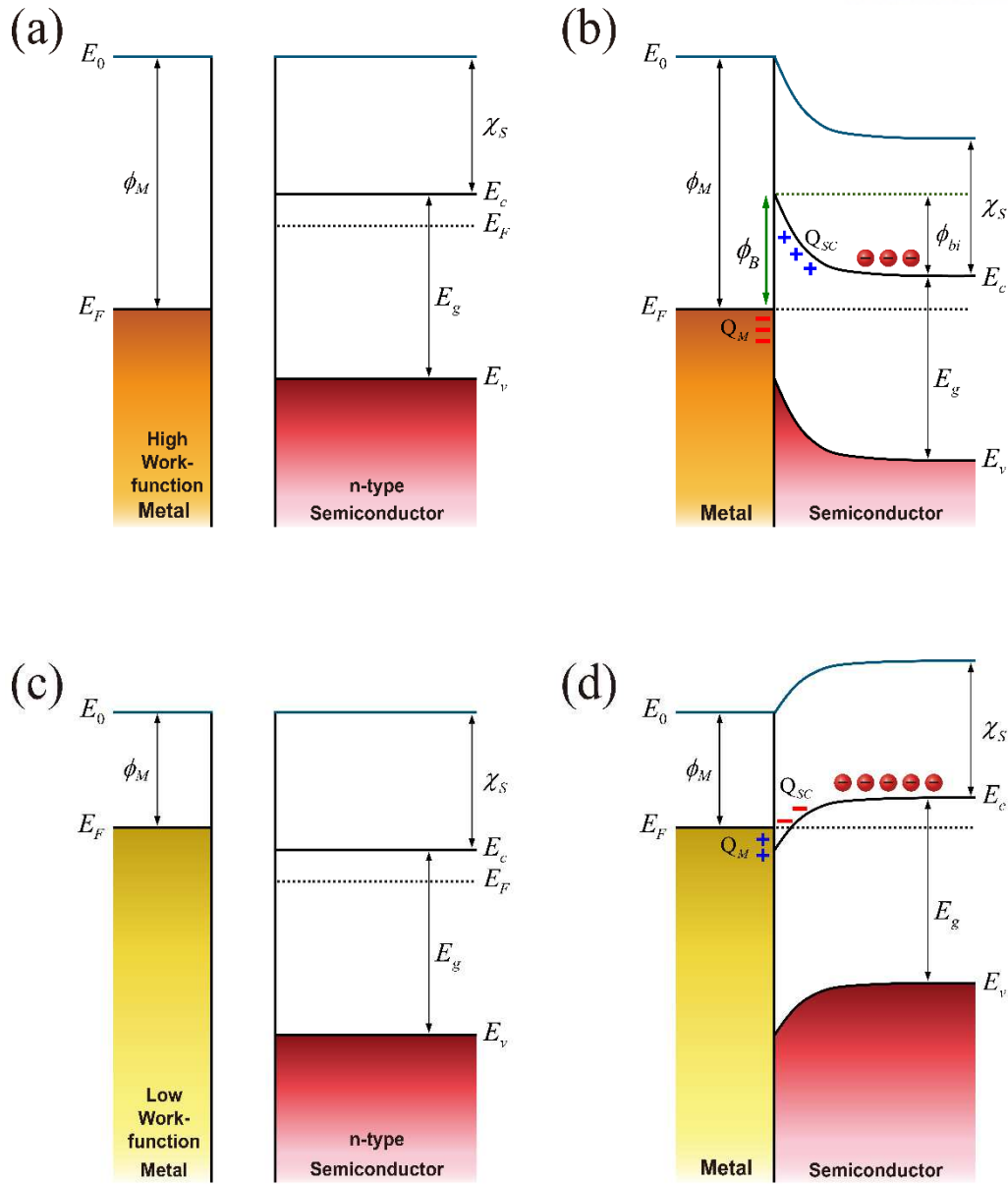


Figure 7. Energy band alignments of the junction formed with metal and n-type semiconductor showing how the Schottky (a,b) or Ohmic (c,d) contacts are determined by the Schottky barrier height and how it depends on the high and low metal work-functions, where ϕ_B is the Schottky barrier height, ϕ_M is the work-function of the metal, ϕ_{bi} is the built-in potential energy, E_F is the Fermi-level, E_0 is the vacuum level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, E_g is the band gap of the semiconductor, Q_M is the charge density on the metal surface, Q_{SC} is the space charge density in the depletion region of the semiconductor, and χ_S is the electron affinity of the semiconductor.

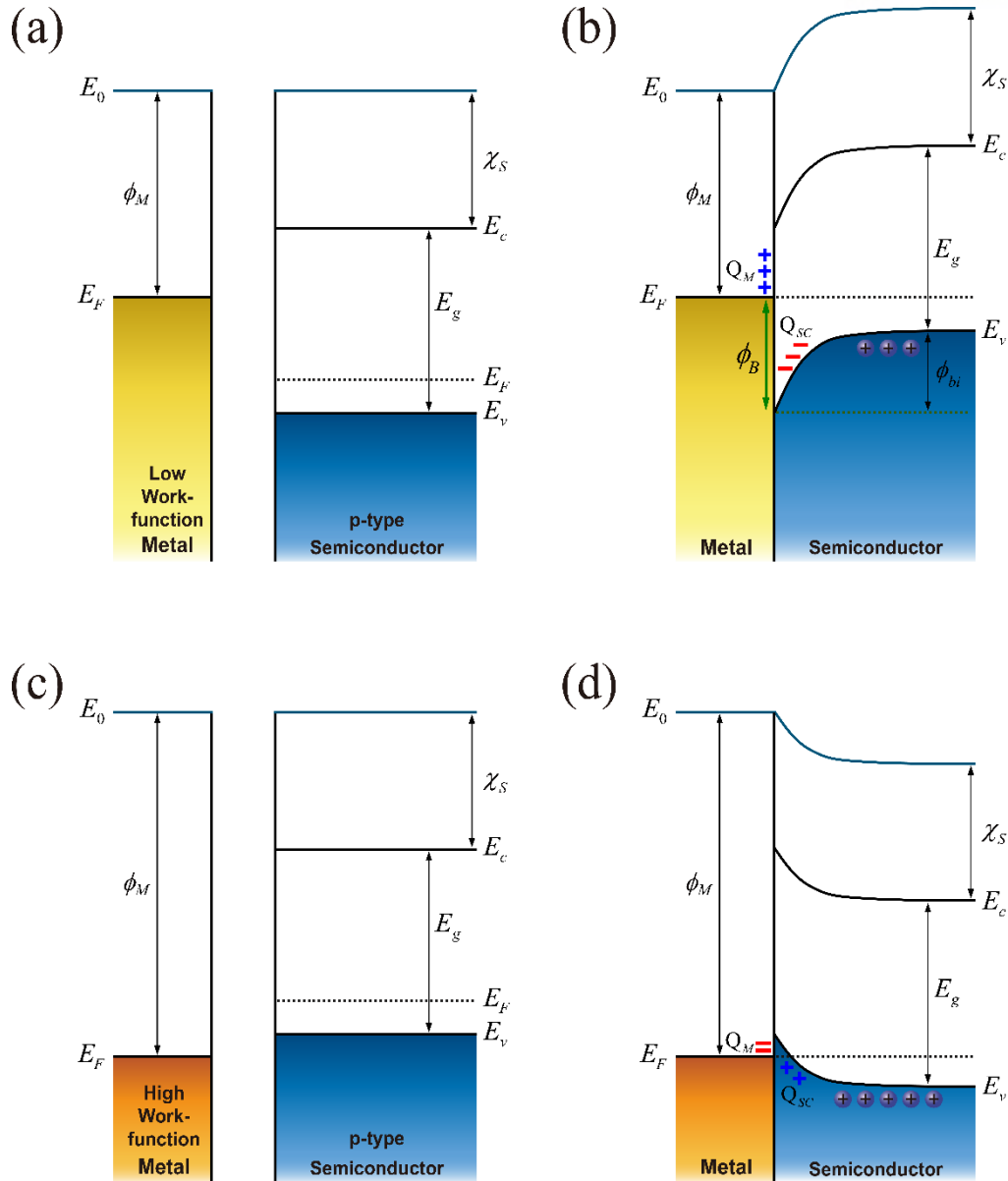


Figure 8. Energy band alignments of the junction formed with metal and p-type semiconductor showing how the Schottky (a,b) or Ohmic (c,d) contacts are determined by the Schottky barrier height and how it depends on the high and low metal work-functions, where ϕ_B is the Schottky barrier height, ϕ_M is the work-function of the metal, ϕ_{bi} is the built-in potential energy, E_F is the Fermi-level, E_0 is the vacuum level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, E_g is the band gap of the semiconductor, Q_M is the charge density on the metal surface, Q_{SC} is the space charge density in the depletion region of the semiconductor, and χ_S is the electron affinity of the semiconductor.

The screening charges Q_M will be induced on the metal surface, compensating the space charges Q_{SC} constructed by the ionized impurities in the depletion region (Equation 6). From the electrostatic analysis on the potential difference to balance the built-in potential with the Poisson's equation [15], the built-in potential energy ϕ_{bi} and the depletion region width W_D in the n-type semiconductor yield Equations 7 and 8 respectively, where ϕ_M is the work-function of the metal, ϕ_S is the work-function of the semiconductor, q is the electric charge constant, V_A is the applied bias voltage, ϕ_B is the Schottky barrier height, E_c is the conduction band edge in the semiconductor, E_F is the Fermi-level, k_B is the Boltzmann constant, T is the absolute temperature, $k_B T$ is the thermal energy (approximately 0.026 eV), N_C is the effective density of states in the conduction band of the semiconductor, N_D is the doping concentration of the n-type semiconductor, ϵ_0 is the permittivity of the vacuum, and κ_s is the dielectric constant of the semiconductor. And then, the expression of density of space charge Q_{SC} in the depletion region is written as Equation 9.

$$Q_M + Q_{SC} = 0 \quad (6)$$

$$\phi_{bi} = \phi_M - \phi_S - qV_A = \phi_B - (E_c - E_F) - qV_A = \phi_B - k_B T \ln\left(\frac{N_C}{N_D}\right) - qV_A \quad (7)$$

$$W_D = \sqrt{\frac{2\epsilon_0\kappa_s}{qN_D}\left(\frac{\phi_{bi}}{q} - \frac{k_B T}{q}\right)} = \sqrt{\frac{2\epsilon_0\kappa_s}{qN_D}\left[\frac{\phi_B}{q} - \frac{k_B T}{q} \ln\left(\frac{N_C}{N_D}\right) - V_A - \frac{k_B T}{q}\right]} \quad (8)$$

$$Q_{SC} = qN_D W_D = \sqrt{2qN_D\epsilon_0\kappa_s\left[\frac{\phi_B}{q} - \frac{k_B T}{q} \ln\left(\frac{N_C}{N_D}\right) - V_A - \frac{k_B T}{q}\right]} \quad (9)$$

If the high work-function metal is contacted to the n-type semiconductor (Figure 7a and Figure 7b), the Schottky contact is formed, electrons above the conduction band of semiconductor and electrons around the Fermi level of the metal cannot come and go easily blocked by the Schottky barrier, and the Schottky barrier height is equal to the energy difference between the metal work-function ϕ_M and the semiconductor electron affinity χ_S (Equation 10). If the low work-function metal is contacted to the n-type semiconductor (Figure 7c and Figure 7d), the Ohmic contact is formed, and electrons above the conduction band of semiconductor and electrons around the Fermi level of the metal can come and go easily. If the low work-function metal is contacted to the p-type semiconductor (Figure 8a and Figure 8b), the Schottky contact is formed, holes below the valence band of semiconductor and electrons around the Fermi level of the metal cannot come and go easily due to the Schottky barrier, and the Schottky barrier height is equal to the energy difference between the semiconductor ionization energy (the sum of the semiconductor band-gap E_g and the semiconductor electron affinity χ_S) and the metal work-function ϕ_M (Equation 11). If the high work-function metal is contacted to the p-type semiconductor (Figure 8c and Figure 8d), the Ohmic contact is formed, and holes below the valence band of semiconductor and electrons around the Fermi level of the metal can come and go easily.

$$\phi_b = \phi_M - \chi_S \quad (10)$$

$$\phi_b = E_g + \chi_S - \phi_M \quad (11)$$

1.4.2 Fermi-Level Pinning Effect

Equation 10 (n-type semiconductor) and Equation 11 (p-type semiconductor) represent the Schottky-Mott rule [196-197], where ϕ_B is the Schottky barrier height, ϕ_M is the work-function of metal, χ_S is the electron affinity of semiconductor, and E_g is the band gap of semiconductor. In this case, it is obvious that the Schottky barrier height ϕ_B directly depends on the metal work-function ϕ_M . However, the Schottky-Mott rule is valid only for the metal/semiconductor junction neglecting the interfacial environments.

From now on, we will take the interfacial environment into consideration, which is more realistic. In reality, the metal/semiconductor interface involves much more complex environmental elements. Starting with the semiconductor as a separate system, it will be discussed why are there differences in the electronic properties between the surface and the bulk of semiconductor, and how they affect the electronic states even inside the forbidden energy band on the semiconductor surface. After that, the environmental elements regarding interface states will be addressed when the semiconductor makes a contact with the metal. Finally, we will review the intrinsic and extrinsic factors that lower the dependence of the metal work-function ϕ_M on the Schottky barrier height ϕ_B .

If we think about two different atoms coming closer to each other, they give rise to the wave-function overlap and such overlapped atomic orbital is irrelevant to the eigenstate of the whole system. From this quantum mechanical point of view, it is predictable that atomic arrangement around the adjacent interface leads to a completely new physical system since the metal and semiconductor are also made up a bunch of atoms. This reasoning implies that the electronic structures and properties of real metal/semiconductor interface is entirely different from that of original semiconductor surface. Considering the energy band of materials stemming from its lattice periodicity, the origin of forbidden energy band of semiconductor is relying on the infinite periodicity of crystal. However, the crystal periodicity in the semiconductor bulk ensuring the infinite lattice is no longer applicable to that around the semiconductor surface. Hence, the energy band of semiconductor is perturbed by the additional electronic states localized in the surface region. In other words, the surface termination brings about the localized electronic states [198-202] inevitably within the band-gap, which resides on the semiconductor surface due to the neutral condition, which is followed by the importance of surface treatments like passivation [203, 204] and cleaving [205, 206]. The localized electronic states on the semiconductor surface are called as the surface states.

As shown in Figure 9, the continuum of surface states within the band gap reveals a specific energy distribution D_{it} in the range from the valence band maximum E_V to the conduction band minimum E_C depending on the atomic arrangements [15, 189, 190]. Here, for all electronic states in the entire surface region, the energy level satisfying the charge neutrality condition is called as the charge neutrality level. It is known that this charge neutrality level E_{CNL} positioning somewhere inside the forbidden energy band of bulk pins the Fermi-level E_F near the surface.

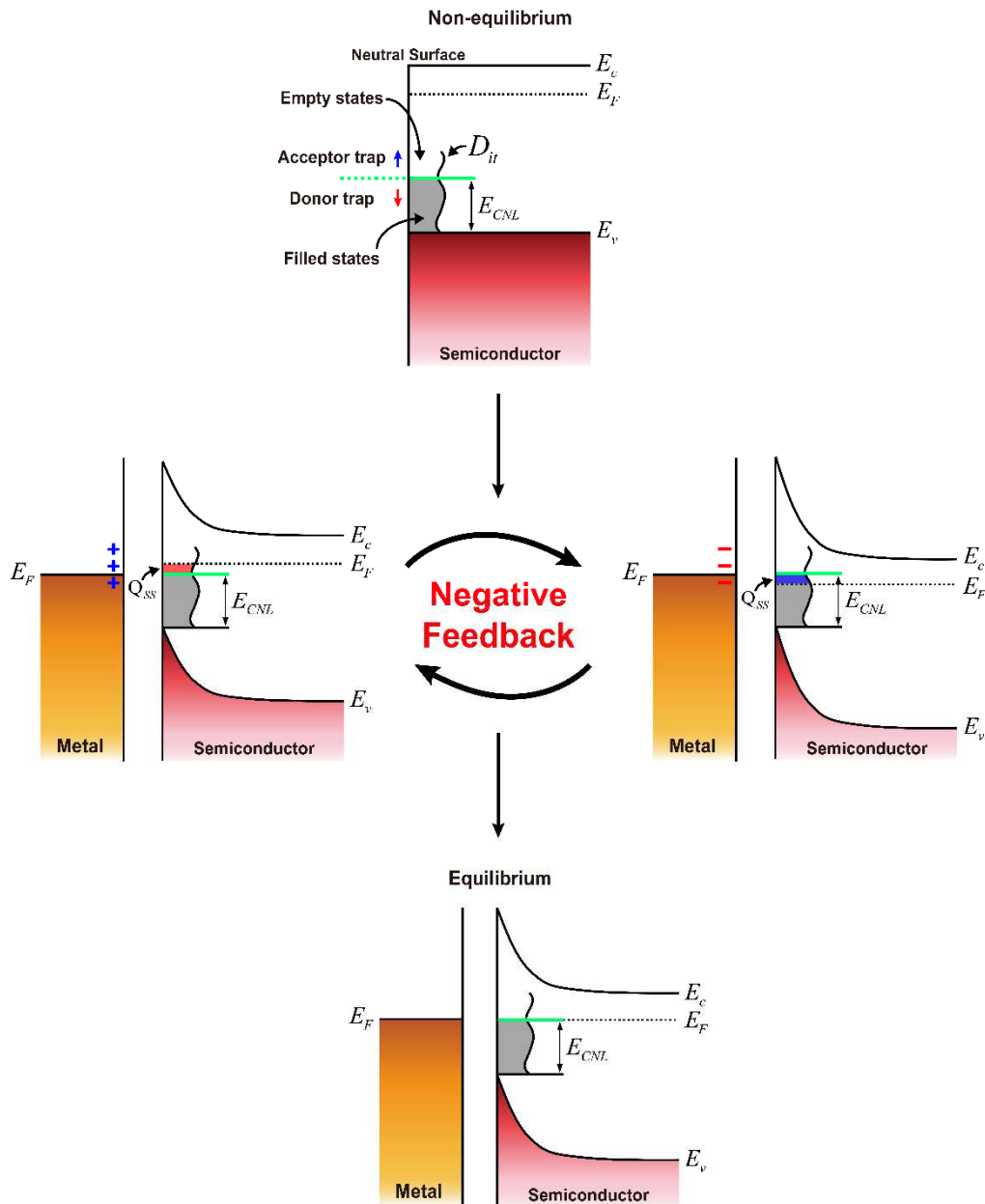


Figure 9. Energy band profiles of n-semiconductor showing the mechanism of Fermi-level pinning effect, where E_F is the Fermi-level, E_{CNL} is the charge neutrality level, E_0 is the vacuum level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, Q_{SS} is the trap charge density on the semiconductor surface, and D_{it} is the density of trap states per unit area per energy.

In equilibrium, the lower energy states are filled and the higher energy states are empty. Each trap state is normally in the charge neutralization. At some point, if the equilibrium is lost under conditions where mobile charge carriers can be exchanged such as in contact with metal, the polarity of these states changes. The surface states above the charge neutrality level E_{CNL} behave like the acceptor trap and the surface states below the charge neutrality level E_{CNL} act as the donor trap. In case of n-type semiconductor (Figure 9a), the acceptor-like trap states above the Fermi-level E_F are neutral because they are empty, and the donor-like trap states below the charge neutrality level E_{CNL} are also neutral because they are filled. However, the electrons can be supplied from the outside to the acceptor-like trap states below the Fermi-level E_F , and the accumulated charges Q_{SS} within the acceptor-like trap states should have negative polarity to balance the charge neutrality condition on the surface (Figure 9b). Accordingly, these negative charges Q_{SS} lower the Fermi-level E_F and bend the energy band around the semiconductor surface. As long as the Fermi-level E_F is higher than the charge neutrality level E_{CNL} , the negative trap charges Q_{SS} remain within the acceptor-like trap states. If the Fermi-level E_F goes down below the charge neutrality level E_{CNL} , the electrons escape from the semiconductor surface and they get out even from under the donor-like trap states where the electrons were originally filled. Consequently, the polarity of charges Q_{SS} on the semiconductor surface turns into positive (Figure 9c). Similar to the negative charges Q_{SS} , these positive charges Q_{SS} within the donor-like trap states raise the Fermi-level E_F the other way as long as the Fermi-level E_F is below the charge neutrality level E_{CNL} .

Due to the exchange of charge carrier, the charges Q_{SS} are continuously accumulated either within the acceptor-like or donor-like trap states until the Fermi-level E_F is aligned to the charge neutrality level E_{CNL} . Thus, the trap charges play a role as the indispensable source providing the negative feedback to pin the Fermi-level E_F to the charge neutrality level E_{CNL} (Figure 9d). The Fermi-level pinning effect refers to this compulsive align of the Fermi-level E_F to the charge neutrality level E_{CNL} on the semiconductor surface. Therefore, it is apparent that the high density of trap states D_{it} offers a much greater degree of the negative feedback, implying the strong Fermi-level pinning effect. Before the energy barrier formation in contact with metal, on the semiconductor surface, the pinning of the Fermi-level E_F to the charge neutrality level E_{CNL} is done. This Fermi-level pinning effect results in the collapse of the Schottky-Mott relationship [196-197]. More concretely, the Schottky barrier height ϕ_B become independent from the metal work-function ϕ_M since the Fermi-level E_F of metal must coincide with the Fermi-level E_F of semiconductor. If the trap states are rich enough to pin the Fermi-level E_F of metal, the dependence of the Schottky barrier height ϕ_B on the metal work-function ϕ_M disappears totally. Such condition is called as the Bardeen limit [207-209], where the Schottky barrier formation is disturbed by the trap states too much so that the Schottky barrier height ϕ_B is completely determined by the properties of semiconductor on the surface.

The Fermi-level pinning effect is not limited to the semiconductor surface. There will be a large discrepancy in the actual charge distribution between the free surface and the contact surface. Similar to the surface states [198-202], the electronic states originated in the trapping of charge carriers at the interface are called as the interface-trap states [210-213]. The interface-trap states are known to be afforded by the presence of the vacuum or the thin insulating layer with the thickness of a few angstroms [207-209] between the metal and the semiconductor.

If we accept the existence of this small gap δ at the contact interface [207-209], it is easily imaginable that an electric dipole layer [214-224] localized at the interface will form by a combination of the screening charge Q_M on the metal surface and the trap charge Q_{SS} on the semiconductor surface. If we assume that the distribution of trap states D_{it} is uniform (i.e., constant trap state D_{it} for each energy level), the relation between the density of trap charge Q_{SS} and the density of trap state D_{it} is written as Equation 12, where D_{it} is the trap states per unit area per energy on the semiconductor surface. Equation 13 shows the charge neutrality condition [15]. If we assume that the slight separation δ is fixed [207-209], the potential energy change Δ_{MS} across the metal/semiconductor interface can be derived by applying the Gauss' law (Equation 14) [214-224], where κ_i is the dielectric constant of the thin insulating layer ($\kappa_i = 1$ for the vacuum). Here, the sign of Δ_{MS} is set to be plus for the potential energy increase and minus for the potential energy decrease across the metal/semiconductor interface.

$$Q_{SS} = -qD_{it} (E_g - E_{CNL} - \phi_B) \quad (12)$$

$$Q_M + Q_{SS} + Q_{SC} = 0 \quad (13)$$

$$\Delta_{MS} = \frac{q\delta}{\epsilon_0\kappa_i} Q_M \quad (14)$$

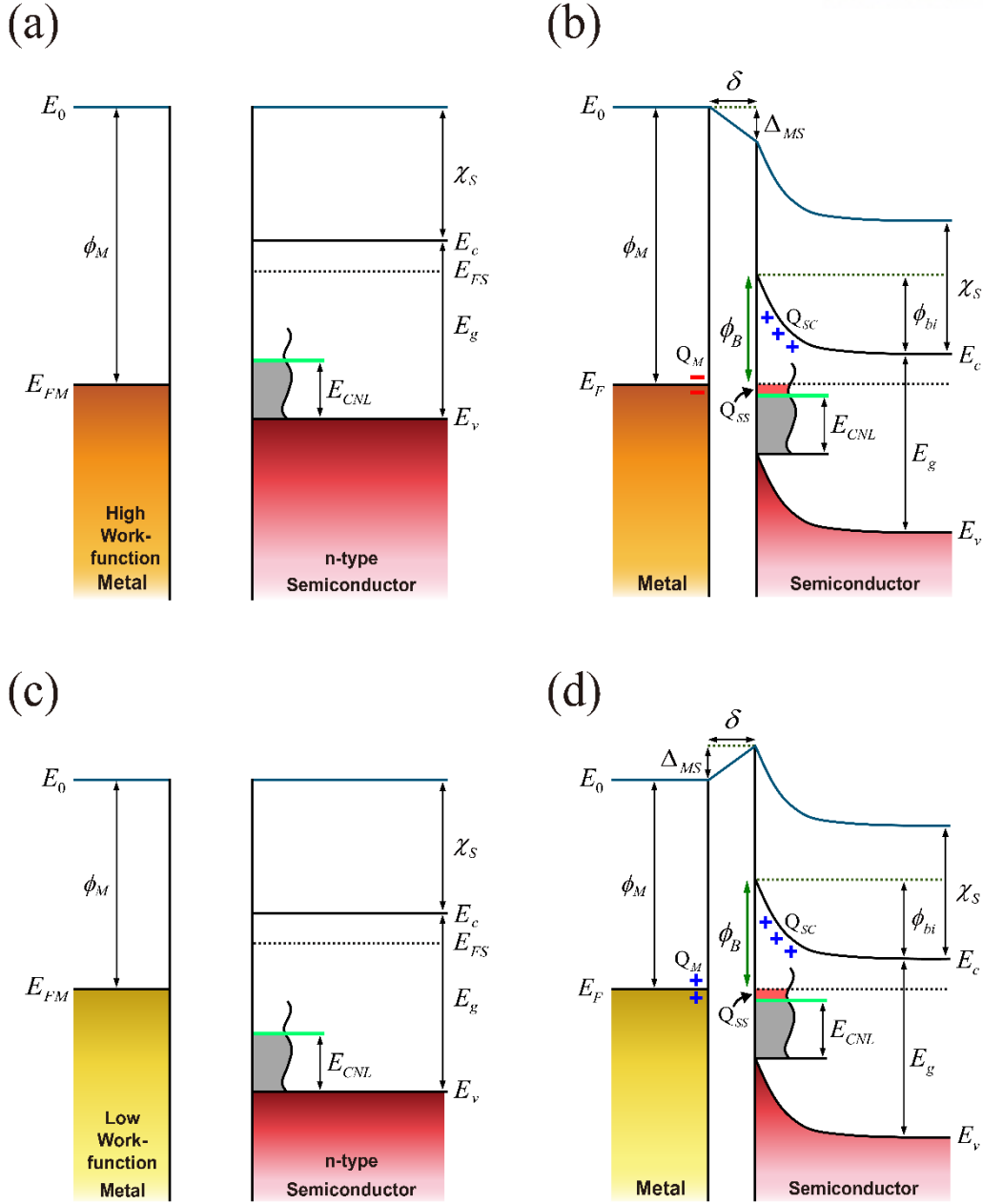


Figure 10. Energy band alignments of metal/n-semiconductor junction showing the fixed separation model [15, 189, 190, 207-224] in the Schottky barrier formation, where ϕ_B is the Schottky barrier height, ϕ_M is the work-function of the metal, ϕ_{bi} is the built-in potential energy, E_{FM} is the Fermi-level of the metal, E_{FS} is the Fermi-level of the semiconductor, E_F is the Fermi-level, E_0 is the vacuum level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, E_{CNL} is the charge neutrality level of the semiconductor, E_g is the band gap of the semiconductor, Δ_{MS} is the potential energy change across the metal/semiconductor

interface, Q_M is the charge density on the metal surface, Q_{SS} is the interface-trap charge density on the semiconductor surface, Q_{SC} is the space charge density, χ_S is the electron affinity of the semiconductor, and δ is the gap distance of the vacuum or the thin insulating layer between the metal and the semiconductor. The magnitude and polarity of screening charge Q_M induced on the metal surface varies depending on the metal work-function ϕ_M . (a,c) Before the Schottky barrier formation, the metal Fermi-level E_{FM} is below the semiconductor charge neutrality level E_{CNL} (a), while the metal Fermi-level E_{FM} is above the semiconductor charge neutrality level E_{CNL} (c). (b,d) After the Schottky barrier formation, a combination of the screening charge Q_M induced on the metal surface and the trap charge Q_{SS} on the semiconductor surface plays a role in the electric dipole layer [214-224] localized at the interface. (b) The negative charges Q_M are induced on the metal surface of the high work-function ϕ_M and the potential energy Δ_{MS} increases across the interface. (d) The positive charges Q_M are induced on the metal surface of the low work-function ϕ_M and the potential energy Δ_{MS} decreases across the interface. Here, the Fermi-level pinning effect is assumed to be so strong that the Schottky barrier height ϕ_B depends on the metal work-function very weakly.

Figure 10 shows the fixed separation model [15, 189, 190, 207-224], which is very useful to inspect the change of potential energy Δ_{MS} in the Schottky barrier formation. As seen in the diagram, Equation 14 can be converted into Equation 15. At zero bias ($V_A = 0$), we can combine Equations 9, 12, 13, 14 and 15 all together into Equation 16. In fact, the square root term originated from the space charge density Q_{SC} is found to have a relatively low value compared to the other terms so that it can be simply neglected. Now, we can reduce Equation 16 to more simplified one by introducing the pinning factor S (Equation 17). And then, the reduced form of Equation 16 is written as Equation 18. Experimental extraction of the pinning factor S can be deduced from Equation 19, which is the slope of the fitted Schottky barrier height ϕ_B as a function of the metal work-function ϕ_M .

$$\Delta_{MS} = \phi_B + \chi_S - \phi_M \quad (15)$$

$$\frac{\varepsilon_0 \kappa_i}{q \delta} (\phi_B + \chi_S - \phi_M) = q D_{it} (E_g - E_{CNL} - \phi_B) - \sqrt{2 q N_D \varepsilon_0 \kappa_s \left[\frac{\phi_B}{q} - \frac{k_B T}{q} \ln \left(\frac{N_C}{N_d} \right) - \frac{k_B T}{q} \right]} \quad (16)$$

$$S = \frac{\varepsilon_0 \kappa_i}{\varepsilon_0 \kappa_i + q^2 \delta D_{it}} = \left(1 + \frac{q^2 \delta D_{it}}{\varepsilon_0 \kappa_i} \right)^{-1} \quad (17)$$

$$\phi_B = S (\phi_M - \chi_S) + (1 - S) (E_g - E_{CNL}) = S \phi_M + I \quad (18)$$

$$S \equiv \frac{\partial \phi_B}{\partial \phi_M} \quad (19)$$

$$I \equiv - \frac{\partial \phi_B}{\partial \phi_M} (E_g - E_{CNL} + \chi_S) + (E_g - E_{CNL}) \quad (20)$$

The corresponding intercept I (Equation 20) provides an useful information about the charge neutrality level E_{CNL} (Equation 21). Focusing on the variables of the pinning factor S shown in Equation 17, the important physical parameters are as follows, the dielectric constant κ_i of the vacuum or the thin insulating layer, the gap distance δ of the vacuum or the thin insulating layer between the metal and the semiconductor, and density of interface-trap states D_{it} on the semiconductor surface. The most remarkable parameter is the interface-trap density D_{it} (Equation 22) [15, 189, 190, 210-224] since it has a great deal of impact on the pinning factor S quantitatively. Here, we revisit two limiting cases, the Schottky-Mott limit [196-197] and the Bardeen limit [207-209], regarding the interface-trap density D_{it} . Interestingly, in accordance with the density of interface-trap states D_{it} , the pinning factor S is in the range between zero (Equation 23, $E_{CNL} = E_g + \frac{S\chi_s + I}{S-1}$ the Schottky barrier height ϕ_B become entirely independent from the metal work-function ϕ_M [Equation 24], the Bardeen limit [207-209]) and one (Equation 25, the dependence of the Schottky barrier height ϕ_B on the metal work-function ϕ_M is absolute [Equation 26], the Schottky-Mott limit [196-197]).

$$E_{CNL} = E_g + \frac{S\chi_s + I}{S-1} \quad (21)$$

$$D_{it} = \frac{1-S}{S} \frac{\epsilon_0 \kappa_i}{\delta q^2} \quad (22)$$

$$S \rightarrow 0 \quad (D_{it} \rightarrow \infty) \quad (23)$$

$$\phi_B = E_g - E_{CNL} \quad (S=0) \quad (24)$$

$$S \rightarrow 1 \quad (D_{it} \rightarrow 0) \quad (25)$$

$$\phi_B = (\phi_M - \chi_s) \quad (S=1) \quad (26)$$

The electronic states on the surface or at the interface is known to arise from intrinsic or extrinsic factors [225-235]. Both the surface and interface of materials are in the quantum mechanically interacting system, where atomic orbitals inevitably overlap, electronic charge transfer is accompanied by positive and negative charge distribution, and physical or chemical reaction occurs.

The diamond type semiconductors containing covalent bonds with the neighboring identical atoms such as Si [236-244] and Ge [245-248] are found to possess the intrinsic surface states because the unpaired valence electrons in the missing atoms on the surface contribute to the electrically active trap states. In principle, on the intrinsic surface of such semiconductor, the number of dangling bonds and density of interface-trap states are almost saturated after native oxide growth and the charge neutrality is generally satisfied except for the degenerate case. Thus, for these intrinsic surface semiconductors, it is known that there are no additional requirements for having a substantial amount of interface-trap states. In more simple words, the intrinsic surface of this kind of semiconductor retains a significant amount trap states regardless of presence of the native oxide grown on the surface.

However, the density and distribution of trap states can be modulated when the surface gets distorted by various extrinsic factors such as defect [249-254], oxidation [255-262], chemisorption [263-271], trapping of holes [272-276], insertion of interlayer [277-283], and intermixing of materials [284-298]. Especially for Si, the remaining dangling bonds can be passivated by the hydrogen-related treatments, which lead to eliminate the charges trapped in the amorphous SiO₂ on the Si and reduce the originally saturated interface-trap states. This is why the hydrogen passivation is included in the RCA cleaning procedures [299-304]. In addition, the formation of silicide, which is implemented in the CMOS processes to make the Ohmic contact, significantly alter the trap states too [305-314].

On the other hand, the zinc-blende type III-V compound semiconductors [315-325] consisting of the covalent bonds with the neighboring alternative atoms such as GaAs [326-339] are commonly known to have the extrinsic surface states. In case of the III-V compound semiconductors, the non-polar reconstructed surface with ultrathin or no native oxide layers induces only a very low density of trap states within the band-gap, while the distorted surface generates the electronic states. It is very difficult that there is no insulating material making up the interfacial layer but only vacuum. The material intermixing including the native oxide grown on the semiconductor surface or the inter-diffusion of metal and semiconductor atoms driven by localized reaction during metal deposition results in a high density of trap states for the III-V compound semiconductors. Therefore, the extrinsic factors [249-298], which influences the structural, electrical, and chemical properties on the surface, are the origin of a high density of trap states on the surface of III-V compound semiconductor.

The Fermi-level pinning effect is manifested in various ways. Here, it is worthwhile to look in the misconception regarding the Fermi-level pinning effect. The common misunderstanding is that it is a phenomenon in which the Fermi-level E_F of metal is fixed to that of semiconductor or the Schottky barrier height ϕ_B appears to have a weak dependence on the metal work-function ϕ_M . They are a kind of half-baked statement because those are the result of Fermi-level pinning effect not the Fermi-level pinning effect itself. Such phenomena resulting from the Fermi-level pinning effect can be achieved through any other processes too. Nevertheless, the above phenomena are widely termed as the Fermi-level pinning effect. In particular, the experimental observation relies on the extraction of the pinning factor S and the charge neutrality level E_{CNL} .

The emphasis here is that the align of Fermi-level E_F to the charge neutrality level E_{CNL} on the semiconductor surface due to the high density of trap states D_{it} is said to be the original definition of the Fermi-level pinning effect. Moreover, its key point is related to the strong correlation with electronic states D_{it} distributed on the surface or trapped at the interface, which are induced by physical or chemical mechanisms occurring at the gap between metal and semiconductor [15, 189, 190, 198-202, 207-224]. As a consequence, the involved physical and chemical mechanisms are of great importance to the origin of the Fermi-level pinning [225-235, 249-298].

In addition to the surface states [198-202], gap states [207-209], interface-trap states [210-213], interface dipole formation [214-224], and intrinsic/extrinsic factors [225-235, 249-298] mentioned so far, there are quite a number of theories explaining the origin of the Fermi-level pinning effect in slightly different ways. One of the other widely known theory is the metal-induced gap states claiming that the electronic states on the semiconductor surface stem from the penetration of the metal wave-function tail into the semiconductor [189, 190, 207-209]. The presence of small gap δ and the charge neutrality level E_{CNL} is still applicable to the theory of metal-induced gap states. Likewise, regarding the origin of the Fermi-level pinning effect, the related theories seem to conflict, but somehow complement each other. Therefore, at this stage, it would be reasonable to state that it is difficult to confirm the origin of the Fermi-level pinning effect arbitrarily or conclusively. However, for one reason or another, the formation of electric dipole layer at the interface plays an essential part in the electronic states on the semiconductor surface, the change of electrostatic potential across the interface, and the Fermi-level pinning effect.

Finally, the Fermi-level pinning effect is occasionally recognized as parasite resistance source. By changing the point of view, it is possible to adjust the principle of device operation arbitrarily, if we can modulate or take advantage of the Fermi-level pinning effect.

1.4.3 Image Force Lowering

The Schottky barrier height ϕ_B seen by the charge carrier coming close to or moving away from the metal/semiconductor interface is known to be effectively reduced by $\Delta\phi$ due to the modified potential energy associated with the image charge reflected in the other side of the interface [15, 340-343]. Compared to the approaching charge carrier, the induced image charge has different polarity but same magnitude. Each distance measured from the interface will be the same too. If the electrons on the semiconductor side approach the interface, the positive charges are positioned on the metal side, the image force is applied to the electrons, and this causes the electrons to be attracted toward the metal. The image force can be converted into the potential energy. This potential energy is called as the image force lowering energy $\Delta\phi$ written as Equation 27, where ϵ_0 is the permittivity of the vacuum, and κ_s is the dielectric constant of the semiconductor, E_{\max} is the maximum electric field (Equation 28) at the semiconductor surface, q is the electric charge constant, N_D is the doping concentration of the n-type semiconductor, ψ is the potential energy (Equation 29) at the semiconductor surface, ϕ_{bi} is the built-in potential energy, ϕ_{B0} is the Schottky barrier height without the image force lowering energy, k_B is the Boltzmann constant, T is the absolute temperature, $k_B T$ is the thermal energy (approximately 0.026 eV), N_C is the effective density of states in the conduction band of the semiconductor, and V_A is the applied bias voltage. The Schottky barrier height ϕ_B with the image force lowering energy $\Delta\phi$ is given by Equation 30. In addition, Equation 31 is referred to as the location x_{\max} where the potential energy is maximized. Under different bias conditions, the image force lowering incorporated energy band diagrams are shown in Figure 11. One thing to note here is that the image charge is noticeable when the charge carrier passes through the interface. The motion of charge carrier caused by an external electric field is not sufficient to induce the image charge. In other words, the image force lowering effect will be observed only in the measurement techniques using the charge carrier transport crossing the interface. Thus, the barrier shift due to the image force lowering should be considered in the current-voltage measurement or internal photoemission spectroscopy not in the capacitance-voltage measurement.

$$\Delta\phi = \sqrt{\frac{q^3 E_{\max}}{4\pi\epsilon_0\kappa_i}} = \left(\frac{q^6 N_D \psi}{8\pi^2 \epsilon_0^3 \kappa_i^3}\right)^{\frac{1}{4}} \quad (27)$$

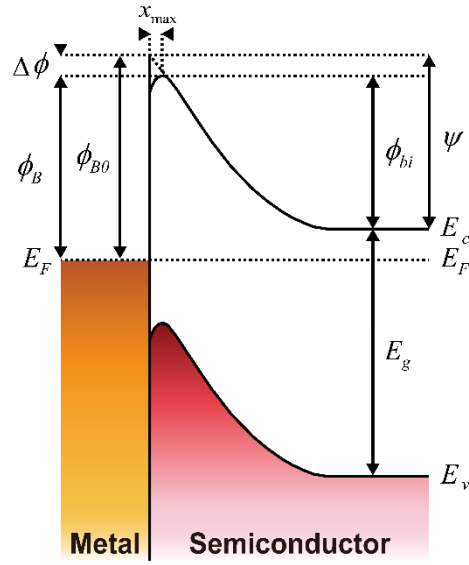
$$E_{\max} = \sqrt{\frac{2N_D\psi}{\epsilon_0\kappa_i}} \quad (28)$$

$$\psi = \phi_{bi} + \Delta\phi = \phi_{B0} - k_B T \ln\left(\frac{N_C}{N_D}\right) - qV_A \quad (29)$$

$$\phi_B = \phi_{B0} - \Delta\phi \quad (30)$$

$$x_{\max} = \sqrt{\frac{q}{16\pi\epsilon_0\kappa_i|E_{\max}|}} = \left(\frac{q^2}{512\pi^2\epsilon_0\kappa_i N_D \psi}\right)^{\frac{1}{4}} \quad (31)$$

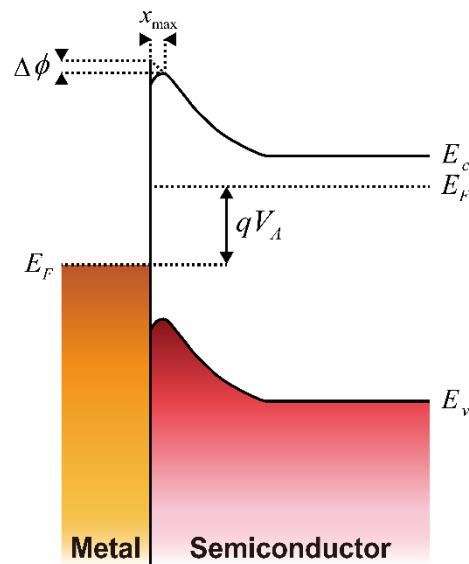
(a)



Zero Bias

$$V_A = 0$$

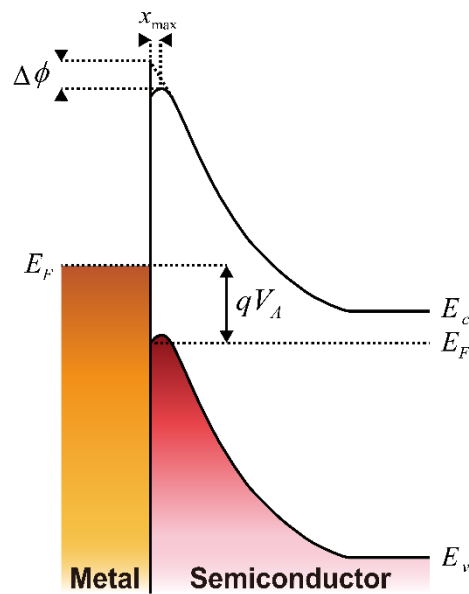
(b)



Forward Bias

$$V_A > 0$$

(c)



Reverse Bias

$$V_A < 0$$

Figure 11. Energy band alignments of metal/n-semiconductor junction under different bias conditions showing the image force lowering, where ϕ_B is the Schottky barrier height with the image force lowering energy, ϕ_{B0} is the Schottky barrier height without the image force lowering energy, $\Delta\phi$ is the image force lowering energy. ϕ_{bi} is the built-in potential energy, ψ is the potential energy at the semiconductor surface, E_F is the Fermi-level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, E_g is the band gap of the semiconductor, x_{max} is the location where the potential energy is maximized, q is the electric charge constant, and V_A is the applied bias voltage.

1.4.4 Transport Mechanism

In solid-state materials, according to the density of states and the Fermi-Dirac statistics, the electronic states available for the charge carrier transport are distributed near the Fermi-level. Because charge carrier can transmit into only the partially filled energy states, the charge carriers in those electronic states play a critical role in the electrical conduction. When two different materials make an intimate contact, the exchange of mobile charge carriers in the partially filled electronic states around the Fermi-level of each material occur. If a bias voltage is applied on the contact, it gives rise to energy difference in the Fermi-level of each material. The Fermi-level difference brings about the delocalized electronic states and the non-equilibrium charge carrier. The charge carrier transport crossing the junction interface induces the current flow through entire circuit which includes the junction itself. Thus, the best way to evaluate the performance of electronic devices is to measure the bias-dependent electric current due to the carrier transport, since the operation characteristics is determined by carrier transport processes across the interface [15, 340-343]. This is why the various transport measurements are performed to examine their electrical properties and extract the related parameters. In case of metal/semiconductor junction, the turn-on current is mainly attributed to the majority carrier transport.

Here, it will be reviewed on the charge carrier transport resulting from thermionic-emission [344-348], tunneling [349-353], and recombination [354-358] occurring at the interface of the Schottky barrier diode. The most commonly used in analysis of the current-voltage characteristic measured on the Schottky contact is the thermionic-emission, which is followed by tunneling and recombination. As shown in Figure 12, the basic carrier transport processes depend on the bias condition in the range where contact resistance and breakdown mechanism are safely neglected. In forward bias (Figure 12a), the reduced built-in potential energy leads to the exponentially increasing current flow with increasing applied bias voltage. In reverse bias (Figure 12b), the increased built-in potential energy results in the saturated current flow before the breakdown.

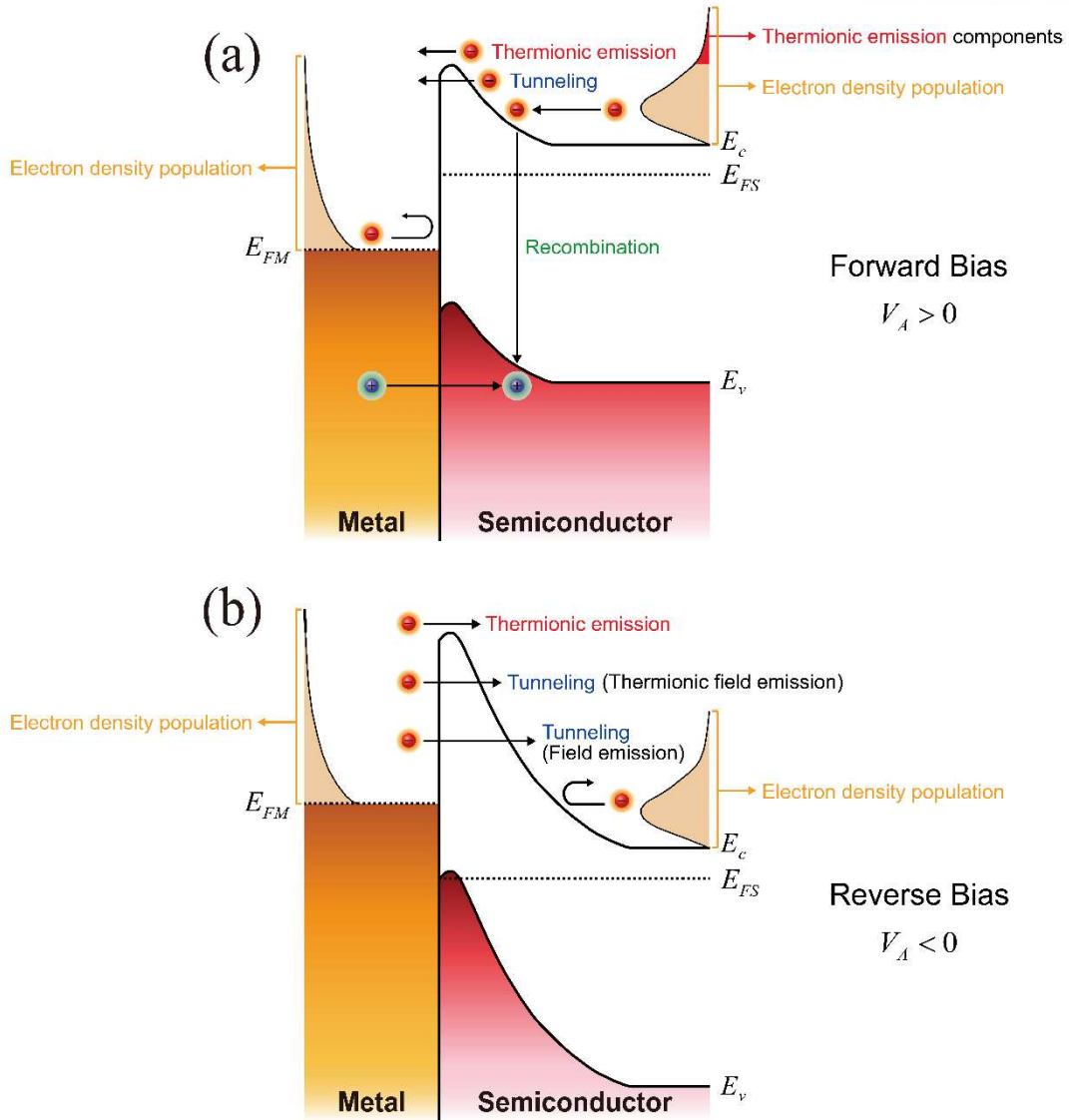


Figure 12. Transport processes in forward-biased (a) and reverse-biased (b) metal/n-semiconductor junction, where E_{FM} is the metal Fermi-level, E_{FS} is the semiconductor Fermi-level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, and V_A is the applied bias voltage.

The thermionic emission is the majority carrier emission over the energy barrier height [344-348]. In case of the metal/n-semiconductor junction, most electrons emit from the semiconductor to the metal under forward bias (Figure 12a) and from the metal to the semiconductor under reverse bias (Figure 12b). The thermionic-emission theory unified with diffusion theory is very practical to extract the Schottky diode parameters and explain the experimental results quantitatively. The expression of current density-voltage characteristic with the thermionic-emission-diffusion theory is described by Equations 32-34, where J_{TE} is the forward-biased current density of the thermionic emission components, J_{TE}^{SM} is the forward-biased current density of the thermionic emission components, J_{TE}^{MS} is the reverse-biased current density of the thermionic emission components, J_{TE} is the total current density of the thermionic emission components, A^{**} is the Richardson constant, T is the absolute temperature, ϕ_B is the Schottky barrier height, k_B is the Boltzmann constant, $k_B T$ is the thermal energy (approximately 0.026 eV), q is the electric charge constant, and V_A is the applied bias voltage.

$$J_{TE}^{SM} = A^{**} T^2 \exp\left(-\frac{\phi_B}{k_B T}\right) \exp\left(\frac{q V_A}{k_B T}\right) \quad (32)$$

$$J_{TE}^{MS} = -A^{**} T^2 \exp\left(-\frac{\phi_B}{k_B T}\right) \quad (33)$$

$$J_{TE} = A^{**} T^2 \exp\left(-\frac{\phi_B}{k_B T}\right) \left[\exp\left(\frac{q V_A}{k_B T}\right) - 1 \right] \quad (34)$$

As shown in Figure 12, the tunneling through the Schottky barrier consists of not only the direct tunneling but also the thermally assisted field emission (thermionic field emission) and the purely field emission (field emission) [349-353]. The thermionic field emission is tunneling of charge carriers between the Schottky barrier height and the energy levels much above the Fermi-level. On the other hand, the field emission is tunneling of charge carriers at energy levels slightly above the metal Fermi level. Since the quantum mechanical tunneling strongly depends on width, height, and shape of the energy barrier, the direct tunneling is predominant in the Schottky contact formed with the heavily doped semiconductors, while the thermionic field emission and the field emission are manifested in the Schottky contact formed with the moderately-doped semiconductors. For the same reason, the tunneling becomes significant at low temperature. Besides, the tunneling through the sharp potential barrier due to the high electric field under reverse-biased contributes to the leakage current. Similarly, the potential barrier near the contact edge is known to be narrow than that near the contact center, which implies that it is more preferable for the charge carriers to tunnel through the energy barrier around the contact edge. These are why the tunneling accounts for a large portion of leakage current in the Schottky contact. The current density of the tunneling components is obtained by the integral of quantum transmission coefficient multiplied by the amount of occupied energy states in the material where the charge carriers emit and the amount of unoccupied states in the material where the charge carriers are injected. They are given by J_{TU}^{SM} (Equation 35) for the forward bias and J_{TU}^{MS} (Equation 36) for the reverse bias, where A^{**} is the Richardson constant, T is the absolute temperature, k_B is the Boltzmann constant, E_{FM} is the metal Fermi-level, ϕ_B is the Schottky barrier height, E_c is the conduction band edge in the semiconductor, F_S is the Fermi-Dirac distribution function for the semiconductor, F_M is the Fermi-Dirac distribution function for the metal, and $T(E)$ is the tunneling probability at certain energy E .

$$J_{TU}^{SM} = \frac{A^{**}T}{k_B} \int_{E_c}^{E_{FM}+\phi_B} F_S (1 - F_M) T(E) dE \quad (35)$$

$$J_{TU}^{MS} = \frac{A^{**}T}{k_B} \int_{E_{FM}}^{E_{FM}+\phi_B} F_M (1 - F_S) T(E) dE \quad (36)$$

The recombination occurring mainly in the depletion region is due to the minority carrier injection from the metal into the semiconductor [354-358]. For the n-type semiconductor Schottky contact, the holes are injected from the metal into the depletion region of the semiconductor under forward bias (Figure 12a). The forward-biased recombination current density in the Schottky contact can be also expressed by that in the p-n junction (Equation 37), where J_{RE}^{SM} is the forward-biased current density of the recombination components, q is the electric charge constant, W_D is the depletion region width, σ is the capture cross sections for electrons and holes, v_{th} is the thermal velocity, N_T is the trap density in semiconductor, n_i is the intrinsic carrier concentration in semiconductor, V_A is the applied bias voltage, k_B is the Boltzmann constant, T is the absolute temperature, $k_B T$ is the thermal energy (approximately 0.026 eV), and τ is the lifetime in the depletion region. It is necessary to point out here that Equation 37 is somewhat overestimated term because it is based on the assumption of maximum recombination rate in most part of the depletion region. In addition, under reverse bias, unless the photo-carrier is generated by the light illumination, the generation rarely occur in the Schottky contact, contrary to the p-n junction.

$$J_{RE}^{SM} = \frac{1}{2} q W_D \sigma v_{th} N_T n_i \exp\left(\frac{qV_A}{2k_B T}\right) = \frac{1}{2} q W_D \frac{n_i}{\tau} \exp\left(\frac{qV_A}{2k_B T}\right) \quad (37)$$

In real Schottky contact, the total current consists of the other non-ideal current sources as well as the transport processes (thermionic emission, tunneling, and recombination) presented so far. The experimentally measured current density-voltage curve is conveniently expressed in the following form (Equation 38) based on the thermionic emission model combined with the ideality factor η [15, 340-358], A^{**} is the Richardson constant, T is the absolute temperature, ϕ_B is the Schottky barrier height, q is the electric charge constant, and V_A is the applied bias voltage, k_B is the Boltzmann constant, and $k_B T$ is the thermal energy (approximately 0.026 eV). Here, $A^{**} T^2 \exp\left(-\frac{\phi_B}{k_B T}\right)$ term is defined as the saturation current density $J_0 = A^{**} T^2 \exp\left(-\frac{\phi_B}{k_B T}\right)$. The ideality factor η increases with the tunneling and recombination components increasing. Likewise, if the non-ideal current sources are introduced, the ideality factor n also increase. The linear extrapolation of current density-voltage curve in log scale gives the Schottky diode parameters. From the slope of the fitted line, represented by $\frac{q}{\eta k_B T}$, we can extract the ideality factor η (Equation 39). In particular, the Schottky barrier height ϕ_B can be extracted from the intercept of the fitted line, which is linked to the saturation current density J_0 (Equation 40). One thing to note is that the barrier shift due to the image force lowering should be included in Equation 40, as explained in Chapter 1.4.3. In other words, the Schottky barrier height ϕ_{B0} at zero bias will be $\phi_B + \Delta\phi$, where $\Delta\phi$ is the image force lowering energy.

$$J = A^{**} T^2 \exp\left(-\frac{\phi_B}{k_B T}\right) \left[\exp\left(\frac{q V_A}{\eta k_B T}\right) - 1 \right] = J_0 \left[\exp\left(\frac{q V_A}{\eta k_B T}\right) - 1 \right] \quad (38)$$

$$\eta = \frac{q}{k_B T} \frac{d V_A}{d (\ln J)} \quad (39)$$

$$\phi_B = \frac{k_B T}{q} \ln \left(\frac{A^{**} T^2}{J_0} \right) \quad (40)$$

1.4.5 Parallel Conduction Model

The interpretation of current density-voltage curve using the thermionic emission model combined with the ideality factor is working on the assumption that the Schottky contact has perfectly uniform planar interface the Schottky barrier is spatially homogeneous. In practice, atomic arrangement at the interface is quite inhomogeneous since it is very difficult to fabricate an abrupt metal/semiconductor contact. The non-uniform interface structure varying from region to region implies that the Schottky contact contains the local Schottky barrier heights much lower than that on the surrounding. Such region is called as the low barrier patches [359-377]. One of the non-ideal current sources is actually attributed to this low barrier patches acting as leakage paths for the junction current. As shown in Figure 13, the current-voltage characteristic of the inhomogeneous Schottky contact containing the low barrier patch is extremely sensitive to the areal percentage of the low barrier patches. As a consequence, the effective Schottky barrier height will be lower than that on the surrounding area.

The variation in the effective Schottky barrier height due to the presence of low barrier patches can be investigated by introducing the parallel conduction model [187-190, 378, 379]. In the model, each Schottky barrier height in the inhomogeneous Schottky contact is assumed to be discrete and considered as the electrically independent current path. And then, the total junction current is simply expressed by the sum of the currents flowing through all individual patches (Equation 41), where I is the total current, A^{**} is the Richardson constant, T is the absolute temperature, q is the electric charge constant, and V_A is the applied bias voltage, η is the ideality factor, k_B is the Boltzmann constant, $k_B T$ is the thermal energy (approximately 0.026 eV), n is the index of each individual patch, ϕ_{Bn} is the Schottky barrier height, and A_n is the junction area of each individual patch. In most cases, each individual low barrier patch is surrounded by the prevailing high barrier region. If we assume here that the inhomogeneous Schottky contact possesses the Schottky barrier height of ϕ_{Low} for the low barrier patch and that of ϕ_{High} for the high barrier region respectively, the areal percentage α of all individual low barrier patches to total junction area A can be estimated from Equation 42. The effective Schottky barrier ϕ_{PC} based on the parallel conduction model is obtained as Equation 43. The portion of low barrier patches can be estimated by matching the calculated effective Schottky barrier height ϕ_{PC} with the measured Schottky barrier height ϕ_B . In general, the total junction current I is governed by the current flowing through the low barrier patches with a very small area portion, implying that the effective Schottky barrier height ϕ_{PC} changes significantly depending on the areal percentage α of the low barrier patches.

$$I = A^{**} T^2 \left[\exp\left(\frac{qV_A}{\eta k_B T}\right) - 1 \right] \sum_n \exp\left(-\frac{\phi_{Bn}}{k_B T}\right) A_n \quad (41)$$

$$I = A^{**} T^2 \left[\exp\left(\frac{qV_A}{\eta k_B T}\right) - 1 \right] \left\{ \alpha A \exp\left(-\frac{\phi_{Low}}{k_B T}\right) + [1 - \alpha] A \exp\left(-\frac{\phi_{High}}{k_B T}\right) \right\} \quad (42)$$

$$\phi_{PC} = -k_B T \ln \left\{ \alpha A \exp\left(-\frac{\phi_{Low}}{k_B T}\right) + [1 - \alpha] A \exp\left(-\frac{\phi_{High}}{k_B T}\right) \right\} \quad (43)$$

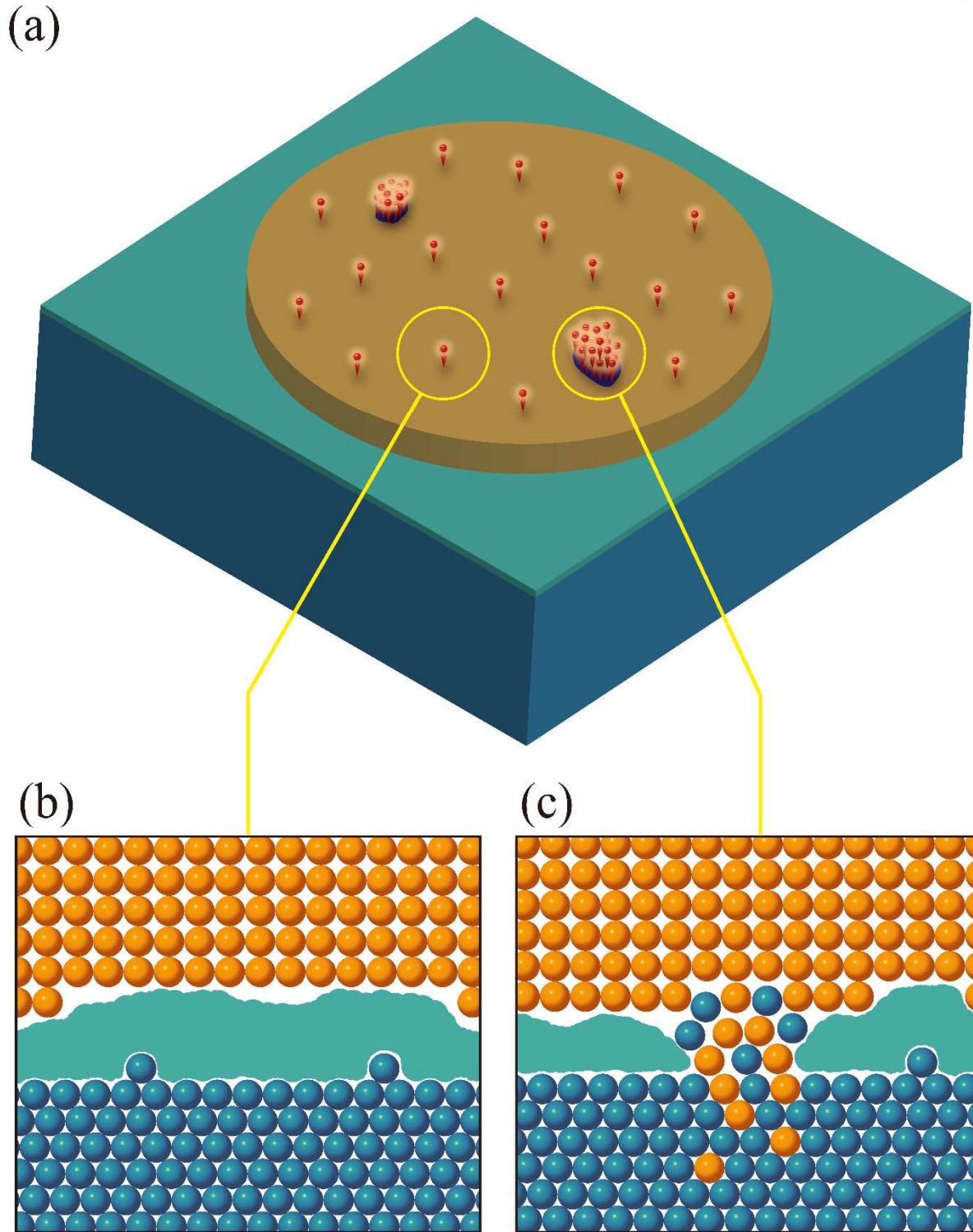


Figure 13. (a) Schematic of the Schottky contact showing that most of the junction current flows through the low-barrier patches in the current-voltage measurement. (b,c) Cross-sectional schematic view of the atomic arrangement at the interfaces of the high barrier region with normal native oxide layer (b) and the low barrier patches induced by material intermixing (c).

1.5 Internal Photoemission

The internal photoemission spectroscopy (IPE) [32-34, 380-387] is an effective technique for determining the interfacial energy barrier by collecting the optically induced mobile charge carrier. When the light is intensely illuminated on the surface of junction formed by two or more different materials such as metal/semiconductor, metal/insulator/semiconductor, and metal/insulator/metal, the mobile charge carriers absorbing the sufficient photon energy reveals the ballistic motion which is not deflected in their traveling path. In other words, the photo-excited hot carriers can transmit from one material into another material in the absence of scattering. Since total energy and transverse momentum component of the charge carriers crossing the interface are generally conserved, the lateral momentum is crucial for overcoming the energy barrier. More concretely, the charge carriers having a component of momentum perpendicular to the surface can surmount over the interfacial energy barrier.

1.5.1 Basic Principle

Figure 14 shows the IPE process consists of optical excitation, hot carrier transport to the surface, overcoming potential barrier, and collection of substrate current. This multi-step model provided by Powell [382] is most widely used as phenomenological description for the IPE mechanism. For the n-type semiconductor Schottky contact, after photoexcitation near the top metal layer, the excited hot carriers will travel through the beneath metal layer with maintaining their trajectory and reach the junction interface without losing their energy. The ballistic carriers arriving at the interface get over the Schottky barrier depending on the magnitude of lateral momentum. The surmounted carriers contribute on the substrate current. The IPE signal comes from this photocurrent measured on the substrate. One of the most interesting aspects of the IPE signal is that it is acquired by the collective contribution of photo-excited carriers in all regions of the junction (Figure 15). This makes the biggest difference with the current-voltage measurement, where most charge carriers flow into the low barrier patches (Chapter 1.4.5). Owing to this, the IPE measurement is not biased to the influence from the small areal fraction of low barrier patches so that it is capable of determining the energy barrier height at the junction interface of prevailing area.

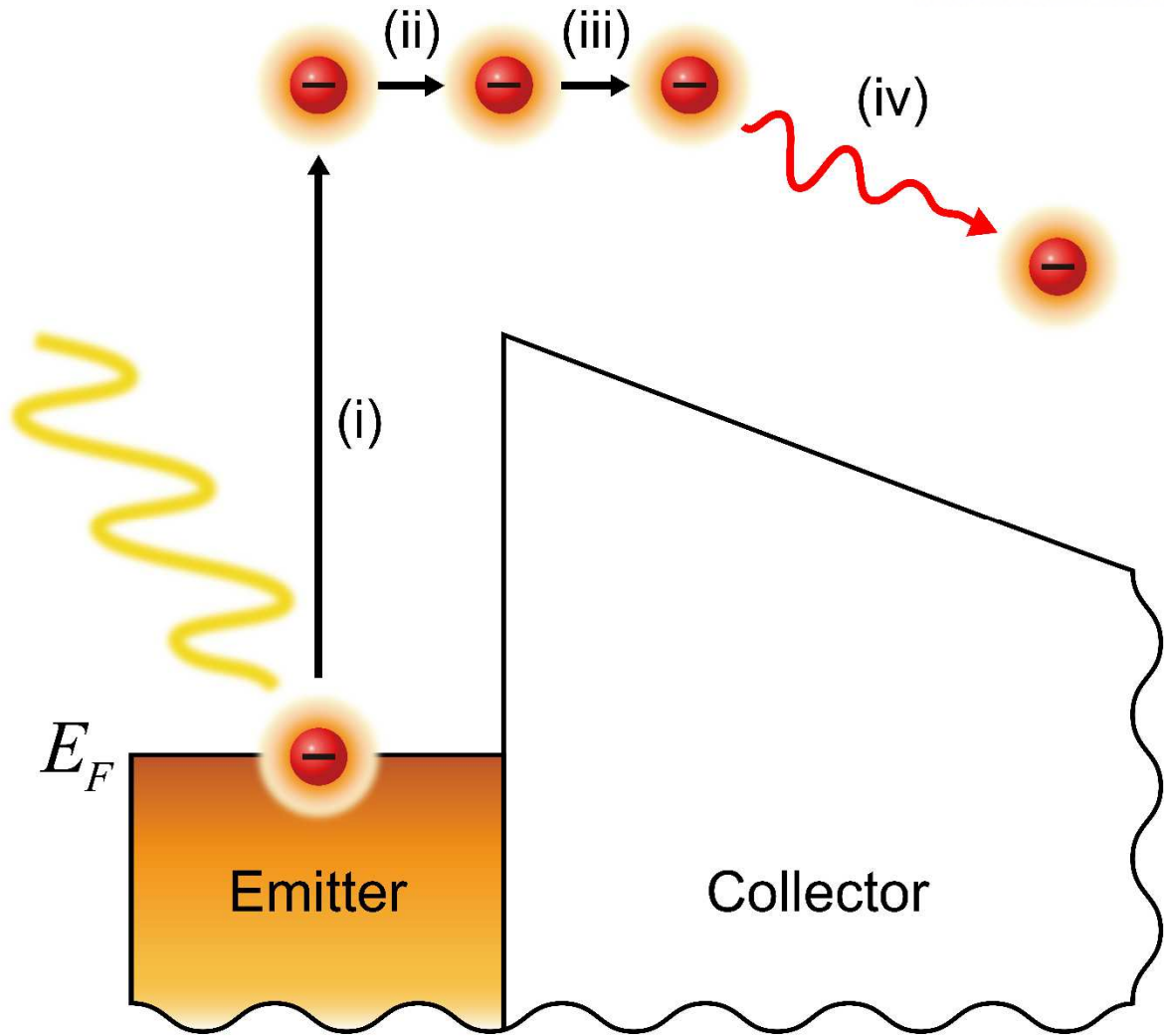


Figure 14. IPE process explained by the multi-step model [382] around the very near interface between emitter and collector, where E_F is the Fermi-level. (i) Optical excitation. (ii) Transport of electron to the surface. (iii) Surmount potential barrier. (iv) Collected as substrate current.

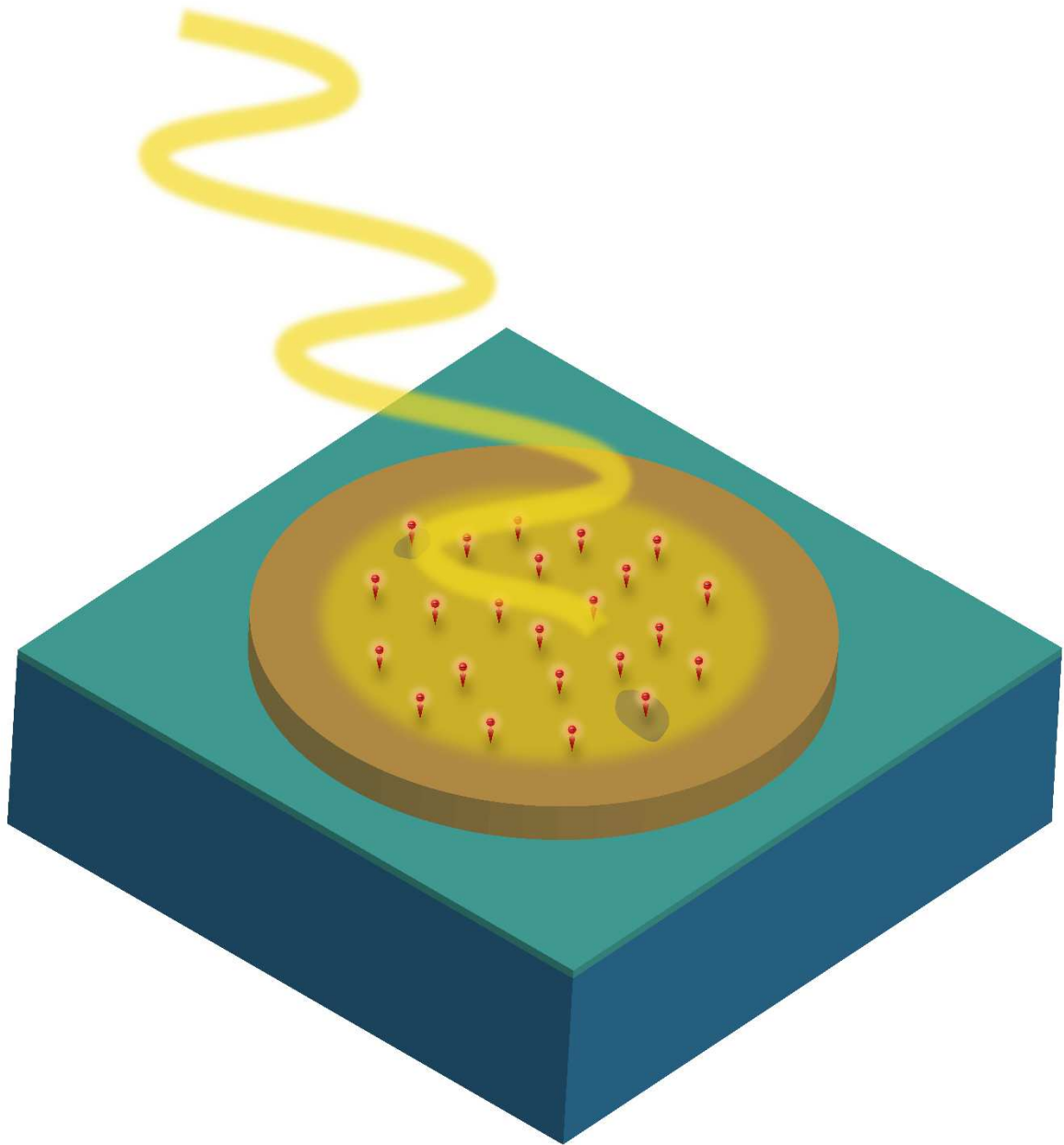


Figure 15. Schematic illustration of the Schottky contact showing that the photocurrent in the internal photoemission spectroscopy is acquired by the collective contribution of photo-excited carriers in all regions of the junction. The IPE measurement is not biased to the influence from the small areal fraction of low barrier patches so that it is capable of determining the energy barrier height at the junction interface of prevailing area.

The important feature of the IPE measurement is emerging from the photoelectric quantum yield Y (the ratio of the number $n_{emitted}$ of emitted electrons to the number $n_{excited}$ of excited electrons). It is necessary to clarify dependence of the measured photocurrent on the photon energy with light power in order to obtain the IPE quantum yield. The quantum yield $Y(h\nu)$ at photon energy $h\nu$ is given by Equations 44 and 45, where $n_{emitted}(h\nu)$ is the number of emitted electrons, $n_{excited}$ is the number of excited electrons, $I_{sample}(h\nu)$ is the photocurrent measured on the sample, $P(h\nu)$ is the incident light power, C is the proportional constant, ϕ_{th} is the threshold energy, and m is the power exponent depending on the quantum yield spectra. In the IPE spectra curve (the graph of IPE quantum yield $Y^{\frac{1}{m}}$ to the power of the reciprocal of the power exponent as a function of photon energy $h\nu$), the interfacial energy barrier can be obtained from the extracted threshold ϕ_{th} . It has to be careful that the threshold energy ϕ_{th} for the power exponent $m = 1$ is not equal to the potential energy barrier height at the interface.

Regarding the power exponent m [380-387], it is predicted that the electrons excited from energy states close to the Fermi level E_F of the metal (Figure 16) follow the Fowler's law ($m = 2$) [380], because the shape of photo-excited carrier distribution around the metal Fermi-level E_F looks like the step-function. On the other hand, the photo-excited electrons from the semiconductor valence band E_v (Figure 17) revealing the linear-function shape of photo-excited carrier distribution function are known to be follow the Powell's interpretation $m = 3$ [382].

$$Y(h\nu) = \frac{n_{emitted}(h\nu)}{n_{excited}(h\nu)} \propto \frac{I_{sample}(h\nu) \times h\nu}{P(h\nu)} \quad (44)$$

$$Y(h\nu) = C(h\nu - \phi_{th})^m \quad (45)$$

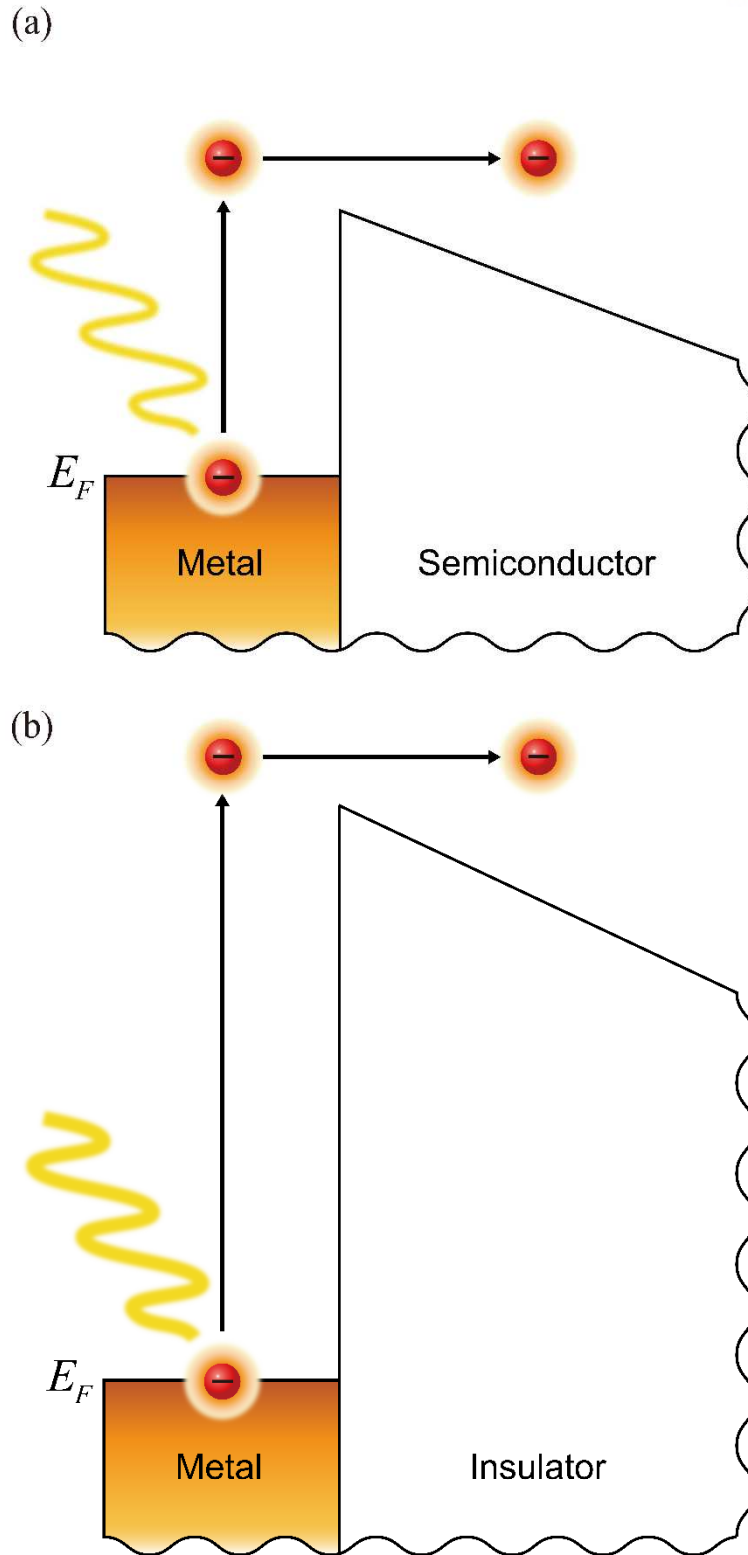


Figure 16. (a,b) Injection of optically excited electron from the metal Fermi-level E_F into the semiconductor (a) or the insulator (b), where the electrons follow the Fowler's law [380].

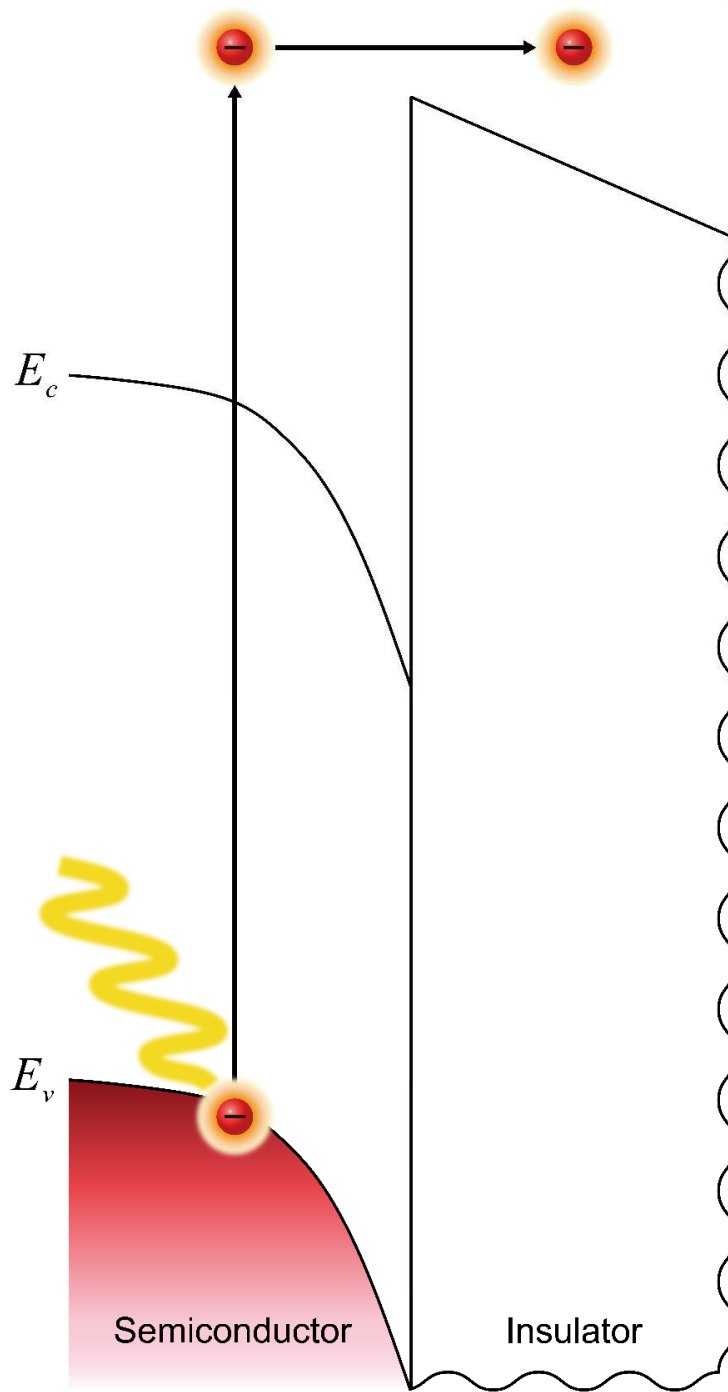


Figure 17. Injection of optically excited electron from the semiconductor valence band E_v into the insulator, where the electrons follow the Powell's interpretation [382].

As discussed in Chapter 1.4.3, the image force lowering energy $\Delta\phi$ should be also included in consideration of the influence of applied electric field on the surface potential energy ψ . This is why the IPE measurement is carried out by varying the substrate bias voltage.

The charge carriers can both get over (Figure 18a) and tunnel through (Figure 18b) the interfacial energy barrier. If the band bending becomes intensified due to the applied bias voltage, the photon-assisted-tunneling [385] can contribute to the photocurrent, unless it is completely limited by the very thick insulator.

Another contribution to the photocurrent can stem from the electrons directly excited from the localized energy states on the semiconductor surface for the metal/semiconductor junction. In general, the injection of excited electron from the metal Fermi-level E_F is responsible for the spectral threshold (Figure 19a). On the other hand, if the metal electrode has deep skin depth larger than its thickness, the light can penetrate into the semiconductor surface and induce the electron excitation from the localized states on it (Figure 19b). For example, the electronic states are known to be localized below the charge neutrality level E_{CNL} of the GaAs surface [388], leading to the strong Fermi-level pinning effect (Chapter 1.4.2). The direct electron excitation in the semiconductor induced by the incident light having the energy of the difference around between the conduction band edge E_c and the charge neutrality level E_{CNL} can contribute to the IPE signal. Thus, it is expected that the hump-shaped quantum yield in the IPE spectra for the Schottky junction implies the existence of localized interface states within the semiconductor band-gap. This is actually what I have identified through the experimental observation [389].

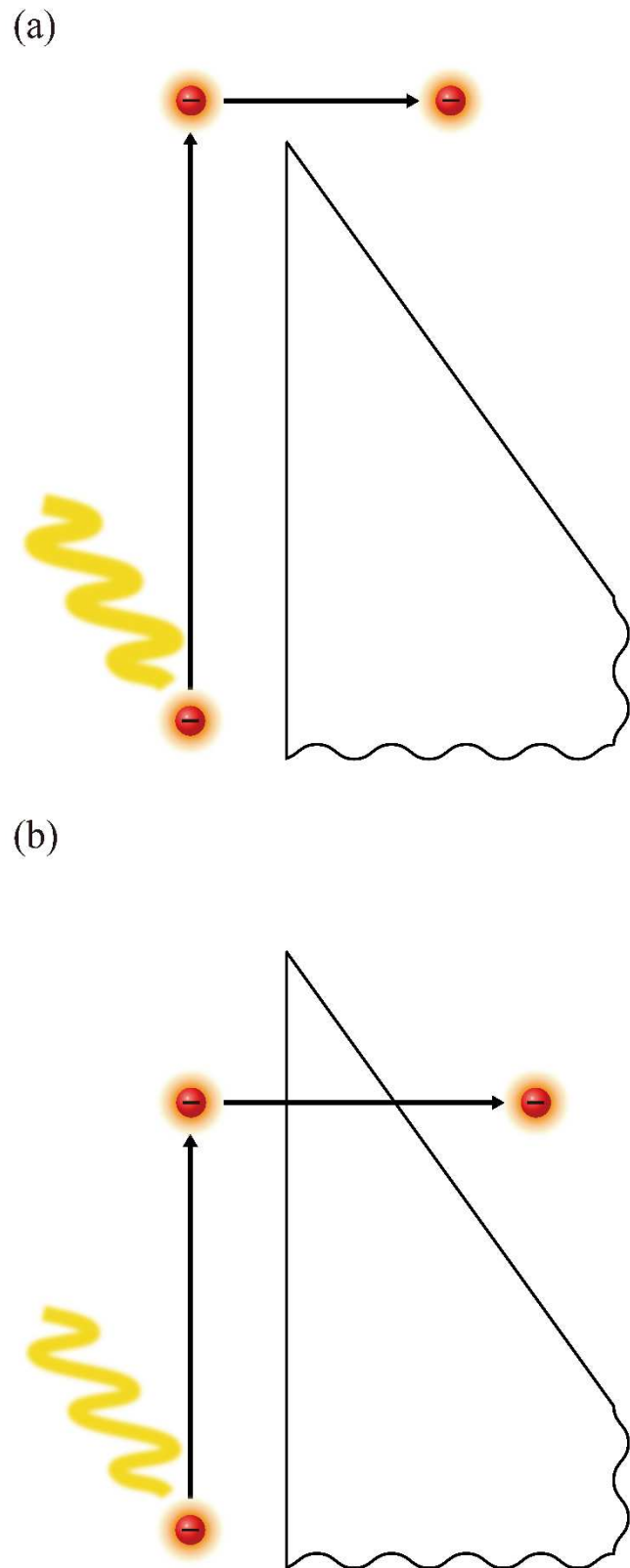


Figure 18. Injection of optically excited electron can directly surmount (a) or tunnel through (b) the interfacial energy barrier.

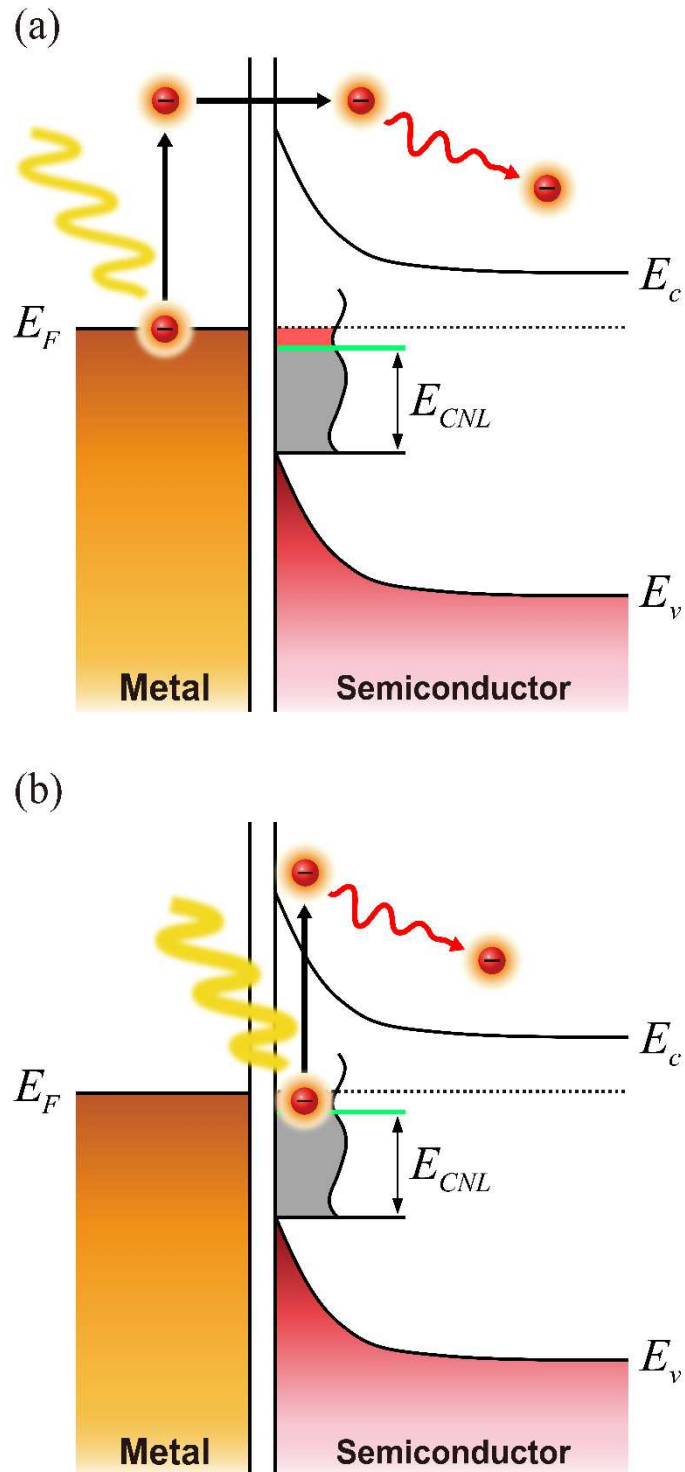


Figure 19. (a,b) Optical excitation of electron from the Fermi-level E_F of the metal (a) or the localized electronic states around the charge neutrality level E_{CNL} of the semiconductor (b) for the metal/semiconductor junction, where E_c is the conduction band edge in the semiconductor and E_v is the valence band edge in the semiconductor.

1.5.2 Experimental Setup

The experimental equipment required for the IPE measurement setup is shown in Figure 20, which consists of Xenon arc lamp, lamp power supply, lamp housing, Ozone eater, Ozone exhauster, optical filter, monochromator, grating, optical fiber, probe station, optical lens, lens holder, low-noise current pre-amplifier, and data acquisition card. The optical components were purchased from the Oriel Instruments (Newport) Corporation. For the different energy (wavelength) range, it is necessary to change the measurement configuration (Figure 21) such as cut-on wavelength of the optical filter, line density of the grating, slit width of the monochromator, transmittance range of the optical fiber, sensitivity of the low-noise current pre-amplifier, and types of the photodiode. By taking these points into consideration, each equipment was organized in the following procedures.

A Xenon arc lamp (Newport 6259 lamp for 300 W and 900-hour lifetime) receiving power through the Newport 70050 black cable plugged into the Newport 69911 power supply (Figure 20c) is used as the white light source with all wavelength. The wavelength-dependent light intensity of lamp should be verified with its spectral irradiance, which is linked directly to the incident light power. The Xenon lamp is mounted in the Newport 66902 lamp housing (Figure 20a). The plus sign of the Xenon lamp should be installed to go up inside the housing. The socket-adaptor should be equipped in the bottom side of the Xenon lamp. It should be warned that fingerprints or other foreign matter on the surface of the lamp can cause explosion after ignition, so be careful not to touch it with bare hands. If the lamp gets fingerprints or other foreign objects on the surface, use alcohol to clean the lamp surface carefully. In general, aware that all light source equipment is sensitive to humidity and it is recommended to wear ultraviolet-screening goggles when testing the lamp. Also note that care must be taken not to exceed the lamp lifetime.

After installing the lamp, adjust the up and down screws to align the lamp so that it is centered on the condenser lens and the emitted light can be maximized. There is a fan on the side of the lamp housing for stable cooling. When we use an Ozone-free lamp like the Newport 6258 model, we can leave the fan open. However, for Newport 6259 model in use, the fan should be wrapped with the Ozone exhauster (Figure 20b) and connected to the Newport 66087 Ozone eater (Figure 20d). Two Newport 66090 replacement filters are in the Ozone eater and their lifetime depends on the Ozone concentration in the airstream. (usually about 4000 hours at 4 ppm).

The lamp housing is sequentially connected to the filter holder (Figure 20f) and the monochromator (Figure 20e). There are four different optical filters are classified in the filter holder according to the cut-on wavelength (Newport 51352 filter #1 for 830 nm, Newport 51320 filter #2 for 630 nm, Newport 51272 filter #3 for 400 nm, and Newport 51250 filter #4 for 309 nm). The photon energy can vary from 0.8 to 5.5 eV using the grating equipped in the monochromator (74160 grating #2 for 600

lines/mm with the wavelength range of 600 ~ 2500 nm and 74167 grating #1 for 2400 lines/mm with the wavelength range of 180 ~ 700 nm).

Note that the resolution of light emitted by the monochromator depends on various factors. Since the grating line density and the light resolution are inversely proportional, if the line density doubles, the resolution gets half the value. On the other hand, the spectral bandwidth of light is proportional to the resolution. The resolution of light is also mediated by the slit width of monochromator. Each round of Newport 74001 slit width controller (Figure 20g) increases the width by 500 micrometers (100 micrometers slit width per grid marking). The maximum slit width of Oriel Cornerstone 260 1/4 m monochromator is about 3 mm.

The monochromatic light emitted from the monochromator is guided to the probe station (Figure 20i) through the optical fiber (Figure 20h). There are two types of optical fiber in use (Newport 77634 black for the wavelength range of 400 ~ 1700 nm and Newport 76840 blue for the wavelength range of 500 ~ 250 nm). The light is focused onto the sample mounted on the stage with the ultraviolet grade fused Silica lenses (Newport SPX011 plano-convex lens for conversion of dispersed light into parallel light and Newport SBX016 bi-convex lens for focusing of parallel light) housed in the lens holder (Figure 20m).

As shown in Figure 22, the design and manufacture process of the lens holder for stably fixing the lens and optical fiber. The lens holder is designed in consideration of diameter of the optical fiber and lenses, focal length of the lenses, distance between the end of optical fiber and the position of lenses. The focused light through the lens holder in the visible wavelength range is shown in Figure 23.

During the IPE measurement (Figure 20m and Figure 24), a low-noise current pre-amplifier (Figure 20j) with a data acquisition card (Figure 20k) is utilized to measure the photocurrent $I_{sample}(h\nu)$ on the sample or photodiode. The sensitivity of a low-noise current pre-amplifier should be adapted to maximize the measured photocurrent. The photocurrent versus the photon energy data can be automatically extracted by LabVIEW and MAX (Measurement & Automation Explorer) programs supported by the National Instruments Corporation. The dark current noise is also automatically corrected in the system by subtracting the dark current from the measured photocurrent.

Figure 25 shows the spectral power distribution of incident light obtained by using two kinds of photodiode (Hamamatsu Photonics G9230-01 InGaAs photodiode (950 ~ 1550 nm) and Hamamatsu Photonics S2281-04 Si photodiode (200 ~ 1180 nm). The incident light power $P(h\nu)$ converted from the photocurrent $I_{photodiode}(h\nu)$ measured on the photodiode divided by the spectral photosensitivity $S(h\nu)$ of the photodiode (Equation 46) is used to calculate the photoelectric quantum yield $Y(h\nu)$ (Chapter 1.5.1). Equations 44-46 can be combined into Equation 47.

$$P(h\nu) = \frac{I_{\text{photodiode}}(h\nu)}{S(h\nu)} \quad (46)$$

$$h\nu \times S(h\nu) \times \frac{I_{\text{sample}}(h\nu)}{I_{\text{photodiode}}(h\nu)} \propto C(h\nu - \phi_{\text{th}})^m \quad (47)$$

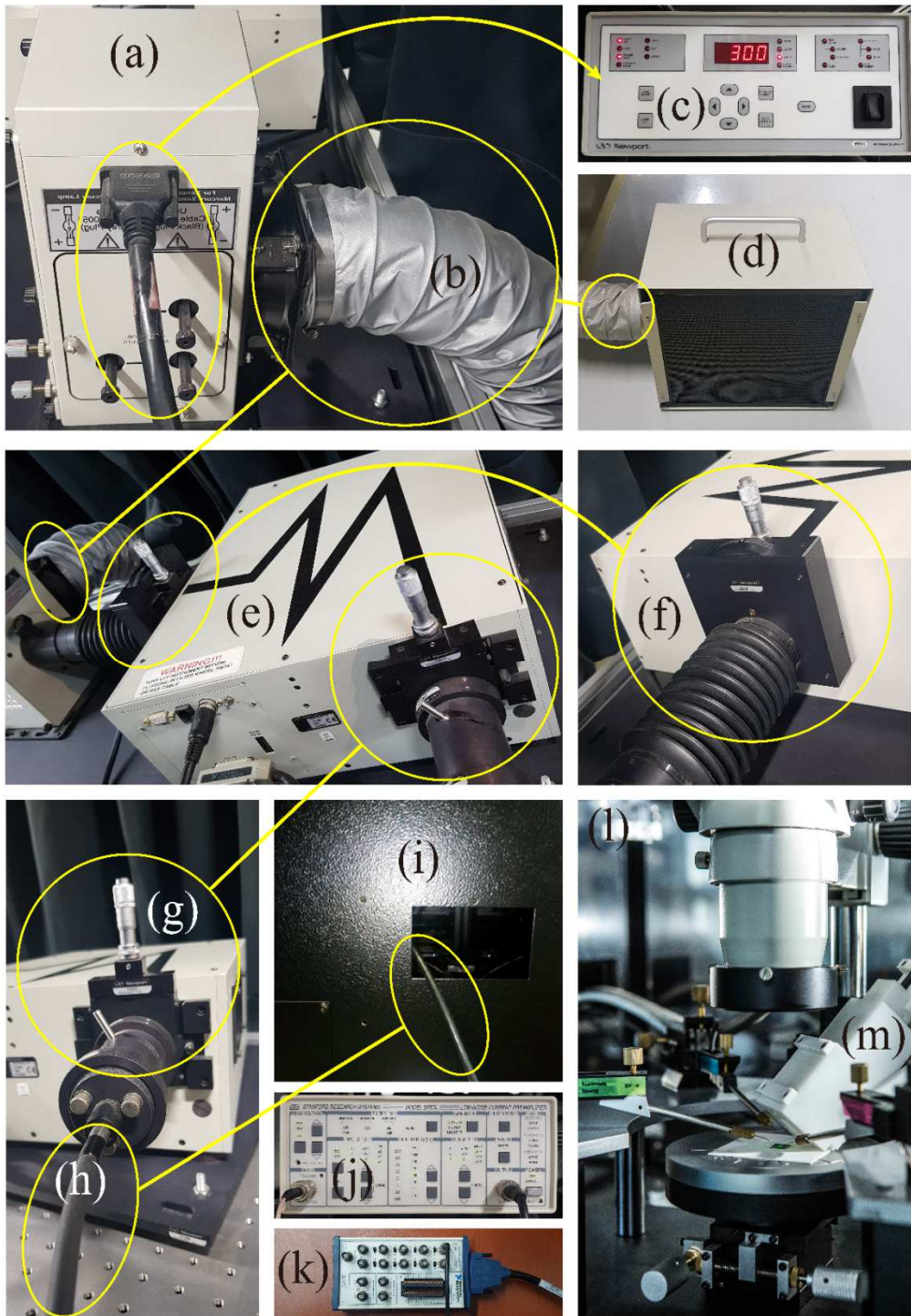
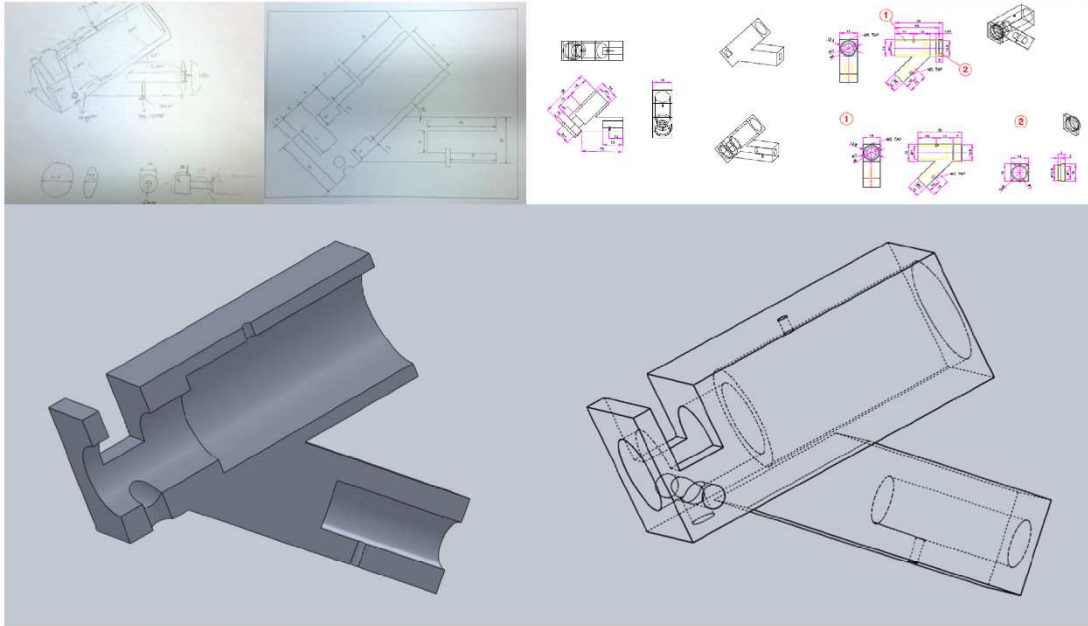


Figure 20. Diagram showing the components of the IPE system. (a) Lamp housing (Xenon arc lamp is mounted in it). (b) Ozone exhauster. (c) Lamp power supply. (d) Ozone eater. (e) Monochromator equipped with two different kinds of gratings. (f) Filter holder (Four different optical filters are sorted in it). (g) Slit width controller. (h) Optical fiber. (i) Probe station. (j) Low-noise current pre-amplifier. (k) Data acquisition card. (l) IPE measurement inside the probe station. (m) Lens holder (Two different optical lens are housed in it).

Photon Energy (eV)	0.5	0.8	1.1	1.3	1.48	1.55	1.8	1.88	1.97	2.07	2.47	2.5	2.8	3.1	3.5	3.87	4.02	4.9	5	5.5	6	6.88
Wavelength (nm)	2480	1560	1127	954	830	800	689	870	630	600	502	495	443	400	354	320	309	276	248	225	207	180
Optical Filter					Filter 1 Cutoff				Filter 2 Cutoff					Filter 2 Cutoff				Filter 4 Cutoff				
Grating	Grating 2											Grating 1										
Optical Fiber	Black OF											Blue OF										
A	Filter 1 / Grating 2 / Black OF Interval: 0.005 eV <Sample> Full Silt (3000 um) <PDS: 52281-01> Full Silt (3000 um) 50 uA/V																					
	Filter 2 / Grating 2 / Black OF Interval: 0.005 eV <Sample> Full Silt (3000 um) <PDS: 52281-01> Full Silt - 12.5 (3000 - 1250 um) 1 mA/V																					
B												Filter 3 / Grating 2 / Black OF Interval: 0.005 eV Sample Full Silt (3000 um) <PDS: 52281-01> Full Silt (3000 um) 1 mA/V										
												Filter 3 / Grating 1 / Black OF Interval: 0.005 eV <Sample> Full Silt - 17.5 (3000 - 1750 um) <PDS: 52281-01> Full Silt - 17.5 (3000 - 1750 um) 20 uA/V										
C												Filter 4 / Grating 1 / Blue OF Interval: 0.005 eV <Sample> Full Silt - 27.0 (3000 - 2700 um) <PDS: 52281-01> Full Silt - 27.0 (3000 - 2700 um) 20 uA/V										
												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 5 uA/V										
D												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										
												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										
E												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										
												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										
F												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										
												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										
G												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										
												Filter 5 / Grating 1 / Blue OF Interval: 0.005 eV Sample Full Silt - 28.5 (3000 - 2850 um) <PDS: 52281-01> Full Silt - 28.5 (3000 - 2850 um) 500 mA/V										

Figure 21. IPE measurement configuration for each energy (wavelength) range.



- ① SBX016 LENS
- ② SPX011 LENS
- ③ GUIDE
- ④ END CAP
- ⑤ OPTICAL FIBER

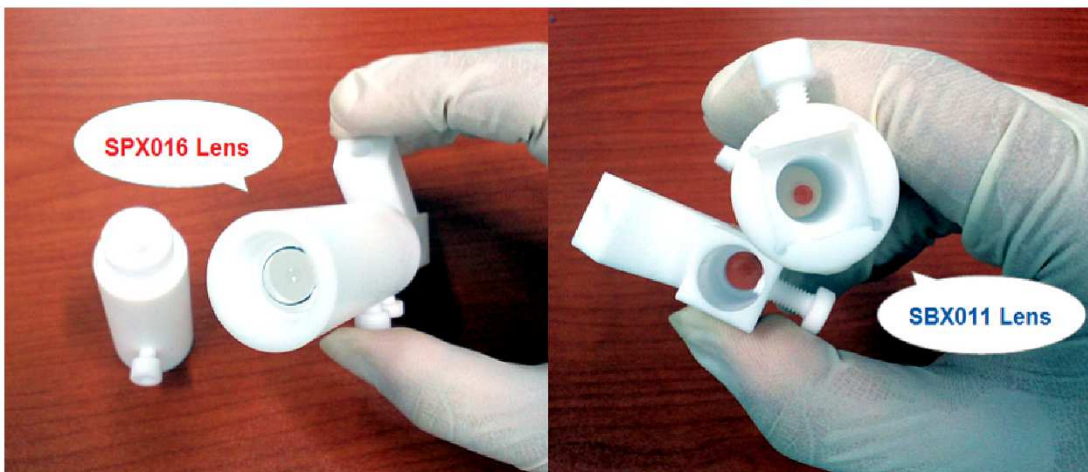
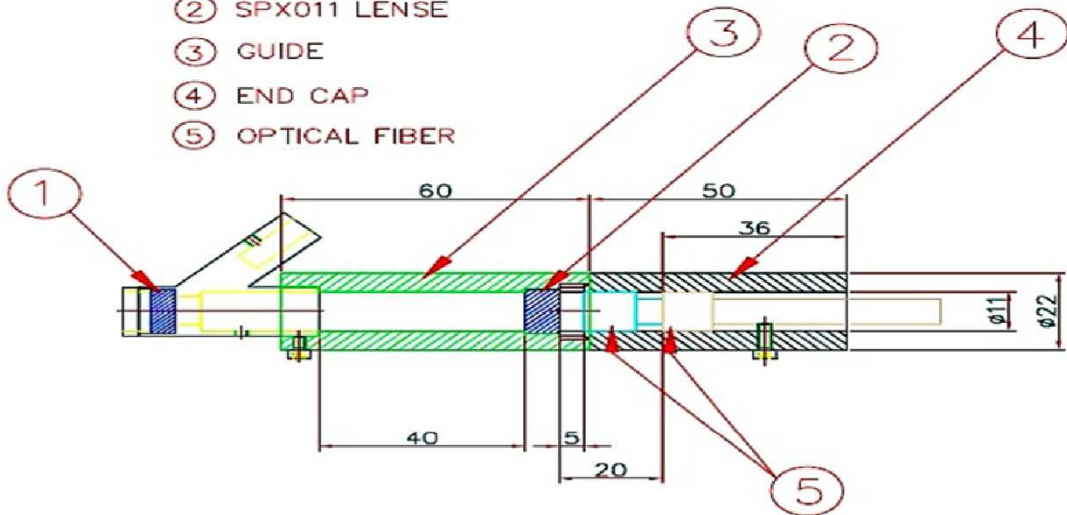


Figure 22. Design and manufacture process of the lens holder.

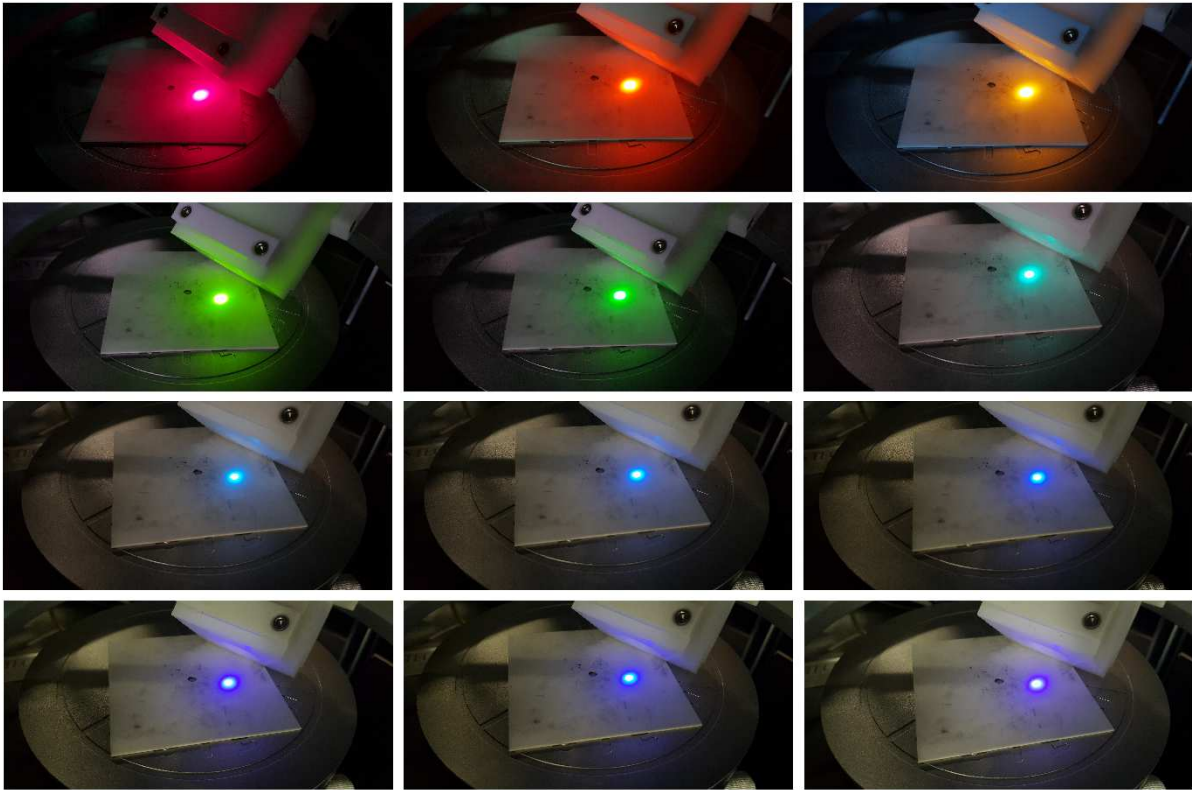


Figure 23. Focused light through the lens holder in the visible wavelength range.

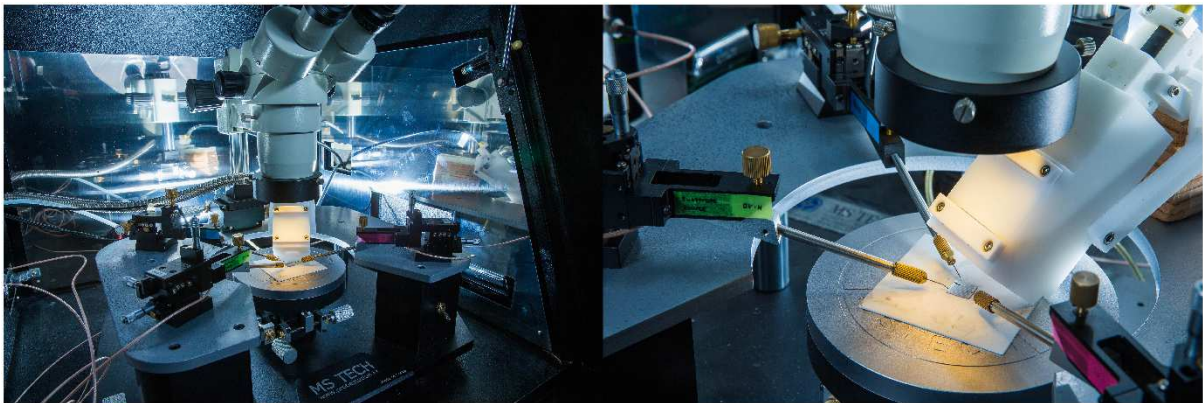


Figure 24. IPE measurement system.

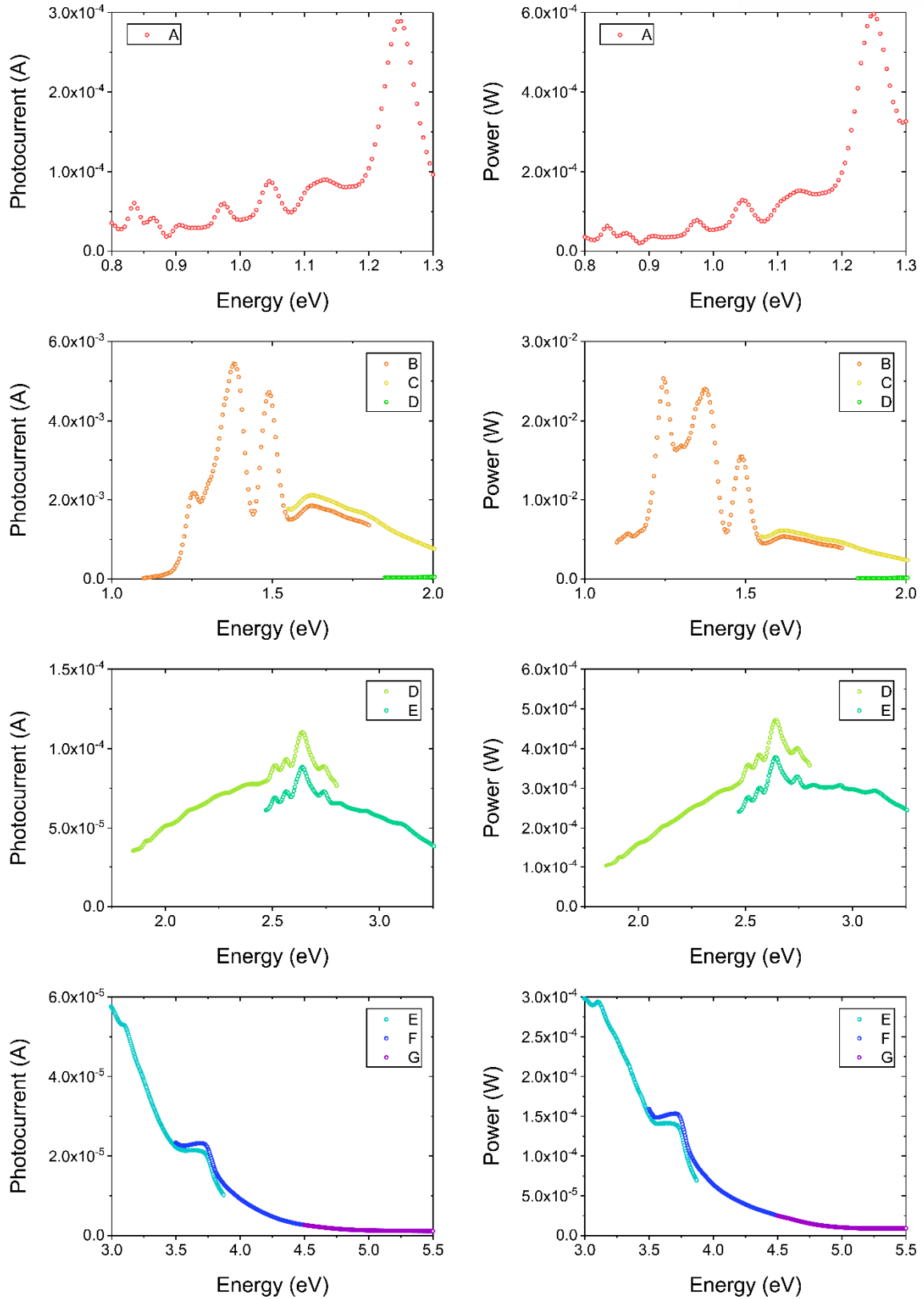


Figure 25. IPE measurement configuration for each energy (wavelength) range.

1.6. Graphene Hetero-Interface

A number of techniques with regard to typical mechanical exfoliating, polymer-assisted (wet, dry, and semi-dry) transferring, roll-to-roll printing of a graphene monolayer onto arbitrary substrates have been developed [390-406]. Those techniques are effective to maximize its mobility, enlarge its surface area, reduce chemical residues or structural defects (Figure 26) generated during the transfer process, and eventually improve its overall quality, uniformity, and reproducibility. The nicely transferred graphene layer reveals well-terminated surface without dangling bonds, which is suitable for a component in hetero-junction. The graphene-based hetero-interface can be combined with metals, semiconductors, and other 2D Van der Waals materials. The issue of improving the electrical contacts [159-162] between graphene and different materials through understanding of charge transfer at the graphene interface [163-166] and charge transport through the graphene interface [167-170] has stimulated a lot of research interest.

(a)



(b)

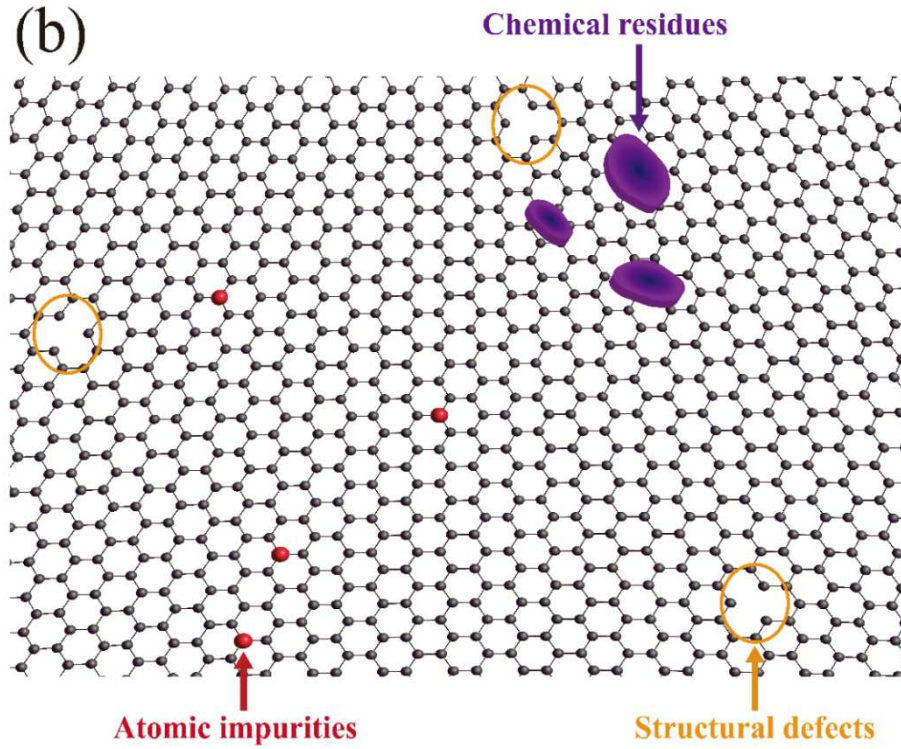


Figure 26. (a) Photo taken near the playground showing the hexagonal mesh structure. (b) Graphene lattice structure drawn with chemical residues, atomic impurities, and structural defects, which is inspired by the photo.

1.6.1 Graphene-Metal Interaction

The electrical contacts between graphene layer and metal electrode is very essential for fabricating the graphene-based devices. It is known that the interaction between graphene and metals induce the charge transfer, varies the adsorption characteristic, derives the different kinds of bonding, shifts the Fermi-level alter the doping of graphene, and forms the interfacial dipole layer [163-164] supported by the density functional theory (DFT) calculations. The interaction dipole charge density is known to exist due to the overlapping of electron wave-functions in the metal/graphene gap [163-164]. The weak interaction of graphene with Al, Ag, Cu, Au, and Pt allows graphene to be physisorbed on metals while the strong interaction of graphene with Co, Ni, Pd, and Ti leads graphene to be chemisorbed on metals [163-164].

The physisorbed graphene involves only short-range interaction. This short-range interaction has effect on the graphene doping and the interface dipole formation but the original band structure of graphene is maintained. As shown in Figure 27, the type and level of doping (the Fermi-level shift from relative to the Dirac point) depends on the physics of graphene-metal interface such as the work-function of metal modified by the adsorption of graphene (generally consistent with the sign and size of interface dipole) as well as the Van der Waals gap (the vacuum separation between graphene and metal).

In other hands, the chemisorbed graphene brings about the hybridization between p_z -orbital in the graphene (illustrated in Figure 4) and d-orbital in metal. This orbital hybridization is considerable chemical reaction to change the electronic property of graphene significantly, destroy the band structure of graphene, banish the Dirac point, and even open the band-gap of graphene. The perturbed graphene namely dramatically creates a much more complicated system with metals, contains the abundant electron carriers like donor, and lower the metal work-function eventually.

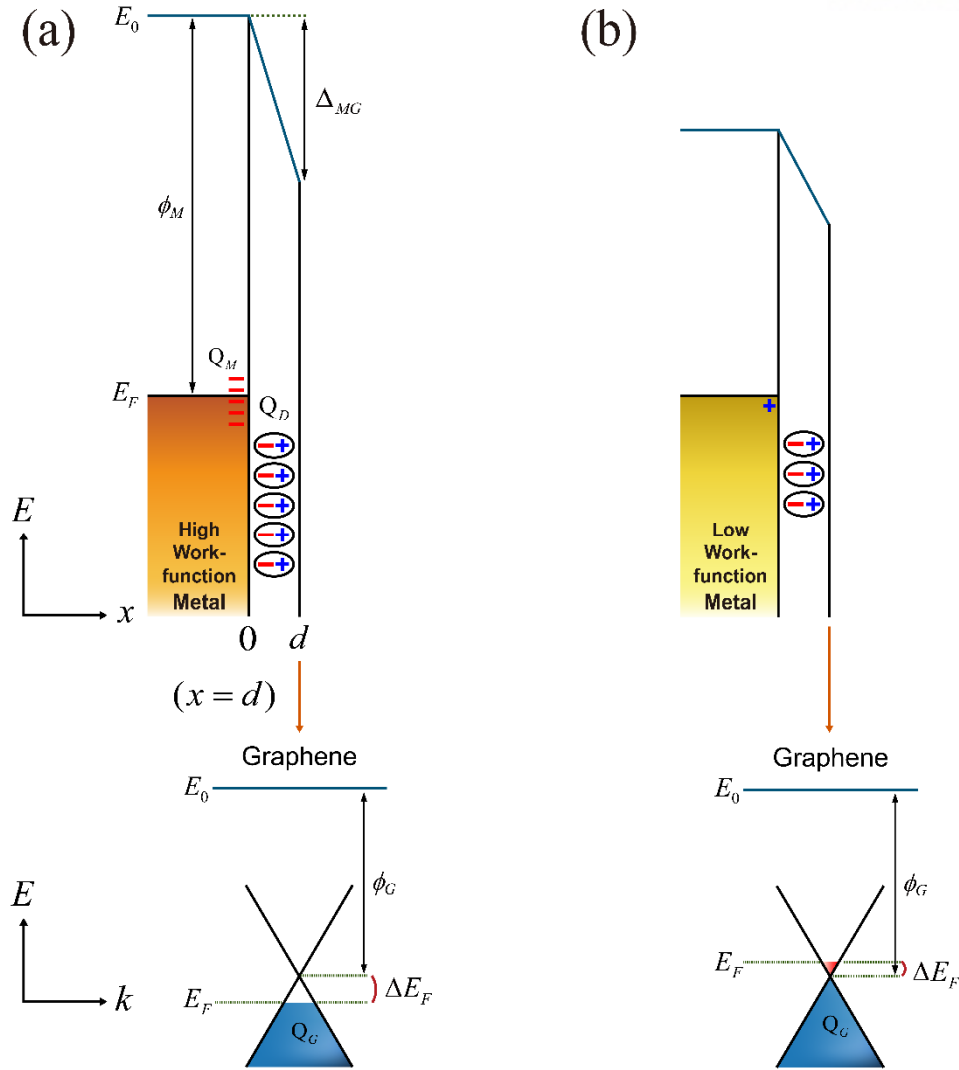


Figure 27. Energy band alignments of metal/graphene junctions with high (a) and low (b) metal work-functions for the physisorbed graphene on metals showing the graphene-metal interaction [163-164], ϕ_M is the work-function of the metal, ϕ_G is the work-function of the graphene, E_F is the Fermi-level, ΔE_F is the Fermi-level shift in the graphene, E_0 is the vacuum level, Δ_{MG} is the potential energy change between the metal and graphene, Q_M is the charge density on the metal surface, Q_D is the dipole charge density, Q_G is the doping charge density of the graphene, and d is the Van der Waals gap distance between the graphene and the metal.

1.6.2 Graphene Diffusion Barrier

Due to the orbital hybridization explained in Chapter 1.3.2, the high dense electron cloud fills the openings in hexagonal lattice of graphene. The compactness of electronic states near the openings is superb, other atoms cannot easily penetrate through the graphene [176, 177, 407-412]. Borrowing this impermeability, we can utilize the atomically-thin graphene layer as a diffusion barrier blocking the material intermixing like a protective coating film as shown in Figure 28. An intact junction formed by the graphene diffusion barrier is utilized to reduce the sub-threshold leakage current or increase the photocurrent signal during the transport measurement of charge carriers crossing the clean interface [177, 389].

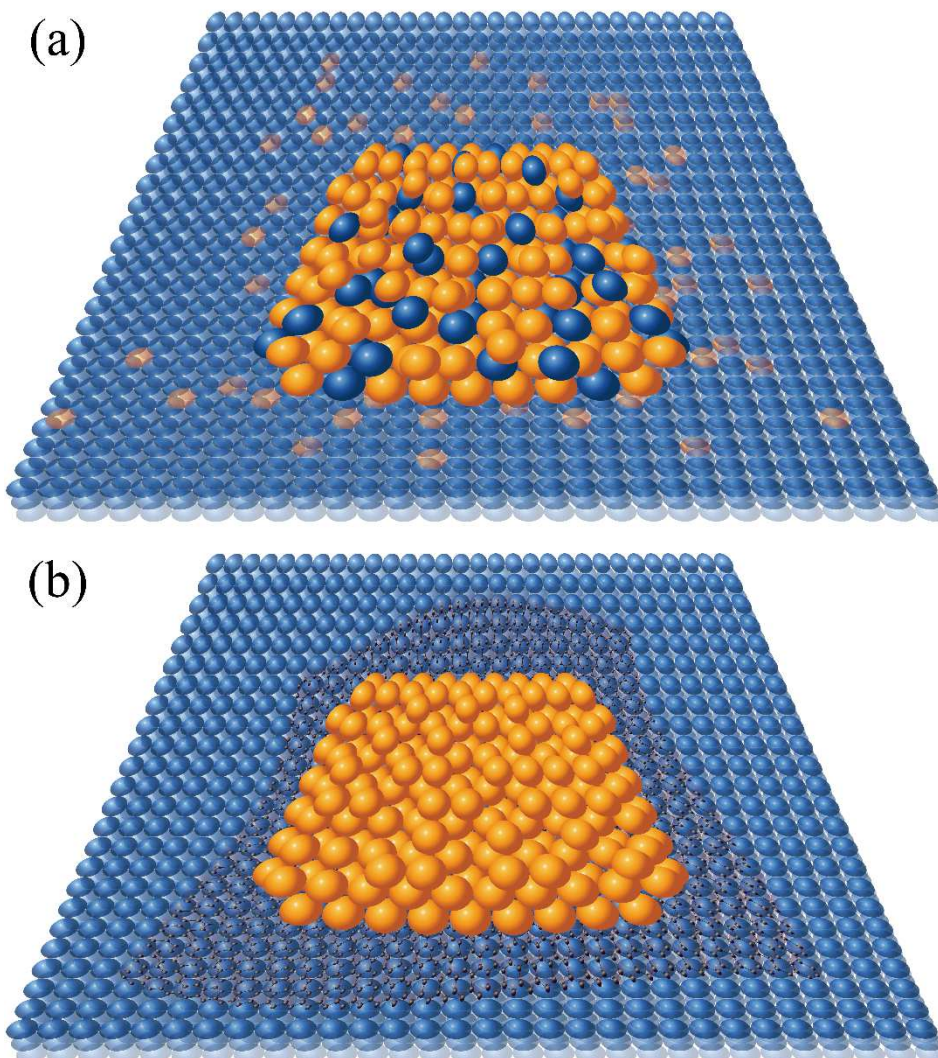


Figure 28. (a) Diffusion of atoms into a solid substrate. (b) Graphene diffusion barrier protecting the surface from atomic diffusion.

1.6.3 Graphene Interlayer

A dimensionality is itself known as a crucial factor related to performance optimization and power consumption in nanoscale device [15]. However, giving degree of freedom to the moving direction of charge carriers creates a much higher level of physical regime. The vertical stacking of graphene with other 2D Van der Waals materials [171-174] is part of this attempt. The mixed-dimensional Van der Waals system can be also interfaced with the graphene [413-415].

From a slightly different perspective, combining graphene-metal interaction [163-164] (Chapter 1.6.1) with graphene diffusion barrier [176, 177, 407-412] (Chapter 1.6.3) makes possible to invent another complex system. Graphene interlayer sandwiched between bulk metal and semiconductor substrate simply looks like 3D/2D/3D hetero-structure. However, ballistic carrier transport measured on the graphene-based hetero-junction introduced in this thesis is considered as 1D parallel charge carrier transport through 2D-layer-interfaced 3D hybrid system.

The functionality of graphene as a diffusion barrier enables to obtain the intact Schottky contacts and investigate the surface states on semiconductor substrate [177]. The interaction between graphene and metal is found to result in forming electric dipole charges at the interface between metal and graphene, which makes the potential differences crossing the interface (Figure 29) [389]. Therefore, by employing the interlayer, it is possible to modulate electronic states at the interface and regulate charge distribution across the interface. In order to discover the hidden physics in the graphene-based hetero-interface, understanding the role of graphene interlayer inserted at the metal/semiconductor junction is one of the main purpose of my research.

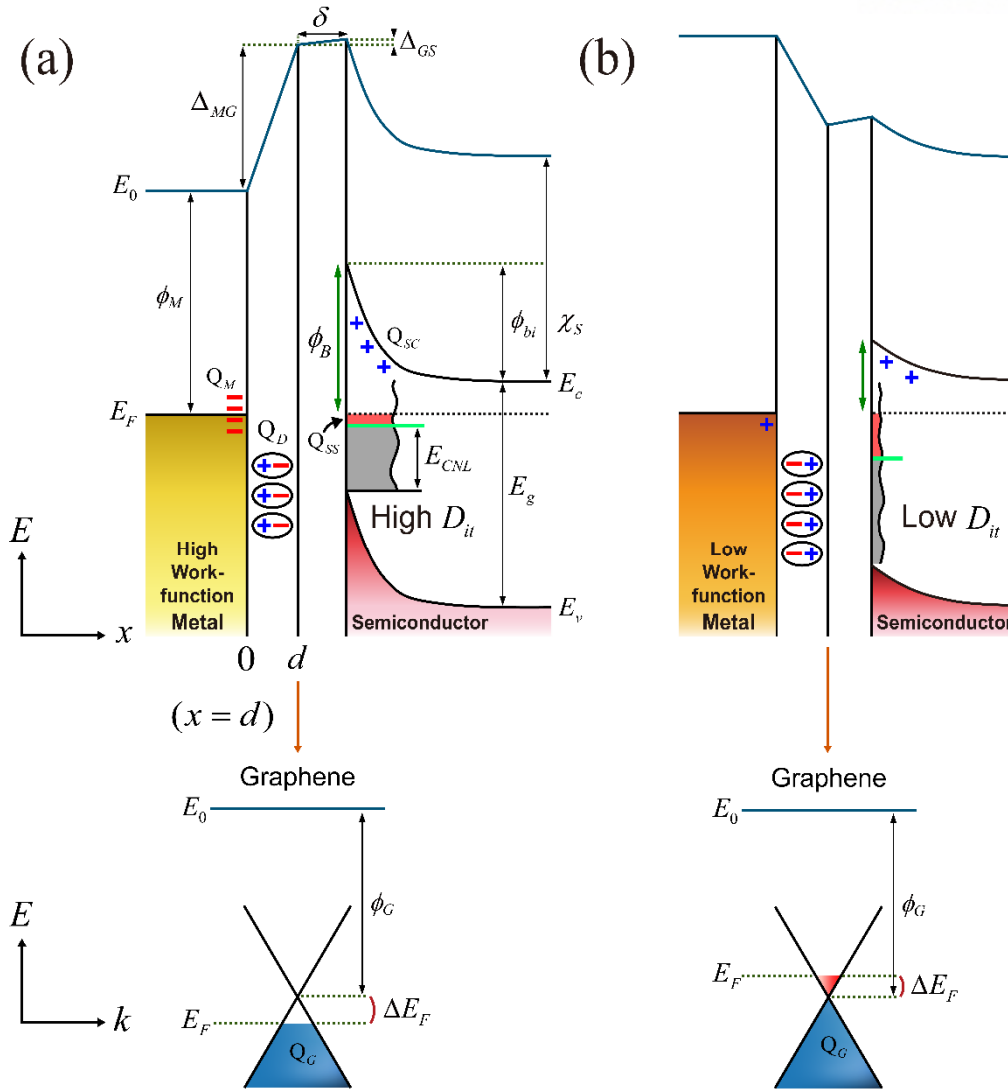


Figure 29. Energy band alignments of metal/graphene/n-semiconductor junctions for the high (a) and low (b) interface-trap densities regions, where ϕ_B is the Schottky barrier height, ϕ_M is the work-function of the metal, ϕ_G is the work-function of the graphene, ϕ_{bi} is the built-in potential energy, E_F is the Fermi-level, ΔE_F is the Fermi-level shift in the graphene, E_0 is the vacuum level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, E_{CNL} is the charge neutrality level of the semiconductor, E_g is the band gap of the semiconductor, Δ_{MG} is the potential energy change between metal and graphene, Δ_{GS} is the potential energy change between graphene and semiconductor, Q_M is the charge density on the metal surface, Q_D is the interaction dipole charge density, Q_G is the doping charge density of the

graphene, Q_{ss} is the interface-trap charge density, Q_{sc} is the space charge density, d is the Van der Waals gap distance between the graphene and the metal. D_{it} is the interface-trap density on the semiconductor surface, χ_s is the electron affinity of the semiconductor, and δ is the gap distance of the vacuum or the thin insulating layer between the graphene and the semiconductor. [389].

1.7 Dirac Fermion Quantum Optics in Graphene

As is well known, the electron as charge quantum is a fermion following the Fermi-Dirac statistics as well as the Pauli exclusion principle [416-418], and it has finite mass and half-odd-integer spin. On the other hand, the photon as light quantum is a boson following the Bose-Einstein statistics and it has zero-mass and integer spin. Since the photon is an exchange particle of a fundamental electromagnetic force, electron emit or absorb the photon to lose or get the energy. But the photon cannot emit or absorb the electron. Moreover, the photon has the speed of light which can never be attained by the maximum speed of electron. In spite of these intrinsic differences between electron and photon, the analogy between ballistic electron propagation and classical wave optics has drawn a great deal of attention by recalling functionality and versatility of optical elements for manipulation of photon such as focusing, collimation, and interference.

Electron quantum optics is the concept of manipulating of electrons in solid like photons in air and controlling the quantum state of propagating electrons. The quantum control of wave nature of the electron can ultimately be utilized for quantum computing or quantum information processing in electronic devices [419-421]. Nevertheless, such quantum effect is not easily detected and only realized in ultraclean samples at cryogenic temperatures under strong magnetic fields. In this connection, the laterally-conducting and vertically-confined two-dimensional electron gas (2DEG) formed at the interface in epitaxial hetero-structures [422-431] ensuring high mobility and ballistic carrier transport has enabled us to develop optimal means for electron quantum optics.

Graphene is considered as another ideal platform to approach electron quantum optics [63-67]. The phenomena traced in classical wave optics are also clearly observed in the graphene such as focusing [73-77], angle-dependent transmission [78-82], collimation [83-87], reflection [98-102], interference [103-107], Aharonov-Bohm oscillation [108-112], localization [113-117], and confinement [118-122].

However, regarding the natural constraints on electron imitating photon, it is quite difficult to steer the electron wave packets with no spatial spreading and manipulate the electronic quantum states. Thus, building a completely controllable electron quantum optics system has still remained as a challenging task.

1.7.1 Klein Tunneling in Graphene

If we imagine a flying ball shot to a wall, we can easily predict the three futures. One is that the ball will hit the wall generously and be reflected from it. Another is that the ball will jump over the wall. The other is that the ball will collide with the wall very harshly, smash it, and go through it. Here, we have to consider the energy related issues and there is no probabilistic causation. As we all recognize, this is the classical picture of the Newtonian mechanics [432-434].

In quantum world, an elementary particle has wave-like motion. In other words, the particle approaching close to a potential barrier can be reflected or transmitted according to different probabilities. Even if the height of potential barrier is lower than the particle's total energy, the particle encountering the wall can be bounced off from the potential barrier which acts like an invisible net. The most interesting point is that the incident particle can penetrate through the potential barrier with its height even greater than the total energy of particle and appear on the opposite side eventually. There is no energy loss in such a process. This quantum tunneling effect is widely known as one of the basic exercise in the quantum mechanics [435-437].

Moreover, Oskar Klein found the unprecedented effect [438, 439] called as the Klein paradox that a potential barrier seen by a charged particle is almost transparent and the backscattering is dramatically suppressed without damping if the height of potential barrier is comparable to the mass of charged particle. In the relativistic quantum mechanics [440-442] that must use the Dirac equation [186] not the Schrödinger equation, the quantum tunneling effect is valid with surprisingly one hundred percent regardless of the height and width of potential barrier at vertical incidence, which refers to the Klein tunneling [68-72].

As explained in Chapter 1.3.2, the charge carrier in the graphene also act like the massless Dirac particle. The particle described by the Dirac equation satisfy the following fundamental conservation laws [72]. The conservation of total energy is valid due to the time-invariance of system. The lateral momentum perpendicular to the interface varies according to the potential profile, while the transverse momentum parallel to the interface is generally conserved. The momentum projection k_y along the y direction is also conserved in accordance with translational invariance (Equations 48 and 49). The x directional velocity operator \hat{v}_x is found to be identical to the x directional pseudo-spin operator $\hat{\sigma}_x$ (Equation 50). Interestingly, its time evolution does include the y directional momentum k_y (Equation 51). Therefore, when the electron initially has zero momentum $k_y(t) = k_y(0) = 0$ along the y direction, the velocity v_x and pseudo-spin σ_x along the x direction are always constant. In other words, a small change in the x direction momentum v_x for backscattering requires the inversion of pseudo-spin. Accordingly, the charge carrier can transmit perfectly along the x direction in the absence of backscattering at normal incidence, which is identical to the Klein tunneling [68-72].

$$\dot{k}_y = \frac{1}{i} [k_y, \hat{H}_{total}] = 0 \quad (48)$$

$$k_y(t) = k_y(0) \quad (49)$$

$$\hat{v}_x = \frac{1}{i} [x, \hat{H}_{total}] = \hat{\sigma}_x \quad (50)$$

$$\dot{\hat{v}}_x = \frac{1}{i} [\hat{\sigma}_x, \hat{H}_{total}] = 2\hat{\sigma}_z k_y \quad (51)$$

Figure 30a shows the electron in the graphene is incident from the left (I) on the sharp square potential barrier (II) of width w and transmitted to the right (III), where ϕ is the incident angle, φ is the transmitted angle escaping from the potential barrier, $k_I = (k_x, k_y) = \frac{E}{\hbar v_F} (\cos \phi, \sin \phi)$ is the incident momentum wave-vector, $k_R = (-k_x, k_y) = \frac{E}{\hbar v_F} (-\cos \phi, \sin \phi)$ is the reflected momentum wave-vector, $k_A = (k_a, k_y) = -\frac{E-U}{\hbar v_F} (\cos \varphi, \sin \varphi)$ is the transmitted momentum wave-vector inside the potential barrier, $k_B = (-k_a, k_y) = -\frac{E-U}{\hbar v_F} (-\cos \varphi, \sin \varphi)$ is the reflected momentum wave-vector inside the potential barrier, $k_T = k_I$ is the transmitted momentum wave-vector escaping from the potential barrier, E is the total energy of the electron, \hbar is the plank constant. v_F is the Fermi velocity, and U is the potential barrier height. The Snell-Descartes law with transverse momentum conservation implies the following relation (Equation 52). The wave-functions in the left (I), the potential barrier (II), and the right (III) are given by ψ_I , (Equations 53-55) ψ_{II} , and ψ_{III} respectively [68. 72], where A is the coefficient corresponding to the k_A , B is the coefficient corresponding to the k_B , R is the reflection probability, and T is the transmission probability. By solving the Equations 53-55 at $x=0$ and $x=w$, we can obtain the transmission probability T represented by Equation 56. The transmitted momentum wave-vector component k_a along the x direction inside the potential barrier is written as Equation 57. It is found that the transmission probability T is greatly influenced by the incident angle $\phi = \tan^{-1} \left(\frac{k_y}{k_x} \right)$ and has nothing to do with the potential barrier width w . Surprisingly, if the incident momentum wave-vector component k_y along the y direction is zero ($\phi=0$ at normal incidence), the transmission probability T becomes one, i.e., the Klein tunneling [68-72].

$$E \sin \phi = -(E - U) \sin \phi \quad (52)$$

$$\psi_{\text{I}} = \left[\begin{pmatrix} 1 \\ e^{i\phi} \end{pmatrix} e^{ik_x x} + \sqrt{R} \begin{pmatrix} 1 \\ -e^{-i\phi} \end{pmatrix} e^{-ik_x x} \right] e^{ik_y y} \quad (53)$$

$$\psi_{\text{II}} = \left[A \begin{pmatrix} 1 \\ -e^{i\phi} \end{pmatrix} e^{ik_a x} + B \begin{pmatrix} 1 \\ e^{-i\phi} \end{pmatrix} e^{-ik_a x} \right] e^{ik_y y} \quad (54)$$

$$\psi_{\text{III}} = \sqrt{T} \begin{pmatrix} 1 \\ e^{i\phi} \end{pmatrix} e^{ik_x x} e^{ik_y y} \quad (55)$$

$$T = \frac{\cos^2 \phi \cos^2 \phi}{\cos^2 \phi \cos^2 \phi \cos^2(k_a w) + \sin^2(k_a w) [1 + \sin \phi \sin \phi]^2} \quad (56)$$

$$k_a = -\frac{U}{\hbar v_F} \sqrt{1 - 2 \left(\frac{E}{U} \right) + \left(\frac{E}{U} \right)^2 \cos^2 \phi} \quad (57)$$

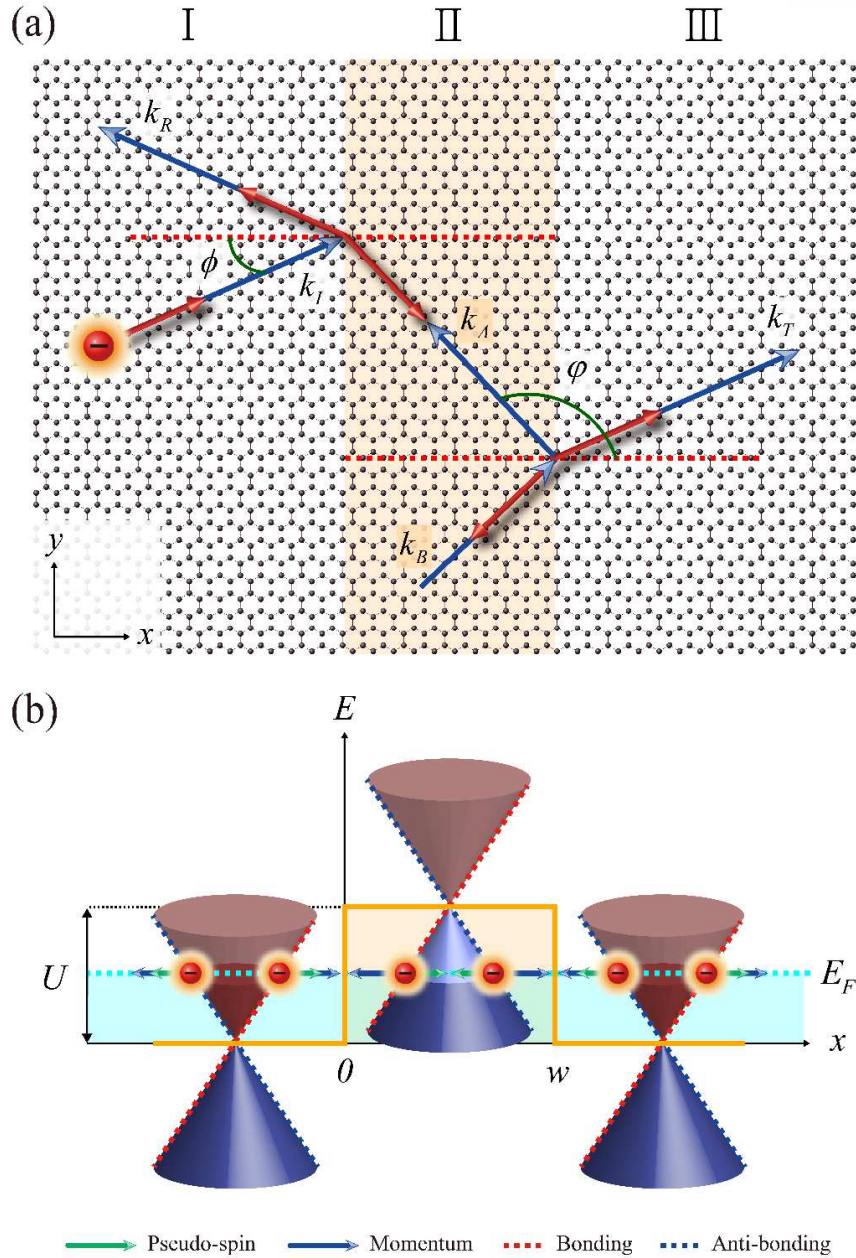


Figure 30. (a) Schematic of the electron in the graphene incident on the sharp square potential barrier of height U and width w , where ϕ is the incident angle, φ is the transmitted angle escaping from the potential barrier, k_I is the incident momentum wave-vector, k_R is the reflected momentum wave-vector, k_A is the transmitted momentum wave-vector inside the potential barrier, k_B is the reflected momentum wave-vector inside the potential barrier, and k_T is the transmitted momentum wave-vector escaping from the potential barrier. (b) The corresponding band structure of graphene [68-72], where E_F is the Fermi-level.

1.7.2 Superlattice Pattern in Graphene

Many researchers have adopted the superlattice on the graphene by using the Kronnig-Penny type periodic structure (Figure 31a) [88-97], nanoribbon [443-446], nanomesh [447-450], nanodot (Figure 31b) [451-454], and ripples [455-458]. Such nanoscale patterns can be achieved by not only the e-beam lithography on the graphene directly but also the fluorination [459], the metal gate electrode [460], and the substrate pre-engineering [461]. The superlattice patterned on the graphene channel can itself be interpreted as an interconnected network for current flow. In other words, the electron dynamics in the well-designed graphene superlattice can pave the way for the advanced electron quantum optics system, containing the Veselago lens [73-82], supercollimator [68-72, 83-87], Andreev-Klein reflector [98-102], and Aharonov-Bohm type or Fabry-Pérot type interferometer [103-122]. In electronic solid-state device, it is possible to avoid splitting of electron flow without any external magnetic fields and realize the localized or confined electron wave packets. Based on that, it is observable the almost perfect ballistic propagation of the electron along the selected direction [68-72, 73-102] and the coherent or damped oscillations of the electron wave packets [103-122].

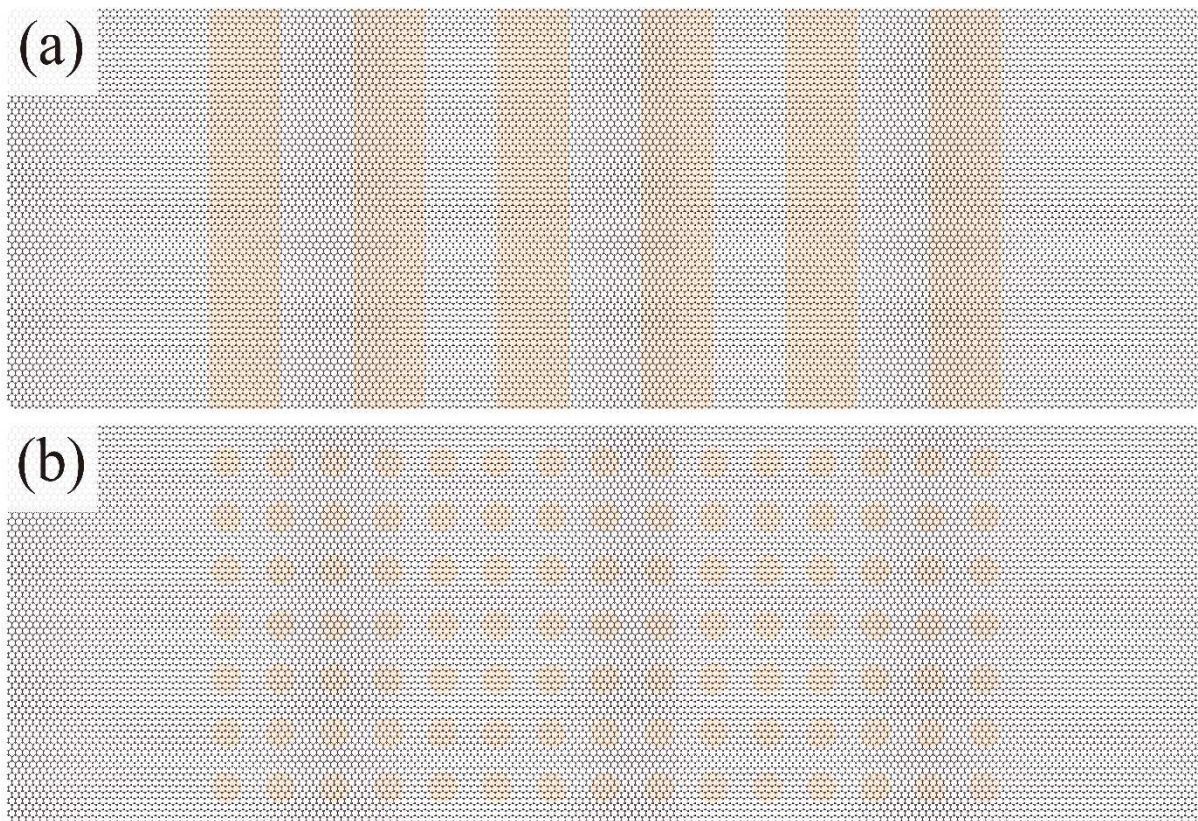


Figure 31. (a,b) Graphene superlattice patterned with the Kronnig-Penny type periodic structure (a) and nanodot (b).

2. Strong Fermi-Level Pinning Effect at Metal/Graphene/Si Junction

As explained in Chapter 1.4, the Schottky barrier formation (Chapter 1.4.1) and charge carrier transport (Chapter 1.4.4) in the metal/semiconductor junction has a crucial link with the physical and chemical phenomena at the interface [15, 340-343]. The major complexity that make it difficult to identify the underlying mechanisms of the barrier formation and carrier transport originate in defect [249-254], oxidation [255-262], material intermixing [284-298]. Many metal and semiconductor atoms take participate in the diffusion at the interface with very thin or no native oxide layer. In case of metal/Si junction, the intermixing of metal and Si atoms driven by the inter-diffusion can modulate the density and distribution of trap states on the Si surface or bring about the silicide formation [284, 285, 462-464]. Even if the Si substrate is processed with RCA cleaning procedures and hydrogen passivation [299-304], the very thin native oxide region exists. In other words, regardless of the surface treatment, the material intermixing occurs inevitably in very small areas, inducing the effective energy barrier height in the small patches much lower than that in the prevailing surrounding (Chapter 1.4.5). The isolated patches act like the leaky current paths in the spatially inhomogeneous Schottky contact [359-377]. Here, we employ the graphene interlayer and insert it at the metal/n-Si(001) interface in order to protect the interface from the material intermixing and establish the ideal junction [177].

2.1 Sample Fabrication

As shown in Figure 32, the metal/Si and metal/graphene/Si junctions sharing the same substrate can be prepared by the partial transfer of the graphene layer onto Si surface previously processed with the RCA cleaning and the hydrogen passivation [177, 299-304, 390-406]. The chemical vapor deposition (CVD) monolayer graphene grown on the Cu foil is spin-coated on the top side with a PMMA film at 5000 rpm for 60 seconds. The graphene on the bottom side should be removed by the reactive ion etching (RIE) with 10 W power for 20 seconds under 10 mTorr pressure maintained by 50 sccm O₂ flow. The Cu foil is etched with an aqueous solution of ammonium persulfate (NH₄)₂S₂O₈ for 48 hours. After etching of the Cu foil, the graphene should be rinsed in deionized water at least five times. The PMMA/graphene stack is then transferred partially on the half of the Si surface leaving the other half uncovered. The PMMA/graphene/Si sample should be dried in clean environment and baked for 15 minutes at 150 °C with blowing of N₂ gas on the sample surface. The PMMA film should be removed [390-406] with acetone more than 24 hours and rinsed with isopropyl alcohol (IPA). Here, the forming gas (H₂, N₂, and Ar) annealing method can be used to minimize the chemical residues. Next, the graphene/Si sample should be also rinsed with isopropanol and heated for 15 minutes at 200 °C again. The blowing of N₂ gas on the sample surface should be followed. The heating and blowing procedures are necessary for driving off all molecular residues including water at the graphene/Si interface and isopropanol on the graphene surface. The Raman spectrum [465-467] is measured on the graphene (Figure 33a) to analyze the intensity of the G peak (~1580 cm⁻¹) and the 2D peak (~2700 cm⁻¹), confirming the quality of the graphene layer on our Si substrate. Now, the metal electrodes are deposited through a circular-shaped shadow mask by using the e-beam evaporation. The graphene-uncovered area deposited by the metal electrode becomes the metal/Si junctions. After removing the metal-uncovered graphene by the RIE with 10 W power for 40 seconds under 10 mTorr pressure maintained by 50 sccm O₂ flow to isolate the region of metal-covered graphene, the region become the metal/graphene/Si junctions. The cross-sectional schematic view of the metal/Si and metal/graphene/Si junctions with the zoom-ins illustrating the interfaces is shown in the Figure 33b [177].

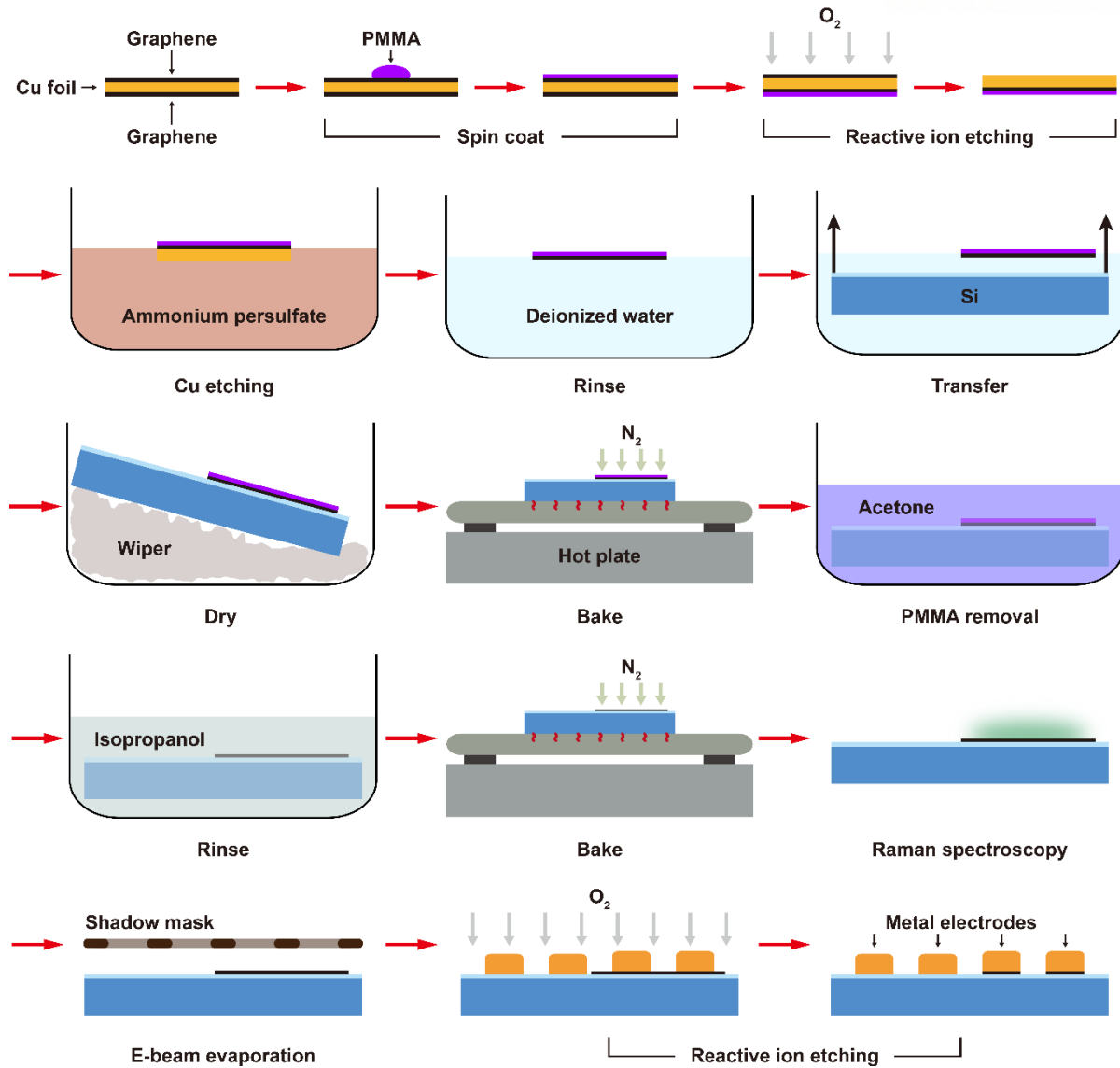


Figure 32. Sample fabrication processes [177, 299-304, 390-406].

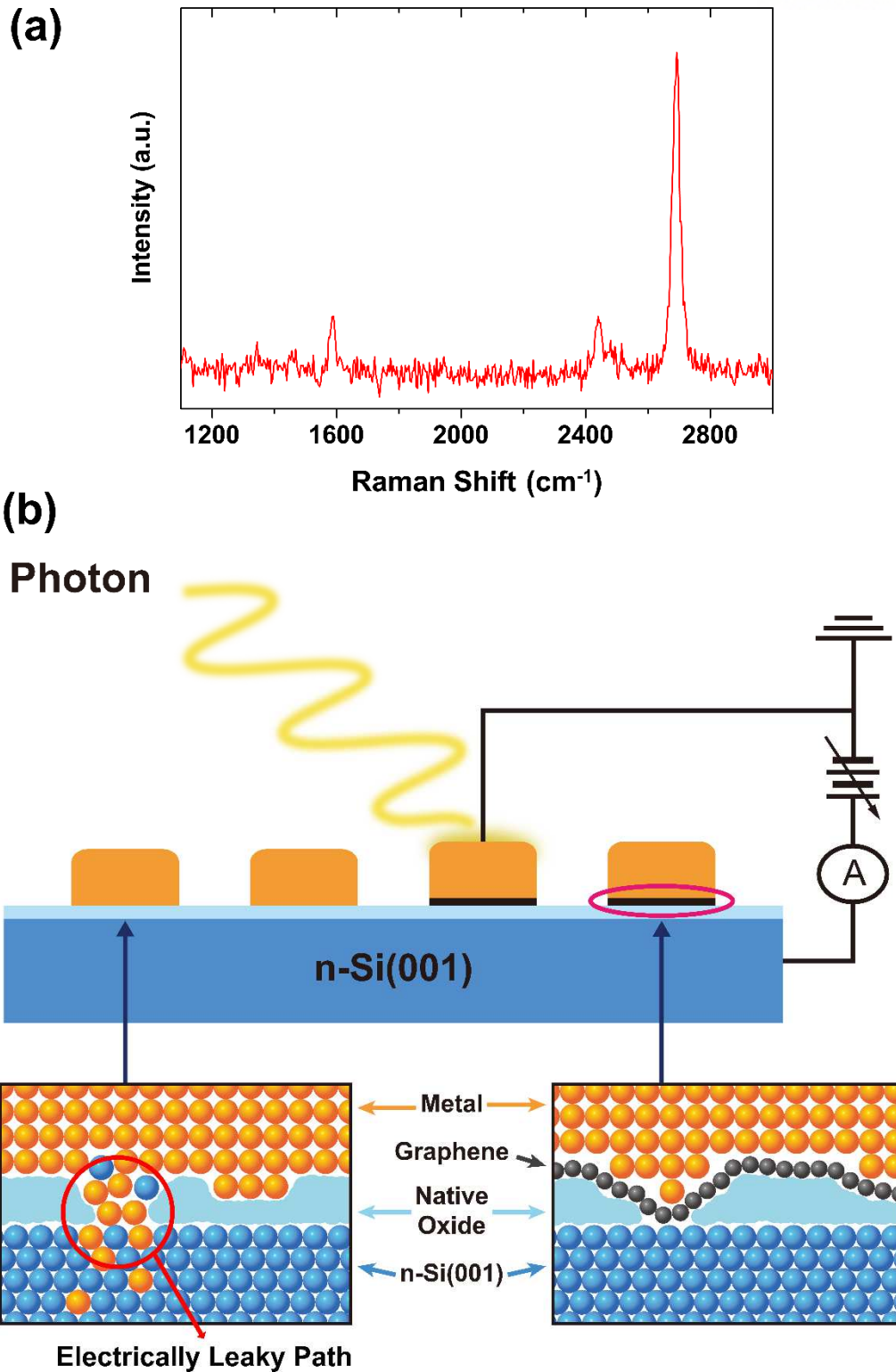


Figure 33. (a) Raman spectrum measured on the graphene [177, 465-467] (b) Cross-sectional schematic view of the metal/Si and metal/graphene/Si junctions [177]. The two zoom-ins illustrates the graphene interlayer blocks the atomic intermixing at the interfaces. The IPE measurement configuration is also included [32-34, 380-387].

2.2 Current-Voltage Measurement

Figure 34 shows the current-voltage (I-V) curves measured on the metal/Si and metal/graphene/Si junctions [15, 177, 340-358]. Interestingly, the reverse-biased leakage current of metal/graphene/Si junction is observed to be much smaller than that of metal/Si junction (Figure 34). This is easily understandable because the I-V characteristics are dominated by low barrier patches [359-377] induced by the local material intermixing (Chapter 1.4.5) and these low barrier patches are blocked by the graphene diffusion barrier [176, 177, 407-412] (Chapter 1.6.2).

The nickel silicide having low electrical resistivity is known to be formed with the diffusion of Ni atoms to the Si substrate [284, 285, 462-464]. The extracted Schottky barrier height of Ni/graphene/Si junction is found to be larger than that of Ni/Si junction (Figure 34a), indicating that the graphene interlayer blocks the nickel-silicon reaction, makes a metal/Si junction intact, and forms a uniform Schottky barrier height.

In case of Pt/Si and Pt/graphene/Si junctions, the I-V extracted Schottky barrier heights are found to be almost identical. This can be understood from the fact that the material intermixing is not so active at the Pt/Si interface relative to the Ni/Si and Ti/Si interfaces [284-298]. This implies that the associated low barrier [359-377] patches would have really small areal fraction in the Pt/Si junction, which is even unnoticeable in the forward-biased current [359-377]. The energy band profile of the small low-barrier patches is known to be pinched-off strongly by the high-barrier surrounding [187-190, 378, 379], the energy barrier height seen by the electron become almost comparable to the high-barrier surrounding for the forward bias. For the pinched-off energy band profile of a very small-size low barrier patch, the influence of the low-barrier patches on the charge carrier transport cannot be revealed by the Schottky barrier height extracted from the I-V (Figure 34b). On the other hand, these pinch-off energy band profile of the small low-barrier patches is also known to be reduced for the reverse bias [187-190, 378, 379], and the small low-barrier patches will provide the preferred paths for current flow under the reverse bias (Chapter 1.4.5). Thus, the reverse-biased leakage current of Pt/Si junction is observed to be much larger than that of Pt/graphene/Si junction (Figure 34b).

It is especially worthy of notice that the Ti/graphene/Si junction is less leaky (about 1000 times smaller) than the Ti/Si junction (Figure 34c), supporting that the graphene interlayer greatly reduces the material intermixing at the interface. The metal-silicon reaction and material intermixing at the Ti/Si interface is known to be much active than Ni/Si and Pt/Si interfaces [284, 285, 462-464]. Hence, the atomically mixed local areas of Ti/Si are much leakier compared to that of Ni/Si and Pt/Si. Even with the graphene interlayer, there will be the small areas where the graphene does not completely cover or the carbon atoms are missing. Accordingly, the I-V extracted Schottky barrier height in Figure 34c is obtained to be smaller than that in Figure 34a and Figure 34b.

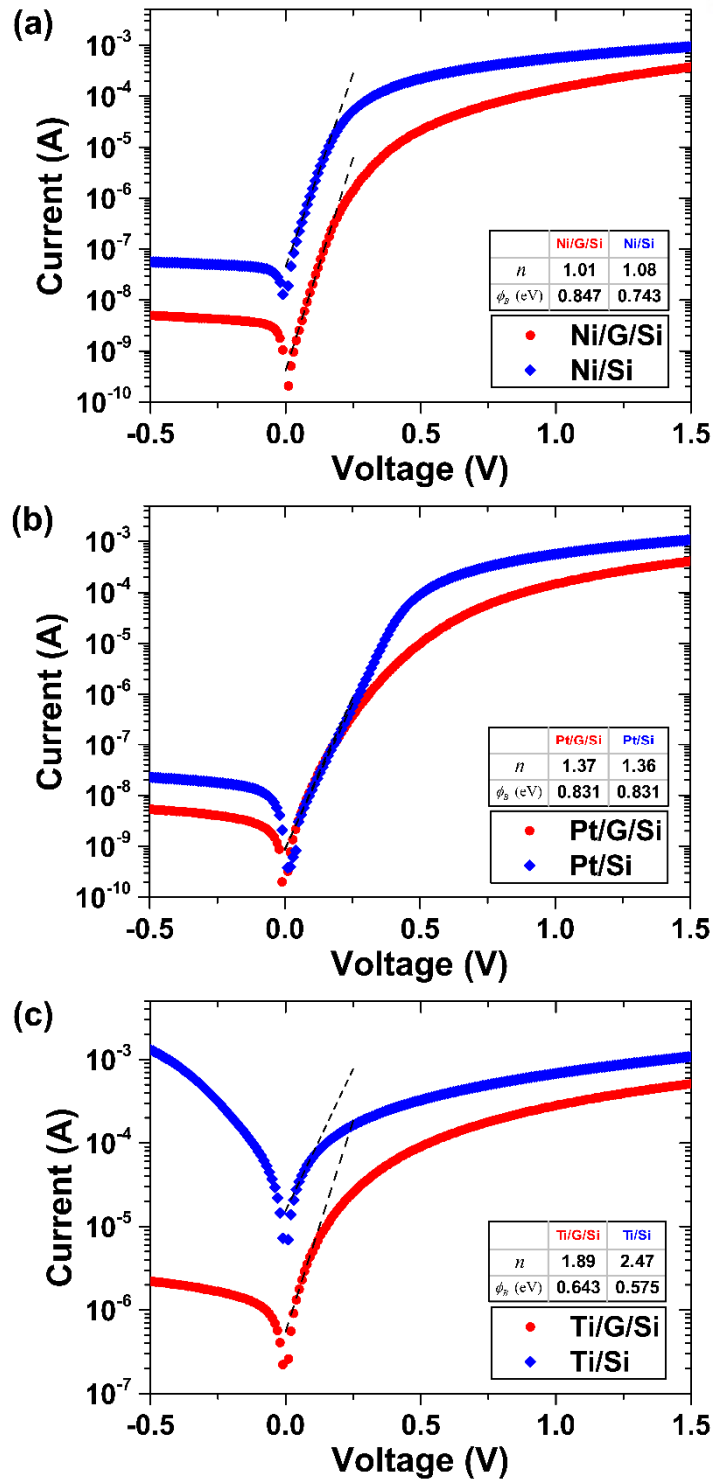


Figure 34. Current-voltage (I-V) curves on the metal/Si and metal/graphene/Si junctions for Ni, Pt and Ti electrodes [15, 177, 340-358].

2.3 Internal Photoemission Measurement

Figure 35 shows the internal photoemission (IPE) quantum yield (Chapter 1.5) [32-34, 380-387] for the metal/Si and metal/graphene/Si junctions [177]. For the Ni/Si junction without the graphene interlayer, the two thresholds are observed (Figure 35a). The additional quantum yield rise in the IPE measurements at the Ni/Si interface could be a result of the barrier lowering due to the material intermixing occurred at the weak spots. Thus, the first threshold represents the low barrier patches [359-377] isolated in the high barrier surrounding and the second threshold does the high barrier region. This two threshold behavior is not identified in the conventional I-V curve (Figure 34a) since the most of junction current flows through the small areas with their local Schottky barrier height and the I-V extracted Schottky barrier height is mainly determined by these low barrier patches [359-377]. On the other hand, our IPE results reveal the two threshold behavior of the Ni/Si junction very clearly, providing experimental evidence for the existence of low barrier patches [359-377] formed by material intermixing at the Ni/Si interface mentioned so far. On the other hand, with the graphene interlayer, one threshold is observed (Figure 35a). Compared to the Ni/Si junction, this single threshold behavior of Ni/graphene/Si junction indicates the formation of homogeneous Schottky contact which could be obtained with the graphene interlayer owing to the its role of diffusion barrier [176, 177, 407-412]. This is consistent with the smaller I-V extracted Schottky barrier height of Ni/Si junction with and without the graphene interlayer (Figure 34a).

For the both Pt/Si and Pt/graphene/Si junction (Figure 35b), the single threshold is observed. Similar to the I-V measurement (Figure 34b), the corresponding Schottky barrier heights are obtained to be almost identical, which can be understood by the inactive material intermixing at the Pt/Si interface. The area of low barrier patches [359-377] of the Pt/Si junction is expected to be so small that the photocurrent from the low barrier patches cannot be distinguishable in IPE measurements.

As confirmed in Figure 34c, the Ti/Si junction is observed to be very leaky so that the photocurrent is overwhelmed by the leakage current. Thus, the corresponding IPE quantum yield was not extracted at all. However, with the graphene interlayer, the IPE yield spectra is well specified and the single threshold is observed for the Ti/graphene/Si junction (Figure 35c).

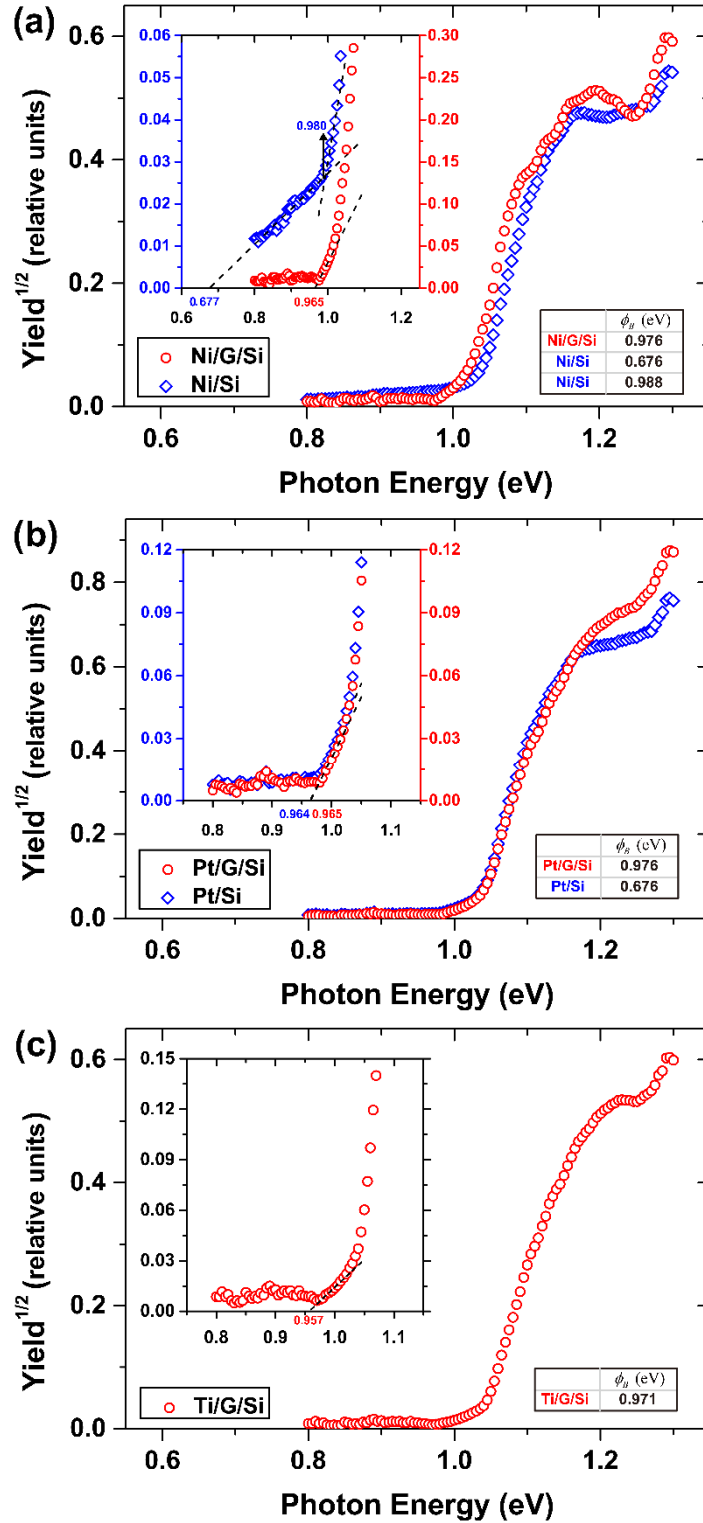


Figure 35. IPE yield as a function of photon energy on the metal/Si and metal/graphene/Si junctions for Ni, Pt and Ti electrodes [32-34, 177, 380-387]. The average Schottky barrier heights including the image force lowering are shown in the tables.

2.4 Transmission Electron Microscopy Image

Figure 36 shows the high-resolution transmission electron microscopy (HRTEM) images of Ni/Si and Ni/graphene/Si junctions. It is found that the thickness of the native oxide layer at the Ni/Si interface varies actually depending on location by examining the structural change across the interface for Figure 36a and Figure 36b taken at two different sites in the same Ni/Si junction. The native oxide layer in Figure 36b is seen to be thinner than that in Figure 36a. In particular, the SiO₂ layer of the red-circled area in Figure 36b looks particularly thin, confirming the non-uniform native oxide layer. The comprehensive analysis of these two figures leads to the following conclusion that the thickness of SiO₂ layer is spatially inhomogeneous and some areas might have pinholes with no SiO₂ layer at all. The material intermixing can occur more easily on the areas with thin SiO₂ layers or pinholes, resulting in formation of local Schottky barrier height lower than the surrounding areas with thicker SiO₂ layers. Between the Ni electrode and Si substrate, the graphene interlayer is seen clearly in Figure 36c. The inserted graphene layer carries out the role of diffusion barrier to form the homogeneous Schottky contact [176, 177, 407-412].

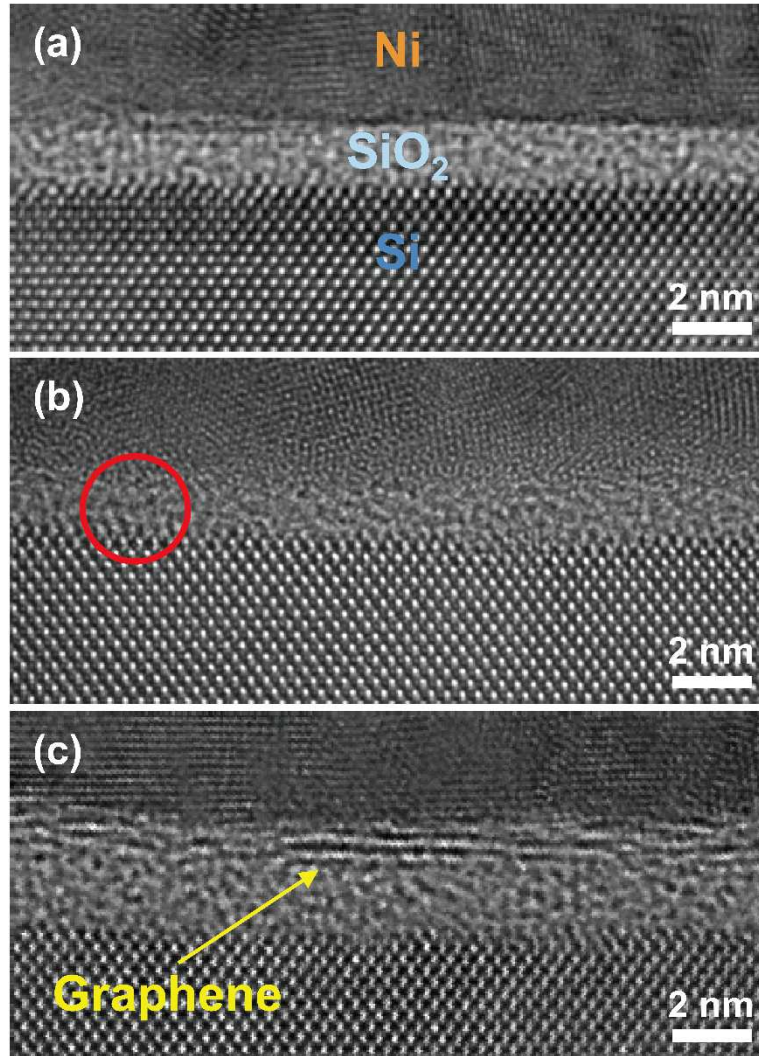


Figure 36. (a,b) Transmission electron microscopy image at two different locations in the same Ni/Si junction. (c) Transmission electron microscopy image of Ni/graphene/Si junction [177].

2.5 Parallel Conduction Model Calculation

As discussed in Chapters 2.3 and 2.4, the two-threshold behavior in the IPE measurement (Figure 35a) does not appear in the I-V measurement (Figure 34a). The I-V characteristics of the inhomogeneous Schottky contact can be influenced by the small portion of low-barrier patches [187-190, 378, 379]. Thusm the IPE measurements [32-34, 380-387] are more suitable for extracting the Schottky barrier height on the prevailing region.

From the parallel conduction model [187-190, 378, 379] the areal fraction of the low barrier patches [359-377] can be estimated (Chapter 1.4.5). For the several different areal fractions of the low barrier patches, Figure 37a shows the calculated I-V curves of the Ni/Si junction possessing the low barrier patches [359-377] surrounded by the prevailing high barrier region. The low Schottky barrier height of the low barrier patches [359-377] is assumed to be the Schottky barrier height extracted from the first IPE threshold (Figure 35a) and the high Schottky barrier height of the prevailing high barrier region is assumed to be the Schottky barrier height extracted from the second IPE threshold (Figure 35a). In order to match the effective Schottky barrier height calculated from the parallel conduction model with the Schottky barrier height extracted from the I-V curve (Figure 34a), the areal fraction of low barrier patches in the Ni/Si junction is estimated to be about 7.6 % (Figure 37b).

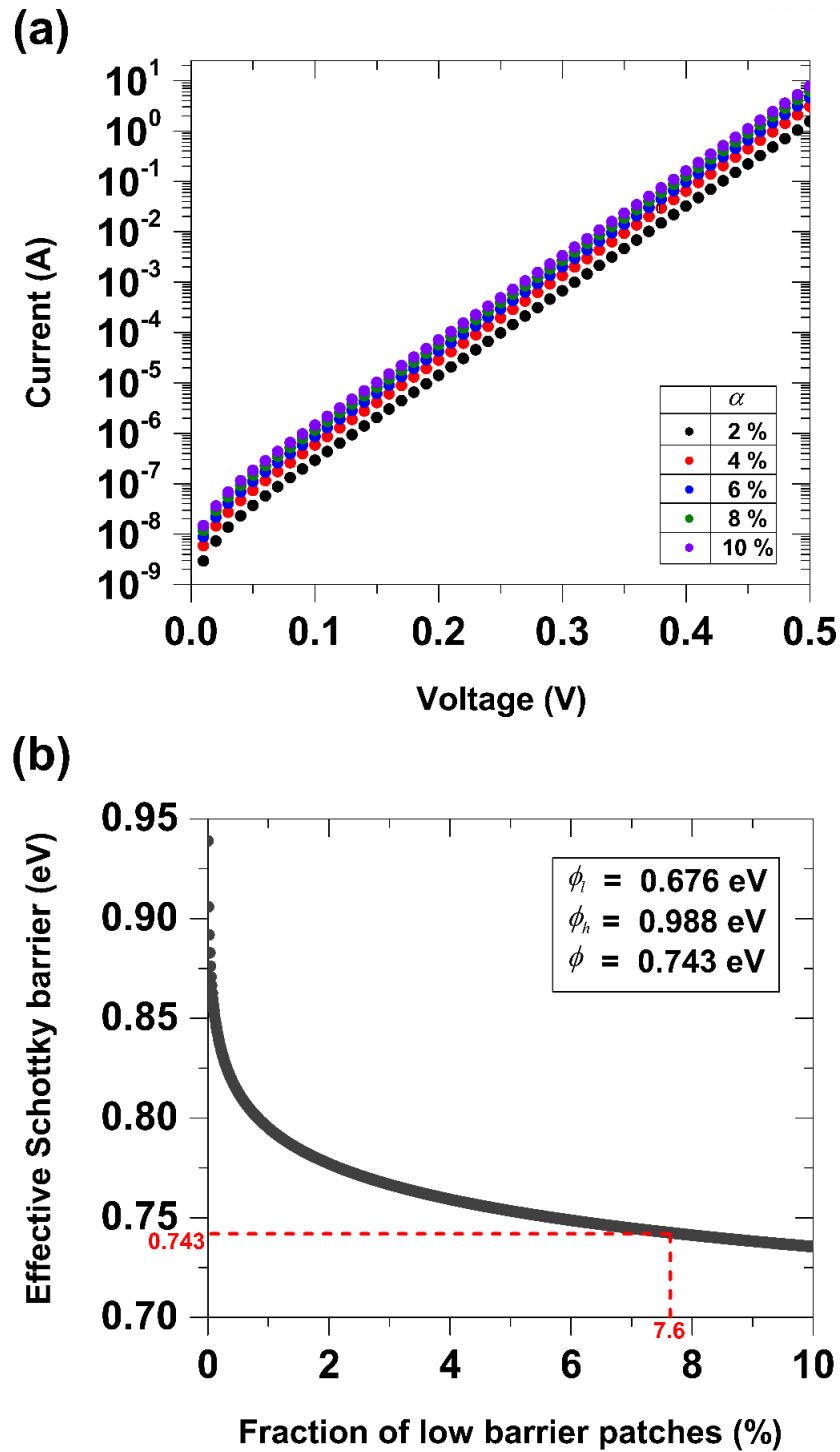


Figure 37. (a) The I-V curves of the Ni/Si junction calculated from the parallel conduction model [177, 187-190, 378, 379] for the several different areal fractions of the low barrier patches [359-377]. (b) The effective Schottky barrier height estimated from the parallel conduction model [177, 187-190, 378, 379] as a function of the areal fraction of low barrier patches.

2.6 Strong Fermi-Level Pinning Effect

As shown in the Figure 38, the Schottky barrier heights of the metal/graphene/Si junctions which are determined from the IPE measurement (Chapter 2.3) obviously show the very weak dependence on the metal work-functions. Almost independence of the Schottky barrier height for the metal work-function implies the strong Fermi-level pinning effect at the interface (Chapter 1.4.2), approaching the Bardeen limit [207-209, 225-235, 249-298]. The metal Fermi-level seems to be almost completely pinned at the charge neutrality level close to the valence band edge of Si. The charge neutrality level is found to be positioned around 0.145 eV above the valence band edge. The atomically impermeable property of the graphene interlayer suppresses the material intermixing, create an environment for studying the ballistic carrier transport across the interface, and provides an efficient platform to explore the Fermi-level pinning effect.

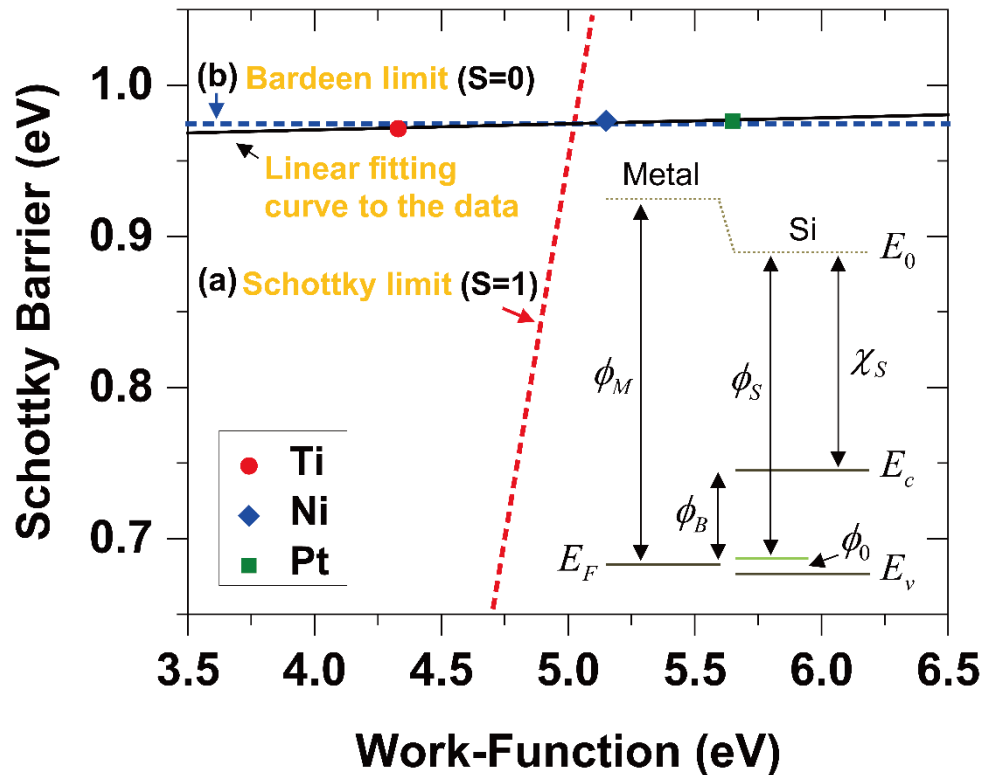


Figure 38. Schottky barrier height of the metal/graphene/Si junction extracted from the IPE measurements as a function of metal work-function [177, 191-194, 245].

2.7 Fermi-Level Pinning Effect Depending on the Junction Area

Following the trend of continuous downscaling of electronic devices, the junction area has become smaller than hundreds nm. The downscaling of electrical contacts has a huge impact on the contact resistance and is directly related to the performance degradation. In particular, with respect to the nanoscale Schottky contact, the I-V characteristics are known to be almost unaffected by the interface Fermi-level pinning effect and the effective Schottky barrier height is supposed to be greatly reduced [159-162, 468-472]. Since the influence of the electric dipole layer at the interface associated with the surface states on the semiconductor substrate is known to be drastically limited around the junction edge, the corresponding Fermi-level pinning effect can be seemingly deactivated by this edge effect [177]. The change of electrostatic potential across the electric dipole layer [15, 189, 190, 207-224] is very essential in the interface Fermi-level pinning effect (Chapter 1.4.2).

If the metal electrode is about μm in size, the area of Schottky junction is so large that the influence of interface electric dipole layer can reach deep into the semiconductor substrate and the energy band profile in the depletion region on the semiconductor side is affected entirely by the interface Fermi-level pinning (Figure 39a and Figure 39c). However, the nanoscale Schottky junction will behave as being unpinned by the influence of the junction edge even if the Fermi-level pinning effect is actually strong at the interface. Moreover, if the occupying area of electric dipole layer at the interface is too small, the influence of the interface electric dipole layer can be limited throughout the junction (Figure 39b and Figure 39d).

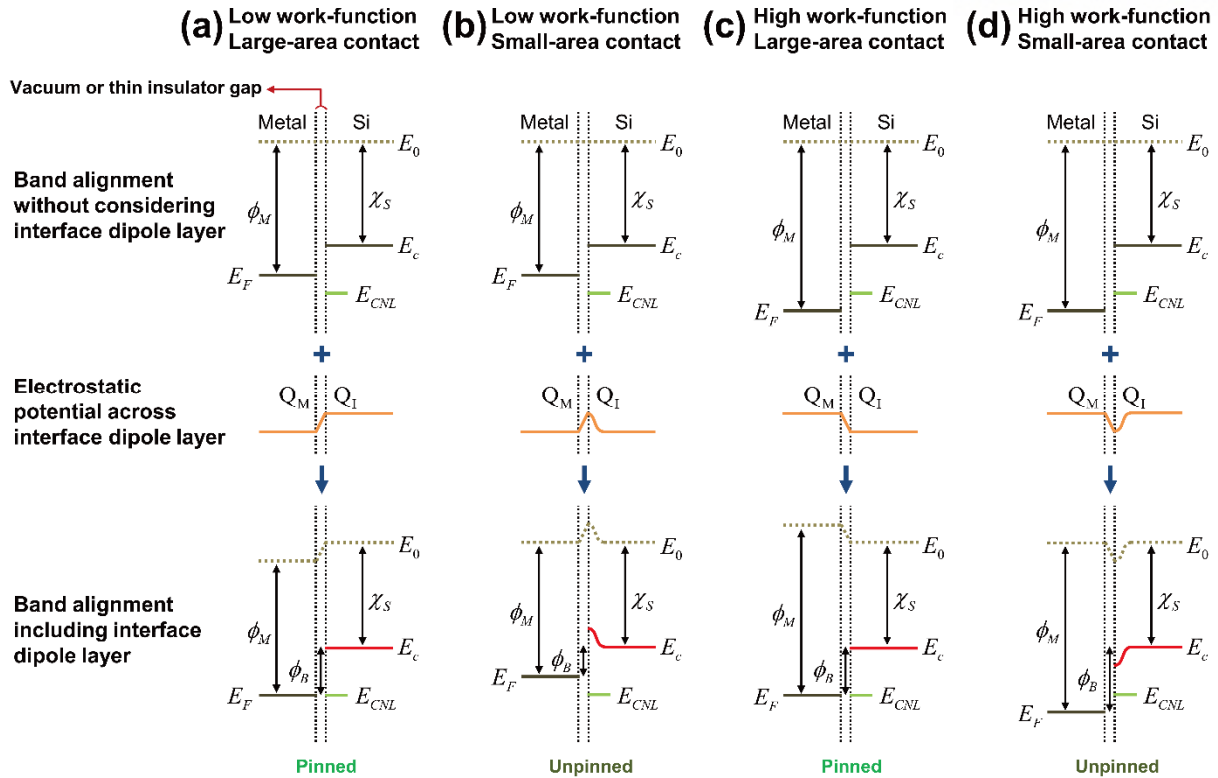


Figure 39. (a-d) Band alignment at the very near the metal/Si interface for large (a,c) and small (b,d) junction areas showing the change of electrostatic potential across interface electric dipole layer [15, 177, 189, 190, 207-224]. The influence of the interface electric dipole layer can be limited very near the interface when the area of electric dipole layer is small (b,d).

2.8 Conclusion

It is systematically demonstrated that the graphene interlayer inserted at the metal/n-Si(001) interface takes the role of a diffusion barrier (Chapter 1.6.2) [176, 177, 407-412], prevents the atomic inter-diffusion substantially ensuring the intact interface, and forms an atomically abrupt Schottky contact. This efficient method adopting the graphene interlayer as a diffusion barrier is particularly useful for protecting the junction from unwanted electrical changes and investigating the Fermi-level pinning effect. The minimized reaction is confirmed with the current–voltage measurements. Most of all, the internal photoemission measurements obviously show the strong Fermi level pinning effect at the intact metal/ Si interface ensured by the graphene interlayer blocking the atomic intermixing [177].

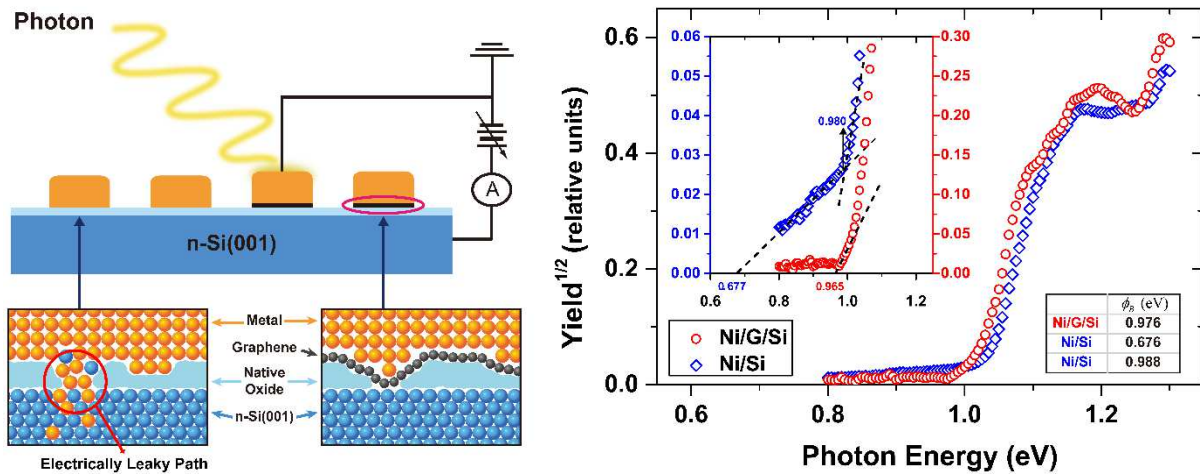


Figure 40. Summary of Chapter 2 [177].

3. Negative Fermi-Level Pinning Effect at Metal/Graphene/GaAs Junction

The previous research in Chapter 2 suggest that the graphene interlayer inserted at the metal/Si junction can be used to form an intact metal/semiconductor junction and investigate the Fermi-level pinning effect at the interface [177]. Interestingly, the graphene interlayer at the metal/GaAs junction turns out to function differently [389]. As discussed in Chapter 1.4.2, the GaAs-like III–V compound semiconductor is known to have the reconstructed surface and contain the low density of surface states [15, 225-235, 249-298, 326-339]. However, if the structure is modified by some extrinsic factors, the surface comes to have the high density of surface states. In addition, during metal deposition, the intermixing of metal, Ga, and As atoms on the low surface-state regions can induce the interface-trap states, resulting in the high trap states similarly to the regions with regular native oxide layer. Therefore, as is well known [326-339], the entire region of the metal/GaAs junction can be governed by the strong Fermi-level pinning effect. On the other hand, if the graphene interlayer is inserted at the metal/GaAs interface and prevents the atomic intermixing [176, 177, 407-412], the regions can preserve the low interface-trap states and induce the weak Fermi-level pinning effect [15, 225-235, 249-298, 326-339]. Furthermore, the Schottky barrier height of the metal/graphene/GaAs junction is found to decrease with the metal work-function increasing. The pinning factor generally ranges between 0 (Bardeen limit) [207-209] and 1 (Schottky-Mott limit) [196-197] depending on the pinning strength [225-235, 249-298] Surprisingly, the negative value of pinning factor has been extracted [389].

3.1 Sample Fabrication

The metal/GaAs junctions with and without the graphene interlayer can be fabricated by following the procedures [389]. The native oxide on the GaAs is etched in a 1:1 diluted solution of ammonia hydroxide in deionized water for 1 minutes followed by DI water rinsing [473]. In order to make ohmic contacts to the GaAs [474, 475], gold-based metals (Ti/Pt/Au, 5/20/500 nm) are deposited near the edge of GaAs substrate using the e-beam evaporation and annealed at 400 °C for 300 seconds using rapid thermal annealing (RTA). The sample is also treated in an ammonia hydroxide etching solution for 3 min followed by DI water rinsing again right before the graphene transfer [473]. As described in Figure 41, the CVD grown graphene monolayer purchased from the Graphene Supermarket is transferred on the GaAs surface. The semi-dry transfer method using thermal release tapes has been used [390-406]. The other details are explained in Chapter 2.1. After the graphene transfer, the quality of graphene on GaAs substrate is examined with the Raman spectrum measurements (Figure 42) [389, 465-467]. The circular-shaped metal electrodes of average diameter ~500 μm are then deposited by using the e-beam evaporation. The metal/GaAs junction is formed on the graphene-uncovered area. The graphene uncovered by metal electrodes is removed with the RIE to isolate each metal/graphene/GaAs junction.

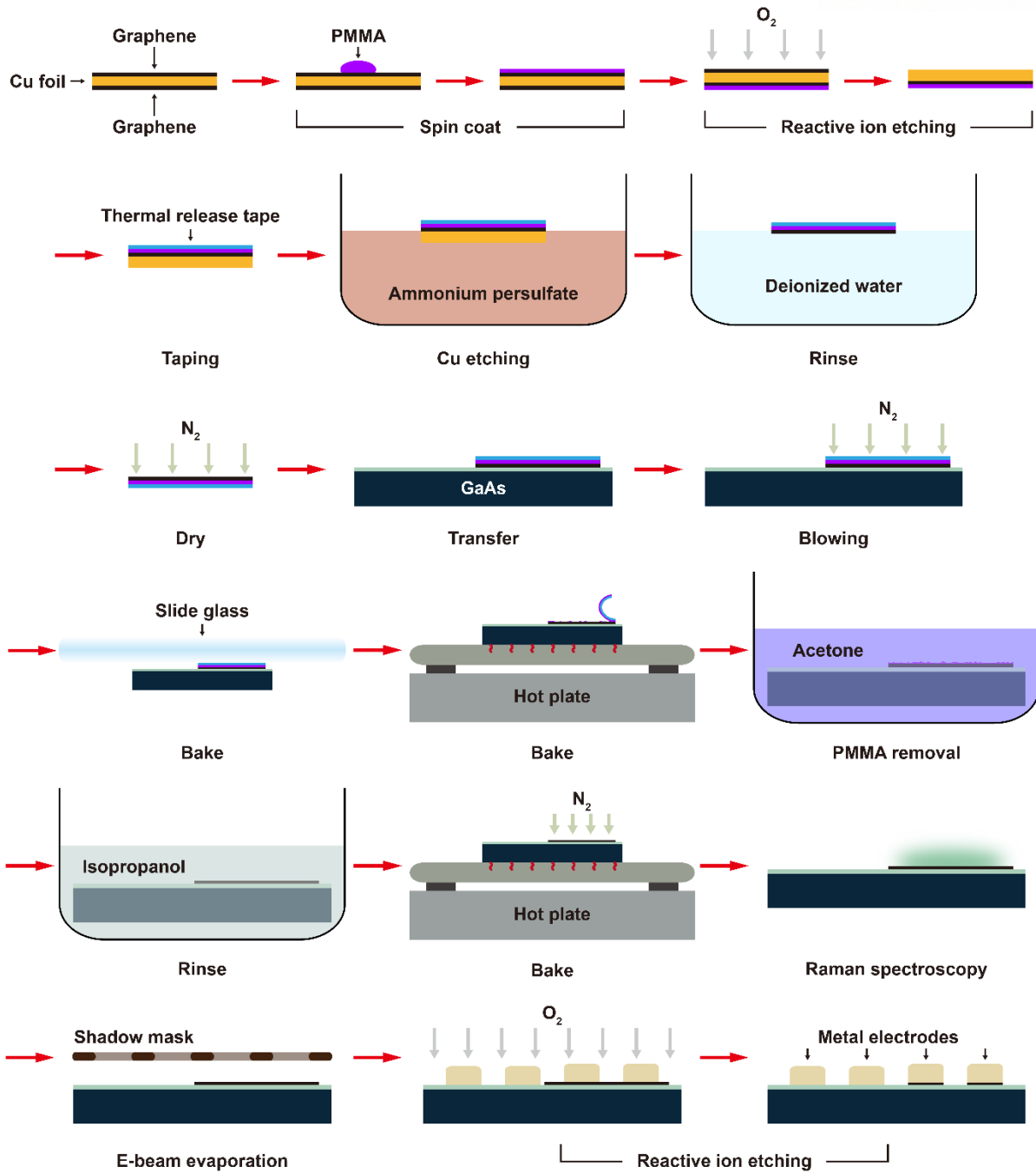


Figure 41. Sample fabrication processes [177, 299-304, 389-406].

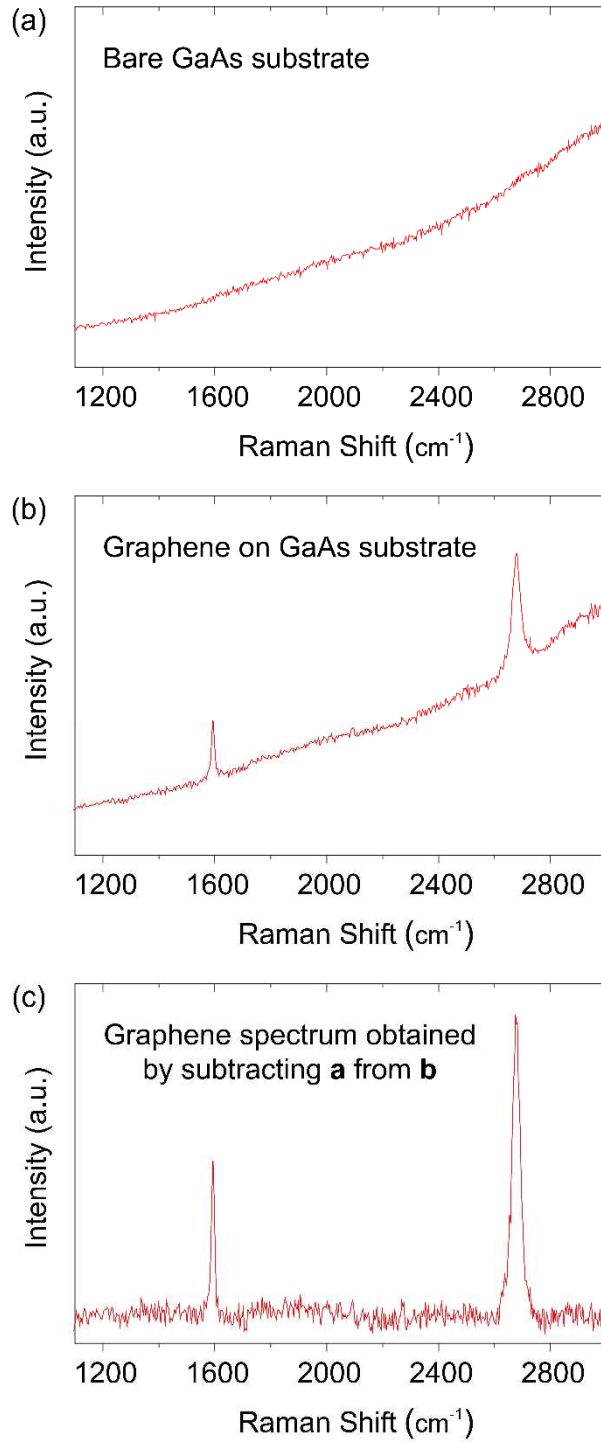


Figure 42. (a-c) Raman spectra measured on the bare GaAs substrate (a), graphene on GaAs substrate (b), and graphene with the GaAs background signal subtracted (c) [389, 465-467].

3.2 Current-Voltage Measurement

The Al/graphene/GaAs (Figure 43a) and Ti/graphene/GaAs (Figure 43b) junctions reveals the rectifying characteristics. Their reverse-biased currents are reduced than the Al/GaAs and Ti/GaAs junctions. On the other hand, the reverse-biased currents of Ni/graphene/GaAs and Pt/graphene/GaAs junctions are strikingly increased than those of Ni/GaAs and Pt/GaAs junctions (Figure 43c and Figure 43d). Moreover, it seems that the rectifying behaviors have almost disappeared. Considering the difference in work-function of metal electrodes, this result is counter-intuitive. However, with the graphene interlayer, it is found that the Schottky barrier heights of Al/graphene/GaAs and Ti/graphene/GaAs junctions are high, and that of Ni/graphene/GaAs and Pt/graphene/GaAs junctions are low. Considering the strong Fermi-level pinning effect on the prevailing GaAs surface [15, 225-235, 249-298, 326-339], it is normally expected that the I-V-extracted Schottky barrier heights of the metal/graphene/GaAs junction should have the values similar to that of the metal/GaAs junction. In other words, the conjecture that the metal-dependent variation in the I-V characteristics of the metal/graphene/GaAs junction originates from the small patches of low interface-trap density can be claimed [389].

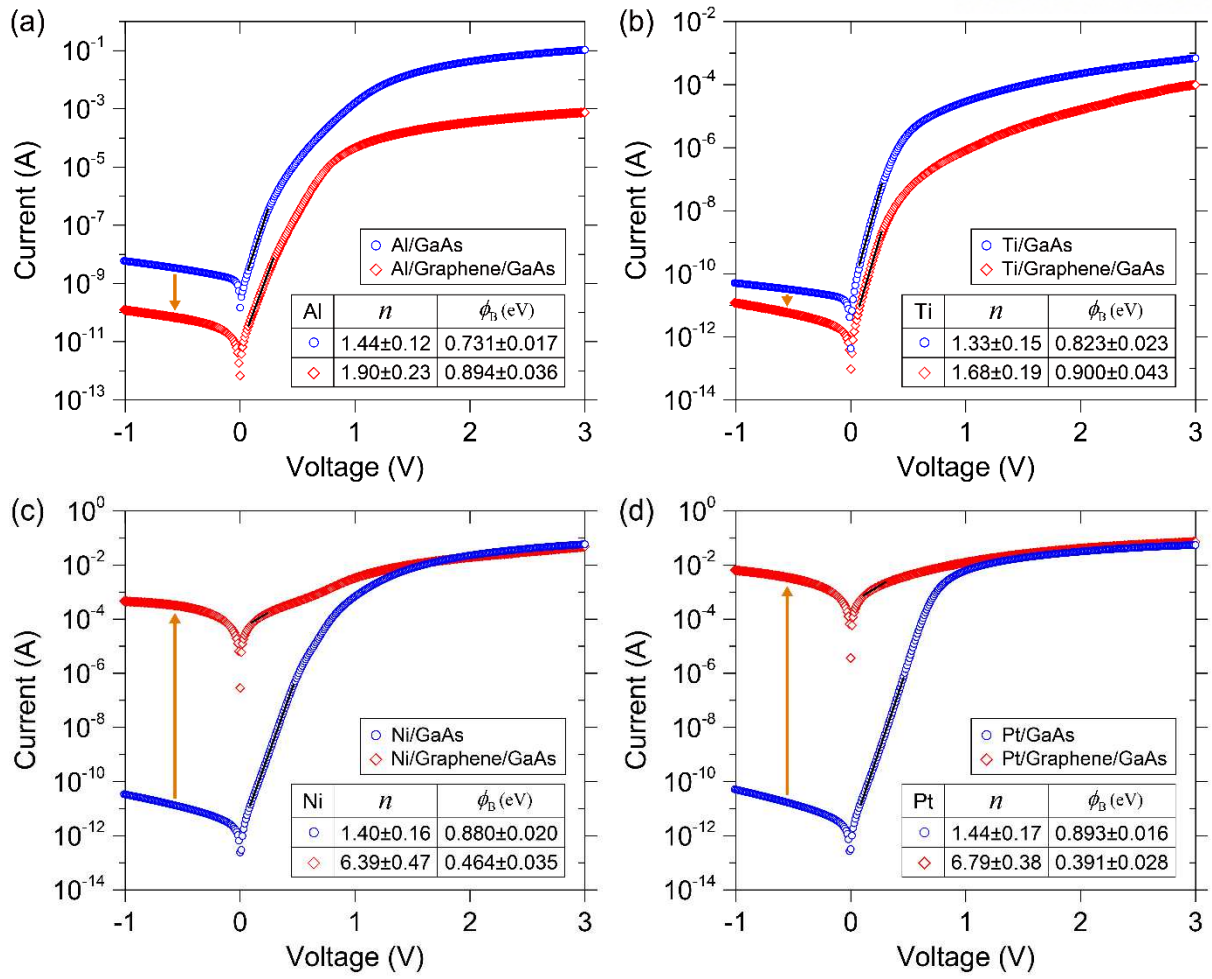


Figure 43. (a-d) I-V characteristics of metal/GaAs junctions with and without the graphene interlayer [389].

3.3 Internal Photoemission Measurement

As explained in Chapter 1.5, the IPE signals are provided by all regions in the junction. However, if the most region of junction is uniform and the region of isolated low barrier patches exists with only a small areal fraction, the IPE spectrum will be dominated by the prevailing region. In other words, the contribution from the low barrier patches will be invisible

The two thresholds of GaAs [476] are clearly observed for the conduction band minima (Γ and L valleys). Here, the first threshold reflects the electron transmission into the Γ valley and represents the commonly accepted Schottky barrier height of the metal/GaAs junction. The the second threshold corresponds to the additional transmission into the L valley. The gap between the first and second thresholds is found to be about 0.29 eV [476]. Since the first and second thresholds are extracted to be considerably identical for all four metal electrodes, it can be claimed that the Fermi-level pinning effect is strong uniformly throughout the entire metal/GaAs junction.

The two common thresholds in the IPE spectra of the metal/graphene/GaAs junctions are observed to be quite similar to those for the metal/GaAs junctions for Al, Ti, and Ni electrodes. On the other hand, for the Pt/graphene/GaAs junction, the excessive leakage current, which is already identified in the I–V characteristics (Figure 43d), overwhelmed the measured photocurrent. The corresponding IPE yield could not be determined (Figure 44d). The similarity in the IPE thresholds implies that the Fermi-level pinning effect at the metal/graphene/GaAs interface is also strong in the major region of junction bearing high interface-trap density.

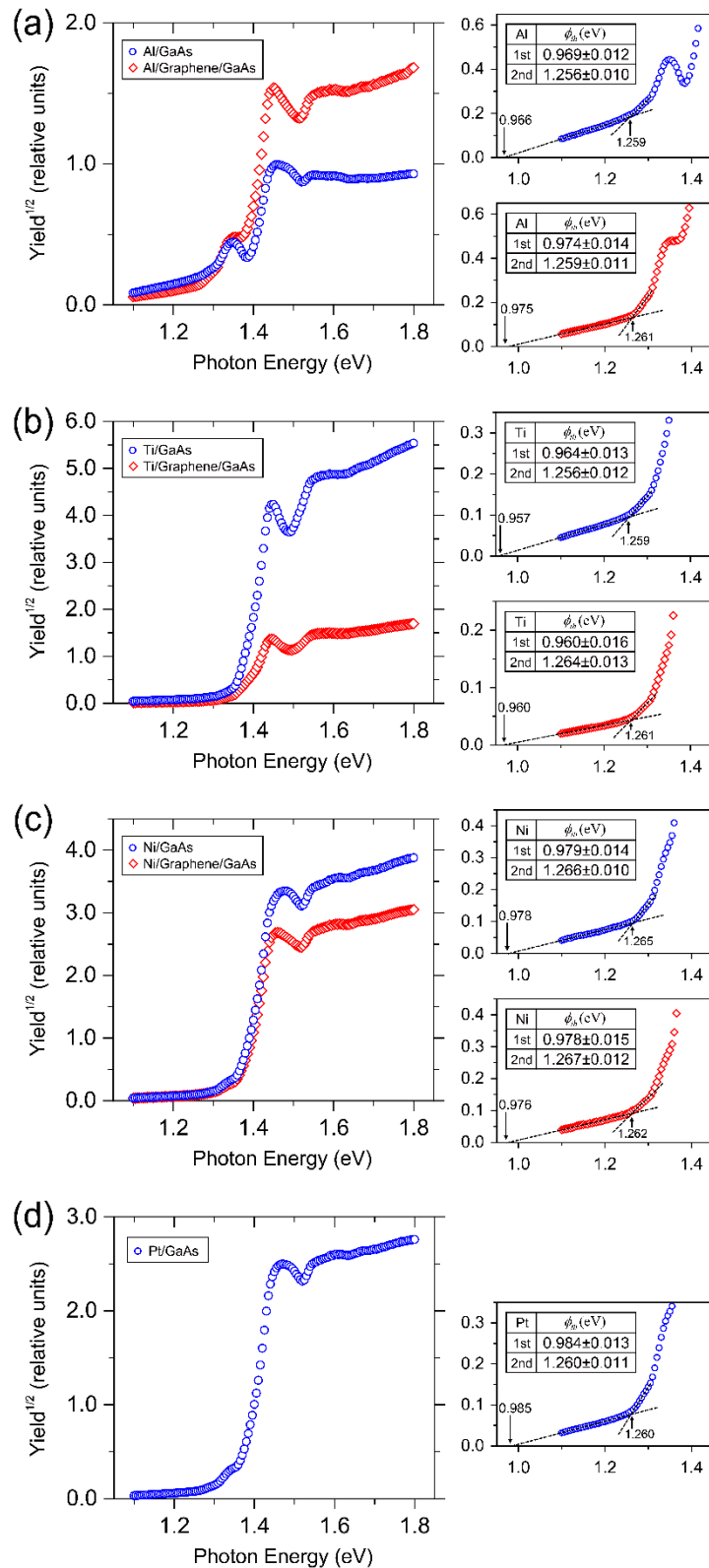


Figure 44. (a-d) IPE quantum yield spectra on the metal/GaAs junctions with and without the graphene interlayer for Al (a), Ti (b), Ni (c), and Pt (d) electrodes [389].

3.4 Direct Optical Excitation from Localized Interface States

The IPE signals will be mainly from the prevailing regions with high interface-trap density. As discussed in Chapter 3.3, the transmission into the Γ or L valleys corresponds to the first and second thresholds. However, the observation of transmission into the X valley of GaAs is interrupted by the humps of the IPE yield around 1.33 eV, which is attributed to the direct optical excitation from the localized interface states to the Γ or L valleys [388] (Chapter 1.5.1 and Figure 19b). The localized interface states expected to be positioned around the charge neutrality level and filled with electrons are responsible for the strong Fermi-level pinning at metal/GaAs junction. As shown in Figure 45, the IPE yield spectra under varying applied reverse bias characterizes how the localized interface states contribute to the IPE yield. Around the photon energy 1.33 eV, the IPE yield humps are found for all metal electrodes even if there is to some extent of metal dependence in their relative strengths. It is readily noticeable that the hump become more pronounced with the applied bias increasing. This implies that more and more electrons excited from the localized interface states can escape and transmit into the conduction band minima of GaAs with the aid of the electric field in the depletion region due to the applied bias.

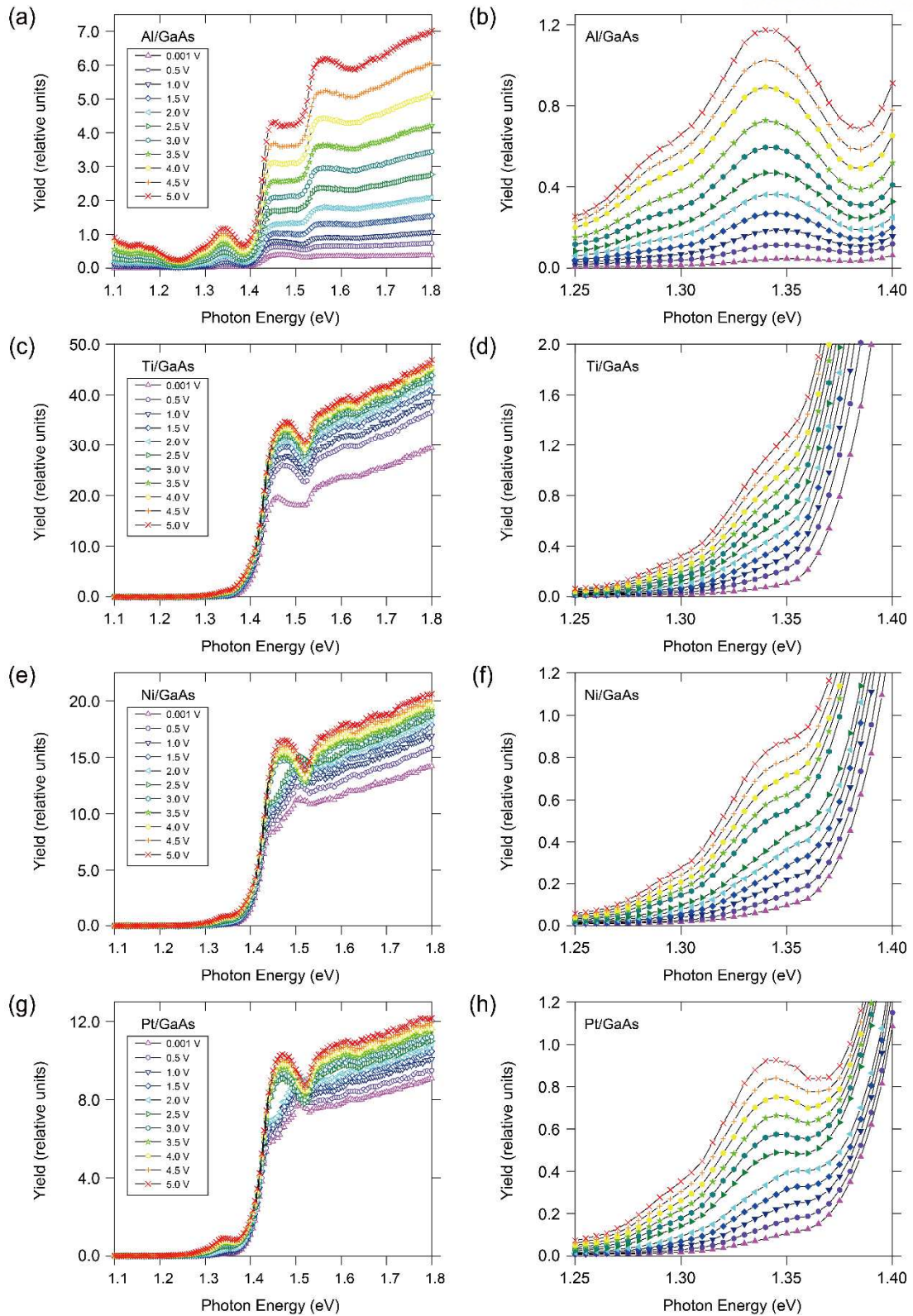


Figure 45: IPE quantum yield on the metal/GaAs junctions under applied reverse bias varying from 0.001 to 5 V [389]. The magnified views of the curves around 1.33 eV are shown in (b), (d), (f), and (h).

3.5 Transmission Electron Microscopy Image

As shown in Figure 46d, Figure 46e, and Figure 46f, the graphene interlayers inserted at the Pt/GaAs interface is seen clearly. It is also confirmed with the high-resolution transmission electron microscopy images taken on the several different sites in the Pt/GaAs (Figure 46b and Figure 46c) and Pt/graphene/GaAs (Figure 46e and Figure 46f) junctions that the thickness of native oxide layer is spatially inhomogeneous. The yellow circles in Figure 46c and Figure 46f indicate that the area of GaAs surface occupied with very thin or no native oxide layer is small. The thickness of oxide layer is estimated to be about 2.82 nm for the Pt/GaAs junction and about 2.27 nm for the Pt/graphene/GaAs junction [477]. Because the oxide layer on the graphene-covered area is passivated while the oxide layer on the graphene-uncovered area is exposed to the air before the metal electrode deposition, compared to that for Pt/graphene/GaAs junction, it is likely to have slightly thicker oxide layer for Pt/GaAs junction on the same GaAs substrate. In addition, the native GaAs oxide is reported to have very small band gap [478], the charge carrier transport across metal/GaAs junction depends significantly on whether the graphene interlayer is inserted at the interface or not, rather than the small difference in the thickness of GaAs oxide layer.

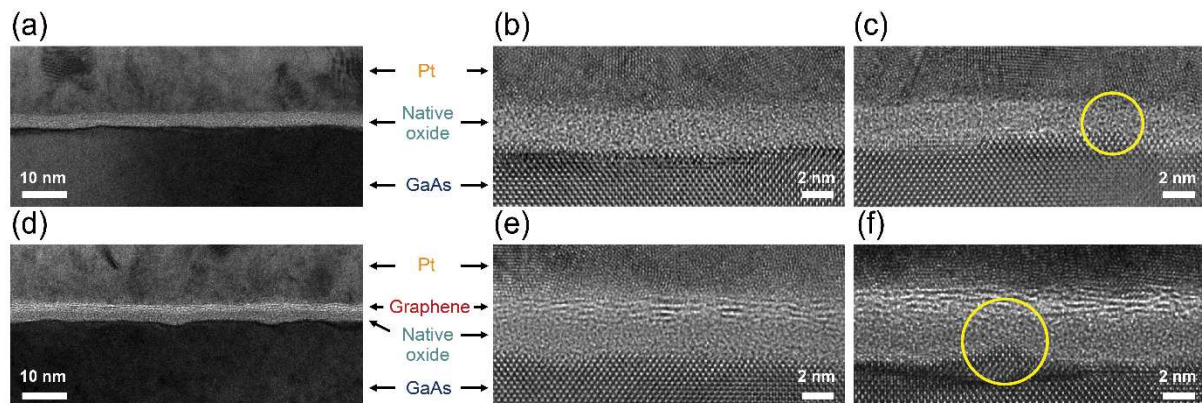


Figure 46: (a-f) Transmission electron microscopy images of Pt/GaAs (a-c) and Pt/graphene/GaAs (d-f) junctions [389]. (a,d) Bright-field images (b,c,e,f) High-resolution images. The yellow circles represent the small-size regions with very thin native oxide layer.

3.6 Negative Fermi-Level Pinning Effect

As shown in in Figure 47, the average Schottky barrier heights extracted from the measured I-V curve (Figure 43) to the thermionic emission model [15, 340-358] or the first threshold in the IPE spectra (Figure 44) with the image force lowering [32-34, 380-387] are plotted as a function of the metal work-functions. As mentioned in Chapter 3.2, for the metal/graphene/GaAs junction, the Schottky barrier height is found to be decrease as the metal work-function increases. The pinning factors are obtained to be - 0.365. In general, the pinning factor is known to range from 0 to 1. However, the pinning factor of our metal/graphene/GaAs reflects the negative value. On the other hand, in the case of IPE measurements, the Schottky barrier heights are extracted to be very similar to each other. The corresponding pinning factors approach to the 0, implying the strong Fermi-level pinning effect.

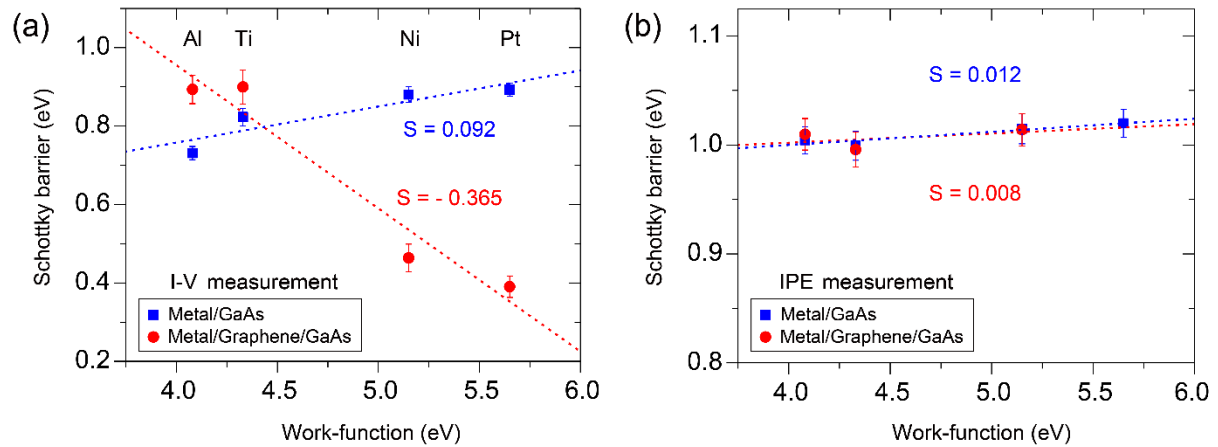


Figure 47. (a,b) I-V-extracted (a) and IPE-extracted (b) Schottky barrier heights of metal/GaAs junctions with and without the graphene interlayer as a function of metal work-function [389].

It is known that the native oxide layer on the GaAs surface consists of Ga_2O_3 , As_2O_3 , and GaAsO_3 , and its structure is considerably stable [479, 480]. In consideration of the growth mechanism of native oxide, the low interface-trap density regions are expected to be very small and randomly distributed on the surface.

Based on the result from I-V and IPE measurements, it can be claimed as shown in Figure 48a and Figure 48b that the entire region of GaAs surface for the metal/GaAs junction will have high interface-trap density [15, 225-235, 249-298, 326-339, 389, 481] due to oxidation (Figure 48a) or material intermixing (Figure 48b). In other words, the Fermi-level pinning effect will seem to be strong throughout the entire region and the current will be uniformly distributed (Figure 48e).

For the metal/graphene/GaAs junctions, as confirmed in the IPE measurement (Chapter 3.3), the prevailing region with regular native oxides will have a large density of interface-trap states (Figure 48c) and the Fermi-level pinning effect on this region will be strong similarly to the metal/GaAs junction case. Above all, the most important region is the small patches with no native oxide layer, where the low interface-trap density is maintained thanks to the protection of the graphene interlayer (Figure 48d). The observed negative Fermi-level pinning effect in the I-V measurements is expected to occur here, the small patches with no native oxide layer. According to the negative Fermi-level pinning effect, in case of the metal/graphene/GaAs junction, the low work-function metal electrodes will lead to form relatively higher Schottky barrier heights on the small patches with no native oxide layer than that on the surrounding regions. Similarly, the Schottky barrier heights on the surrounding regions with regular native oxides will have the comparably high Schottky barrier heights with the low work-function metal electrodes. Thus, the junction current will flow comparably in both the small patches and the prevailing regions (Figure 48f). On the other hand, with the high work-function metal electrodes, the small patches with no native oxide layer will form the low Schottky barrier heights just like the low barrier patches [359-377] and bear the leaky current paths [187-190, 378, 379]. Therefore, the junction current mostly flows through the small patches with no native oxide layer compared to the prevailing regions (Figure 48g).

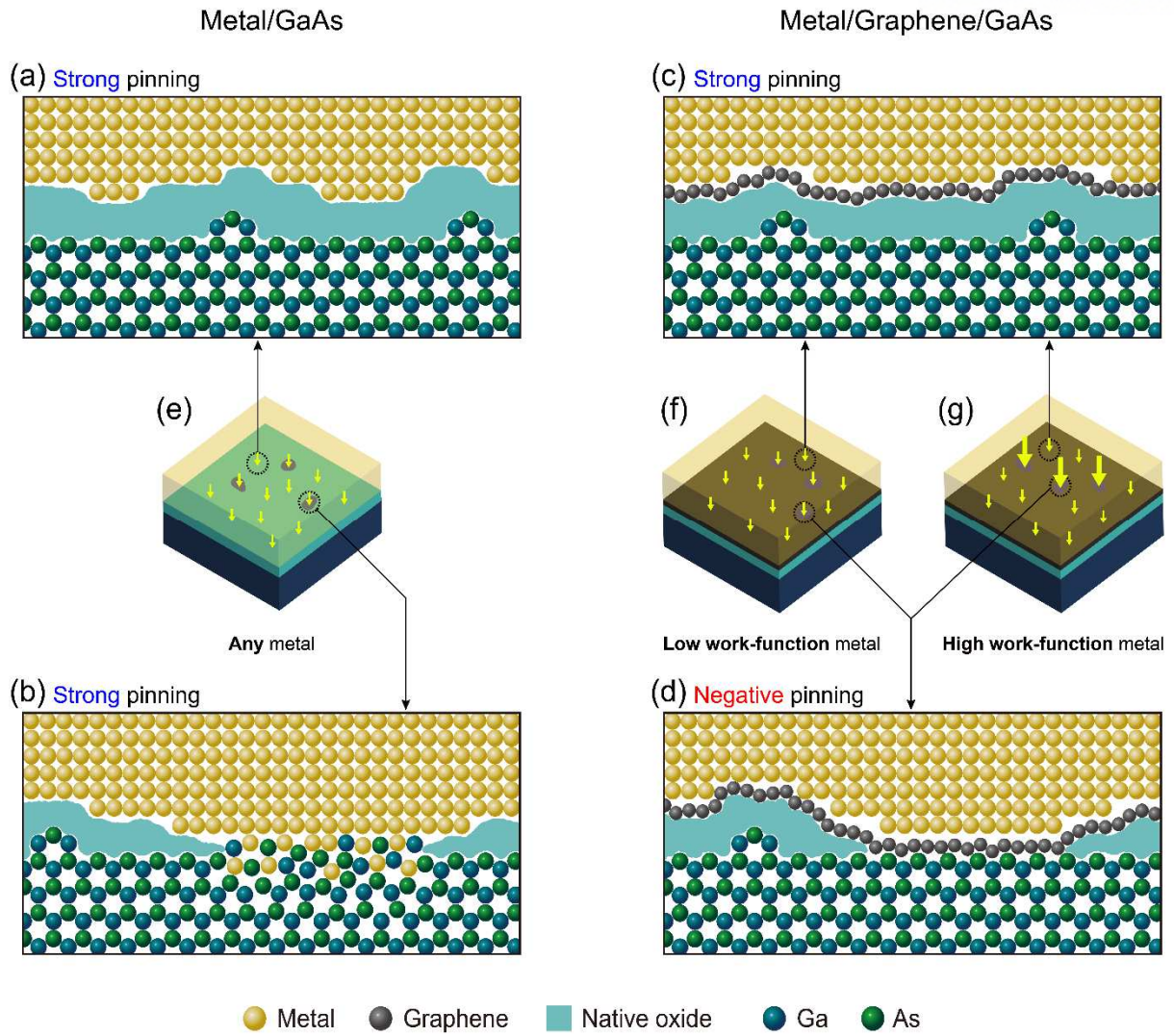


Figure 48. (a-d) Atomic arrangements at the metal/GaAs and metal/graphene/GaAs interfaces. (e-g) Schematics of metal/GaAs junctions with and without the graphene interlayer [389].

3.7 Energy Band Profile across Interface

The energy band profiles across the metal/graphene/GaAs junction for high and low interface-trap density regions is obtained [389] by performing the electrostatic modeling with the FlexPDE [482-484]. In order to explain the negative Fermi-level pinning effect, the variable of the first importance is the interaction dipole charge density Q_D [163-164], which is discussed in Chapter 1.6.1 and Chapter 1.6.3. In this modeling, as shown in Figure 49, the interaction dipole charge density Q_D indicates the charges on the graphene side, that is to say, the positive sign of Q_D signifies the positive charges on the graphene and negative charges on the metal, vice versa. It is necessary to verify whether the observed negative Fermi-level pinning effect can occur without the interaction dipole layer so that the Schottky barrier height ϕ_B and pinning strength S for various interface-trap densities D_{it} on the GaAs surface are calculated by assuming $Q_D = 0$. As shown in Figure 50a, if the interaction dipole charge density is not considered $Q_D = 0$, the pinning strength is always calculated to be positive in the typical range for III-V compound semiconductors [389, 485]. If the interaction dipole charge density Q_D is estimated arbitrarily to match with the I-V-extracted ϕ_B for $D_{it} \geq 10^{13} \text{ eV}^{-1}\text{cm}^{-2}$, as shown in Figure 50b, the Q_D is found to increase dramatically and have the physically impossible values [225-235, 249-298, 326-339, 389, 481]. As compared with the IPE measurements (Figure 44), this confirms that the negative Fermi-level pinning effect should occur on the low interface-trap density ($D_{it} \leq 10^{13} \text{ eV}^{-1}\text{cm}^{-2}$) regions, which is also consistent with our conjecture discussed in Chapter 3.6. Since it is expected that the interaction dipole layer uniformly formed throughout the entire contact, each metal should be assumed to have a certain constant Q_D in the metal/graphene/GaAs junction regardless of the locally varying interface-trap density D_{it} on the GaAs surface. Here, the interaction dipole charge densities Q_D are obtained for the low interface-trap density $D_{it} = 5 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ (fitting the I-V measured ϕ_B) and the high interface-trap density $D_{it} = 5 \times 10^{14} \text{ eV}^{-1}\text{cm}^{-2}$ (assumed to be the high interface-trap density on the prevailing region). The calculated relevant potentials and charges are listed in Figure 50c. In order to visualize these parameters, the band profiles across the Al/graphene/GaAs and Pt/graphene/GaAs interfaces are shown in Figure 51, following the form discussed in Chapter 1.6.3 and Figure 29.

The following is a detailed description of the finite element electrostatic modeling [389]. The electrostatic potential drop $U(x)$ from the vacuum level is given by the solving the Poisson's equation $\nabla^2 U(x) = -\frac{\rho(x)}{\epsilon_0 \epsilon_r}$, where x is real coordinate perpendicular to the metal/graphene/GaAs junction, $\rho(x)$ is the net charge density, ϵ_0 is the permittivity of vacuum, and ϵ_r is the dielectric constant for the GaAs substrate [486]. As shown in Figure 49, it is defined that x is zero at the metal surface, the vacuum gap between metal surface and graphene layer in $0 < x < d$, the graphene layer at $x = d$, the vacuum gap between the graphene layer and the GaAs substrate in $d < x < 2d$, and the GaAs substrate in $2d < x < X$. According to the Gauss' law, the net charge density $\rho(x)$ across the metal/graphene/GaAs junction would be zero. The charge density is zero ($\rho(x) = 0$) in the vacuum gaps at metal/graphene ($0 < x < d$) or graphene/GaAs ($d < x < 2d$) contact (Figure 49). The charge density $\rho(x)$ can be written as $\rho(x) = -q[N_D - n(x)]$ in the GaAs substrate, where q is the electronic charge, $N_D = 5 \times 10^{16} \text{ cm}^{-3}$ is the doping concentration of the n-GaAs substrate, and $n(x) = N_C \exp\left(-\frac{E_C(x) - E_F(x)}{k_B T}\right)$ is the concentration of free electron in the GaAs substrate, $N_C = 4.7 \times 10^{17} \text{ cm}^{-3}$ is the effective density of states in the conduction band of the GaAs, $E_C(x) = \phi_M - \chi_S - qU(x)$ is the conduction band edge of the GaAs substrate, EF is the Fermi-level, k_B is the Boltzmann constant, T is the absolute temperature, $k_B T$ is the thermal energy (approximately 0.026 eV), ϕ_M is the metal work-function, and $\chi_S = 4.07 \text{ eV}$ is the electron affinity of the GaAs [15, 486]. Now, we can think of the thin charge sheets Q_M , Q_G , and Q_{SS} are located at $x = 0$, $x = d$, and $x = 2d$ [15, 163, 164, 189, 190, 207-224, 389, 487], where Q_M is the surface free charge density on the metal surface, $Q_G = \frac{q\Delta E_F |\Delta E_F|}{\pi \hbar^2 v_F^2}$ is the doping charge density of graphene, $Q_{SS} = -qD_{it}(E_g - E_{CNL} - \phi_B)$ is the interface-trap charge density on the GaAs surface, $\Delta E_F = \phi_M - \phi_G - qU(d)$ is the Fermi-level shift in the graphene, \hbar is the reduced Planck constant, $v_F = 10^6 \text{ m/s}$ is the Fermi velocity of graphene, $\phi_G = 1.5 \text{ eV}$ is the graphene work-function, D_{it} is the interface-trap density on the GaAs surface, $E_g = 1.424 \text{ eV}$ is the band gap of the GaAs, E_{CNL} is the charge neutrality level of the GaAs, and $\phi_B = \phi_M - \chi_S - qU(2d)$ is the Schottky barrier

height of the metal/graphene/GaAs junction [15, 163, 164, 189, 190, 207-224, 389, 487]. Here, the sign of ΔE_F is determined by the charge carrier type of the graphene ($\Delta E_F > 0$ for p-type graphene and $\Delta E_F < 0$ for n-type graphene). Two opposite sign of interaction dipole charges Q_D are assumed to be located at $x=0$ and $x=d$. The boundary conditions are assigned as $U(0) = 0$,

$$U(2d + X) = \phi_M - \chi_S - k_B T \ln\left(\frac{N_C}{N_D}\right), \quad \lim_{\varepsilon \rightarrow 0} \int_{d-\varepsilon}^{d+\varepsilon} \rho(x) dx = Q_G + Q_D, \quad \lim_{\varepsilon \rightarrow 0} \int_{2d-\varepsilon}^{2d+\varepsilon} \rho(x) dx = Q_{SS}. \quad \text{The}$$

voltage drop $\Delta_{MG} = \frac{Q_G - Q_D}{C}$ across the metal/graphene interface and the voltage drop

$$\Delta_{GS} = -\frac{Q_{SS} + Q_{SC}}{C} \quad \text{across the graphene/GaAs interface can be also obtained from the modeling [15,$$

163, 164, 189, 190, 207-224, 389, 487], where $C = \frac{\varepsilon_0}{d}$ is the capacitance of vacuum gap per unit

area, $Q_{SC} = \sqrt{2\varepsilon_0\varepsilon_r N_D (\phi_{bi} - k_B T)}$ is the space charge density in GaAs, and

$$\phi_{bi} = \phi_B - k_B T \ln\left(\frac{N_C}{N_D}\right) \quad \text{is the built-in potential energy.}$$

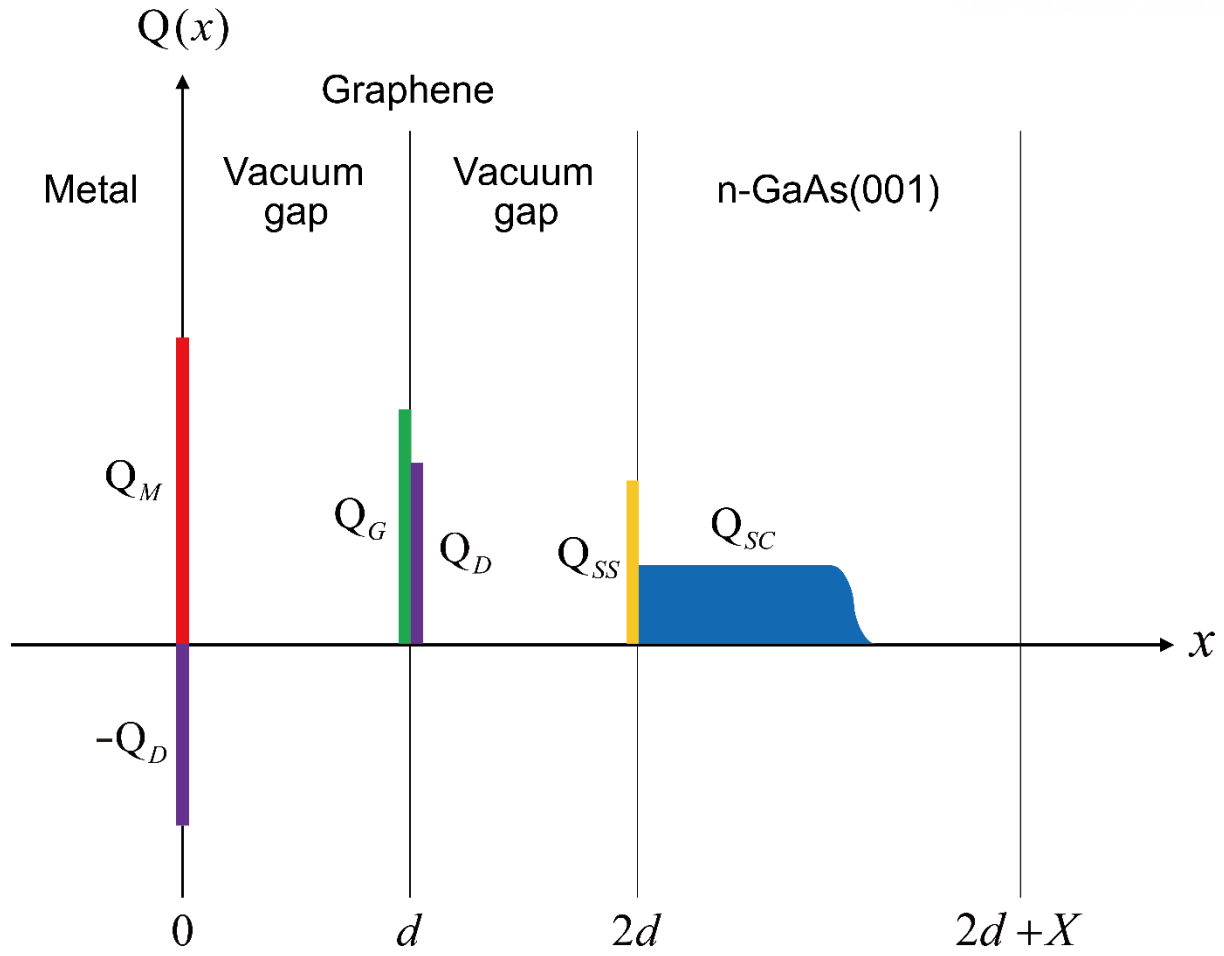


Figure 49. Charge distribution across the metal/graphene/GaAs junction [389], where Q_M is the metal surface charge density, Q_D is the interaction dipole charge, Q_G is the doping charge density of the graphene, Q_{SS} is the interface-trap charge density, Q_{SC} is the space charge density in the depletion region, d is the thickness of the vacuum gap, and X is the thickness of the GaAs substrate.

(a)

D_{it} ($\text{eV}^{-1}\cdot\text{cm}^{-2}$)		0	1×10^{12}	5×10^{12}	1×10^{13}	5×10^{13}	1×10^{14}	5×10^{14}	1×10^{15}
Calculated ϕ_B (eV) (assuming $Q_D = 0$)	Al	0.187	0.229	0.356	0.459	0.704	0.766	0.826	0.834
	Ti	0.283	0.322	0.442	0.535	0.738	0.784	0.829	0.836
	Ni	0.681	0.691	0.722	0.746	0.805	0.821	0.937	0.840
	Pt	0.808	0.810	0.816	0.821	0.834	0.838	0.841	0.842
S		0.412	0.384	0.301	0.234	0.082	0.045	0.010	0.005

(b)

D_{it} ($\text{eV}^{-1}\cdot\text{cm}^{-2}$)		0	1×10^{12}	5×10^{12}	1×10^{13}	5×10^{13}	1×10^{14}	5×10^{14}	1×10^{15}
Estimated Q_D ($10^{-6}\text{ C}\cdot\text{cm}^{-2}$) (to fit with the I-V measured ϕ_B)	Al	-5.87	-5.92	-6.13	-6.39	-8.62	-11.84	-54.48	-149.98
	Ti	-5.23	-5.29	-5.52	-5.81	-8.35	-12.05	-62.69	-178.49
	Ni	1.60	1.74	2.27	3.09	18.61	60.31	1286.07	5048.71
	Pt	3.35	3.51	4.29	5.58	28.57	89.08	1843.13	7210.81

(c)

Metal	Al		Ti		Ni		Pt	
ϕ_M (eV)	4.08		4.33		5.15		5.65	
Q_D ($10^{-6}\text{ C}\cdot\text{cm}^{-2}$)	-6.13		-5.52		2.27		4.29	
D_{it} ($\text{eV}^{-1}\cdot\text{cm}^{-2}$)	5×10^{12}	5×10^{14}	5×10^{12}	5×10^{14}	5×10^{12}	5×10^{14}	5×10^{12}	5×10^{14}
E_{CML} (eV)	0.582	0.413	0.582	0.413	0.582	0.413	0.582	0.413
ϕ_B (eV)	0.895	1.008	0.901	1.008	0.465	0.995	0.392	0.993
ΔE_F (eV)	0.521	0.539	0.529	0.546	-0.039	0.167	-0.135	0.106
Δ_{MG} (V)	0.941	0.959	0.699	0.716	-0.689	-0.483	-1.285	-1.044
Δ_{GS} (V)	-0.056	0.039	-0.058	0.032	0.074	0.398	0.097	0.456
Q_M ($10^{-6}\text{ C}\cdot\text{cm}^{-2}$)	-3.364	-3.306	-3.467	-3.412	0.234	0.848	0.498	1.215
Q_G ($10^{-6}\text{ C}\cdot\text{cm}^{-2}$)	3.197	3.424	3.295	3.511	-0.018	0.328	-0.216	0.133
Q_{SS} ($10^{-6}\text{ C}\cdot\text{cm}^{-2}$)	0.042	-0.251	0.047	-0.231	-0.302	-1.308	-0.361	-1.480
Q_{SC} ($10^{-6}\text{ C}\cdot\text{cm}^{-2}$)	0.125	0.133	0.125	0.133	0.087	0.132	0.079	0.132

Figure 50. (a) Schottky barrier height ϕ_B and pinning strength S by assuming $Q_D = 0$ and varying D_{it} for the metal/graphene/GaAs junctions. (b) Estimated Q_D to match with the I-V-extracted ϕ_B by varying D_{it} for the metal/graphene/GaAs junctions. (c) Calculated relevant potentials and charges for the metal/graphene/GaAs junctions [191-194, 389].

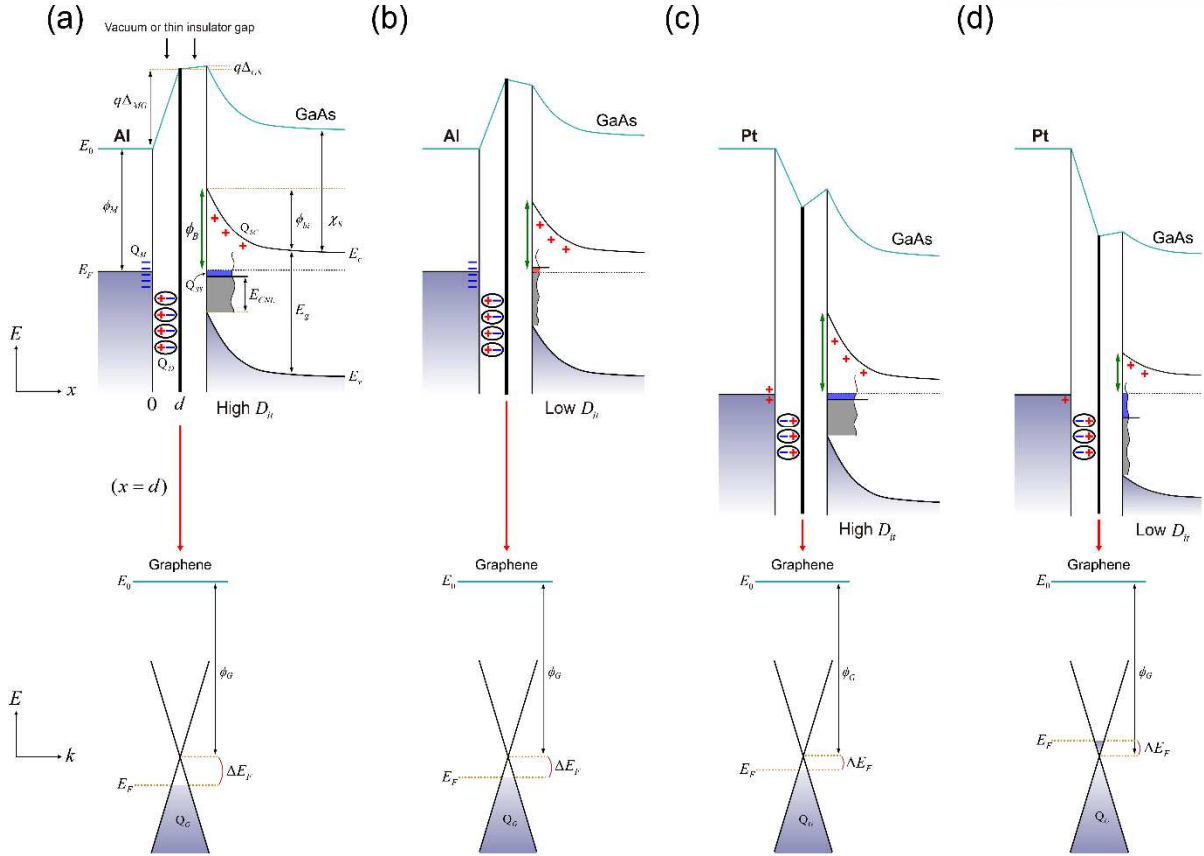


Figure 51. Energy band alignments of metal/graphene/n-GaAs junctions for the high (a,c) and low (b,d) interface-trap densities regions, where ϕ_B is the Schottky barrier height, ϕ_M is the work-function of the metal, ϕ_G is the work-function of the graphene, ϕ_{bi} is the built-in potential energy, E_F is the Fermi-level, ΔE_F is the Fermi-level shift in the graphene, E_0 is the vacuum level, E_c is the conduction band edge in the semiconductor, E_v is the valence band edge in the semiconductor, E_{CNL} is the charge neutrality level of the semiconductor, E_g is the band gap of the semiconductor, Δ_{MG} is the potential energy change across the metal/graphene interface, Δ_{GS} is the potential energy change across the graphene/semiconductor interface, Q_M is the charge density on the metal surface, Q_D is the interaction dipole charge density, Q_G is the doping charge density of the graphene, Q_{SS} is the interface-trap charge density, Q_{SC} is the space charge density in the depletion region, d is the Van der Waals gap distance between the graphene and the metal. D_{it} is the interface-trap density on the semiconductor surface, and χ_S is the electron affinity of the semiconductor [389].

3.8 Electronegativity Difference and Interaction Dipole Charge

Based on the the finite element electrostatic modeling (Chapter 3.7), the Schottky barrier heights ϕ_B are calculated for four different combinations of the interaction dipole charge density Q_D and the interface-trap density D_{it} . As shown in Figure 52a, the negative value of pinning factor for the metal/graphene/GaAs junction is found to be obtained only with $Q_D \neq 0$ for the low interface-trap density D_{it} . For the Pt/graphene/GaAs junction, it is also found that Q_D must have positive sign to obtain the measured small value of Schottky barrier height ϕ_B . In fact, this polarity coincides with the DFT calculation results [163-164] discussed in Chapter 1.6.1. However, the polarity of Q_D for the Al/graphene/GaAs junction is found to be negative in order to match with the measured Schottky barrier height. According to the DFT calculations [163-164], the polarity of Q_D for the Al/graphene interface should be positive and its magnitude is much smaller than that of Pt/graphene interface. Considering the electrostatic potential drops across the gap between the metal and the graphene, the positive sign of Q_D is expected to always lower the Schottky barrier height of metal/graphene/n-semiconductor junction, relative to the metal/ n-semiconductor junction without the graphene interlayer. However, as seen in Figure 52a, the Schottky barrier height of Al/graphene/GaAs junction on the low interface-trap density regions is obtained to be quite low with $Q_D = 0$ or $Q_D > 0$ (blue circle in Figure 52a). In other words, it is necessary for $Q_D < 0$ in order to match the experimentally measured large Schottky barrier height (red square in Figure 52a).

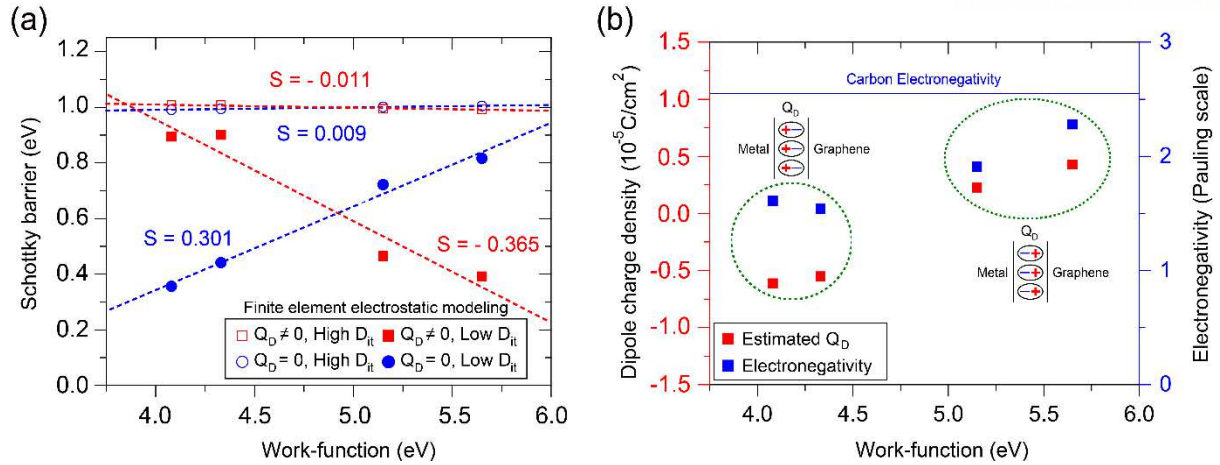


Figure 52. (a) Calculated Schottky barrier height ϕ_B of metal/graphene/GaAs junction from the finite element electrostatic modeling as a function of the metal work-function [191-194] for the low interface-trap density $D_{it} = 5 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ and the high interface-trap density $D_{it} = 5 \times 10^{14} \text{ eV}^{-1} \text{ cm}^{-2}$. The interaction dipole charge densities Q_D are chosen to be zero or the values obtained in the Figure 50c. (b) Calculated Q_D from the finite element electrostatic modeling and conventional values of the metal atom electronegativity [488] as a function of the metal work-function [191-194]. Two circles indicate two groups categorized with the opposite polarities of interaction dipole charge Q_D [389].

Figure 6b shows the calculated Q_D and the metal atom electronegativity [488] as a function of metal work-function [191-194]. The exchange correlation potential for electrons is known to be attractive to the metal surface, that is, the metal attracts the electrons on the metal surface [163-164, 489]. And the atomic electronegativity values of all the metals are seen to be smaller than that of carbon. Thus, the interacting electrons can be attracted more toward the graphene side, inducing the $Q_D > 0$.

Now, the question is how the $Q_D < 0$ of Al/graphene/GaAs junction is possible. Here, we can think of the electronegativity difference between the metal and the carbon atom. Compared to carbon, the atomic electronegativities of Al and Ti is quite smaller than that of Ni and Pt (Figure 6b). Thus, the attracting direction of interacting electrons can be shifted toward the graphene side so as to reverse the direction of the exchange correlation force, leading to the $Q_D < 0$. As the Ni and Pt have the high work-functions, the difference of electronegativity value from the carbon is seen to be smaller than the Al and Ti (Figure 6b). Thus, considering this exchange correlation, it is expected that the interacting electrons of Ni and Pt are shifted toward the metal, resulting in the $Q_D > 0$.

3.9 Parallel Conduction Model Calculation

Our Ni/graphene/GaAs junction [389] reveals the low Schottky barrier height estimated from the I-V measurements (Figure 43c) and the high Schottky barrier height (1.020 eV) on the prevailing region identified from the IPE measurements (Figure 44c), indicating that this junction is quite suitable for employing the parallel conduction model [187-190, 378, 379] for the thermionic emission [15, 340-348] through an inhomogeneous Schottky contact. It is expected that the Schottky barrier height of the low barrier patches [359-377] would be lower than the I-V extracted Schottky barrier height, two different cases of 0.4 eV and 0.3 eV are considered to estimate the areal fraction of low barrier patch. The I-V extracted Schottky barrier height (0.464eV) should be the effective Schottky barrier height of the inhomogeneous Ni/graphene/GaAs junction consisting of high and low Schottky barrier heights. Figure 53a and Figure 53b show the I-V curves of Ni/graphene/GaAs junction and Figure 53c and Figure 53d provide the estimated effective Schottky barrier height of the junction as a function of the areal fraction of low-barrier small patches (Chapter 1.4.5). According to the parallel conduction model calculation [187-190, 378, 379], it is estimated the low barrier portion would be about 8.15 % and 0.18 % for 0.4 eV and 0.3 eV, respectively. Here, the estimated areal fraction 0.18 % for 0.3 eV is really small. Moreover, this low-barrier fraction might be even smaller since the actual could be lower than 0.3 eV. This result implies that the low-barrier region of Ni/graphene/GaAs junction with no native oxide layer [illustrated in Figure 48d and Figure 51d] indeed occupies a very small areal fraction. This is believed to be the reason why it is quite difficult to locate any of the small patches by using the cross-sectional high-resolution transmission electron microscopy images (Chapter 3.5 and Figure 46). Furthermore, The ratio of current flowing through the low barrier patches to that flowing through the high barrier region is obtained to be about 2.19×10^9 in order to produce the measured I-V curve correctly [389]. Thus, it is claimed that the entire junction can become so leaky [359-377]. This is also consistent with our interpretation (Chapter 3.6) claiming that most of the junction current flows through those low-barrier patches in the actual I-V measurements. With this parallel conduction model [187-190, 378, 379], it is reasonably explainable how the small patches affect the I-V characteristics of the entire junction even with its areal fraction being very low.

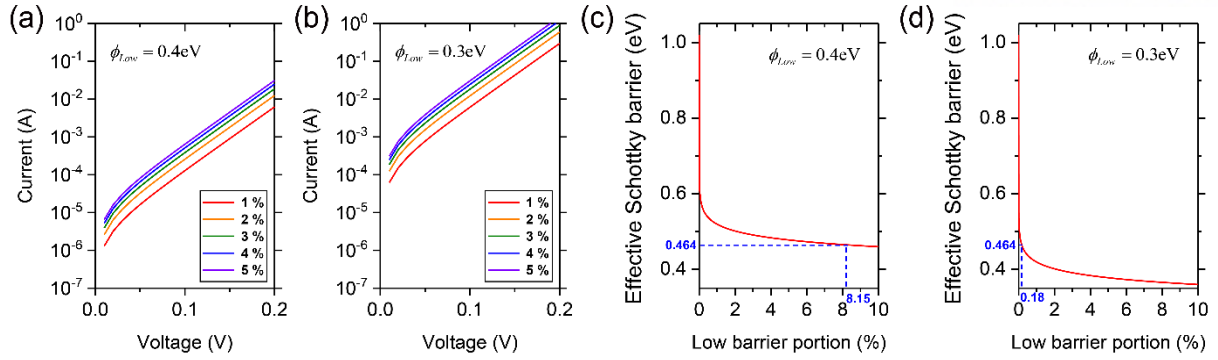


Figure 53. Parallel conduction model calculation for the Ni/graphene/GaAs junction. (a,c) I-V curves of the Ni/graphene/GaAs junction for several different low-barrier portion. (c,d) Effective Schottky barrier height of Ni/graphene/GaAs junction as a function of low-barrier portion. The blue dashed line shows the estimation of low-barrier portion to match the calculated effective Schottky barrier with the Schottky barrier height extracted from the I-V measurements. The low barrier is assumed to be 0.4 eV (a,c) and 0.3 eV (b,d) respectively. The high barrier High of prevailing region is 1.020 eV for (a)-(d), which is assumed to be identical to the Schottky barrier extracted from the IPE measurements.

3.10 Conclusion

It is experimentally observed that the negative Fermi-level pinning effect occurs on the region of GaAs surface with low interface-trap density in the metal/graphene/n-GaAs(001) junction [389], resulting from the electric dipole layer formed at the metal/graphene contact [163-164] due to the overlapping of electron wave-functions. This unusual negative Fermi-level pinning effect [389] can be understood with the interaction dipole charge at the metal/graphene contact [163-164]. In order to explain the observed negative pinning factor, the interacting electrons at the metal/graphene interface should be attracted more toward the graphene side for low work-function metals, bearing the increase of electrostatic potential across the interface. For high work-function metals, the interacting electrons should be attracted more toward the metal side, making the electrostatic potential decrease across the interface accordingly. The change of electrostatic potential across the metal/graphene interface signifies the modulation of effective metal work-function. The low interface-trap density regions, protected by the graphene interlayer, are found to have the local Schottky barrier affected directly by the interaction dipole layer at the metal/graphene contact. It is also discussed that the polarity of interaction dipole layer, indicating the position of interacting electrons, is likely to be determined by the interplay of exchange repulsion and electronegativity difference between metal and carbon atoms [389]. Based on this work, it can be claimed that the graphene interlayer can invert the effective metal work-function very efficiently and suggest the new of forming Schottky and Ohmic-like contacts simultaneously with the identical (particularly high work-function) metal electrodes on a GaAs-like semiconductor substrate possessing low surface-state density or the other 2D Van der Waals semiconducting materials [9].

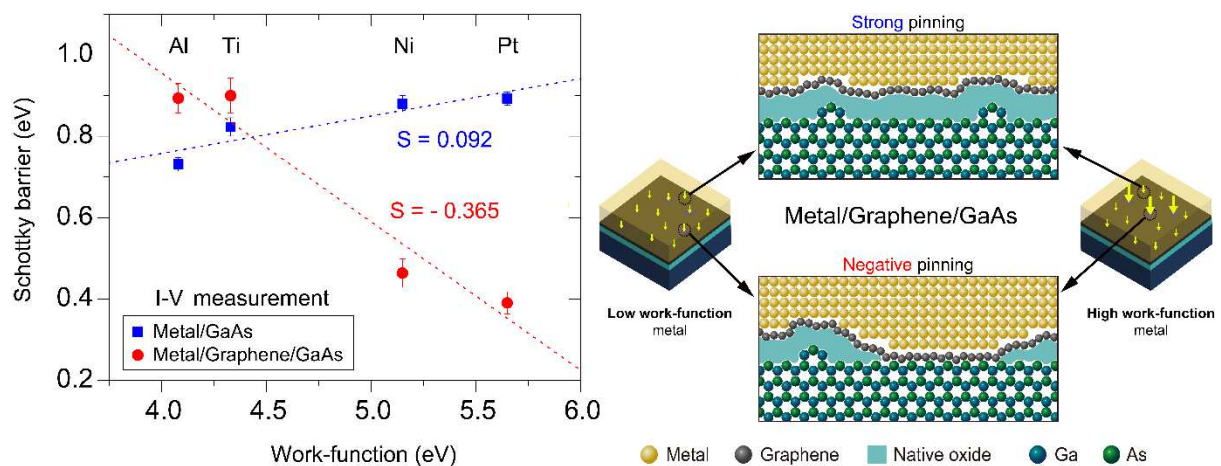


Figure 54. Summary of Chapter 3 [389].

4. Recombination Enabling Low Temperature Rectification at Graphene/Si Junction

The graphene/semiconductor Schottky diode has been extensively explored for device applications [151-154, 490-510], exhibiting not only a rectifying behavior but also a broad spectral range of photo-detection. In particular, the graphene/semiconductor contact is engineered to deeply understand the physics occurring at the interface, and enhance the electrical [151-154, 490, 492, 493, 495, 497-499, 502, 509, 510] or [491, 494, 496, 500, 501, 503-508, 511] optical properties. It is also reported that the reverse-biased current in the graphene/semiconductor junction is not saturated due to both the image force barrier lowering (Chapter 1.4.3) and the graphene doping enhanced barrier lowering [495, 498, 499]. The doping enhanced barrier lowering effect [495, 498, 499] relies on the fact the transferred CVD graphene is inevitably p-doped [512]. Meanwhile, the recent studies [499, 502] suggest that the non-ideal I-V characteristics is mainly attributed to the recombination [354-358] in addition to the interface-trap states and the barrier inhomogeneity [187-190, 210-213, 378, 379]. Although the metallic contaminant introduced on the graphene layer is expected to be the source of recombination [499, 502], it is also considered that the diffusion of hole carriers directly supplied from the p-type graphene into the semiconductor depletion layer leads to the increase of recombination current. Here, the graphene field-effect-transistor gated with Si depletion layer is fabricated to investigate the charge carrier transport mechanism across the graphene/Si junction and verify the doping type of graphene layer at the same time. The temperature-dependent I-V measurements provide the important clue in clarifying the non-ideal current source in the small forward-bias regime.

4.1 Sample Fabrication

The graphene field-effect-transistor gated with the Si depletion layer without the SiO₂ insulating layer can be fabricated with the following step. First, the n-type Si substrate is processed with the RCA cleaning [299-304, 390-406]. The 30-nm-thick Al₂O₃ insulating layer is then deposited on the Si surface using the atomic layer deposition (ALD). The stripe-shaped trench pattern is made with the conventional UV photolithography and the patterned region is etched with the buffered HF (BOE). The metal electrodes (Ti/Au, 5/50 nm) are deposited on the Al₂O₃ layer through a shadow mask by using the e-beam evaporation. The exposed Si surface is treated again with the RCA cleaning and the hydrogen passivation [299-304, 390-406]. The CVD grown graphene monolayer is then transferred on the whole surface of the sample [390-406] (Chapter 2.1). After transferring the graphene, the quality is examined with the Raman spectrum measurements (Figure 55) [465-467]. The rectangular-shaped graphene channel connecting the metal electrodes is patterned with the e-beam lithography and the RIE etching. As shown in Figure 56, the graphene channel between the metal electrodes is contacted to the Si surface and gated with not the common SiO₂ insulating layer but the Si depletion layer.

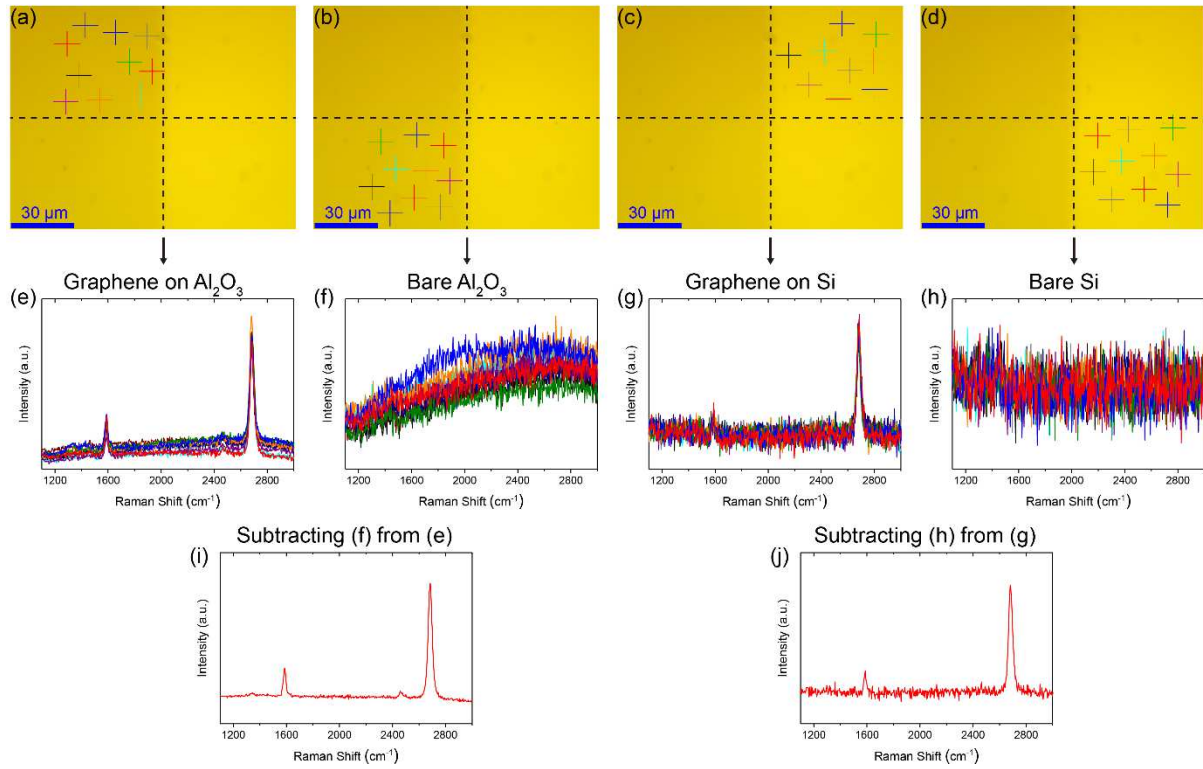


Figure 55. (a-d) Optical microscope image with the position indicator taken on the graphene on Al_2O_3 (a), the bare Al_2O_3 (b), the graphene on Si (c), and the Bare Si (d). (e-h) Raman spectra measured on the corresponding region [465-467]. (i) Raman spectrum of graphene with the Al_2O_3 background signal subtracted. (j) Raman spectrum of graphene with the Si background signal subtracted.

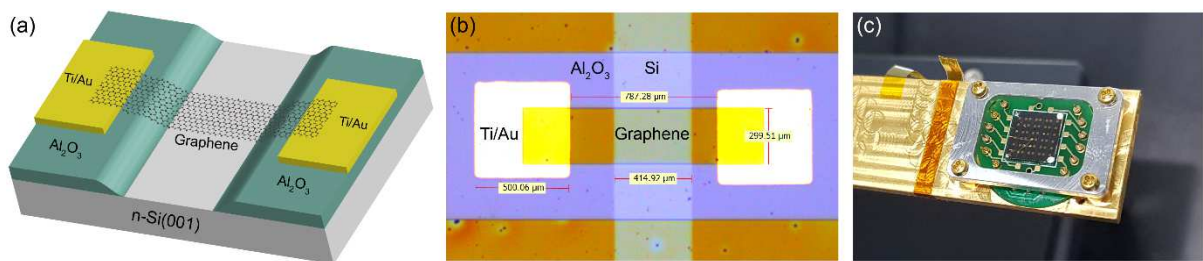


Figure 56. (a) Schematic illustration of device structure. (b) Optical microscope image taken on the graphene channel. (c) Device mounted on the cryogenic temperature measurement system.

4.2 Temperature-Dependent Current-Voltage Measurement

As shown in Figure 57, by varying the temperature, the current-voltage measurement is performed on the graphene field-effect-transistor gated with the Si depletion layer to characterize the transport properties across the graphene channel or the graphene/Si interface.

Averaged over several different samples, the series resistance R_{DS} between the two electrodes at the zero gate voltage is estimated about 7.84 k Ω (Figure 57a and Figure 57d), which will be the sum of the graphene channel resistance R_{CH} and the Ti/graphene contact resistance $2R_{CO} = \frac{2\rho_C}{WD_T}$, where ρ_C is the area specific contact resistivity, W is the graphene channel width, D_T is the transfer length known to be much smaller than the length (D_L or D_R) of graphene contact with the electrode on the left or right side [513-520]. Figure 58 shows the geometry parameters mentioned above. The graphene channel resistance is given by $R_{CH} = R_S \frac{L}{W}$, where R_S is the graphene sheet resistance and L is the graphene channel length. By assuming the area specific contact resistivity $\rho_C = 30 \text{ k}\Omega\mu\text{m}^2$ for the Ti/graphene contacts and $D_T = 0.1 \mu\text{m}$ [513-520], it is estimated that the graphene sheet resistance R_S for our sample is about 2.24 k Ω/\square .

Figure 57h and Figure 57i show the temperature-dependent current-voltage characteristics measured on the graphene/Si (Figure 57b) and Pt/Si (Figure 57c) junctions. As is well known [15, 187-190, 340-343], both junctions reveal the rectifying behavior at room temperature and the suppressed the forward and reverse biased currents with decreasing the temperature. However, depending on the temperature, it is seen that the rectifying behavior of the Pt/Si junction disappears more rapidly than that of the graphene/Si junction, and the current suppression becomes significant for the Pt/Si junction compared to the graphene/Si junction.

As shown in Figure 57j, the drain-to-source channel current in the graphene field-effect-transistor gated by the Si depletion layer (Figure 57d) reveals the low-efficient switching characteristics, which is likely to be disrupted by the current leaking through the graphene/Si contact (Figure 57e and Figure 57k). The sum of the channel current (Figure 57j) and the leakage current (Figure 57k) is shown in Figure 57l. Corrected with the leakage current flowing through the graphene/Si contact, Figure 57l reveals the enhanced switching characteristics compared to Figure 57j. Nevertheless, Figure 57l still reveals the low-efficient switching characteristics, implying that the gating with the Si depletion layer on the graphene layer is not so effective (Figure 57f). One thing to note clearly here is that the Dirac voltage is observed to be positive, verifying that the graphene layer is p-doped.

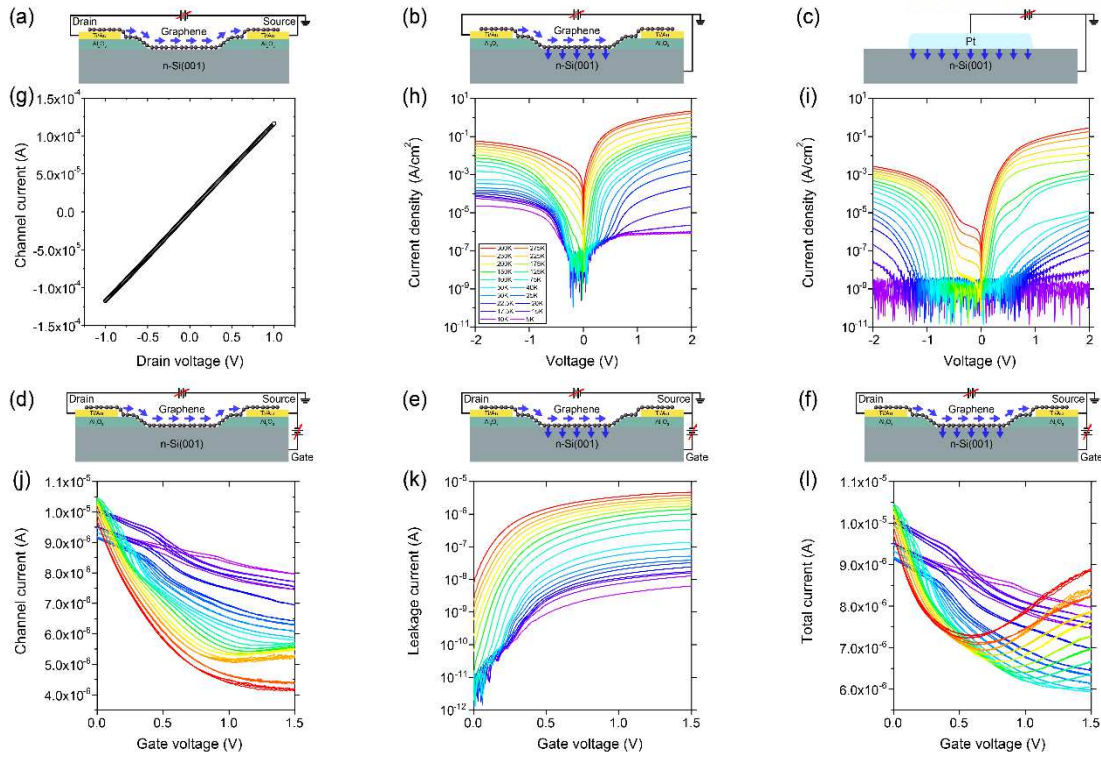


Figure 57. (a-f) Device structure and measurement configuration. (g) Graphene channel current versus drain voltage. (h) Current-voltage curves of the graphene/Si junction. (i) Current-voltage curves of the Pt/Si junction. (j) Graphene channel current versus gate voltage. (k) Graphene/Si leakage current versus gate voltage. (l) Total current flowing through graphene channel and graphene/Si junction versus gate voltage.

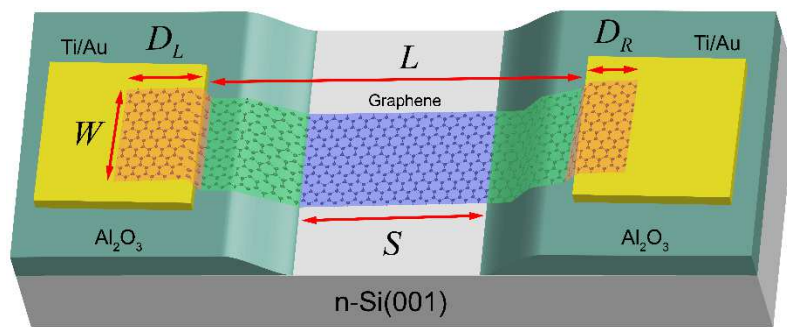


Figure 58. Device structure with geometry parameters, where W is the graphene channel width, L is the graphene channel length, S is the length of contact with Si, D_L is the length of graphene contact with Ti/Au electrode on the left side, and D_R is the length of graphene contact with Ti/Au electrode on the right side.

4.3 Improved Rectification Ratio at Low Temperature

The temperature-dependent Schottky barrier height and the ideality factor are shown in Figure 59b for the graphene/Si junction and Figure 59c for the Pt/Si junction. The extracted Schottky barrier height decreases with the temperature decreases. The smaller Schottky barrier height at lower temperature is very likely to be due to the suppression of the thermionic emission effect [15, 187-190, 340-343]. The increase of ideality factor at lower temperature usually indicates the presence of barrier inhomogeneity [15, 187-190, 359-377]. However, the strong variation in the ideality factor of Pt/Si junction in comparison with graphene/Si junction might imply the different transport mechanism for graphene/Si junction. It is also observed that the rectification ratio at 2V plotted in Figure 59c is quite similar around the room temperature (≥ 250 °C) for the graphene/Si and the Pt/Si junctions. However, the rectification ratio of the Pt/Si junction is reduced sharply with decreasing the temperature, while that of graphene/Si junction is maintained up to the low temperature (≥ 30 K). This implies that the charge carrier transport mechanism for graphene/Si and Pt/Si junctions might be different with each other and the non-ideal behavior of graphene/Si junction will be attributed to the other mechanism for charge carrier transport [15, 187-190, 340-353] (Chapter 1.4.4).

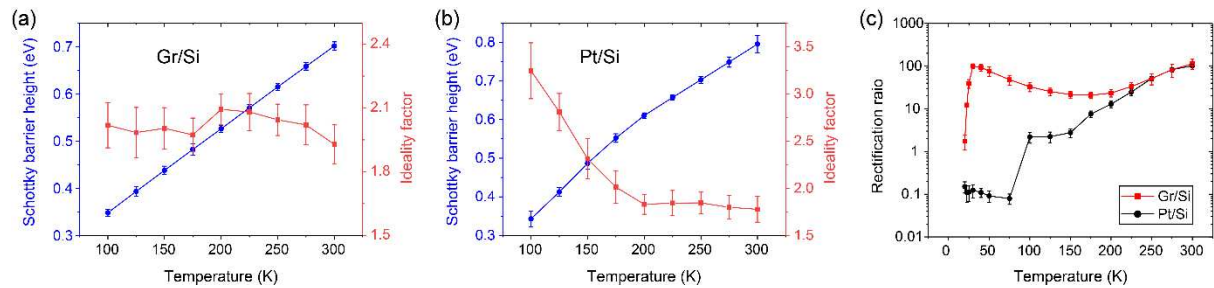


Figure 59. (a,b) Temperature-dependent Schottky barrier height and ideality factor with their standard errors for the graphene/Si (a) and the Pt/Si (b) junctions. (c) Rectification ratio at 2V.

4.4 Thermionic Emission Versus Recombination

The modified thermionic emission model for graphene/semiconductor Schottky contact [499, 502, 521] combined with the image force barrier lowering (Chapter 1.4.3) the graphene doping enhanced barrier lowering [495, 498, 499], and the series resistance [15, 187-190, 340-343] is adopted to analyze the current-voltage curve measured on our graphene/Si junction.

The modified thermionic emission equation for graphene/Si junction is given by Equation 58, where J_{TE}^G is the thermionic emission current density, q is the electric charge constant, k_B is the Boltzmann constant, T is the absolute temperature, $k_B T$ is the thermal energy (approximately 0.026 eV), \hbar is the plank constant. v_F is the Fermi velocity, V_A is the applied bias voltage, J is the total current density, A is the contact area, R is the series resistance, n is the ideality

factor. ϕ_{B0} is the zero bias Schottky barrier height, $\Delta\phi_1 = \left(\frac{q^3 N_D |\psi_s|}{8\pi^2 \epsilon_0^3 \kappa_s^3} \right)^{\frac{1}{4}}$ is the image force barrier

lowering energy, N_D is the doping concentration ($\sim 1 \times 10^{15} \text{ cm}^{-3}$) of the n-type Si,

$\psi = \phi_{bi} + \Delta\phi_1 = \phi_{B0} - k_B T \ln \left(\frac{N_C}{N_D} \right) - q(V_A - JAR)$ is the potential energy at the Si surface, ϕ_{bi} is

the built-in potential energy, $N_C = 2 \left(\frac{m^* k_B T}{2\pi \hbar^2} \right)^{\frac{3}{2}}$ is the effective density of states in the conduction

band of the Si [522], m^* is the effective mass in Si. ϵ_0 is the permittivity of the vacuum, κ_s is the

dielectric constant of the semiconductor, and $\Delta\phi_2$ is the graphene doping enhanced barrier lowering

energy. The graphene doping enhanced barrier lowering energy $\Delta\phi_2$ can be obtained [495, 498, 499]

by solving the charge neutrality condition $Q_G + Q_{SS} + Q_{SC} = 0$ [15, 163, 164, 189, 190, 207-224,

389, 487], where $Q_G = \frac{q \Delta E_F |\Delta E_F|}{\pi \hbar^2 v_F^2}$ is the doping charge density of graphene,

$Q_{SS} = -q D_{it} [E_g - E_{CNL} - (\phi_{B0} - \Delta\phi_1 - \Delta\phi_2)]$ is the interface-trap charge density on the Si surface,

$Q_{SC} = q N_D W_D$ is the space charge density in Si, D_{it} is the interface-trap density on the Si surface,

E_g is the band gap of the Si, E_{CNL} is the charge neutrality level of the Si, and $W_D = \sqrt{\frac{2\epsilon_0 \kappa_s |\psi|}{q N_D}}$

is the depletion region width. It should be noted that the increase of reverse-biased current is

attributed to the image force barrier lowering energy $\Delta\phi_1$ and the graphene doping enhanced barrier lowering energy $\Delta\phi_2$ [495, 498, 499]. The sign of ΔE_F should be positive for p-type graphene as confirmed in Figure 57l.

The measured data is well reproduced with the fitting curve obtained with Equation 58 by assuming $n = 1.75$, $\phi_{B0} = 0.7$, and $J = J_{TE}^G$ (Figure 60a). As discussed in Chapter 4.3, it is considered that the non-ideal effect of graphene/Si junction is due to the other transport mechanism [15, 187-190, 340-353], not the presence of barrier inhomogeneity [15, 187-190, 359-377]. Based on the recent studies [499, 502] claiming that the recombination current [354-358] dominates the non-ideal behavior of the forward-biased current in the graphene/Si junction, the measured data is well reproduced with the sum of the thermionic emission current and recombination current by assuming $n = 1$, $\phi_{B0} = 0.7$, and $J = J_{TE}^G + J_{RE}^G$ (Figure 60b), where J_{RE}^G is the recombination current density [15, 499, 502], n_i is the intrinsic carrier concentration in the Si [523], $\tau = \tau_0 \exp\left(-\frac{E_c - E_r}{k_B T}\right)$ is the recombination lifetime in the Si [524-527], τ_0 is the recombination lifetime constant, E_c is the conduction band edge in the Si, and E_r is the recombination energy level. Note that $\tau_0 = 10 \mu\text{s}$ and $E_c - E_r = 0.365 \text{ eV}$ for the best fitting of the measured data.

$$J_{TE}^G = \frac{qk_B^3}{\pi\hbar^3 v_F^2} T^3 \exp\left[-\frac{q(\phi_{B0} - \Delta\phi_1 - \Delta\phi_2)}{k_B T}\right] \left\{ \exp\left[\frac{q(V_A - JAR)}{nk_B T}\right] - 1 \right\} \quad (58)$$

$$J_{RE}^G = \frac{qW_D n_i}{2\tau} \left\{ \exp\left[\frac{q(V_A - JAR)}{2k_B T}\right] - 1 \right\} \quad (59)$$

As shown in Figure 60b, it is quite interesting that the measured forward-bias current can be reproduced with the thermionic emission independently with $n \neq 1$ or the sum of the thermionic emission and the recombination with $n = 1$. It is seen that the recombination current dominates in the small forward-bias regime ($0 \sim 0.2$ V). Comparing Equation 58 with Equation 59, the slope of the natural logarithm of the current density $\ln J$ as a function of the applied bias voltage V_A in the small forward-bias regime is the $\frac{q}{nk_B T}$ for the thermionic emission (Equation 58) and $\frac{q}{2k_B T}$ for the recombination (Equation 59). As shown in Figure 59b, the ideality factor extracted from the current-voltage curve measured on the Pt/Si junction increases with the temperature decreasing, which is known to be due to the presence of barrier inhomogeneity [15, 187-190, 359-377]. On the other hand, the ideality factor extracted from the slope in the current-voltage curve measured on the graphene/Si junction (Figure 59a) remains at about the similar value around 2. As is well known, the thermionic emission decreases rapidly with decreasing temperature [344-348]. From this point of view, we can make conjecture that the non-ideal effect of the graphene/Si junction in the small forward bias regime actually stems from the recombination and the recombination is somehow maintained up to around 100 K.

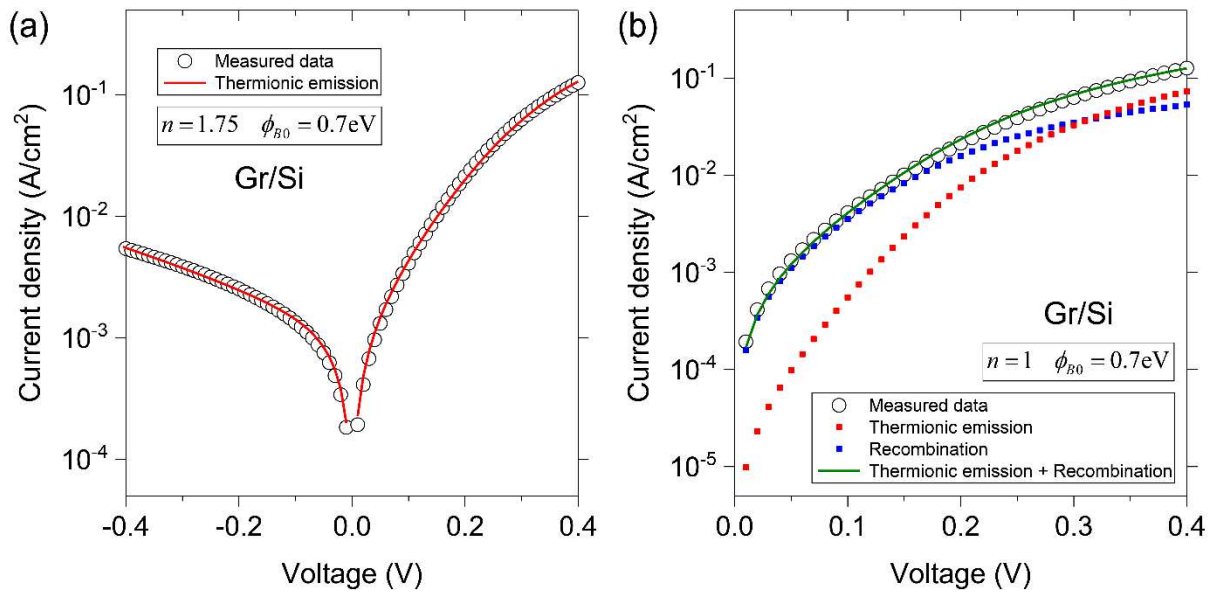


Figure 60. (a,b) Current density-voltage curve for the graphene/Si junction. (a) Measured data with the fitting curve to the thermionic emission current density J_{TE}^G with $n = 1.75$ and $\phi_{B0} = 0.7$. (b) Measured data with the fitting curve to the thermionic emission current density J_{TE}^G and recombination current density J_{RE}^G with $n = 1$ and $\phi_{B0} = 0.7$.

The cubic of the temperature T^3 is in the coefficient of equation for the thermionic emission current density J_{TE}^G [499, 502, 521] (Equation 58). On the other hands, the coefficient of equation for the recombination current density J_{RE}^G [15, 499, 502] (Equation 59) consists of more complex temperature-dependent parameters such as the depletion region width $W_D = \sqrt{\frac{2\epsilon_0\kappa_s|\psi|}{qN_D}}$, the potential energy $\psi = \phi_{B0} - k_B T \ln\left(\frac{N_C}{N_D}\right) - q(V_A - JAR)$ at the Si surface, the effective density of states $N_C = 2\left(\frac{m^*k_B T}{2\pi\hbar^2}\right)^{\frac{3}{2}}$ in the conduction band of the Si [522], the intrinsic carrier concentration $n_i = 5.29 \times 10^{19} \left(\frac{T}{300}\right)^{2.54} \exp\left(-\frac{6726}{T}\right)$ in the Si [523], and the recombination lifetime $\tau = \tau_0 \exp\left(-\frac{E_c - E_r}{k_B T}\right)$ in the Si [524-527]. Based on the thermionic emission current density J_{TE}^G [499, 502, 521] (Equation 58) and recombination current density J_{RE}^G [15, 499, 502] (Equation 59), the temperature-dependent current-voltage curve is plotted in Figure 61, which reveals the stark difference between the thermionic emission and the recombination. Comparing with the measured one (Figure 61a), both the current density of thermionic emission J_{TE}^G with $n = 1.75$ (Figure 61b) and the current density of thermionic emission J_{TE}^G with $n = 1$ (Figure 61c) are suppressed very significantly with the temperature decreasing. On the other hands, the reduction of current density of recombination J_{RE}^G with $n = 1$ (Figure 61d) is relatively slow depending on the temperature. Accordingly, the current density of the sum of the thermionic emission and the recombination $J_{TE}^G + J_{RE}^G$ with $n = 1$ (Figure 61e) reveals that total current is dominated by the recombination. This is consistent our result claiming that the that recombination actually plays an important role in the charge carrier transport mechanism across the graphene/Si interface and the recombination is maintained up to the low temperature. Based on this result, it can be claimed that the low temperature rectification at the graphene/Si interface [151-154, 528] occurs due to the recombination.

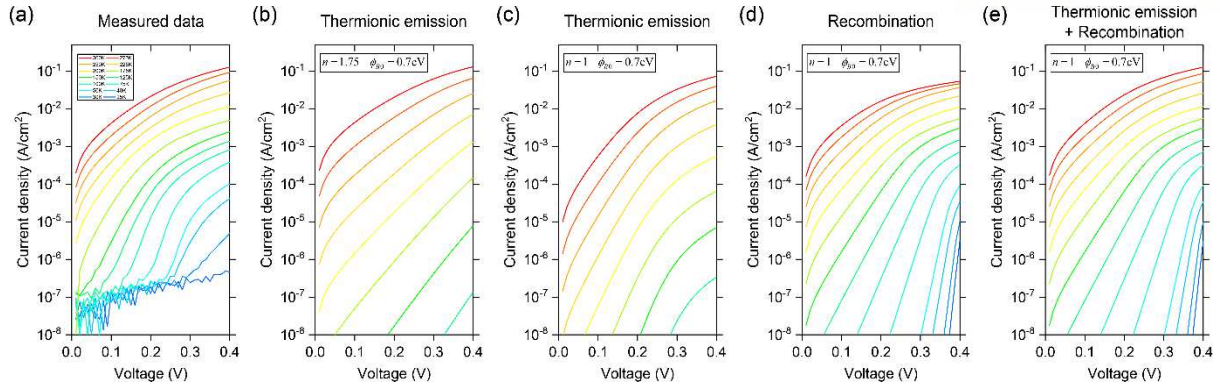


Figure 61. (a-e) Current-voltage characteristics of the graphene/Si junction for the measured one (a), the thermionic emission J_{TE}^G with $n = 1.75$ (b), the thermionic emission J_{TE}^G with $n = 1$ (c), the recombination J_{RE}^G with $n = 1$ (d), and the sum of the thermionic emission and the recombination $J_{TE}^G + J_{RE}^G$ with $n = 1$ (e).

4.5 Recombination Current due to the Hole Carriers Supplied from Graphene

Figure 62a shows the ratio of the recombination current J_{RE}^G to the sum of the thermionic emission current and the recombination current $J_{TE}^G + J_{RE}^G$, showing that the recombination process is actually predominant in the small forward bias regime and the total current is totally governed by the recombination current below 200 K. The energy band diagrams with the relevant potential energy parameters and charge carrier transport mechanisms are shown in Figure 62b for the zero bias, Figure 62c for the forward bias, and Figure 62c for the reverse bias. As confirmed in Figure 57l, the graphene is p-doped and possess a considerable amount of the hole carriers. Therefore, unlike the conventional metal/Si junction where the holes are generally limited in the metal electrode, the hole carriers supplied from the graphene can be directly injected into the Si surface and the Si depletion layer under the forward bias (Figure 62b). It is likely that the injected holes encountering the electrons in the Si depletion layer will contribute to the recombination current in the small forward bias regime. Since the depletion region width W_D shrinks with the increase of the applied bias voltage V_A , the recombination ratio shown in Figure 62a is reduced in the higher forward bias. As shown in Figure 61 and Figure 62a, the recombination current in the graphene/Si junction seems to survive at the low temperature up around 100 K. This is also likely because the depletion region width W_D increases as the temperature decreases [15], raising a possibility of meeting the injected holes supplied from the graphene and the electron coming from the Si bulk. It is also noted that the image force barrier lowering energy $\Delta\phi_1$ and the graphene doping enhanced barrier lowering energy $\Delta\phi_2$ cause the increase of reverse-biased current [495, 498, 499].

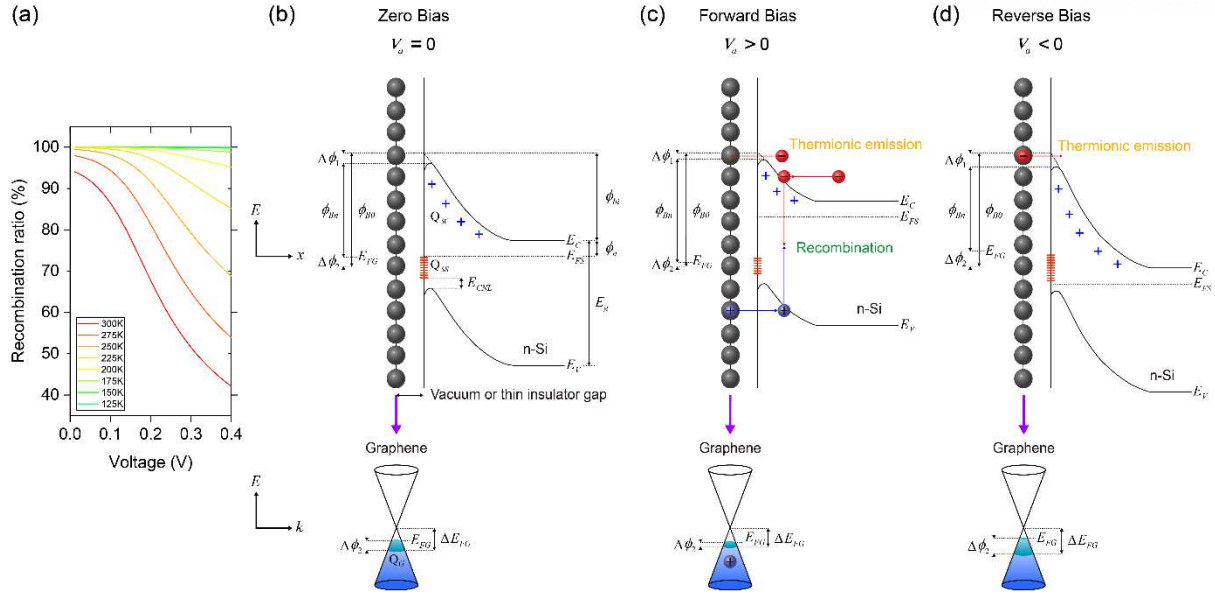


Figure 62. (b-d) Energy band diagram shown in the upper side is drawn as a function of position in the junction and the corresponding linear energy dispersion relation of graphene with the Fermi-level indicated is drawn below [389], where ϕ_B is the Schottky barrier height, ϕ_{B0} is the zero bias Schottky barrier height, $\Delta\phi_1$ is the image force barrier lowering energy, $\Delta\phi_2$ is the graphene doping enhanced barrier lowering energy, ϕ_{bi} is the built-in potential energy, E_{FG} is the Fermi-level of the graphene, ΔE_{FG} is the Fermi-level shift in the graphene, E_{FS} is the Fermi-level of the Si, E_C is the conduction band edge in the Si, E_V is the valence band edge in the Si, E_{CNL} is the charge neutrality level of the semiconductor, E_g is the band gap of the Si, Q_G is the doping charge density of the graphene, Q_{SS} is the interface-trap charge density on the Si surface, Q_{SC} is the space charge density in the depletion region of the Si.

4.6 Conclusion

The graphene field-effect-transistor without the SiO₂ insulating layer is fabricated to investigate the temperature-dependent carrier transport properties across the graphene channel or the graphene/Si interface. The p-type doping of graphene is also verified with the simultaneous transport measurement gated with the Si depletion layer developed by the positive bias on the Si substrate. It is found that the non-ideal effect of the graphene/Si junction stems from the recombination process dominating in the small forward bias regime since the hole carriers supplied from the p-doped graphene function as the source of recombination occurring in the Si depletion region. This implies that the recombination can be maintained up to the low temperature owing to the increased depletion width. Unlike conventional metal/semiconductor diode losing its function at low temperature, the graphene/Si Schottky diode can preserve the performance characteristics as a rectifier and offer the possibility to utilize a new class of diode that can operate even at the low temperature comparable to the room temperature.

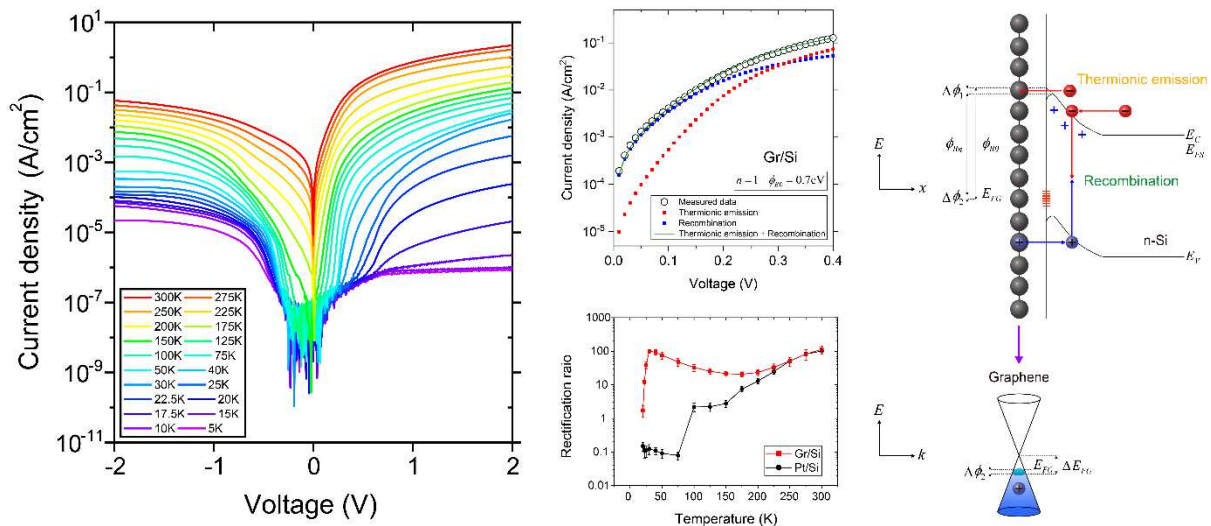


Figure 63. Summary of Chapter 4.

5. Enhanced Thermionic Emission and Tunneling at Junction Edges

As explained in Chapter 1.4.2 and Chapter 2.7, the origin of Fermi-level pinning effect is known to be the electric dipole layer associated with the trap states on the semiconductor surface [15, 189, 190, 207-224]. The electric dipole layer is known to be restricted near the junction edge since the effective contact between the metal and the semiconductor for the charge transfer is reduced at the edge. Thus, the influence of interface electric dipole layer is expected to be limited when the occupied area of electric dipole layer is relatively too small so that the charge density on the semiconductor surface is restricted [159-162, 177, 468-472, 529-532]. In that case, the energy band profile in the depletion region on the semiconductor side appears not to be affected by the Fermi-level pinning effect, since the influence of interface electric dipole layer cannot reach deep into the semiconductor substrate. This area-dependent effect of interface electric dipole layer relies on the fact that the surface charge density at the center of the small-area Schottky junction will be comparable to that at the edge. More specifically, as the contact size of Schottky junction gets small below about hundreds nanometer, the magnitude of leakage current component will be largely increased mainly flowing through the junction edge where the Fermi-level pinning effect is seemingly limited. Accordingly, the current-voltage characteristics of nano-junction will seem to be almost unaffected by the interface Fermi-level pinning effect although the actual Fermi-level pinning effect is strong at the entire junction [177]. This is a crucial phenomenon directly related to the nanoscale device operation (Chapter 1.4.4). Here, it is experimentally demonstrated that the effective Schottky barrier height of Al/Si and Al/Graphene/Si junctions decreases with the lateral width of junction decreasing. From the finite-element electrostatic modeling to obtain the energy band profile across the junction and the numerical calculation to estimate the current flowing through the junction, as the lateral size of junction becomes smaller, it is found that the potential barrier gets narrower and the current-voltage characteristic is governed by the thermionic emission and the tunneling of charge carriers around the junction edge. It is also believed that our work can provide a physically-reasonable clue for understanding the drastic size-dependent variation of current-voltage characteristic in the nanoscale device architecture.

5.1 Sample Fabrication

The lateral-size-varying Al/Si and Al/graphene/Si junctions shown in Figure 64 are prepared as follows. The n-type ($\sim 1 \times 10^{15} \text{ cm}^{-3}$) Si substrate is first cleaned with the RCA process [299-304]. The 30-nm-thick Al_2O_3 insulating film is deposited by using the atomic layer deposition (ALD). In order to fabricate the wide trenches in the Si substrate, the stripe patterns are created by photolithography processing. The exposed Al_2O_3 regions are then removed by buffered oxide etchant (BOE) wet etching for 20 sec. After the photoresist removal, the samples are treated in methanol for rinsing. The monolayer graphene grown with chemical vapor deposition (CVD) was transferred onto the substrates. It is noted that the semi-dry transfer method is employed to minimize the water molecule trapping at the interface [390-406]. The metal electrodes consisting of Ti/Au (10/50 nm) are then deposited through a shadow mask on the Al_2O_3 /Si surface by using the e-beam evaporation. The samples are dipped in a BOE etching solution once again to remove any native oxide. The rectangular-shaped width-varying patterns covering both the metal electrode and the Si trench are written by the e-beam lithography. Subsequently, the Al electrodes of 50 nm are deposited by the using e-beam evaporation. After the lift-off process, the Raman spectroscopy are carried out near the Al electrodes on Si trench. As shown in Figure 65, the quality of transferred graphene is identified by comparing the Raman spectra of the graphene-uncovered region with that of the graphene-covered region [465-467]. Finally, the graphene uncovered by Al electrodes are removed with reactive ion etching (RIE) to isolate each junction. The Al/Si and Al/graphene/Si junctions are formed on the graphene-uncovered and graphene-covered regions respectively.

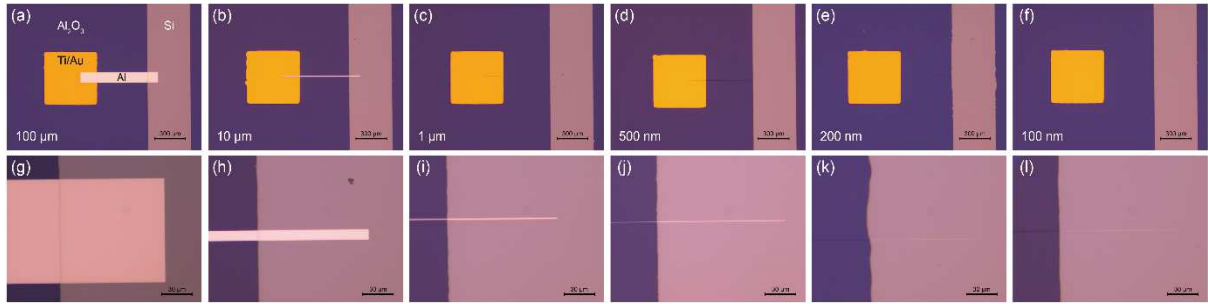


Figure 64. (a)-(l) Optical microscope images of the Al/Si junction formed on the Si-trench under the Al_2O_3 . The contact size of junction is controlled by the lateral width of the Al electrode connected with the Ti/Au pad on the Al_2O_3 . (a) 100 μm , (b) 10 μm , (c) 1 μm , (d) 500 nm, (e) 200 nm, (f) 100 nm. (g)-(l) the corresponding magnified view of (a)-(f).

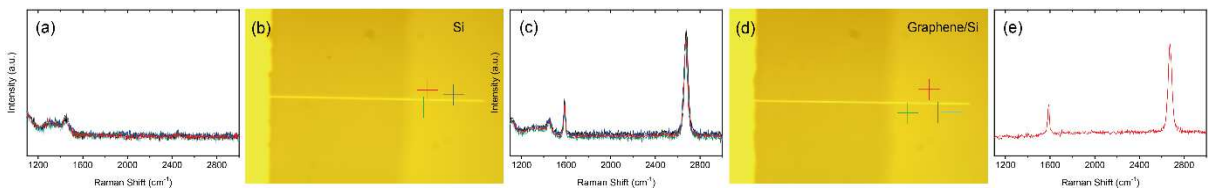
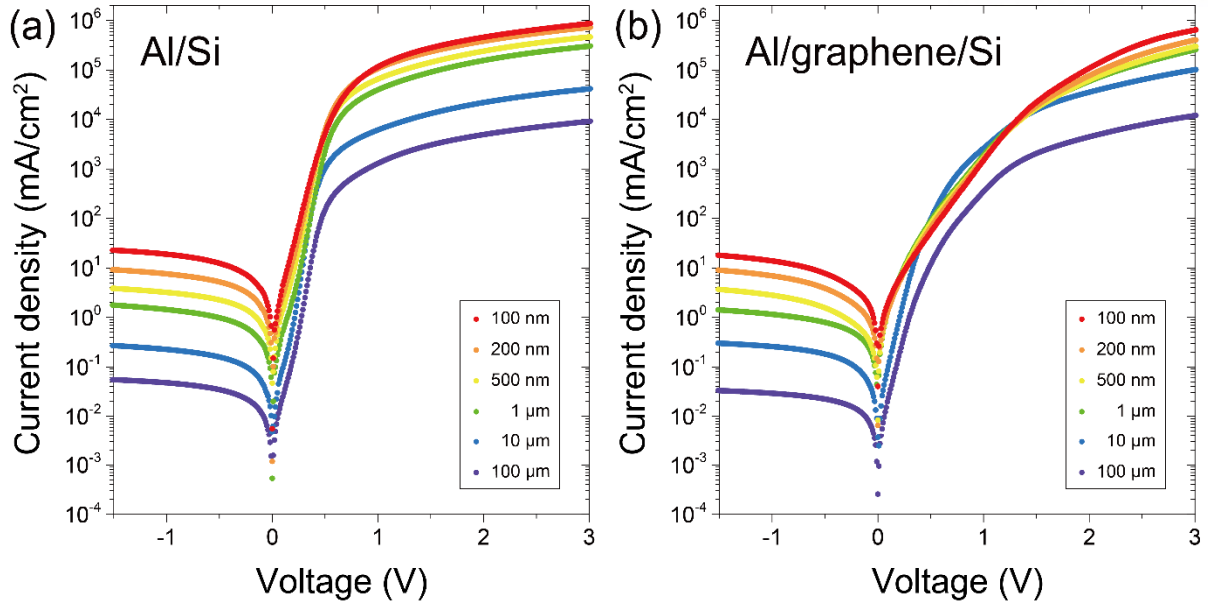


Figure 65. Raman spectra of the bare Si (a) measured on (b), the graphene on Si (c) measured on (d), graphene with the Si background signal subtracted (e) [465-467].

5.2 Current-Voltage Measurement

Figure 66 show the current density-voltage curves measured on Al/Si and Al/graphene/Si junctions depending on the lateral size. The typical rectifying characteristic appears in Al/Si junction (Figure 66a) and the non-ideal forward-bias behavior is observed in Al/graphene/Si junction (Figure 66b). Averaged over several different junctions by adopting the thermionic emission model [15, 340-358], the extracted Schottky barrier heights and ideality factors are listed in Figure 66c. The effective Schottky barrier heights scale down with the lateral size of junction. Interestingly, the non-ideal effect in Al/graphene/Si junction becomes striking and saturated as the lateral width of junction decreases.

Regarding the reverse-bias leakage current, it is reported that the local material intermixing of metal and Si atoms inducing the low barrier patches in the metal/Si junction and increasing the leakage current can be blocked by the graphene diffusion barrier [177]. If the atomic interdiffusion at the interface is active enough, the reverse-bias leakage current of metal/Si junction will be increased, while that of metal/graphene/Si junction can be effectively suppressed with the graphene interlayer preventing the interdiffusion. However, the reverse-bias leakage current of Al/Si junction (Figure 66a) is somehow similar to that of Al/graphene/Si junction (Figure 66b). This implies that the atomic reaction at the Al/Si interface used in this work does not occur quite actively and the reverse-bias leakage currents of our Al/Si and Al/graphene/Si junctions are not attributed to the inhomogeneity-related leakage current. Meantime, the reverse-bias leakage current is noticeably increased with the downscaling of Al electrode, indicating that the reverse-bias leakage currents arise from the other mechanism.



(c)

Lateral width		100 μm	10 μm	1 μm	500 nm	200 nm	100 nm
Al/Si	ϕ_B (eV)	0.774	0.733	0.693	0.664	0.644	0.627
	n	1.83	1.89	1.98	1.99	2.05	2.09
Al/graphene/Si	ϕ_B (eV)	0.747	0.713	0.622	0.619	0.620	0.609
	n	2.35	2.14	3.90	4.19	4.37	5.16

Figure 66. (a,b) Current density-voltage curves measured on the Al/Si (a) and the Al/graphene/Si (b) junctions depending on the lateral width of Al electrode. (c) Extracted Schottky barrier heights and ideality factors depending on the lateral size.

5.3 Energy Band Profile across Interface

In order to understand the influence of electrostatic environment between nano and bulk geometries on the leakage current near the edge of the Schottky junction, as shown in Figure 67, the conduction energy band distributions at around the Al/Si interface are plotted by performing the finite element electrostatic modeling with a commercial software package FlexPDE [482-484]. The schematic of device structure shown in Figure 67a is employed for the modeling by varying the lateral width of Al electrode. As can be seen from the cross-sectional band profiles across the center and edge of Al/Si junction in Figure 68, the depletion width shrinks smaller with the downscaling of lateral width. This is found at both the center (Figure 68a) and the edge (Figure 68b). The number of charge carriers tunneling through the Schottky barrier is expected to increase sharply as the depletion width decreases [15, 349-353, 533, 534]. In particular, from the center to the edge, the Schottky barrier height decreases and the depletion width becomes thinner. This implies that both the thermionic emission current due to the low Schottky barrier height and the tunneling current due to the narrow barrier width at the edge of the Schottky junction lead to the modification in I-V characteristics. Actually, this expectation is in agreement with the increased reverse-bias leakage current in Figure 66a. Based on this result, it can be claimed that the reverse-bias leakage currents of Al/Si and Al/graphene/Si junctions are attributed to the edge-related leakage current.

Interestingly, the difference in depletion width between the center and the edge is significantly reduced in the nanoscale contacts (Figure 68d), compared to the wide planar contacts (Figure 68c). In other words, the energy band profiles across the center of nano-junction (Figure 68d) drops rapidly compared to that of planar-junction (Figure 68c). This is likely because the electric field at the center, just as that at the edge, is affected by the surrounding semiconductor bulk in the nano-sized junction. At this stage, it looks worthwhile to review the metal/semiconductor nano-junction, which is categorized into two cases in general. One is the nano-size metal contacts to bulk semiconductor, which is associated with the geometrically-induced nonlocal environmental pinning effect [535]. The other is the metal to semiconductor nano-contacts, deriving the environmental pinning effect from quantum confinement [536]. As mentioned previously, the origin of Fermi-level pinning is known to be the electric dipole layer brought about by the interface states on the semiconductor surface [15, 189, 190, 207-224]. Since the weighted charge distribution is lower at the edge in comparison with at the center, the influence of electric dipole layer changing the electrostatic potential across the interface is expected to be limited near the edge. This is actually what is observed in Figure 68c. However, as the junction lateral size relatively gets too small, there would be no significant change in the effect of interface dipole layer on the energy band profile between the center and the edge, which is identified in Figure 68d.

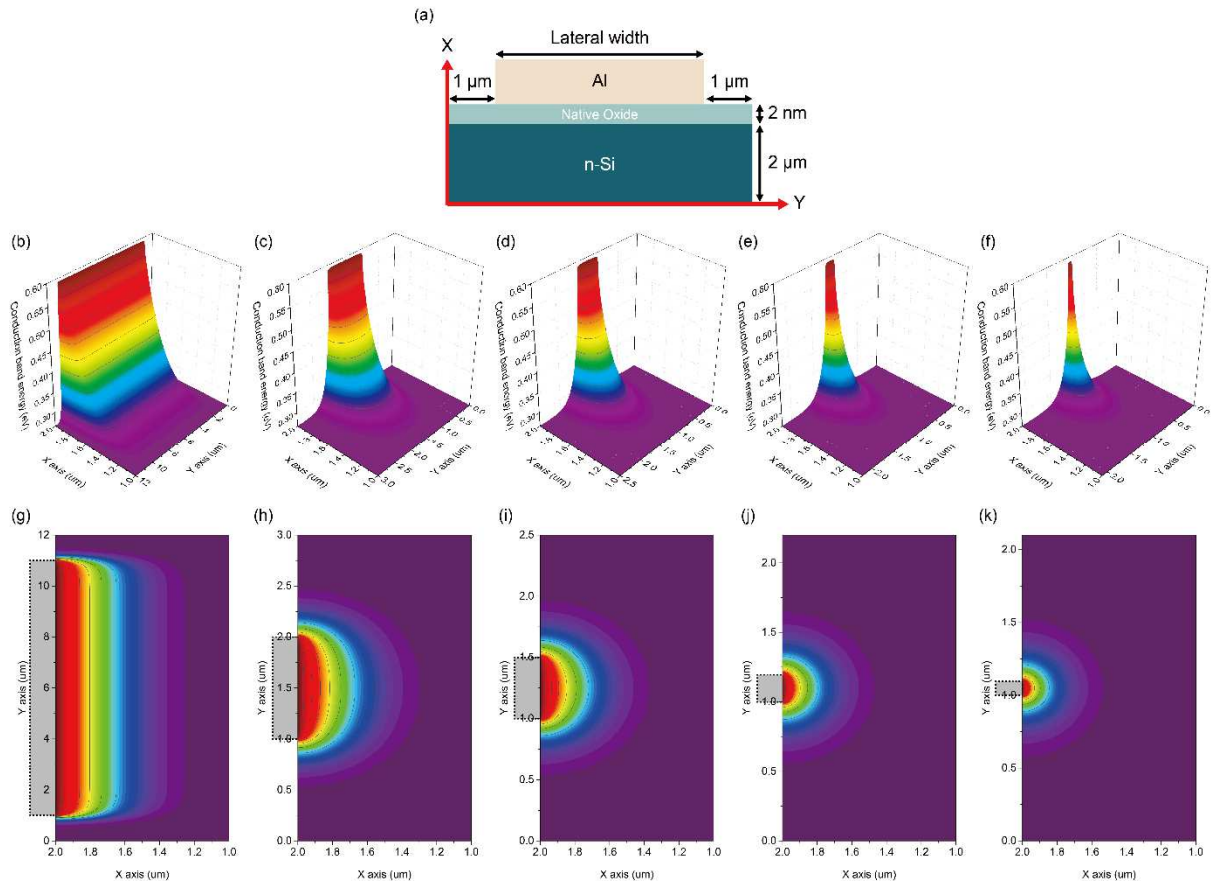


Figure 67. (a) Schematic of device structure employed for the modeling. (b)-(k) Conduction energy band distributions at around the Al/Si interface by varying the lateral width of Al electrode. 3D-view: 10 μm (b), 1 μm (c), 500 nm (d), 200 nm (e), 100 nm (f). 2D-view: 10 μm (g), 1 μm (h), 500 nm (i), 200 nm (j), 100 nm (k). The gray rectangles in (g)-(k) represent the areas of Al electrode.

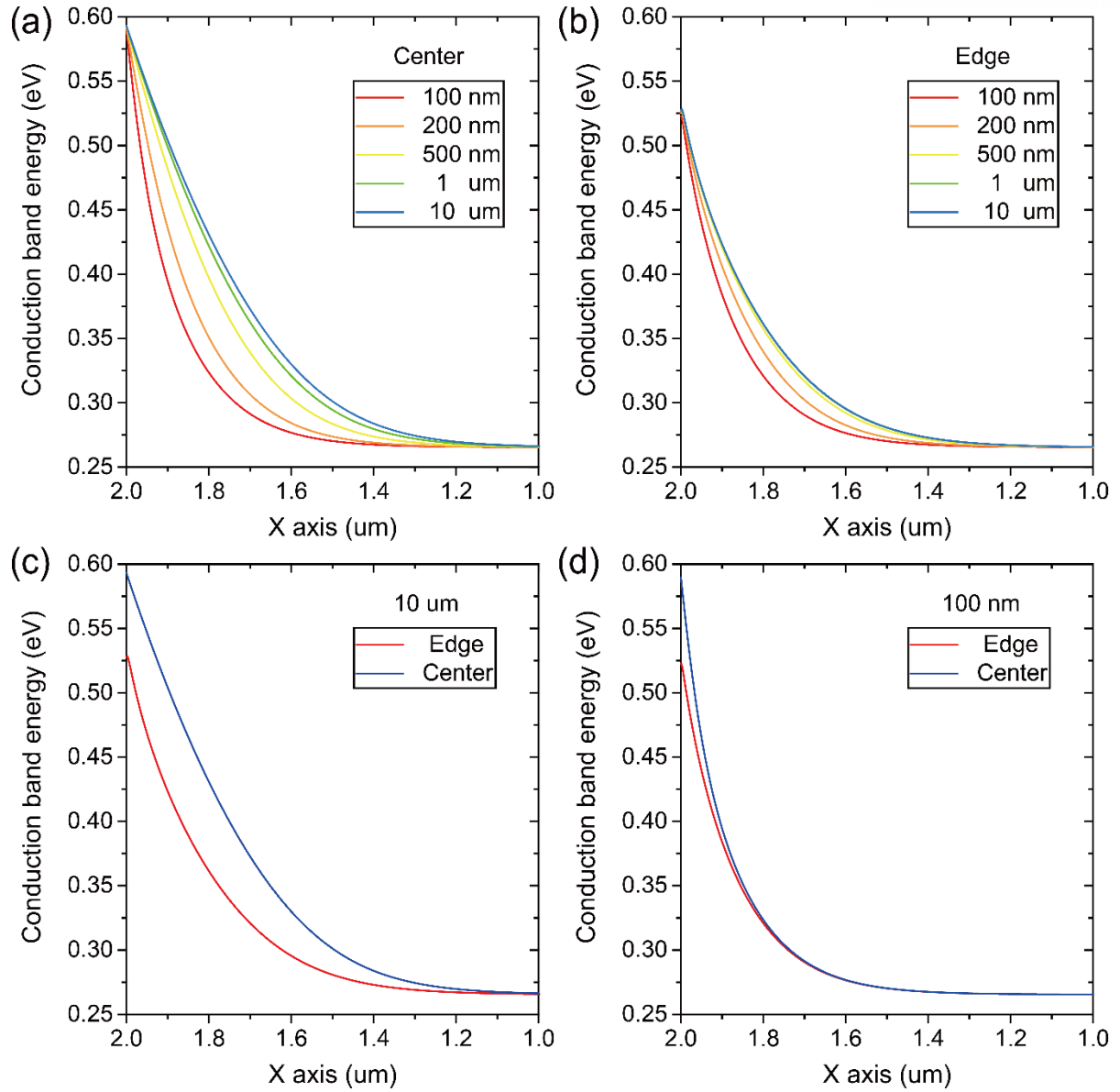


Figure 68. (a)-(d) Conduction energy band profiles across the center and the edge of Al/Si junction by varying the lateral width of Al electrode. (a) center, (b) edge, (c) 10 μm, (d) 100 nm.

5.4 Thermionic Emission Versus Tunneling

In order to address the deviation of edge-related leakage currents between the nano-size Schottky junction and the wide-planar one, the thermionic emission and tunneling currents flowing across the center and the edge of Al/Si junction are calculated with a MATLAB program [15, 340-344, 349-353, 533, 534, 537]. As shown in Figure 69, the smaller the lateral size of junction, the larger the reverse-bias leakage current, which is in agreement with the experimental observation in Figure 66a. In addition, the thermionic emission current at the center (Figure 69a) is found to be smaller than that at the edge (Figure 69b). Likewise, the tunneling current at the center (Figure 69c) is also seen to be smaller than that at the edge (Figure 69d). This is because the barrier height and the barrier thickness at the center (Figure 68a) are higher and wider than those at the edge (Figure 68b). It is known that the thermionic emission is determined by the Schottky barrier height, while the tunneling depends on both the Schottky barrier height and the thickness [15, 340-344, 349-353]. The thermionic emission current (Figure 69a and Figure 69b) is observed to be larger than the tunneling current (Figure 69c and Figure 69d). Hence, it can be claimed that the Schottky barrier height substantially influences on the thermionic emission rather than the tunneling. Depending on the lateral size, the change in tunneling current (Figure 69c and Figure 69d) is more noticeable than that in thermionic emission current (Figure 69a and Figure 69b). As mentioned just before, the tunneling strongly depends on the thickness of Schottky barrier because the narrow barrier width results in a high electric field at the interface [15, 340-344, 349-353]. It is apparent that the Schottky barrier thickness becomes narrow (Figure 68a and Figure 68b) and the tunneling current increase (Figure 69c and Figure 69d) in accordance with decreasing of lateral junction size. This phenomenon is expected to be significant in the Schottky junction with narrower barrier thickness fabricated with the more highly-doped Si substrate than those used in this work.

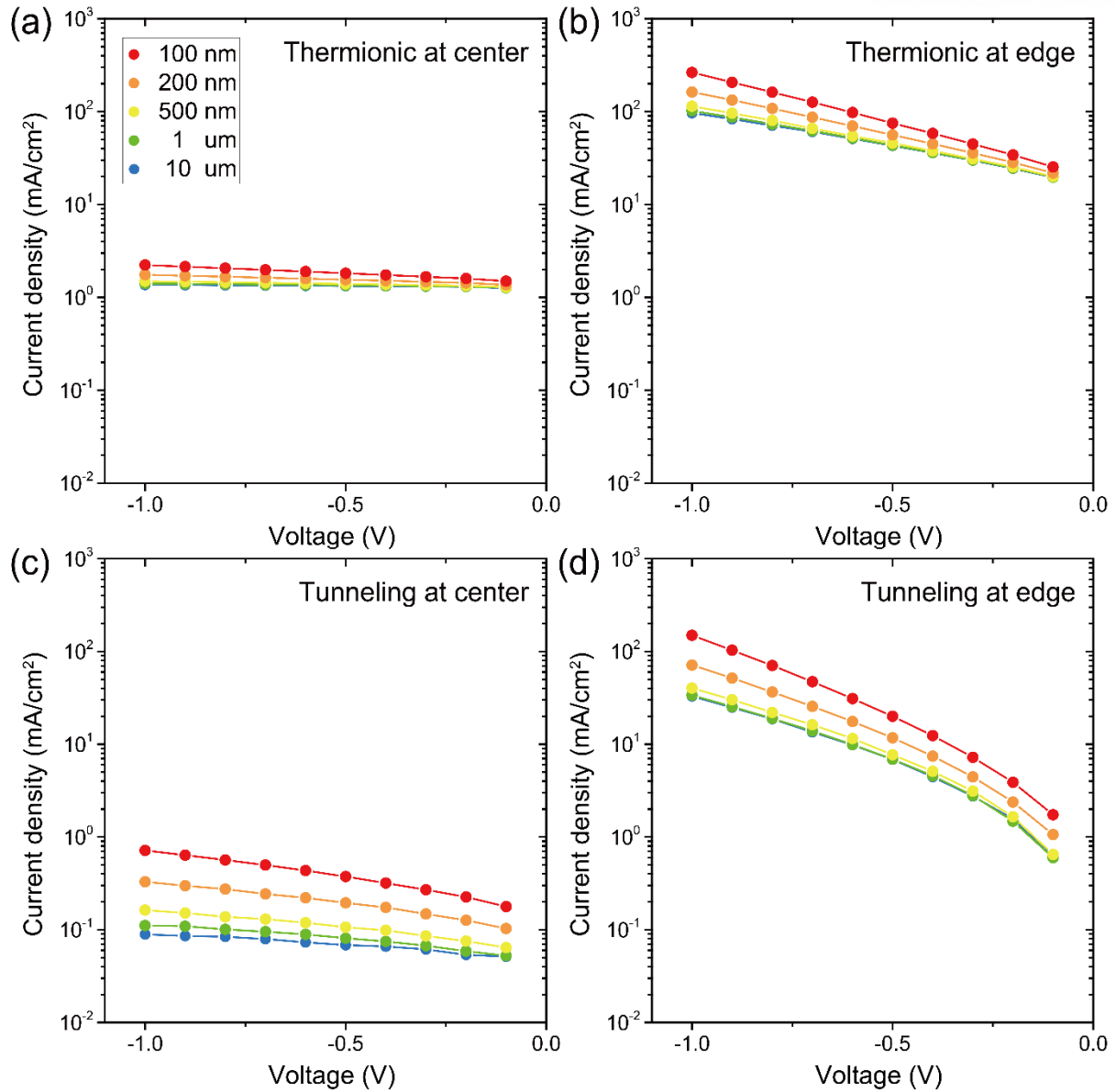


Figure 69. (a)-(d) Current density-voltage curves calculated on the center and the edge of the Al/Si junction by varying the lateral width of the Al electrode. (a) Thermionic emission current at the junction center, (b) Thermionic emission current at the junction edge, (c) Tunneling current at the junction center, (d) thermionic emission current at the junction edge.

5.5 Edge Current Enhanced with Downscaling of Lateral Width

Based on our I-V measurement in Figure 66, band profile in Figure 68, and current calculation in Figure 69, it can be claimed as follows. In case of the Al/Si junction (Figure 70a and Figure 70c), the dominant conduction mechanism is responsible for the thermionic emission and the tunneling, which are enhanced at the junction edge (Figure 70c) due to the reduced barrier height and thickness. Because the depletion region where the recombination takes place is thin at the junction edge, the recombination will be low. On the other hand, for the Al/graphene/Si junction (Figure 70b and Figure 70d), the recombination is expected to become significant with the graphene interlayer. The graphene is considered to be p-doped and a substantial amount of the hole carriers supplied from the p-doped graphene interlayer can be injected into the Si depletion region, contributing to the recombination eventually. What is interesting in this point is that the depletion width, *i.e.*, the Schottky barrier thickness itself is the competing factor determining both the tunneling and the recombination. As seen in Figure 66, the saturated non-ideal I-V characteristic under the forward-bias seems to be attributed to the interplay of tunneling and recombination especially for the nano-Schottky junction.

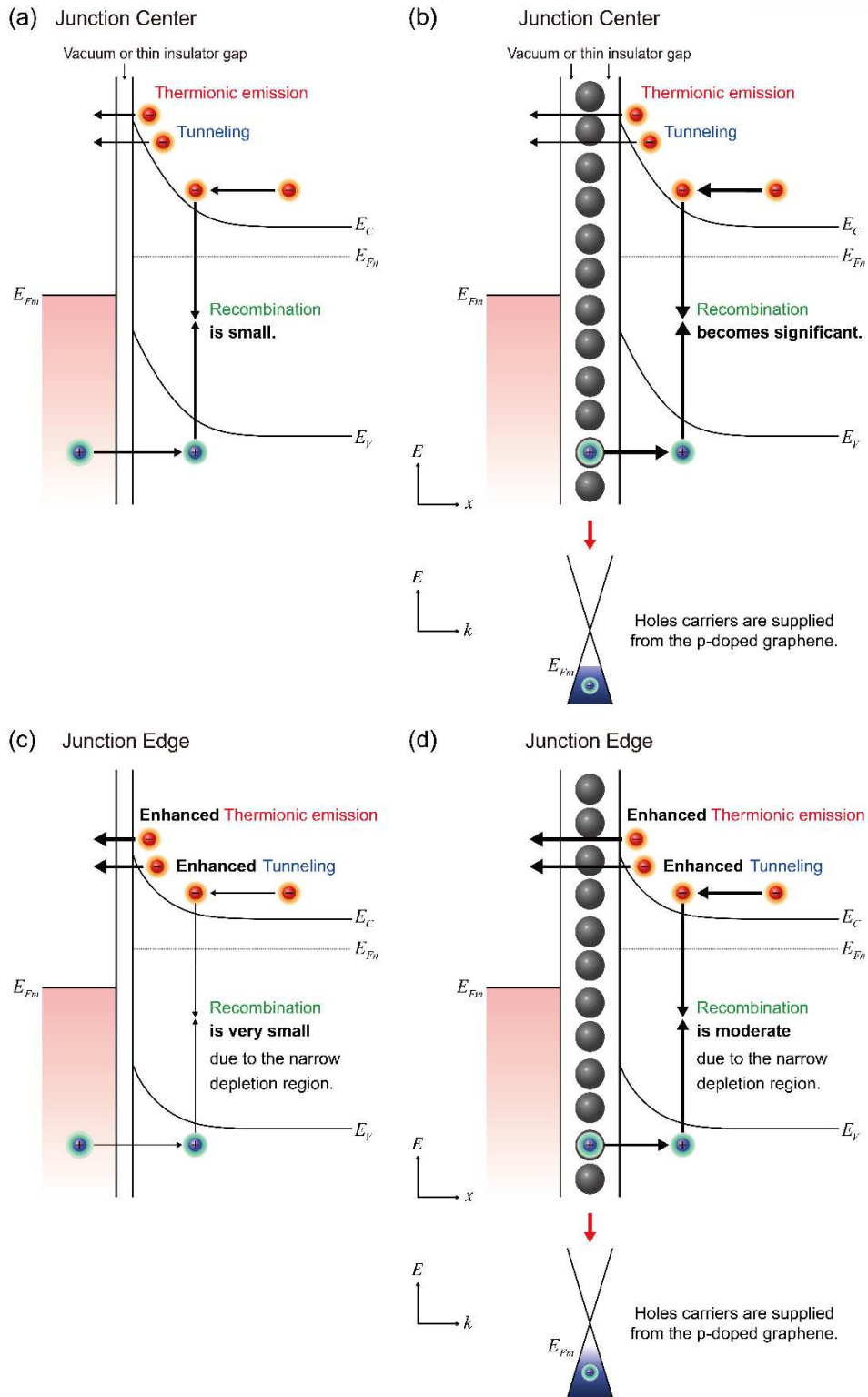


Figure 70. (a)-(d) Schematic of illustrating the transport mechanisms in the metal/Si junction at the junction center (a) and the edge (c) and the metal/graphene/Si junction at the junction center (b) and the edge (d) described by thermionic emission, tunneling, and recombination [389].

5.6 Conclusion

It is experimentally observed that the effective Schottky barrier height of Al/Si and Al/graphene/Si junctions are reduced with decreasing the lateral size of Al electrode. It is found that the thermionic emission and the tunneling of charge carriers across the interface near the junction edge provide a plausible explanation for the downscaling effect in Al/Si and Al/graphene/Si junctions. The dominance of the edge current component in the total junction current implies that the lateral-size-dependent charge carrier transport is mainly attributed to the low effective Schottky barrier height formed around the junction edge. The forward-biased current of Al/graphene/Si junction is enhanced in comparison with that of Al/Si junction, which is attributed to the recombination process regarding the hole carriers injected from p-doped graphene, which is consistent with Chapter 4. The low resistance conduction path is generally considered to be the most important factor in the leakage current so that this work provides the useful information to solve the leakage current problems in the nanoscale devices.

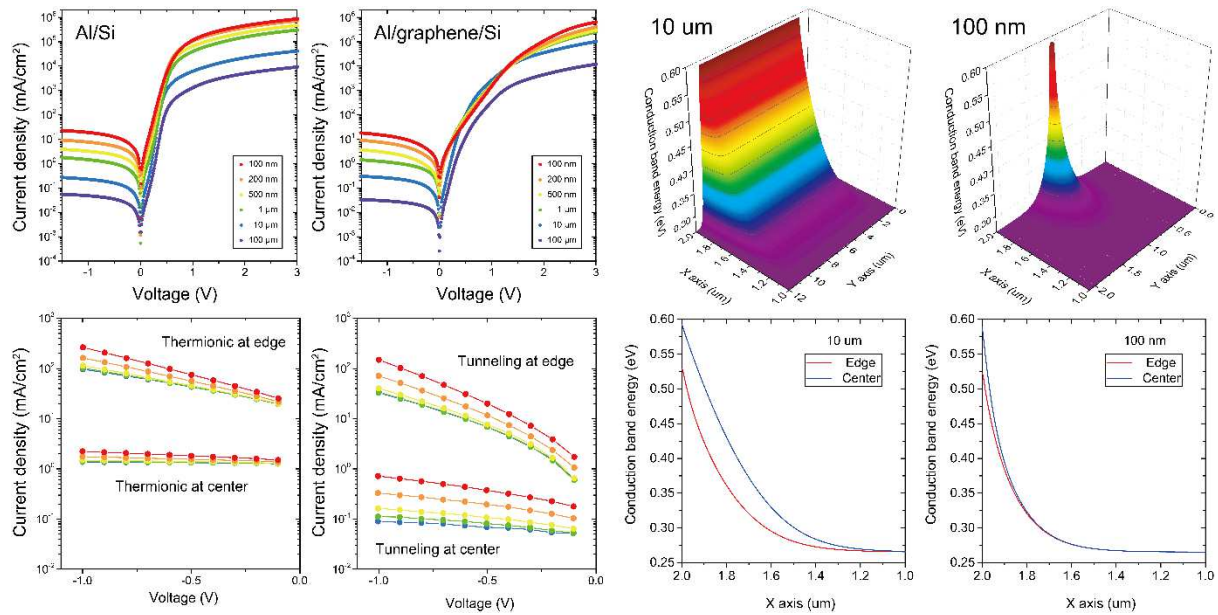


Figure 71. Summary of Chapter 5.

6. Electrically-Controlled Carrier Guiding in Single-Channel Graphene Superlattice Device

As discussed in Chapter 1.3.2 and Chapter 1.7.1, the ballistic charge carrier in the graphene satisfies the fundamental conservation laws and acts like the massless Dirac particle described by the Dirac equation [68-72, 186]. Here, the theoretical calculations on the time-evolving probability density of electron wave packets propagating in the graphene superlattice structure are performed, showing that the propagation direction and the spread of electron wave packets in the graphene channel sensitively depend on the magnitude of superlattice potential. The graphene superlattice is adopted by a Kronnig-Penny type of periodic potential generated with alternating n-and p-type doping regions in the graphene. The single-channel multi-drain graphene superlattice device can be used to guide the charge carriers to a specific direction just by controlling the electrostatic environment in the channel, inspiring a new perspective in the conductance switching mechanism of the graphene device and achieving a high on-off current ratio regardless of zero band-gap property of graphene.

6.1 Device Geometry

The single-channel multi-drain graphene device is designed with pristine graphene (Figure 72a) or superlattice graphene (Figure 72e). If we assume the probability density distribution of a Gaussian localized electron wave packets in the pristine graphene at initial (Figure 72b), the electron probability density distribution can be tracked with time-evolving (Figure 72d) or time-integrated (Figure 72c) forms. As shown in Figure 72c and Figure 72d, the electron packets propagate in the form of a concentric circle with the pristine graphene.

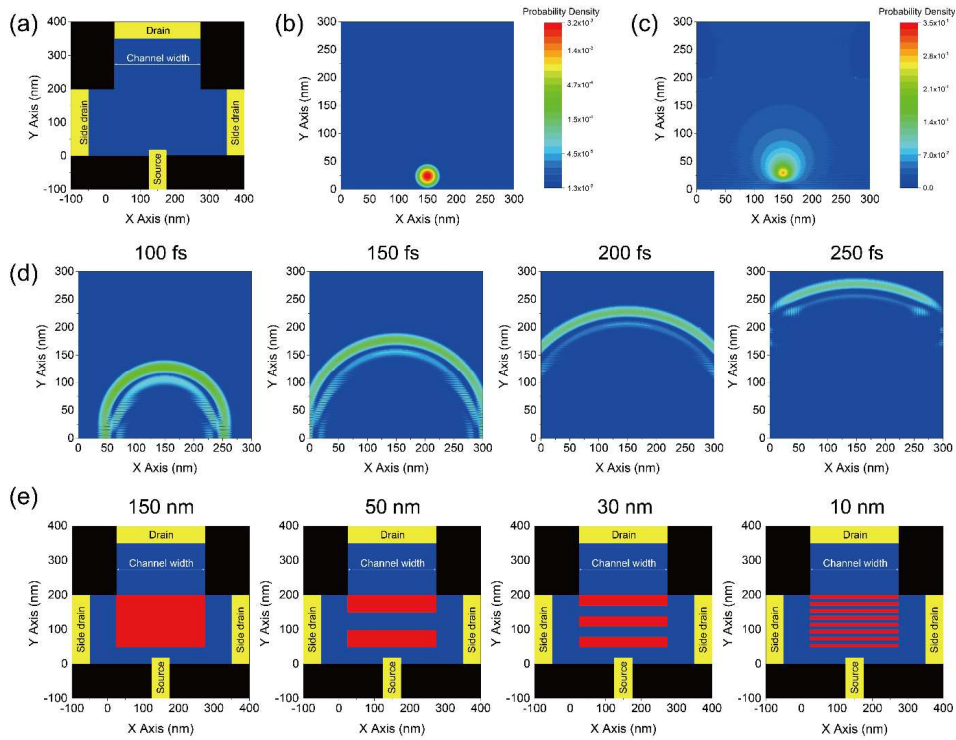


Figure 72. (a) Device geometry of pristine graphene device with channel (blue) on insulating substrate (black) in xy coordinate space. (yellow): metal electrodes of source, drain, and side drain. (b) Electron probability density distribution of Gaussian localized wave packets in pristine graphene at initial with the central wave vector \mathbf{k}_c set by the energy $E(k_c) = E_0 = \hbar v_F |\mathbf{k}_c| = 0.02$ eV of incident electron wave packet. (c) Time-integrated probability density distribution of electron wave packets in the pristine graphene. (d) Time-evolving probability density distributions of electron wave packets in pristine graphene at 100 fs, 150 fs, 200 fs, and 250 fs. (e) Device geometry of superlattice graphene device with channel (blue) on insulating substrate (black) in xy coordinate space. (red): superlattice potential with different half-period lengths (150 nm, 50 nm, 30 nm, and 10 nm).

6.2 Electron Trajectory Incident to Graphene Superlattice Potential

Recalling the electron quantum optics [63-67] in the graphene as discussed in Chapter 1.7.1 and Chapter 1.7.2, the electron trajectory passing through the potential barrier reveals Klein tunneling [68-72] and negative refraction [73-77]. If the incidence is perpendicular to the surface of potential barrier in graphene, the electron can tunnel the potential barrier with probability regardless of its height and width, *i.e.*, the absence of back-scattering [68-72]. In addition to that, owing to the negative refraction [73-77], the angle-dependent transmission [78-82] and the collimation [83-87] can be achieved with the periodic potentials in graphene [88-92], so-called the graphene superlattice [93-97]. The trajectories of electron incident to the graphene superlattice are illustrated in Figure 73 and Figure 74.

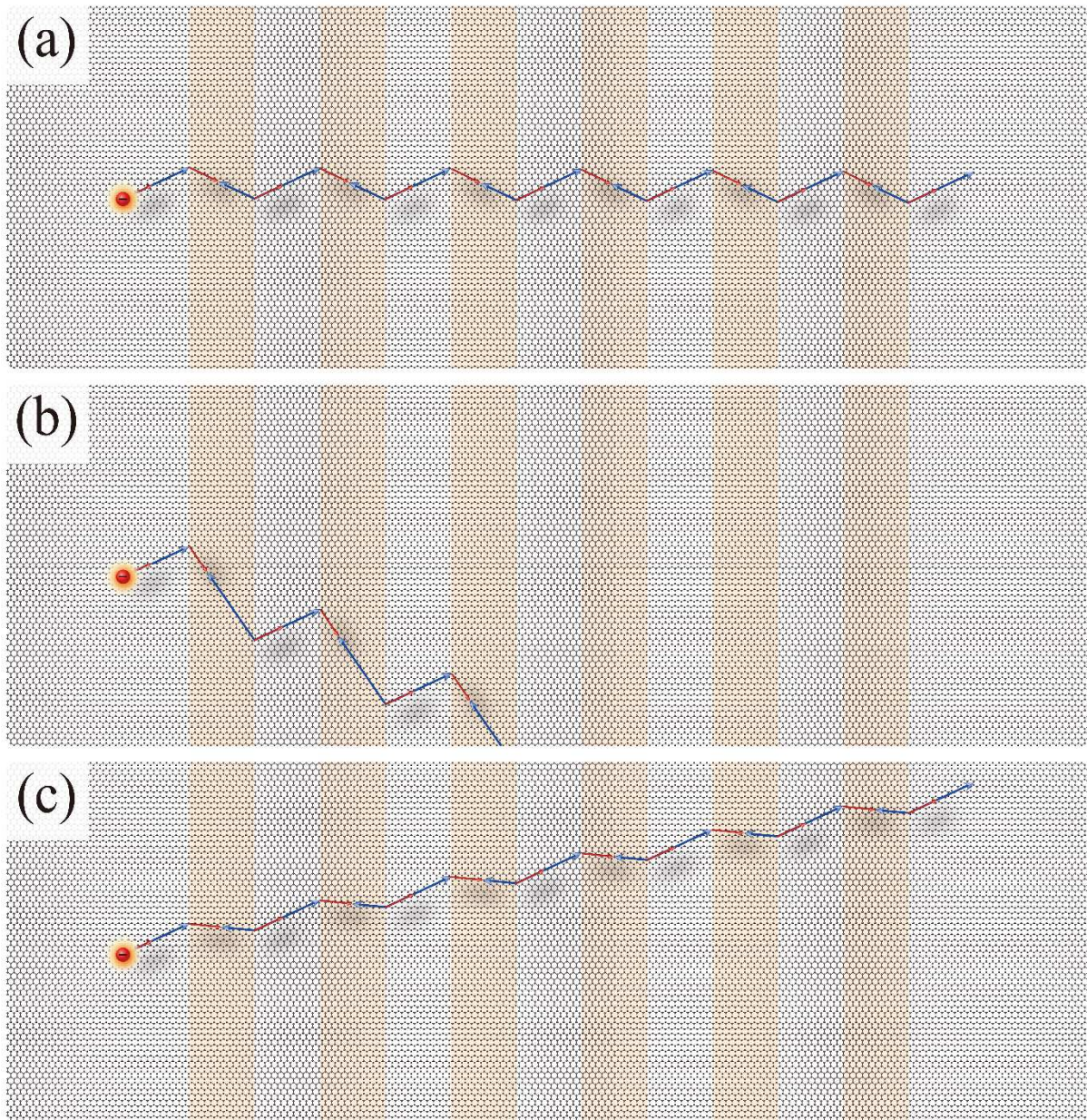


Figure 73. (a,b,c) Schematic of trajectories of electron incident to the graphene superlattice (Chapter 1.7.1 and Chapter 1.7.2). The incident angle is 30° and the magnitude of superlattice potential is moderate (a), extensive (b), minor (c).

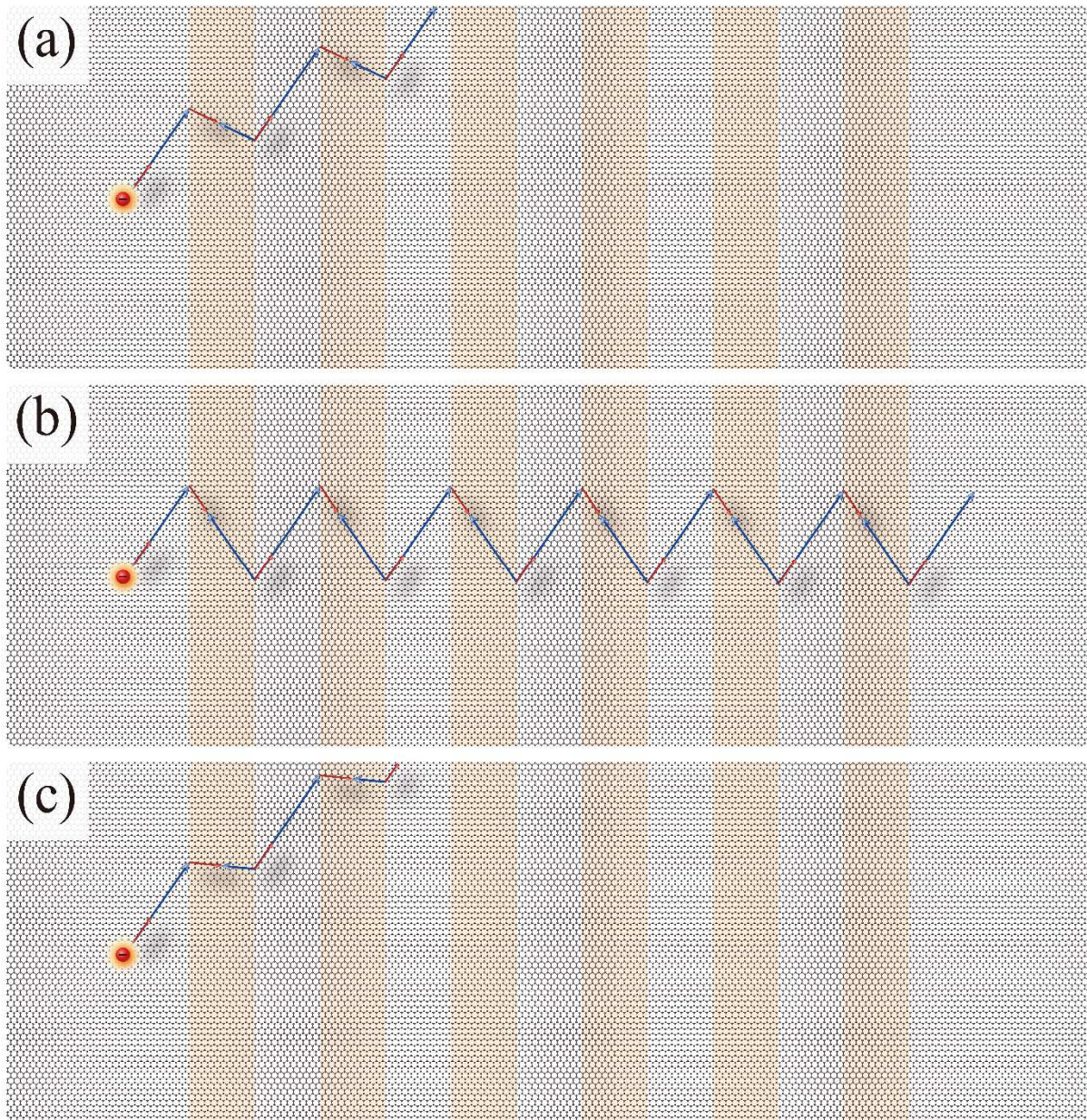


Figure 74. (a,b,c) Schematic of trajectories of electron incident to the graphene superlattice (Chapter 1.7.1 and Chapter 1.7.2). The incident angle is 60° and the magnitude of superlattice potential is moderate (a), extensive (b), minor (c).

6.3 Time-Evolving Electron Probability Distribution in Graphene Superlattice

The Gaussian wave packets Ψ of the massless Dirac fermion in the graphene is given by Equation 60, where A is the wave-function coefficient, k_x is the momentum wave-vector component along the x direction, k_y is that along the y direction, $X = 30$ nm is the spatial extent along the x , $Y = 30$ nm is the spatial extent along the y , s is the band index (1 for the conduction band and -1 for the valence band), $u_{i,j}^n$ is the first row column component, $v_{i,j}^n$ is the second row column component, and is U the potential magnitude. Based on the conservation of total energy and the transverse momentum parallel to the interface, The time-evolution of Gaussian wave packets can be obtained with Equations 61-63, [63-97] by applying the $\hat{H}_{total} \Psi(x, y, \Delta t) = i\hbar \frac{\partial}{\partial t} \Psi(x, y, \Delta t)$ of the time evolution of the wave-function with the energy of an incident electron with the central wave vector \mathbf{k}_c , $\Delta x = \Delta y = 1$ nm, $\Delta t = 0.1$ fs,

$$U(x+2L) = U(x), \text{ and } U(x) = \begin{cases} 0 & (0 < x < L) \\ U & (L < x < 2L) \end{cases}.$$

$$\Psi(x, y, 0) = A \exp[i(k_x x + k_y y)] \exp\left[-\left(\frac{x^2}{2X^2} + \frac{y^2}{2Y^2}\right)\right] \begin{pmatrix} 1 \\ s \exp\left[i \tan^{-1}\left(\frac{k_y}{k_x}\right)\right] \end{pmatrix} = \begin{pmatrix} u_{i,j}^n \\ v_{i,j}^n \end{pmatrix} \quad (60)$$

$$\Psi(x, y, \Delta t) = \begin{pmatrix} 1 + \frac{\Delta t}{i\hbar} U(x) & v_F \Delta t \left(i \frac{\partial}{\partial y} - \frac{\partial}{\partial x} \right) \\ -v_F \Delta t \left(i \frac{\partial}{\partial y} + \frac{\partial}{\partial x} \right) & 1 + \frac{\Delta t}{i\hbar} U(x) \end{pmatrix} \Psi(x, y, 0) \quad (61)$$

$$u_{i,j}^{n+1} = u_{i,j}^{n-1} + \frac{2U_i}{i\hbar} \Delta t u_{i,j}^n + v_F \Delta t \left(i \frac{v_{i,j+1}^n - v_{i,j-1}^n}{\Delta y} - \frac{v_{i+1,j}^n - v_{i-1,j}^n}{\Delta x} \right) \quad (62)$$

$$v_{i,j}^{n+1} = v_{i,j}^{n-1} - v_F \Delta t \left(i \frac{u_{i,j+1}^n - u_{i,j-1}^n}{\Delta y} + \frac{u_{i+1,j}^n - u_{i-1,j}^n}{\Delta x} \right) + \frac{2U_i}{i\hbar} \Delta t v_{i,j}^n \quad (63)$$

Based on the above equations, the transmission coefficient for the electron wave packet incident on the graphene superlattice with the different lengths of half- period within the same channel length is obtained by varying the magnitude of superlattice potential. As shown in Figure 75, the propagation direction and angular spread of electron wave packets strongly depends on superlattice potential magnitude or periodicity.

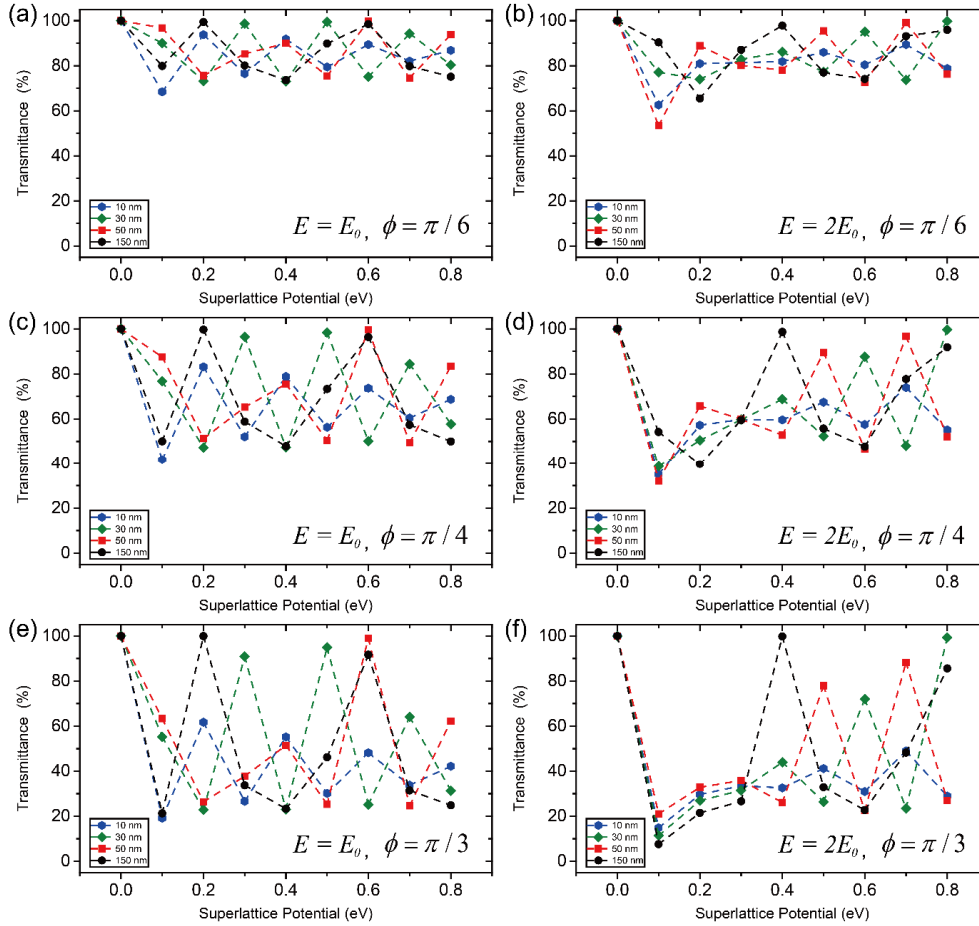


Figure 75. (a-f) Transmission coefficient for the electron wave packet incident on the graphene superlattice with the different lengths of half- period (150 nm, 50 nm, 30 nm, and 10 nm) within the same channel length as a function of the magnitude of superlattice potential. (a) $E(k_c) = E_0$ and $\phi = \frac{\pi}{6}$, (b) $E(k_c) = 2E_0$ and $\phi = \frac{\pi}{6}$, (c) $E(k_c) = E_0$ and $\phi = \frac{\pi}{4}$, (d) $E(k_c) = 2E_0$ and $\phi = \frac{\pi}{4}$, (e) $E(k_c) = E_0$ and $\phi = \frac{\pi}{3}$, and (f) $E(k_c) = 2E_0$ and $\phi = \frac{\pi}{3}$, where $E(k_c)$ is the energy of incident electron wave packet with the central wave vector \mathbf{k}_c and ϕ is the incident angle.

The time-evolving electron probability density distributions in the single-channel multi-drain graphene device under the superlattice potential with the different lengths of half-period (Figure 72e) by varying the applied voltage to the superlattice potential barrier are shown in Figure 76 for 150 nm, Figure 77 for 50 nm, Figure 78 for 30 nm, and Figure 79 for 10 nm. The single-channel multi-drain graphene device is designed with the pristine graphene (Figure 72a) or the superlattice graphene (Figure 72e). Because of the influence of the superlattice on the electron trajectory as described in Figure 73 and Figure 74, the electron wave packets propagate in the collimated form depending on the applied voltage to the superlattice potential barrier, no longer in the form of concentric circles.

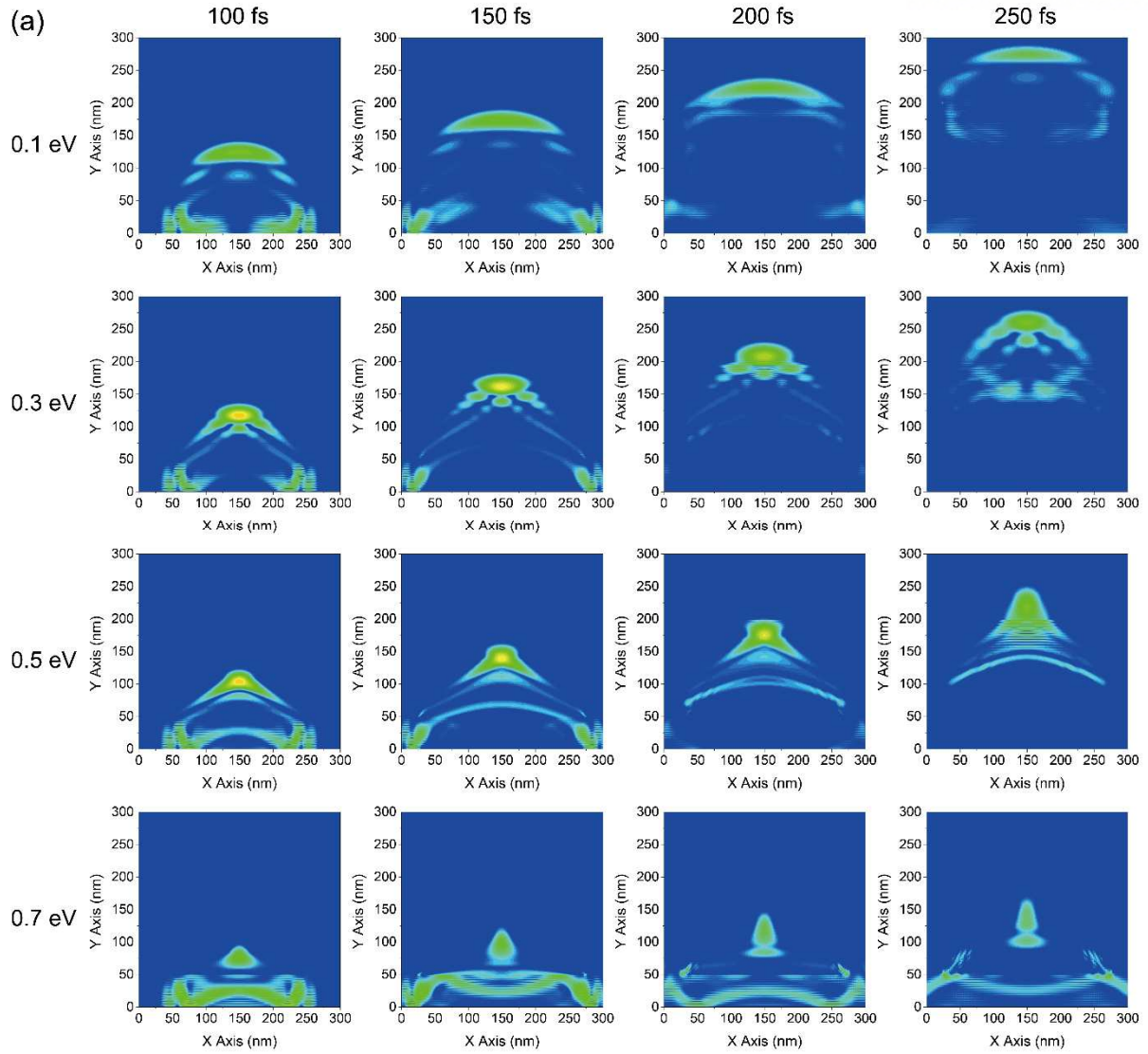


Figure 76. Time-evolving probability density distributions of electron wave packets in the graphene superlattice device with the 150 nm of half-period length by varying the applied voltage (0.1 eV, 0.3 eV, 0.5 eV, and 0.7 eV) to the superlattice potential barrier at 100 fs, 150 fs, 200 fs, and 250 fs.

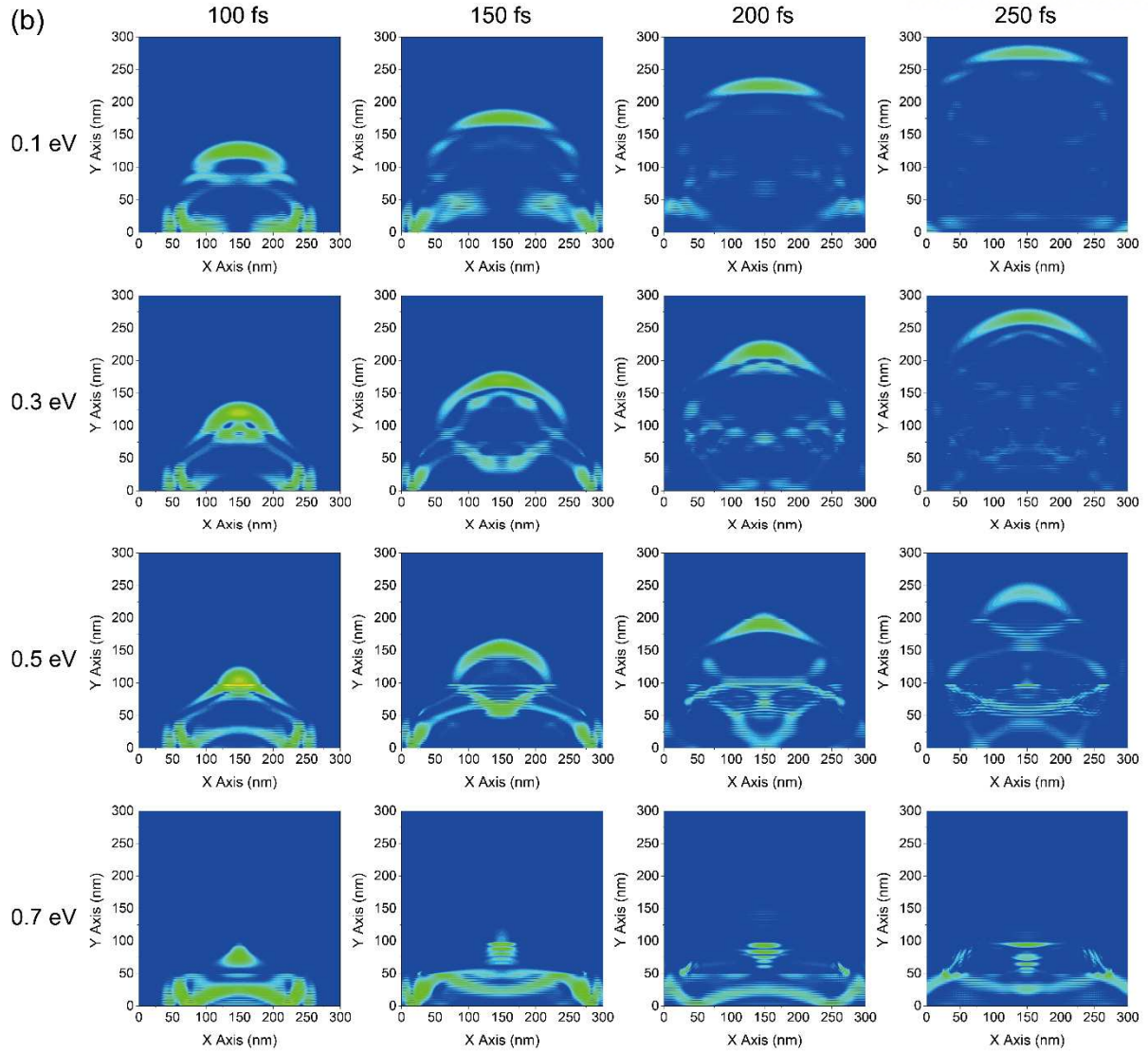


Figure 77. Time-evolving probability density distributions of electron wave packet in the graphene superlattice device with the 50 nm of half-period length by varying the applied voltage (0.1 eV, 0.3 eV, 0.5 eV, and 0.7 eV) to the superlattice potential barrier at 100 fs, 150 fs, 200 fs, and 250 fs.

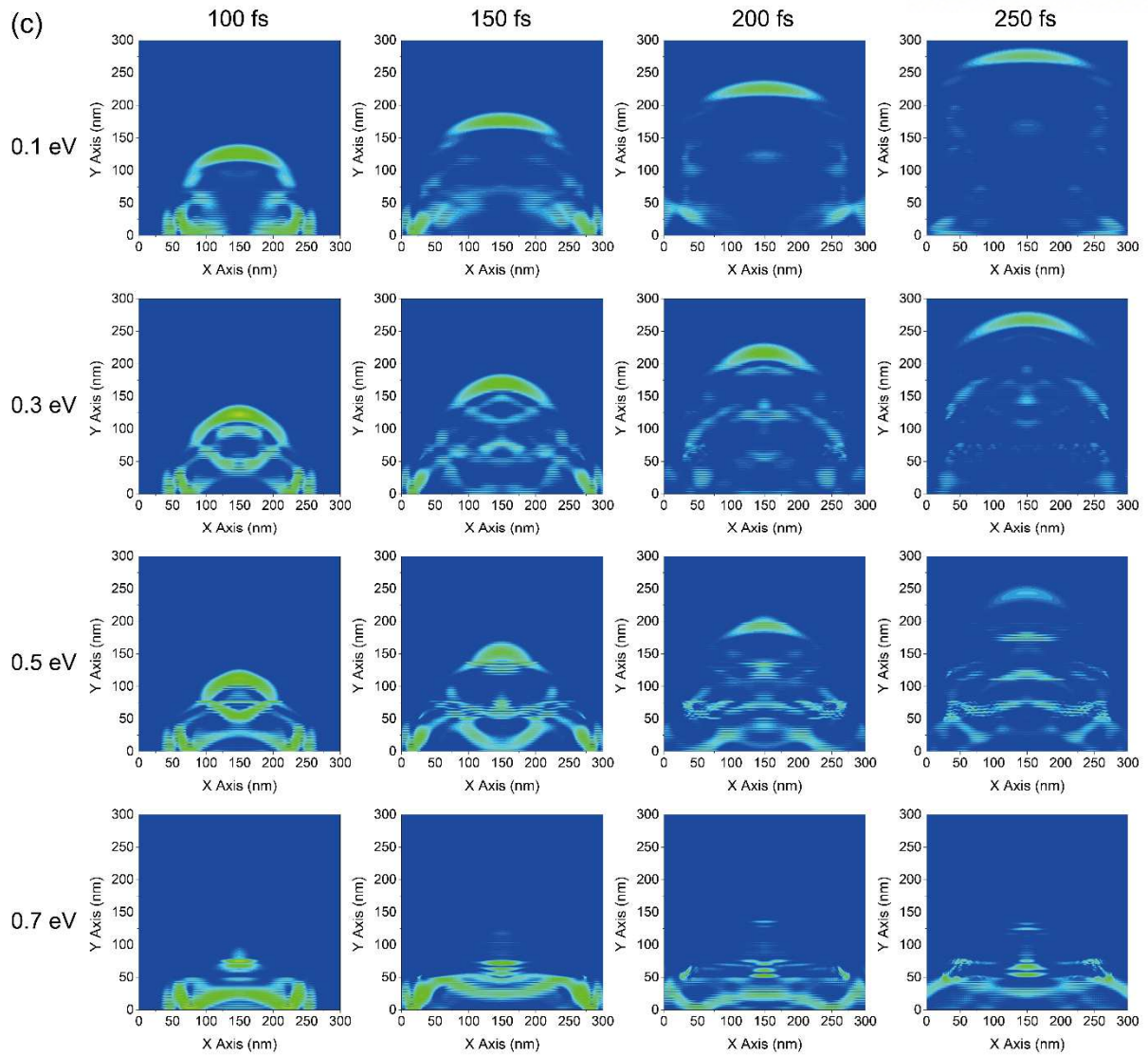


Figure 78. Time-evolving probability density distributions of electron wave packet in the graphene superlattice device with the 30 nm of half-period length by varying the applied voltage (0.1 eV, 0.3 eV, 0.5 eV, and 0.7 eV) to the superlattice potential barrier at 100 fs, 150 fs, 200 fs, and 250 fs.

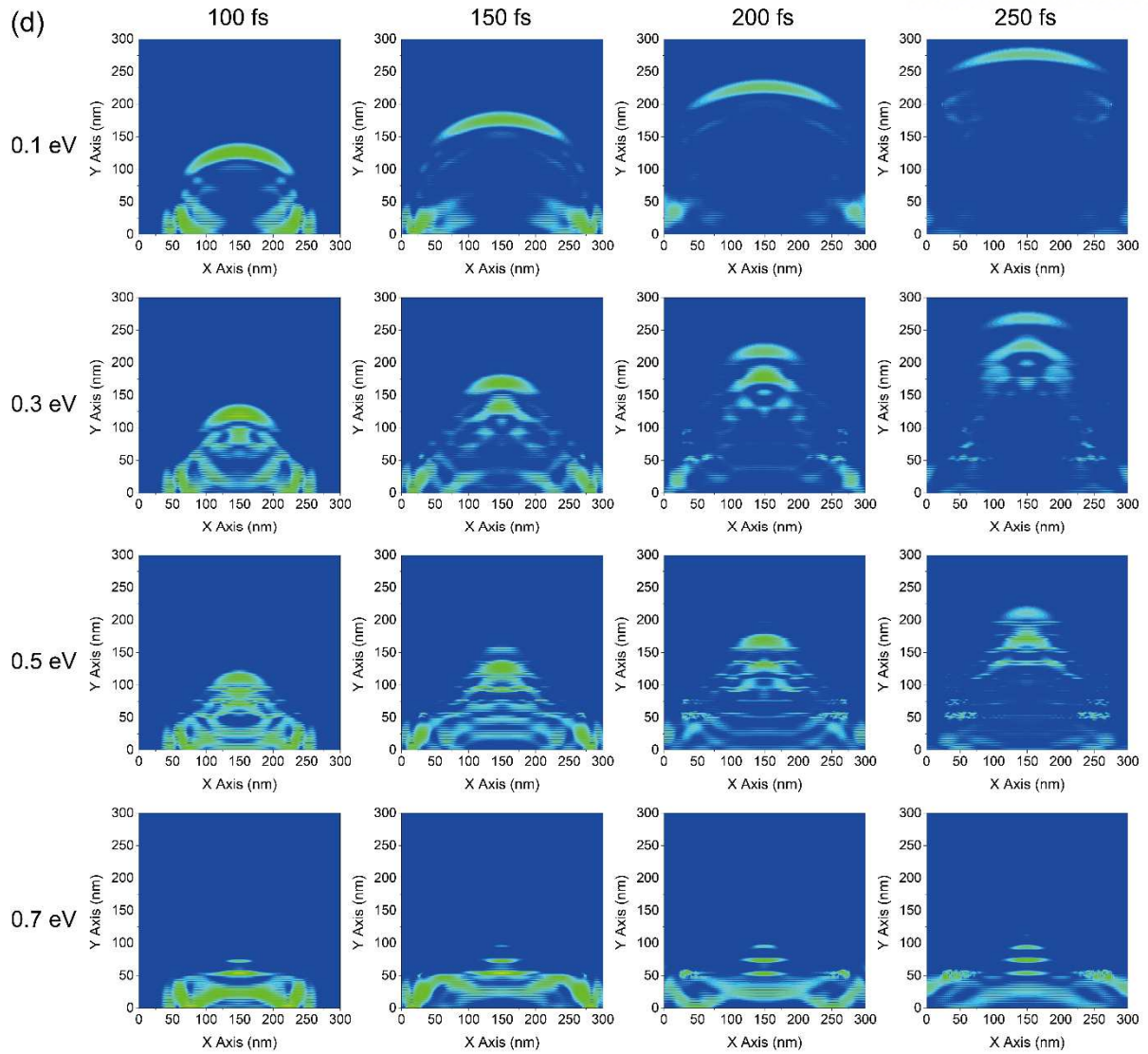


Figure 79. Time-evolving probability density distributions of electron wave packet in the graphene superlattice device with the 10 nm of half-period length by varying the applied voltage (0.1 eV, 0.3 eV, 0.5 eV, and 0.7 eV) to the superlattice potential barrier at 100 fs, 150 fs, 200 fs, and 250 fs.

6.4 Time-Integrated Electron Probability Distribution in Graphene Superlattice

The corresponding time-integrated electron probability density distributions are shown in Figure 80. As seen in the figure, the ratio between the number of electrons flowing into the drain electrode and that of electrons flowing into the side drain can be modulated arbitrarily.

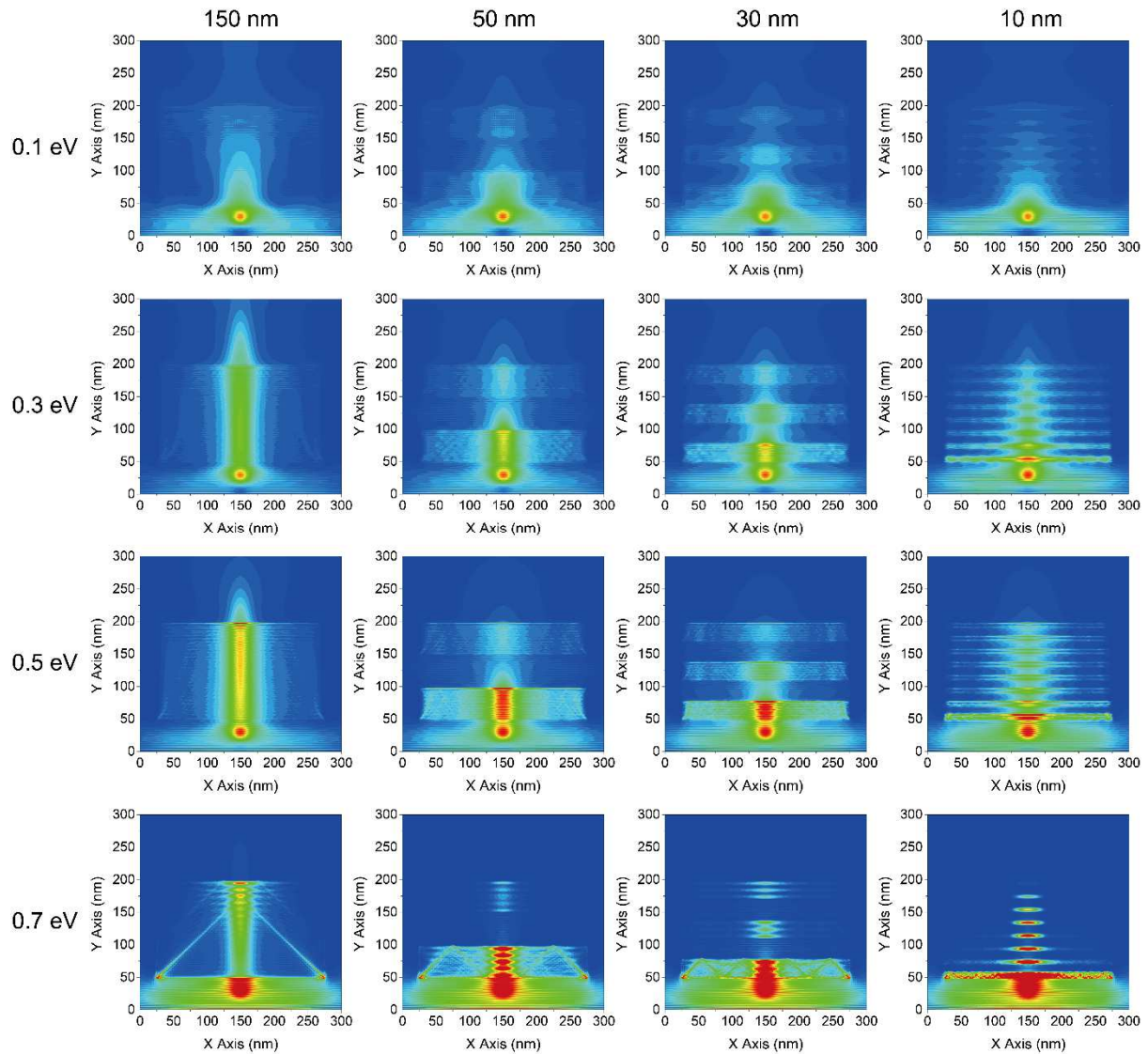


Figure 80. Time-integrated probability density distributions of electron wave packet in the graphene superlattice device with the different lengths of half- period (150 nm, 50 nm, 30 nm, and 10 nm) by varying the applied voltage (0.1 eV, 0.3 eV, 0.5 eV, and 0.7 eV) to the superlattice potential barrier.

6.5 Superlattice-Periodicity-Dependent On-Off Current Ratio

. The electrons flow into either drain or side drain. If the total current is set to be the sum of drain current and side drain currents, the drain current over total current as a function of the magnitude of superlattice potential with the different lengths of half- period is obtained as shown in Figure 81. As a result of comparative analysis of different energies of incident electron wave packets, it is found that the higher energy (Figure 81b and Figure 81d) increases the number of electrons flowing through the drain due to the increased portion of normal incident electrons corresponding to the Klein tunneling compared to the smaller energy (Figure 81a and Figure 81c). Accordingly, for the higher energy, the current ratio to the side drain cannot be sufficiently modulated by varying the applied voltage to the superlattice potential. This implies that the voltage difference between the drain and the source should not be so large in order to better control the current into the side drain. Furthermore, it is difficult for the electrons to reach to the side drain with the wider channel width (Figure 81c and Figure 81d) by considering the angular spread of electron wave packets. Thus, the narrower channel width (Figure 81a and Figure 81b) is more suitable for controlling the electrons reaching to the side drain.

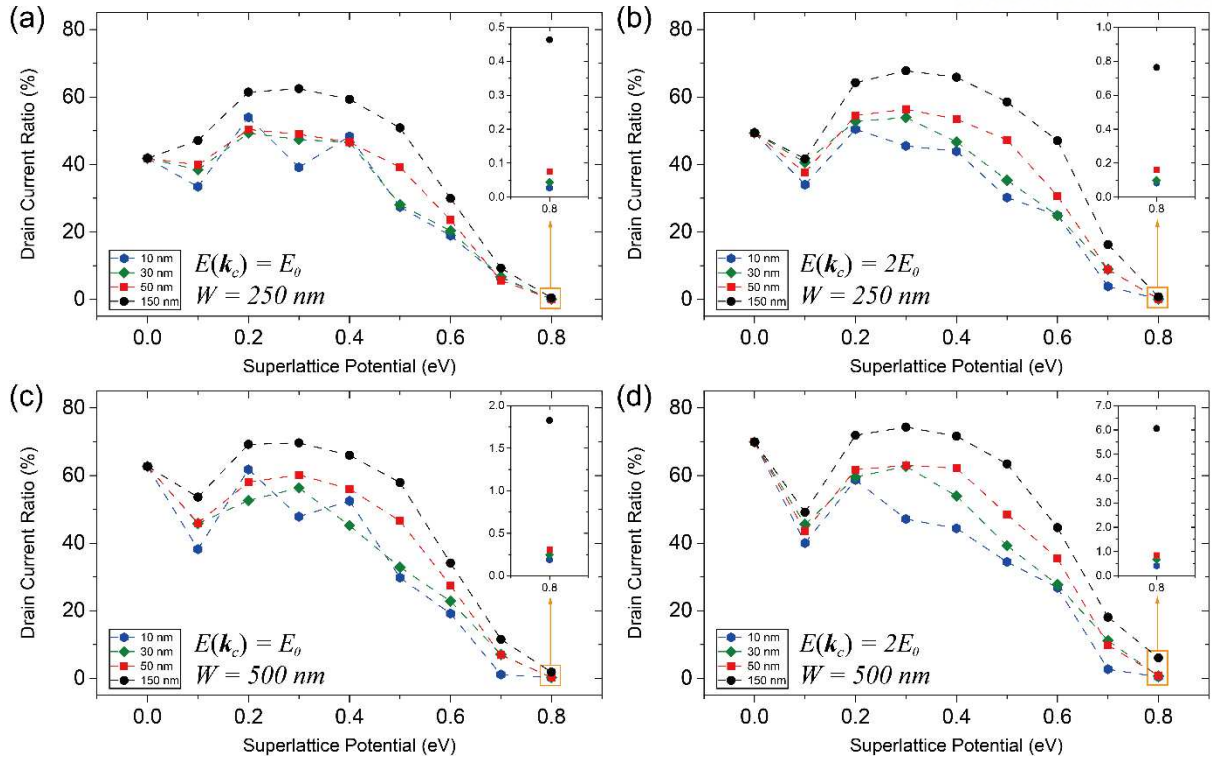


Figure 81. Drain current ratio (drain current over total current) as a function of the magnitude of superlattice potential with the different lengths of half- period (150 nm, 50 nm, 30 nm, and 10 nm). (a) $E(\mathbf{k}_c) = E_0$ and $W = 250$ nm, (b) $E(\mathbf{k}_c) = 2E_0$ and $W = 250$ nm, (c) $E(\mathbf{k}_c) = E_0$ and $W = 500$ nm, (d) $E(\mathbf{k}_c) = 2E_0$ and $W = 500$ nm, where $E(\mathbf{k}_c)$ is the energy of incident electron wave packet with the central wave vector \mathbf{k}_c and W is the channel width. Note: electrons flow into either drain or side drain (total current = drain current + side drain currents).

As shown in Figure 82, the on-off current ratio is obtained as the ratio between the maximum and minimum number of electrons flowing into the drain electrode based on the current ratio in Figure 81. The smaller length of superlattice period and the narrower width of channel reveal the higher switching ratio.

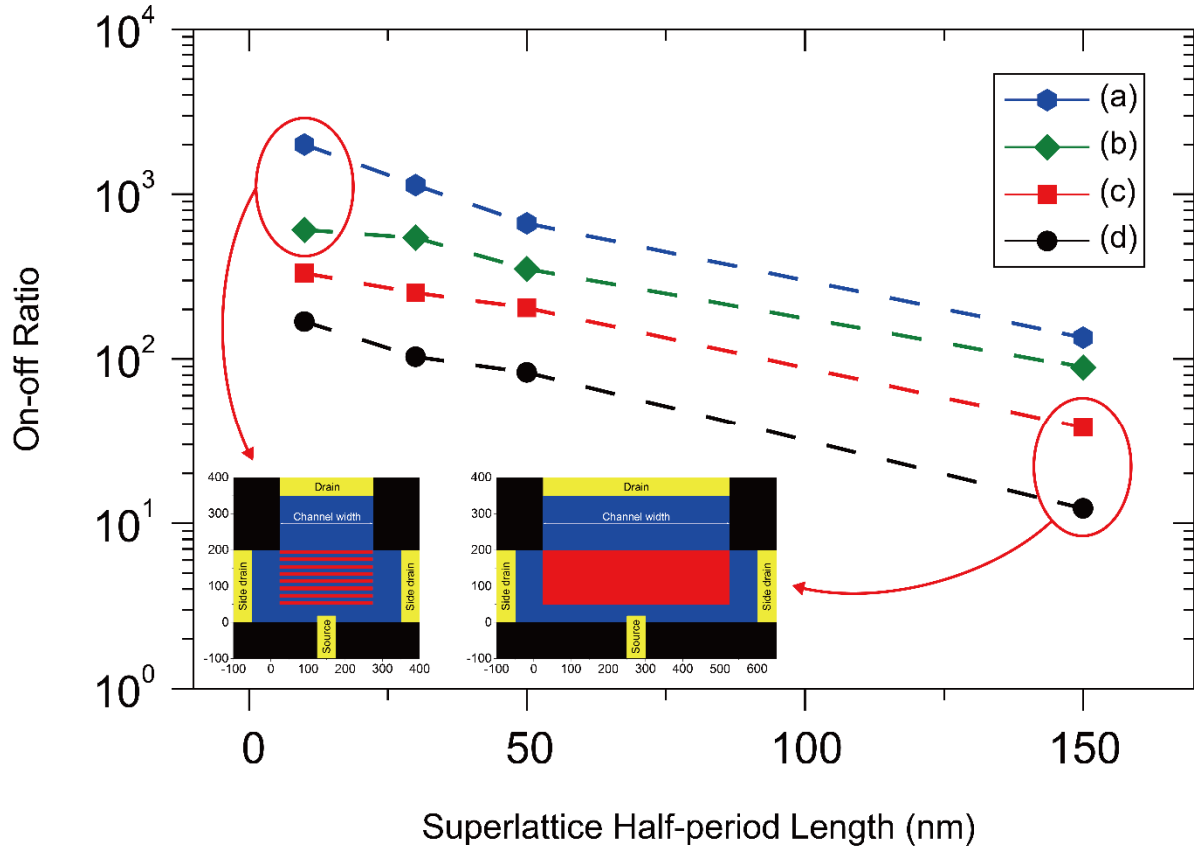


Figure 82. On-off current ratio as a function of the superlattice half-period length. (a) $E(\mathbf{k}_c) = E_0$ and $W = 300$ nm, (b) $E(\mathbf{k}_c) = 2E_0$ and $W = 300$ nm, (c) $E(\mathbf{k}_c) = E_0$ and $W = 600$ nm, (d) $E(\mathbf{k}_c) = 2E_0$ and $W = 600$ nm, where $E(\mathbf{k}_c)$ is the energy of incident electron wave packet with the central wave vector \mathbf{k}_c and W is the channel width.

6.6 Conclusion

It is demonstrated that the single-channel multi-drain graphene device where charge carriers are guided to a specific direction on purpose can be realized with the superlattice structure. Both propagation direction and angular spread of electron wave packet in the single graphene channel can be manipulated just by tuning the magnitude of applied bias or the length of the superlattice period. The ratio between the number of electrons flowing into the drain electrode and that of electrons flowing into the side drain is found to be modulated arbitrarily by tuning the magnitude of the superlattice potential. This work provides a scalable method to fabricate the graphene device large on-off current ratio while maintaining a high carrier mobility of graphene, but also paves the way to control the practically available off-state of the graphene device overcoming the zero band-gap nature.

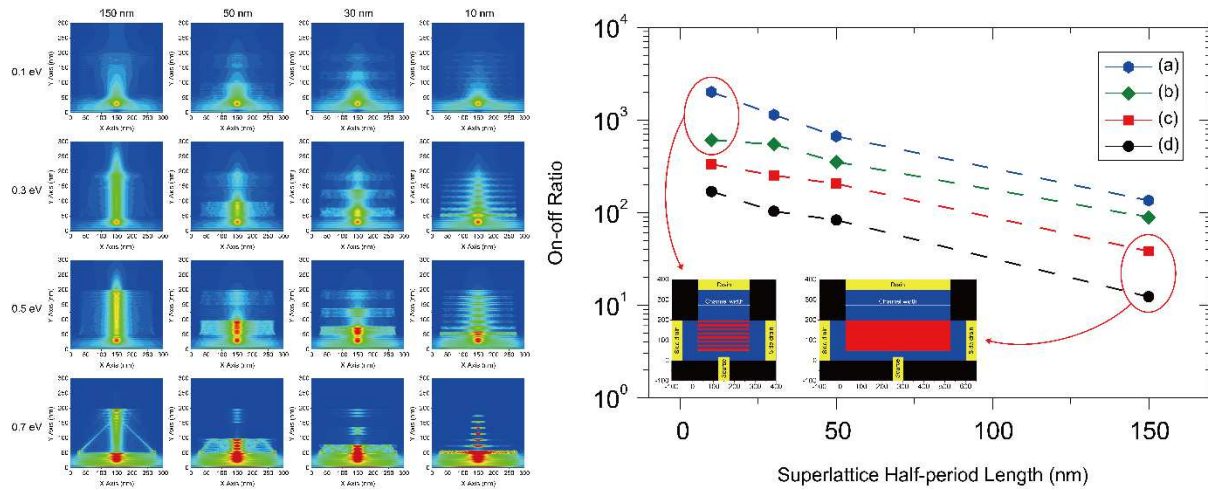


Figure 83. Summary of Chapter 6.

Appendix 1. Graphene Superlattices

The Kronnig-Penny type one-dimensional external periodic potential is introduced in Chapter 6. In the real device application, the alternating n- and p-type doping regions on the graphene channel can be formed by applying the proper voltages on the comb-shaped top gate electrode and the global bottom gate electrode (Figure 84 and Figure 85).

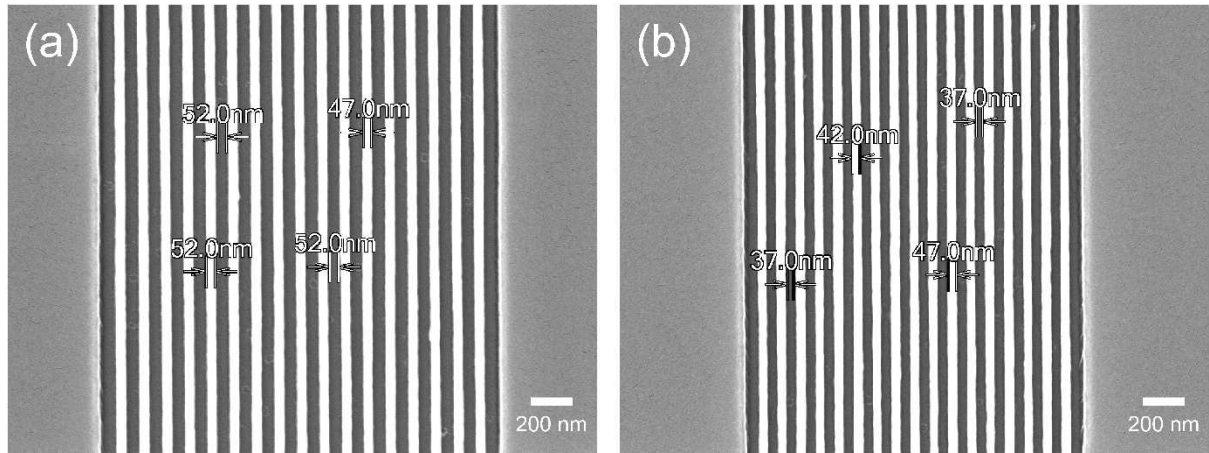


Figure 84. (a,b) Scanning electron microscopy images taken on the Kronnig-Penny type superlattice structure with different lengths of half- period, about 50 nm (a) and 40 nm (b).

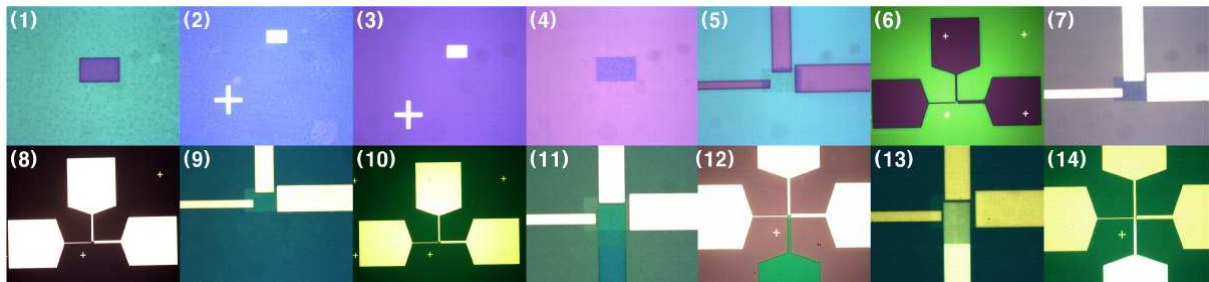


Figure 85. Fabrication process of the graphene superlattice device.

As discussed in Chapter 1.7.2, the well-designed superlattice structure patterned on the graphene channel functions as an interconnected network for current flow [88-97, 443-461]. In addition to the Kronnig-Penny type periodic structure [88-97] with translational invariance, the nanomesh [447-450, 461]. As shown in Figure 86, by addressing artificially patterned square- or triangular superlattices in the graphene channel, the transport pathway of charge carrier can be modulated depending on its width, interval, shape, and periodicity.

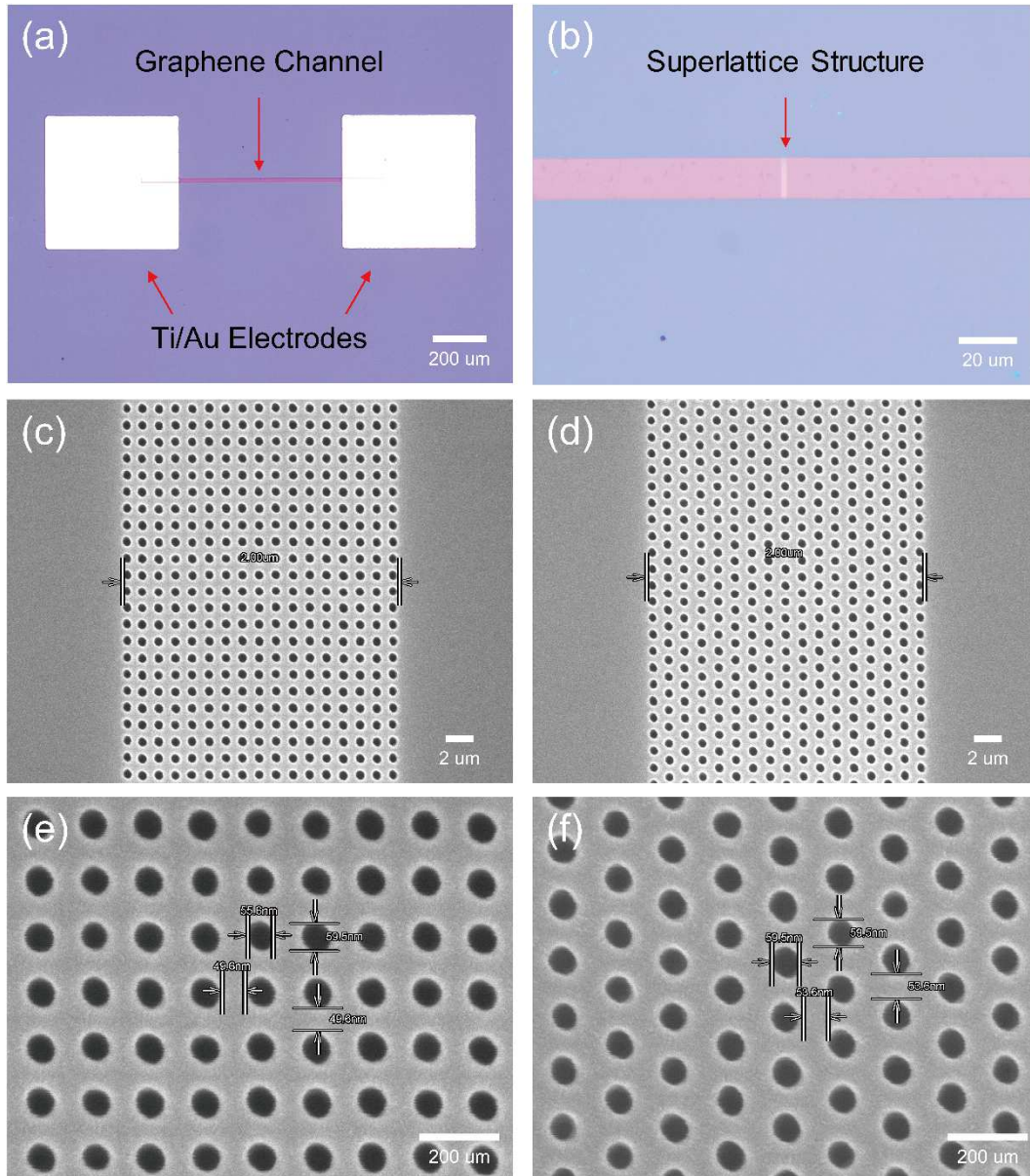


Figure 86. (a,b) Optical images taken on the graphene channel (a) with the superlattice structure (b). (c,e) Scanning electron microscopy images taken on the square superlattice structure. (d,f) Scanning electron microscopy images taken on the triangular superlattice structure.

Appendix 2. Artificial Randomized Defects with Metal Adatom on Graphene

The artificial randomized defects induced by the metal adatom deposition on the graphene channel [147-150] can be interpreted as the graphene superlattice as well.

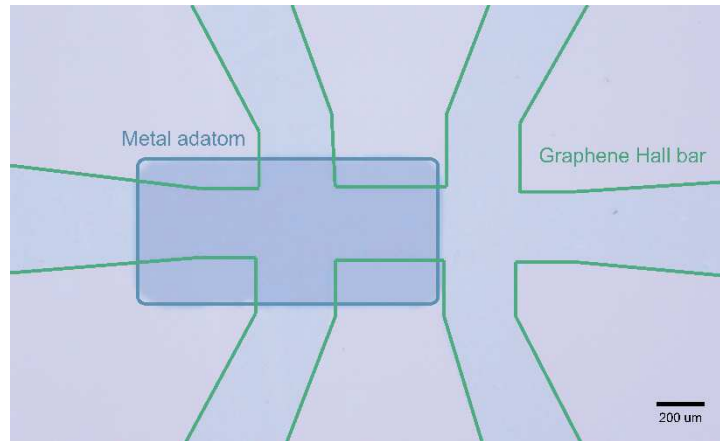


Figure 87. Optical image taken on the graphene Hall bar with the metal adatom.

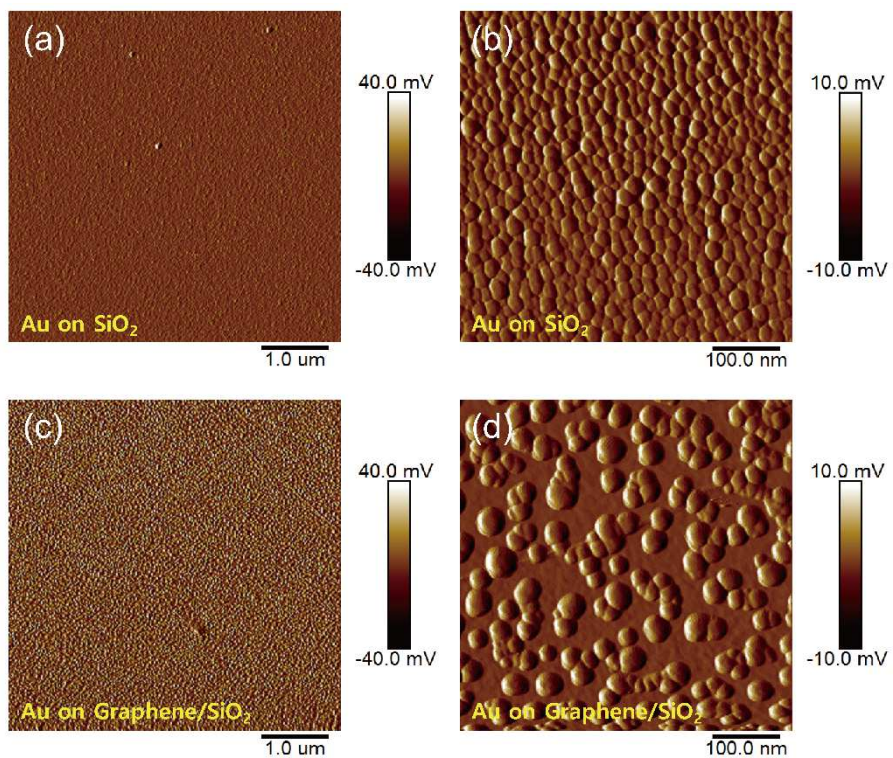


Figure 88. (a-d) Atomic force microscopy images taken on the Au on SiO₂ (a,b) and the Au on graphene/SiO₂ (c,d).

Appendix 3. Graphene Aharonov-Bohm Interferometer

The conductance oscillation involving localization and confinement can be also observed in the graphene with the quantum interference signature [103-122]. The Aharonov-Bohm interferometer is the most typical form for the experimental observation of conductance oscillation [108-112]. Figure 89 shows the pattern of Aharonov-Bohm interferometer with the quantum point contact and the side gate.

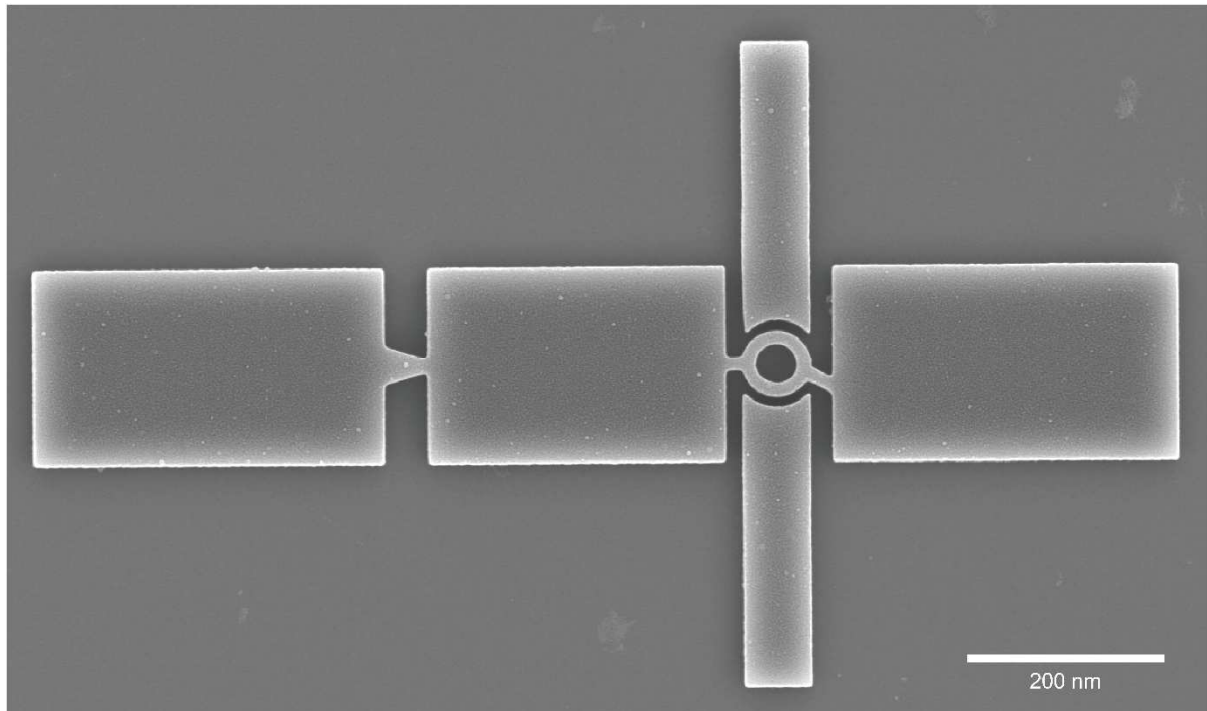


Figure 89. Scanning electron microscopy image taken on the pattern of Aharonov-Bohm interferometer.

Conclusion and Outlook

In this dissertation, two different aspects of the ballistic carrier transport (Chapter 1.2) through the graphene (Chapter 1.3) were studied (Figure 90). Regarding the out-of-plane ballistic carrier transport (Chapter 1.2.2), the ballistic carrier transport across the graphene hetero-interface (Chapter 1.6) was highlighted owing to the IPE measurement (Chapter 1.5) enabling the direct determination of interfacial energy barrier in the entire region of Schottky junction (Chapter 1.4) with the hot carrier transport. By employing the idea of the graphene diffusion barrier (Chapter 1.6.2) and the graphene interlayer (Chapter 1.6.3), the theoretically predicted strong Fermi-level pinning effect at the metal/Si interface was experimentally explored (Chapter 2). Based on the electric dipole layer formed by graphene-metal interaction (Chapter 1.6.1), the uncommon negative Fermi-level pinning effect at the metal/GaAs interface (Chapter 3) was also observed with the graphene interlayer (Chapter 1.6.3), which is readily new discovery of unusual nature in device physics. It was found that the low barrier patches induced by the material intermixing of metal and Si atoms in the conventional metal/Si junction can be blocked (Chapter 2) by the graphene diffusion barrier (Chapter 1.6.2), while the low interface-trap region of GaAs surface can be preserved (Chapter 3) with the graphene diffusion barrier (Chapter 1.6.2). The areal fraction of low barrier patches was estimated with the parallel conduction model (Chapter 1.4.5). The graphene field-effect-transistor gated with the Si depletion layer characterizing the transport properties across the graphene channel or the graphene/Si interface (Chapter 4) revealed the the non-ideal effect of the graphene/Si junction stemming from the recombination process in the small forward bias regime. It was expected that the recombination current (Chapter 1.4.4) due to the hole carriers supplied from p-doped graphene (Chapter 1.3) survives at low temperature, offering the possibility to operate the diode at low temperature (Chapter 4). It was also demonstrated in the lateral size scaling Schottky junction (Chapter 5) with and without graphene interlayer (Chapter 1.6.3) that the charge carrier transport across the interface is mainly attributed to the thermionic emission and the tunneling (Chapter 1.4.4) near the junction edge due to the low effective Schottky barrier height. The result will contribute to solving the leakage current problems in the nanoscale device (Chapter 5). With regard to the in-plane ballistic carrier transport (Chapter 1.2.3), the ballistic carrier transport in the graphene under the superlattice was investigated by importing the useful concepts in electron quantum optics (Chapter 1.7). It was found that the propagation direction and angular spread of electron wave packets can be modulated (Chapter 6) by tuning the superlattice potential magnitude or periodicity. The superlattice combined with the idea of single-channel and multi-drain can be used to control the off-state of graphene device (Chapter 6). In conclusion, the research covered in this dissertation provides a creative perspective on the conductance switching in nano device by implementing exotic quantum phenomenon or designing a new types of architecture.

It is just like steering the electrons to imitate the photons or installing a roadblock to control the current flow. The results will not only stimulate the research interests searching for new physical phenomena in the fields of nanomaterial and device physics but also have enormous implications on the relevant communities in making next-generation electronic device. Further research needs to be required to understand the carrier transport mechanism across the interface or the fundamental physics occurring at the interface.

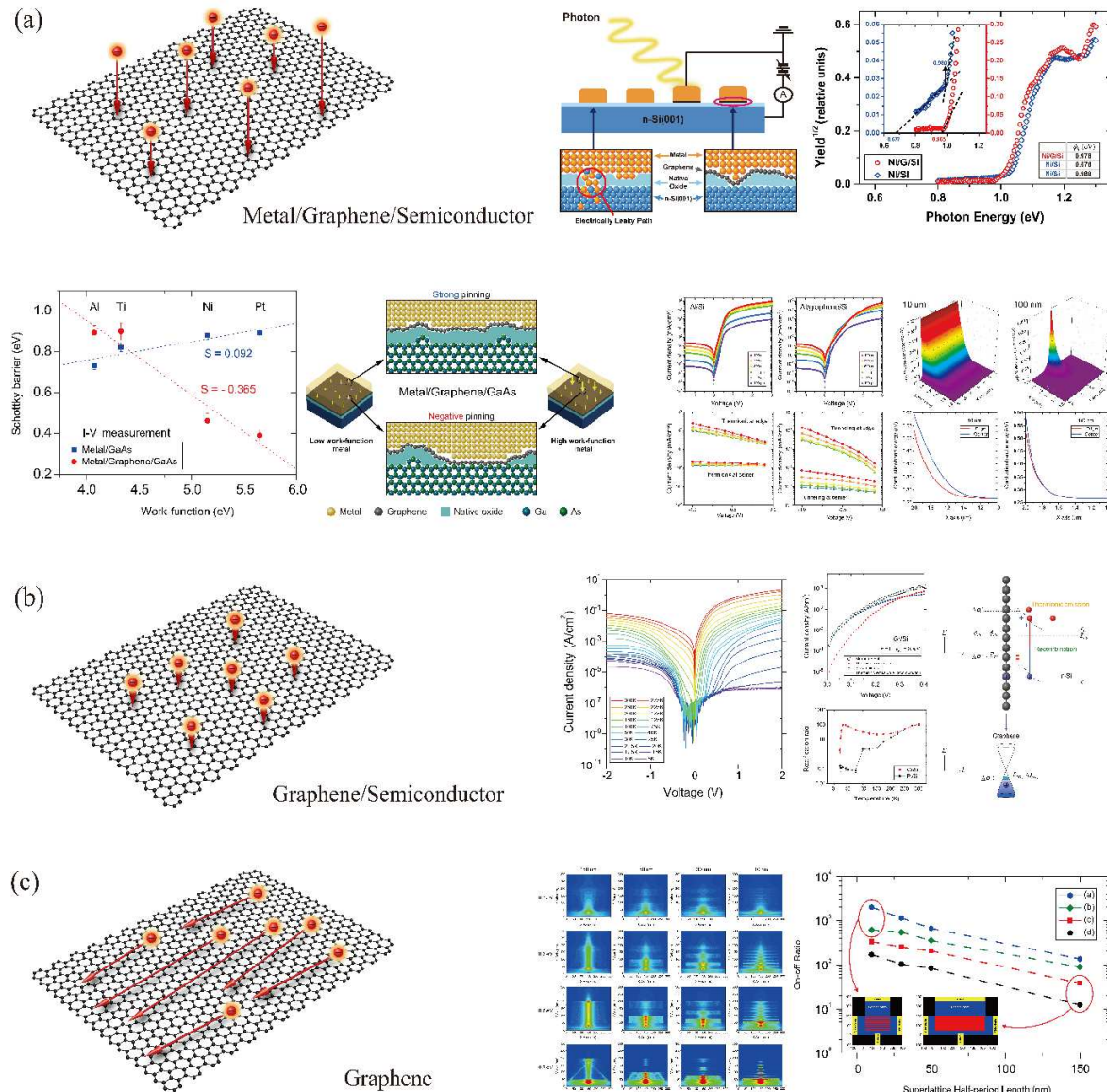


Figure 90. Summary and outline of dissertation. (a,b) Out-of-plane ballistic carrier transport through graphene (a) Ballistic carrier transport across metal/graphene/semiconductor interface. (b) Ballistic carrier transport through graphene/semiconductor interface. (c) Ballistic carrier transport in graphene channel.

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Curriculum Vitae

<Personal Details>

Name: Hoon Hahn Yoon

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<Education>

Ulsan National Institute of Science and Technology, Republic of Korea (03/2014 – Present)

M.S/Ph.D. in Physics, (Advisor: Prof. Kibog Park)

Dissertation: Ballistic Carrier Transport Through Graphene: Out-of-Plane and In-Plane Aspects

Ulsan National Institute of Science and Technology, Republic of Korea (03/2010 – 02/2014)

B. S. in Device Physics, Mechanical System Design and Manufacturing (dual major)

Selected to deliver the graduation speech as a valedictorian.

<Research Experience>

Ulsan National Institute of Science and Technology (03/2014 – Present)

Ph.D. Student in Emergent Materials and Devices Lab (Advisor: Prof. Kibog Park)

■ Research area: Quantum Transport at Interface, Ballistic Carrier Transport across Interface, Graphene Electronics, Internal Photoemission Spectroscopy, Electron Quantum Optics.

Korea Research Institute of Standards and Science (01/2012 – 02/2012)

Intern Researcher in Nano Quantum Research Group, (Supervisor: Dr. Nam Kim)

■ Experience: Quantum-dot Single-Electron Pump Device.

<Technical skills>

Equipment set-up: built several measurement systems in a single probe station.

- Internal Photoemission (IPE) spectroscopy system with Xenon lamp, Monochromator, Optical filter & fiber, Current Amplifier, DAQ, etc.

- Current-Voltage (I–V) measurement system (2-terminal & 3-terminal) with SMU.

- Capacitance-Voltage (C–V) measurement system with LCR meter.

- Low-Temperature Measurement system with helium compressor.

Electrical Measurement: Internal Photoemission (IPE), Current-Voltage (I–V), Capacitance-Voltage (C–V). Low-Temperature Measurement.

Wafer Prep: Si, GaAs (Cleaning, Ohmic contact formation, Wire bonding, etc.)

Graphene Transfer: Wet & Dry.

Etching: Reactive-Ion Etching, Wet Etching.

Growth: Sputtering, Atomic Layer Deposition.

Patterning: Photolithography, E-beam Lithography.

Annealing: Rapid Thermal Annealing.

Structure Analysis: Raman Spectrum, Scanning Electron Microscopy, Ellipsometer.

Calculation: Parallel conduction model for I-V characteristics of an inhomogeneous Schottky contact, Time-evolving probability density of electron wave packets in graphene under superlattice potential, Ballistic carrier transport of injected hot electrons into interface or subsurface.

Programs: Labview, Latex, Origin, Illustrator, Matlab, EndNote, AutoCAD, Word, PowerPoint, Excel.

<Teaching Experience>

Teaching Assistant, Ulsan National Institute of Science and Technology

Advanced Placement Course of General Physics (07/2017 – 01/2018)

General Physics Lab (08/2016 – 12/2016)

Advanced Placement Course of General Physics (07/2016 – 01/2017)

Electromagnetism I (03/2016 – 06/2016)

Advanced Placement Course of General Physics (07/2015 – 01/2016)

Mathematical Physics I (08/2015 – 12/2015)

Mathematical Physics II (03/2015 – 06/2015)

Advanced Placement Course of General Physics (07/2014 – 01/2015)

Modern Physics (08/2014 – 12/2014)

Quantum Mechanics I (03/2014 – 06/2014)

Modern Physics (08/2013 – 12/2013)

General Physics I (03/2013 – 06/2013)

General Physics II (08/2012 – 12/2012)

General Physics I (03/2012 – 06/2012)

Korea International Mathematics Tournament of the Towns (07/2011 – 08/2011)

Advanced Placement Course of General Physics (01/2011 – 02/2011)

General Physics for International Students (12/2010 – 02/2011)

General Physics for International Students (06/2010 – 08/2010)

Mentoring & Tutoring

Prep (UNIST Admission Office Mentoring Program) (03/2012 – 02/2014)

Help Room (General Physics, Calculus) (09/2010 – 06/2012)

<Awards>

Excellence Award for Oral Presentation (2019)

Korean Physical Society Spring Meeting

Korean Physical Society

Oral Presentation Award (2018)

Korea Global Ph.D. Fellow Annual Conference

National Research Foundation of Korea

Excellence Award for Poster Presentation (2018)

Poster presentation in Korean Physical Society Busan-Ulsan-Gyeongnam Branch Meeting

Korean Physical Society

Poster Presentation Award (2017)

Korea Global Ph.D. Fellow Annual Conference

National Research Foundation of Korea

Oral Presentation Award (2016)

Korea Global Ph.D. Fellow Annual Conference

National Research Foundation of Korea

Excellence Award for Poster Presentation (2015)

Poster presentation in Korean Physical Society Spring Meeting

Korean Physical Society

Excellent Award (2012)

Undergraduate Research Program

Korea Foundation for the Advancement of Science and Creativity

Oral Presentation Award (2012)

Physics Festival & Contest

Samsung Advanced Institute of Technology

Oral Presentation Award (2011)

Physics Festival & Contest

Samsung Advanced Institute of Technology

<Honors>

Global Ph.D. Fellowship (03/2015 – Present)

Korean Ministry of Education & National Research Foundation of Korea

National Science and Engineering Scholarship (03/2010 – 02/2014)

Admission fee and full-tuition support for undergraduate studies

National Research Foundation of Korea

Science-gifted Student (04/2004 – 02/2006)

Korea Daegu City Office of Education

<Journal Publications>

Google Scholar: scholar.google.com/citations?user=X1WgkCsAAAAJ

[1] **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Kyuhyung Mo, Gahyun Choi, Hu Young Jeong, Jong Hoon Lee, and Kibog Park*, "Negative Fermi-Level Pinning Effect of Metal/n-GaAs(001) Junction with Graphene Insertion Layer", *ACS Appl. Mater. Interfaces*, 11 (50), 47182-47189 (2019).

[2] Sungchul Jung, **Hoon Hahn Yoon**, Hanbyul Jin, Kyuhyung Mo, Gahyun Choi, Junghyun Lee, Hyesung Park, and Kibog Park*, "Reduction of Water-Molecule-Induced Current-Voltage Hysteresis in Graphene Field Effect Transistor with Semi-Dry Transfer Using Flexible Supporter", *J. Appl. Phys.*, 125 (18), 184302 (2019).

[3] Gahyun Choi, **Hoon Hahn Yoon**, Junhyung Kim, Sungchul Jung, Yonuk Chong, and Kibog Park*, "Multi-Level Capacitive Memory Effect in Metal/Oxide/Floating-Schottky Junction", *J. Korean Phys. Soc.* 74 (10), 979-983 (2019).

[4] Jeongsu Jang, Yangjin Lee, Jun-Yeong Yoon, **Hoon Hahn Yoon**, Jahyun Koo, Jeongheon Choe, Sungho Jeon, Jongbaek Sung, Jungwon Park, Won Chul Lee, Hoonkyung Lee, Hu Young Jeong, Kibog Park, Kwanpyo Kim*, "One-Dimensional Assembly on Two-Dimensions: AuCN Nanowire Epitaxy on Graphene for Hybrid Phototransistors", *Nano Lett.*, 18 (10), 6214-6221 (2018).

[5] **Hoon Hahn Yoon**, Sungchul Jung, Gahyun Choi, Junhyung Kim, Youngeun Jeon, Yong Soo Kim, Hu Young Jeong, Kwanpyo Kim, Soon-Yong Kwon, and Kibog Park*, "Strong Fermi-level Pinning at metal/n-Si(001) Interface Ensured by Forming an Intact Schottky Contact with a Graphene Insertion Layer", *Nano Lett.*, 17 (1), 44-49 (2017).

[6] Gahyun Choi, **Hoon Hahn Yoon**, Sungchul Jung, Youngeun Jeon, Jung Yong Lee, Wook Bahng,

and Kibog Park*, "Schottky Barrier Modulation of Metal/4H-SiC Junction with Thin Interface Spacer Driven by Surface Polarization Charge on 4H-SiC Substrate", *Appl. Phys. Lett.*, 107 (25), 252101 (2015).

[7] **Hoon Hahn Yoon**, Wonho Song, Junhyung Kim, and Kibog Park*, " Low-Temperature Rectifying Graphene/n-Si(001) Schottky Diode due to Recombination of Hole Carriers Supplied from p-doped Graphene", in preparation.

[8] **Hoon Hahn Yoon**, Wonho Song, Junhyung Kim, Gahyun Choi, Sungchul Jung, and Kibog Park*, "Enhanced Contribution of Edge Current in Al/Si and Al/Graphene/Si Junctions with Lateral Size Scaling; Thermionic Emission, Tunneling, and Recombination Aspects", in preparation.

[9] **Hoon Hahn Yoon**, Jung-Yong Lee, Wonho Song, and Kibog Park*, "Electrically-Controlled Carrier Guiding in Single-Channel Multi-Drain Graphene Superlattice Device", in preparation.

[10] **Hoon Hahn Yoon**, Sungchul Jung, Wonho Song, Junhyung Kim, and Kibog Park*, "Charge Carrier Transport Modulation in Graphene with Square and Triangular Superlattices", in preparation.

<Conferences>

[1] **Hoon Hahn Yoon**, Wonho Song, Gahyun Choi, Sungchul Jung, Kyuhyung Mo, Junhyung Kim, and Kibog Park*, "Enhanced Contribution of Edge Tunneling Effect to Current-Voltage Characteristics of Al/Si and Al/Graphene/Si Junctions with Lateral Size Scaling", presented at Korean Physical Society Spring Meeting, Gyeongju, April 24th 2019.

[2] Jeongsu Jang, Yangjin Lee, Jun-Yeong Yoon, **Hoon Hahn Yoon**, Jahyun Koo, Hoonkyung Lee, Kibog Park, Kwanpyo Kim*, "AuCN Nanowire Epitaxy on Graphene for Hybrid Phototransistor", presented at Korean Physical Society Spring Meeting, Gyeongju, April 25th 2019.

[3] Sungchul Jung, **Hoon Hahn Yoon**, Hanbyul Jin, Kyuhyung Mo, Gahyun Choi, Junghyun Lee, Hyesung Park, and Kibog Park*, "Reduction of Current-Voltage Hysteresis in Graphene Field Effect Transistor Achieved with Dry Transfer Using Flexible Tape Supporter", presented at American Physical Society March Meeting, Boston, MA, March 5th 2019.

[4] **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Kyuhyung Mo, Gahyun Choi, Hu Young Jeong, Jong Hoon Lee, and Kibog Park*, "Negative Fermi-Level Pinning Effect Observed in Metal/GaAs Junction with Graphene Insertion Layer", presented at the 26th Korean Conference Semiconductors, Hoengseong, Gangwon-Do, February 15th 2019.

[5] **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Gahyun Choi, Kyuhyung Mo, Kibog Park*, "Negative Fermi-level Pinning Effect Observed in Metal/GaAs Junction with Graphene

Insertion Layer", presented at Korea Global Ph.D. Fellow Annual Conference, Incheon, November 10th 2018.

[6] Gahyun Choi, Wonho Song, Kyuhyung Mo, Sungchul Jung, **Hoon Hahn Yoon**, Junhyung Kim, and Kibog Park*, "Electrical Properties of Metal/4H-SiC Junction Modulated by Graphene Insertion Layer", presented at Korean Physical Society Fall Meeting, Changwon, October 25th 2018.

[7] **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Gahyun Choi, Kyuhyung Mo, Hu Young Jeong, Jong Hoon Lee, and Kibog Park*, "Electrical Properties of Intact Metal/Semiconductor Contact Formed with Graphene Insertion Layer", presented at 2nd Korea LED-Optoelectronics Society Meeting, Kwangju, Korea, August 21st 2018.

[5] Gahyun Choi, Kyuhyung Mo, Sungchul Jung, **Hoon Hahn Yoon**, Wonho Song, Junhyung Kim, and Kibog Park*, "Enhanced Fermi-Level Pinning in Metal/4H-SiC Junction with Graphene Insertion Layer", presented at ICPS 2018 (34th International Conference on the Physics of Semiconductors), Montpellier, France, August 1st 2018.

[9] Sungchul Jung, **Hoon Hahn Yoon**, Junhyung Kim, Jung-Yong Lee, Kyuhyung Mo, and Kibog Park*, "Carrier Transport in Lateral Graphene/Fluorinated-Graphene/Graphene Tunnel Junction Formed with Area-Selective Fluorination", presented at ICPS 2018 (34th International Conference on the Physics of Semiconductors), Montpellier, France, August 1st 2018.

[10] Kibog Park*, **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Gahyun Choi, Kyuhyung Mo, Jong Hoon Lee, and Hu Young Jeong, "Negative Fermi-Level Pinning at Metal/GaAs Junction Occurring with Graphene Insertion Layer", presented at ICPS 2018 (34th International Conference on the Physics of Semiconductors), Montpellier, France, July 31st 2018.

[11] **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Kyuhyung Mo, Gahyun Choi, Hu Young Jeong, Jong Hoon Lee, and Kibog Park*, "Metal-Graphene Interaction Inducing Negative Fermi-level Pinning in Metal/Graphene/n-GaAs(001) Junction", presented at Korean Physical Society Busan-Ulsan-Gyeongnam Branch Meeting, Ulsan, June 15th 2018.

[12] Sungchul Jung, **Hoon Hahn Yoon**, Hanbyul Jin, Kyuhyung Mo, Gahyun Choi, Junghyun Lee, Hyesung Park, and Kibog Park*, "Dry Transfer of Graphene Using Flexible Supporting Layer to Minimize Water Molecule Trapping at Interface", presented at Korean Physical Society Busan-Ulsan-Gyeongnam Branch Meeting, Ulsan, June 15th 2018.

[13] Sungchul Jung, **Hoon Hahn Yoon**, Hanbyul Jin, Kyuhyung Mo, Gahyun Choi, Junghyun Lee, Hyesung Park, and Kibog Park*, "Minimization of Water Molecule Trapping at Graphene/Substrate Interface Using Dry Transfer with Flexible Supporting Layer", presented at Korean Physical Society Spring Meeting, Daejeon, April 25th 2018.

[14] **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Kyuhyung Mo, Hu Young Jeong, Jong Hoon Lee, and Kibog Park*, "Negative Fermi-level Pinning Effect Observed in Metal/GaAs Junction with Graphene Insertion Layer", presented at Korean Physical Society Spring Meeting, Daejeon, April 25th 2018.

[15] **Hoon Hahn Yoon**, Wonho Song, Sungchul Jung, Junhyung Kim, Gahyun Choi, Kyuhyung Mo, Kibog Park*, "Negative Fermi-level Pinning Effect Observed in Metal/GaAs Junction with Graphene Insertion Layer", presented at American Physical Society March Meeting, Los Angeles, CA, March 2018.

[16] **Hoon Hahn Yoon**, Wonho Song, Jung-Yong Lee, and Kibog Park*, "Electrically-Controlled Carrier Guiding in Single-Channel Graphene Device", presented at Korea Global Ph.D. Fellow Annual Conference, Busan, December 15th 2017.

[17] Jeongsu Jang, Yangjin Lee, Jun-Yeong Yoon, **Hoon Hahn Yoon**, Jahyun Koo, Jeongheon Choe, Jungwon Park, Won Chul Lee, Hoonkyung Lee, Hu Young Jeong, Kibog Park, and Kwanpyo Kim*, "Epitaxial Growth of AuCN Nanowires on Graphene for Hybrid Phototransistors", presented at International Conference on Advanced Materials and Device Meeting, Jeju, December 8th 2017.

[18] Jeongsu Jang, Yangjin Lee, Jun-Yeong Yoon, Jeongheon Choe, **Hoon Hahn Yoon**, Hu Young Jeong, Kibog Park, Kwanpyo Kim*, "Phototransistors with Epitaxially-Grown AuCN Nanowires on Graphene", presented at Material Research Society Fall Meeting, Boston Massachusetts, November 30th 2017.

[19] Jeongsu Jang, Yangjin Lee, Jun-Yeong Yoon, **Hoon Hahn Yoon**, Jahyun Koo, Jeongheon Choe, Jungwon Park, Won Chul Lee, Hoonkyung Lee, Hu Young Jeong, Kibog Park, and Kwanpyo Kim*, "Epitaxial Growth of AuCN Nanowires on Graphene for Hybrid Phototransistors", presented at Korean Physical Society Fall Meeting, Gyeongju, October 27th 2017.

[20] **Hoon Hahn Yoon**, Wonho Song, Jung-Yong Lee, and Kibog Park*, "Electrically-Controlled Carrier Guiding in Single-Channel Graphene Device", presented at Korean Physical Society Fall Meeting, Gyeongju, October 26th 2017.

[21] Kibog Park*, **Hoon Hahn Yoon**, Sungchul Jung, Gahyun Choi, Junhyung Kim, Youngeun Jeon, Yong Soo Kim, Hu Young Jeong, Kwanpyo Kim, and Soon-Yong Kwon, "Strong Fermi-Level Pinning at Intact Metal/Si Interface Formed with Graphene Diffusion Barrier", presented at American Physical Society March Meeting, New Orleans, LA, March 14th 2017.

[22] **Hoon Hahn Yoon**, Sungchul Jung, Gahyun Choi, Junhyung Kim, Youngeun Jeon, Yong Soo Kim, Hu Young Jeong, Kwanpyo Kim, Soon-Yong Kwon, and Kibog Park*, "Formation of Intact Schottky Junction with Graphene Diffusion Barrier", presented at Korea Global Ph.D. Fellow Annual

Conference, Sejong, December 21st 2016.

[23] **Hoon Hahn Yoon**, Sungchul Jung, Gahyun Choi, Junhyung Kim, Youngeun Jeon, Yong Soo Kim, Hu Young Jeong, Kwanpyo Kim, Soon-Yong Kwon, and Kibog Park*, "Formation of Intact Schottky Junction with Graphene Diffusion Barrier", presented at Korean Physical Society Fall Meeting, Kwangju, October 19th 2016.

[24] **Hoon Hahn Yoon**, Sungchul Jung, Gahyun Choi, Junhyung Kim, Youngeun Jeon, Yong Soo Kim, Hu Young Jeong, Kwanpyo Kim, Soon-Yong Kwon, and Kibog Park*, "Strong Fermi-Level Pinning at Metal/n-Si(001) Interface Ensured by Forming an Intact Schottky Contact with a Graphene Insertion Layer", presented at Korean Physical Society Busan-Ulsan-Gyeongnam Branch Meeting, Busan, August 22nd 2016.

[25] Sungchul Jung, Junhyoung Kim, **Hoon Hahn Yoon**, Han Byul Jin, Gahyun Choi, Jung-Yong Lee, Daejin Eom, and Kibog Park*, "Multi-Level Memory Effect of CVD Graphene Transferred on SiO₂ by Controlled Hydron Adsorption at Interface", presented at American Physical Society March Meeting, Baltimore, MD, March 17th 2016.

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<Other Activities>

Society of Global Ph.D. Fellows activity

Board committee of Global Ph.D. Fellowship Society (2015 – 2019)

Organized conferences; Global Ph.D. Fellow Annual Conferences (2016 – 2019)

Official website: <https://www.gpfsociety.org/sgpf>

Alumni network activity

The first president of UNIST Alumni Association to foster long-term relationships with UNIST's alumni through various programs. (2016 – 2019)

Official website: <http://alumni.unist.ac.kr/>

Student council activity

The first president of UNIST Graduate Student Association to dedicate in creating an academically inspiring environment for all graduate students. (2016 – 2017)

Official website: <https://www.facebook.com/gsaunist>

Social activity

Member of National Unification Advisory Council in Republic of Korea (2015)

Summer school activity

Summer School of Condensed Matter Physics held by Korea Physical Society and Korea Institute for Advanced Study (2015)

Club activity

The third vice president of UNIST Club Association (2012)

The second president of UNIST math & physics academic club, Elite Of Elites (2011)

Volunteer activity

Lecturer on support center of creative learning & career education in Ulsan, Korea (2014)

Lecturer on career exploration at Bangeojin high school in Ulsan, Korea (2013)

Lecturer on career exploration at Daegun high school in Daegu, Korea (2011)

Acknowledgement

I would like to express my sincere gratitude to all for taking time to read my doctoral dissertation. First of all, I am deeply grateful to my adviser, Prof. Kibog Park. He is a truly honest researcher as well as a great mentor who always give careful advice and sincere counsel with a bright smile. During the first semester of my freshman year, I took a general physics course, and the instructor guided students in developing both rigorous conceptual frameworks and creative insights into physics. I respected him and loved his lectures. After that, I had the chance to take his other courses including quantum mechanics and solid state physics. In his class, he briefly introduced his research topics. I began to pay attention to his descriptions of continuous innovation of device technology and the correlation between physics and engineering. I wanted to participate in his research, and he responded with kindness. After I entered his Emergent Materials and Devices Lab, I was attracted to the research he conducted and his methods in approaching device physics. I have never had a second thought about choosing his lab since I started to work here. I am sorry that I have no more time to receive his instruction. I received the best training to reinforce my strengths and make up for my weaknesses.

I would like to express sincere appreciation to the committee members, Prof. Jiwon Chang, Prof. Kwanpyo Kim, Prof. Kyoung-Duck Park, Prof. Changhee Sohn for taking time on their busy schedule and examining the thesis with thoughtful advice.

Besides, I am deeply thankful that I could work with lab colleagues, Heungseok Go, Dr. Youngeun Jeon, Dr. Hanbyul Jin, Dr. Sungchul Jung, Dr. Gahyun Choi, Jung Yong Lee, Junhyung Kim, Kyuhyung Mo, Wonho Song, Jin Young Park, Jaehyeong Jo, Eunseok Hyun. I will never forget their kind help and deep understanding. Despite my many shortcomings, there were many things that were complemented owing to their efforts.

I would like to also recognize the research collaboration from Prof. Soon-Yong Kwon, Prof. Hu Young Jeong, Jong Hoon Lee, the passionate lecture from Prof. Hai Woong Lee, Prof. Jaeup Kim, Prof. Chae Un Kim, Prof. Noejung Park, Prof. HyungJoon Cho, Prof. EunMi Choi, Prof. Moses Chung, Prof. Cheol-Min Ghim, Prof. Min Sup Hur, Prof. Hosub Jin, Prof. Jinguook Kim, Prof. Jung-Woo Yoo, and the administrative support from Prof. Pann-Ghill Suh, Prof. Hyeon Suk Shin, Prof. Franklin Bien, Prof. Taesung Kim, Hyung-Il Kim, Min-Jae Kim, Lu-Da Lee, Hae-Ra Kang, Kang-O Kim, Taijin Park, Chorok Oh, Jaehyun Kim, Jaewon Han, Mihyang Seok.

Special Thanks

Looking back on time spent at UNIST, I have been along with UNIST for almost 10 years, about one third of my life. Meantime, I could witness the beginning of UNIST and remarkable development of UNIST. Thanks to UNIST, I was able to study in a good environment inspiring academic interests continuously without worrying about school expenses. I am grateful to the all faculties and officials who are always making efforts for development of UNIST and welfare of students.

Growing up with UNIST, I was able to widen my mind, open my eyes to see the world, and enrich my life thanks to the cultural activities that filled me with joyful memories. Just like the wave can pare the rock, the flow of daily life and habits in UNIST became a big wave and carved me. Getting together with UNIST friends and making efforts to accept their diverse ideas was a big learning process. The actions of having heated discussions with them overnight and worrying together about a better future made me what I am now, and gave me a sense of ownership of UNIST. I feel like that I have been assigned a mission to become physicist, scientist, or the other talented one, who can pay back to the social community and contribute to the human lives with personal growth.

Reminding the word “If you want to go fast, go alone, if you want to go far, go together.”, I have participated in almost all of challenging activities, fund-raising donations, and volunteer works led by UNIST’s people. I was really moved by their interest in solving community and global problems. The time spent in UNIST is an unforgettable memory to me, and I was happy because it was spent at UNIST. I could have experienced a deep sense of responsibility and burden, extending the range of obligation from our community to the world. It was a great honor to be selected to deliver the graduation speech as undergraduate valedictorian. I also appreciate to be given the opportunity to lay a foundation stone of the alumni association and contribute to its development. As the number of alumni increases, it is believed that the time will come soon when communication and networking among alumni members needed. I hope to meet again and cooperate with them some day in the future.

I would like to begin thank Seonghwan Kim, Hongmin Kim, Sowon Lim, Cheol Hyeon Park, Dayoon Kang, Kang Taek Lee, Hyeongsun Jeong, Taeyang Yang, Sook Yoon, Yongkyung Oh, Hyo Jung Sim, Woo Cheol Jeon, Yul Hui Shim, Hyunah Kang, Do Young Kim, Joohee Kim, Chan Hoon Choi, Kyoung Hwan Kim, Haeseong Jang, Hyunyong Lee, Kwangmin Kim, Jiyeon Lim, Jonghyun Park, Geun-Woo Lee, Dasom Park, for participating in many activiteis with me and offering insightful suggestions.

I must thank Kyubeen Kwon, JongHyeob Lee, Hyeongju Kim, Bojeong Seo, Jeongsu Jang, Bumsu Kim, Hyeongju Jeon, Chanwoo Park, Sewon Jeong, Hyunki Kim, Youngsang Kong, Hyewon Kang, Chan-Eun Park, Seonga An, Sunmean Kim, Myeonggon Park, E-san Jang, Byongkyu Lee, Sangyeong Jeong, Jiman Hong, Leeyeong Kim, Taeho Seong, Seyeon Yoo, Soosung Kim, Jahae Choi, Seongho

Yoo, Hansol Kim, Changwon Seo, Kyungjin Kwak, Yongjoon Cho, Minji Go, Hyeon Ho Noh, Hakbong Lee, Ji-Eun Lee, Jaewoong Lee, Sejin Jung, Ji-Hoon Ha, Boram Kim, Jaeyeon Yu, Yoo Lim Cheon, Ikjoong Kim, Jaehun Park, Geunsik Bae, Jiyong Cheon, Dayeong Kang, Jeongwoong Park, Seung Wan Yoo, Seongwoo Cho, Kyungdon Choi, Eunseo Kim, Hwanhee Kim, for sharing special memories and experiencing invaluable synergy.

I also had great pleasure of feeling strong solidarity with Jeong Hun Kim, Daehyeon Han, Dongkyu Lee, Jaehui Hwang, Junyoung Park, KyungMan Heo, Byeongmin Kwak, Yungun Kim, Byeong Woo Kim, Min Woo Park, An JeHyun, Bongho Bae, Kyungin Baek, Kwon Eunji, Hyeonseo Nam, Sun Beom Kwon, Jinwon Jang, Jisoo Lee, Gangmin Choe, Sang Woo Kim, Hyungmin Choi, Jaeyun Kim, HoKyung Kim, Mingony Kim, Hyenwoo Jo, Sangseop Song.

I would like to especially thank to Eunku Park, Gyeong-Gyun Ha, Jeongheon Choe, Dongbin Shin, Teyoun Kang, Ryoungwoo Jang, Byung Kyu Na, for helpful discussion. Thanks to their advices, I was able to remind my academic motivation.

I am deeply indebted to Sung Min Lee, Yangjin Lee, Sung Beom Cho, Seongsoo Choi, Hagyoul Bae, Hojun Lee, Min Sun Yi, Jiyong Na, DaeHee Hwang, SeongShick Ryu, Eun-Young Han, Soohwan An, Jin Ho Yun, Jin-Ju Jeong, Kangeun Ko, Heijun Jeong, Ji Eun Bae, Younghyun Lim, Heein Yoon, Seojin Choi, Jun-Ho Choi, Seong-Yeol Kim, for expanding mind about interdisciplinary research.

I gratefully acknowledge the counseling from Seunghoo Jeong, Anjung Lee, Hanvit Kim, Songil Lee, Hak-Hyeon Kim, Jin Hoon Kim, Sung-Ho Kim, Yeonho Chang, Heejae Nam. Their advices were a great help in getting over hardship.

I should not forget to thank my old friends, Changyeol Baek, Hyunjin Song, Hyowon Kim, Hyeongjin Jeon, Kyeonghun Geum, for encouraging me all the time.

Once again, I give sincere thanks to Prof. Kibog Park who has led the way to grow as the true researcher. I could have gained a lot of valuable learning thanks to his delicate advice.

Lastly, thank you, my dear parents, my father Deok Hyun Yoon and my mother Eun Hyang Lee, for sending true love and unwavering support.