Master's Thesis

A Column-parallel Single-Slope ADC with Signal-Dependent Multiple Sampling Technique for CMOS Image Sensor

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List of abbreviations

Number	Abbreviation	Word & Phrase
1	CCD	Charge coupled device
2	CMOS	Complementary metal-oxide semiconductor
3	CIS	CMOS image sensor
4	APS	Active pixel sensor
5	ADC	Analog to digital converter
6	SNR	Signal-to-noise ratio
7	SAR	Successive approximation
8	LSB	Least significant bit
9	MSB	Most significant bit
10	S&H	Sample and hold
11	PPD	Pinned photodiode
12	FD	Floating diffusion
13	DAC	Digital to analog converter
14	SF	Source follower
15	SEL	Selection
16	RST	Reset
17	PWM	Pulse width modulation
18	CDS	Correlated double sampling
19	STD	Standard deviation
20	MS	Multiple sampling
21	I-TOF	Indirect Time-of-flight
22	1H-time	1 Horizontal time (1 row time)
23	MF	Multiple frame
24	DNL	Differential nonlinearity
25	INL	Integral nonlinearity
26	CONV	Conventional
27	Long RST	Long reset
28	Short RST	Short reset
29	TDC	Time-to-digital converter

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Abstract

Both Charge-Coupled Device (CCD) and Complementary Metal-Oxide Semiconductor (CMOS) image sensor have same starting point – they convert light photons into electrons. Recently, CMOS image sensor (CIS) has been developed significantly. CIS is much less expensive to manufacture than CCD sensor. Also, CIS has advantages over high speed, low noise and low power consumption. Therefore, such features can be used for many applications.

In general, CIS has the number of incoming photons dependent noise characteristics. In the bright condition, photon shot noise is dominant in CIS compared with other noise sources. Photon shot noise cannot be reduced by circuit technique in single frame. However, CIS has high SNR in bright condition because the slope of the increase in signal is faster than the slope of increase in noise. But, in the dark condition, photon shot noise is not dominant in CIS. Random noises have dominance In CIS in the dark condition. These effects of noises can be reduced by circuit techniques. In the same way, Indirect Time-of-Flight (I-TOF) sensor has similar characteristics. When it measures long distance, its depth accuracy is reduced because of lack of incoming photons same as CIS in the dark condition. Therefore, same circuit technique can be used for pursuing beneficial effects on CIS and I-TOF sensor.

To increase SNR in CIS, imposing gain in correlated double sampling stage as pre-amplifier. Therefore, it can increase SNR and reducing effects of readout random noises. However, it cannot increase gain highly as we want because of saturation problem and large power consumption. Therefore, it is not an advantageous method of low power systems. Otherwise, the multiple sampling technique had been proposed. It averages out all of the readout random noises by sampling several times [7]. Therefore, noise power is reduced in the inverse of sampling number and in voltage domain, noise rms value is reduced in the inverse of square root of sampling number. However, sampling several times increases readout time which is proportional to sampling number significantly. Therefore, to alleviate trade-offs coming from multiple sampling, several approaches is developed in the past. Typical examples are signal-dependent multiple sampling technique, pseudo multiple sampling technique and conditional multiple sampling technique.

First, the pseudo multiple sampling technique decreases resolution of ADC for keeping conventional readout time [8]. Therefore, all of the pixels will be sampled several times, regardless of the value of those pixel values. Therefore, it has a limitation of effects of multiple sampling because of quantization noise due to large quantization step for achieving larger sampling number.

Second, the signal dependent multiple sampling technique has been proposed [9]. It changes its

sampling number according to pixel values. However, this concept can be achieved after operation of conventional readout. Therefore, it at least doubles readout time compared with conventional one.

Finally, conditional multiple sampling technique has been proposed [10]. Similarly, the number of samplings is changed depending on the pixel value. However, it divides into two cases; the bright condition and the dark condition. Therefore, its boundary errors will be significant in output images.

The proposed ADC can achieve conserving readout time with using multiple ramp generators. Also, it can change the sampling number according to pixel values gradually without sacrificing resolution of ADC [12]. It is composed with column-level digital logic for ramp selection and ripple local counter then size problem is not critical problem. Therefore, it can reduce boundary errors through the sample counter of the intermediate level. With this concept, adjusting the number of ramp generators, depending on the application, it can take the appropriate sampling number and reduces the power consumption consideration. Therefore, proposed ADC is new concept of signal-dependent multiple sampling technique with several ramp generators without sacrificing ramp resolution and readout time.

Chapter 1.

Introduction

1. Solid-state image sensor

The solid-state image sensor has been developed significantly in the last twenty years. Also, under the influence of the 'Fourth Industrial Revolution', The solid-state image sensor is expected to continue its previous rapid growth. The sustained growth in miniaturization of the semiconductor industry and the prevalence of Internet of Things (IoT) had greatly influenced the development of solid-state image sensor. The first solid-state image sensor based on semiconductor was photodiode arrays which accept photons, where photodiodes were directly connected by metal wire which had large capacitance value. Therefore, its readout speed is too slow and noise performance was poor in the past.

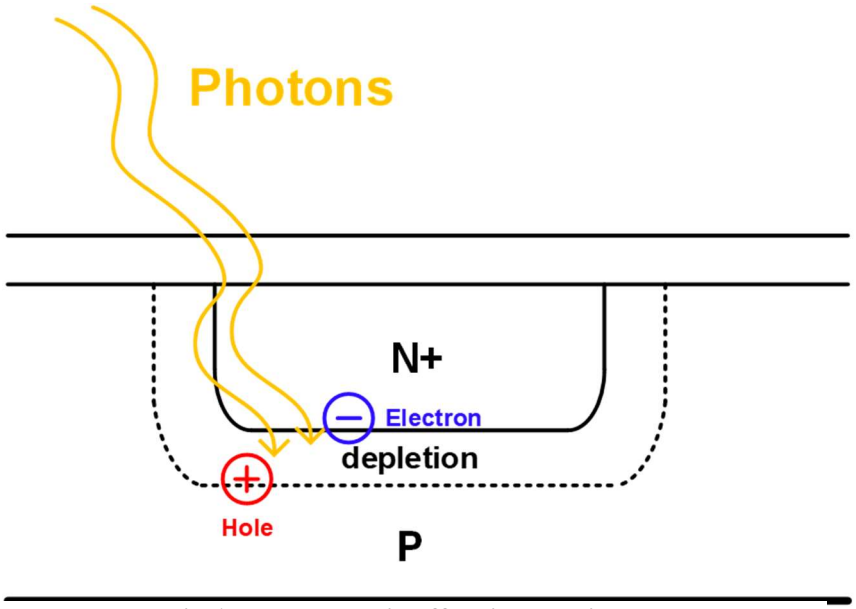


Fig 1. Photoelectric effect in p-n diode

$$E_{ph.} = hf \ (h: flank\ constant, f: frequency\ of\ light)$$

$$E_{elec.} = E_{ph.} - W = hf - W = \frac{1}{2}mv^2 \ (W: Work\ function)$$

Eq 1. The energy equation of photoelectric effect

Before we start to compare two types of image sensor, we should understand the main principle of image sensor. Image sensor is based on photoelectric effect theorized by Albert Einstein. This theory describes the emission of electrons when light hits a material. Therefore, from this phenomenon, Einstein had proposed that a beam of light is not a wave propagating through space, but rather a collection of discrete wave packets like photons. This is how electrons are produced in photodiode when light is emitted. Therefore, as light intensity increases, generated electrons will increase proportional to light intensity. Therefore, detecting and calculating light intensity by counting the number of electrons generated by photons is main function of image sensor. However, there are two methods for counting the number of electrons. To put it simply, one method is that calculating the number of electrons formed to charge domain and other method is that calculating it from voltage domain. Therefore, we should understand the pros and cons of those two methods.

In 1969, Willard S. Boyle and George E. Smith of the AT&T Bell laboratory developed the world's first charge transfer technology. Major principle is that electric charge on surface of semiconductor is transferred from one storage capacitor to the next. This principle served as the basis of the development of CCD sensors. Strictly, CCD is a device that moves charges in a broader sense, usually moving charges within a device into areas where they can be manipulated (digitalized, etc.). Detail method is described in below. After that, the charge transferred from each pixel is sequentially shifted to single output stage. In the output stage, charge is converted to voltage domain by op-amplifier and this voltage value is sampled by analog-to-digital converter to make digital image based on its voltage value. By transferring charge to single output, it has very high homogeneity between each pixel value and good noise performance. However, to operate CCD sensors, voltages from 10V to 20V are needed. Because large current value is needed to charge and discharge capacitance which value is up to nano farads within nanoseconds. Therefore, CCD sensors require large power consumption. This disadvantage is main critical point of using CCD sensors in these days. Therefore, from this critical disadvantage, CMOS image sensors which are using APS pixel, can have a chance to become pervasive in solid-state image sensor market.

Basically, Principle of CMOS image sensor (CIS) had been proposed to 1960s. However, CIS performance was worse than that of CCD sensor. Although CIS had advantages in inherently lower production costs and lower power consumption compared to CCD sensor, they were significantly disadvantageous to picture quality compared to CCD sensor in the early 2000s. Therefore, CIS are used most of the cell phone cameras or CCTVs not DSLR. However, as the CMOS process is developed, in other words the performance APS pixel based on CMOS technology has been

developed significantly due to the steady miniaturization in microelectronics and photodiode arrays. In contrast to the previous photodiode arrays and CCDs, APS pixels have their own voltage amplifier which can convert charge value to voltage domain. From this feature, photodiode which has small photocurrent value can drive metal wires which have large capacitance by using in-pixel amplifier rather than connecting photodiode with metal wires directly. However, CIS have fixed pattern noise (FPN) because of process variations (oxide thickness, size of transistor, doping concentration) from the local voltage amplifier. This noise deteriorates performances of CIS. Unlike CCDs, by imposing selection switch into each pixel, we can select our regions of interest (ROI) by controlling row and column selector.

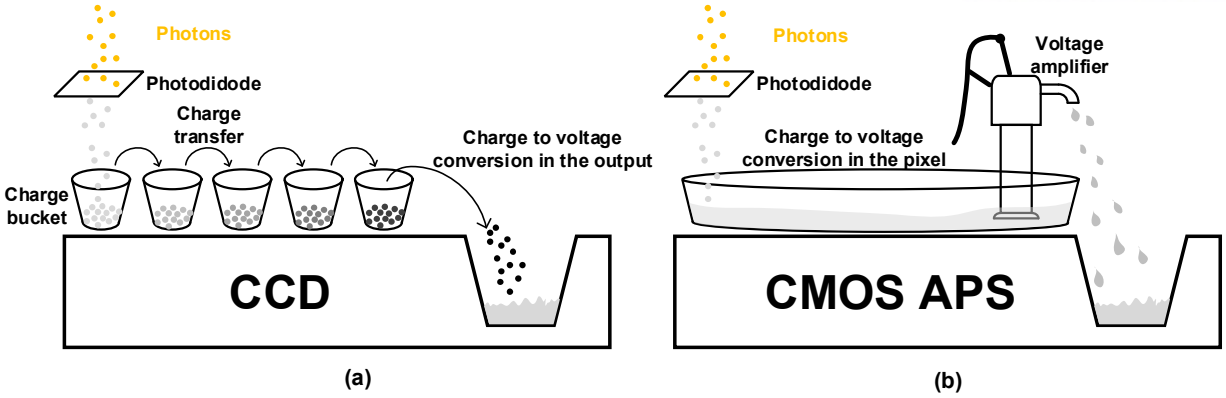


Fig 2. CCD and CMOS operation principle with hydrostatic equivalent

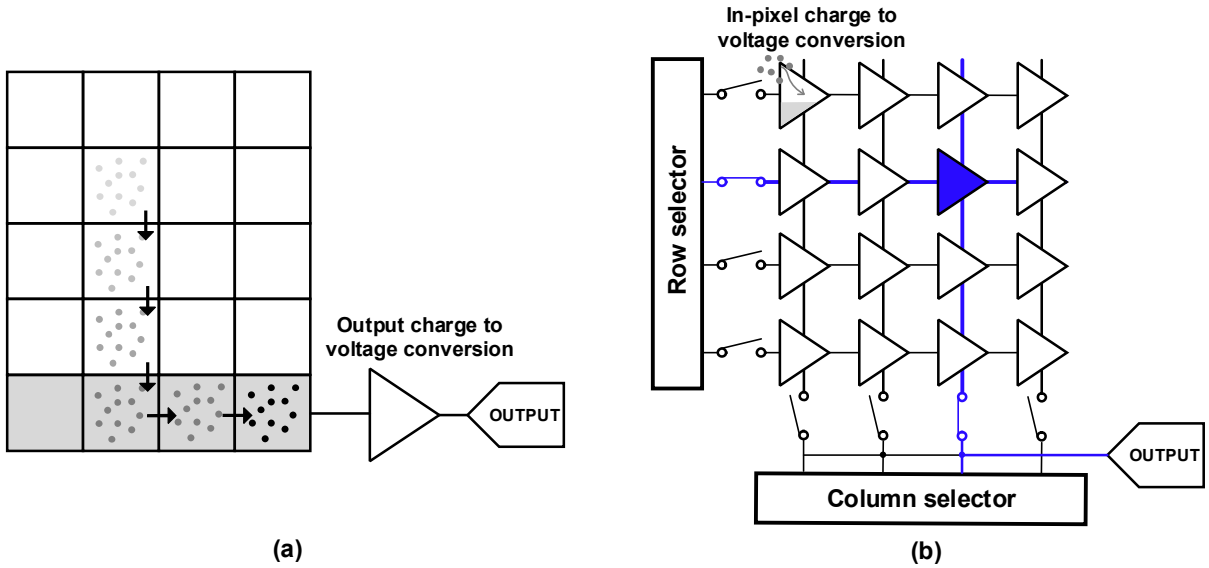


Fig 3. CCD and CMOS APS pixel array operation principle

The main difference between CCDs and CMOS APS pixels is described above figures. In figure 2, Its operation is described by hydrostatic equivalent. Let assume circle figure is electron or photon and water drop is voltage. In CCDs (Fig1-1 (a)), the photodiodes receive photons and then generate electrons. The charge bucket holds its their own generated electrons. After that, when readout stage, its electrons in the bucket are transferred to next bucket in charge domain until final output stage like analog shift register. At the final output stage, electrons transferred to output stage are converted voltage value by one amplifier as described in Fig1-2 (a). Therefore, its readout speed is limited due to using only sone amplifier at output stage. However, its noise performance is better than CIS because of homogeneity from using one amplifier. The important technique in CCDs is transferring electrons to next charge bucket without any loss and noise. For example, Let assume transfer efficiency is 99% and it needs 100 times of transfer to reach output stage. The last remaining charges are only $(99\%)^{100} \approx 36.6\%$. Therefore, increasing transfer efficiency over 99% ($\approx 99.999)\%$ is the most important technique in CCDs.

In contrast, CMOS APS pixel can convert electrons(charges) to voltage in each pixel in Fig 1-1(b). In other words, its pixel output is voltage domain which is main difference between CCD. Therefore, process variations in each pixel deteriorate image results directly. From this feature, In Fig1-2(b), CMOS APS pixel array can be composed with row and column selectors. Therefore, the image information can be directly connected to output.

Both type of solid-state image sensor (CCD, CMOS APS pixel) can be realized based on Metal Oxide Semiconductor (MOS) technologies. However, its development is somewhat different though having same origin. CCD technology is focusing on increasing transfer efficiency in charge domain and CMOS APS pixel technology is focusing on development of photodiode and low noise pixel and readout circuitry. Therefore, in these days, the performance of the CIS is gradually close or over to that of the CCD sensor and the advantages (high speed, low power consumption, ROI) are highlighted, the solid-state markets are gradually changed from CCD sensor to CIS in early 2010.

Feature	CCD	CMOS
Pixel output	Electrons (charge)	Voltage
Chip output	Voltage (analog)	Bits (digital)
Fill factor	High	Moderate
Amp. mismatch	N/A	Moderate
System noise	Low	Moderate
System complexity	High	Low
Sensor complexity	Low	High
Responsivity	Moderate	Slightly better
Dynamic range	High	Moderate
Uniformity	High	Low to moderate
Speed	Moderate to high	Higher
Biasing and Clocking	Multiple, higher voltage	Single, lower voltage

Table 1. Comparison table about CCD vs CMOS APS

2. Low light imaging

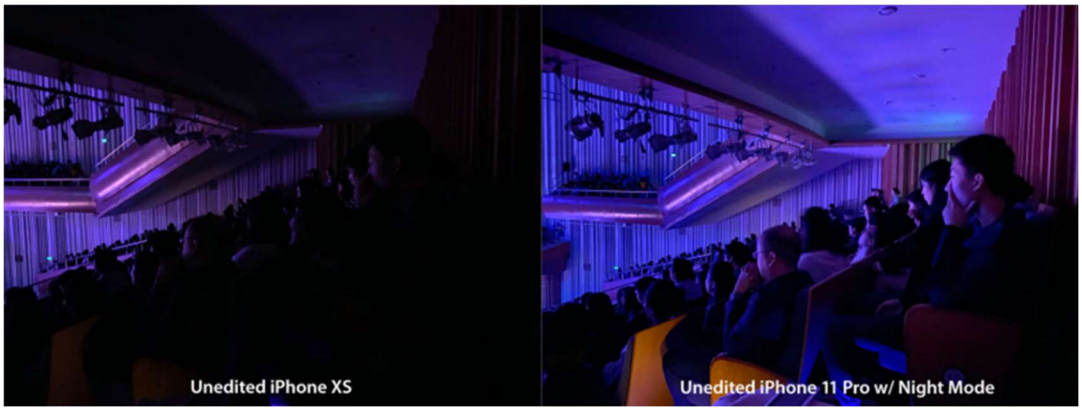


Fig 4. Examples of low light imaging (left side: low SNR & Right side: high SNR)

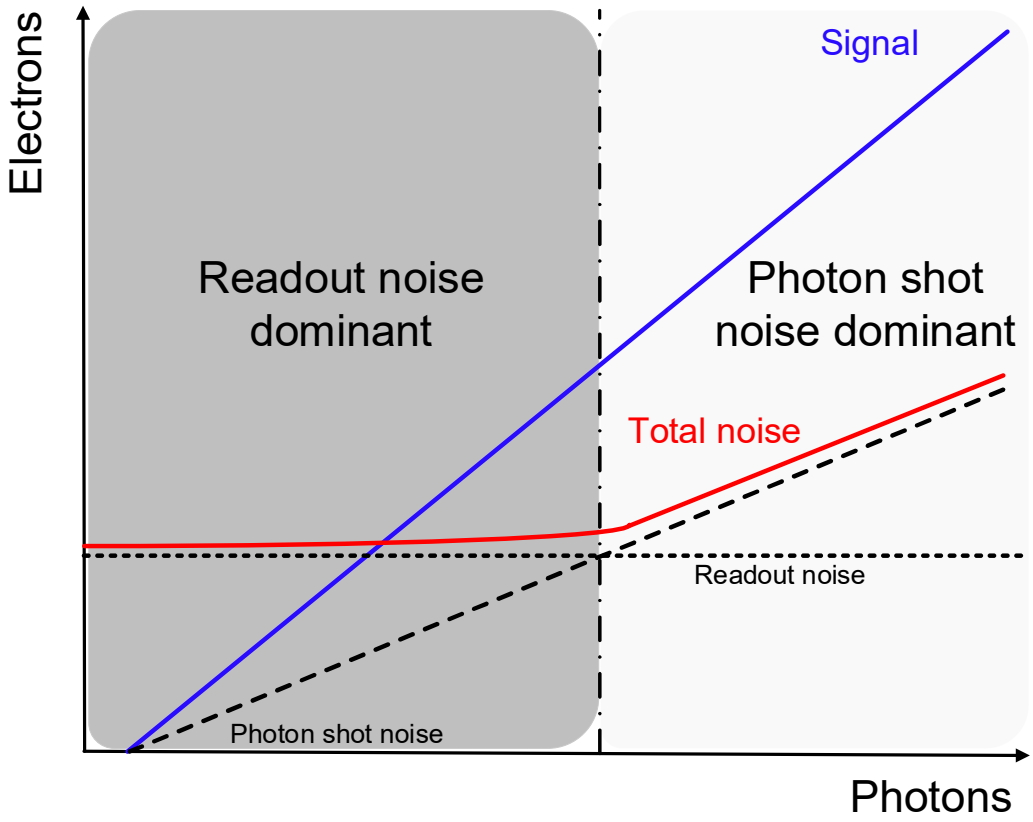


Fig 5. Noise characteristic curves of CMOS image sensor

Recently, many people want to get good quality of image in the dark conditions. As we know, the image quality in the low light condition is very poor comparing with one in bright condition. Therefore, research for low light imaging is being conducted in field of image sensors [16] and [17].

The reason for poor image quality in the dark conditions can be seen form the graph above. In the bright conditions, in other words, if the number of incoming photons is large, SNR is very high. Therefore, we can get a good image quality. However, on the contrary, it has low SNR characteristics in the dark

conditions. Thus, in the dark conditions, there is no choice but to produce a noisy image in CIS. Therefore, to increase SNR in low light condition, pixel level and readout circuit level researches are under way in industry.

3. Research motivation

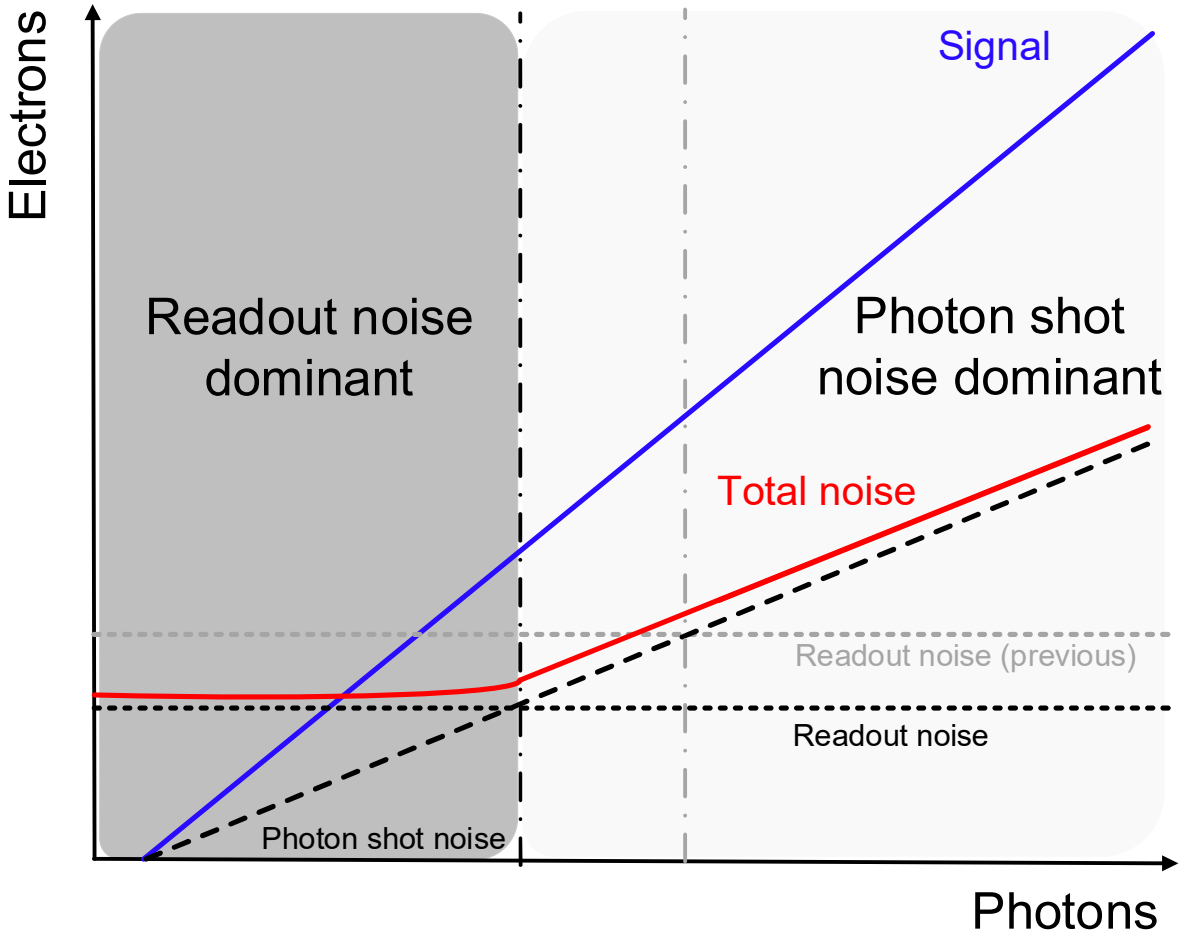


Fig 6. Noise characteristics with suppression readout noise in CMOS image sensor

For low light imaging, suppression readout nose in the dark conditions is needed. Therefore, if we can suppress readout noise by circuit technique, we can increase SNR in the dark condition (reducing the readout noise dominant area). The interesting thing is that suppression readout noise is not effective in the bright conditions due to dominance of photon shot noise. Therefore, we only need suppression readout noise in the dark condition. In other words, signal-dependency for suppression of readout noise is needed and effective. In my opinion, combining signal-dependency with conventional analog circuit technique, we can make effective image sensor for low light imaging.

Chapter 2.

ADCs in CMOS image sensor

1. ADC structures in CMOS image sensor

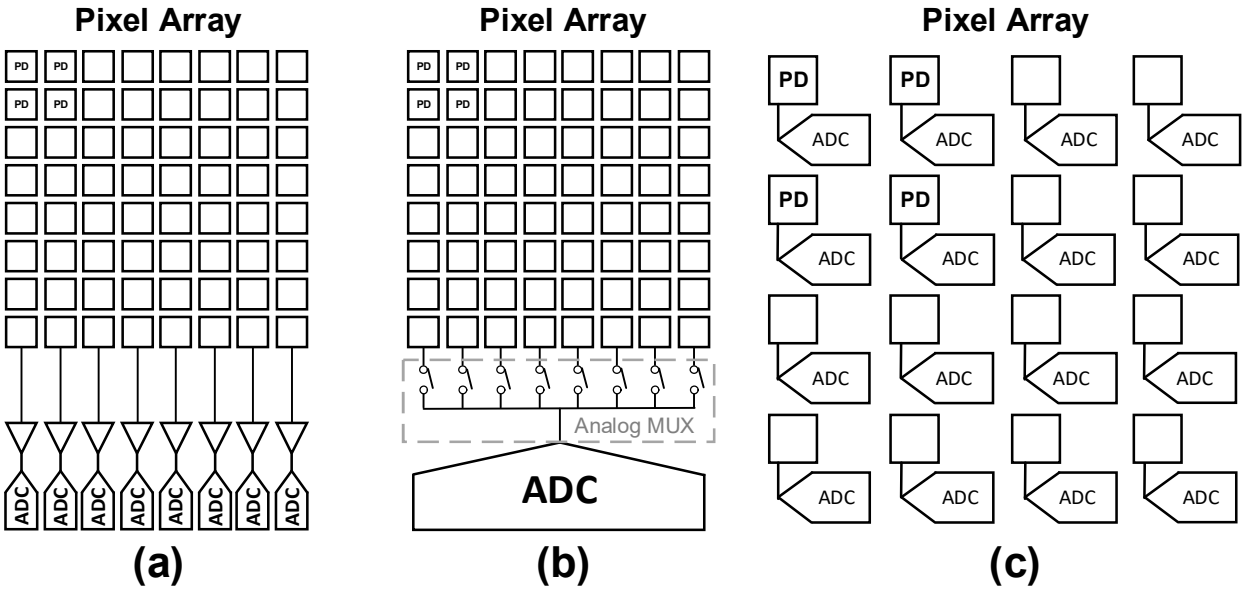


Fig 7. Three types of ADC structures in CMOS image sensor (a): column-parallel structure (b): single ADC structure (c): in-pixel ADC structure

The analog signal generated by the pixel are converted to digital domain by ADC. The specifications of the readout circuit are determined by how quickly the signal will be converted during conversion process. The ADC structure in CIS can be divided into three types of structure. One of them is single ADC structure. In this structure, one ADC handles readout of all pixel values Its readout time is significantly larger than other structure and it is proportional to the multiplication of the number of rows and the number of columns. Other structure is column-parallel ADC structure. ADCs are located in each pixel column then one ADC handles readout of one column of pixel values. Its readout time is reduced than single ADC structure and it is proportional to the number of rows. The last thing is in-pixel ADC structure. Each pixel own their own ADC then all of the conversion can start simultaneously. However, using this structure will result significantly large size of pixels and large power consumption due to ADCs. Therefore, column-parallel ADC structure is proper structure of CIS concerning with readout time, pixel size and power consumption.

2. ADC architectures

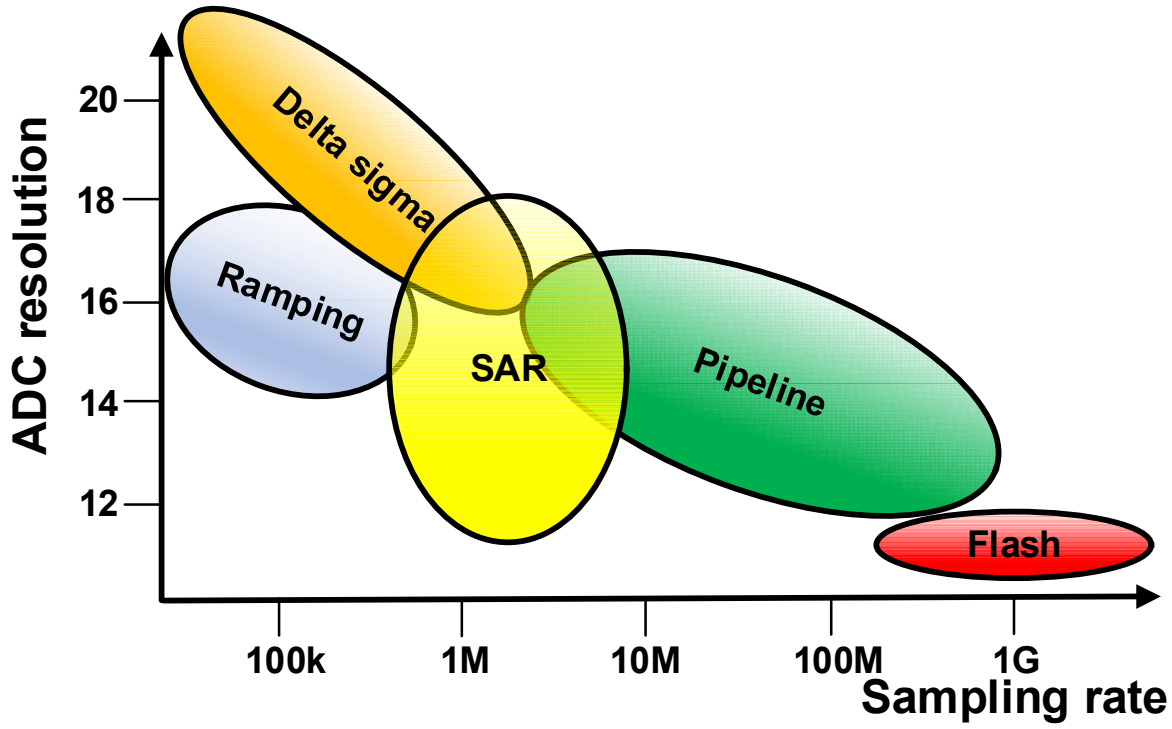


Fig 8. ADC architectures used according to sampling rate and resolution

The analog-to-digital converter (ADC) is used not only CIS but also mixed-signal system-on-chip (SoC). Therefore, designers are needed to select appropriate ADC for their applications. Basically, designers should select their sampling rate and ADC resolution (ENOB) for their system. First, flash or parallel architectures convert value in parallel. Therefore, flash is the fastest ADC type compared with other ADC architectures. However, to do conversion in parallel, it needs many comparators and resistors. Therefore, it consumes large power compared with others. From these reasons, flash or parallel architectures are used in lower-bit resolution applications generally. Second, ramping architectures convert analog to digital by measuring the amount of time when their reference signal and sampled signal are same. These types of converters can provide high resolution. However, its application is limited to slow sampling rate. Third, pipelined architectures are composed with cascade conversion stages. Each conversion stages operate fast in lower resolution. Then, each stage provide residue to next stage. Also, latency will be high due to origin of architecture. Fourth, SAR architectures quantize the input signal step-by-step with successive approximation algorithm. The last ADC architecture to be described is delta sigma ADC. The principle of architecture is to estimate the value of a signal roughly, obtain the error, and then use the cumulative error to correct the error. It can generate high oversampling rates and bit stream data. Therefore, conversion value is represented by accumulation of bit stream in long period. It is specialized in high resolution applications.

2-1. Flash ADC

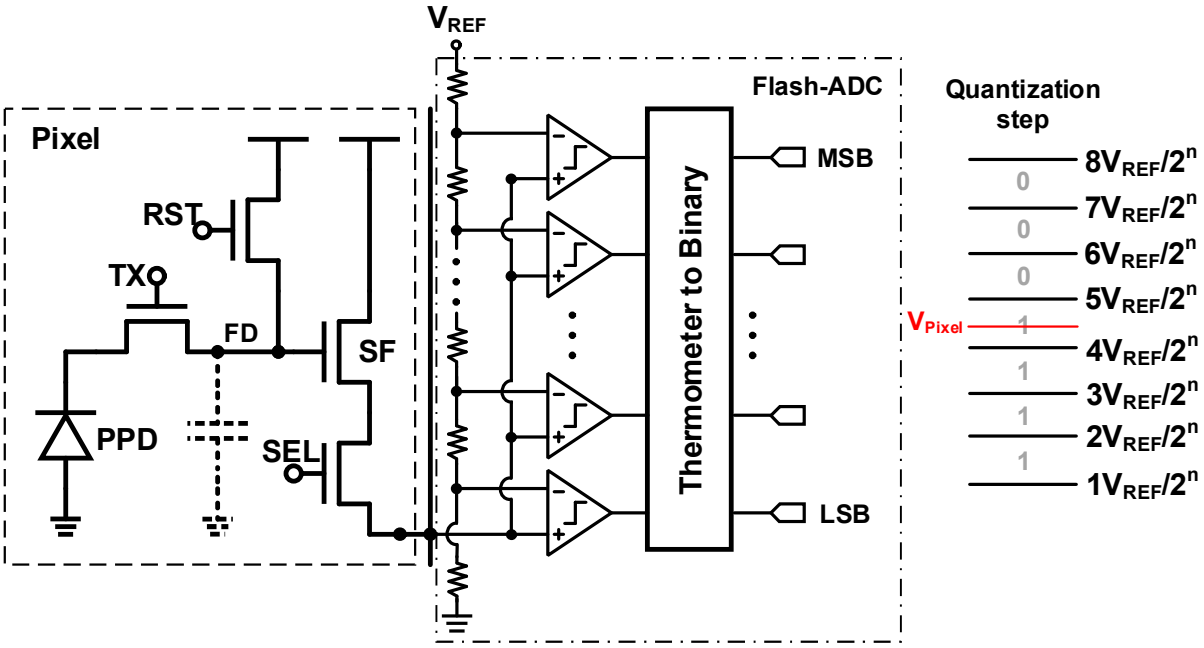


Fig 9. Flash analog-to-digital converter circuit and operation of 3-bit case

The flash ADC have the fastest conversion time than other types of ADCs because It can convert analog value to digital value in parallel. Flash ADC need 2n-1 comparators (n: the number bits) and 2n resistors. Therefore, its power consumption and size of ADC increases as the number bits increase. Therefore, it can be used in only single ADC structure. In addition, as the number of bit increase, input parasitic capacitance will increases. pixel SF with small current bias cannot load its output to ADC input because of large capacitance. From this reason, pixel SF is needed to large current bias to load to ADC input capacitance then it is needed to be consider in notion of power consumption. Therefore, resolution is limited to 5-8bit level which is not enough to realize high quality images. From these reasons, Flash ADC is not used generally in CIS.

2-2. Pipelined ADC

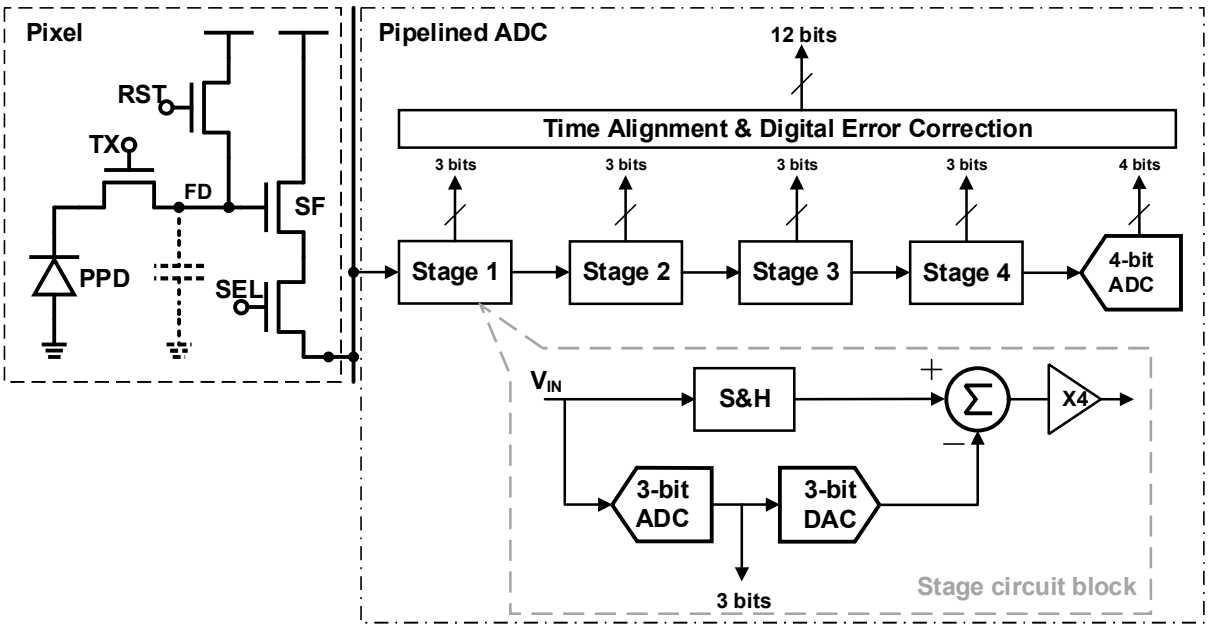


Fig 10. Pipelined analog-to-digital converter circuit with four 3-bit stages (each stage resolves 2 bits)

The Pipelined ADC uses a great many lower bit flash ADCs and MDACs to get high resolution with many raw bits and digital error correction from raw data. Therefore, it can reduce power consumptions compared with flash ADC which have same number of bits. However, Pipelined ADC need many comparators because of using many flash ADCs. Therefore, its size is big issue to use in CIS application. From this reason, pipelined ADC is generally used in single ADC structure in CIS.

2-3. Digital pixel ADC

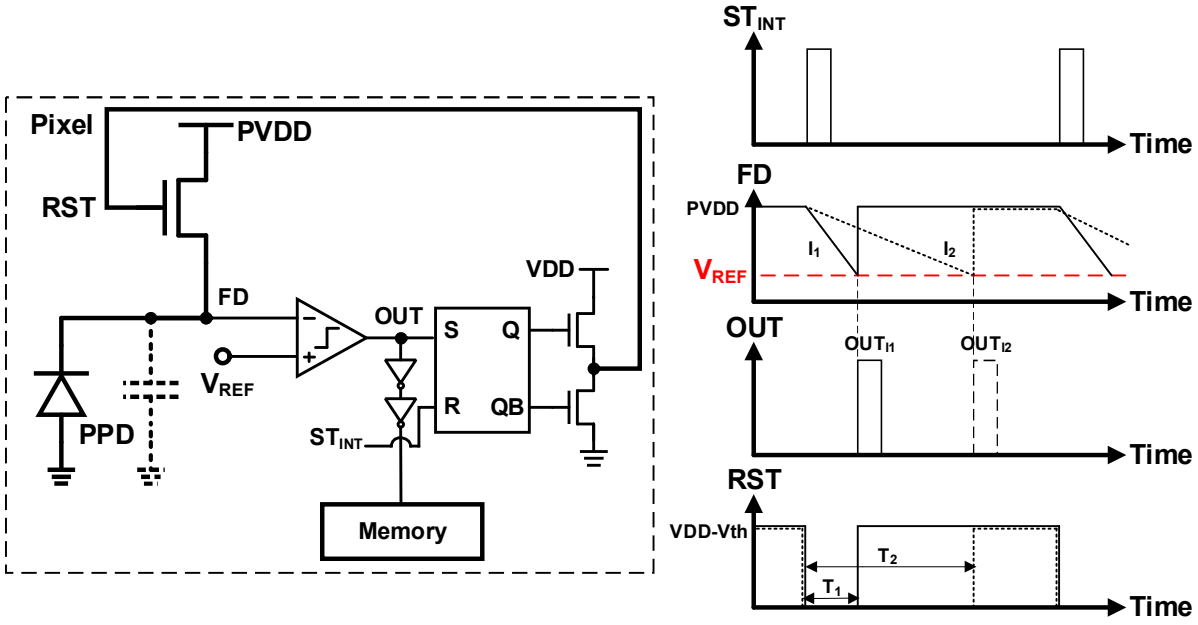


Fig 11. Digital pixel ADC with its operations

Digital pixel has been proposed to achieve in-pixel ADC structure in CIS since 2001. From this structure, it can achieve 10000 frames/s CMOS image sensor [4]. As we know, due to get enough pixel resolution in in-pixel ADC structure, ADC structure is needed to be smaller than other types of ADCs. Therefore, digital pixel composed with simple digital block, comparator and memory has been proposed. This method starts from assumption that photocurrent is linear function to light intensity. Therefore, FD voltage can be modelled as ramp signal with constant slope. When it starts integration, FD voltage goes down due to generated photocurrent then at some moment, FD voltage will be same with V_{REF} voltage. After that, comparator output will toggle to high. If we can calculate time between integration start time and comparator toggling time, then we can calculate light intensity. Therefore, time-to-digital converter (TDC) is needed to achieve this approach by measuring time when comparator output toggles to high. Due to large size of pixel, its resolution become significantly reduced compared with other pixels. Also, large power consumption from many comparators is critical issue. However, in recent years, because of technology development of 3D-stacking, realizing small pixel size of digital pixel can be possible. Therefore, some companies are researching in-pixel ADC structure with digital pixel.

2-4. Delta sigma ADC

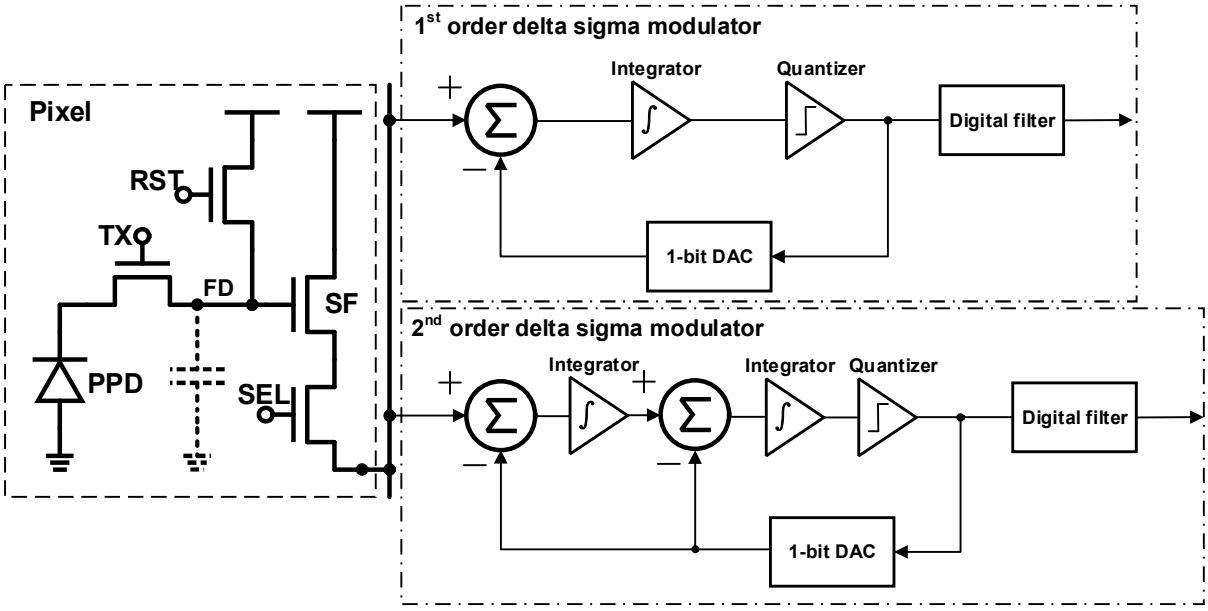


Fig 12. 1st order and 2nd order delta sigma ADC circuits

The latest CMOS image sensors are needed to high resolution which is over 14bits for reducing temporal noise. However, typical ADC architectures will consume large power to achieve high resolution and need calibration block which is big constraints of limited areas. Therefore, delta sigma ADC with noise shaping technique can generate high resolution conversion results. However, to get conversion results, accumulation of bit stream to get conversion data is needed because delta sigma ADC generates bit stream data serially. Therefore, conversion time is somewhat longer than other types of ADC architectures. In notion of design, the design of digital filters is quite tricky. In addition, to get more higher resolution results, order of delta sigma modulator is needed to be increased and stability of delta-sigma modulation loop is needed to be considered.

2-5. Successive Approximation ADC

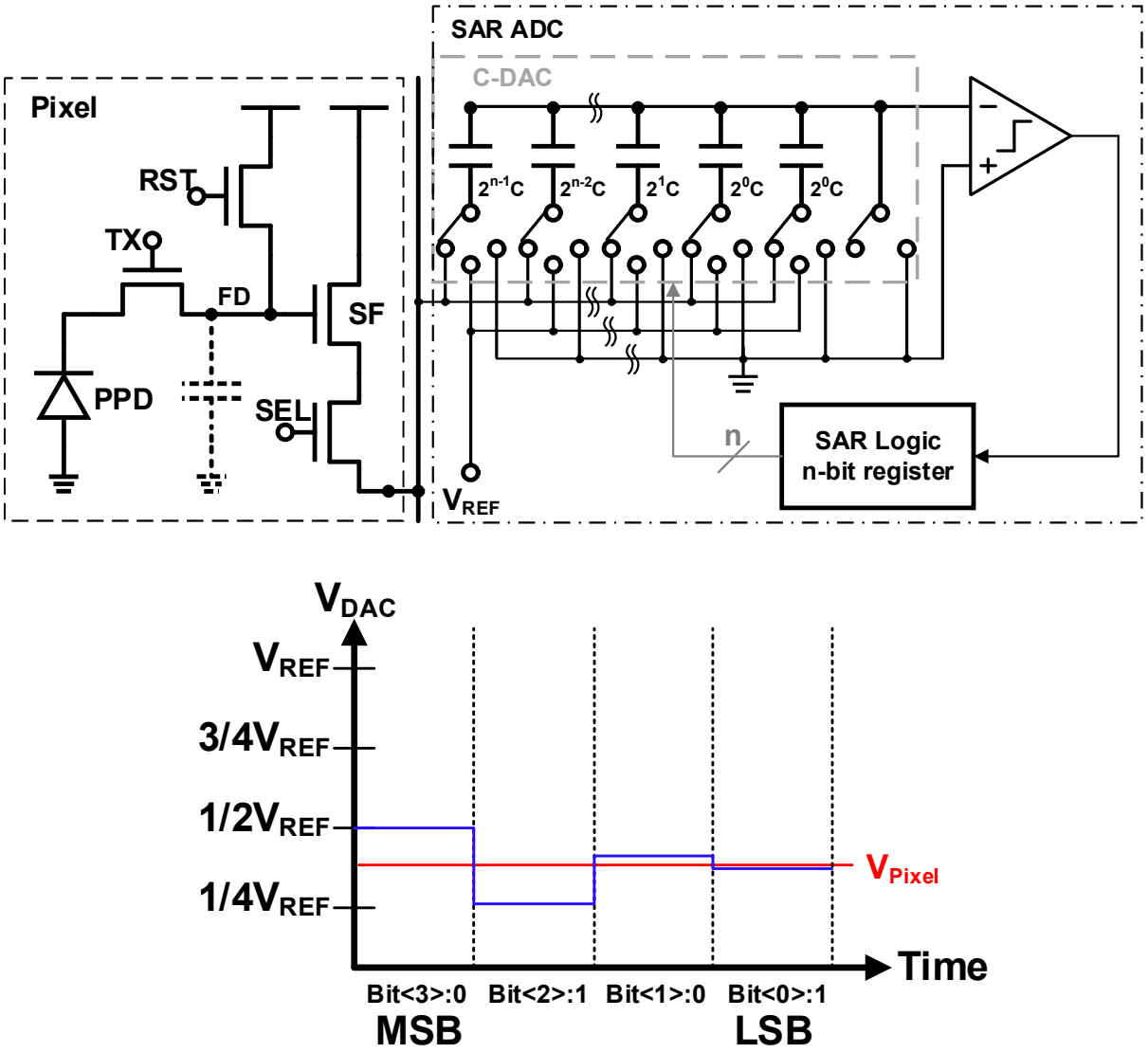


Fig 13. Successive approximation analog-to-digital converter circuits and operation 4-bit case

The successive approximation ADC(SAR-ADC) is composed with a comparator, capacitor DAC, SAR logic digital block and n-bit register. It has faster conversion time than single-slope ADC because for realizing n-bit resolution, theoretically, SAR-ADC only need n clocks. However, as the number of bit increase, total capacitor summation value 2^n which size is significantly large. This is fatal issue for using SAR-ADC in CIS. However, as the CMOS technology develops, minimizing capacitor size while keeping capacitance value is possible. Therefore, SAR-ADC can be used in column-level ADC structure in CIS. Also, by using circuit technique, capacitor splitting method in capacitor DAC can be applied to reduce total capacitor size which is large burden for usage. However, Linearity problem coming from capacitor splitting is observed. In combination with the single-slope ADC(SS-ADC) on the back page, Hybrid SS-SAR ADC or SAR-SS ADC have been proposed in [5]

and [6]. The order of names is determined by which type of ADCs is operated first. More discussion is needed about what order it is more effective to get high quality of image. Therefore, Hybrid ADCs can reduce the burden coming from capacitor size, although the conversion time is somewhat increased compared to the SAR ADC.

2-6. Single-Slope ADC

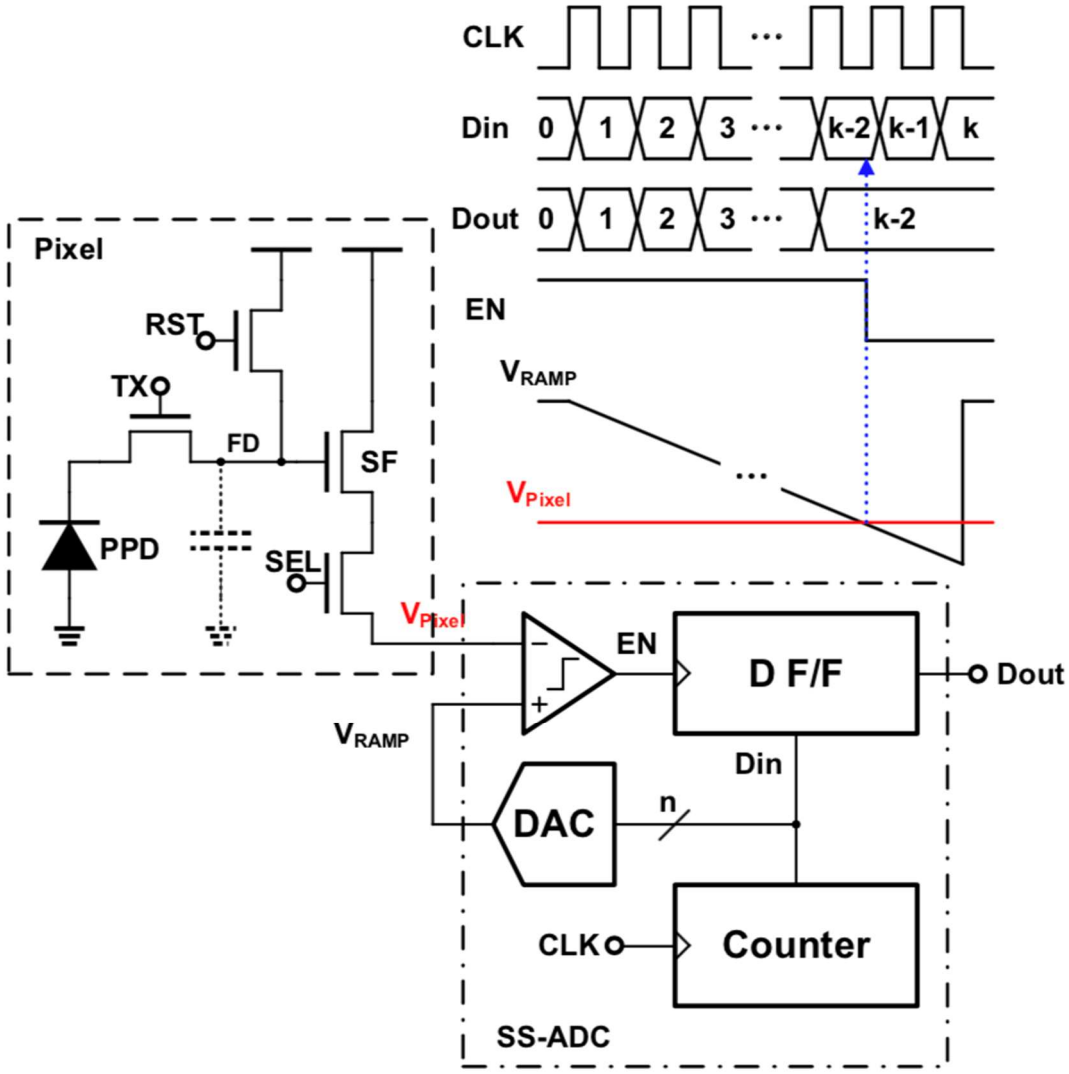


Fig 14. Conventional single-slope analog-to-digital converter circuit and its operation

$$T_{CONV\_ADC} = T_{clk} \times 2^n$$

n: bit resolution

Eq 2. Conversion time equation of single-slope analog-to-digital converter

The conventional single-slope ADC is composed with one global ramp signal generator and one global counter. In each column, it has one comparator and D flip-flop for converting analog value to digital value. When ADC operation starts, the ramp signal goes down along specific and intended slope. Also, global counter starts counting when ADC operation begins. When the ramp signal and pixel value is same, comparator will toggle their output then D flip-flop will transfer counter value to their output. Therefore, it has simplicity for operation and smaller size than other ADC types. From these reasons, single-slope ADC is used in most of CMOS image sensors. However, its conversion

time is longer than other type of ADCs. Therefore, its frame rate is somewhat lower than other type of ADCs. The most critical drawback is lack of time efficiency. For example, if pixel value is high, as soon as ADC operation starts, comparators will toggle their output. Therefore, most of the conversion time will be wasted. To handle with this problem, many approaches have been proposed in the past.

3. Chapter summary

ADC structure	ADC architecture
Single ADC structure	Flash ADC Pipelined ADC
Column-parallel ADC structure	Single-Slope ADC SAR ADC Delta sigma ADC
In-pixel ADC structure	Digital pixel (PWM) Time to Digital Converter

Table 2. ADC structures table in CIS with appropriate ADC architectures

In this chapter, we learned about the ADC structures in CIS and types of ADC architectures. Therefore, we can arrange it by the following table. First, flash ADC and Pipelined ADC are generally used in single ADC structure in CIS because of their huge power consumption and the fastest conversion time. Second, single-slope ADC, SAR ADC and delta sigma ADC are generally used in column-parallel ADC structure which is the most popular ADC structure in CIS. These ADC types generate moderate readout speed and resolution and low power consumption compared with other ADCs. Finally, digital pixel or time-to-digital converter circuit are generally used for realizing in-pixel ADC structure which all of pixel have their own ADC. Therefore, its pixel size become larger than other ADC structure. To realizing in-pixel ADC structure, ADC architecture should consume less power and smaller size compared with other ADC ones.

Chapter 3.

Noises in CMOS image sensor

1. Overview of noises in CMOS image sensor

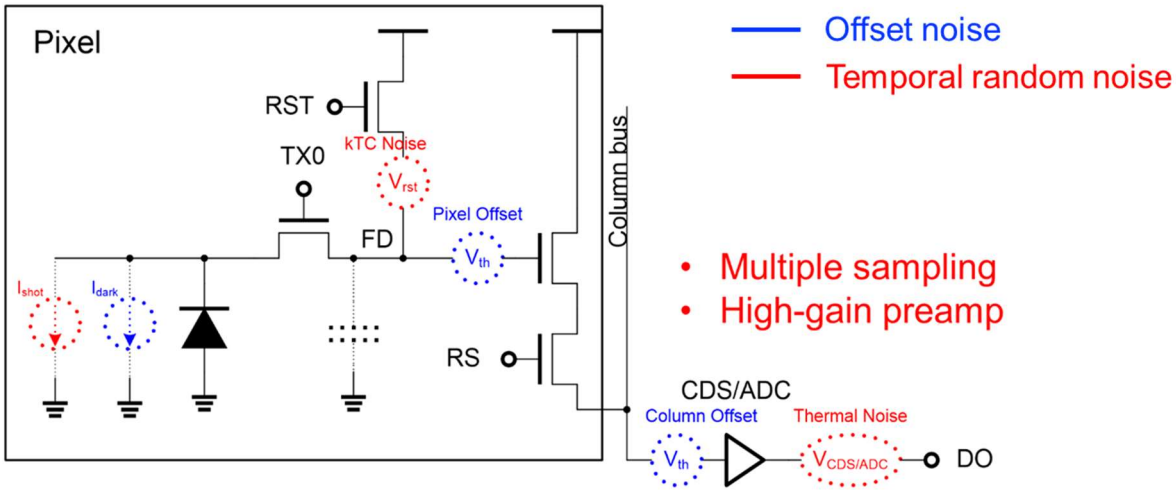


Fig 15. Noise components in CMOS image sensor

In CIS, there are many noise components which degrade the performance of CIS. Therefore, reducing or suppression these noise components is important to improve the performance of CIS. First, blue dotted noise components are offset noise which can be eliminated by double sampling. Operation of CIS is that measuring reset value, then measuring the signal value in the same readout circuit. Therefore, it can be neglected due to operation of CIS. In addition, kTC noise (reset noise) can be eliminated by correlated double sampling in 4T pixel operation. Therefore, it is neglected in commercial color image sensor in industry. However, it is needed to be considered when pixel is not 4T pixel. Next, photon shot noise is noise caused by quantum characteristics of light. It is not possible to reduce photon shot noise in single frame. More analysis about these noise components are written in next page.

2. Noise components in CMOS image sensor

2-1. Reset noise (kTC noise)

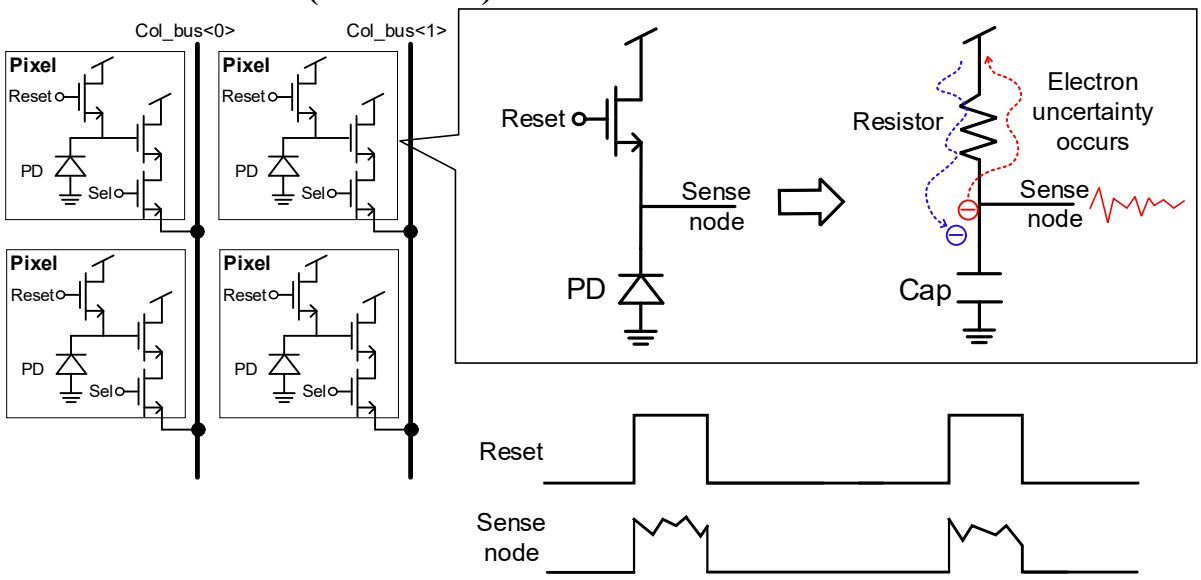


Fig 16. Reset noise in CMOS image sensor

Reset noise is coming from uncertainty of movement of electrons in resistor. When reset transistor is on, reset transistor can be modeled as resistor and photodiode can be modeled as capacitor. Therefore, sense node voltage will fluctuate because of thermal noise. However, after turning off reset transistor, sense node voltage will freeze at certain random level. It can cause errors in sensor output because pixel reset value have irreversible errors. However, in these days, almost color CIS adopts true-correlated double sampling technique because of using 4T-pixel. Therefore, reset noise is not significant thing in CIS which is using 4T-pixel operation. However, in I-TOF, it cannot use 4T-pixel operation structurally. Therefore, it can use pseudo-correlated double sampling technique which cannot eliminate reset noise in pixel completely. The multiple sampling technique cannot reduce reset noise because of freeze of reset noise. In my opinion, if we turn on reset transistor when we do multiple sampling reset value, thermal noise can be averaged out because thermal noise is not freeze and continuous. Therefore, we can derive exact phase results because I-TOF phase value is calculated only subtracting each phase. Also, charge injection noise coming from reset transistor will be subtracted when we calculate phase value.

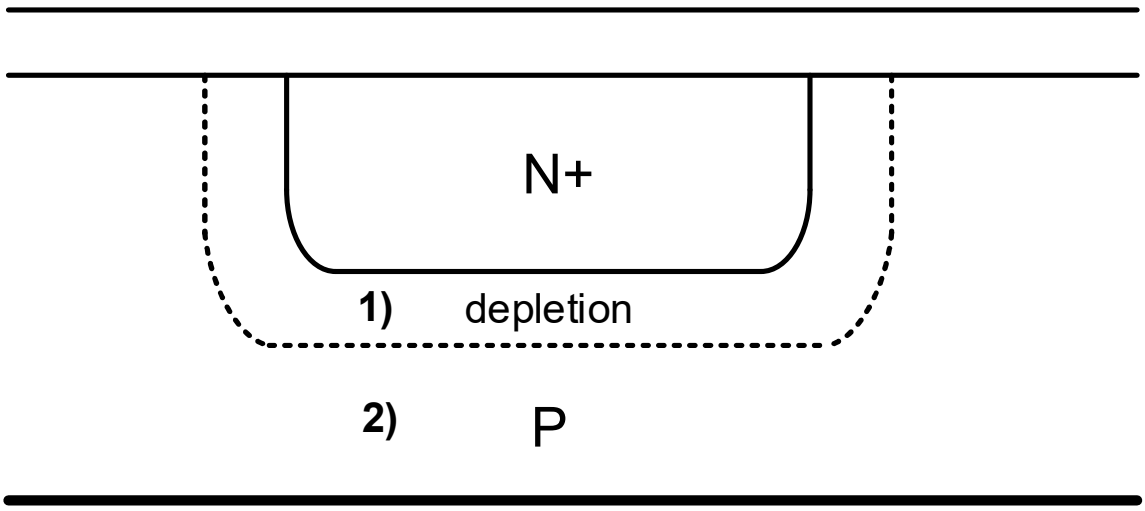
$$\Delta Q_{reset} = \sqrt{k \cdot T \cdot C}$$

$$\Delta V_{reset} = \sqrt{\frac{k \cdot T}{C}}$$

Eq 3. Reset noise equation in charge domain and voltage domain

Analytically, reset noise value is determined by floating diffusion (sense node) capacitance. Reset noise in charge domain increase as capacitance increases. However, in voltage domain, reset noise value decrease as capacitance increases. However, capacitance cannot increase infinitely, due to conversion gain of pixel which determined sensitivity of pixel. In terms of I-TOF applications, I-TOF pixel cannot increase capacitance due to need for high sensitivity of near infrared light to reduce integrating which is bottleneck for sensor speed. From these several reasons, reset noise is dominant source in I-TOF applications.

2-2. Dark current



1) Generation in the depletion region
2) Diffusion from a p-sub

Fig 17. Dark current sources in diode structure

$$I_{R-G} = AW\frac{qn_i}{\tau_g} = AW\frac{q\sqrt{N_cN_v}}{\tau_g}\exp\left(-\frac{E_g}{2k_BT}\right)$$

Eq 4. Recombination-generation current equation

$$I_{DIFF} = \mathrm{A}q\left(\frac{D_n n_{po}}{L_n} + \frac{D_p n_{no}}{L_p}\right) = \mathrm{A}q\left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right)N_C N_V \exp\left(-\frac{E_g}{k_BT}\right)$$

Eq 5. Minority carrier diffusion current equation

The dark current is the photo-detector current in no illumination condition. Therefore, it can cause errors in image sensor outputs because this current is not generated by photons. This current is generated mainly due to the random generation of electron-hole pairs within the depletion region of diodes. This current is called recombination-generation current. For example, electron in valance band can be excited by thermal energy. If its energy is over bandgap energy of silicon, it can jump up to conduction band and generate electron-hole pair. Therefore, the dark current have relationship with bandgap energy of materials and thermal energy. Therefore, generation rate of electron-hole pairs is proportional to absolute temperature. From another point of view, generation rate of electron-hole pairs is related to specific crystallographic defects within the depletion region. These defects can generate unstable energy state, then electrons can jump up to conduction band easily via energy state of defects. Therefore, the dark current spectroscopy can be used to determine ratio of defects presented in device by acquiring dark current histogram.

2-3. Photon shot

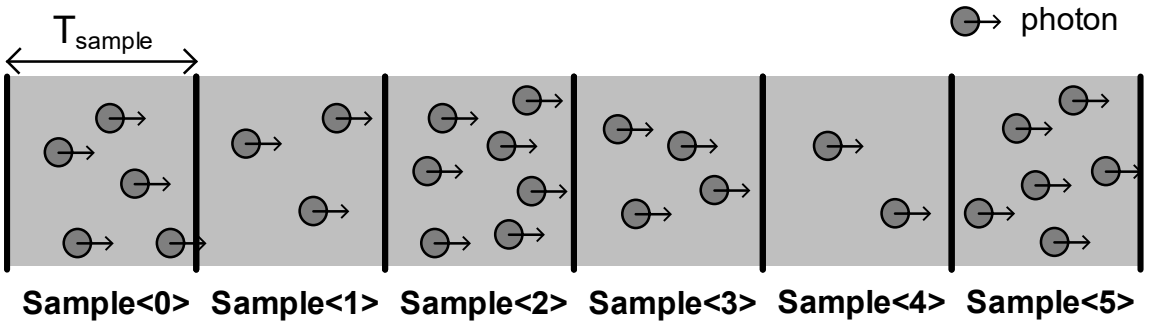


Fig 18. Photon shot noise in CMOS image sensor

The photon shot noise can be described the statistical Poisson-distributed nature of the arrival process of photons and the generation process of EHPs(electron-hole pairs) [2]. Briefly, if we apply exactly same light intensity CIS, Each samples will annotate different photon numbers seen as Fig 3-5. The standard deviation of the photon shot noise is analyzed as square root of the number of photons N:

$$\Delta N_{p\_shot} = \sqrt{N}$$

Eq 6. Photon shot noise equation

Therefore, photon shot noise is increased as bright condition. Some readers may have question about this phenomenon. Previously, I have written that SNR in bright condition is larger than the dark condition. The fact is that SNR increases because the signal intensity increases more than shot noise increases. Therefore, SNR in bright condition is larger than the dark condition. Photon shot noise cannot be reduced in single frame. To relieve effect of shot noise, averaging out several frames are needed. In same way, multiple sampling which samples same value several times is not effective to reduce photon shot noise.

2-4. Flicker noise

The flicker noise is generated by semiconductor traps which is originated from defects between oxide and substrate [14]. These traps capture or release charge carriers randomly. Therefore, wide size of transistor is needed to relieve effect of flicker noise. However, in CIS, source follower in pixel is dominant flicker noise source but it cannot increase size to reduce flicker noise because of shrinking size of pixels.

$$\Delta V_{flicker} = \sqrt{\frac{K}{C_{OX}WL} \cdot \frac{\Delta f}{f}}$$

Eq 7. Flicker noise equation in voltage domain

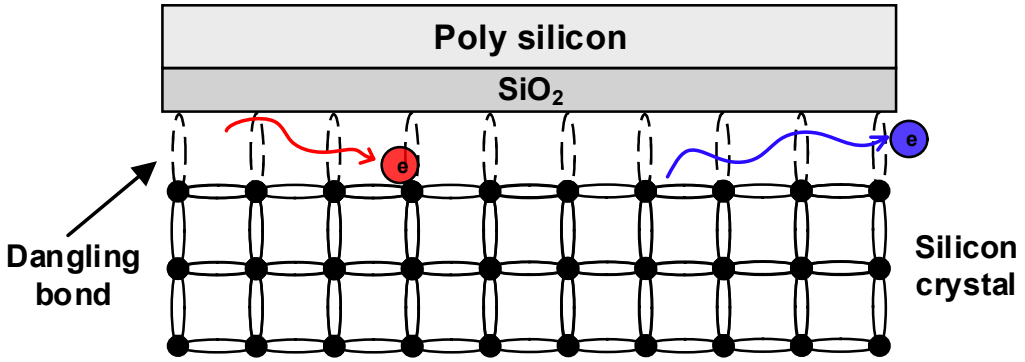


Fig 19. Dangling bond effect between oxide-silicon interface

K is the process dependent factor ($\approx 10^{-25} V^2F$), C_{OX} is oxide capacitance and f is frequency. In addition, pixel source follower is main noise factor in flicker noise. Therefore, reducing effects of flicker noise coming from source follower by circuit techniques are needed to be considered to provide high quality images.

2-5. Random telegraph noise

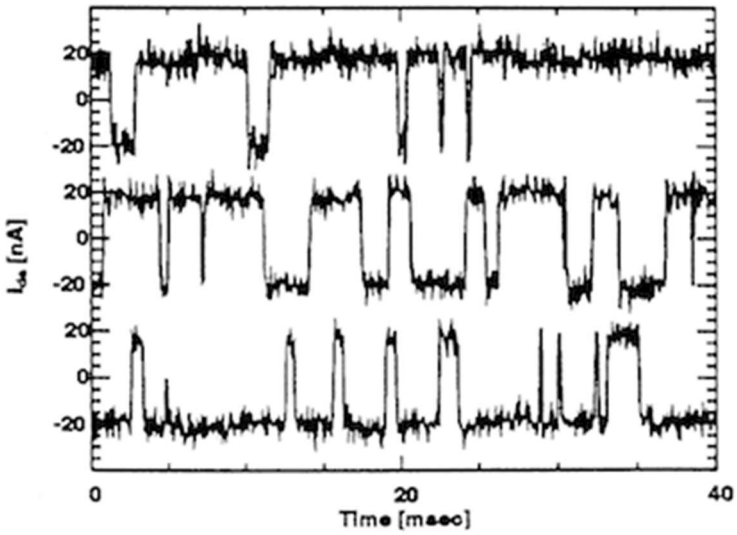


Fig 20. Graph of random telegraph noise in current domain

Random telegraph noise (burst noise) is a type of electronic noise that occurs in ultra-thin gate oxides and semiconductors. It generates sudden transitions in voltage or current domains. In voltage domain, it is as high as several hundred microvolts at unpredictable times. Also, it maintains sudden changed value from milliseconds to seconds. If it happens when transistor is connected speaker, it sounds like popcorn popping. Therefore, it is called popcorn noise. Also, flicker noise and random telegraph noise have same origins. In other words, flicker noise in large devices is caused from summation of many random telegraph noise in small area insulator [15].

In CIS, pixel size is shrinking rapidly. Therefore, size of source follower in pixel is decreasing with development of fabrication technologies. Therefore, insulator size become smaller. From this reason, random telegraph noise become dominant noise source and it can cause significant errors especially in dark conditions. Also, it is hard to eliminate effects of random telegraph noise by multiple sampling or high gain pre-amplifier circuits due to it lasts from milliseconds to seconds which is much longer than sampling frequency. Therefore, in device level, many pixel and circuit designers have been studying to reduce this noise in device levels.

3. Chapter summary

There are several noises which can deteriorate quality of results in CIS. Some noises like freeze reset noise, photon shot noise and random telegraph noise are irreversible. Therefore, circuit technique is hard to be applied to reduce effects of noise. However, other noises like flicker noise and thermal noise coming from readout circuit and pixel circuit can be reduced by circuit techniques like using high gain pre-amplifier and multiple sampling technique to increases SNR. Therefore, it is important which noise can be reduced and how to decrease its effects of these In the next chapter, we will handle techniques which can reduce temporal noises in CIS.

Chapter 4.

Circuit techniques for suppression noises in CIS

1. Conventional suppression noises techniques

1-1. High gain pre-amplifier technique

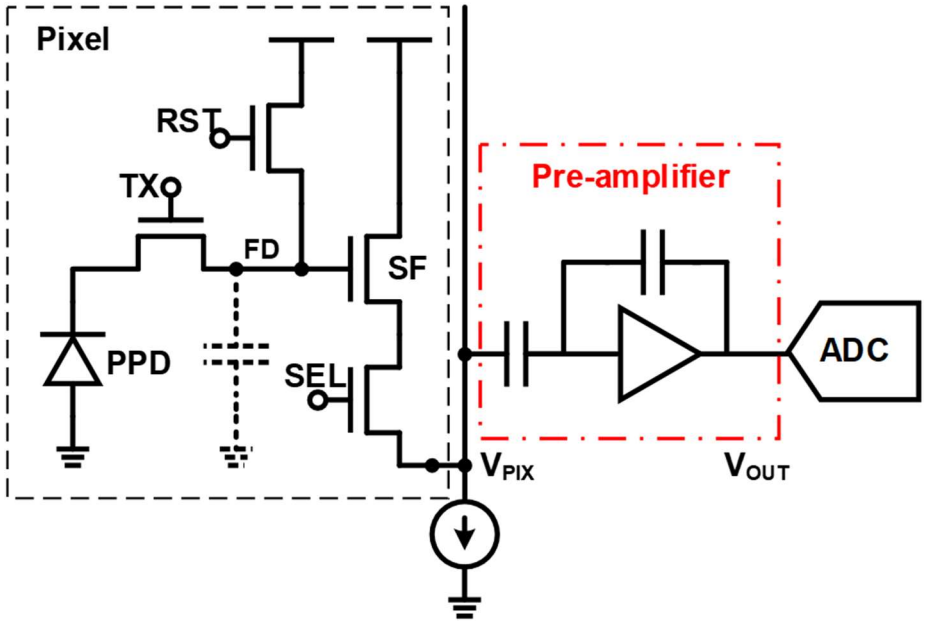


Fig 21. High gain pre-amplifier technique for suppression readout noise

$$V_{PIX} = V_{RST} - V_{SIG} + v_{n\_PIX}$$

$$V_{OUT} = AV_{PIX} + v_{n\_READ}$$
$$= A(V_{RST} - V_{SIG} + v_{n\_PIX}) + v_{n\_READ}$$

v_{n_PIX}: noises coming from pixel
v_{n_READ}: noises coming from readout circuit

Eq 8. High gain pre-amplifier technique noise suppression equation

The high gain pre-amplifier is generally used in column-parallel way in CIS. Generally, it can increase photo signal sensitivity and suppress thermal noise coming from readout circuits. The high gain pre-amplifier operates analog correlated double sampling (CDS) to eliminate pixel offset, kTC noise and column offset by sampling reset signal and photo signal in the same column. However, thermal noise

and flicker noise coming from source follower in pixel are amplified with photo signal. In other words, it has limitation to suppress noises coming from behind readout circuits. Also, dynamic range of pixel output will be decreased and large power consumption from using op-amp should be needed to be considered.

1-2. Multiple sampling technique

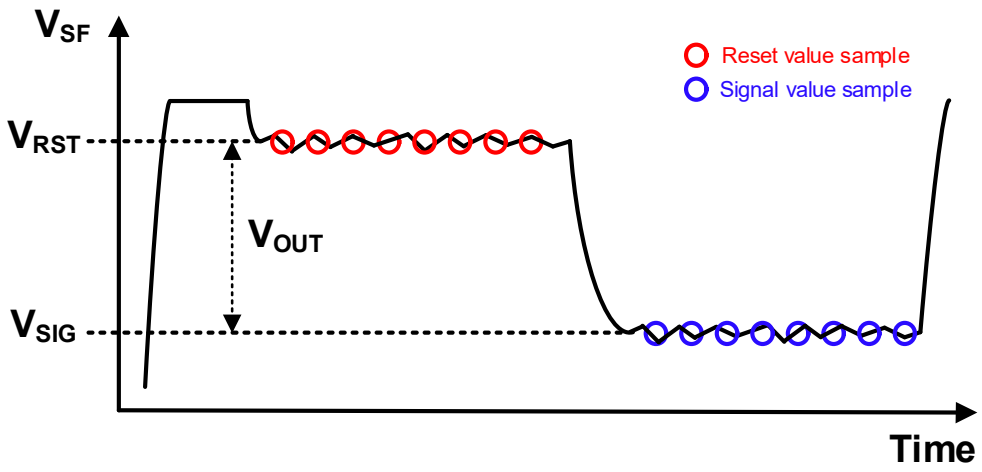


Fig 22. Multiple sampling technique for suppression readout noise

$$V_{OUT=M} = \frac{1}{M}\sum_{i=1}^{M}(V_{RST} - V_{SIG})$$

$$\sigma_{V_{OUT=M}} = \frac{\sigma_{V_{OUT=1}}}{\sqrt{M}}$$

Eq 9. Multiple sampling technique noise suppression equation

Thermal noises can be modeled by gaussian distribution. Therefore, increasing sampling number can reduce noise power to 1/M factor (M: sampling number). Multiple sampling technique is effective for suppression noises without decrease of dynamic range of pixel output. However, readout time will be increased to by M factor because of increase of sampling number.

From previous chapter, we know that most of image sensors use column-parallel structure with single-slope ADC because of size efficiency. However, conversion time of single-slope ADC is much longer than other types of ADCs. Therefore, attaching multiple sampling technique with single-slope ADC is

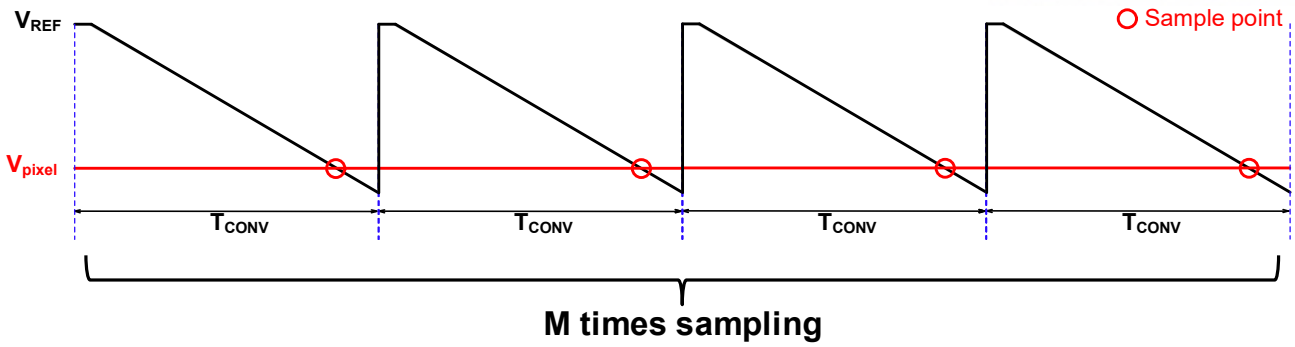


Fig 23. Multiple sampling technique with single-slope ADC

$$T_{MS\_ADC} = T_{clk} \times 2^n \times M$$

n: bit resolution

M: Sampling number

Eq 10. Conversion time of multiple sampling with single-slope ADC

inefficient in notion of framerate of image sensors. To overcome these shortcomings, many researches about multiple sampling technique with single-slope ADC have been conducted previously.

2. Previous multiple sampling techniques

2-1. Pseudo multiple sampling technique

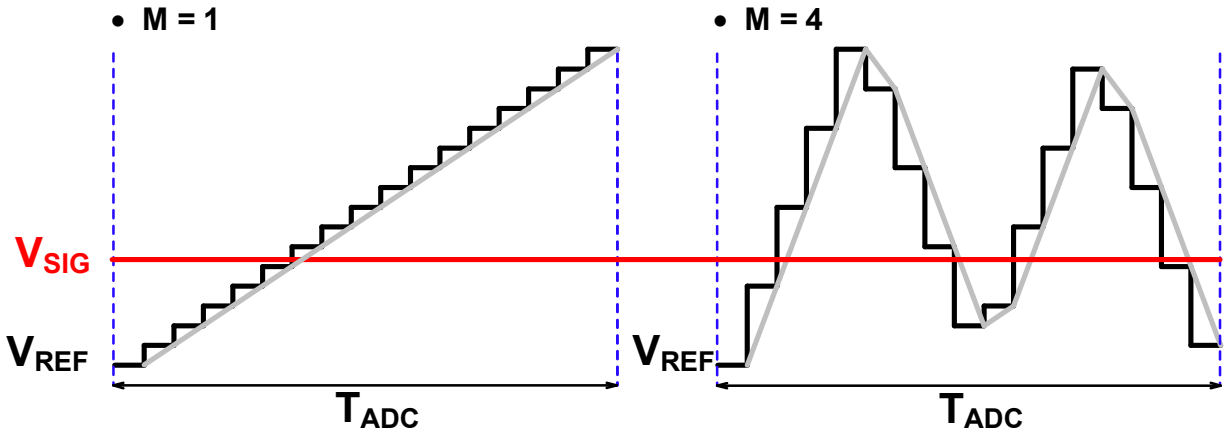


Fig 24. Operation of pseudo multiple sampling technique (M: sampling number)

The conversion time is increased due to increasing the sampling number. Therefore, the pseudo multiple sampling technique has been proposed [8]. It has focused to conserve readout time same with conventional SS-ADC readout time. It increases quantization step of ADC when the sampling number increases. Therefore, it achieves multiple sampling technique without sacrificing readout time. However, due to quantization noise coming from increasing quantization step, multiple sampling effect is limited compared with other conventional multiple sampling technique. Also, signal-dependency have been not applied in this technique. Therefore, in the bright conditions, multiple sampling effect is limited due to dominance of photon shot noise.

2-2. Signal-dependent multiple sampling technique

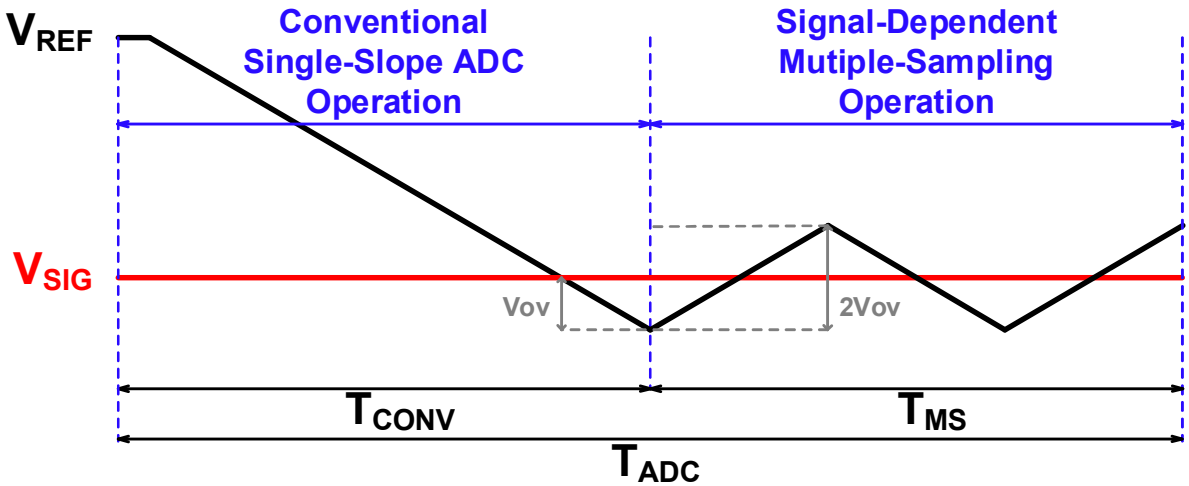


Fig 25. Operation of signal-dependent multiple sampling technique

As we know, multiple sampling technique is not efficient in the bright conditions due to dominance of photon shot noise. Therefore, signal dependency concept has been proposed [9]. it focused to increase the sampling number when pixel signal is dark. However, conventional single-slope operation should be done first to check location of pixel values to do multiple sampling. Therefore, it increases readout time compared with conventional SS-ADC. In notion of circuit technique, each column should have their own ramp generator. Therefore, integrator or current steering DAC cannot be used because of size in this technique. In this paper, it uses pull-up and down current source and capacitor to generate local ramp signals. Therefore, it will be susceptible to PVT variation and mismatch between pull-up and pull-down current sources.

2-3. Conditional multiple sampling technique

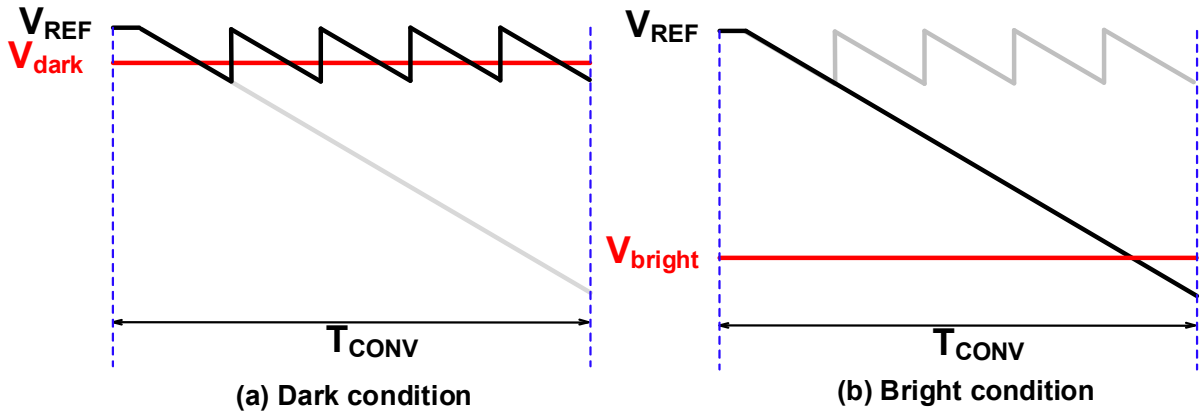


Fig 26. Operation of conditional multiple sampling technique

To increase SNR in dark condition, conditional multiple sampling technique have been proposed [10]. in this technique, do multiple sampling in dark condition and do single sampling in the bright condition with two global ramp generators without increasing readout time. However, it has drawback when pixel output is in the boundary between the dark and bright condition. In other words, its signal dependency is limited.

3. Chapter summary

	Pseudo MS	Signal dependent MS	Conditional MS
Readout time	☺	☹	☺
Signal dependency	☹	☺	😐
MS effect	☹	☺	☺
Ramp generator	Global	Column-level	Global
Silicon prove	☺	☹	☺

Table 3. Comparison table of previous works of multiple sampling technique

In conclusion, many researchers have been conducted to apply multiple sampling technique to reduce readout noise and mitigate the trade-offs from it in the past. Also, multiple sampling effect, signal dependency and readout time have deep relationship of trade-offs coming from multiple sampling technique. For example, signal dependency or increasing quantization step should be sacrificed to conserve readout time. Also, power consumption and size are also basic issues for adopting multiple sampling technique. Therefore, we need compromise each function and design issues to mitigate trade-offs.

Chapter 5.

Proposed signal-dependent multiple sampling ADC

1. Proposed signal dependency concept

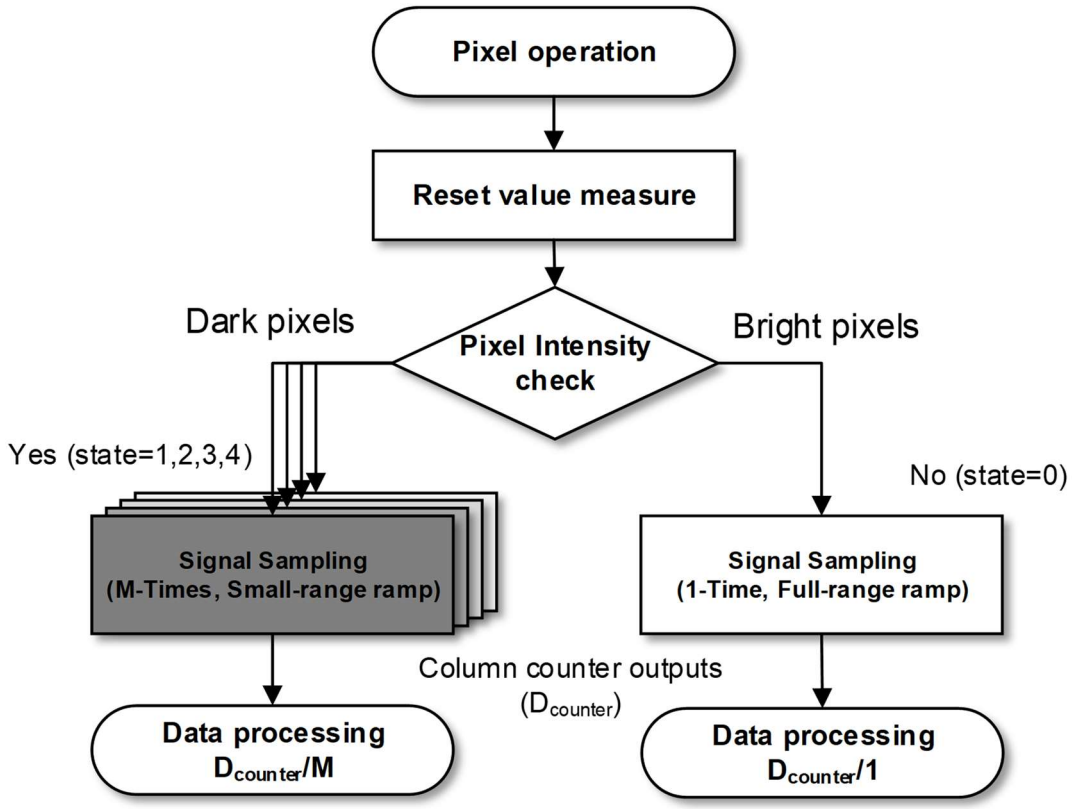


Fig 27. The algorithm for signal dependency concept operation

In CIS, there are inevitably dark pixels and bright pixels, and in between, moderate dark pixel exists. Therefore, dark pixels need many sampling numbers for reducing RN. However, bright pixels don't need many sampling numbers because of shot noise dominance and it have enough SNR comparing with other conditions. On the other hand, pixels with moderate brightness need a moderate sampling numbers which is larger than sampling number of bright pixels and smaller than sampling number of dark pixels. From these reasons, I will propose signal-dependent multiple sampling technique which can change sampling number according to brightness of pixels.

For example, from below figure, if pixel is in the darkest condition, it will select Ramp3 as reference signal for achieving maximum multiple sampling numbers. Similarly, if pixel have moderate dark

value, it will select Ramp2 as reference signal for moderate multiple sampling numbers and Ramp1 will be chosen to bright pixel for single sampling. As shown in figure, proposed idea will not increase readout time comparing with conventional SS-ADC which is same with Ramp1 signal but achieve signal-dependent multiple sampling technique just adding some global ramp signals [12].

Through this proposed signal dependency concept, I can converse readout time compare with conventional SS-ADC and keep quantization steps. Therefore, dark photo signal will be sampled with maximum sampling number and bright photo signal will be sampled at once.

	Pseudo MS	Signal dependent MS	Conditional MS	Proposed MS ADC
Readout time	☺	☹	☺	☺
Signal dependency	☹	☺	😐	☺
MS effect	☹	☺	☺	☺
Ramp generator	Global	Column-level	Global	Global
Silicon prove	☺	☹	☺	☺

Table 4. Comparison table of previous works and proposed concept of ADC

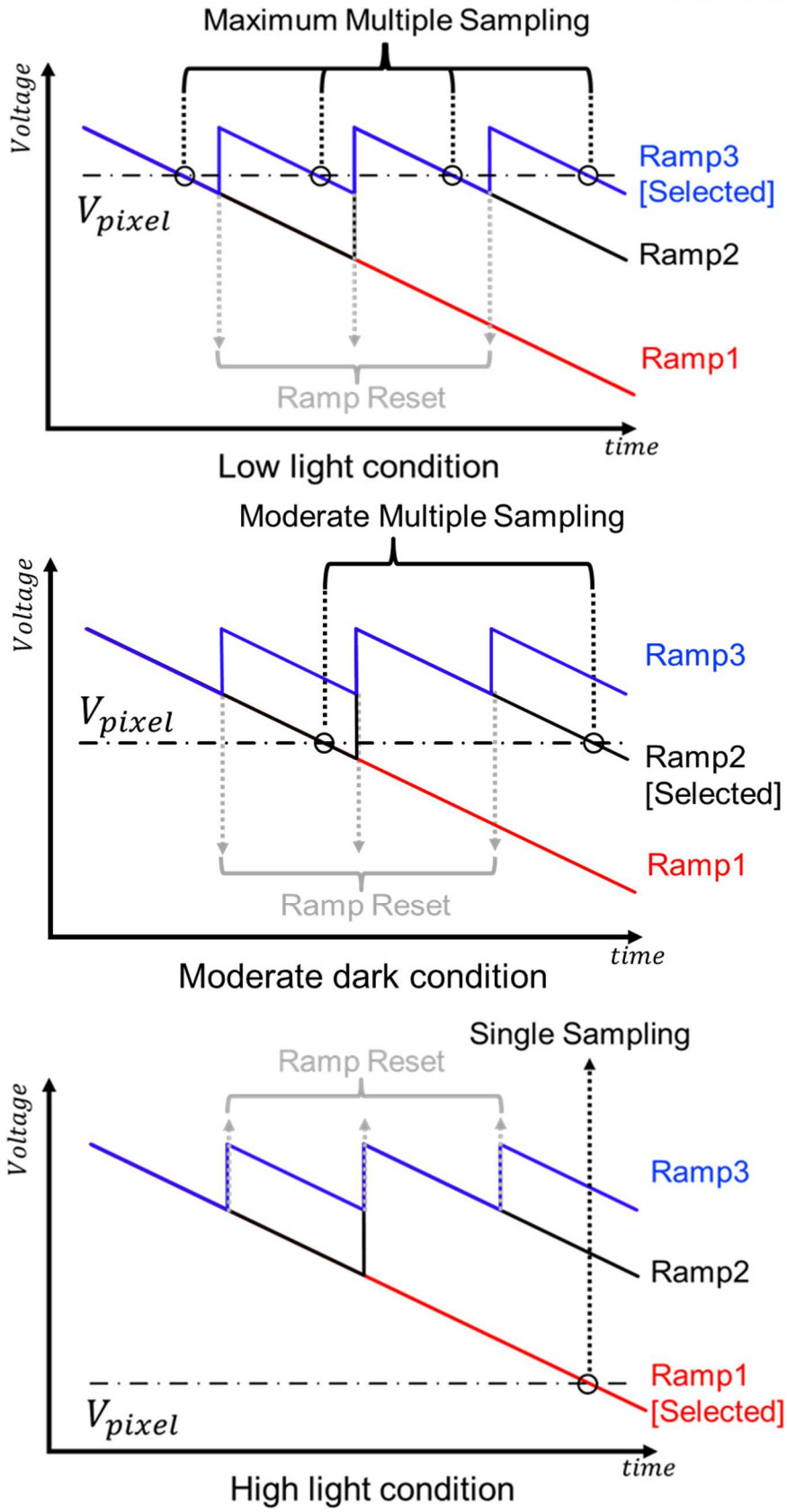


Fig 28. Proposed signal-dependent multiple sampling technique operations

2. Proposed ADC architecture

2-1. Architecture overview

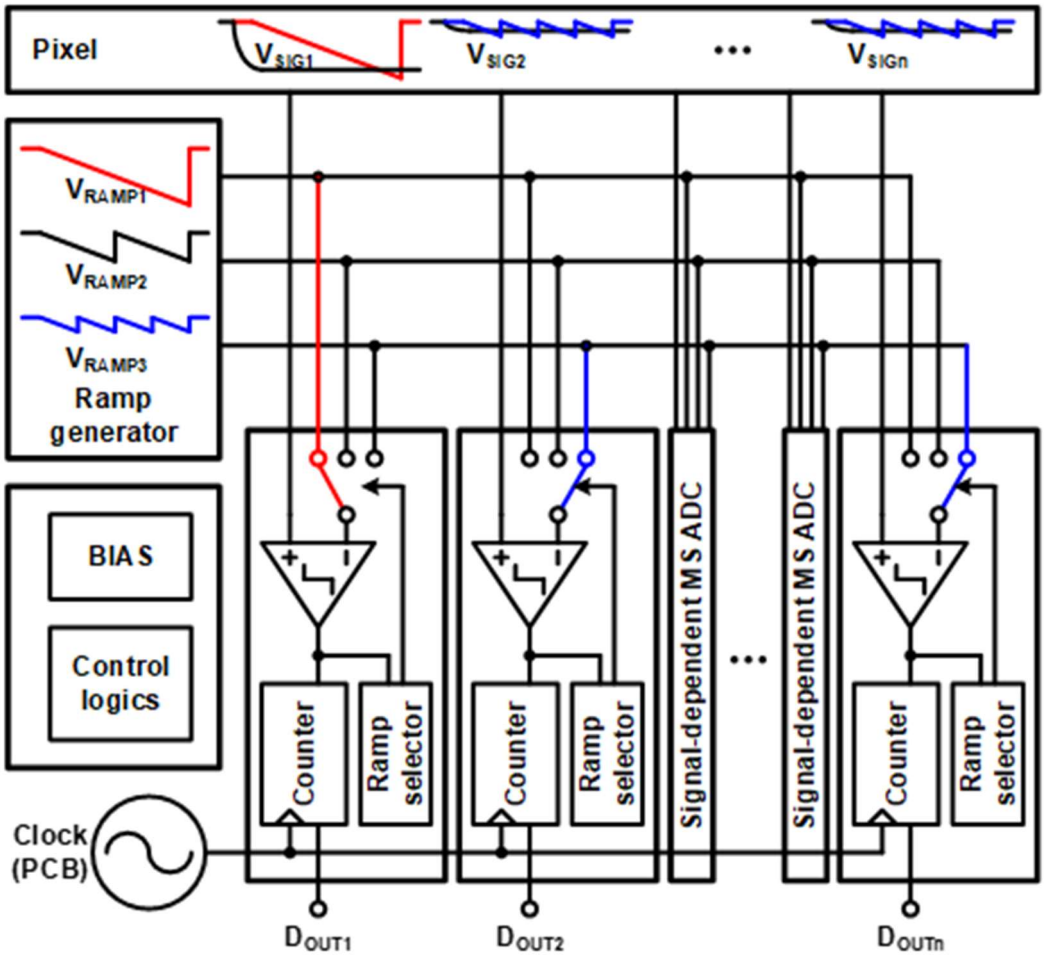


Fig 29. Proposed signal-dependent multiple sampling ADC block diagram

$$T_{ADCk} = T_{clk} \times M_k \times 2^{(n-k)} = T_{clk} \times 2^n = T_{CONV\_ADC}$$

$$M_k(\text{Sampling number}) = 2^n / 2^{(n-k)} = 2^k$$

$$k = 0,1,2,3,4 \Rightarrow M_k = 1,2,4,8,16$$

Eq 12. Conversion time of proposed signal-dependent multiple sampling ADC

Before achieving and realizing the proposed signal dependent multiple sampling technique, I adopt column-parallel ADC structure for achieving moderate readout time and power consumption. For achieving multiple sampling technique, multiple ramp generators are needed (Ramp1, Ramp2, Ramp3). Also, each column needs simple ramp selector block to achieve signal dependency. Therefore, there are not big difference between proposed ADC and conventional SS-ADCs. I can keep simplicity benefit of conventional SS-ADC but achieve signal-dependent multiple sampling technique with simple block.

Below figure is about overall operation of proposed ADC. For the simplicity, Figure is indicating only Ramp1, Ramp2, Ramp3 and Ramp4 signals. Ramp4 is the global signal for achieving maximum sampling number and Ramp3 and Ramp2 are the global signal for doing moderate sampling number. Ramp1 is the full-range global signal for single sampling of the brightest pixels. Ramp_RST signal is for pull-up of each ramp generator to reset their initial state. Therefore, each ramp generator has their own Ramp_RST signal. Also, each ramp generator has their own Ramp_EN signal for indicating the appropriate region of each ramp signal. For example, if comparator output toggles at Ramp3_EN region, this column will choose Ramp3 for moderate multiple samplings.

First, all columns are reset and selected to Ramp1 signal then when ADC conversion start, Ramp1 signal goes down with constant slope, then each counter count the number of clocks before comparator output toggles to high. If comparator output goes high at certain region, column choose appropriation ramp generator for their pixel value. When RAMP4_RST become high, the all ramp signals except RAMP4 stop to go down and RAMP4 goes to initial value of ramp generator. After resetting RAMP4, ADC conversion start in same ways. Through these simple logic, signal-dependent multiple sampling technique is achieved conserving readout time.

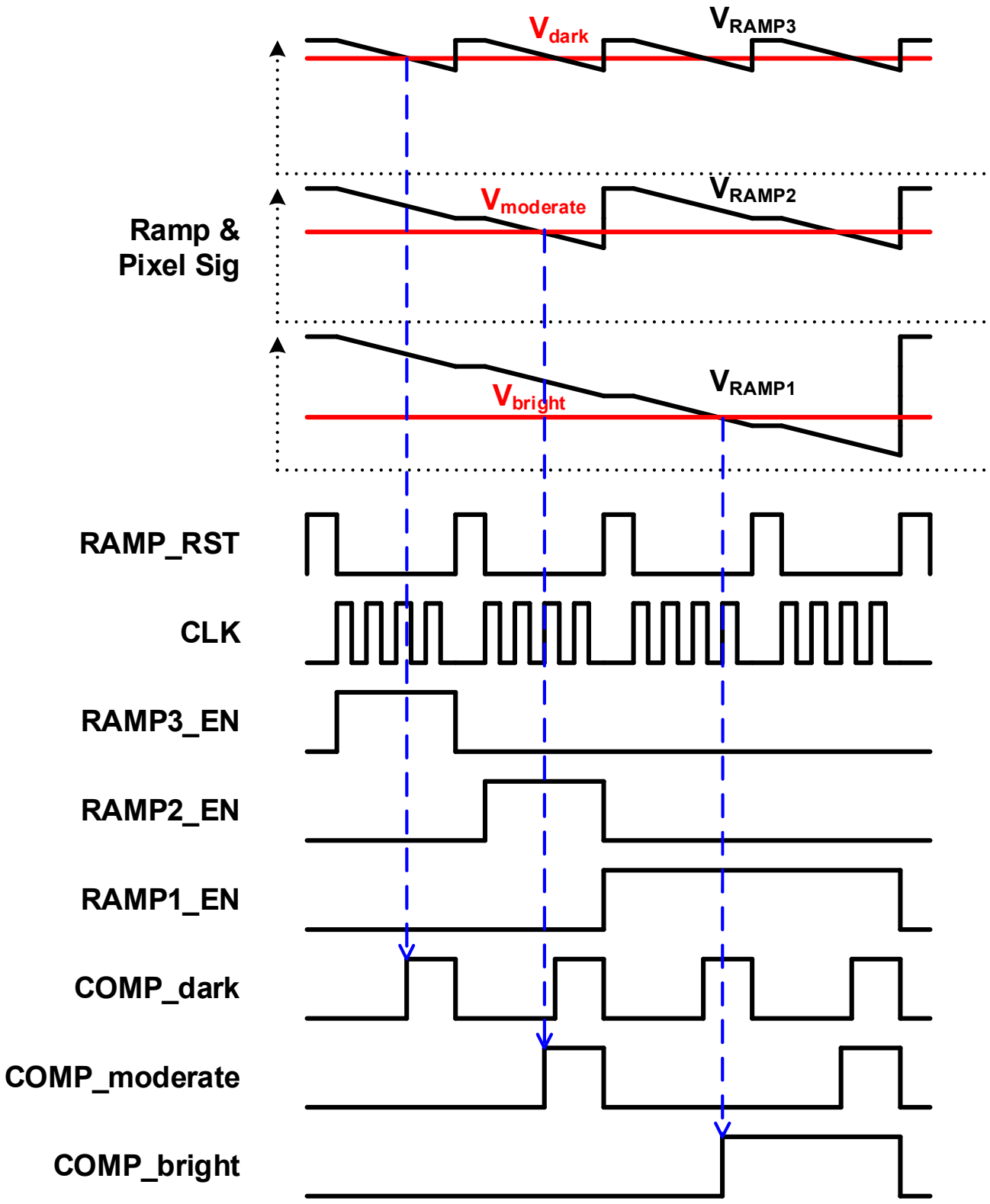


Fig 30. Proposed signal-dependent multiple sampling ADC operation timing diagram

2-2. Ramp enable signal generator

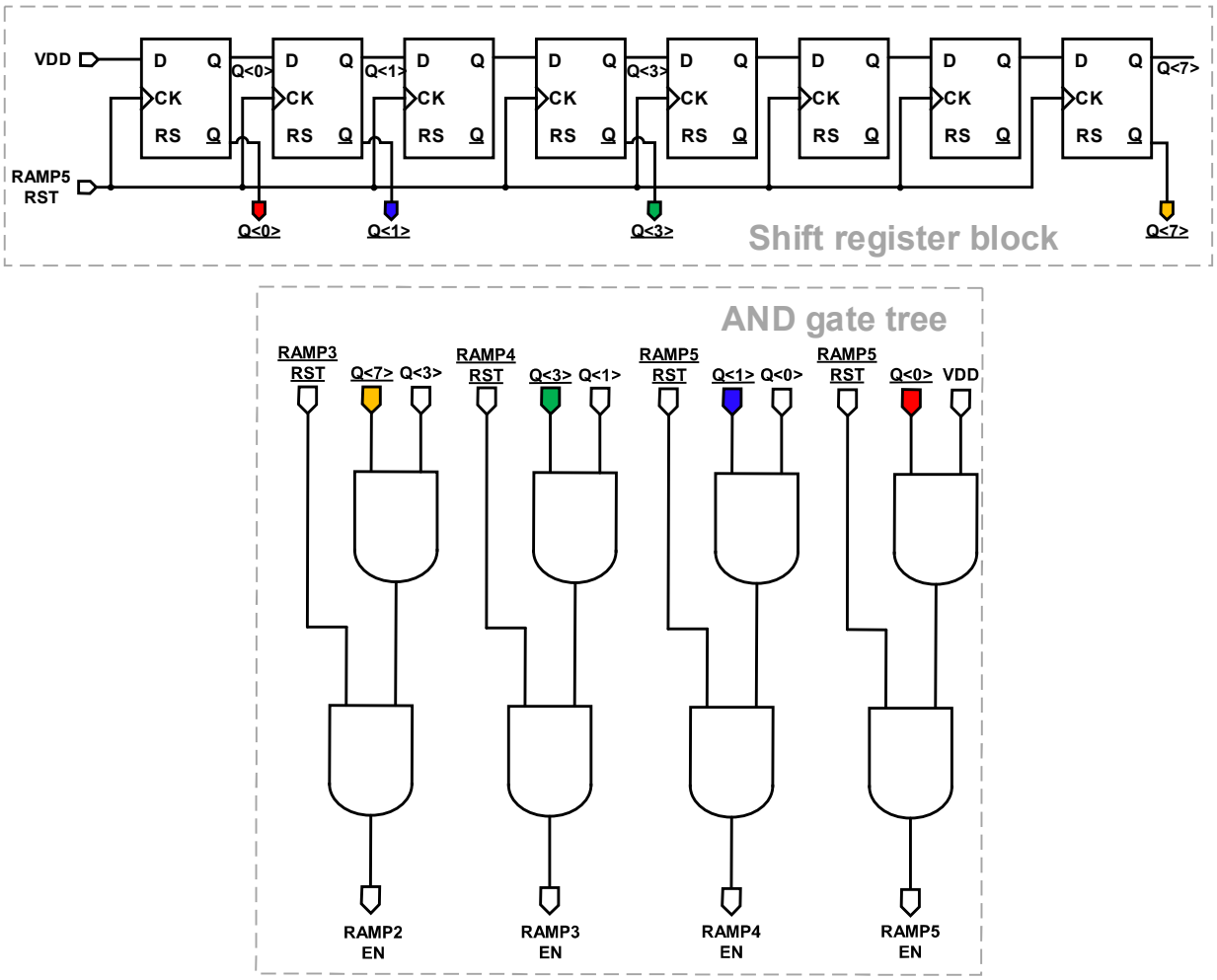


Fig 31. Scheme for ramp enable signal generator

In scheme of proposed ADC, *'Ramp EN'* signal defines the region of pixel value for selecting appropriate ramp signal. if each comparator toggle at certain region of *'Ramp EN'*, ADC can detect the intensity of pixel. Therefore, it is important global signal for checking intensity of pixels. In figure 31, *'Ramp EN'* signals are generated by shift register and AND gate trees to make simple digital logics. With this scheme, we can get appropriate timing diagram for operation of proposed ADC drawn in figure 32.

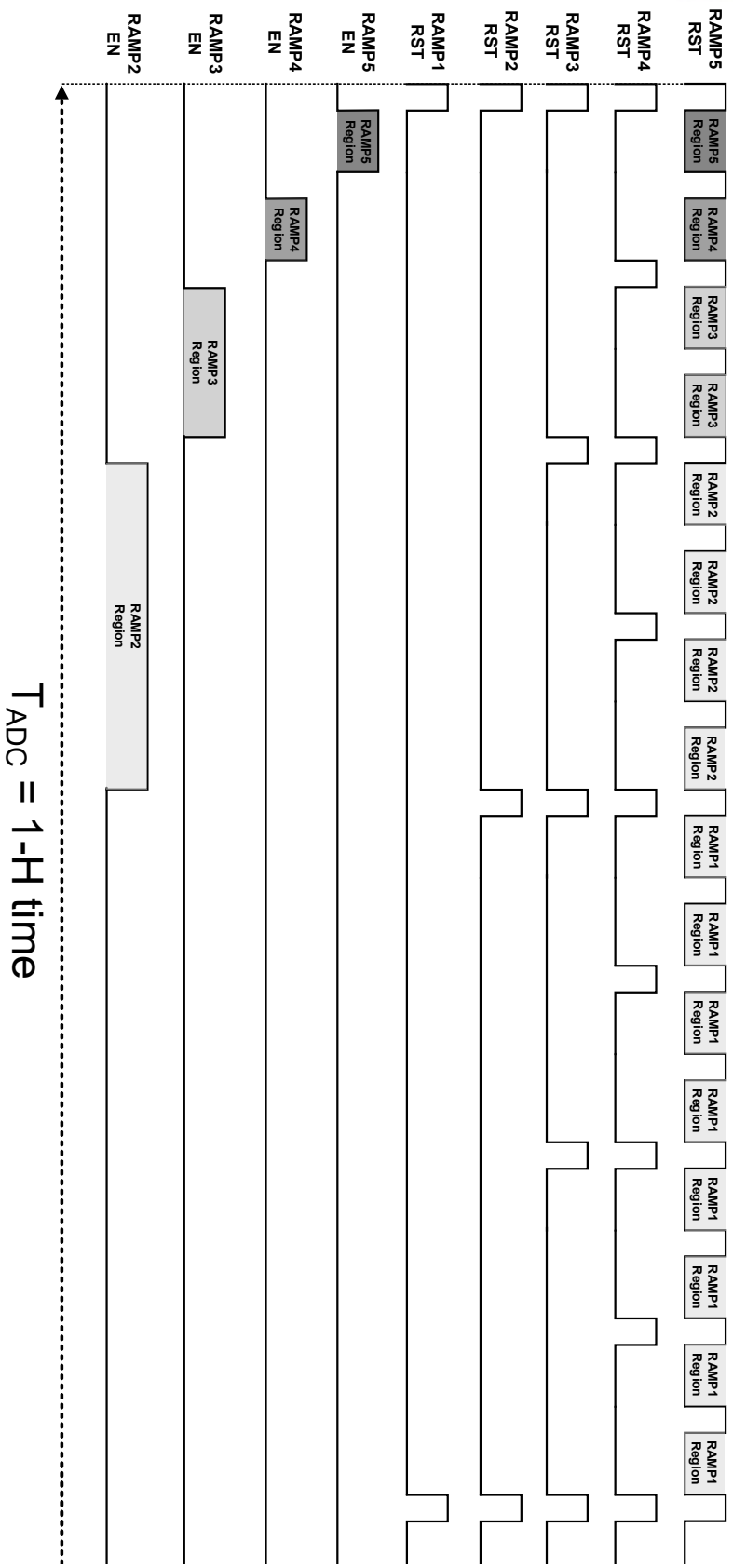


Fig 32. Timing diagram for ramp enable signals and reset signals

2-3. Ramp selector

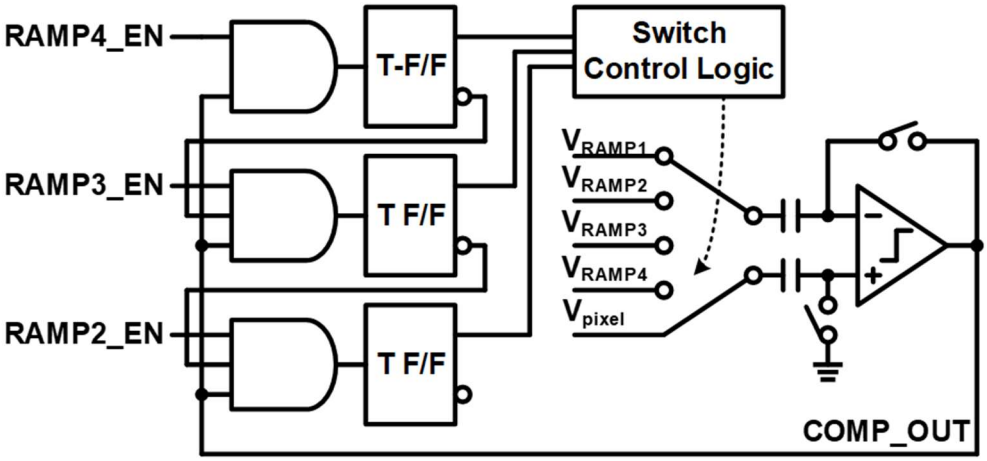


Fig 33. Scheme for ramp selector circuit

Each column has their own ramp selector for select appropriate ramp signal for multiple sampling signal dependently. With *'Ramp EN'* signal and *'COMP OUT',* T flip-flop is toggled when the 'Ramp EN' and 'COMP OUT' are high. And then with switch control logic, it can select appropriate ramp signal.

2-4. Cap modifying slope calibration scheme

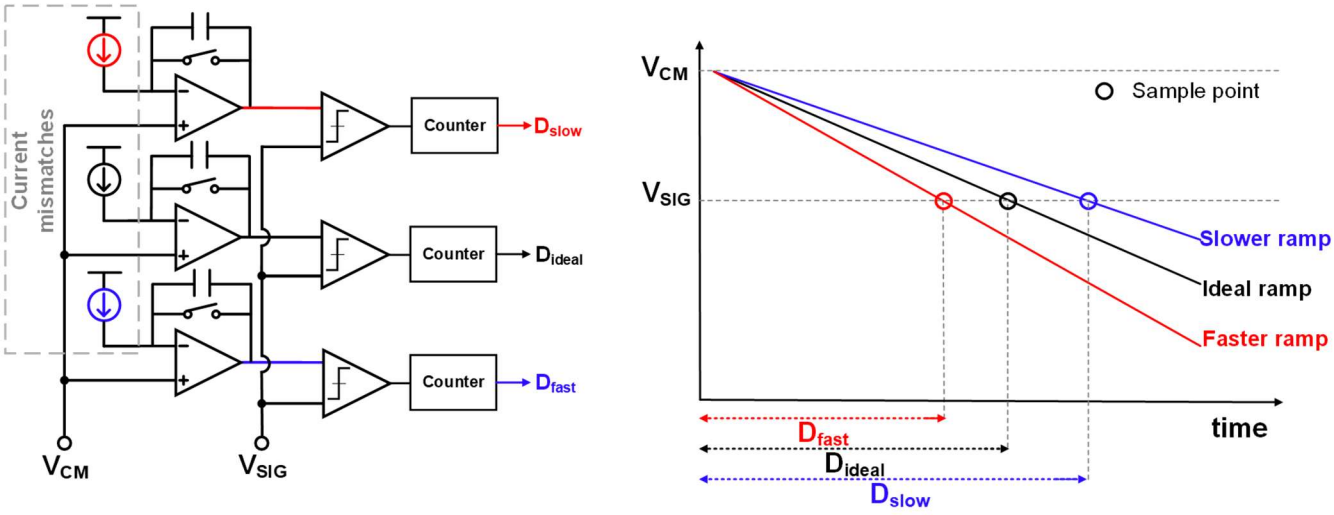


Fig 34. Problem of slope mismatches ($D_{fast} \neq D_{ideal} \neq D_{slow}$)

In proposed ADC scheme, multiple ramp generators are needed for multiple sampling. However, if its slope can be different because of mismatches of integration current source, capacitor and amplifier. Therefore, these ramp generators can provide different values despite of the conversion of the same analog values (V_{SIG}). In other words, from figure 34, D_{fast}, D_{ideal} and D_{slow} are different because of mismatches of ramp slopes

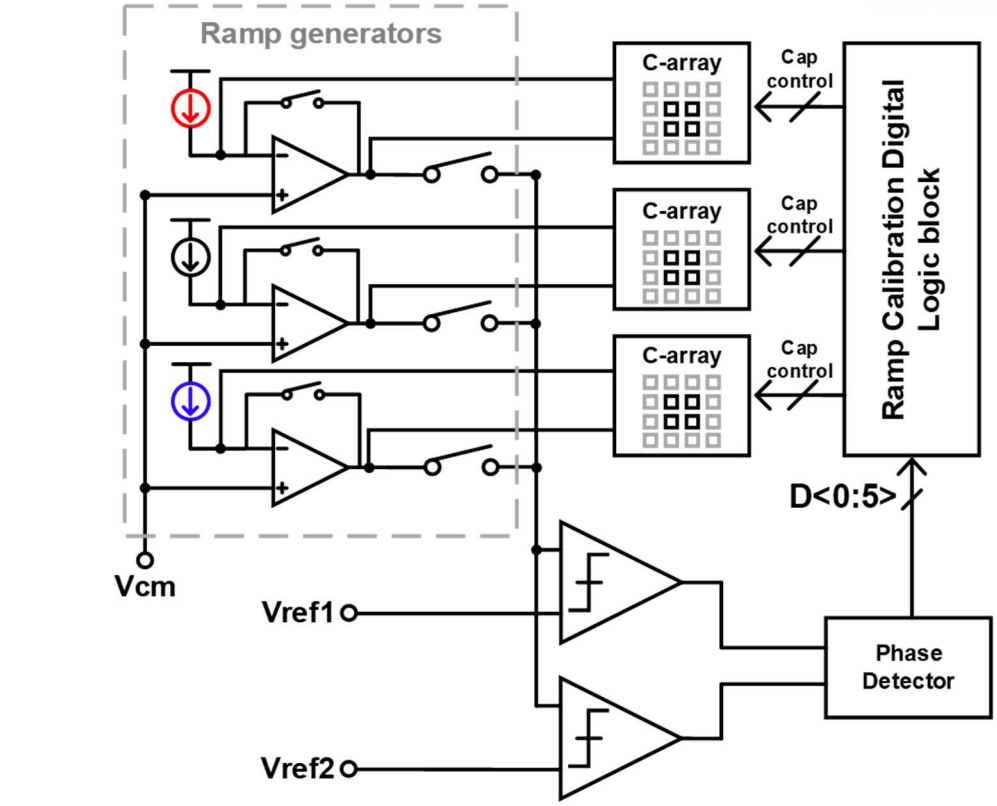


Fig 35. Scheme for cap modifying slope calibration

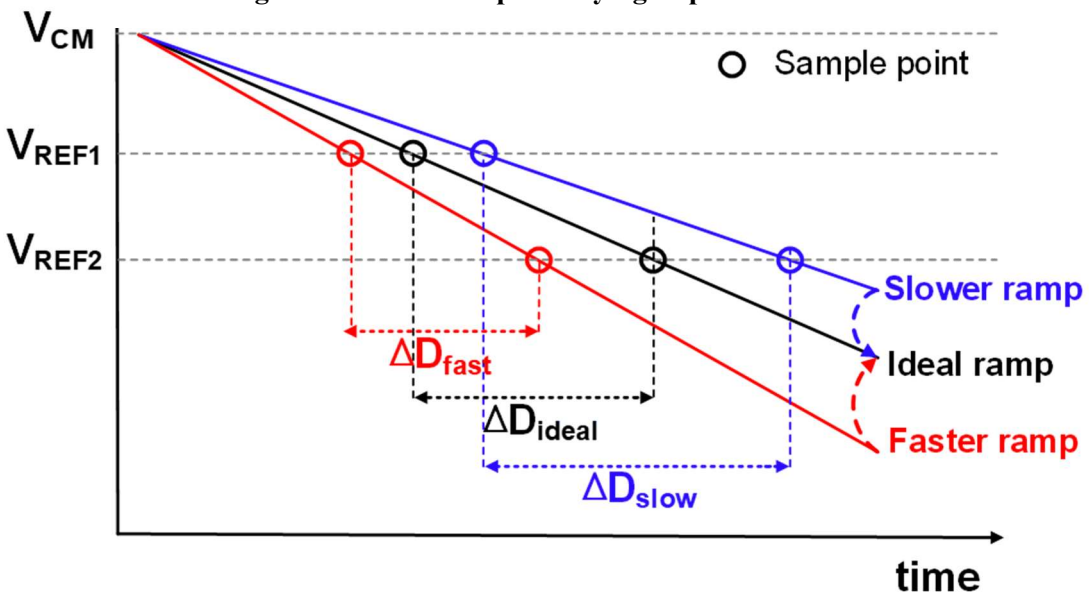


Fig 36. Operation of cap modifying slope calibration

Therefore, to change slope of ramp generators (integrators), we should change the integration current or the number of integration capacitors. To get high resolution for compensation, smaller unit integration current source or smaller unit integration capacitor is needed. However, it is hard to make

small integration current which is lower than 1nA. Therefore, I choose to change the number of integration capacitors for compensate mismatches of ramp generators slopes.

$$D_{ideal} - (\Delta D_x) = \Delta N_{cap}$$
$$N_{ideal\_cap} + \Delta N_{cap} = N_{cali\_cap}$$
※ N: the number of cap

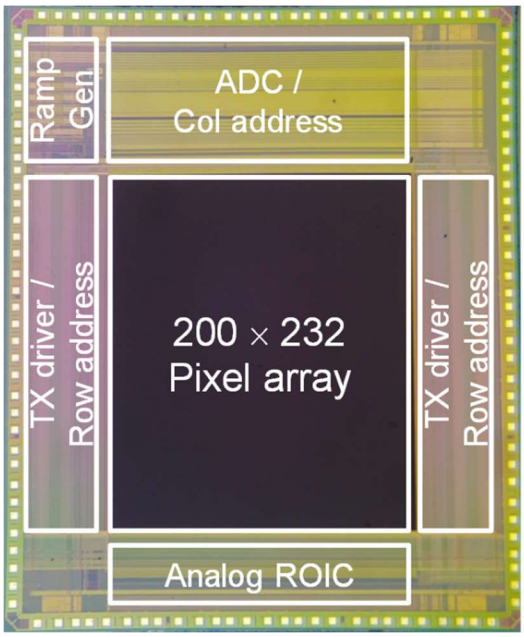
Eq 13. Equation for cap modifying slope calibration

From Eq 13., we can know that D_{ideal} and N_{ideal_cap} because it is intended in our design stage. Then, using two reference voltages (V_{ref1},V_{ref2}) and two comparators, we can detect delta digit values (ΔD_x: ΔD_{slow}, Δ_{Dfast}). We can match ramp slope to ideal ramp slope from these delta digit values by changing the number of capacitors (ΔN_{cap}). Using this scheme, multiple ramp generators can follow ideal ramp generator slope.

Chapter 6.

Measured Results

1. Design specification



I-TOF sensor specification				
Fabrication process	0.11um 1P4M CIS			
Pixel resolution	200 x 232			
Pixel pitch [um]	14.4um			
Chip size [mm²]	30			
Supply [V]	3.3V / 1.5V			
Frame rate [fps]	60			
ADC resolution[bit]	10			
MS number	**16**	**8**	**4**	**2**

Table 5. Design specification table

For enlarging applications of proposed ADC, I designed indirect Time-of-Flight sensor with proposed ADC. Therefore, at the long distance, in other words, when the reflected light is decreased, the depth accuracy with operation of proposed ADC will be increased compared with operation of conventional single-slope ADC because of multiple sampling effects. Sensor was fabricated with 0.11um DBHitek 1P4M for CIS process. The pixel resolution is 200x232 because of large pixel pitch size (14.4um). I used 3.3V for analog block and 1.5V for digital block. Then I can get 60 frame per second with 50Mhz clock signal. ADC resolution is 10bit for mobile applications and multiple sampling number is 16, 8, 4 and 2. Analog ROIC is for testing point of pixel operations. I used NI Labview DAQ system for measuring the performance of sensor and ADC.

2. Multiple sampling effect measurement results

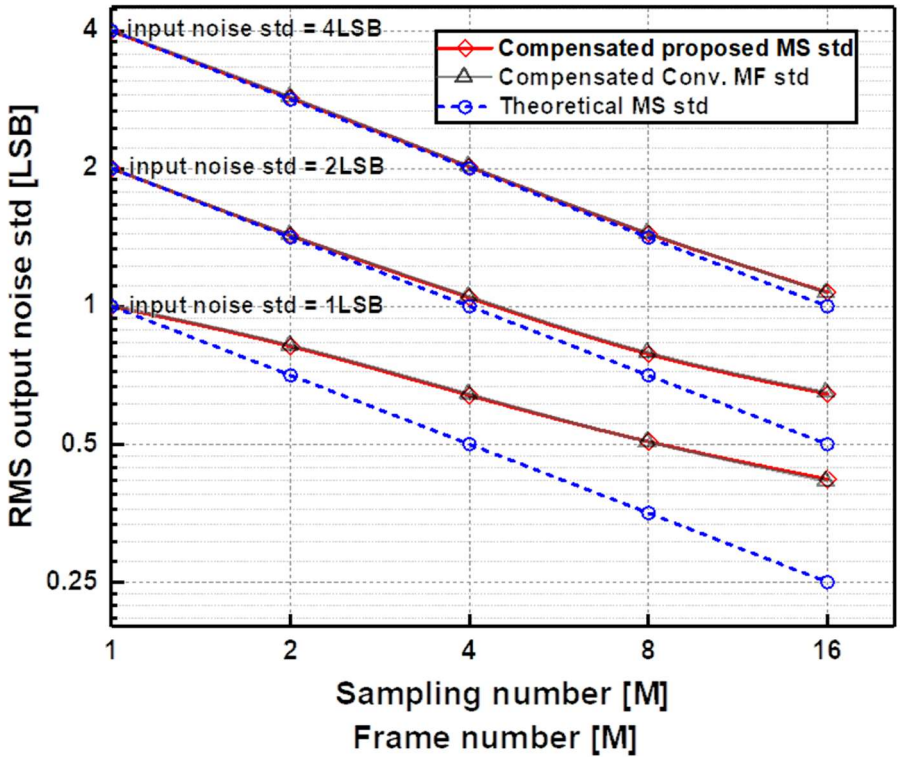
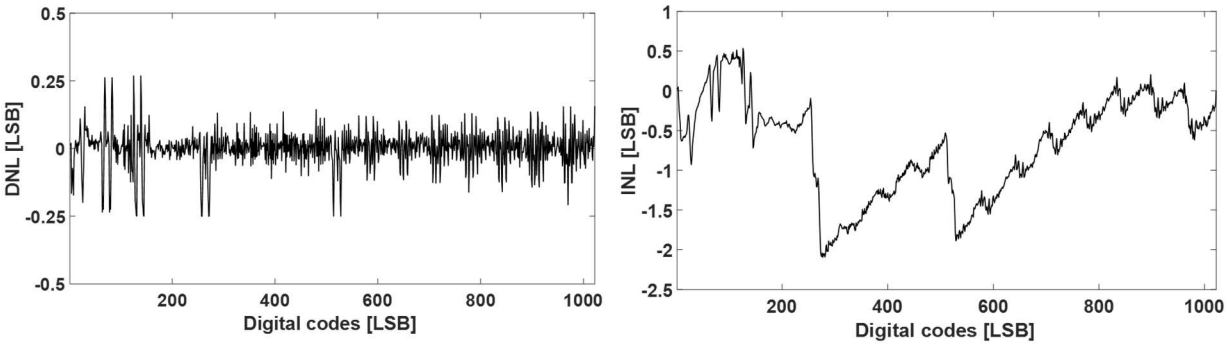


Fig 37. Plot of effects of multiple sampling effect with theoretical curve (MF: multiple frame, MS: multiple sampling)

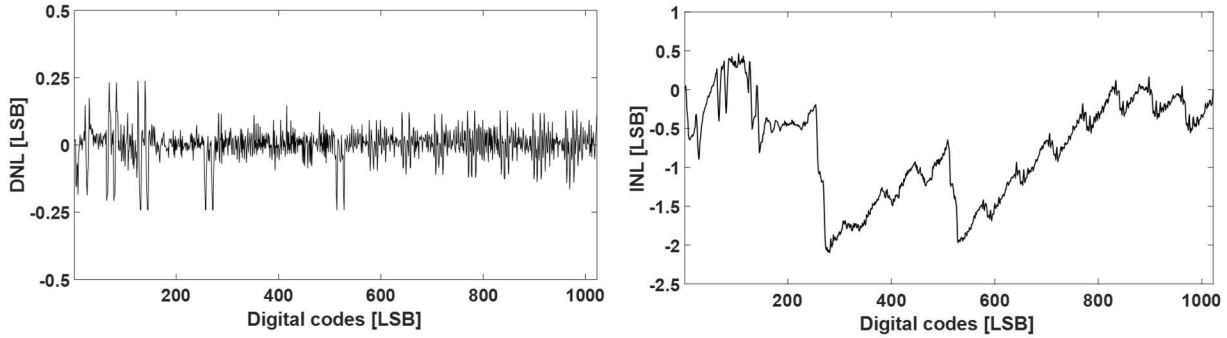
Above figure is showing the effect of multiple sampling with proposed ADC. First, blue line indicate that the theoretical effects of multiple sampling and black line is results of conventional single-slope ADC with multiple frames for indicating effect of conventional multiple sampling effects. Finally, red line is results of proposed ADC with changing the sampling number (input change). As the standard deviation of input noise increases, the multiple sampling become effective. However, if standard deviation is lower than 1LSB, multiple sampling effect is limited because of dominance of quantization noise. Therefore, we can conclude that proposed ADC follow the theoretical effects of multiple sampling well.

3. Linearity measurement



• DNL: +0.268/-0.249 • INL: +0.534/-2.095

Fig 38. DNL and INL results of proposed ADC without slope calibration



• DNL: +0.237/-0.242 • INL: +0.465/-2.093

Fig 39. DNL and INL results of proposed ADC with slope calibration

Because of using multiple ramp generators, Linearity is critical because of mismatches of each ramp generator. However, unlike what we were worried about it, DNL and INL results without slope calibration is good enough. The ADC which have DNL <0.5 LSB is enough for using in image sensors. Also, INL is not critical for image sensors because of photon shot noise make worse the sensor linearity than ADC does. In DNL and INL results with slope calibration, DNL and INL are better slightly. Therefore, we can conclude that slope calibration works well in proposed ADC architecture.

4. Power break

In figure 40, proposed ADCs total power consumption (400 ADCs) is 114mW with multiple ramp generators. However, digital power consumption is larger than other blocks because of multiple ADCs for column-parallel structure. Therefore, for using proposed ADC architecture in CIS, the power consumption of ramp generators is not considerable. In figure 41, this figure is showing power consumption of conventional single-slope ADC. Comparing with it, proposed ADC power increases only 15.1% with maximum 16 sampling number. In addition, in figure 42, it is indicating that the estimation of power consumption of conventional multiple sampling with single-slope ADC for 16 times sampling number. To match frame rate, 16 times faster ADC is needed. Therefore, digital power will increase over 16 times comparing with one of the conventional single-slope ADC. Comparing with it, proposed ADC can decrease 87.8% power consumption with signal-dependency for multiple sampling.

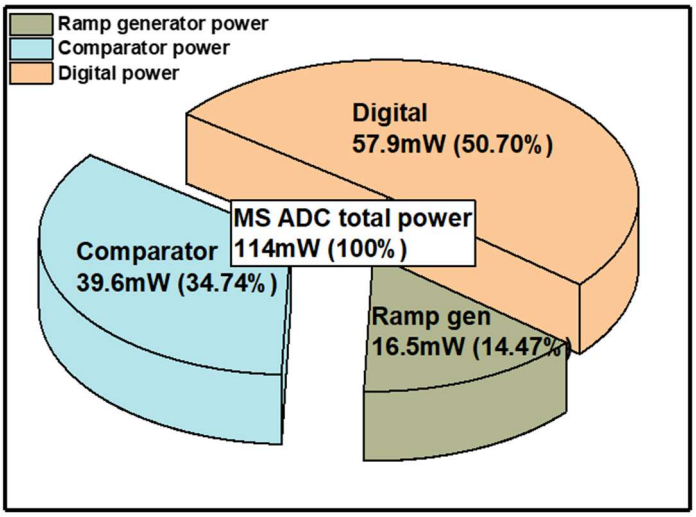


Fig 40. Proposed ADC power consumption (400ADCs)

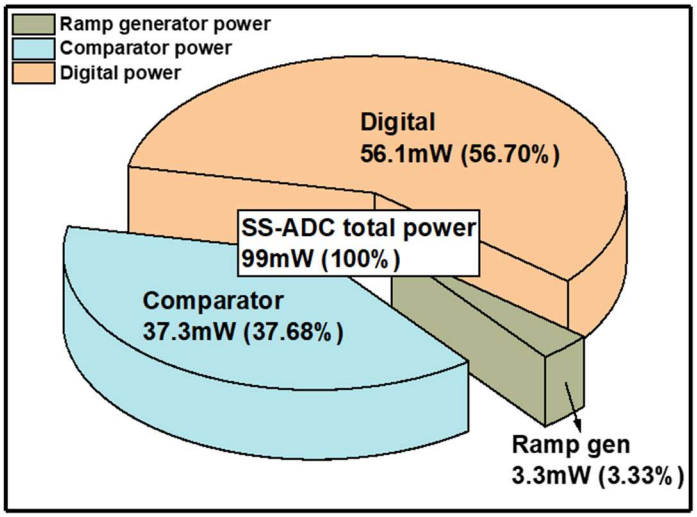


Fig 41. Conventional single-slope ADC power consumption (400 ADCs)

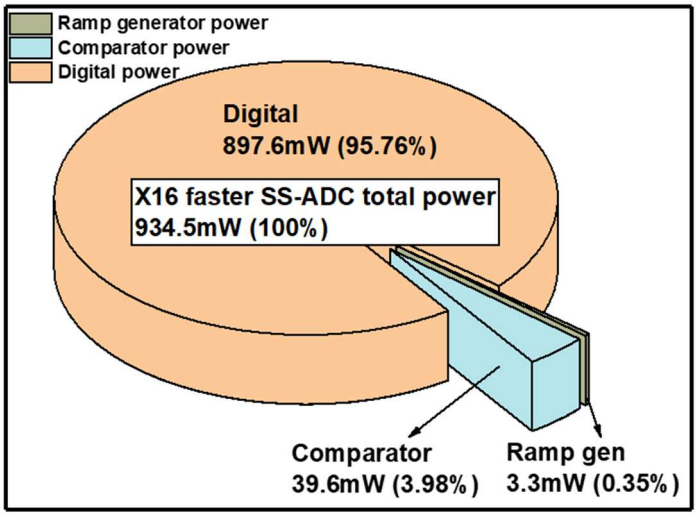


Fig 42. 16 times faster conventional single-slope ADC for 16 sampling number estimated power consumption (400 ADCs)

5. Depth measurement results

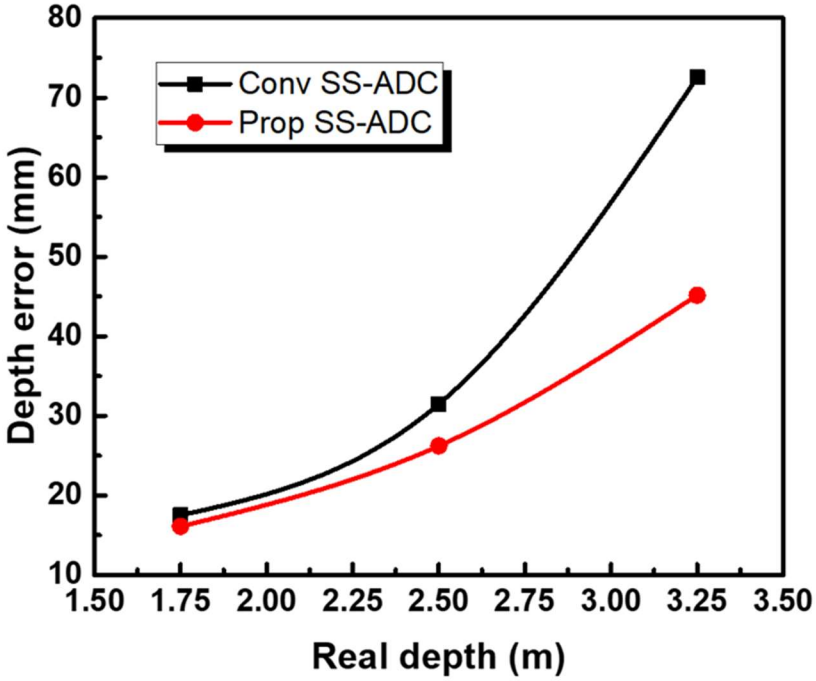


Fig 43. Results of depth accuracy measurement

In figure 43, it is showing the depth accuracy with changing the read depth. In short distance, the reflected light is large enough then depth accuracy is better than long distance. Therefore, in the region, multiple sampling effect is not effective with small sampling number. Only 6% depth error decreases compared with conventional single-slope ADC. However, as the distance increases, the reflected light is small to get good depth accuracy. Therefore, depth error is increased. With proposed ADC, we can suppress depth error by multiple sampling effects to 38% compared with conventional single-slope ADC. Therefore, it is effective not only color imaging but also depth imaging. We can conclude that proposed ADC can be used all of applications of image sensors.

Chapter 7.

Conclusion and further works

1. Conclusion

In this research, several noises coming from pixels and readout circuit can be suppressed by conventional analog circuit techniques. Especially, from the noise characteristics of CIS, noise suppression technique is important in the dark conditions compared with the bright conditions. As we have seen before, using high gain pre-amplifier technique can suppress noises coming from readout circuit. However, it cannot suppress pixel noises because these is in front of the amplifier. Also, pixel output range is limited due to output saturation of amplifier. In other words, dynamic range of CIS is limited due to gain of pre-amplifier. Also, it is hard to be used in low power CIS because of large power consumption of amplifier.

However, multiple sampling technique can suppress not only readout noises but also pixel noises. Also, compared with high gain pre-amplifier technique, power consumption is lower than using high-gain pre-amplifier technique and it can keep the dynamic range of CIS. The biggest drawback to multiple sampling is that increasing readout time proportional to the sampling number. In other words, it increases readout time. In addition, increasing readout time is much more critical for using single-slope ADC which is used dominantly in CIS because its readout speed is much slower than other types of ADC. However, this drawback can be eliminated with proposed signal-dependent multiple sampling technique. It can keep the framerate of CIS via selective sampling number according to the light intensity of pixels. In other words, increasing sampling number in the dark conditions compared with the bright conditions to suppress noise is effective way for increasing the performance of CIS for low light imaging.

I applied proposed signal-dependent multiple sampling technique to I-TOF sensor for demonstrating that proposed ADC can be used all applications based on CIS like color, depth and medical imaging. From the results, depth accuracy of long distance increased significantly due to increasing sampling number automatically while keeping framerate of I-TOF sensor. Also, using proposed cap modifying slope calibration technique, DNL/INL of ADC can be increased without any missing codes. In other words, slopes of multiple ramp generator can be calibrated with simple digital logics.

2. Reset noise (kTC noise) suppression idea in depth imaging

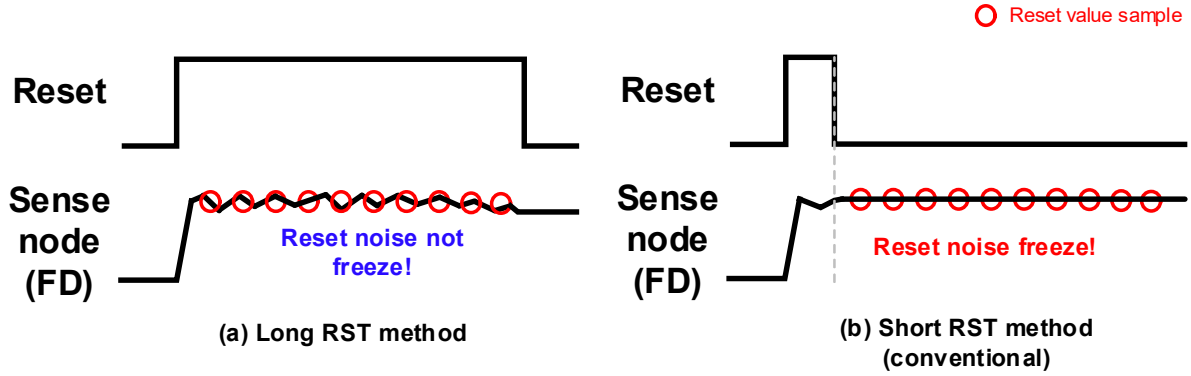


Fig 44. Comparison Long RST method and Short RST method

In chapter 3, we know that Reset noise (kTC noise) is dominant for 3-T pixels because of uncorrelation between reset value and signal value. Therefore, in I-TOF applications, reset noise worsen the depth accuracy. Therefore, to reduce effects of reset noise, by turning on reset transistor in pixel during multiple sampling of reset value, reset value is not freeze and it can be averaged out and it can reduce the noise power to 1/M. Therefore, we can reduce the standard deviation of reset value. In my opinion, accurate analysis about effect of multiple sampling in reset noise is needed. Before analyzing it, I can do measurement with changing digital codes of FPGA in test PCB board.

3. Depth measurement results

In *'short RST'* (conventional reset operation), reset voltage is freeze. Therefore, the effect of multiple sampling is limited to suppress readout noises. However, in *'Long RST'*, reset voltage is not freeze. Therefore, standard deviation of reset value is slight reduced comparing with operation of *'short RST'*. Therefore, depth error reduced by maximum 6.7%. If this analysis works well, we can make more accurate depth sensor via this multiple sampling technique.

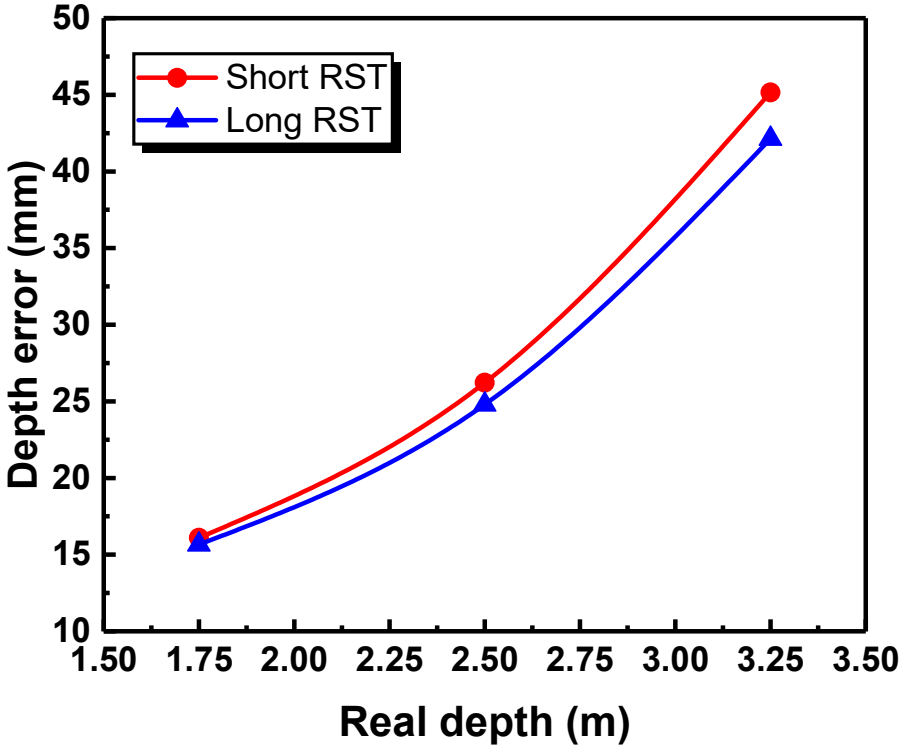


Fig 45. Results of depth accuracy measurement (Long RST vs Short RST)

REFERENCES

[1] D. Stoppa, et al., “Time of Flight image sensors in 0.18 uCMOS technology: A Comparative Overview of Different approaches” Proceedings of the international image sensor workshop, p. 2011.

[2] R. Lange, “3D Time-of-flight distance measurement with custom solid-state image sensors in CMOS/CCD-technology” Ph.D. Dissertation 2000.

[3] S.-J. Kim, et al., “A 1920×1080 3.65μm-Pixel 2D/3D Image Sensor with Split and Binning Pixel Structure in 0.11μm Standard CMOS,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2012, pp. 396-397.

[4] S. Kleinfelder, et al., “A 10 000 frame/s CMOS digital pixel sensor,” IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 2049–2059, Dec. 2001.

[5] F. Tang, et al., "Two-step single slope/SAR ADC with error correction for CMOS image sensor", Sci. World J., vol. 2014, 2014.

[6] M. Kim, et al., “An Area-Efficient and Low-Power 12-b SAR/Single-Slope ADC Without Calibration Method for CMOS Image Sensors” in IEEE Transactions on Electron Devices, vol. 63, issue: 9, Sep. 2016.

[7] S. Kawahito, et al., “Noise Reduction Effects of Column-Parallel Correlated Multiple Sampling and Source-Follower Driving Current Switching for CMOS Image Sensors,” in International Image Sensor Workshop (IISW), Jun. 2009.

[8] Y. Lim, et al., “A 1.1e- Temporal Noise 1/3.2-inch 8Mpixel CMOS Image Sensor using Pseudo-Multiple Sampling,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2010, pp. 396–397.

[9] Y. Shinozuka, et al., “A Single-Slope Based Low-Noise ADC with Input-Signal-Dependent Multiple Sampling Scheme for CMOS Image Sensors,” in Proceeding of IEEE Int. Symp. Circuit and Systems (ISCAS), May 2015, pp. 357-360.

[10] S.-F. Yeh, et al., “A 0.66erms− Temporal-Readout-Noise 3-D-Stacked CMOS Image Sensor With Conditional Correlated Multiple Sampling Technique, IEEE J. Solid-State Circuits, vol. 53, no. 2, pp. 527-537, 2018.

[11] M. F. Snoeij, et al., "Multiple-ramp column-parallel ADC architectures for CMOS image sensors", IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2968-2977, Dec. 2007.

[12] S. Lee, et al., “A Low Noise Single-Slope ADC with Signal-Dependent Multiple Sampling Technique,” in Proc. of International Image Sensor Workshop (IISW), Jun. 2019, pp. 92-94.

[13] S.-J Kim, et al., “A Three-Dimensional Time-of-Flight CMOS Image Sensor With Pinned-Photodiode Pixel Structure,” IEEE Electron Device Lett., vol. 31, no. 11, pp. 1272–1274, Nov. 2010.

[14] B. Razavi, “Noise,” in *Design of Analog CMOS Integrated circuits*. New York: McGraw-Hill Education, 2017, ch. 7, pp. 219-265.

[15] S. Lee, et al., “Design of a Time-of-Flight Sensor With Standard Pinned-Photodiode Devices Toward 100-MHz Modulation Frequency,” IEEE Access, vol. 7, no. 1, pp. 130451-130459, Sep. 2019.

[16] K. H. Lundberg, “Noise Sources in Bulk CMOS,” [Online]. Available: http://web.mit.edu/klund/www/papers/UNP_noise.pdf

[17] Apple, “iPhone 11 pro,” [Online]. Available: https://www.apple.com/kr/iphone-11-pro

[18] A. Mann, “iPhone 11 pro camera review,” [Online]. Available: http://austinmann.com/trek/iphone-11-pro-review-china