THE PEAK WINDOWING FOR PAPR REDUCTION IN SOFTWARE DEFINED RADIO BASE STATIONS[*]

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Abstract. *The utilization of the techniques for Peak to Average Power Ratio (PAPR) reduction makes the wireless infrastructure conform to rigorous telecommunication standard specifications (error vector magnitude (EVM), bit error rate (BER), transmit spectrum mask (TSM)). In modern modulation schemes reduction of PAPR is important requirement for distortion free and energy-efficient operation of power amplifiers (PA). In this paper novel implementation of Peak Windowing method for PAPR reduction in Software Defined Radio (SDR) Base Stations (BS) is presented. The measurement results in terms of EVM and ACPR are given for 5 MHz, 10 MHz, 15 MHz, 20 MHz Long-Term Evolution (LTE) and Wideband Code Division Multiple Access (WCDMA) modulations. In case of 10MHz LTE signal, we achieved PAPR = 8 dB, EVM = 2.0%, ACPR -52dBc at modulated PA output, antenna point.*

Key words: *Peak to Average Power Ratio; Peak Windowing, Software Defined Radio*

1. INTRODUCTION

In radio frequency (RF) transceivers, power amplifiers (PA) consume the most power among the analog circuits; thereby its energy-efficiency is an important design requirement. PA nonlinearity causes high out-of-band radiation, inter-carrier interference and bit error rate (BER) performance degradation. The digital predistortion (DPD) is proven to be an effective method for PA linearization decreasing in-band and out-of-band distortions [2, 3]. DPD improves PA energy-efficiency and reduces the exploitation expenses of RF transceivers. Peak-to-average power ratio (PAPR) of the signal $s(n)$ is defined as the ratio of peak power and the average power of a signal:

$$PAPR_{dB} = 10 \log_{10} \frac{\|s(n)\|_{max}^2}{s_{rms}^2} \qquad (1)$$

Modern modulation schemes exhibit frequent occurrence of large signal peaks. In the presence high PAPR waveforms, PA cannot be efficiently linearized by DPD [4]. The solution which supports the DPD to compensate distortions is dealing with signals with reduced PAPR. In this case it is possible to increase transmitted signal average power, avoid PA operation in non-linear region and improve PA energy efficiency [5]. The utilization of PAPR reduction techniques in modern modulation schemes became an obligation.

The flexibility to implement variety of modulation schemes is important feature of Software Defined Radio (SDR) systems. Because of this property, the SDR is our choice for the implementation of RF Base Station (BS). New implementation of PAPR reduction technique, operating in SDR based BS, is presented in the paper. In conjunction with DPD, it is promising solution to achieve good PA linearity and energy-efficiency.

In the literature there are many studies in which the DPD and PAPR reduction methods are realized using expensive laboratory equipment and where modulated waveforms are produced using Matlab software and Vector Signal Generators (VSG). Our PAPR reduction implementation is based on SDR board which is a part of BS.

To assess the performance of PAPR reduction method we used following figures of merit: Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM). Telecommunication standards define minimum requirements in terms of ACPR and EVM for different modulation schemes [6].

This paper is organized as follows. Related work is given in the following section. The Section III describes the technique for PAPR reduction and implementation in SDR hardware. Measurement results of the PAPR method are presented in Section IV. The results are obtained using following schemes: Long-Term Evolution (LTE) and Wideband Code Division Multiple Access (WCDMA). The Section V is reserved for discussion. Finally; conclusion is drawn in final section.

2. RELATED WORK

A number of methods have been proposed for PAPR reduction. They can be generally divided into two major groups: receiver-dependent methods and receiver-independent methods. In receiver-dependent methods, the PAPR is reduced by increasing complexity of the RF receiver [7]. In this case, the transmitter sends additional data which is decoded at receiver for reliable reconstruction of useful information. The disadvantage of receiver-dependent methods is reduction of data rate which is caused by transmission of additional data. Examples of receiver-dependent methods are Tone Reservation [8], Selective Mapping [9] and Partial Transmit Sequence [10] methods.

The receiver-independent methods don't transmit any additional data and don't modify the structure of receiver. Instead, the shape of the transmitted signals is modified by limiting the magnitude of large peaks [5, 11]. The disadvantage of their utilization is increase of in-band distortions and spectral regrowth. The receiver-independent techniques include Clipping and Filtering (CAF) [12, 13], Peak Windowing (PW) [14], [15], Peak Cancellation (PC).

The CAF is the simplest method for PAPR reduction. Since clipping operation is a nonlinear process it results in high in-band and out-of-band distortions. Clipping operation

is followed by low-pass filtering (LPF) operation which is employed to eliminate the spectrum regrowth.

In PW large signal peaks are multiplied with a specific window function [11]. In an advanced PW proposed in [14], new weighting coefficients are obtained whenever successive peaks are found within a half of the window length. In [15], sequential asymmetric suppression (SAS) PW method and optimally weighted windowing were proposed for PAPR reduction. The focus was to reduce unwanted attenuation of the signal caused by closely spaced peaks.

In [16] a hybrid peak windowing (HPW) is proposed which minimizes the distortion by changing the PAPR reduction method. When a single peak is detected in the period of half of the window length, the peak is shortened using PW. When successive peaks are detected within the same period, the HPW eliminates the peaks using CAF method.

However, an experimental validation of PW method and its disadvantages induced by its application in SDR BS are not reported in the literature.

3. PEAK-TO-AVERAGE POWER RATIO REDUCTION

3.1. Peak Windowing Method

We have adopted PW algorithm for PAPR reduction because it can be easily implemented in SDR BS. Besides, it provides flexibility to apply different modulation schemes. The operation of hard clipping is described by (2):

$$y(n) = c(n)x(n),$$
<div align="right">(2)</div>

where signals $x(n)$ and $y(n)$ represent the input and clipped output signals respectively, each consisting of I and Q signal components. The clipping operation is modeled by $c(n)$:

$$c(n) = \begin{cases} \dfrac{Th}{|x(n)|}, |x(n)| > Th \\ 1, |x(n)| \leq Th \end{cases}$$
<div align="right">(3)</div>

The clipping operation forces peaks in the signal envelope to stay below the threshold, denoted with Th in (3). At the same time, clipping operation produces sharp edges in the $y(n)$ reflecting in increased signal distortion. In PW method, sharp edges of clipped signal peaks are smoothened by multiplication of the original signal in the region of the peaks with a windowing function. To avoid sharp edges in $y(n)$ and keep the signal envelope below Th, the clipping function $c(n)$ is replaced by $b(n)$, given by (4). The Kaiser, Hamming or Hann windowing functions can be used for realization of $w(n)$ [17-18].

$$b(n) = 1 - \sum_{k=-\infty}^{k=\infty} (1 - c(k))w(n-k)$$
<div align="right">(4)</div>

The output signal $y(n)$ is a convolution of the original signal $x(n)$ and the applied windowing function.

$$y(n) = b(n)x(n)$$
<div align="right">(5)</div>
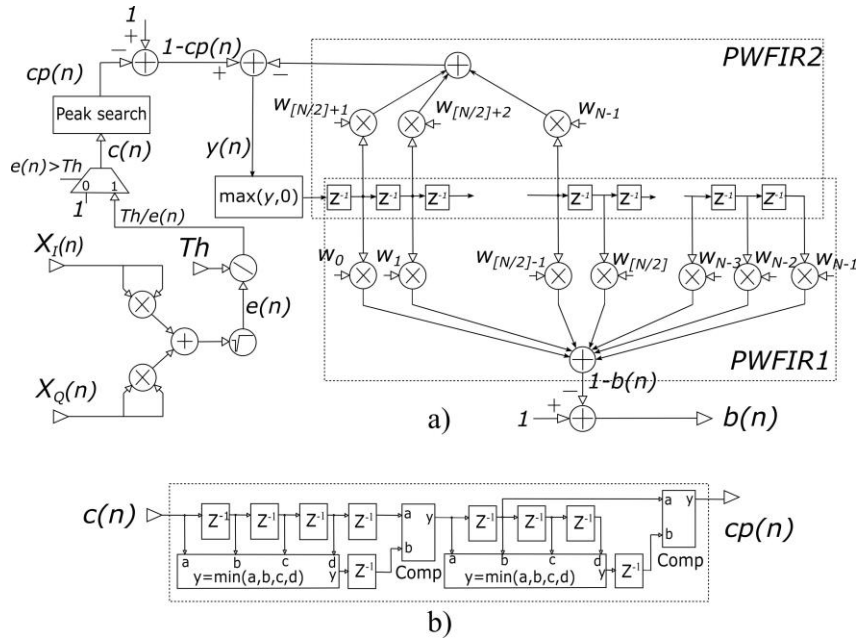
3.2. Peak Windowing Operations

Fig. 1 a) The Peak Windowing PWFIR architecture b) the structure of Peak Search block

The operation described by (4) is implemented by finite impulse response (FIR) filter with symmetric impulse response, denoted with PWFIR, which architecture is described in this section in detail. The implementation of PW consists of several stages. The PW preprocessing operations are depicted in the Fig. 1a [19]. To determine envelope $e(n)$ the I/Q components $x_I(n)$ and $x_Q(n)$ of the input signal are squared, summed and square-rooted. The envelope $e(n)$ is then compared to threshold *Th*. According to (3), if amplitude of $e(n)$ is greater than *Th*, clipping function $c(n)$ is formed as the value of *Th*, divided by $e(n)$. Otherwise, $c(n)$ value is set to one.

The *Peak search* block is introduced in preprocessing stage to find local minimum values of the signal $c(n)$. If a sample is not a local minimum, then the output signal of *Peak search* block (signal $cp(n)$), is set to one. If a sample is recognized as local minimum, the value of this sample is passed to the output $cp(n)$. *Peak search* block examines the sequence of seven consecutive $c(n)$ samples. The value of seven is chosen based on results of simulations in which the LTE 10MHz and WCDMA waveforms are used. The structure of *Peak search* block is given in the Fig. 1b. The operation of block *Comp* is described by (6).

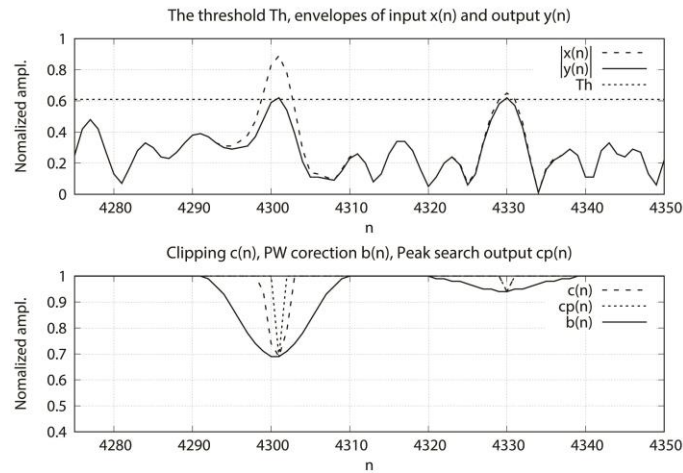$$y(n) = \begin{cases} a, a = b \\ 1, a \neq b \end{cases} \tag{6}$$

Fig. 2 The top panel gives signals *Th*, the envelopes of input and output signals; the bottom panel depicts signals $c(n)$, $cp(n)$ and $b(n)$.

The description of PWFIR filter architecture is presented in the Fig.1a [19]. The PWFIR takes at input signal is $1-cp(n)$ and generates $1-b(n)$. Negative values of $1-cp(n)$ are substituted by zeros. The signal $b(n)$ is used for gain correction of input samples $x_I(n)$ and $x_Q(n)$. Before these signals are multiplied with $b(n)$, they are delayed for the period equal to the delay of PWFIR filter.

The difference between $c(n)$ and $b(n)$ is minimized by choosing narrow window lengths, revealing in decreased EVM values. If clipping operation happens frequently, neighboring windows may overlap and the difference between $c(n)$ and $b(n)$ becomes larger [18]. To reduce windows overlapping the feedback structure is employed. The feedback structure adjusts the input values of $cp(n)$ preventing that the signal is clipped more than it is really needed. The feedback structure reduces the EVM in situations when successive peaks in $cp(n)$ occur within the time interval which is less than half of a window length [19].

The signals, illustrating the PW method, are given in the Fig. 2. Top panel presents the envelope of input signal $x(n)$, containing the peaks that are greater than the threshold level *Th*, and the envelope of the resulting signal $y(n)$, which is constrained to *Th*. The bottom panel depicts the clipping functions $c(n)$, modified clipping function $cp(n)$ and the resulting gain correction signal $b(n)$. As it can be seen from Fig. 2, the amplitudes of local minimum of the signals $c(n)$, $cp(n)$ and $b(n)$ are equal. Also, the amplitude of output signal envelope is precisely limited to *Th*.

3.3. Hardware implementation of PW technique

To implement preprocessing stage, the square, division and square-root circuits are designed. Architecture description of these circuits can be found in [20]. Arithmetic circuits are pipelined and operate at clock frequency which is equal to input and output signals data rate of 30.72 MSps, which is the rate defined by 3G and 4G standards [6]. All arithmetic circuits are implemented in 18-bit fixed point precision which has not influence on PAPR reduction algorithm performance.

PWFIR filter structure, which is depicted in the Fig. 1a, can be divided into two parts, the filter PWFIR1, producing output signal $1-b(n)$, and the PWFIR2 which generates the feedback signal $f(n)$. For filter coefficient implementation we choose the Hann windowing function. The coefficients are generated by following equation:

$$w(k) = \frac{1}{2}\left(1 - \cos(2\pi\frac{k}{N-1})\right), 0 \leq k \leq N-1, \tag{7}$$

where N is the window length.

PWFIR1 is designed as 40-tap FIR filter. The value of $N = 40$ is determined by simulations [21]. For, example, in case of filter size equal to $N = 40$ and clipping threshold of $Th = 0.7$, the out-of-band distortions, obtained at the output of PW block, are minimized down to system's noise floor. The filter length N and coefficients are programmable. Namely, the PWFIR1 block has provision to change filter order in the range from 1 to the maximum equal to 40. Besides, new filter coefficients can easily be loaded.

The architecture of PWFIR1 filter is based on multiply-and-accumulate (MAC) circuitry and it is optimized for implementation in FPGA. The number of utilized multipliers is reduced by multiplexing input data and operation at clock frequency which is four times larger than the sampling rate. The PWFIR1 operates at the clock frequency of 122.88 MHz and input and output data rate is equal to 30.72 MS/s. The architecture is additionally optimized by the fact that filter has linear-phase and therefore, symmetrical coefficients around the center tap. The symmetry of filter coefficients enables additional reduction of the number of multiplication operations by factor of two. The arithmetic precision is 18-bit and it does not impact the PW performance. Architecture utilizes the 18x18 bit embedded FPGA DSP multipliers and provides up to 20 programmable coefficients. The number of coefficients is halved because of coefficients symmetry. As the result of architecture optimizations, the PWFIR1 block occupies only 10 FPGA DSP blocks which are needed for implementation of only five embedded 18x18 bit multipliers.

The detailed architecture of PWFIR1 is given in the Fig. 3a. The PWFIR1 coefficient value at index j is determined by (8) and (9). The coefficients have indexes in range from 0 to 19. Whenever the relation (9) is met, the coefficient at index j is determined by (8). Otherwise, coefficient is equal to zero.

$$h_{PWFIR1}(j) = w\left(j - \left(20 - \left[\frac{N+1}{2}\right]\right)\right) \tag{8}$$

$$20 - \left[\frac{N+1}{2}\right] \leq j \leq 19 \tag{9}$$

In Fig. 3a, signal clk is the clock signal, while enable signal Xen determines input and output data rates. Input signal is sampled at the positive edge of clk whenever $Xen = 1$. Filter coefficients H_i and input samples D_i are stored in Mem and $Dmem$ memory blocks respectively.
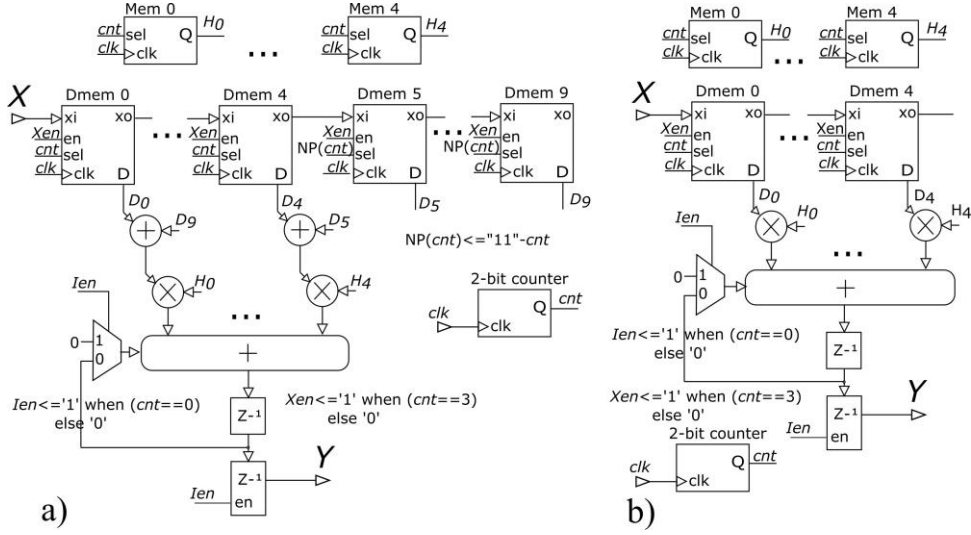
Fig. 3 Architecture of a) PWFIR1 and b) PWFIR2 module

Both *Mem* and *Dmem* are addressed by 2-bit binary counter *cnt*. Five *Mem* blocks provide signals from H_0 to H_4; ten *Dmem* blocks give signals D_0 to D_9. In each clock cycle, outputs *Mem* and *Dmem* are multiplied and the result is fed to the digital integrator:

$$Sum = \sum_{j=0}^{4}(D_j + D_{9-j}) * H_j \tag{10}$$

Delayed input enable signal *Ien* is used to set the integrator feedback signal to zero whenever the calculation starts. After four clock cycles, output signal *Y* calculates the filter output. Output signal *Y* is provided by latching the integrator output controlled by *Ien* as well. At positive edge of *clk* when *Xen* = 1, counter is reset and the process is repeated. The coefficients memory blocks are implemented as dual port register arrays. Similarly, data memory is implemented as single port register array. Multipliers are implemented by 18×18 bit FPGA DSP blocks.

PWFIR2 architecture is given in the Fig. 3b. It provides up to 20 programmable filter coefficients which are stored in a register array and are indexed in the range from 0 to 19. The coefficients of PWFIR2 are determined by (11) whenever condition in (12) is met. Otherwise, coefficient at index *j* is equal to zero.

$$h_{FIR2}(j) = w\left(\left[\frac{N+1}{2}\right] + j\right) \tag{11}$$

$$0 \le j \le \left[\frac{N}{2}\right] - 1 \tag{12}$$

In Fig. 3b five *Mem* blocks provide signals from H_0 to H_4; also five *Dmem* blocks give D_0 to D_4. In each clock cycle, outputs *Mem* and *Dmem* are multiplied and the following sum is calculated:

$$Sum = \sum_{j=0}^{4} D_j \cdot H_j \qquad (13)$$

4. MEASUREMENT RESULTS

In this section, the results of the measurements are reported. [22] We utilized the SDR board which includes a transceiver IC covering the frequency range up to 3.8GHz [23] and additional on-board FPGA IC in which the PAPR reduction circuits are implemented. Test waveform can be uploaded and played from WFM RAM block for the development or demo. In the real applications, WFM RAM blocks are not required. CPU Core performs functions of BB digital modem which are application specific, WCDMA or LTE [24] for example, and provides the input signal of PAPR reduction block.

The PAPR reduction block output signal is filtered by symmetrical 40-TAP low-pass FIR filter. The utilization of FIR filter is necessary because of two reasons. First, it compensates distortions generated by BB digital modem. Else, the FIR filter removes residual out-of-band distortions generated by PAPR reduction block. The filter length, which maximum is equal to 40, is programmable as well the filter coefficients. The FIR provides up to 20 programmable coefficients which can be changed to support utilization of different modulation schemes. The FIR architecture is identical to architecture of PWFIR. The FIR is optimized using the same optimization methods implemented in PWFIR. The time multiplexing and symmetry of coefficients are exploited to reduce the number of FPGA multipliers by factor of 8.

The moderate output power PA with saturated power of 19dBm and supply voltage equal to 5V is used in the measurements. Transmitted signal output power is set to *Pout* = 6 dBm. The SDR board RF center frequency is set to 763 MHz.

The results are reported by analyzing PAPR, ACPR and EVM of the PA output signal. In the measurements the PWFIR filter order *N* is changed (*N* = 9, 19, 29 and 39). Different clipping thresholds *Th* are examined; the value of *Th* is decreased from 1.0 down to 0.6 in steps of 0.04. For each combination of threshold *Th* and filter order *N*, the PAPR, ACPR and EVM are measured by Spectrum Analyzer.

In different test cases following waveforms are used: 5 MHz, 10 MHz, 15 MHz and 20 MHz LTE Test Model 3.1 (E-TM 3.1) and WCDMA. In particular, the E-TM 3.1 test specification applies to most LTE modulation schemes at maximum power, and this specification is regarded as the most rigorous and one of the most important specifications of all EVM test specifications [16].

4.1. Test Case 1: 10MHz LTE Test Model 3.1 Waveform

For E-TM 3.1 10MHz LTE waveform, the cut-off frequency of FIR filter is set to 10MHz. The measured PAPR vs. threshold graph is presented in Fig. 4a. As it can be seen from Fig. 4a, the PAPR vs. threshold curve exhibits almost linearity. The PAPR value of unmodified waveform signal is 10.2dBm. When threshold value is set to 0.7, the PAPR of

output signal is reduced by 3dB. The EVM versus PAPR plot is given in the Fig. 4b. The EVM results are obtained at PA output after waveform is processed by PAPR reduction and low-pass FIR filter blocks. When $Th = 1.0$ is selected, the block for PAPR reduction is bypassed. In this case the EVM is equal to 1.2%. As it is shown in Fig. 4b, the EVM is decreased with reduction of PWFIR filter length N. For example, the combination of $N = 9$ and $Th = 0.6$ yields to EVM = 5.8%. In the case of $N=39$ and $Th = 0.6$, EVM = 7.7%.
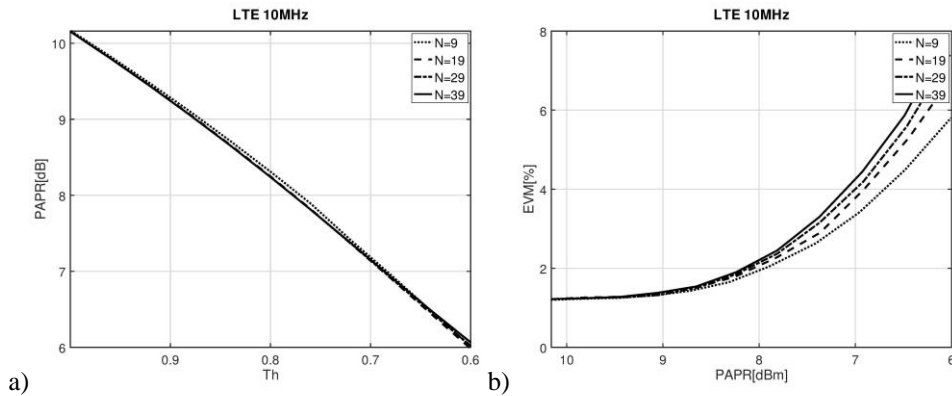

Fig. 4 a) PAPR vs. *Th* for 10MHz LTE; b) EVM for 10MHz LTE as a function of *N* and PAPR.
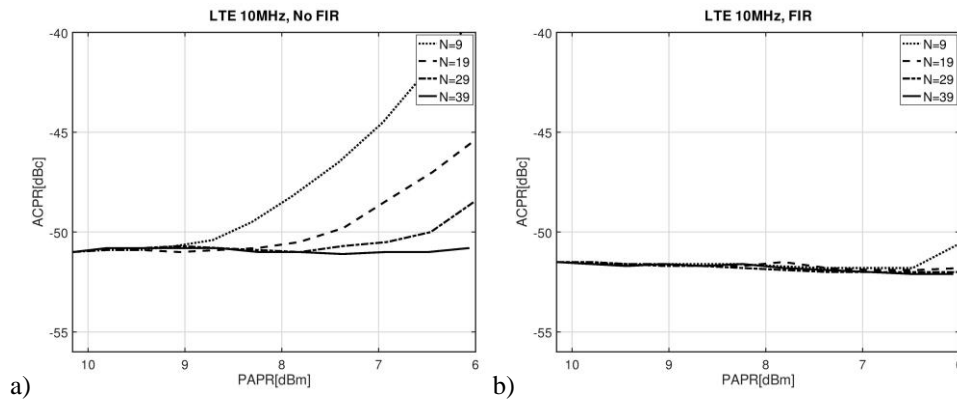

Fig. 5 ACPR for 10MHz LTE as a function of PAPR when: a) FIR filter is not used; b) FIR is applied.

The Figs. 5a and 5b give the ACPR values, obtained at PA output, as a function of PAPR and *N*. The measurements are performed for two cases: when low-pass FIR filtering operation is bypassed and in the case when FIR block is utilized. The figures clearly point the necessity of low-pass filtering. If the filtering is not performed, the ACPR can only be improved when large *N* value is chosen, *N*=29 for example. If low-pass filter is used, the ACPR results become insensitive to selection of *N*. In this case, when parameters $Th = 0.6$

and $N = 19$ are chosen, out-of-band distortions are reduced to the systems noise floor and the ACPR is equal to -52dBc. The utilization of low-pass FIR not only reduces the out-of-band distortions at PW block output but also enables the usage of shorter PWFIR window lengths, which gives better results in terms of EVM. When PAPR is decreased to 8 dB, the EVM = 2% and ACPR = -52dBc.

Similar results stand for In BS application, where the 10 MHz LTE waveform is amplified using 10 W modulated output power PA with integrated DPD. The reduction of PAPR down to 8 dB by proposed block gives the performance at PA output of EVM = 2% and ACPR = -52 dBc, obtained at 39.5 dBm modulated output power.

4.2. Test Case 2: 10 MHz LTE when different window functions are used

In the previous test case Hann window function is applied. However, in the realization of coefficients $w(n)$ different window functions can be used. We considered the other window functions that behave differently from Hann function: the Hamming and Blackman-Harris for example. We measured PAPR, ACPR and EVM values of the signal at PA output in the cases when Hann, Hamming, Blackman-Harris functions are separately applied. The results in terms of ACPR and EVM are given in Fig. 6a and 6b respectively. In the measurements the FIR filter is left bypassed. Different window lengths are considered in the figures: $N = 9$, $N = 19$ and $N = 39$.
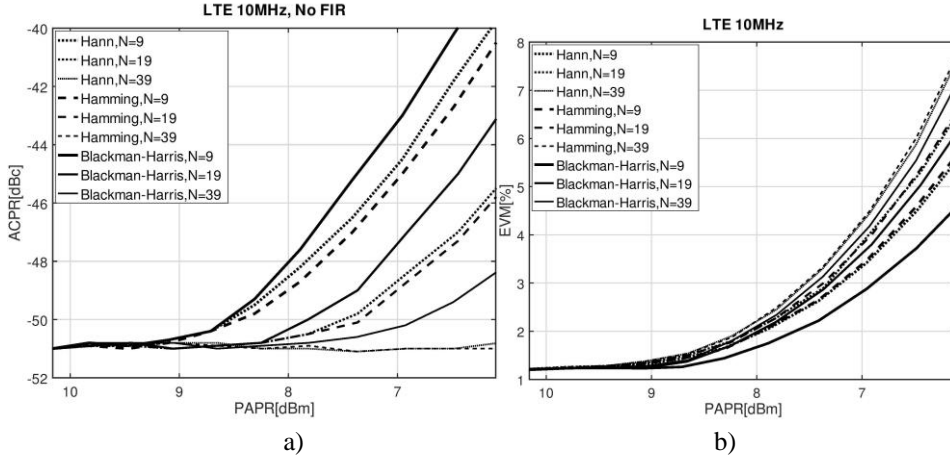

Fig. 6 a) ACPR and b) EVM as a function of PAPR and N when 10MHz LTE waveform and different window functions are used: Hann, Hamming and Blackman-Harris

4.3. Test Case 3: 5 MHz LTE Test Model 3.1

For 5 MHz LTE waveform the cut-off frequency of low-pass FIR filter is set to 5 MHz. In this test case the Hann window function is applied. The EVM versus PAPR plot is given in the Fig. 7a. The Fig. 7b depicts the ACPR results, obtained at PA output, as a function of PAPR and N. These results presented in the Fig. 7b are obtained in the case when low-pass FIR filtering operation is bypassed.

In the case when low-pass FIR block is used and the PAPR is reduced by 2 dB down to PAPR = 8.2 dB, the amount of out-of-band distortions is reduced down to −55 dBc and EVM = 2%.
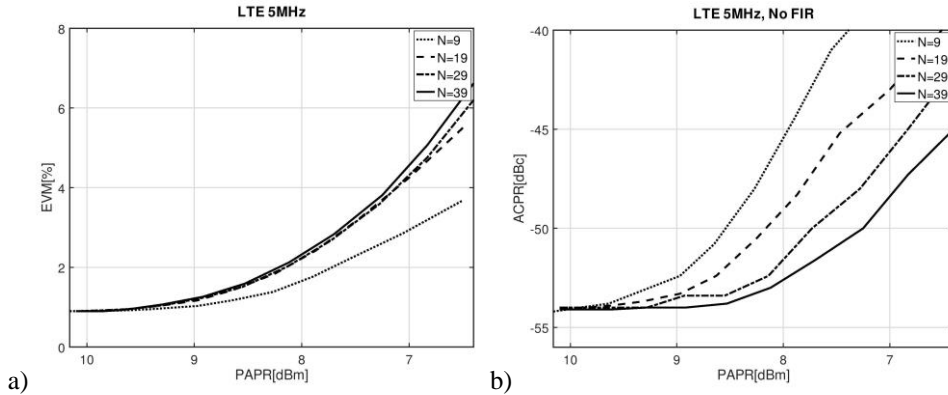
Fig. 7 a) EVM and b) ACPR as a function of *N* and PAPR for 5 MHz LTE

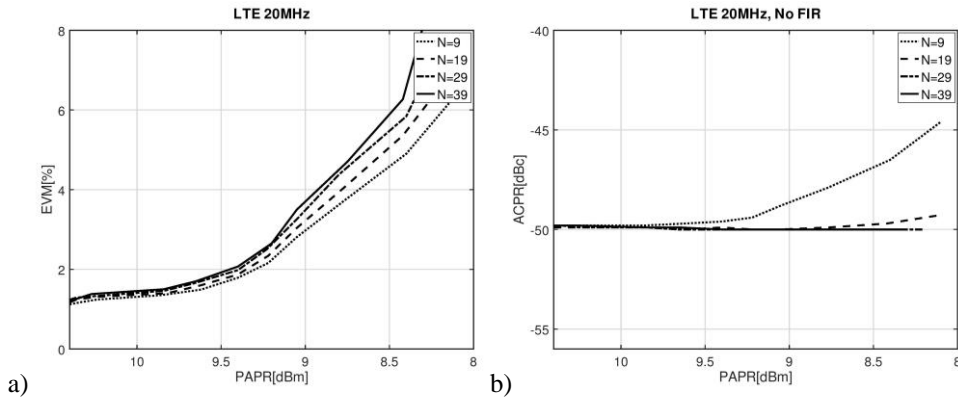### 4.4. Test Case 4: 20 MHz LTE Test Model 3.1

Fig. 8 a) EVM and b) ACPR as a function of *N* and PAPR for 20 MHz LTE.

In the test case of 20 MHz LTE the cut-off frequency of low-pass FIR filter is set to 20 MHz. The results in terms of EVM in ACPR are given in Figs. 8a and 8b respectively. The utilization of low-pass FIR filter is necessary when $N = 9$. In other cases of $N = 19$, $N = 29$ and $N = 39$, the ACPR is equal to −50.2 dBc. When PAPR is decreased by 2dB, the EVM = 5.36%.

4.5. Test Case 5: WDMA Test Model 1

In case of WCDMA Test model 1 waveform, the coefficients for 5 MHz low-pass filter are loaded in the FIR. Besides, we have applied the Hann function. The EVM vs. PAPR plot is given in the Fig. 9a. The PAPR value of unclipped WCDMA signal is

10.6 dBm. The EVM is then 1.1%. When *Th* is reduced to 0.7, the PAPR of output signal is reduced by 3dB. Increase of *N* yields in increase of EVM. The Fig. 9b depicts the ACPR results obtained for WCDMA input waveform when signal filtering is not used. When FIR block is used the out-of-band distortions are reduced to the systems noise floor and ACPR becomes equal to -55dBc.
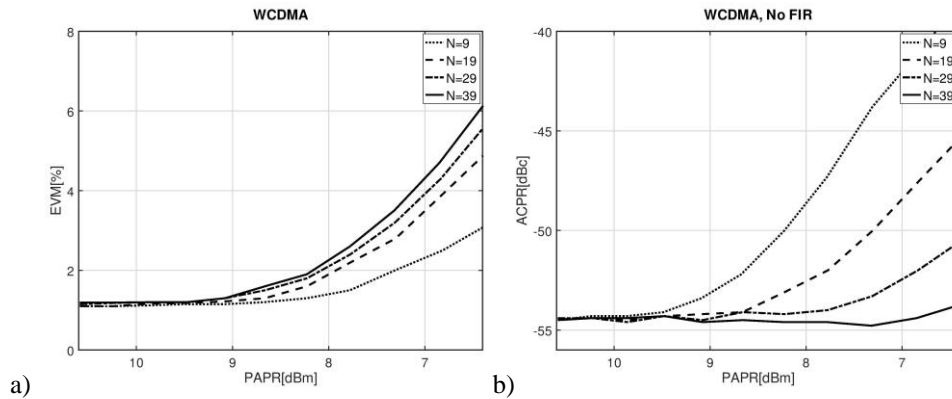

Fig. 9 a) EVM and b) ACPR as a function of *N* and PAPR for WCDMA

5. DISCUSSION

A signal envelope containing high peaks is an unwanted characteristic of modern modulation schemes. This can be seen in the examples of WCDMA and 10MHz LTE waveforms. For the reduction of such high signal peaks we use the PW method.

The original version of PW method, found in [11, 19], is modified by introducing novel *Peak search* block. Compared to the original PW implementation, after utilization of new *Peak Search* block, the absolute value of the difference between local minimum values of gain correction $b(n)$ and the clipping signal $c(n)$ is minimized. This difference is minimized invariantly to the clipped signal amplitude value. As the result of equalization of amplitudes of $b(n)$ and $c(n)$, the peaks in output signal envelope are more accurately constrained to the threshold *Th*, resulting in lower EVM values.

The PWFIR order does not affect the PAPR, but does affect ACPR and EVM. Besides, the ACPR and EVM depend on the threshold level. We investigated the trade-off between smaller PAPR and larger signal distortions.

In our PW implementation, the low-pass FIR is employed to reduce the out-of-band distortions. After processing with the low-pass FIR, high-frequency signal components are eliminated and implemented block manifests improved ACPR performance. As it can be seen from measured results, the out-of-band distortion is reduced down to system's noise floor. Also, the utilization of low–pass FIR enables selection of lower PWFIR window lengths, which yields to lower EVM, conforming strict telecommunication standards [6].

The novel architecture of PWFIR is created to fulfill two main requirements: to be programmable and to save the FPGA resources. The programmability enables changing of modulation scheme by adjustment of PWFIR parameters. Namely, the PWFIR circuit

has provision to change window filter length and filter coefficients. Beside options of modifying the PWFIR configuration, we have option to specify the clipping threshold.

The PWFIR architecture is dedicated for FPGA implementation and it is optimized to save the FPGA chip resources. The number of multipliers in PWFIR is reduced eight times. Time multiplexing reduces the number of multipliers by factor of four. The throughput of PWFIR implementation is equal to sample rate of 30.72 MSps, which is defined by 3G and 4G LTE standards [6]. The circuits operate at clock frequency of 122.88 MHz; this frequency is determined by propagation delays of embedded FPGA multiplier blocks. The PWFIR architecture is additionally optimized by a factor of two exploiting the symmetry of PWFIR filter coefficients. Each of PWFIR1 and PWFIR2 filter occupy exactly 10 FPGA DSP blocks, implementing only five 18×18 bit multipliers. Additional 10 bit multipliers are used for realization of low-pass FIR filter block, which architecture is similar to the architecture of PWFIR filters. The arithmetic precision of digital blocks implemented within FPGA is 18-bit and it does not have influence on PW performance. The utilization of FPGA resources is given in the Table 1.

Table 1 The occupied ALTERA Cyclone V FPGA resources

Digital block	combinatorial ALUT	dedicated logic registers	DSP blocks
PAPR reduction block	2168	3389	14
FIR	1523	2168	10

The results in terms of ACPR, EVM and PAPR, obtained for different modulation schemes – 5 MHz, 10 MHz, 15 MHz, 20 MHz LTE E-TM 3.1 and WCDMA, are summarized in the Table 2. In all measurements the PAPR of input signal is reduced by 2 dB. As bandwidth of waveform is increased, the EVM and ACPR results become worsened. For example, for 20 MHz LTE the ACPR is equal to -50.2 dBc, compared to −55 dBc obtained for 5MHz LTE signal. The EVM of 20 MHz signal is equal to 5.36%.

Table 2 The measured ACPR, EVM and PAPR for 5MHz, 10MHz, 15MHz, 20 MHz and WCDMA when PAPR of input waveform is reduced by 2dB

	5 MHz LTE	10 MHz LTE	15 MHz LTE	20 MHz LTE	WCDMA
ACPR[dBc]	-55	-51.8	-51.3	-50.2	-55
EVM[%]	1.9	1.9	2.93	5.36	1.4
PAPR[dB]	8.2	8.2	8.2	8.4	8.6

In order to evaluate the performance of the proposed PAPR reduction, it is compared with the CAF [12], original PW [14] and HPW [16] methods which are found in literature. The PWFIR filter length $N = 19$ and the LTE 10MHz E-TM 3.1 waveform are used. Fig. 10 summarizes the performance comparison of proposed method and the existing methods. The proposed method outperforms the CAF, original PW and HPW schemes in terms of the EVM. Besides, the measured EVM is much below than EVM = 8%, the value required by standards, even in the case when PAPR is reduced down to 6 dB.
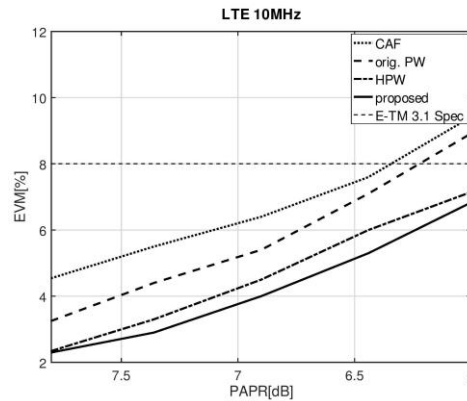
Fig. 10 Comparison of EVM vs. PAPR plots of proposed method with references. The
          LTE 10MHz E-TM 3.1 waveform is used

Different window functions are considered in the realization of PWFIR filter. Han
and Hamming functions produce similar results in EVM and ACPR. The Blackman
Harris gives better results in EVM but ACPR is significantly worsened. In the papers
which are used for comparison, waveforms are generated by laboratory equipment. After
the waveforms are processed by Matlab software, implementing the PAPR reduction,
they are up-converted to RF by VSG. In all references the DAC resolution is greater or
equal than 14 bits. In our case the resolution of input waveforms, as well as the resolution
of embedded DAC, located in LMS7002 transceiver IC, is equal to 12 bits.

6. CONCLUSION

The state-of-the-art modulation schemes exhibit large PAPR values, enhancing the
non-linear effects of power amplifiers (PA) and increasing the running cost of RF base
stations. This paper presents novel Peak Windowing PAPR reduction method dedicated
for implementation in SDR based RF base stations. The PA is constrained to operate
within its linear region using PW method which employs low-pass filtering for complete
elimination of residual out-of-band distortion. Besides, the novel *Peak search* block is
created in preprocessing stage of PW to precisely constrain the envelope of the output
signal to selected threshold. In conjunction with feedback path in PW architecture, the
Peak search block reduces amount of in-band distortion. The advantage of implemented
hardware is that it can be used in different modulation schemes. Namely, to support
various schemes, the PW module provides adjustment of different window lengths,
threshold levels and loading of new filter coefficients. To demonstrate performance of
PAPR reduction method the WCDMA, 5MHz, 10MHz, 15MHz and 20MHz LTE
modulations are utilized. The PAPR, EVM and ACPR are obtained by spectrum analyzer
at PA output, antenna point. We show that proposed method exhibits better performance
in terms of in-band distortions than the receiver-independent methods found in literature.
Besides, novel PAPR reduction architecture reduces the number of embedded multipliers
and it is therefore suitable for implementation in FPGA ICs.

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