A Method for Improving Conversion Rate and Accuracy of a Capacitance-to-Digital Converter

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***Abstract*—Capacitance-to-Digital Converter (CDC) ICs available in the market use square wave excitation signals but a sinusoidal excitation is preferred in various applications, such as ice detection, liquid level measurement, humidity measurement, proximity sensing, etc. A dual slope technique based CDC that employs a sinusoidal excitation has been reported recently, but it requires a large number of excitation cycles, to complete an accurate conversion. This paper presents an improved CDC that employs a specially designed method to achieve high accuracy even when a much smaller number of excitation cycles, than the reported scheme, are employed to complete the conversion. A prototype CDC has been developed and tested. In comparison with an existing CDC, the new CDC achieved a substantial reduction (by a factor of 4000) in the number of excitation cycles during integration period, resulting in an improved update rate. Worst case error observed from the prototype CDC was less than 0.24%.**

Keywords-capacitance-to-digital converter; sinusoidal excitation; conversion rate; accuracy; capacitive sensor.

I. INTRODUCTION

Industrial and scientific applications of capacitive sensors are numerous [1], [2]. Some of the important applications are ice detection [3], proximity sensing [4]-[6] humidity measurement [7], flow measurement [8], etc. Change in capacitance of the sensor is conventionally measured using bridge based circuits [9], phase sensitive detection based schemes [10] followed by an analog-to-digital converter for digitized output. Capacitance-to-Digital Converters (CDC), in which the capacitive sensor is an integral part of the CDC that provides a direct digital output are also available. These CDCs work based on charge balance, dual-slope [11], sigma-delta [12] techniques. In many capacitive sensing applications, a sinusoidal excitation is preferred [1], [5]-[8], [13], [14] but most of the CDCs available [11], [12] use dc or square wave excitation. Recently, a CDC that uses a sinusoidal source as excitation was developed [15]. Though it possesses all the advantages such as high accuracy, immunity to noise, etc. of a dual-slope converter [16], it requires a large number of excitation cycles to complete an accurate conversion, leading to a low conversion speed. It will be advantageous if the conversion speed can be increased without losing its accuracy. In this paper, a method is proposed to achieve fast conversion rates keeping its accuracy high. Operation of the CDC, methodology to achieve high accuracy even at high conversion speeds, details of the prototype developed and test results are discussed in the rest of the paper.

II. CAPACITANCE-TO-DIGITAL CONVERTER WITH SINUSOIDAL EXCITATION

A. Operation of the CDC

A block diagram of a dual-slope CDC that provides digital value of capacitance of the sensor, which is excited with a sinusoidal electrical excitation [15] is given in Fig. 1. A brief note on operation of the same is given in this section. Capacitive sensor C_x is an integral part of the CDC. The CDC has a known capacitance C_S, switches S_1, S_2 and S_3, control and logic unit (CLU) along with an integrator formed by opamp OA, resistance R and feedback capacitor C_F. The sensor is excited from source $v_{in} = V_m \sin\omega t$, where $\omega = 2\pi f$ and $f = 1/T$, T is the time period of excitation sine wave. The CDC has two phases of operation, an auto-zero phase and a conversion phase. The conversion phase consists of a preset integration period of time T_1 and a de-integration period T_2 as shown in Fig. 2. During T_1, the CLU sets S_1 in position-1 causing a charging current $C_x \omega V_m \cos\omega t$ to flow through the capacitor C_x. This current, also flows through Z_{F1}. In the prototype, Z_{F1} was realized using a capacitor C_{F1}. The output v_{o1} of the charge amplifier, formed using OA_1, is given to node-1 of S_2 and also to an amplifier with gain -1 (formed by opamp OA_2, two resistors R_A). Its output $v_{o2} = - v_{o1}$. It is given to node-0 of S_2. Voltage signals v_{o1} and v_{o2} can be represented as $v_{o1} = -(C_x/C_{F1})V_m \sin\omega t$ and $v_{o2} = (C_x/C_{F1})V_m \sin\omega t$ respectively. S_3 is in position-1 throughout T_1. The CLU keeps S_2 in position-0 for $v_{in} > 0$ otherwise it is in position-1. CLU gets the data about $v_{in} > 0$ or not, via comparator OC_1. Thus, during T_1, the resulting voltage v_i at the input of the integrator will be uni-polar as indicated in Fig. 2. Thus, for every half cycle of v_{o1}, output v_{oi} of integrator will change by V_{KX}, where V_{KX} is given by (1).

$$V_{KX} = -C_x(2V_m / R\omega C_{F1} C_F). \tag{1}$$

During the interval of first half cycle, the charge transferred $Q(t)$ to C_F can be represented by (2). At the end of $T/2$, total charge stored in C_F is $Q_{\left(\frac{T_C}{2}\right)} = V_{KX} C_F$.

$$Q(t)\Big|^{T_1} = \frac{|V_{KX}|}{2} C_F (1 - \cos\omega t) \tag{2}$$

During the negative half cycle of v_{o1}, the v_i remains a positive signal due to the action of CLU and S_2 as mentioned above. Thus on completion of one excitation cycle, the charge

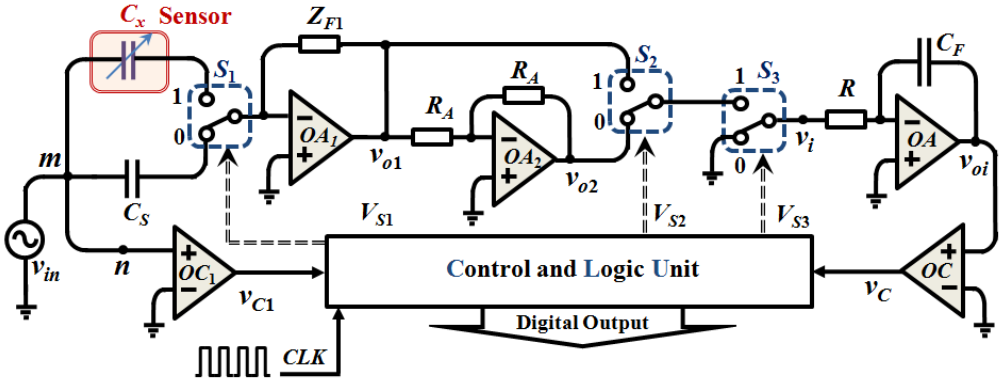

Fig. 1. Block diagram representation of the proposed CDC with a high frequency clock source *CLK*. Details of the clock is explained in section-III. Operation of the circuit is given in section-II. C_x is the sensor capacitance and C_S is a known capacitor.

acquired by C_F will be $2Q_{\left(\frac{T_C}{2}\right)} = 2V_{KX}C_F$, and corresponding change in v_{oi} will be $2V_{KX}$. This process is continued till time $t = T_1 = N_1T$, where N_1 is the number of excitation cycles in T_1 as shown in Fig. 2. Total charge $Q(T_1)$ acquired by C_F during T_1 is given by (3).

$$Q(T_1) = 2N_1|V_{KX}|C_F = 4N_1C_x(V_m / R\omega C_{F1}) \qquad (3)$$

As soon as integration period ends, the CLU sets S_1 to position-0, including the known capacitance C_S in the circuit. Switch S_3 is maintained at position-1 during T_2. The voltage signals v_{o1} and v_{o2} will be then, $v_{o1} = -(C_S/C_{F1})V_m \sin\omega t$ and $v_{o2} = (C_S/C_{F1})V_m \sin\omega t$ respectively.

In de-integration period T_2, the CLU keeps S_2 in 1 whenever $v_{in} > 0$ and in 0, otherwise. The resulting signal v_i during T_2 is shown in Fig. 2. On completion of first half cycle of v_i, during T_2, the integrator voltage will change by V_{KS}, as given in (4). The change in v_{oi} is in such a way that it progresses towards zero. The charge $Q(t)|^{T_2}$ in C_F as a function of time can be represented as in (5). The same occurs during the next half cycle and total change in charge in C_F after one full cycle of input excitation will be $2Q_{\left(\frac{T_C}{2}\right)} = 2V_{KS}C_F$.

$$V_{KS} = C_S(2v_m / R\omega C_{F1}C_F). \qquad (4)$$

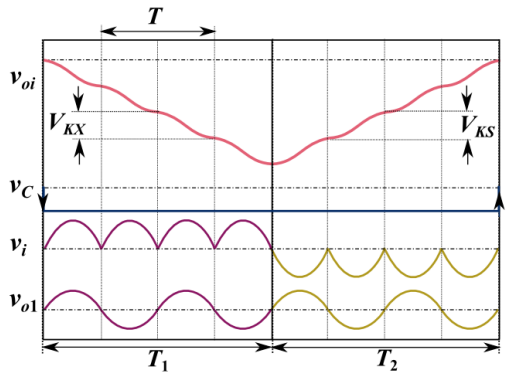

Fig. 2. Voltage signals at important nodes of the CDC, when $C_x = C_S$. v_{o1}, v_i, v_C, v_{oi} represent output of OA_1, input signal to integrator, output of comparator *OC* and integrator output respectively.

$$Q(t)|^{T_2} = \left|\frac{V_{KS}}{2}C_F(\cos\omega t - 1)\right| \qquad (5)$$

This process will continue till all the charge acquired during T_1 is discharged (v_{oi} becomes zero at this point) and the comparator output v_C changes from low to high as in Fig. 2. This is recognized by CLU as end of conversion phase. The de-integration time T_2 (= N_2T) is noted using counter unit of CLU. Total charge acquired during T_2 is given in (6).

$$Q(T_2) = 2N_2V_{KS}C_F = 4N_2C_S(V_m / R\omega C_{F1}) \qquad (6)$$

This is equal to the magnitude of total charge acquired by C_F during T_1, given in (3), thus we can write

$$4N_1C_x(V_m / R\omega C_{F1}) = 4N_2C_S(V_m / R\omega C_{F1})$$

Or, we can represent unknown capacitance C_x as in (7), where N_1 is a preset count, N_2 is a measured count and C_S is a known capacitance.

$$C_x = (N_2 / N_1)C_S \qquad (7)$$

B. Measurement Clock Signal, CLK

The time T_1 is generated and time T_2 is measured using the counter in the CLU. This counter can use a clock which can have a higher frequency f_C than excitation frequency f, i.e.,

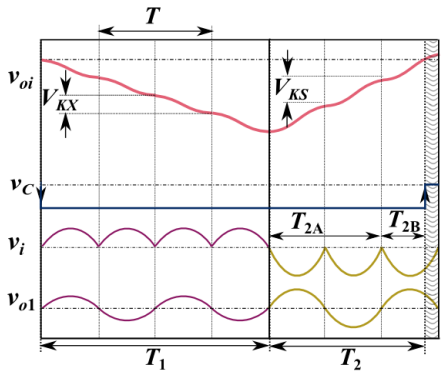

Fig. 3. Voltage signals at important nodes of the CDC, when $C_x < C_S$. The conversion is complete before completion (partial cycle shown in shaded area) of the final/last excitation cycle. This will introduce a large non-linear error in the output, especially for small values of N_2.

$f_C = nf$, where n is an integer. In such a case, T_1 can be represented as $T_1 = N_{1C}T_C$, where N_{1C} is the number of clock counts required to complete T_1 and T_C is the clock period. Similarly, the de-integration time T_2 will get modified as $T_2 = N_{2C}T_C$, where N_{2C} is the number of clocks taken to complete T_2. Thus, (7) will get modified as in (8).

$$C_x = (N_{2C} / N_{1C})C_S \tag{8}$$

C. Non-linear Error and Conversion Rate

The above expressions (7) and (8) are valid when C_x is an integer multiple of C_S. For example, if $C_x < C_S$ then v_i and V_{KX} during T_1 and v_{oi} at the end of T_1 will be less than that shown in Fig. 2. Waveforms for such a condition are shown in Fig. 3. Since C_S has not changed, the value of V_{KS} will remain same. In this condition, during T_2, the v_{oi} will reach zero before completion of a half cycle of v_i as indicated in Fig. 3. Since the charge transfer during the cycle is not a linear function of time, as in (5), such a situation will introduce an error in the computation of C_x, using (7).

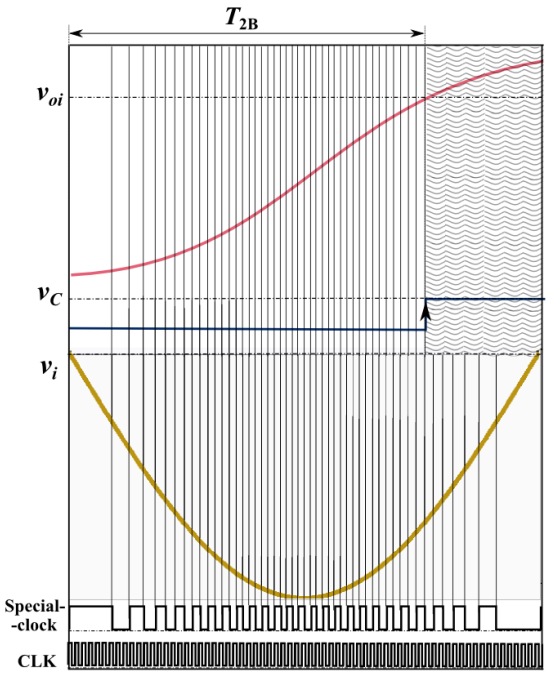

Fig. 4. Exploded view of the final cycle during T_2, indicated in Fig. 3. Conversion is complete during this cycle; hence charge transferred to C_F by this partial cycle (time before wavy shaded area) of v_i is less than $V_{KS}C_F$. As the charge transferred to C_F during this cycle is not linearly related to time, this introduces an error in calculation of C_x, which can be large when a few number of excitation cycles are used as in Fig. 2 and Fig. 3. In this figure, the v_i is sliced into 50 equal areas (in this drawing, this number is chosen arbitrarily as an example and it can be much larger than 50, in actual practice). The vertical lines separate these equal areas. Charge transferred to C_F by each of these areas is equal $V_{KS}C_F/50$. By using this information, i.e., the number of equal areas within the partial cycle, the error introduced in the conversion can be substantially reduced. This can be achieved using (a) look-up table, (b) a suitable algorithm or (c) a special clock as shown. If a normal clock is used [for methods (a) and (b)] for measurement of time, then, its time period should be smaller than the smallest width of the equal area indicated.

This non-linearity occurs only in the final excitation (half) cycle. Thus, if we choose a large value for N_2 (and N_1), the associated error will be relatively small. But, this directly increases conversion time [15], leading to very low conversion rate. Next section discusses a method to correct for this non-linearity, hence enabling the CDC to complete the conversion in a few cycles of input excitation, significantly improving the conversion rate.

III. A Method for Acheiving a High-Speed CDC Having Negligible Non-linear Error Owing to Partial Excitation Cycle

Let us split the de-integration period T_2 into two parts, T_{2A} and T_{2B}. T_{2A} represents the time taken to complete the full-cycles of v_i, while T_{2B} indicates the duration of partial cycle of v_i as indicated in Fig. 3. For the case shown in Fig. 3, $T_{2A} = T$ (two complete half cycles of input excitation). When we measure the time using a high frequency clock as described in Section II-*B*, the total count of the counter during T_2 can be split into counts N_{2CA} during T_{2A} and counts N_{2CB} for the duration T_{2B}. In such a case, (8) will get modified as

$$C_x = \left[\frac{N_{2CA}}{N_{1C}} + \frac{N_{2CB}}{N_{1C}}\right]C_S . \tag{9}$$

N_{2CA} represents counts corresponding to complete cycles of v_i while that of N_{2CB} gives the counts corresponding to the partial half-cycle. As mentioned in the previous section, there will be error (associated with term N_{2CB}) in the computation of C_x as the charge transfer to C_F is not linearly related to time and hence count N_{2CB}, within a cycle of v_i.

If the charge transferred to the C_F within a half-cycle of v_i can be split into small but equal amount of charge packets and if CLU counts the number of packets during the time T_{2B}, we will get a count that is linearly related to the actual charge transferred to C_F. For example, Fig. 4 shows a half-cycle of v_i which is split into m (= 50) portions, each having equal area. Each equal area portion in v_i contribute an equal amount of charge (or charge packet) to C_F. Once the measurement of T_{2B} is made using *CLK*. The number of charge packets within this period can be obtained by various methods including (a) using a look-up table of computed and stored values of number of charge packets for each N_{2CB} in a half-cycle, or (b) once the N_{2CB} is known from counter, the number of charge packets can be computed using the expression (10).

$$N^m_{2CB} = n\left[1 - \cos\left(2\pi N_{2CB}/n\right)\right]/4 \tag{10}$$

Then the corrected count $N^m_{2C}(= N_{2CA} + N^m_{2CB})$ during T_{2B} can be used to compute C_x, given in (9). A flow chart for implementing this method is given in Fig. 5. The third method is (c) by employing a circuit to generate a special clock. The special clock signal will have a transition (either from low to high or vice versa) whenever charge in C_F reaches that of value of a charge packet (corresponding to equal area). The circuit that provides such a special clock is given in Fig. 6. Input to this circuit is v_{in}, as indicated. It has two switches S_4 and S_5, an integrator, a comparator OC_2 which controls the switch S_5,

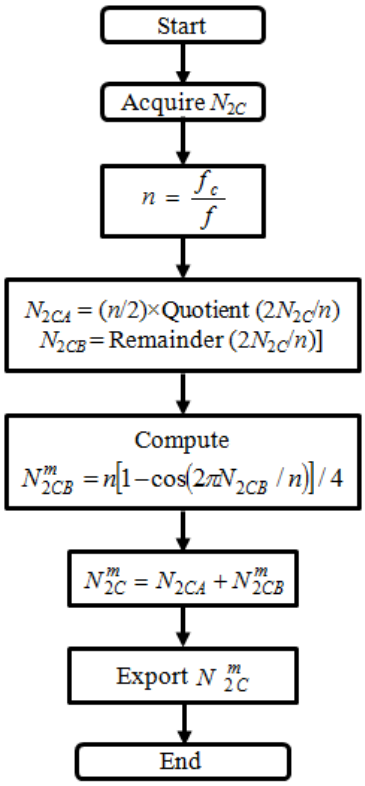

Fig. 5. Algorithm showing the steps for obtaining N_{2C}^{m} which will have less non-linear error compared to count N_{2C} obtained from the counter part of the CDC.

comparator OC_1 (from the proposed CDC shown in Fig. 1) and a XOR gate which controls switch S_4 . Let us assume, initially that the v_{oi2} is lower than V_R (a dc voltage) and output of OC_2 is high. Then S_4 is in position-0 and S_5 will be in position-1. Since now (in this condition) input to integrator is connected to $-v_{in}$, v_{oi2} will increase with time. Once v_{oi2} reaches V_R, the OC_2 will change its state from high to low setting S_4 to position-1 and S_5 to position-0. In this case, integrator input is connected to v_{in}, hence the integrator voltage v_{oi2} will decrease towards zero. Once it reaches zero, OC_2 will change its state to high. Then the circuit operates as explained above. The above explanation for position of switch S_4 is valid for $v_{in} > 0$. For $v_{in} < 0$, the switch S_4 will be in position-1 when OC_2 is high. It will be at 0, otherwise. This is ensured by the action of an XOR gate. By doing this, it makes sure that if integrator has to go towards zero, its input will be $-v_{in}$ (which is a positive quantity as $v_{in} < 0$) and it will be v_{in} if v_{oi2} has to increase towards V_R. Since input to the integrator is a sine wave and output of OC_2 changes its position whenever v_{oi2} changes from 0 to V_R (receiving a charge packet of $C_{F2}V_R$) or V_R to 0, i. e., receiving a charge packet of $-C_{F2}V_R$, the output signal v_{C1} changes its state (transition from low to high or high to low), providing a special clock that helps to split the sine wave duration into equal areas that provides charge packets of equal value to the main integrator capacitor C_F of the converter, as required by the method (c) listed above. Once the CDC uses the special clock, the counter needs to increase its count by one whenever there is a transition in the special clock. In this condition, the integrator time T_1 can be set as time taken by the converter to complete

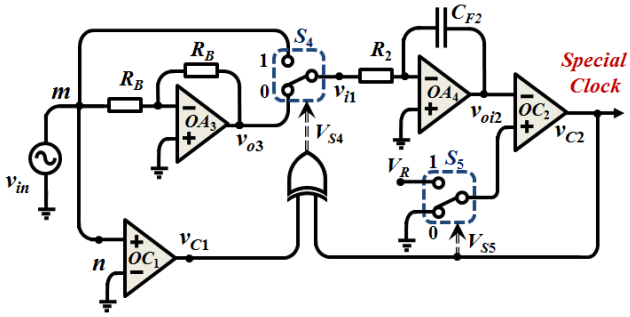

Fig. 6. Block diagram of the circuit which provides special clock that can be used by the CDC shown in Fig. 1. It consists of an inverting amplifier (opamp OA_3, resistors R_B, R_B), integrator (opamp OA_4, resistors R_2, capacitor C_{F2}), comparator OC_2, two switches S_4 and S_5 and an XOR gate. OC_1 is already a part of the CDC as indicated in Fig. 1.

N_{SP1} transitions of special clock. Similarly, the counter output during de-integration time T_2 will be the number of transitions N_{SP2} of the special clock until v_{oi} reaches zero. The charge acquired by C_F during integration period will be $\frac{V_{KX}C_F}{m}N_{SP1}$, where $\frac{V_{KX}C_F}{m}$ is the charge per packet and m is the number of packets during a half cycle of excitation cycle. Similarly, amount of discharge during de-integration per charge packet will be $\frac{V_{KS}C_F}{m}$ and total amount of discharge will be $\frac{V_{KS}C_F}{m}N_{SP2}$, irrespective of presence of partial excitation cycle. Since the magnitude of charge acquired and the amount discharged are equal, we can write

$$\frac{V_{KX}C_F}{m}N_{SP1} = \frac{V_{KS}C_F}{m}N_{SP2}$$

$$\text{Or } C_x\frac{N_{SP1}}{m}(2V_m/R\omega C_{F1}) = C_S\frac{N_{SP2}}{m}(2V_m/R\omega C_{F1})$$

$$\text{Or} \quad C_x = \frac{N_{SP2}}{N_{SP1}}C_S. \tag{11}$$

Since N_{SP1} and N_{SP2} in (11) represent number of charge packets received by C_F during integration and de-integration period, respectively, the value of C_x is now available in digital domain by taking the ratio of the present count N_{SP1} and measured count N_{SP2} and then multiplying it with known value of capacitance C_S. As explained earlier, in the new method, by using the counts N_{SP1} and N_{SP2} (corresponding to the number of charge packets) the error introduced (in the earlier method) owing to presence of partial cycle of excitation is substantially reduced.

IV. Experimental Setup And Results

In order to test the efficacy of the proposed algorithm a prototype of the proposed CDC was built and tested in the laboratory. An external clock *CLK* with a frequency 2 MHz was given to the CLU using an Agilent function generator 33220A. Various circuit parameters of the CDC chosen were

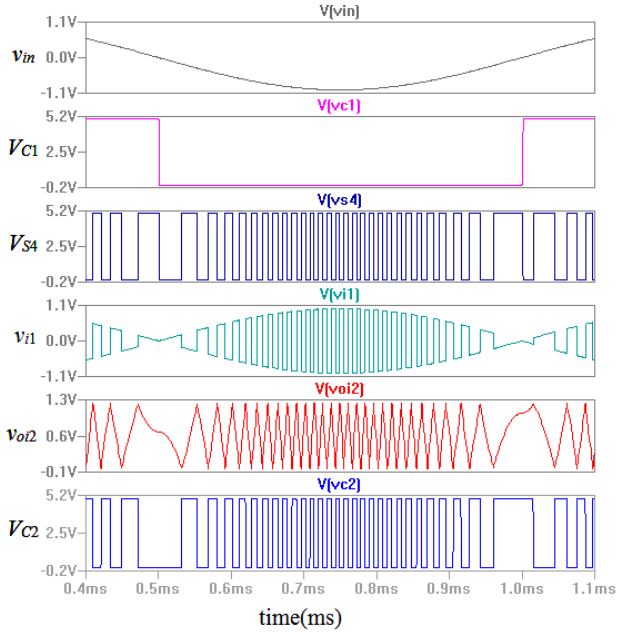

Fig. 7. Waveforms at important points in the circuit used for generating special clock that can be used by the CDC, shown for negative half excitation cycle of v_{in}. The circuit was simulated in a SPICE based environment (For illustration purpose the value of m was chosen to be 55).

C_{F1}= 470 pF, R = 39.541 kΩ, R_A = 80.923 kΩ, C_F= 33 nF, C_S = 180 pF, N_{1C} = 10000, etc. A resistor R_{F1} = 1 MΩ is kept in parallel to C_{F1} so as to provide a path for the flow of input bias current of opamp OA_1. A passive phase lead network is put in between nodes m and n to compensate the effect of R_{F1}. A standard variable capacitance box having an accuracy of ±0.01% manufactured by Neptun, Geretsried, Germany was used to emulate the sensor capacitance C_x. The sensor was excited using a sinusoidal signal v_{in} = 1sin2000πt. Switch S_2 was implemented using IC CD4053. Opamps OA, OA_1, OA_2 were realized using IC OP07. IC LM311 was used as comparators OC, OC_1. Switch S_1 was implemented using two low on resistance IC MAX4601. IC MSP430G2553 [17] served as the CLU. The functioning of the special clock circuit has been verified by conducting a simulation study using LTSPICE. In the simulation, the parameters of the switches, opamp's and comparators were given as that of IC's CD4053, OP07, LM311 respectively. A reference voltage of 1.2 V was set and the number of transitions in a half cycle was observed.

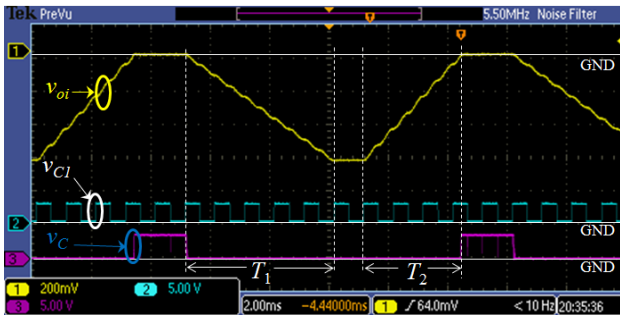

Fig. 8. Snapshot of output voltage v_{oi} along with comparator outputs v_C and v_{C1} of the CDC.

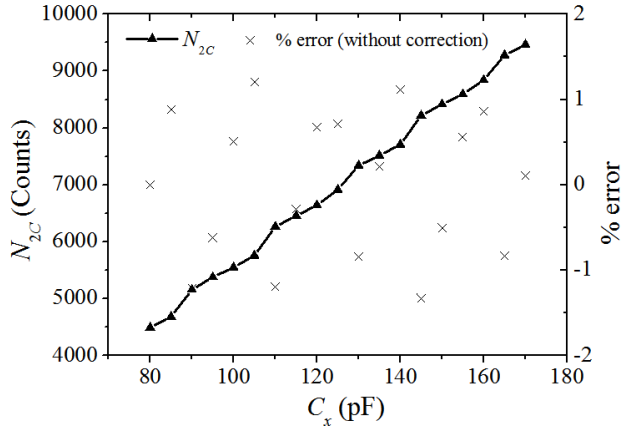

Fig. 9. Output count N_{2C} obtained from the counter unit of the CLU with sensor capacitance C_x. This large error shows the need of a modified CDC.

Fig. 7 shows waveforms at important points in the circuit used for generation of the special clock that can be used by the CDC. The value of m was chosen as 55 for illustration of the special clock. The capacitance C_x was varied from 80 pF to 170 pF in steps of 5 pF and its corresponding de-integration counts N_{2C} and N_{2C}^m were noted down. A snapshot of the output v_{oi} along with comparator outputs v_C and v_{C1} is shown in Fig. 8. At the end of every integration and de-integration periods, the switch S_3 is put in position-0 for a time period of one excitation cycle (if de-integration occurs with a partial cycle at the end, this time is more than one excitation cycle). During this time, the capacitor neither charges nor discharges as the input v_i of integrator OA is connected to ground. This can be observed in Fig. 8. It can also be seen that the converter completes the conversion within a few number of input excitation cycles, achieving a higher conversion rate compared to the CDC reported in [15]. The error characteristics for the actual N_{2C} obtained from the counter unit is shown in Fig 9. The count based on the new method (a), N_{2C}^m and its error characteristics are shown in Fig. 10. It can be seen that the error has decreased noticeably based on the new method. The total conversion time

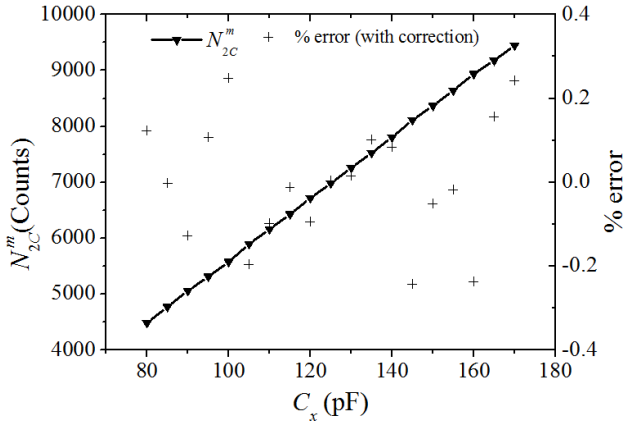

Fig. 10. Output count N_{2C}^m based on the new method (a) along with its error characteristics from the new CDC for change in sensor capacitance C_x.

worked out to be less than 10 ms for a full scale value of sensor capacitance C_1. The new CDC (≈ 13 bit) has similar update rate compared to AD7151 (12-bit, 10 ms) but it is faster than AD7747 (24-bit, 124 ms). AD7151 and AD7747 use square wave signal for excitation whereas the new CDC employs a sine wave.

V. Conclusion

A Capacitance-to-Digital Converter (CDC) that uses a sinusoidal excitation for the capacitive sensor and provides a digital output, based on dual-slope technique, is presented. When dual-slope technique is employed along with sinusoidal excitation, it has been noticed that large errors are introduced owing to the non-linear change in the integrator output of the converter as a function of time. This is more pronounced when small number of excitation cycles is used, during the conversion time. The CDC reported in this paper presents a novel method that reduces this error. A prototype of the proposed CDC has been developed and tested. Worst case error obtained from the new CDC is 0.24%. A CDC reported earlier, showed higher accuracy but uses 4000 times more excitation cycles, in the integration period, than the new CDC.

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