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Multi-Level Analysis of On-Chip Optical Wireless Links

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Featured Application: Optical wireless communication on-chip may represent a breakthrough in the development of chip multi-core-processors, paving the way towards kilo-cores architectures. Beneficial fallout can be then envisaged in many technical fields, like augmented/virtual-reality, artificial-intelligence, automotive communications and data-centers for cloud-computing.

Abstract: Networks-on-chip are being regarded as a promising solution to meet the on-going requirement for higher and higher computation capacity. In view of future kilo-cores architectures, electrical wired connections are likely to become inefficient and alternative technologies are being widely investigated. Wireless communications on chip may be therefore leveraged to overcome the bottleneck of physical interconnections. This work deals with wireless networks-on-chip at optical frequencies, which can simplify the network layout and reduce the communication latency, easing the antenna on-chip integration process at the same time. On the other end, optical wireless communication on-chip can be limited by the heavy propagation losses and the possible cross-link interference. Assessment of the optical wireless network in terms of bit error probability and maximum communication range is here investigated through a multi-level approach. Manifold aspects, concurring to the final system performance, are simultaneously taken into account, like the antenna radiation properties, the data-rate of the core-to core communication, the geometrical and electromagnetic layout of the chip and the noise and interference level. Simulations results suggest that communication up to some hundreds of μm can be pursued provided that the antenna design and/or the target data-rate are carefully tailored to the actual layout of the chip.

Keywords: networks-on-chip; optical connections; wireless communications; ray tracing; plasmonic antennas

1. Introduction

Nowadays, the advent of applications in technical fields like augmented/virtual-reality, artificial-intelligence, automotive communications, data-centers for cloud-computing triggers a widespread demand for high computational power. Therefore, trends in computation processes are fostering the development of Chip-Multicore-Processors/High-Performance-Computing architectures, where many cores are integrated together to meet the request for the continuous performance growth [1].

In this framework, chips with up to one thousand cores have been envisaged as expected outcome of this new many-core era [2]. Nevertheless, providing the cores with mutual interconnections poses several challenges related to layout design, communication latency/bandwidth, and power consumption, with increasing complexity as the number of cores grows up [3,4].

In spite of its simplicity, traditional bus architectures cannot easily scale up to a large number of processing elements due to limitations in bandwidth and latency [1], and are likely to be discarded in favor of Networks-on-Chip (NoC), where wires and routers are embedded on the same chip with cores and cache banks [3,5]. Although NoC scalability is better compared to bus solutions, it is nevertheless still limited, as propagation delays and losses of electrical wires do not scale down at the same rate as transistors [6]. Optical interconnect can improve propagation issues, but on the other end Optical-Network-on-Chip (ONoC) may suffer from additional losses due to imperfect coupling with off-chip laser and/or electro-optical conversion, as well as from extra power-expenditure for the resonance frequency tuning of optical devices like micro-rings [6]. Furthermore, cross-talk risks threaten (O)NoC design, to an extent that becomes harsher as the number of processing elements increases and the network deployment becomes more tangled. 3D integration, where the vertical dimension is also exploited to stack different circuit components, can be a viable solution in some specific situations [7], but fabrication issues limit the implementation of on-chip multi-planar layouts on the mainstream technologies as Silicon Photonics.

In order to overcome the bottleneck of physical interconnections, Wireless Network on Chip (WiNoC) are being considered an interesting solution [3–5,8]. Since millimeter-wave antennas undergo obvious problems of on-chip integration, Optical Wireless Networks-on-Chip (OWiNoC) have been recently investigated [9,10], aiming at keeping the main benefits of WiNoC (short latency, simpler network design) but easing the antenna integration process. As wireless communications on-chip are expected to complement wired solutions, rather than to replace them [2,11], OWiNoC also benefit from full compatibility with optical, physical networks which may be also deployed on the same chip.

The design of OWiNoC encompasses several challenging tasks, spanning from optical antenna design and wireless channel modeling to management and mitigation of interference issues, which always rise up as the wireless propagation channel is inherently shared among simultaneous wireless communications. This paper aims at providing a comprehensive insight into these different aspects, with special attention to the impact of noise and interference on bit-error-probability and maximum achievable distances by means of simulations carried out in some reference, study cases. The main topic under investigation is the on-chip wireless optical communication in point-to-point links, and therefore any network optimization feature is simply not taken into account so far.

The paper is organized as follows: after a survey on previous studies and activities on networks-on-chip provided in Section 2, the main features of on-chip wireless links at optical frequency are outlined in Section 3. Interference issues and performance assessment in OWiNoC are addressed in Section 4, whereas the results of the simulations are discussed in Section 5. Some conclusions are finally drawn in Section 6.

2. Background on Networks-On-Chip

Scaling up multi-core chips through standard technologies for physical interconnects poses several performance issues like heat dissipation, latency and speed bottleneck, due to the physical limits of metallic tracks. Therefore, wireless solutions represent today a valid NoC breakthrough to overcome these problems [2,8], especially for long-haul ranges within the chip. According to the existing literature, WiNoC have been mainly investigated at frequency up to hundreds of GHz [12–16].

Although the alleged power savings (either in pJ/bit or mW/Gbps) of optical technologies for on-chip interconnections is nowadays still under debate [3,17], the advantages of large spectrum and wavelength-division multiplexing (WDM) seem anyway beneficial for thousand-cores chip.

Therefore, the extension of the wireless solution to the optical domain represents an interesting topic of investigation, also in light of the minor attention so far devoted to OWiNoC [10,18,19]. A survey

on the major studies and papers already published on wired and wireless NoC is summarized in Table 1 for the sake of brevity.

Table 1. Survey on Networks-on-Chip -related studies.

Interconnect Solution	NoC Technology	Related References
Physical Interconnection	Networks-on-Chip (NoC)	[1,5,20,21]
	Optical Networks-on-Chip (ONoC)	[5,6,11,20,22]
Wireless Networks	Millimeter wave and THz (WiNoC)	[4,5,8,17,23,24]
	Optical (OWiNoC)	[9,10,18,19,24]

A comprehensive performance assessment of a network-on-chip usually spans several different aspects such as the number of NoC elements (links, routing, switch elements) [2,23], the latency [2,12,17,24], the chip area [5,25], the communication distances [2], the data-rate [2], and the bit error probability (BEP) [2,22]. The analysis carried out in this paper is primarily focused on both the communication range and the BEP.

3. Physical Description of the On-Chip, Optical Wireless Link

Regardless of the many technological stages involved in its overall manufacturing process, an integrated circuit is often roughly represented as a layered structure as shown in Figure 1. The first stage of the process flow (front-end-of-line—FEOL) aims at the deployment of the electrical/electronic circuit components into the semiconductor (e.g., silicon) layer. Some metallization and dielectric layers are then interleaved in the next steps (back-end-of-line, BEOL), and holes are finally etched through the insulating material to connect the metallic layers, which provide the required interconnects among the circuit elements underneath [26].

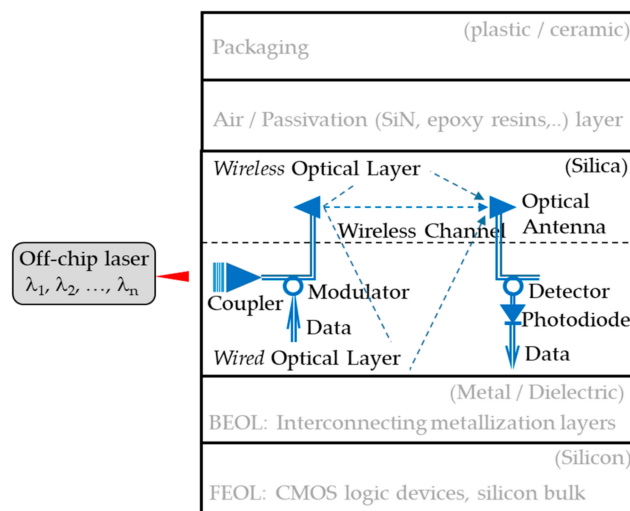


Figure 1. Layered representation of the chip structure.

Various viable solutions have been proposed in the literature for the inclusion of the optical layer in the chip stack. For example, the optical layer can be placed on-top of the electronic interconnection layers [27,28] as shown in Figure 1, or in plane with it [29–31]. The layer stack is finally completed by additional upper layers accounting for possible passivation/filling materials and for the outer package enclosure. It is worth mentioning that a further layer might be present, either on the top or at the bottom, corresponding to a possible heat sink.

The on-chip optical wireless communication indeed occurs in the optical layer, as sketched in Figure 1, which can be regarded as a wireless evolution of the on-chip optical wired link outlined

in [6]. According to the OWiNoC paradigm, the optical layer is further split into a wireless and a wired part, the former consisting of the optical antennas spreading the core-to-core signals into the wireless channel, the latter including the optical elements interfacing the cores to the optical antennas.

This sketch of possible implementations of OWiNoC aims at introducing the main, representative features of the optical layer layout further addressed in the following subsections.

3.1. Physical Optical Interconnects

The source of the optical power at the transmitting link end can be an external off-chip laser coupled to the optical bus [11,32], emitting a nominal power P_{TX} on the bus, steady in time according to the expected working temperature of commercial GPU/CPU architectures. Then, a dedicated micro ring resonator (MRR) can be used to provide both electrical-to-optical conversion [33] and On-Off Keying (OOK) Non-Return-to-Zero (NRZ) amplitude modulation [17] with a bandwidth B_{opt} over the optical carrier. The modulated signal is finally routed towards the optical antenna (see Section 3.2) and wirelessly spread within the chip. As shown in the block scheme in Figure 2, an integrated optical amplifier may be present before the transmitting antenna, in order to cope with the large path loss coming from the optical wireless channel and to push the received signal strength to the level required to drive the digital logic in the lower, electrical layer [6]. Beyond the wireless channel, the optical incoming field is first gathered by the optical receiving antenna, then directed into the optical bus and finally filtered off by another MRR. A photodiode (PD) with responsivity η_{PD} reconstitutes the OOK signal in the electrical domain, ready to be demodulated.

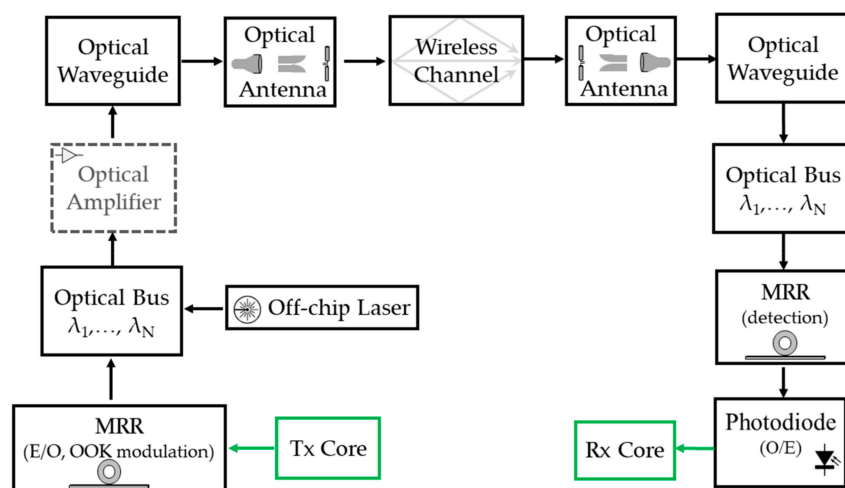


Figure 2. Block scheme of the on-chip, optical wireless link.

As long as the analysis is limited to a single link, symbols detection errors are due to the propagation impairments (briefly discussed in Section 3.3) and to the noise effects experienced by the optical communication system. Since the thermal noise is often acknowledged as the dominant noise contribution [34], other noise sources like the PD shot noise and the relative intensity noise of the laser have been neglected herein. Conversely, in a multi-link scenario mutual interference among the different, simultaneous communications may arise, to an extent greatly dependent on antennas radiation properties, spacing and position. These issues will be discussed more in detail in the following Sections 4 and 5. Although an effective implementation of O(Wi)NoC could benefit from WDM [11,35,36], this work involves no multiplexing scheme (e.g., simulations are run with only one WDM channel), in order to focus the investigations on the influence of antennas and core distances, excluding any issues above the physical layer.

3.2. Optical Antennas

In order to evaluate the propagation and the performances of the wireless links in OWiNoC, some study cases based on different antenna configurations are here considered. Actually, the antenna coupled to the optical waveguide is one of the key elements in the OWiNoC design as it allows to switch from wireless to wired optical propagation and vice versa. At the transmitting section, the antenna radiates in the surrounding medium the optical signal that comes from the input waveguide. The radiated signal propagates wirelessly and it is then transferred to an output waveguide by the receiving antenna. The analysis of propagation and performance of point-to-point optical wireless links carried out in the following sections relies on the two configurations of plasmonic antennas shown in Figure 3a,b, respectively.

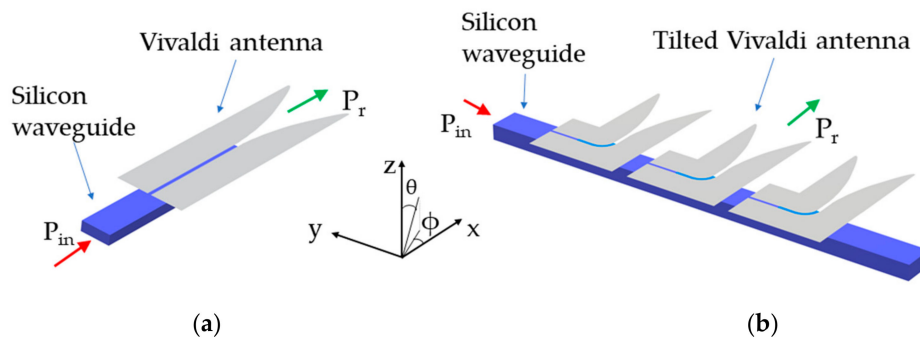


Figure 3. Scheme of the single Vivaldi antenna (a) and of the tilted Vivaldi antenna array (b) coupled to a silicon waveguide.

In particular, Figure 3a outlines the single antenna configuration [9], consisting of a silver plasmonic Vivaldi $1.75 \mu\text{m}$ long and $0.57 \mu\text{m}$ wide. The antenna is coupled to a silicon waveguide ($0.38 \mu\text{m} \times 0.22 \mu\text{m}$) through a slotted plasmonic waveguide with length $1.63 \mu\text{m}$. The optical signal (P_{in}) is launched into the Si waveguide and it is vertically coupled to a plasmonic slot waveguide, which is separated from the dielectric one by a dielectric layer. The antenna, obtained by shaping the plasmonic slot waveguide according to a Vivaldi profile, radiates the optical signal in the surrounding medium (P_{r}) in the positive x direction. The behavior is reciprocal when the antenna is used as receiver. The antenna array configuration is instead represented in Figure 3b [37], where multiple Vivaldi antennas are fed by the same Si waveguide. Each antenna is 90° tilted with respect to the Si waveguide. This geometrical rotation allows a 90° -tilt of the radiation pattern with respect to the waveguide propagation direction. Moreover, this layout implements a travelling wave excitation of the array, which guarantees compact sizes of the overall radiator (about $3.5 \mu\text{m} \times 8.7 \mu\text{m}$ for a 5-antennas array).

Although the details on the design and on the radiation characteristics of the two antenna configurations are provided in [9,37] the antennas gain function in the $\phi = 0^\circ$ (xz) and in the $\theta = 90^\circ$ (xy) planes is plotted in Figure 4a and in Figure 4b for the sake of self-consistency. In particular, the reported curves refer to the single Vivaldi antenna (black continuous), and to the antenna array with $N = 3$ (blue dotted) and with $N = 5$ (green dashed) elements. The results shown in Figure 4 were obtained by the FDTD simulations of the antennas radiating in an infinite homogeneous medium with refraction index $n = 1.44$ (i.e., corresponding to silica, see Table 2), which was implemented in the numerical model by perfectly matched layer boundary conditions. The radiation diagrams were calculated by near-to-far field projections of the fields recorded on a closed box, surrounding the different antenna configurations.

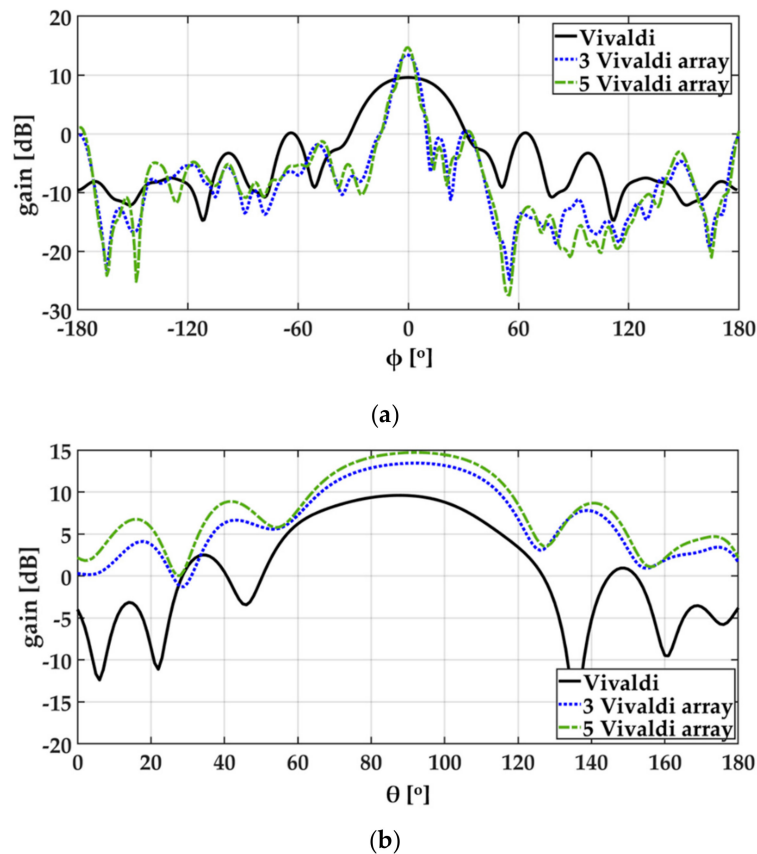


Figure 4. Gain functions in the $\theta = 90^\circ$ (xy) plane (a) and in the $\phi = 0^\circ$ (xz) plane (b) for the single Vivaldi antenna (black curve), the antenna array with $N = 3$ (blue dotted curve) $N = 5$ (green dashed curve) elements.

The three antenna layouts correspond to different antenna gain values ($G = 9.90$ dB, $G = 13.45$ dB and $G = 14.70$ dB for the single, three- and five elements configuration, respectively), which take also into account the actual efficiency in the electromagnetic coupling between the silicon waveguide and the transmitting/receiving antenna. These antennas are exploited in the following to assess the impact of different radiation properties on the electromagnetic propagation in the multilayer environment and on the point-to-point link performance.

It is worth pointing out that the multi-level numerical approach proposed in this paper is virtually applicable to every optical antenna configuration, such as multiple-feed arrays of plasmonic antennas [38] or dielectric antennas [19,39] and to every multilayered environment.

3.3. Optical Wireless Channel

According to the chip layered representation, the electromagnetic waves springing out from the on-chip transmitting antenna are expected to bounce onto the interfaces between the layers, thus triggering multipath effects [8,10,14,16,18]. Assuming the antennas buried in a SiO_2 layer limited by two different, unbounded media on the lower and on the upper side [10,18], multipath is fundamentally generated by the multiple reflections between the interfaces (Figure 5) and can be evaluated by means of the Ray Tracing (RT) approach discussed in [10]. It is worth pointing out that the RT modeling is particularly tailored to the investigation of the optical wireless channel, as geometrical optics is known to be an asymptotic theory, i.e., its accuracy increases at higher frequency.

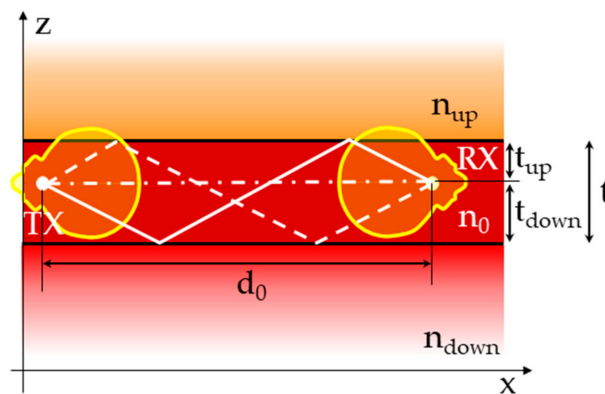


Figure 5. Ray tracing evaluation of on-chip wireless propagation.

Compared to other wireless networks, where the possible mobility of nodes and/or objects over quite large areas produces random-like fluctuations of the received signal intensity, the on-chip wireless channel is confined and static, as the chip layout is fixed and known beforehand [24]. Therefore, propagation modeling at chip-level is quite well fit for characterization through deterministic approaches like RT, which require the a priori knowledge of the physical environment.

In order to run the RT simulation, both geometrical and electromagnetic properties of the link have to be set, the former referring to the SiO₂ layer thickness (*t* in Figure 5), to the antennas distance from the interfaces (*t_{up}* and *t_{down}*) and to the link distance (*d₀*), the latter consisting of the materials refraction index (*n_{down}*, *n₀* and *n_{up}*). A 3D representation of the antenna radiation patterns is also necessary as input file. The assessment carried out in this work is limited to the Vivaldi antenna configurations briefly discussed in the previous section [9,37], but any other radiation diagrams can be embedded into the RT tool, provided that they are encoded in the required format.

Although propagation in Figure 5 is limited to the *xz* plane, a 3D description of the antenna patterns is nevertheless helpful, as the RT model can be then easily run regardless of the antenna orientation with respect to the propagation plane, e.g., for the assessment of the power received from an interfering transmitter. The geometrical/electromagnetic parameters considered herein for the RT simulations are summarized in Table 2.

Table 2. Main input parameters for the Ray Tracing simulations.

Geometrical		Electromagnetic	
<i>t_{down}</i>	2 μm or 3 μm	frequency	193.5 THz ($\lambda_0 = 1.55 \mu\text{m}$)
<i>t_{up}</i>	2 μm or 3 μm	<i>n_{down}</i>	3.47 (Silicon, metal otherwise)
<i>t</i>	<i>t_{down}</i> + <i>t_{up}</i>	<i>n₀</i>	1.44 (Silica)
<i>d</i>	tens to hundreds of μm	<i>n_{up}</i>	1 (Air)
		antenna	single/array of plasmonic Vivaldi antenna [9,37]

4. Performance Assessment of Optical Wireless Networks-on-Chip

The performance of a communication link is often characterized in terms of bit error probability (BEP). In a binary, optical communication system, BEP can be defined as the probability that the received photocurrent transmitting 0 is detected above the decision threshold, or it is detected below the threshold while transmitting 1. In the literature related to Wireless NoC [4,19,22] BEP is usually experimentally assessed or estimated by means of analytical formulas for single link, which can be computed based on the estimated value of the received power after the photodiode. However, wireless network design always requires a careful study of cross-link interferences, which may occur among simultaneously links exploiting the same (optical) channel. In fact, the spatial reuse of optical wavelengths improves significantly the transport capacity in OWiNoC, since the number of simultaneous communications will not be limited by the number of available wavelengths. On the

other hand, wavelength reuse can trigger co-channel interference, which can harshly degrade the system performance, if not effectively handled and mitigated. Hence, the design of OWiNoC can greatly benefit from an interference-aware framework for BEP evaluation. By exploiting the analytical approach in [40,41] compliance of different link configurations with the target performance for the on-chip communication can be investigated.

In a general OWiNoC scenario, $I + 1$ transmitters using the same optical wavelength can be present, with only one useful transmitter TX_0 for the desired receiver RX_0 and the other I transmitters (TX_1, TX_2, \dots, TX_I) causing interference to RX_0 while communicating with their corresponding receivers. The optical power (i.e., the power of the unmodulated optical carrier) of the received desired signal is here denoted by P_0 , and the normalized optical power of the i -th received interfering signal is denoted by $x_i = P_i/P_0$, with $i = 1, 2, \dots, I$. The received power values depend on the radiation properties of the antennas, their spacing and orientation and on the propagation characteristics of links.

In this paper, BEP performance is investigated for the following, two simple OWiNoC scenarios. In the former case (Figure 6a), two parallel links, separated by the distance Δ , carry data in the same direction up to a distance d_0 . The optical signal from TX_0 to RX_0 is exposed to the interference of the signal coming from TX_1 , which may therefore affect the communication BEP. In the latter scenario (Figure 6b), an additional, parallel, interfering link is introduced at a distance Δ' from the reference link TX_0 – RX_0 .

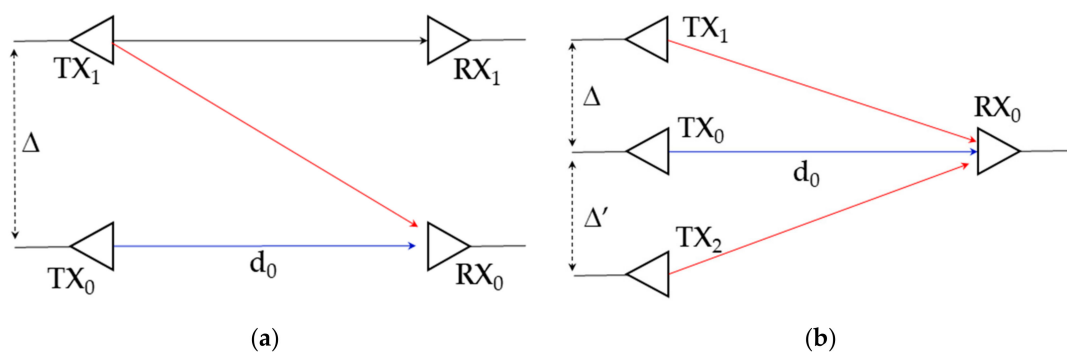


Figure 6. Optical Wireless Networks-on-Chip scenario with a single (a) and with two (b), parallel interfering link(s).

For each OWiNoC scenario, the received powers can be evaluated with FDTD or RT tools as discussed in the following Section 5.1. For a given transmitted optical input power P_{in} , the received power can be computed as $P_i = PG_i \cdot P_{in}$, where PG_i is the path gain of the channel between the i -th transmitter and the reference receiver RX_0 .

The performance analysis carried out in Section 5.2 assumes that all links use intensity modulation OOK with NRZ pulses and direct detection. If the bits of the data sources have the same probability of 1/2, the average power $P_{in,av}$ of the modulated signal is one half of the power of the unmodulated carrier. The BEP is evaluated as a function of signal-to-noise ratio (SNR) and normalized interference powers ($x_i, i = 1, \dots, I$), where $SNR = 4\gamma^2$, with $\gamma = \eta_{PD} \cdot P_0 / (2\sigma_{th})$ depends on the unmodulated received power, the responsivity η_{PD} of the photodetector and the standard deviation σ_{th} of the additive Gaussian noise at the receiver. Since the thermal noise is the dominant noise most often associated with p-i-n receivers (at least for low level of detected power) [34], noise variance σ_{th}^2 does not depend on transmitted bits and can be computed as $\sigma_{th}^2 = 4 \cdot K \cdot T_{eq} / (2 \cdot R_L \cdot T)$, where K is the Boltzman’s constant, T_{eq} is the noise temperature of the receiver, R_L is the resistance of the receiver and $T = 1/R_b$ is the bit interval of the transmitted data. Here, as a reference, the values of system parameters in Table 3 are considered for the numerical evaluations [34,42].

Table 3. Reference system parameters.

System Parameter	Value
$P_{in,av}$	0 dBm
η_{PD}	0.7 A/W
R_b	10 Gbit/s
T_{eq}	600 K
R_L	1 k Ω
K	1.38×10^{-23} J/k

In particular, the method in [40,41] is used to analytically evaluate the BEP by taking into account all the random variables (RVs) in the optical wireless communication system. The RVs include the bits sent by all transmitters, the optical carriers phases and time offsets of the asynchronous interfering links, and the Gaussian noise.

It is worth mentioning that inter-symbol interference is here neglected, i.e., the delay spread related to multipath propagation is assumed (much) smaller than the bit time interval. Based on a reverberation model, delay spread was estimated equal to some nsec. at mmWave (300 GHz) and roughly one order of magnitude lower at 100 THz [24]. As the on-chip environment is not fully reverberating, first experimental assessments in the mmWave band returned lower values, e.g., equal to 100 psec. in [12], which might therefore correspond to about 10 psec. in the infrared/optical bands. In order to avoid inter-symbol interference, $T \gg 10$ psec. is required, i.e., $R_b \leq 10$ Gbit/s is approximately needed. According to these considerations, $R_b = 10$ Gbit/sec. has been therefore set in Table 3 as a main target. This value is of the same order of magnitude as the channel throughput considered in previous studies [4,6,8,17,35,43].

5. Results and Discussion

This section includes the results of the simulations carried out in some study cases, aiming at the assessment of OWiNoC link performance in terms of SNR and BEP. The outcomes of the corresponding link-level RT simulations are discussed, highlighting some general trends and constraints for the feasibility of wireless networks-on-chip at optical frequency.

5.1. Ray Tracing Analysis of the Optical Wireless Channel

RT reliability for on-chip propagation prediction is shown in Figure 7 against FDTD simulations of an optical wireless link between the plasmonic Vivaldi antenna shown in Figure 3a and presented in [9] and for different thickness of the silica layer. Path Gain (PG) plotted in Figure 7 is the ratio between the power seized by the receiving antenna and the power supplied to the transmitting one. In spite of the very different computation effort required by RT and FDTD, with computation time respectively equal to few seconds and several hours, the overall root mean square error is equal to 4.5 dB. Considering that RT accuracy for PG modeling in cellular systems for personal communications may commonly correspond to an average RMSE of several dBs, results are here quite in agreement. According to this outcome, surface wave propagation, which has been sometimes claimed as a major propagation mechanism [13,16] does not seem so significant, at least in the considered situations. In fact, it would be accounted for by the FDTD simulation only and therefore would result in a much poorer comparison between the models. The sensitivity of the PG values to the SiO₂ layer thickness in Figure 7 provides further evidence of the strong multipath effect affecting the on-chip propagation, as variations comparable to the wavelength completely change the interference pattern of the rays, thus resulting in a shift of the maxima/minima of the power level.

It is worth pointing out that in both cases PG is on the average greater compared to what it would be in free space (dotted line in Figure 7), thus meaning that on-chip wireless communications can benefit from better propagation conditions than free space. As outlined in [10], this is the result of a sort of guiding effect triggered by the multiple reflections within the antenna layer up to a distance

that depends on the antenna radiation properties, the material at the interfaces and the thickness of the layers [10].

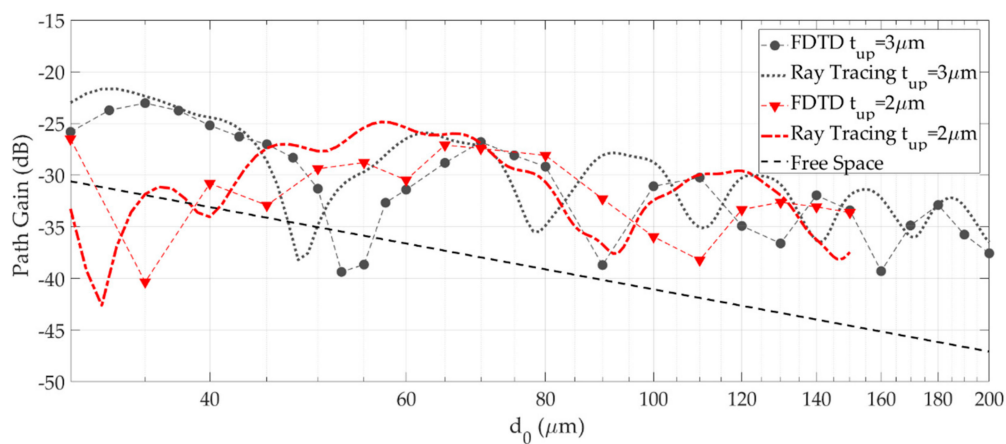


Figure 7. Ray Tracing-FDTD comparison, Si-SiO₂-Air layered structure, $t_{\text{down}} = 3 \mu\text{m}$, plasmonic, single Vivaldi antenna facing each other at both link ends.

Taking advantage of the computational agility of RT, the impact of materials, antennas and layers thickness on the optical wireless channel is further investigated in Figure 8. In addition to purely dielectric interfaces, which are representative on the on-chip layered environment, highly reflective interfaces has been also taken into account for the sake of comparison. In the RT tool, they have been implemented as metals based on the Drude theory [44]. As shown in Figure 8, interference is clearly stressed if total reflection occurs at the interface(s)—e.g., with metal filling the lower layer instead of silicon—as the ray's intensities keep similar compared to the case where a greater power leakage occurs at the interface.

Increasing the antenna gain—e.g., considering an array of three/five plasmonic Vivaldi antennas instead of a single one—results in a greater PG on the average, although it can also impair the aforementioned guiding effect, to the extent that pursuing a directivity as large as possible may not represent a convenient target [10].

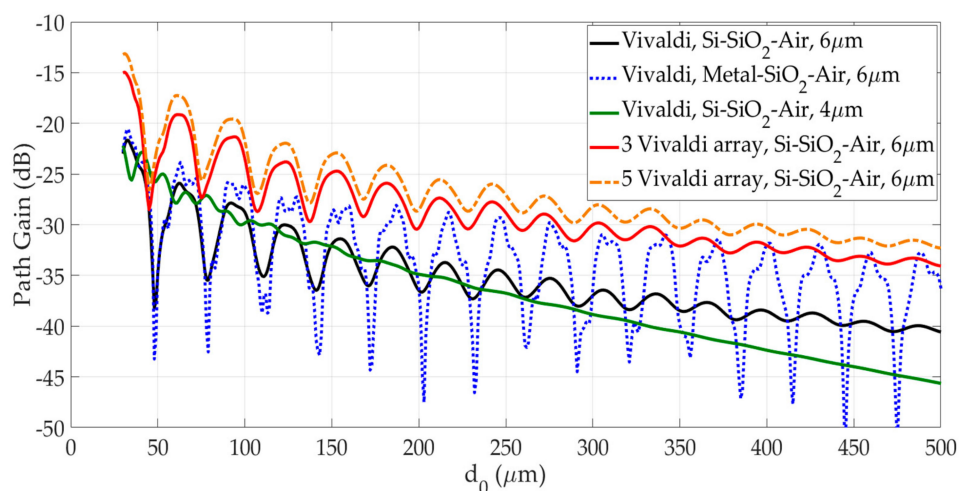


Figure 8. On-chip wireless channel sensitivity to material-, antenna-, and layer-thickness.

Finally, a reduction in the antenna layer thickness seems to alleviate multipath effects in Figure 8, although at the expense of the power decay trend at larger distance [10]. Therefore, the choice of the best thickness should also take into account the communication distance target. More in general, many aspects concur to the system performance in a somehow interlaced way, i.e., it is hardly possible

to optimize a single parameter regardless of the others. This is the main motivation for the link-level assessment of the optical wireless communication on-chip discussed in this work.

5.2. Link Level Assessment of Bit Error Probability

BEP results are first presented for the scenario with one interfering link (Figure 6a), by considering the reference system parameters of Table 3, Vivaldi optical antennas and path gain values obtained from RT simulations. Since the BEP depends on the positions of both desired and interfering transmitters, the results are displayed in the form of a two-dimensional map where the BEP is reported for each pair of values (d, Δ) .

The results in Figure 9a are derived for links using single plasmonic Vivaldi antennas placed in the middle of a SiO_2 layer with $6 \mu\text{m}$ thickness. According to the system parameters values in Table 3, a received power at least equal to -25.7 dBm is necessary to overcome the noise level to the extent corresponding to a target $\text{BEP} = 10^{-6}$. Link performance is significantly impaired by the multipath effects, which make the link reliability not uniform in the parameter space (d, Δ) and fully unsatisfactory for $d > 70 \mu\text{m}$ due to the noise level, and for $\Delta/d < 1/3$ due to the interference. The link is unreliable in a wide range of d values between 40 and 60 μm due to a multipath induced path gain notch (Figure 8). The domains of the (d, Δ) space with BEP lower than the target represent the coverage areas for the link (light to dark blue in Figure 9a).

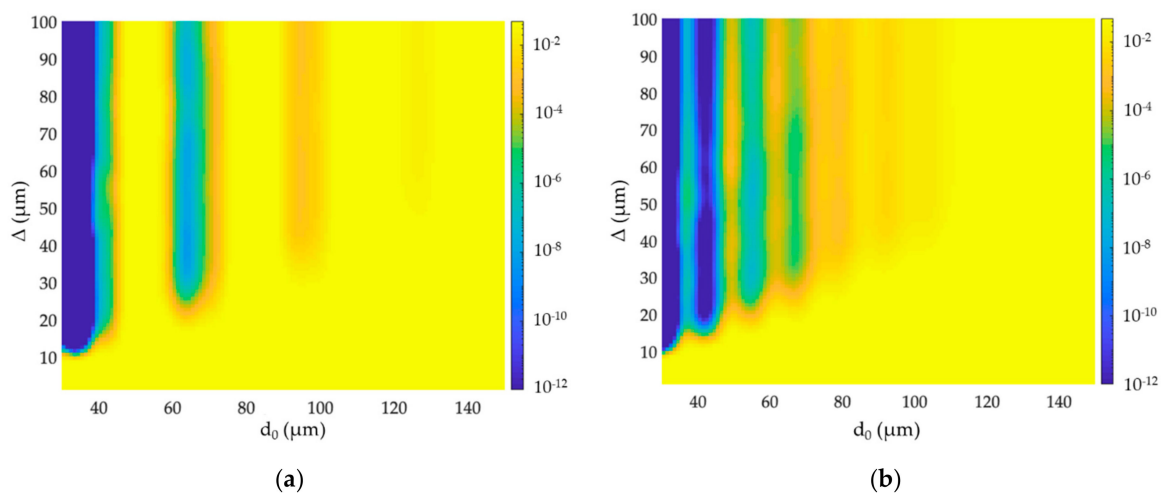


Figure 9. Bit error probability (BEP) map in the space (d, Δ) for the scenario in Figure 6a with Vivaldi antennas and $t = 6 \mu\text{m}$ (a) and $t = 4 \mu\text{m}$ (b).

As the multipath conditions change by varying the SiO_2 layer thickness (Figures 7 and 8) also the coverage zones are likely to change accordingly. This is illustrated in Figure 9b where the thickness of the SiO_2 layer is decreased to $4 \mu\text{m}$. Comparison of the two figures shows that the width of path gain holes is reduced, but the maximum coverage shrinks to $d < 55 \mu\text{m}$ at the same time due to a worse range dependence of PG.

In summary, on-chip wireless optical communications between plasmonic Vivaldi antenna buried in a few μm silica layer are mainly noise limited, with a maximum coverage distance lower than $100 \mu\text{m}$. Interference represents a significant issue only in case the interfering links are quite close, with spacing not exceeding few tens of μm .

To extend the coverage region of a noise limited link, antennas should be designed to have a larger gain. As shown Figure 8, this may be accomplished with (Vivaldi) antenna arrays. The path gain increases by nearly 6 dB with 3 elements array and by nearly 8 dB with 5 elements array. An array of 5 plasmonic Vivaldi antenna in a SiO_2 layer with thickness of $6 \mu\text{m}$ is considered in Figure 10a. As expected, the coverage zones are larger than those in Figure 9a, with a maximum communication distance equal to nearly $240 \mu\text{m}$. Since the antenna array has a narrower beamwidth than the single

element, the link is also more protected against interference, with interfering effects basically vanishing for $\Delta/d > 1/12$. Moreover, the coverage is more uniform in the (d, Δ) domain, because the increase in the antenna gain reduces the occurrence of situation where the received signal intensity drops below the detection threshold.

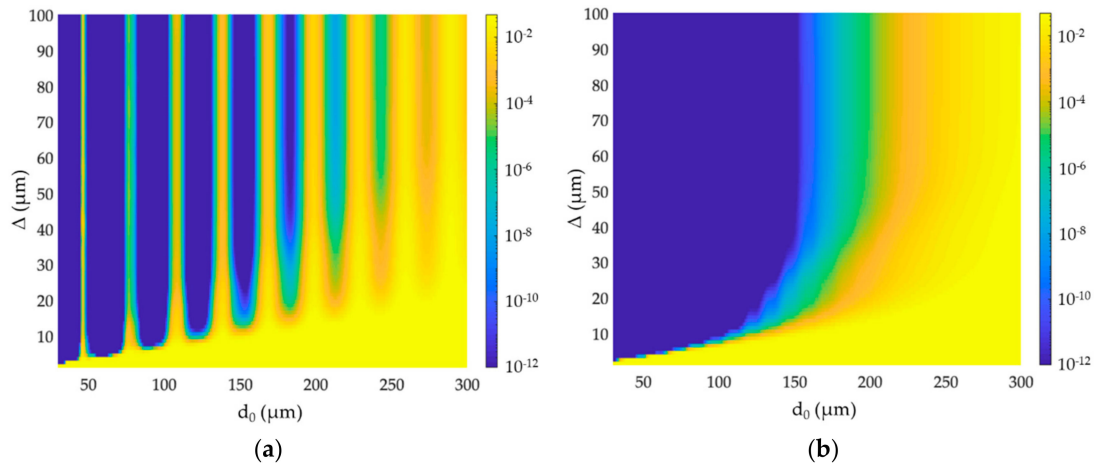


Figure 10. BEP map in the space (d, Δ) for the scenario in Figure 6a with 5-elements Vivaldi antenna and $t = 6 \mu\text{m}$ (a) and $t = 4 \mu\text{m}$ (b).

Figure 10b shows the BEP map obtained with a 5-element Vivaldi antenna array and SiO_2 thickness of $4 \mu\text{m}$. Similarly to the results shown in Figure 9b, the thinner dielectric layer mitigates the multipath effects by smoothing the path gain notches, and therefore the coverage area turns out to be more uniform on the whole. Nevertheless, it also becomes smaller compared to Figure 10a, with a maximum communication range equal to nearly $180 \mu\text{m}$. This value is smaller than the corresponding value in Figure 10a, as expected, because the path gain decays more rapidly at large distances if the layer thickness is reduced (see Figure 8).

In order to stretch the extension of the coverage zone pursuing its smoothness at the same time, a possible option is the reduction of data rate requirements for the communication link. In fact, with a smaller data-rate the noise bandwidth in the receiver scales down as well, whereas the resistance R_L can be scaled up because of the reduced receiver bandwidth requirements. In this way, the noise power level decreases and the receiver sensitivity increases. The BEP map in Figure 11 refers to the same situation considered in Figure 10a with data-rate $R_b = 1 \text{ Gbit/s}$ and $R_L = 10 \text{ k}\Omega$. The coverage zone uniformly extends to a maximum distance of nearly $600 \mu\text{m}$, provided that the links spacing is large enough to keep interference under control.

This result also highlights the existence of a further trade-off between wireless communication distance and data-rate, which might be taken into account in the design of the wireless network. Preserving reliable communications with data-rate of the order of 10 Gbit/s even at longer distances might be possible, provided that a greater design efficiency is pursued, e.g., improving the coupling with the off-chip laser, or increasing the gain of the antennas and/or the responsivity of the photodiode.

The scenario with two interfering links is finally addressed in Figure 12, where $\Delta = \Delta'$ is considered for the sake of simplicity. As for Figure 10a, 5-element Vivaldi antenna arrays and thickness of the SiO_2 layer equal to $6 \mu\text{m}$ are assumed. Although noise is still the heaviest limiting factor, interference is doubled and its effect is therefore slightly increased, hampering the optical communication when $\Delta/d < 1/8$ approximately. Hence, in the presence of more interfering links, the inter-link distance Δ has to be increased to keep the same protection level against interference. It should be noted that the value of Δ/d (or the values of $\Delta_1/d, \dots, \Delta_i/d$, in a more general setting) that limits the coverage zones depends on the antenna radiation diagram, the number of the interferers and their power, which has to be evaluated for each specific application scenario.

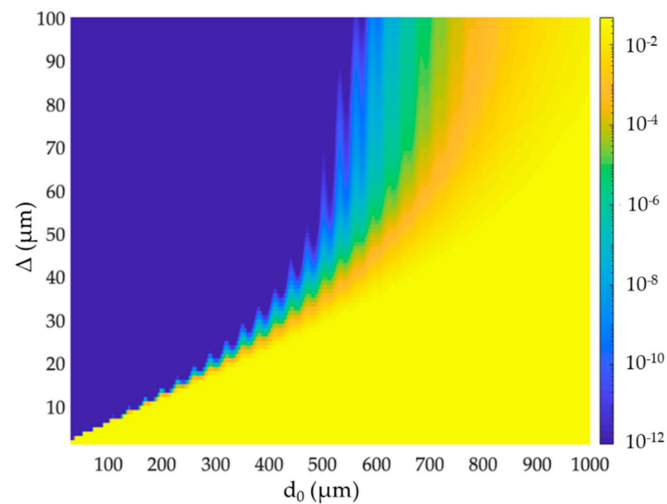


Figure 11. BEP map in the space (d, Δ) for the scenario in Figure 6a with $R_b = 1$ Gbit/s and $R_L = 10$ k Ω , 5-elements Vivaldi antenna arrays and $t = 6$ μm .

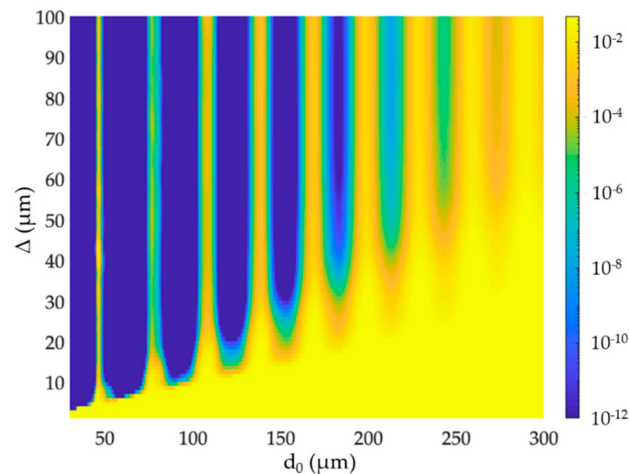


Figure 12. BEP map in the space (d, Δ) for the scenario in Figure 6b with 5-elements Vivaldi antenna arrays and $t = 6$ μm .

6. Conclusions

Optical wireless networks-on-chip are investigated in this work by means of simulations carried out in some reference cases and according to a multi-level analysis, i.e., taking into account the main factors simultaneously affecting the performance of the on-chip, point-to-point communication. In particular, bit error-probability and communication range have been assessed in relation to the antenna radiation properties, the geometry and the constituting material of the chip, the mutual position of the interfering links and other system parameters like the data-rate, the noise power and the photo-diode responsivity at the receiver side.

Results show that in all the considered cases communications seem primarily limited by noise, with interference representing an issue only if the interfering links are quite close each other. For instance, in presence of one/two interfering links equipped with plasmonic Vivaldi antennas (gain ~ 10 dB), interference effect is basically negligible (compared to noise) as the links spacing is larger than few tens of μm . The communication range compliant with a target data rate of 10 Gbit/s turns out to be lower than 100 μm when the antennas are buried in a few μm silica layer, whereas it is more than doubled if a 5 dB gain increase is achieved resorting to Vivaldi array configurations. Further extension of the coverage area up to some hundreds of μm can be accomplished reducing the data-rate, as long as this may be acceptable. Otherwise, to keep the channel throughput to values fully competitive with other

interconnect technologies, further efforts on the project of OWiNoC are required, e.g., aimed at the design of optical nano-antennas with larger gain.

Regardless of its extension, uniformity of the coverage area is jeopardized by multipath propagation, which can result in spots where communications reliability is prevented by the heavy multipath loss. Reducing the thickness of the dielectric layer including the antennas can contrast this multipath effect, but it would also worsen the received power range dependence at the same time.

In conclusion, as many factors simultaneously concur to the overall link performance in a somehow interlaced fashion, the optimization of each design parameter is likely to be possible only in the framework of a comprehensive, multi-level assessment.

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