A Sub-1V, 350 µW, 6.5 dB integrated NF Low-IF Receiver Front-End for IoT in 28nm CMOS

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***Abstract*— This paper presents a highly efficient low-IF receiver front-end for IoT applications. The low-noise trans-impedance amplifier (LNTA) combines a transformer-based network for scaling up the source impedance together with passive g_m-boosting and current-reuse techniques to achieve better noise and 12x current saving compared with a Common Gate (CG) stage. A complex channel-selection filter with center frequency and passband of 2 and 1.4 MHz respectively is implemented after the passive mixer with a g_m-boosted CG stage. Built in 28 nm CMOS, the proposed receiver occupies an active area of 0.1 mm^2, it is supplied with 0.9 V and consumes only 350 µW, while showing a minimum NF of 6.2 dB at the channel of interest. The RF performance of the proposed receiver is very competitive with state-of-the-art ultra-low-power receivers, while it consumes the lowest power.**

Keywords*— *ultra low-power (ULP), current reuse, gm-boosting, complex filter, IoT.

I. Introduction

Due to the explosion of Wireless Sensor Network (WSN) and Internet-of-things (IoT), intense research has been directed toward ultra-low power RF transceivers. To minimize power consumption, most RF transceivers trade-off power consumption versus sensitivity (i.e. receiver NF). As an example, state-of-the-art transceivers for Bluetooth-Low Energy (BLE) [1-3,5] achieve a NF>10 dB with sub-mW power [2,3], or a NF<6.5 dB consuming >1.5 mW [1,5]. At the same time, a sub-1 V supply voltage allows to reduce the complexity of the power management unit. In the literature there are two common approaches to minimize power consumption in RF transceivers. First, use a drastically reduced supply voltage [1,2], second, recycle the bias current several times [3,4, 6-8]. Relying on a reduced supply voltage results in a considerable increase of the chip area. This is because bulky inductors are frequently used to perform the biasing of the active devices. For instance, the designs in [1] and [2] have a chip area of 2.5 mm^2 and 1.65 mm^2 while they are supplied from 0.3 V and 0.18 V and consume 1.6 mW and 382 µW respectively. On the other hand, several blocks can be stacked on top of each other while using a larger supply voltage to improve power efficiency. In [3] extensive current reuse is applied: the low-noise amplifier (LNA), the mixer, the voltage-controlled oscillator (VCO) and the baseband input stage are stacked under a 0.8 V supply. The receiver draws only 530 µA. However, stacking several blocks degrades the overall performance (e.g. NF larger than 15 dB is reported) and could result in unwanted cross-talk between blocks due to poor isolation. Similarly, in [4], current reuse is used in the front-end signal path (i.e. the combination of RF and baseband stage) while a lower supply is used for the LO generation. The circuit achieves good linearity and noise, making it suitable for most low power applications but, even excluding the VCO, its power consumption exceeds our sub-mW target. Following a similar approach, in [8] a partially stacked LNA-baseband receiver is reported for SoC coexistence that achieves a remarkable OOB-IIP3 of 6 dBm. Even though sharing bias current between LNA and the first stage of both I and Q baseband trans-impedance amplifiers (TIAs) improves the frontend linearity, such a receiver still draws 1.4 mA from 1.8 V. Unfortunately, such a high supply may not be available in ULP systems [1-7] and the power dissipation is relatively high for IoT applications [2,3,6,7]. This paper reports a sub-1 V ULP low-IF receiver front-end for IoT applications. Exploiting several techniques like source impedance up-scaling, gm-boosting and current reuse, leads to a sub-3dB NF LNA with only 80 µA bias current. Additionally, channel selection filtering is performed using a complex gm-boosted common-gate (CG) TIA, which is robust to offsets. The resulting ULP receiver has the lowest power consumption and low NF among all prior sub-mW receiver designs.

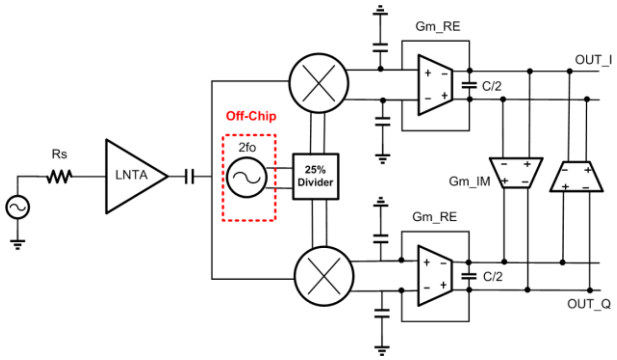

Fig.1. Proposed frontend architecture

II. Receiver Front-End Architecture

Power consumption in a receiver front-end for IoT is the key metric, thus a proper architecture has to be chosen. The zero-IF architecture has no image issue but is affected by some problems, including 1/f noise, DC-offset and even-order distortion, which make it unsuitable for low power operation. Low-IF is the most appealing architecture to address the above-mentioned issues, even though it requires to implement image rejection. Fortunately, in some standard like BLE, blocking requirements are typically very relaxed for nearby channels. Hence, both image rejection and channel selection can be

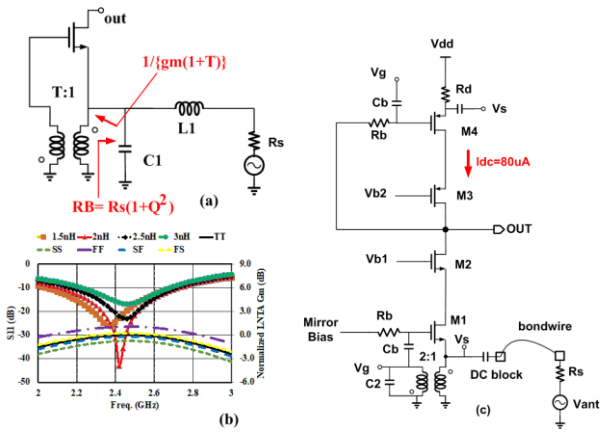

Fig.2. (a) Simplified input matching network, (b) simulated bonding effect on s_{11} and normalized LNTA Gm over PVT, (c) proposed LNTA.

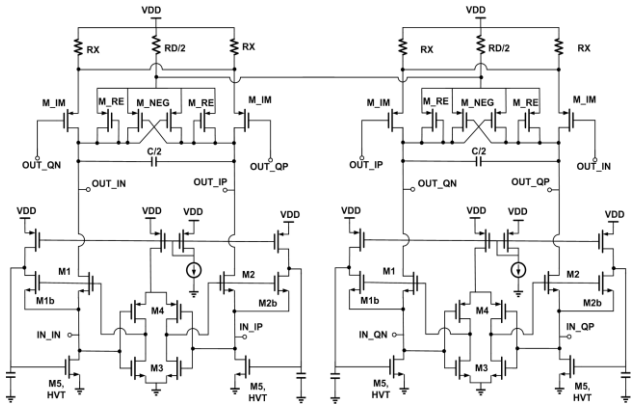

Fig.3. Proposed Gm-boosted CG baseband stage with complex load.

achieved using complex filters. A very low intermediate frequency (IF) (e.g. 1 MHz or less) demands a high selectivity channel selection filter to prevent flicker noise and DC offset from degrading sensitivity. On the other hand, the demodulator performance and the image rejection can be improved by choosing a high IF (e.g. 3 MHz or more), but at the cost of more power dissipation. As a compromise, a 2 MHz IF frequency for a channel bandwidth of 1 MHz are chosen in this work. The block diagram of the proposed current-mode architecture is shown in Fig. 1. It consists of a low-noise trans-impedance amplifier (LNTA) that converts the input voltage to current, followed by current-mode passive mixers driving the complex channel selection filters, which use a Gm-boosted CG topology.

A. LNTA Design

Inductive source degeneration is one of the most popular LNA topologies. Such a circuit can be designed to significantly lower power consumption while adding little noise at the cost of using a big inductor at the gate terminal [6]. This inductor has to be off-chip, leading to higher cost and board complexity. On the other hand, CG amplifiers have better frequency response and linearity, but power matching defines the device transconductance, which makes it, in its basic form, unsuitable for ULP applications. To lower the bias current required by a CG LNTA to implement input matching, our first step is to use an L-match network (implemented with L1 and C1 in Fig. 2a) before the CG device. Such a technique provides 3 dB of voltage gain before the active device and at the same time scales up the source impedance to 100 Ω. This yields a 2x power savings with a modest noise degradation due to passive losses. More substantial power savings are possible increasing the impedance transformation ratio, at the cost of higher passive losses, higher sensitivity to parasitic elements and degraded linearity. As a second step, an inverting transformer with turns ratio of 1:2 (T=2 in Fig. 2a) placed between the source and the gate of the input transistor is used to provide g_m boosting. This lowers the impedance seen at the source of the transistor by a factor of 3 and also improves the noise by the same factor. Combining the two techniques leads to a 6x power saving and 3x noise reduction at the cost of one transformer and one inductor, as shown in Fig. 2a. A transformer with k<1, can be modeled as an ideal impedance transformer with both a parallel and a series inductance at its primary. Moving capacitance C1 from the primary to the secondary, the series inductance forms an L-match that increases the effective transformer voltage boosting factor from 2 to 2.5. This reduces the required value of the explicit inductance L1, making it feasible to rely solely on the bond wire inductance to implement it, significantly reducing chip area. Impedance matching robustness to L1 variations is verified by simulations shown in Fig. 2b. Fig 2b shows that the simulated gain varies by +/- 1.4 dB due to PVT and by less than +/- 0.5 dB in the 2.2-2.7 GHz band. The proposed solution has the same power efficiency of the one proposed in [6] but with 40% more transconductance and 50% less noise. An additional factor of 2 in power saving, without NF degradation, can be achieved using the complementary P-N current reuse scheme reported in Fig. 2c. Notice that the noise of Rd in the PMOS side of the circuit is negligible since, thanks to the low bias current, Rd can be as large as 1.5 kΩ for a 0.9 V supply. Finally, the cascode devices considerably enhance the driving impedance seen by the base-band (BB) stages. This lowers the BB output noise contribution or alternatively allows to drastically lower BB power consumption for the same noise. In summary, in the proposed LNTA, the device g_m needs to be only $(12Rs)^{-1}$ for input matching while the effective transconductance (Gm) is $1/(\sqrt{2}Rs)$ and, neglecting transformer losses, $F=1+\gamma/3$ and the simulated LNTA IIP3 is -8dBm.

B. Baseband Stage

A BB complex filter provides simultaneous channel selection and image rejection in Low-IF receivers. Complex poles can be created by shifting the real poles of the low pass filter along the imaginary axis to create a complex passband transfer function. This can be done using two cross-coupled transconductances between I and Q paths (transistors M_{IM} in Fig. 3). A complex Gm-C filter has the potential to minimize power consumption [4] but includes a common-mode (CM) positive feedback loop, formed by the cross-coupled I and Q Gm-C integrators. It can be shown that, if the IF frequency is chosen to be greater than the passband bandwidth, as required to lower 1/f noise, CM instability can occur. To ensure stability, in [3], additional cross-coupled transistor pairs were introduced in the load to implement a differential-mode negative resistance and a CM positive resistance (transistors M_{NEG} in Fig. 3). However, noise is degraded and, even if stable, the circuit remains quite susceptible to mismatches and offsets. The solution proposed in

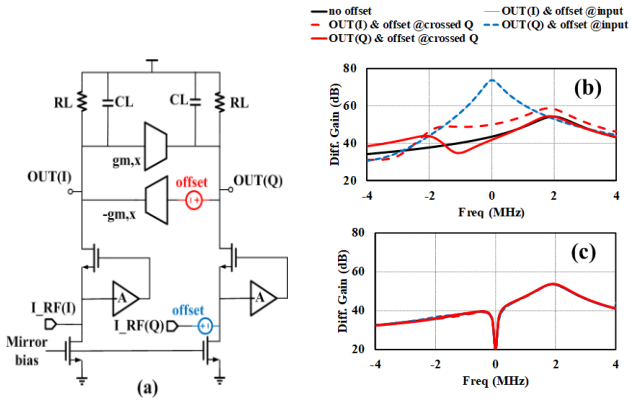

Fig.4. (a) Conceptual BB schematic for offset effect on the differential signal transfer function, (b) using a simple mirror bias and without Rd, Rx (c) with the proposed topology insensitive to offsets.

this paper is to place a power efficient Gm-boosted CG amplifier, that acts as a current-buffer, between the passive mixer and the complex Gm-C load, as shown in Fig. 3. Lower input impedance and much lower noise is achieved by allocating most of the current in the boosting amplifier (transistors M3-4) while reducing the current in the CG (transistors M1-2). As done in [3], cross-coupled transistors M_{NEG} boost differential and reduce CM trans-impedance but with much less additional noise thanks to the reduced current. Drastic noise improvement comes at the cost of lower linearity and earlier compression. To further improve CM stability two additional things are done. First, in both the I and Q branch, the common sources of cross-coupling transistors M_{IM} are resistively degenerated, thereby reducing the CM cross-coupling trans-conductance, without affecting the differential one. Second, the common-sources of M_{RE} and M_{NEG} for the I and Q branches are shorted together and degenerated with a resistor for proper biasing. This creates an additional feedback that reduces the gain of the CM loop involving I and Q branches, pushing it well below unity, while it has no effect on the differential loop. A negative feedback loop through M5 is added to control, in a precise and robust way, the current that runs through M1, M1b and into the complex load. A capacitor C_M (~ 8 pF) is placed at the gate of M5 to stabilize the loop. Notice that if M1 was biased with a simple current mirror, its 1.6 µA nominal DC current could be potentially modulated by the offset present at the output of the passive mixer. This would result in unequal currents into the I/Q branches (as shown in blue in Fig. 4), which could cause large mismatches and even potential instability. In addition, the degeneration resistors Rx and Rd used in the loads reduce the effect of any offset present between the gain of the cross coupled I and Q sides of the filter ($V_{OFF\text{-}IQ}$ in Fig. 4). Without them, the offset could cause unequal transfer functions at the I and Q outputs (as shown in red in Fig. 4). According to simulations, for the same channel bandwidth and center frequency, with the degeneration resistors and the feedback input bias loop (proposed topology) and without them (like in [3]) a CM rejection of -20 dB and -4 dB respectively would result. Finally, the TIA input impedance is:

$$Z_{in} = \frac{1}{g_{m1}(1+((g_{m3}+g_{m4}).(r_{o3}\|r_{o4}))} \quad (1)$$

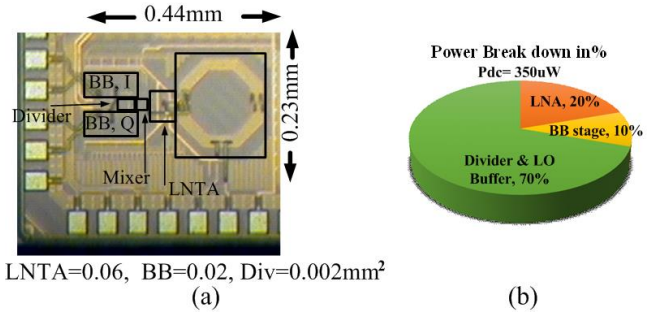

Fig.5. (a) Chip micrograph (b) and power dissipation breakdown.

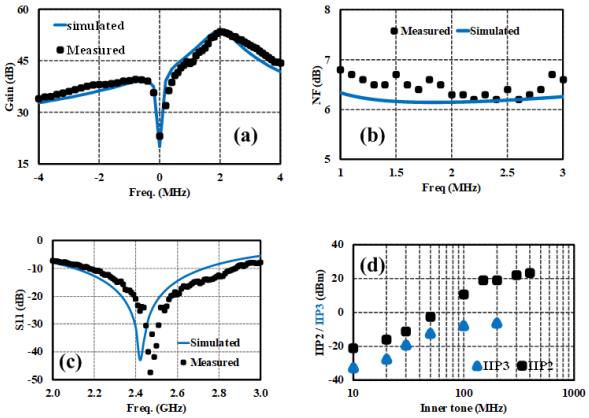

Fig.6. Measured results: (a) Conversion gain, (b) NF, (c) S11, (d) IIP3/2.

The complex pole frequency of the filter is given by:

$$\omega_{complex} = \frac{(gm_{RE}-gm_{NEG})}{[1+(gm_{RE}-gm_{NEG})R_D]C} + j\frac{gm_{IM}}{(1+gm_{IM}R_X)C} \quad (2)$$

where C is the load capacitance while r_o and gm are the output impedance and the transconductance of a generic transistor.

III. Experimental Results

A prototype ULP receiver that operates at 2.4-2.5 GHz was implemented in a standard 28 nm CMOS technology. The chip micrograph is shown in Fig. 5a and occupies an active area of 0.1 mm^2. The front-end consumes only 350 µW of power from a 0.9 V supply, excluding the VCO (Fig. 5(b)). For BLE applications, owing to the relaxed phase noise requirements, the VCO power can be quite low, e.g. the VCO in [7] consumes only 65 µW from an 0.8 V supply voltage. The proposed RX has 53.3 dB conversion gain at the 2 MHz IF frequency and provides 15.3 dB image rejection (IR) as shown in Fig. 6(a). Additional IR can be achieved by cascading a second order complex Gm-C filter at BB (with only 40 µW additional power consumption [3]) or adding a polyphase filter at the BB output. In both cases no NF degradation would result because of the significant gain in front. The minimum NF in the band around the 2 MHz IF frequency is 6.2 dB while the integrated noise over a 1 MHz band is 6.5 dB. Fig. 6(c) shows a good s_{11} in the 2.4-2.5 GHz band, where NF varies less than 0.4 dB. Fig. 6(d) shows the receiver IIP3/2 versus offset with respect to the LO, where the intermodulation product is always kept at 2MHz. The

TABLE I: PERFORMANCES SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RECEIVERs

	This work*	[1]	[2]	[3]	[4]	[5]
Tech (nm)	**28**	65	28	130	65	28
Architecture	**Low-IF**	Low-IF	DC	Low-IF	Low-IF	DT-Low IF
Vdd (V)	**0.9**	0.3	0.18	0.8	1.2/0.6	1
Chip Pdc (µW)	**350**	**1600**	**382**	**600**	**2700**	**2750**
Pdc (µW) w/o VCO	**350**	**1000**	**230**	**530**	**1700**	**2350**
NF (dB)	**6.5**	**6.1**	**11.3**	**15.8**	**9**	**6.5**
Gain (dB)	**53.3**	83	34.5	55	55	46
IIP3 IB/OOB (dBm)	**-32/-8**	-20.6/NA	-12.5/NA	-17/NA	NA/-6	-19/NA
IRR (dB)	**15.3**	NA	26.2	30	28	26
Chip Area [mm^2]	**0.1**	**2.5**	**1.65**	**0.25**	**0.3**	**0.97**
Area ** [mm^2]	**0.1**	**~1.8**	**~1**	**~0.15**	**~0.24**	**~0.6**

*excluding VCO (VCO power can be as low as 65 µW [7]), ** excluding other blocks, estimated from the chip photos.

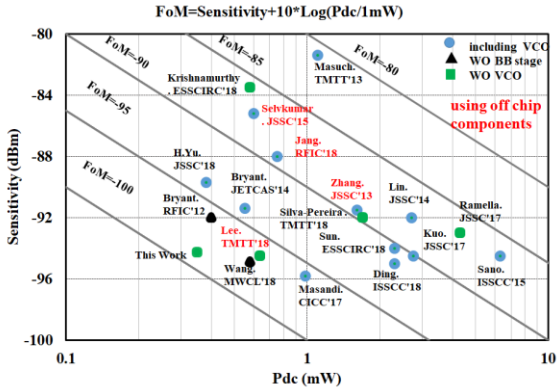

Fig.7. Sensitivity versus power consumption.

RX OOB-IIP3 which is -8 dBm when placing two tones at 100 MHz and 198 MHz away from the LO. Fig. 6 shows also the receiver OOB-IIP2 which is 23 dBm when placing two tones at LO+200MHz and LO+202MHz. For in-band signal and close by frequency, both IIP3 and IIP2 degrade and do not satisfy the BLE specs. This is due to the complex filters and can be improved increasing the current in the CG transistors at essentially no power cost but with some noise degradation. Comparison with the state-of-the-art is given in Table I. Our solution (excluding VCO) consumes the least power among all prior works and does not require high Q off-chip components. While [1, 5] have similar NF, the proposed solution has lower power and area by sacrificing linearity. Moreover, even though [2, 3] implement also sub-mW receivers, they have a NF at least 5 dB higher. Benchmark of only sensitivity versus power consumption of low power RX is shown in Fig.7 [5]. In this plot, sensitivity is obtained based on measured NF in desired channel bandwidth and considering SNR=13 dB. The proposed receiver front-end achieves a FoM of -99 dB, and even adding an extra 100 µW for the VCO (i.e. twice the value of [7]) the resulting -98 dB FoM is still the lowest. Finally, the RX performance has good robustness to process variation.

IV. CONCLUSION

A 0.9 V, 2.4 GHz Low-IF receiver front-end suitable for IoT applications was designed. It has a LNTA that requires only 80 µA for 50 Ω input matching. Scaling up of the source impedance, passive gain boosting and current sharing were used to achieve this result. A Gm-boosted CG amplifier loaded with complex poles selects a 1.4 MHz channel bandwidth cantered at 2 MHz and performs image rejection. In 28 nm CMOS, the receiver consumes 350 µW and has 6.5 dB integrated NF and an OOB-IIP3 of -8 dBm. The receiver achieves a FoM of -99 dB, which to the best knowledge of the authors is the best FoM among ULP receiver frontends reported in the literature. Finally, according to the simulation, IIP3 can be improved by 10 dB at lower offset, at the cost of 3x higher current in CG branch (i.e. in total 10 µA additional current for RX) and less than 1dB NF degradation. Therefore, we conclude that our receiver should be able to exceed the BLE requirements.

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