UNIVERSIDADE FEDERAL DE SANTA CATARINA
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Márcio Bender Machado

ULTRA-LOW-VOLTAGE OSCILLATORS WITH APPLICATION TO ENERGY HARVESTING CIRCUITS

Florianópolis

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Tese submetida ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina para a obtenção do grau de Doutor em Engenharia Elétrica.
Orientador: Dr. Carlos Galup-Montoro
Co-orientador: Dr. Márcio Cherem Schneider

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Márcio Bender Machado

OSCILADORES DE ULTRA-BAIXA-TENSÃO COM APLICAÇÃO EM CIRCUITOS DE CAPTAÇÃO DE ENERGIA

Esta Tese foi julgada adequada para obtenção do Título de Doutor em Engenharia Elétrica e aprovada em sua forma final pelo Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina.
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Carlos Galup-Montoro, Dr.
Coordenador do Curso

Carlos Galup-Montoro, Dr.
Orientador

Márcio Cherem Schneider, Dr.
Co-orientador

Banca Examinadora:

Mohamad Sawan, Dr.

Wilhelmus Adrianus Maria Van Noije, Dr.

Hamilton Klimach, Dr.

Andre Augusto Mariano, Dr.

Paulo Augusto Dal Fabbro, Dr.

Jefferson Luiz Brum Marques, Dr.

A meus pais, Paulo e Celina, a meus irmãos, Marcelo e Lilia, aos meus sobrinhos Lucas, Leo, Nina e Francisco e a Rôsmari, com a qual compartilhei esta jornada.

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ULTRA-LOW-VOLTAGE OSCILLATORS WITH APPLICATION TO ENERGY HARVESTING CIRCUITS

Márcio Bender Machado

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Advisor: Carlos Galup-Montoro, Dr.
Co-advisor: Márcio Cherem Schneider, Dr.
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Keywords: minimum supply voltage, analog circuits, ultra-low-voltage oscillators, ultra-low-voltage step-up converters, zero-VT transistor, energy harvesting.
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This thesis describes the analysis and design of oscillators and charge pumps that can operate with very low supply voltages. The focus is on operation of the MOS transistor in the triode region owing to the limited voltage options available. Special attention has been given to the properties of the zero-VT transistor due to its high drive capability at low voltage. In order to investigate the minimum supply voltage for MOSFET oscillators, three topologies were studied. Two of them, namely the enhanced swing ring and the enhanced swing Colpitts oscillators, can operate with supply voltages below the thermal voltage, kT/q. Simplified theoretical expressions for the minimum supply voltage, oscillation frequency and minimum transistor gain of the oscillators were derived. Measurement results obtained using prototypes built with zero-VT transistors verified the operation of the oscillators for a supply voltage as low as 30 mV and 3.5 mV with high swing amplitude for arrangements built with integrated and off-the-shelf inductors, respectively. The application of the ultra-low-voltage oscillators to energy harvesting circuits was addressed in this work. In order to convert the ac signal of the oscillator into a dc signal, the popular Dickson charge pump converter was employed. Expressions for the output voltage, input resistance and power converter efficiency of the Dickson charge pump operating at ultra-low voltages were derived. Experimental results obtained with prototypes built with the enhanced swing ring oscillator and the Dickson charge pump confirmed the feasibility of obtaining a dc output equal to 1 V at current consumptions of 100 nA and 1 μA from input voltages of 10 mV and 23 mV, respectively.

OSCILADORES DE ULTRA-BAIXA-TENSÃO COM APLICAÇÃO EM CIRCUITOS DE CAPTAÇÃO DE ENERGIA

Márcio Bender Machado

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Orientador: Carlos Galup-Montoro, Dr.
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O presente trabalho apresenta a análise, projeto e experimentação de osciladores e conversores dc-dc elevadores operando a muito baixas tensões de alimentação. Devido aos baixos valores de tensão de alimentação de interesse deste trabalho, especial atenção foi dada à operação do transistor MOS na região triodo e às propriedades do transistor zero-VT, graças a sua alta capacidade de corrente para baixas tensões. Com o objetivo de investigar a mínima tensão de alimentação de osciladores a MOSFET, três topologias foram estudadas. Duas delas, chamadas de oscilador em anel com elevada excursão de sinal e oscilador Colpitts com elevada excursão de sinal, podem trabalhar com tensões de alimentação inferiores à tensão térmica, kT/q. Expressões simplificadas para a mínima tensão de alimentação, frequência de oscilação e mínimo ganho do transistor foram derivadas para cada topologia. Resultados experimentais obtidos com protótipos implementados com transistores zero-VT comprovam a operação dos osciladores com tensões tão baixas quanto 30 mV e 3,5 mV em circuitos construídos com indutores integrados e discretos, respectivamente. A aplicação dos osciladores a circuitos de captação de energia (energy harvesting circuits) a partir de fontes de alimentação de ultra-baixa-tensão foi estudada neste trabalho. Com o propósito de converter tensões ac geradas pelos osciladores em sinais dc, o clássico conversor Dickson foi utilizado. Expressões para a tensão de saída, resistência de entrada e eficiência de conversão de potência do conversor Dickson operando a ultra-baixas-tensões foram derivadas. Re-

sultados experimentais obtidos com protótipos construídos com o oscilador em anel com elevada excursão de sinal e com o conversor Dickson, provaram a possibilidade de se obter uma tensão dc na saída de 1 V para correntes de carga de 100 nA e 1 μA a partir de tensões de entrada de 10 mV e 23 mV, respectivamente.

RESUMO EXPANDIDO

Introdução

A crescente demanda pela autonomia de energia de circuitos relacionados às modernas redes de sensores sem fio e às aplicações biomédicas tem motivado uma redução drástica da potência consumida pelos circuitos eletrônicos atuais. Sistemas complexos capazes de monitorar *in vivo* as atividades de órgãos humanos através, por exemplo, de eletrocardiogramas, eletroencefalogramas ou medidores de pressão ocular e mesmo com capacidade de estimular tecidos humanos, são desenvolvidos consumindo micro-watts de potência [1]-[4]. Devido aos baixos valores de potência consumidos, estes circuitos abrem caminho para uma nova classe de captadores de energia de ultra-baixa-tensão – ULV (*ultra-low-voltage*) e ultra-baixa-potência – ULP (*ultra-low-power*) com capacidade de operar internamente ou ao redor do corpo humano.

Neste cenário, intensa pesquisa tem sido desenvolvida de modo a permitir a colheita de energia através do movimento, calor, luz ou mesmo da glicose presente no corpo humano. Células fotovoltaicas operando em ambientes de baixa luminosidade, geradores termoelétricos, operando a partir da diferença de temperatura entre o corpo-humano e o meio externo e células combustível gerando energia a partir da glicose presente no corpo-humano [17], são exemplos de fontes de energia com potencial de suprir a recente demanda por autonomia de energia. Entretanto, devido a fatores construtivos ou a restrições de área, a tensão gerada por estas fontes varia de dezenas a poucas centenas de milivolts. Assim, de modo a permitir que estas fontes de energia alimentem os circuitos eletrônicos atuais que, em geral, demandam tensões de alimentação de pelo menos 500 mV, conversores elevadores de tensão devem ser utilizados.

Entretanto, elevar tensões da ordem de kT/q, a tensão térmica ($\approx$26 mV à temperatura ambiente), não é uma tarefa simples. De fato, independente da topologia de conversor elevador utilizada, de modo a controlar a transferência de carga e permitir a elevação de tensão, um sinal oscilatório é necessário. Porém, devido à dificuldade em se inicializar osciladores eletrônicos a partir de tensões DC inferiores a 100 mV, o projeto do oscilador se configura como um gargalo no projeto de conversores dc-dc elevadores operando a ultra baixas tensões.

Recentemente, diversos trabalhos têm proposto soluções para

inicializar o conversor usando chaves mecânicas [33], transformadores [28] ou osciladores em anel com um complicado ajuste externo da tensão de limiar VT [10], [59]. Ainda assim, a mínima tensão de inicialização de conversores reportada é de 35 mV [33], ainda com o custo extra em área associado ao uso de indutores e capacitores externos. Neste contexto, o presente trabalho propõem uma redução extrema da tensão de alimentação de osciladores eletrônicos de modo a permitir a elevação de tensões dc tão baixas quanto a tensão térmica, kT/q. Resultados experimentais utilizando transistores zero-VT comprovaram os limites mínimos da tensão de alimentação de osciladores deste trabalho.

A aplicação dos osciladores a circuitos de elevação de tensão foi também estudada nesta tese. Aplicando um modelo do conversor Dickson desenvolvido nesta tese, válido para tensões de operação muito baixas, resultados experimentais comprovaram a possibilidade da conversão de tensão dc-dc a partir de valores de tensão tão baixos quanto 10 mV.

De modo a obter a operações dos circuitos apresentados nesta tese a partir de muito baixas tensões, em todos os projetos desenvolvidos foram utilizados transistores do tipo zero-VT devido à alta capacidade de corrente mesmo operando a ultra baixas tensões.

Objetivos Específicos

- Propor circuitos analógicos que operem a muito baixas tensões.
- Explorar topologias que permitam a obtenção dos limites mínimos de tensão de alimentação de osciladores eletrônicos;
- Desenvolver protótipos de osciladores de tensão com capacidade de operar com tensões de alimentação abaixo do limite de tensão dos circuitos digitais, o limite de Meindl (36 mV à temperatura ambiente) [20];
- Aplicar os osciladores de ultra baixa tensão a circuitos de captação de energia;
- Estudar, modelar e desenvolver um protótipo de conversor dc-dc elevador com capacidade de elevar tensões tão baixas quanto a tensão térmica kT/q.

Resultados

De modo a buscar atingir operação com valores próximos aos limites mínimos de tensão de alimentação de osciladores, três topologias foram apresentadas neste trabalho. Baseado em uma topologia em anel com carga LC, o oscilador em anel indutivo - IRO (*inductive ring oscillator*) apresenta um limite teórico mínimo de tensão que corresponde à metade do limite teórico mínimo de tensão do inversor CMOS (limite de Meindl), 36 mV à temperatura ambiente. Já os osciladores em anel indutivo e Colpitts, ambos com elevada excursão de sinal – ESRO (*enhanced swing ring oscillator*) e ESCO (*enhanced swing Colpitts oscillator*), respectivamente, não apresentam rígidos limites mínimos de tensão, que variam de acordo com razões entre componentes passivos e com as perdas inseridas pelos componentes. Análises considerando a frequência de oscilação, mínimo ganho e mínima tensão de alimentação para inicializar os osciladores, derivadas para cada topologia, exploram o espaço de projeto de osciladores operando a ultra-baixas-tensões.

De modo a comprovar a operação dos osciladores apresentados, seis protótipos foram implementados e testados. Quatro deles, totalmente integrados através da tecnologia IBM 130 nm, possuem tensões de inicialização de 86, 53, 46, e 30 mV, empregando as topologias ESCO, IRO (7 estágios), IRO (2 estágios) e ESRO, respectivamente. Usando transistores zero-VT integrados através do mesmo processo e componentes passivos com alto fator de qualidade, dois protótipos baseados nas topologias ESCO e ESRO são capazes de iniciar oscilações a partir de tensões de alimentação tão baixas quanto 15 e 3,5 mV, respectivamente. Vale ressaltar que os osciladores implementados a partir da topologia ESRO atingiram uma excursão de sinal de 500 mV pico a pico, a uma tensão de alimentação de 77 e 8 mV, considerando o protótipo totalmente integrado e usando indutores externos, respectivamente. Uma redução drástica da potência consumida ainda é verificada através dos protótipos implementados.

Considerando os baixos valores de tensão de interesse deste trabalho, o modelo convencional do conversor Dickson [58] que considera constante a queda de tensão sobre os diodos não pôde ser aplicado. Assim, um modelo que considera a queda de tensão nos diodos a partir da corrente de carga do conversor e das características físicas dos diodos é proposto nesta tese. Expressões para a tensão de saída, resistência de entrada e eficiência de conversão de energia do conversor operando a muito baixas tensões foram derivadas.

Resultados experimentais aplicando os modelos desenvolvidos sobre os osciladores e o conversor Dickson, ambos operando a ultra baixas tensões comprovaram a possibilidade da conversão de tensão dc-dc a partir de valores de tensão tão baixos quanto kT/q. Três protótipos foram implementados gerando uma saída dc de 1V a partir de uma tensão de entrada V_{in}=86 mV (para uma corrente de carga I_L=1 μA), V_{in}=23 mV (para I_L=1 μA) e V_{in}=10 mV (para I_L=100 nA) considerando um protótipo totalmente integrado, um outro integrado exceto pelos indutores externos e um terceiro usando componentes discretos, respectivamente.

Até o momento da escrita desta tese, este trabalho apresenta a menor tensão de operação de osciladores e conversores dc-dc elevadores totalmente integrados ou mesmo utilizando componentes externos.

Durante o desenvolvimento deste trabalho, três artigos foram submetidos a periódicos internacionais (dois publicados e um aguardando o processo de revisão), sete artigos publicados em anais de conferências internacionais e seis trabalhos submetidos a workshops em três países, Estados Unidos, México e Brasil. Além disso, o artigo intitulado *"10 mV - 1 V Step-up converter for energy harvesting applications"* recebeu o prêmio de melhor artigo do SBCCI 2014, *the best paper award of the 27th SBCCI*, que foi realizado em Aracajú, SE, Brazil.

Comentários Finais

Neste trabalho, utilizando-se transistores do tipo zero-VT operando na região linear, indutores com alto fator de qualidade e topologias simples, porém ideias para operação a ultra-baixas-tensões, é comprovada a operação de circuitos analógicos muito abaixo do limite de Meindl. Tal resultado, além de demonstrar a possibilidade de circuitos analógicos operarem com limites mínimos de tensão abaixo dos de circuitos digitais, abre novas possibilidades dentro das recentes demandas da eletrônica moderna, que requer rígidas especificações de consumo de potência e baixos níveis de tensão. Desta forma, ainda há muito a ser feito em relação extensão dos conceitos de ultra-baixa-tensão apresentados neste estudo a sistemas eletrônicos práticos e ao aprimoramento das topologias trabalhadas, incluindo testes de variabilidade e de variação de temperatura e a integração dos mesmos

em tecnologias mais modernas.

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LIST OF ABBREVIATIONS

AC - Alternating current
CMOS - Complementary metal oxide semiconductor
DC - Direct current
EDA - Electronic design automation
ESCO - Enhanced swing Colpitts oscillator
ESRO - Enhanced swing ring oscillator
GSM - Global System for Mobile
IRO - Inductive ring oscillator
JFET - Junction field effect transistor
MOS - Metal oxide semiconductor
MOSFET - Metal oxide semiconductor field effect transistor
NMOS - N-type metal oxide semiconductor
PCE - Power converter efficiency
PMOS - P-type metal oxide semiconductor
QFN - Quad flat no-leads
RF - Radio frequency
SI - Strong Inversion
SMD - Surface mounted devices
TEG - Thermoelectric generator
UICM - Unified current control model
ULP - Ultra low power
ULV - Ultra low voltage
VLSI - Very large scale integration
WI - Weak inversion

LIST OF SYMBOLS

a - Voltage gain V_d/V_s
C_{db} - Drain-bulk capacitance
C_{gb} - Gate-bulk capacitance
C_{gd} - Gate-drain capacitance
C_{gs} - Gate-source capacitance
C_{jd} - Drain junction capacitance
C'_{ox} - Oxide capacitance per unit area
C_{ox} - Oxide capacitance
f_{osc} - Oscillation frequency
f_T - Transistor unit gain frequency
g_m - Gate transconductance
g_{mb} - Bulk transconductance
g_{md} - Drain transconductance
g_{ms} - Source transconductance
G_P - Inductor parallel conductance
I_0 - Modified Bessel function of the first kind of order zero
I_1 - Modified Bessel function of the first kind of order one
I_D - Drain current
I_{DC} - dc current consumption
I_F - Forward saturation current
i_f - Forward normalized current
I_L - Load current
I_R - Reverse saturation current
i_r - Reverse normalized current
I_{sat} - Diode saturation current
I_S - Specific current (normalization current)
I_{SQ} - Sheet normalization current ($I_S/(W/L)$)
k - Boltzmann's constant
K_L - Ratio L_2/L_1
L - Channel length
n - Transistor slope factor
n - Diode ideality factor
N - Number of stages
P_{in} - Input power
P_{loss} - Power loss due to the diodes of the Dickson charge pump
P_{out} - Output power
q - Electronic charge
Q - Inductor quality factor
R_S - Inductor series resistance

R_{Therm} - Internal resistance of the thermoelectric generator
S - Seebeck coefficient
T - Absolute temperature
V_A - Peak amplitude of a sine signal
V_B - Bulk voltage
v_d - Small-signal drain voltage
V_d - Diode forward voltage drop
V_D - Drain voltage
V_{DS} - Drain-source voltage
V_G - Gate voltage
V_{GS} - Gate-source voltage
v_s - Small-signal source voltage
V_S - Source voltage
V_P - Pinch-off voltage
V_P - Peak voltage of a square signal
V_{PP} - Peak-to-peak voltage
V_T - Threshold voltage
V_{DD} - Supply voltage
$V_{DD,min}$ - Minimum supply voltage
V_{Therm}- The thermoelectric generator open circuit voltage
W - Channel width
Δf - Offset frequency
Δ_T - Temperature difference
ϕ_t - Thermal voltage
$\mathcal{L}(f)$ - Phase noise
μ - Effective mobility
ϕ - Phase shift between the output and the input
ω - Angular frequency

1 INTRODUCTION

The recent demand for energy autonomy has pushed the power budget of some critical circuits in wireless sensor nodes and implantable biomedical applications to low values. Complex systems able to monitor *in vivo* the activity of human organs, such as in electrocardiogram, electroencephalogram or intraocular pressure examinations, and even to stimulate human tissues, consuming some dozens of micro-watts [1], [2], [3], [4], open space for a new class of ultra-low-power (ULP) and ultra-low-voltage (ULV) energy harvesting generators, with the capability to operate around or inside the human body [5], [6]. However, due to the low voltage levels generated by these energy sources (as low as 50 mV), the use of electronic circuits that can operate, or at least start up, with such low voltages, is mandatory.

In addition, lowering the supply voltage of electronic circuits is one of the most effective strategies for achieving low energy consumption [7], [8]. In fact, the dynamic power consumption of digital circuits is proportional to the square of the supply voltage. Thus, to meet the recent demand for miniaturization and energy autonomy, the search for ultra-low-voltage and ultra-low-power circuits has never been more intense.

The main objective of this research was the extreme reduction of the supply voltage of a very important electronic component, the oscillator. This component, which is of great importance in communication systems, is also essential for the boosting of lower voltages (such as those generated by the ULV harvested sources) to the higher levels needed to supply current electronics ($V_{DD} > 500$ mV).

Employing appropriate circuit techniques and native devices, the generation of oscillations from less than 4 mV of supply voltage is demonstrated herein, opening the path to controlling the operation of step-up converters able to convert input voltages of the order of 10 mV to 1V at the output.

1.1 ULP/ULV ENERGY HARVESTING SOURCES

Motivated by the demand for energy autonomy for devices operating around or inside the human body, intensive research in the field of solar, thermal, motion and biological energy scavenging has been carried out. A comparison between the power delivery capabil-

ity of some harvesting sources applicable to sensor networks is shown in Table 1 [9].

Table 1: Typical power delivery capability of some energy harvesting sources [9].

Source	Harvested Power
Light $_{Outdoor}$	10 mW/cm^2
Light $_{Indoor}$	10 μW/cm^2
Motion $_{Human}$	4 μW/cm^2
Thermal energy $_{Human}$	30 μW/cm^2

As an example of a well-developed technology [9], photovoltaic cells are used as a power supply for many ULP applications, such as that illustrated in Fig. 1, which shows a wristwatch powered by a solar cell. In an outdoor environment the voltage generated by a photovoltaic cell can be of the order of some volts, but indoors this decreases to a few hundred millivolts [10], [11]. Another interesting ULV energy harvesting source is obtained by trees, which a difference of pH between the tree and the soil can generate voltages ranging from 50 mV to 200 mV for outdoor applications [12].

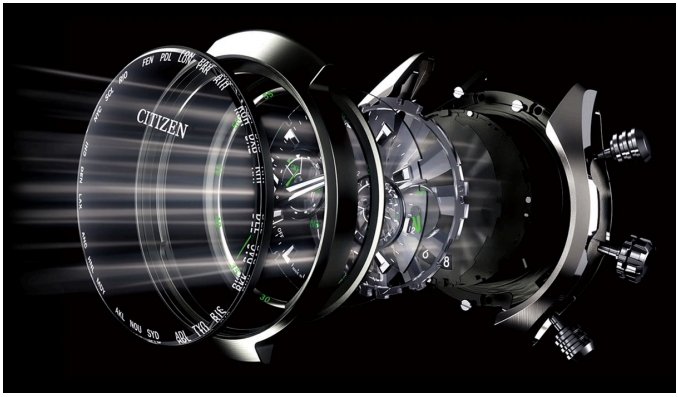


Figure 1: Wristwatch built with a photovoltaic cell. Source: www.citizenwatch.com.

The energy provided by the difference in temperature between the human body and the environment is a very convenient way to supply power to electronics. In fact, the thermoelectric generator (TEG), which converts temperature differences into electrical energy using the Seebeck effect has been intensively studied for wearable appli-

cations [5], [6], [9], [13] since its introduction in 1978 by Bulova to supply power to a wristwatch.

TEGs are commonly comprised of a large number of thermocouples (association of legs of n-type and p-type semiconductor materials), connected thermally in parallel and electrically in series, as shown in Fig. 2 [5]. A TEG modeled by a voltage source V_{Therm} in series with a resistance R_{Therm} generates an open voltage given by $V_{Therm} = S.\Delta_T$, where Δ_T is the temperature difference and S is the Seebeck coefficient.

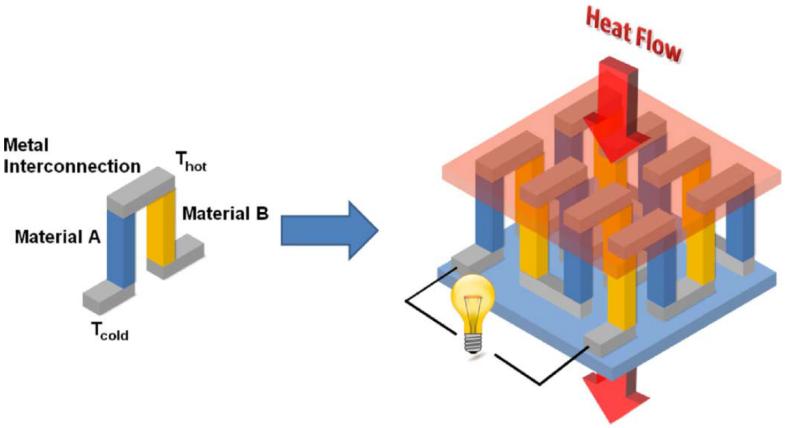


Figure 2: Internal connections of a thermoelectric generator. Source [5].

In wearable applications, the voltage generated by TEGs is usually too small to directly supply current electronics ($V_{DD} > 500$ mV). Due to the thermal resistances of the sink source (the human body) and the environment, it is hard to obtain an effective temperature difference higher than 1°C [5]. Also, due to constructive limitations, it is impossible to obtain simultaneous optimization of the power generated and the voltage [5]. In order to maintain an internal resistance of a few ohm, the S value for commercial TEGs normally ranges from 10 to 75 mV/K, providing around a few dozen millivolts at the output in wearable applications.

The use of fuel cells which generate energy from the human body is a very attractive option, particularly for biomedical applications. Without the need for battery replacement, fuel cells have been the object of study since the 1960s [14]. Recently, some authors have verified the possibility of delivering micro-watts from glucose inside the human body [15], [16], for example, from the cerebrospinal fluid,

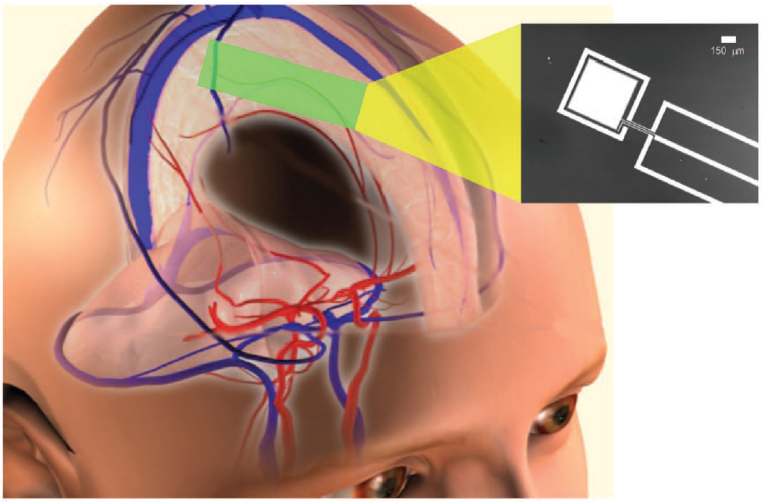


Figure 3: Power extraction from cerebrospinal fluid using an implantable glucose fuel cell. Source [17].

as illustrated in Fig. 3 [17]. However, the voltage generated ranges from dozens to a few hundred millivolts.

Thus, due to the ULV levels generated by these energy harvesting sources, a boost converter is needed to provide a supply voltage of the order of 1 V, as commonly required in the current electronics sector.

1.2 THE SIGNIFICANCE OF ULTRA-LOW-VOLTAGE ELECTRONICS

The need for portable and greener computing is at the origin of ultra-low-voltage (ULV) digital circuits operating with supply voltages in the range of 100-400 mV (see, for example, [18] and references therein). The motivation for continuously reducing the supply voltage is as intense as ever because of the continuous development of very-large-scale integration (VLSI) technologies, as can be seen in recent publications [7], [18]. In [19], Meindl, based on the weak inversion model of the CMOS inverter of [20], concluded that the lower bound for the supply voltage of the CMOS inverter is

$$V_{DD,min} = 2\phi_t \ln(1+n) \tag{1.1}$$

where $\phi_t = kT/q$ is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge and n is the slope factor. For an ideal MOSFET ($n = 1$) at room temperature, (1.1) gives $V_{DD,min} = 36$ mV. This minimum value for the supply voltage results from the analysis of the static transfer curve of the CMOS inverter with matched n- and p-channel MOSFETs. The maximum voltage gain, which occurs at the midpoint of the voltage transfer curve, must be higher than unity and the supply voltage required to achieve this gain is given by (1.1). CMOS digital circuits are getting closer to the lower boundary for V_{DD} given by (1.1). The use of feedback to match the subthreshold n- and p-channel MOSFET currents allows digital CMOS circuits in a standard 180 nm CMOS technology to operate at $V_{DD} = 4kT/q$ [21]. More recently, operation at room temperature with $V_{DD} = 62$ mV was achieved using logic gates built around Schmitt triggers [22].

For analog circuits, the minimum practical supply voltage has generally been considered to be higher than the minimum necessary for the operation of digital circuits. The reason for this is that, in most analog circuits, one or more transistors that operate in saturation are stacked between V_{DD} and ground and thus the supply voltage needs to be at least 100 mV (see [23] and the referenced therein for a discussion on the $V_{DD,min}$ of analog circuits). However, rectifiers have appeared recently as an exception to this rule. In effect, recent studies [24], [25] motivated by energy harvesting show that rectifiers and voltage multipliers can operate efficiently even with input voltages below the thermal voltage kT/q.

Blocking oscillators using JFETs [26] or native MOSFETs [27], [28] also operate with V_{DD} below 100 mV . The oscillators of refs. [26], [27] act as start-up circuits in off-the-shelf energy harvesting devices capable of operating from supply voltages as low as 20 mV provided by thermoelectric generators. Since transistors are not able to provide the necessary voltage gain at such low supply voltages, the supplementary gain necessary to start up oscillations is obtained from feedback transformers with primary-secondary turns ratios of around 1:100. A web-site [29] reports some blocking oscillators prototype circuit that starts to oscillate at very-low-voltages at the expense of some discrete transformers.

A reduction in V_{DD} is usually related to degradation of the MOS performance, indicated by a reduction in the gate transconductance. However, as shown in [8] and [30], a reduction in the MOSFET threshold voltage, V_T, is a very attractive way to mitigate the lack of tran-

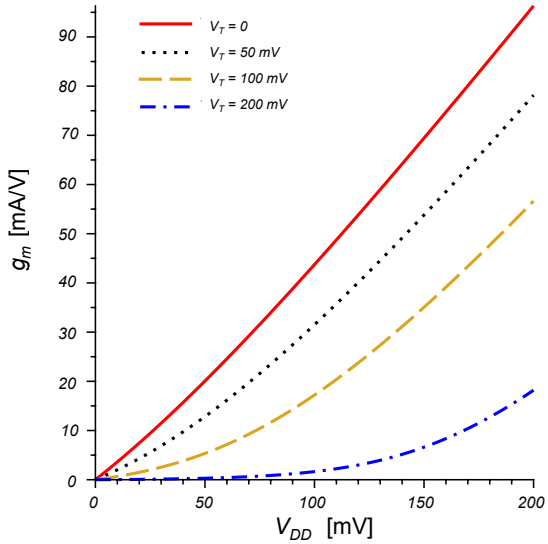


Figure 4: Relation between g_m and V_{DD} for V_T = 0, 50, 100, and 200 mV.

sistor performance at low voltages. In order to illustrate this, Fig. 4 shows the theoretical variation in g_m (obtained from the MOSFET model presented in Appendix A) in terms of V_{DD} for V_T ranging from 0 to 200 mV. The graph was obtained for $V_S = V_B = 0$, $V_D = V_G = V_{DD}$. $I_S = 280$ μA for all calculated curves.

1.3 THE NATIVE TRANSISTOR

Selecting an appropriate technology is of paramount importance for ULV circuits. Enhancement-mode devices, such as MOS transistors with threshold voltage in the range of 0.3-0.5 V, operate with very low current density for supply voltages below 100 mV and are thus of very limited practical utility. On the other hand, depletion-mode devices, such as MOSFETs or JFETs, can supply relatively high current densities for low supply voltages, but they present two drawbacks; they are neither available in conventional technologies nor provide enough voltage gain for low voltages.

In between enhanced and depletion devices, MOS transistors with zero or near zero threshold voltage are particularly suitable for ULV circuits due to their current drive capability and sufficient voltage gain at very low supply voltages. As can be seen in the experi-

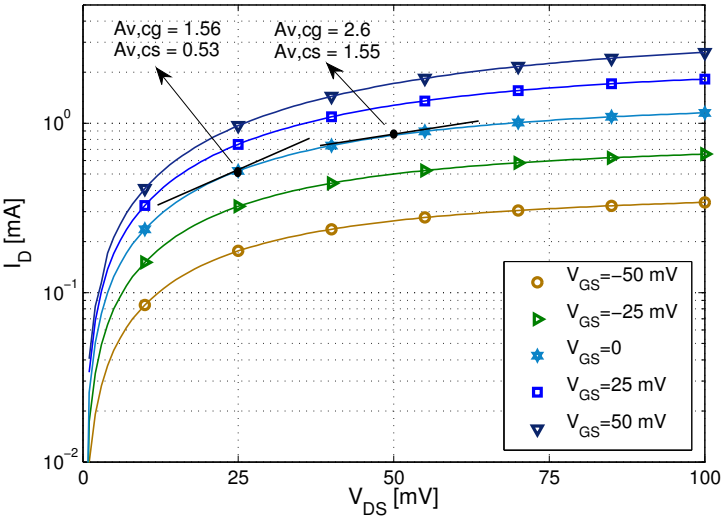


Figure 5: I_D *vs.* V_{DS} ($V_S = V_B$) characteristics for a zero-VT transistor with W/L=2500 μm/420 nm.

mental plot of I_D *vs.* V_{DS} for a zero-VT transistor in Fig. 5, the device presents a current capability of some hundreds of micro-amperes, even for low-V_{DS}.

The close-to-zero value of the threshold voltage of a zero-VT n-type MOS transistor, also called a native transistor, is achieved by blocking the p-well implants (a fabrication step commonly employed to control the V_T in modern technologies). Because of the low p-well doping, the short- channel effects of zero-VT transistors are more severe than in standard devices [8], [31]. Thus, in order to mitigate these, the minimum dimensions of the zero-VT transistor are greater than those of the standard MOSFET. In the IBM 130 nm technology, the minimum W and L of the zero-VT are 3000 and 420 nm, whereas those of the standard transistors are 160 and 120 nm, respectively.

The intrinsic voltage gains of the common-gate and common-source amplifiers, $A_{v,cg}$ and $A_{v,cs}$, respectively, of a zero-VT transistor are also shown in Fig. 5. Considering the operation of the transistor in weak inversion (WI) in the triode region [32],

$$A_{v,cg} = \frac{g_{ms}}{g_{md}} = e^{\frac{qV_{DS}}{kT}} \tag{1.2}$$

$$A_{v,cs} = \frac{g_m}{g_{md}} = \frac{1}{n}\left(e^{\frac{qV_{DS}}{kT}} - 1\right) \tag{1.3}$$

where g_{ms} and g_{md} represent the source and drain transconductances, respectively. For the common-source amplifier, the voltage gain equals unity for $V_{DS} = (kT/q)\ln(1+n)$. Regenerative logic circuits require a voltage gain of at least unity for their proper operation. Therefore, in the case of the "symmetric" CMOS inverter, the minimum supply voltage $V_{DD} = 2(kT/q)\ln(1+n)$ deduced in [19] can be directly derived from (1.3). For ideal MOSFETs, *i.e*, $n = 1$, $V_{DDmin} =$ 36 mV at room temperature.

On the other hand, the common-gate amplifier provides a voltage gain of greater than unity for $V_{DS} > 0$. This property of the common-gate amplifier is very useful for lowering the supply voltage limit for the operation of oscillators.

1.3.1 Comparison between Standard, Low-VT and Zero-VT Transistors

In order to compare the usefulness of MOS transistors for low supply voltages, we can use the ratio of the drain current to the transistor gate area as a figure of merit or, equivalently, the transconductance-to-gate-capacitance ratio g_m/C_{ox}, which is proportional to the unity gain or cutoff frequency f_T of the device. Figure 6 shows the f_T values for zero-VT, low-VT and standard transistors in terms of the supply voltage for minimum-channel-length devices in the 130 nm CMOS technology. Nominal threshold voltages are 5, 245 and 340 mV, respectively. The current densities I_D/W for the three types of transistors with $V_{GS} = V_{DS} = 50$ mV are around 300 nA/μm, 980 pA/μm and 140 pA/μm, respectively.

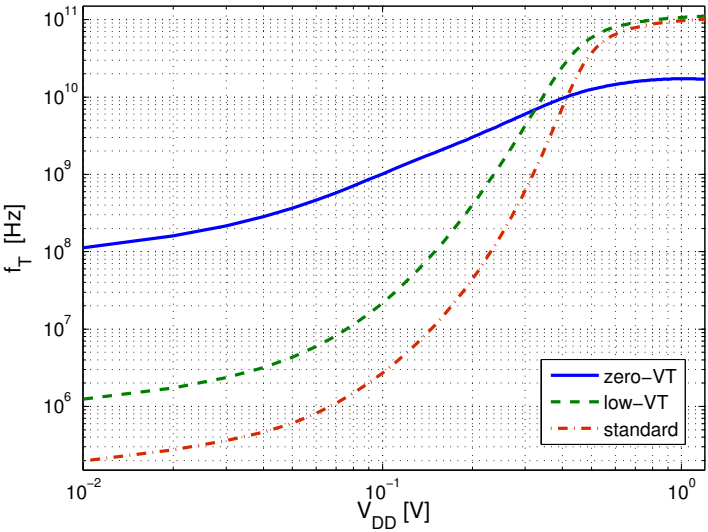


Figure 6: First-order approximation of the intrinsic cutoff frequency of the zero-VT (W/L=3μm/0.42μm), low-VT (W/L=0.84μm/0.12μm), and standard (W/L=0.84μm/0.12μm) transistors of the 130 nm CMOS technology. The transconductance g_m was simulated for $V_S = V_B = 0$, and $V_D = V_G = V_{DD}$.

The curves for the first-order approximation of the intrinsic cutoff frequencies in Fig. 6 clearly show the advantage of the zero-VT transistor over the low-VT and standard transistors for low supply voltages in applications where high current drive capability and/or high frequency operation is a must. Note that for supply voltages below 50 mV, the zero-VT transistor is faster than the low-VT transistor by two orders of magnitude and it is almost three orders of magnitude faster than the standard transistor. On the other hand, for supply voltages of some hundreds of mV the speed of the zero-VT transistor becomes lower than those of the other two transistors since its channel length is around three times the length of the channel of the other two transistors.

The experimental characterization of the zero-VT transistors used in this study is shown in Appendix B.

1.4 PURPOSE OF THIS STUDY

Following the current trend toward low supply voltages, in this research several oscillator configurations were explored for energy harvesting applications, at ultra-low voltages.

Considering the energy harvesting sources mentioned above, converting levels as low as 10 mV to a dc voltage in the range of 0.5 - 1.0 V, typically required to power current electronic circuitry, is not an easy task. In fact, as can be seen in the conceptual scheme of a step-up converter in Fig. 7, independently of the step-up converter topology, an oscillatory signal is needed in order to control the energy transfer between energy storage devices. However, due to the extreme difficulty associated with generating oscillatory signals from supply voltages below 100 mV, the generation of oscillations from energy harvesters represents a "bottleneck" in the design of ULV converters. Despite the fact that in the last few years mechanical switches, external transformers, or post-layout tuned oscillators have been used in some topologies to address this subject [10], [28], [33], obtaining a further reduction in V_{DD} using fully-integrated and discrete oscillators remains an unsolved problem. Also, due to the losses associated with the active switches, the operation of boost converters with the ability to start up with supply voltages below 100 mV has still to be demonstrated.

Employing native transistors operating in the triode region, high Q inductors and simple topologies, a reduction of the minimum supply voltage of oscillators to levels lower than the thermal voltage, kT/q, is proposed herein. An energy harvesting application is also addressed in this thesis. With a consistent theoretical model of the Dickson charge pump, the dc voltage conversion from very low voltages is verified experimentally.

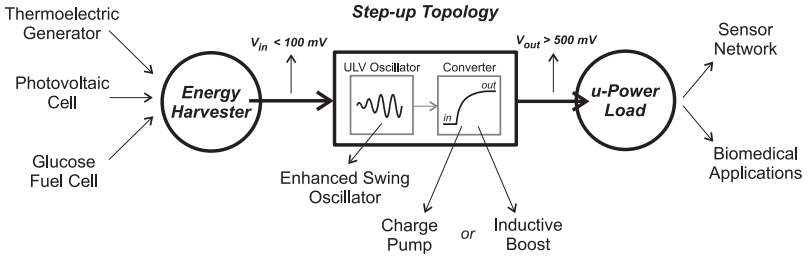


Figure 7: The conceptualization of an ULV step-up topology.

1.5 ORGANIZATION OF THE MANUSCRIPT

This manuscript is divided into six chapters. Following this introduction, Chapter 2 introduces three ULV oscillator topologies. The analysis and the experimental results for each arrangement are presented in Chapters 2 and 3, respectively. The study on the charge pump operating from very low voltages is described in Chapter 4. The experimental results obtained from a circuit design based on the analysis detailed in Chapters 2 and 4 for ULV oscillators and the Dickson charge pump are reported in Chapter 5. The main results of this thesis are summarized in Chapter 6. The MOSFET model, the characterization of the zero-VT transistor and a list of implemented chips and published papers are presented in the Appendices.

2 ULTRA-LOW-VOLTAGE OSCILLATORS

With the aim of reducing, as far as possible the minimum supply voltage of oscillators, in this chapter three topologies which can operate well below 100 mV of V_{DD} are presented. Two of these topologies, namely the inductive ring oscillator (IRO) and the enhanced swing ring oscillator (ESRO), are based on a ring topology, while the third, the enhanced Colpitts oscillator (ESCO), is based on the classical Colpitts oscillator. In order to reach the minimum operational voltage levels, high drive capability zero-VT transistors are employed.

For circuits with supply voltages of 100 mV or less, transistors usually operate in weak (WI) or moderate (MI) inversion. Additionally, there is not sufficient voltage headroom to operate MOS transistors in saturation. For these reasons, in this study a transistor model valid in all operating regions was employed, which is summarized in Appendix A.

For each oscillator, theoretical expressions are provided for the oscillation frequency, the minimum transistor gain and the minimum supply voltage. At the end of the chapter, a comparative table of the oscillators summarizes the main results.

2.1 THE INDUCTIVE RING OSCILLATOR - IRO

Starting up a conventional ring oscillator with a power supply below 100 mV is extremely difficult [34]. The minimum value of the supply voltage, $V_{DD,min}$, is usually limited by the imbalance of the threshold voltage of the PMOS/NMOS transistors of the logic inverter caused by within-die and die-to-die variations [34]. In order to obtain an oscillator which starts up from a $V_{DD,min}$ value lower than that of the conventional ring oscillator, the inductive ring oscillator shown in Fig. 8 can be used. This topology, which replaces the PMOS transistor of logic inverters with an inductor, can not only reduce $V_{DD,min}$ but also boost the amplitude of the oscillations beyond the supply voltage. It should be noted that when the number of stages is $N = 2$ the inductive ring is reduced to the widely used cross-coupled LC oscillator.

In the recent years, many papers on inductive ring oscillators have been published [35]-[39]. The goal of these studies was to achieve tera-Hz frequencies, very low phase-noise and/or multiple phase signals, but the focus was not on low supply voltage operation.

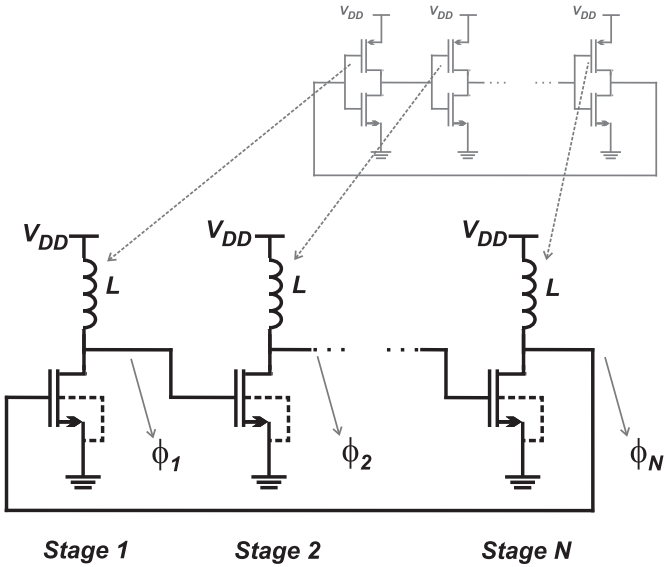


Figure 8: Schematic diagram of an N-stage inductive ring oscillator.

2.1.1 Analysis

The analysis of the N-stage IRO is based on the simplified small-signal equivalent circuit of a single stage of the IRO shown in Fig. 9, where g_m and g_{md} represent the gate and drain transconductances, respectively, C is the sum of all parasitc capacitances between the drain node and the ac ground, and G_P models the inductor losses. For the sake of simplicity, here it can be assumed that the drain-to-gate capacitance C_{gd} is negligible. A complete analysis of the IRO, including C_{gd}, can be found in Section 2.1.1.4. The transfer function of the single stage in Fig. 9 is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md} + G_P + \frac{1}{sL} + sC} \tag{2.1}$$

which can be written as

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md} + G_P} \frac{1}{1 - j\tan\phi} \tag{2.2}$$

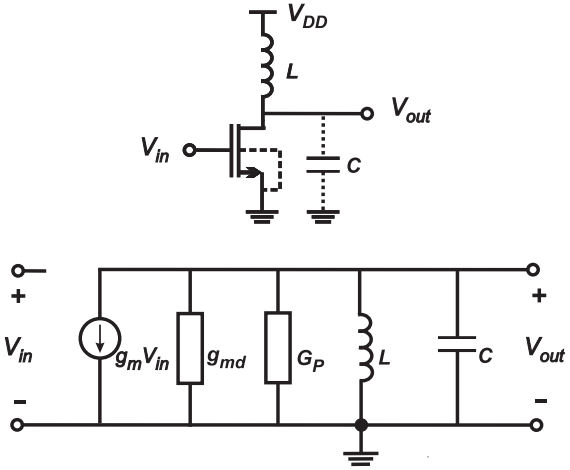


Figure 9: Simplified small-signal model of a single stage of the inductive ring oscillator.

$$\tan\phi = \frac{1 - LC\omega^2}{\omega L(g_{md} + G_P)} \tag{2.3}$$

where ϕ is the phase shift between the output and the input signals.

The condition of loop gain equal to unity for oscillation requires the phase shift ϕ between two adjacent stages to be

$$\phi(k) = \frac{2k\pi}{N} \tag{2.4}$$

where N is the number of stages and k is an integer number. Except for $N = 2$ and 4, more than a single value for the phase shift satisfies the phase condition required for oscillation, as shown in Fig. 10. However, as explained in [37] and [40], the circuit tends to oscillate at the frequency for which the gain is the highest. For an even number of stages we have $\phi = \pi$, while for the case of an odd number of stages $\phi = (N-1)\pi/N$.

2.1.1.1 Frequency of Oscillation

From the phase-shift between two contiguous stages of the oscillator, the oscillation frequency can be found. Therefore, from (2.3),

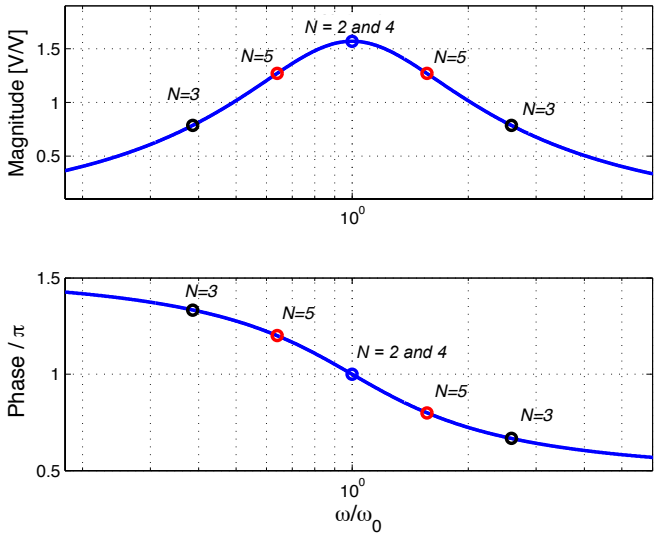


Figure 10: Magnitude and phase, (from (2.2)), of the transfer function of a single stage of the inductive ring oscillator with indication of the possible phase-shit values which satisfies (2.4) for N ranging from 2 to 5.

we can calculate the oscillation frequency ω as

$$\frac{\omega}{\omega_0} = \sqrt{1 + \frac{(\tan\phi)^2}{4Q^2}} - \frac{\tan\phi}{2Q} \tag{2.5}$$

where $\omega_0 = 1/\sqrt{LC}$ is the resonant frequency of the LC tank and $Q = 1/[(g_{md} + G_p)\omega_0 L]$ is the quality factor of the stage. Note that when the condition $\phi = \pi$ holds, which is the case for an even number of stages, ω equals ω_0.

The dispersion relation of a stage (eq. (2.5)), which shows the dependence of ω/ω_0 on ϕ, is shown in Fig. 11. It is clear that, for $Q >$ 100, we have $\omega/\omega_0 \cong 1$.

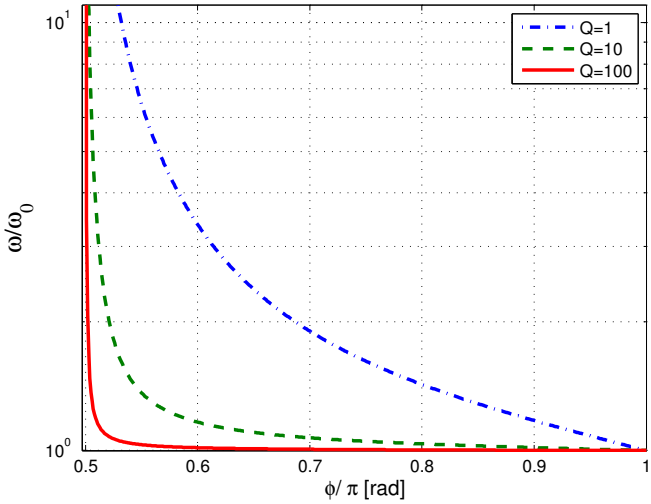


Figure 11: The dispersion relation of a single stage of the inductive ring oscillator for different quality factors.

2.1.1.2 Minimum Transistor Gain Required for Oscillation Start-up

Based on (2.2), considering the loop gain of an N-stage IRO, given by

$$H(j\omega) = \left(-\frac{g_m}{g_{md} + G_P}\right)^N \frac{1}{(1 - j\tan\phi)^N} \tag{2.6}$$

the requirement of greater than unity gain for the starting up of oscillations is satisfied for

$$\frac{g_m}{g_{md} + G_P} \frac{1}{\sqrt{1 + (\tan\phi)^2}} > 1 \tag{2.7}$$

Since the relation between source, drain and gate transconductances, g_{ms}, g_{md}, and g_m, respectively, is $g_m = (g_{ms} - g_{md})/n$ (Appendix A), where n is the transistor slope factor, the minimum transistor gain

g_{ms}/g_{md} required for oscillation is obtained from (2.7) as

$$\frac{g_{ms}}{g_{md}} > 1 + n\sqrt{1+(\tan\phi)^2}\left(1+\frac{G_P}{g_{md}}\right) \tag{2.8}$$

2.1.1.3 Minimum Supply Voltage Required for Oscillation Start-up

From the MOSFET model described in Appendix A and equation (2.8), it is possible to calculate the minimum supply voltage required for the start-up of the oscillator. From the expression for the drain-source voltage (V_{DS}) in Appendix A, we have

$$\frac{V_{DS}}{\phi_t} = \frac{\phi_t}{2I_S} g_{md}\left(\frac{g_{ms}}{g_{md}} - 1\right) + \ln\frac{g_{ms}}{g_{md}} \tag{2.9}$$

For each transistor in Fig. 8 we have the following dc values: $V_S = V_B = 0$ and $V_G = V_D = V_{DD}$. It can be noted from (2.9) that, for a fixed g_{md}, the minimum $V_{DS}(= V_{DD})$ is reached for the minimum value of the g_{ms}/g_{md} ratio given in (2.8). Thus, based on (2.8) and (2.9) we find that the minimum supply voltage required to start up the oscillator is

$$V_{DD} = \frac{\phi_t^2}{2I_S} n g_{md}\left(1+\frac{G_P}{g_{md}}\right)\sqrt{1+(\tan\phi)^2} + \phi_t \ln\left[1 + n\sqrt{1+(\tan\phi)^2}\left(1+\frac{G_P}{g_{md}}\right)\right] \tag{2.10}$$

The minimum voltage supply limit of the IRO topology can be obtained assuming that the transistor operates only in weak inversion, $\phi = \pi$ and that the inductor losses are negligible. Thus, from (2.10)

$$V_{DD,lim} = \phi_t \ln(1+n) \tag{2.11}$$

for the case of an even number of stages. Assuming that n =1, the limit given by (2.11) is around 18 mV at room temperature. This limit shows that the circuit can theoretically operate with one half the value of the Meindl limit [19] of digital circuits, which for a CMOS inverter is 36 mV at room temperature. This result was to be expected since the condition required for oscillation of a ring oscillator with an even number of stages (loaded with an infinite-Q tank) is that the voltage gain of the transistor equals unity. The unity gain of a transistor operating in weak inversion is obtained for a power supply of 18 mV at room temperature [32].

2.1.1.4 The Effect of C_{gd} on the Oscillation Frequency

A single stage of the inductive ring oscillator, as well as its small-signal model with the inclusion of the gate-drain capacitance C_{gd}, is shown in Fig. 12, where the symbols have the same meaning as in Fig. 9.

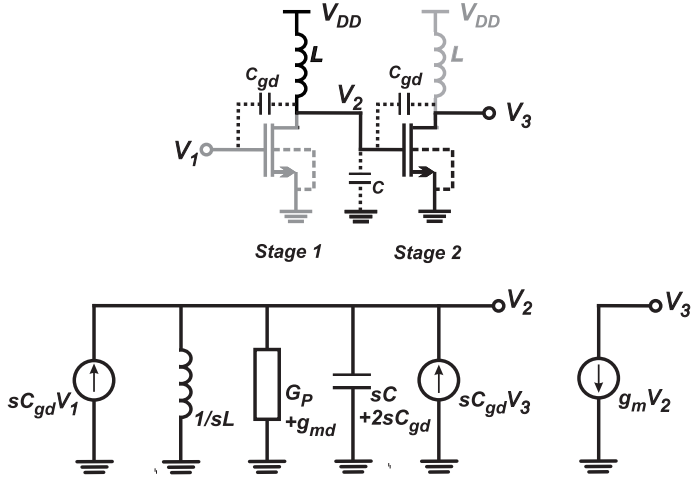


Figure 12: Single stage of the inductive ring oscillator and its corresponding small-signal model considering the effect of C_{gd}.

The phase shift ϕ between two adjacent stages of the ring oscillator is given by $\phi = 2k\pi/N$, where N is the number of stages and k is an integer. Since the node voltages in Fig. 12 are related as $V_2 = V_1 e^{j\phi}$ and $V_3 = V_2 e^{j\phi}$, the small-signal circuit in Fig. 12 can be redrawn as shown in Fig. 13

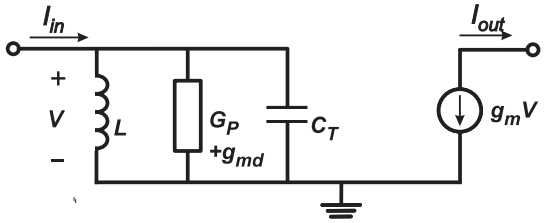


Figure 13: Small-signal model equivalent to a single stage of the inductive ring oscillator considering the effect of C_{gd}.

where C_T is given by

$$C_T = C + 2C_{gd} - C_{gd}(e^{j\phi} + e^{-j\phi}) = C + 2C_{gd}(1 - \cos\phi) \tag{2.12}$$

Thus, the transfer function of the single stage in Fig. 13 is calculated as

$$\frac{I_{out}}{I_{in}} = -\frac{g_m}{g_{md} + G_P + \frac{1}{sL} + sC_T} \tag{2.13}$$

It is worth noting that, with the exception of the value for the capacitance, (2.13) is identical to (2.1). In this case, the resonant frequency ω_0 is given by

$$\omega_0^2 LC_T = 1 \tag{2.14}$$

The value of C_T, which is dependent on the phase shift between the stages, calculated from (2.12), is shown in Table 2. As can be seen, for an even number of stages $\phi = \pi$ and thus $C_T = C + 4C_{gd}$.

Table 2: Equivalent capacitance C_T calculated according to the number of stages of the IRO.

N	ϕ	C_T
2	π	$C + 4C_{gd}$
3	$2\pi/3$	$C + 3C_{gd}$
4	π	$C + 4C_{gd}$
5	$4\pi/5$	$C + 3.62C_{gd}$
6	π	$C + 4C_{gd}$
7	$6\pi/7$	$C + 3.8C_{gd}$

2.1.2 Simulation of the IRO Topology

In order to verify the analysis presented above, steady-state simulations with the IRO considering several numbers of stages, were performed using the Cadence Spectre simulator and the parameters of the IBM 130 nm technology. Each stage was built from the same zero-VT transistor with $W/L = 250\ \mu$m$/0.42\ \mu$m and an inductor with $L = 100$ nH and $Q \approx 8$ at 500 MHz, both available in this technology. The waveform at the gate terminal of each stage of the topology of

Fig. 8, for N ranging from 2 to 5 is shown in Fig. 14. As expected, the phase shifts for an IRO oscillator with 2, 3, 4, and 5 stages were π, $2\pi/3$, π, and $4\pi/5$, respectively. For the figure, each arrangement was simulated for $V_{DD} = V_{DD,min}$.

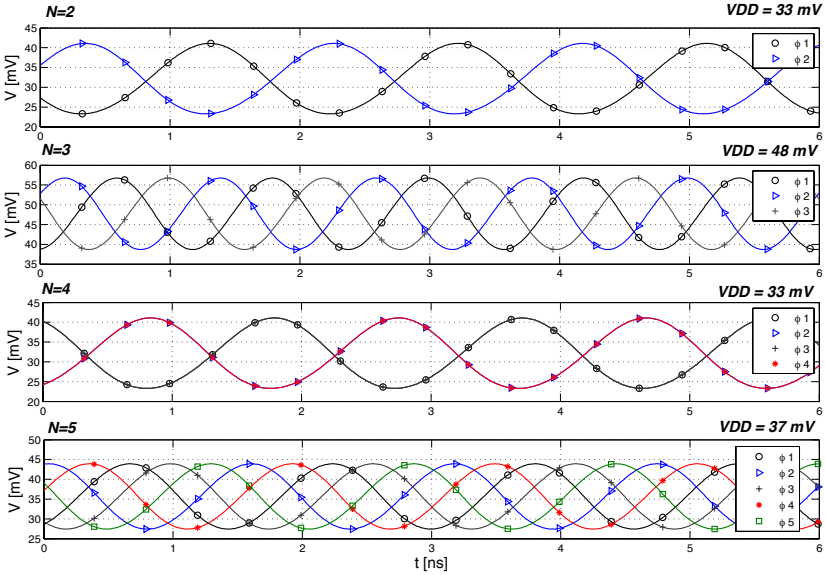


Figure 14: Simulated voltage waveforms at the gate terminal of each stage of the IRO for N = 2, 3, 4, and 5.

A comparison between the simulated and calculated oscillation frequencies (equation (2.14)) and minimum V_{DD} (equation (2.10)) is shown in Table 3. For the calculations, the transistor parameters I_S, n, and g_{md} were simulated following the procedure in Appendix B. The transistor capacitances $C = C_{gs}+C_{gb}+C_{db}+C_{jd}$ and C_{gd} were extracted via the dc operational point simulation. The peak-to-peak amplitude (V_{PP}) was simulated at V_{DD}=50 mV.

As can be seen in Table 3 the minimum V_{DD} is obtained for an even number of stages (with $\phi = \pi$). Additionally, for an even N, the circuit will oscillate at the lowest frequency. The dependence of the minimum supply voltage on the number of stages is illustrated in Fig. 15.

Table 3: Comparison between the simulated and calculated oscillation frequency (equation (2.14)) and minimum V_{DD} (equation (2.10)). The oscillation frequency was simulated for $V_{DD} = V_{DD,min}$.

N	ϕ	f_{osc}		$V_{DD,min}$		V_{PP}^{*}
		simulated	calculated	simulated	calculated	simulated
2	π	522 MHz	595 MHz	33 mV	29 mV	106 mV
3	$2\pi/3$	835 MHz	1 GHz	48 mV	44 mV	18 mV
4	π	522 MHz	595 MHz	33 mV	29 mV	106 mV
5	$4\pi/5$	638 MHz	748 MHz	37 mV	32.3 mV	79 mV
6	π	522 MHz	595 MHz	33 mV	29 mV	106 mV
7	$6\pi/7$	595 MHz	687 MHz	35 mV	30 mV	90 mV

*V_{PP} simulated at V_{DD} = 50 mV.

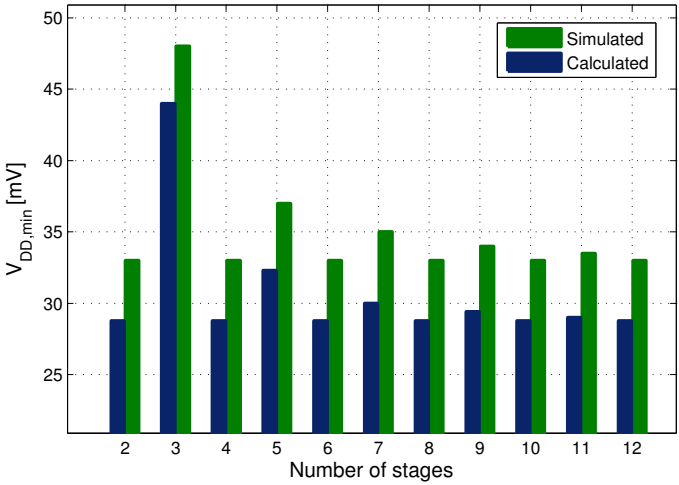


Figure 15: Calculated and simulated $V_{DD,min}$ *vs.* number of stages of the IRO using a 130 nm technology.

2.2 THE ENHANCED SWING RING OSCILLATOR - ESRO

A variation in the IRO topology able to reduce further the $V_{DD,min}$ is the enhanced swing ring oscillator (ESRO) shown in Fig. 16

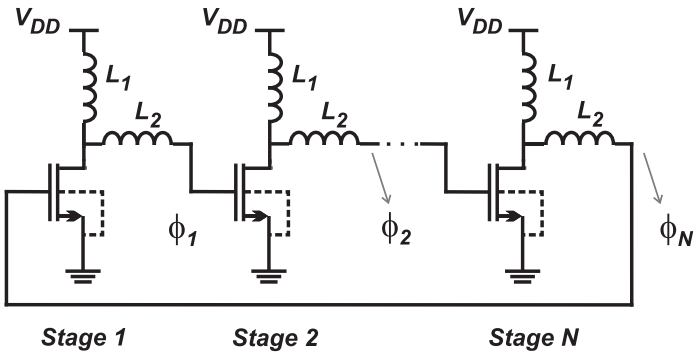


Figure 16: Schematic diagram of an N-stage enhanced swing ring oscillator (ESRO).

[35], [36] . Due to the inclusion of a second inductor L_2 between each stage, the ESRO can extend the oscillation amplitude far beyond the supply voltage, even operating with extremely low supply voltages.

The simplified small-signal equivalent circuit of a single stage of the ESRO is shown in Fig. 17, where R_{S2} represents the series resistance of inductor L_2, G_{P1} is the parallel conductance of L_1 and the other symbols have the same meaning as in Fig. 9. In order to simplify the mathematics, we have not taken into account the transistor capacitances C_{gd} and C_{gs}. However, according to the applications they can be considered.

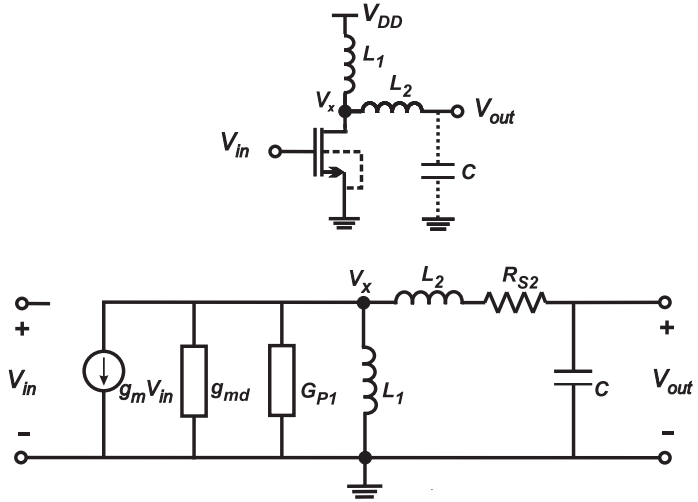


Figure 17: Simplified small-signal model of a single stage of the ESRO.

2.2.1 Analysis

The transfer function of the single stage in Fig. 17 is

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{sC + \left(g_{md} + G_{P1} + \frac{1}{sL_1}\right)(L_2Cs^2 + R_{S2}Cs + 1)} \tag{2.15}$$

which, for $s = j\omega$, becomes

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{(g_{md} + G_{P1})(1 - L_2C\omega^2) + \frac{R_{S2}C}{L_1}} \frac{1}{1 + j\left(\frac{[L_1+L_2+L_1R_{S2}(g_{md}+G_{P1})]C\omega^2-1}{(g_{md}+G_{P1})\omega L_1\left(1-L_2C\omega^2\right)+R_{S2}C\omega}\right)} \tag{2.16}$$

The condition of loop gain equal to unity for oscillation requires the phase shift ϕ between two contiguous stages to be $\phi = 2k/N$, where N is the number of stages and k is an integer. Similarly to the IRO topology, the circuit will oscillate at the frequency for which the voltage gain is the highest, although more than one value for the phase shift satisfies the phase condition required for oscillation, as shown in Fig. 18. As for the first ring arrangement, for an even number of stages, the phase shift for oscillation is $\phi = \pi$, while for an odd number of stages $\phi = (N-1)\pi/N$. Thus, once the number of oscillator stages has been decided upon, the phase-shift between two contiguous stages of the oscillator is found.

As can be seen in Fig 18, the minimum gain for starting up the oscillator can be obtained for a phase shift ϕ which differs from π, as is the case of the IRO topology for an even number of stages. This is due to the inclusion of a second inductor L_2 between two contiguous stages.

2.2.1.1 Frequency of Oscillation

The phase shift ϕ between V_{out} and V_{in} calculated from (2.16) is

$$\phi = \pi - \tan^{-1}\left(\frac{[L_1 + L_2 + L_1R_{S2}(g_{md} + G_{P1})]C\omega^2 - 1}{(g_{md} + G_{P1})\omega L_1(1 - L_2C\omega^2) + R_{S2}C\omega}\right) \tag{2.17}$$

From (2.17), considering the case of a ring oscillator with an even number of stages ($\phi = \pi$), the oscillation frequency ω can be calcu-

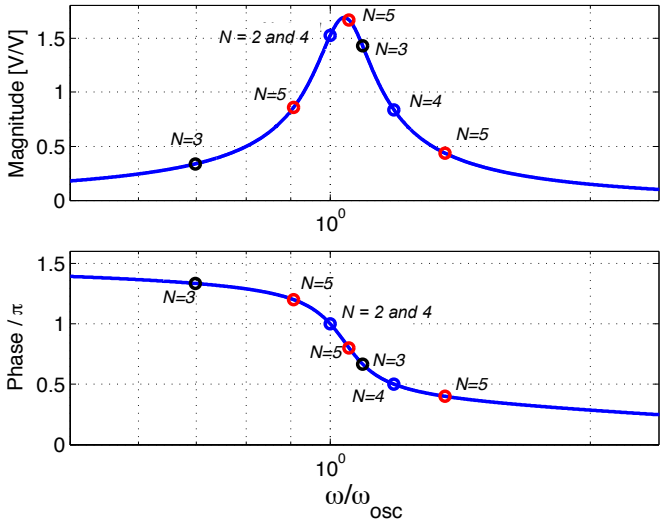


Figure 18: Magnitude and phase of the transfer function of a single stage of the ESRO. Frequency normalized by (2.18).

lated as

$$\omega = \frac{1}{\sqrt{[L_1 + L_2 + L_1 R_{S2}(g_{md} + G_{P1})]C}} \tag{2.18}$$

which, for lossless inductors, reduces to

$$\omega = \frac{1}{\sqrt{(L_1 + L_2)C}} \tag{2.19}$$

2.2.1.2 Minimum Transistor Gain Required for Oscillation Start-up

From (2.16), the greater-than-unity gain required to start up oscillations is achieved for

$$g_m > \left[(g_{md} + G_{P1})\left(1 - L_2 C\omega^2\right) + \frac{R_{S2}C}{L_1}\right]\sqrt{1 + (\tan\phi)^2} \tag{2.20}$$

since $g_m = (g_{ms} - g_{md})/n$ (see Appendix A), (2.20) can be rewritten as

$$\frac{g_{ms}}{g_{md}} > 1 + n\left[\left(1 + \frac{G_{P1}}{g_{md}}\right)\left(1 - L_2 C\omega^2\right) + \frac{R_{S2}C}{L_1 g_{md}}\right]\sqrt{1 + (\tan\phi)^2} \qquad (2.21)$$

Rewriting the inductor losses of L_2 as a parallel conductance G_{P2} and assuming that the inductor Q is high and that the resonant frequency can be approximated by (2.19), the transistor gain required for oscillation (equation (2.21)) can be written as

$$\frac{g_{ms}}{g_{md}} > 1 + n\left[\left(1 + \frac{G_{P1}}{g_{md}}\right)\frac{1}{1 + K_L} + \frac{G_{P2}}{g_{md}}\frac{K_L^2}{1 + K_L}\right]\sqrt{1 + (\tan\phi)^2} \qquad (2.22)$$

where $K_L = L_2/L_1$.

The curves in Fig. 19 represent the minimum gain g_{ms}/g_{md} calculated from (2.22) for the case in which the quality factors of the inductors are equal, *i.e.* $G_{P1}/G_{P2} = L_2/L_1$, $n = 1$, and the practical case of an even number of stages ($\phi = \pi$). As is clear from Fig. 19, there is an optimum value for the L_2/L_1 ratio that minimizes the ratio of the transconductances required for oscillation. The optimum value for L_2/L_1 that minimizes the right-hand side of (2.22), for $G_{P1}/G_{P2} = L_2/L_1$, is

$$K_{L,opt} = \frac{L_2}{L_1}\Big|_{opt} = \frac{1}{2}\left(\sqrt{1 + \frac{4g_{md}}{G_{P2}}} - 1\right) \qquad (2.23)$$

Using (2.23) to minimize the required gain g_{ms}/g_{md}, we find that

$$\frac{g_{ms}}{g_{md}}\Big|_{opt} = 1 + \frac{2n}{1 + K_{L,opt}} \qquad (2.24)$$

2.2.1.3 Minimum Supply Voltage Required for Oscillation Start-up

We follow the same procedure used for the IRO topology to calculate the minimum voltage. For each transistor we have the dc values $V_S = V_B = 0$ and $V_G = V_D = V_{DD}$. For a fixed g_{md}, the minimum $V_{DS}(= V_{DD})$ is reached combining the equation for the minimum g_{ms}/g_{md} ratio given in (2.21) and the expression for the drain-source

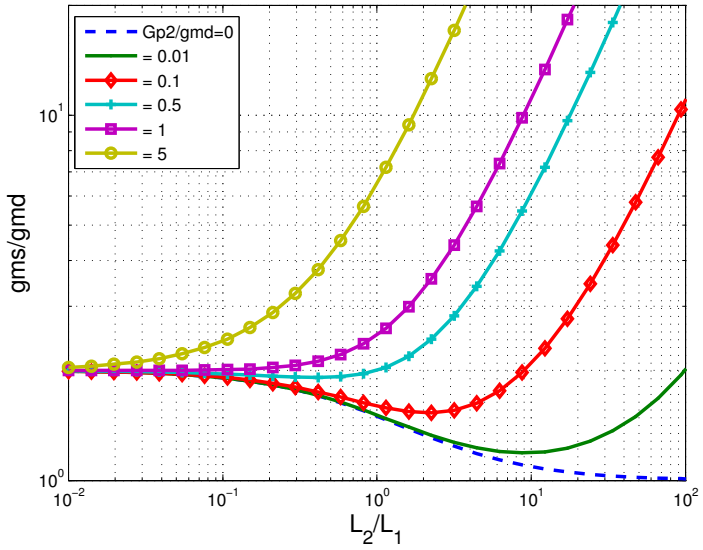


Figure 19: Minimum transistor intrinsic gain (to start up oscillations) versus L_2/L_1 ratio with G_{P2}/g_{md} as a parameter. The inductors are assumed to have equal quality factors.

voltage (V_{DS}) in Appendix A. Thus,

$$V_{DD} = \frac{\phi_t^2}{2I_S} n g_{md} \left[\left(1 + \frac{G_P}{g_{md}}\right)\left(1 - L_2 C\omega^2\right) + \frac{R_{S2}C}{L_1 g_{md}} \right] \sqrt{1 + (\tan\phi)^2} + \phi_t \ln\left\{ 1 + n\left[\left(1 + \frac{G_P}{g_{md}}\right)\left(1 - L_2 C\omega^2\right) + \frac{R_{S2}C}{L_1 g_{md}} \right] \sqrt{1 + (\tan\phi)^2} \right\} \quad (2.25)$$

For an even number of stages ($\phi = \pi$) (2.25) reduces to

$$V_{DD} = \frac{\phi_t^2}{2I_S} n g_{md} \left[\left(1 + \frac{G_P}{g_{md}}\right)\left(1 - L_2 C\omega^2\right) + \frac{R_{S2}C}{L_1 g_{md}} \right] + \phi_t \ln\left\{ 1 + n\left[\left(1 + \frac{G_P}{g_{md}}\right)\left(1 - L_2 C\omega^2\right) + \frac{R_{S2}C}{L_1 g_{md}} \right] \right\} \quad (2.26)$$

Finally, the limit for the minimum supply voltage of the ESRO topology can be calculated neglecting the losses in the inductors and assuming that the transistor operates in weak inversion and the reso-

nant frequency is approximated by (2.19), which yields

$$V_{DD,min} = \phi_t \ln\left(1 + n\frac{L_1}{L_1 + L_2}\right) \tag{2.27}$$

If $L_2 >> L_1$, the voltage gain of the transistor can be (much) lower than unity. Thus, for high values of L_2/L_1 the enhanced swing ring oscillator is capable of oscillating at supply voltages well below the thermal voltage, as experimentally verified in Chapter 3.

2.2.2 Simulation of the ESRO Topology

The steady-state simulation of the voltage at the gate terminal of each transistor of the ESRO topology for arrangements with $N = 2$, 3, 4, and 5 is shown in Fig. 20. In the simulation the devices are zero-VT transistors with $W/L = 1000\ \mu$m$/0.42\ \mu$m and inductors $L_1 = 22$ nH ($Q_1 \approx 11$ at 500 MHz) $L_2 = 100$ nH ($Q_2 \approx 8$ at 500 MHz), available in the IBM 130 nm technology. Each curve in Fig. 20 was obtained for $V_{DD} = V_{DD,min}$.

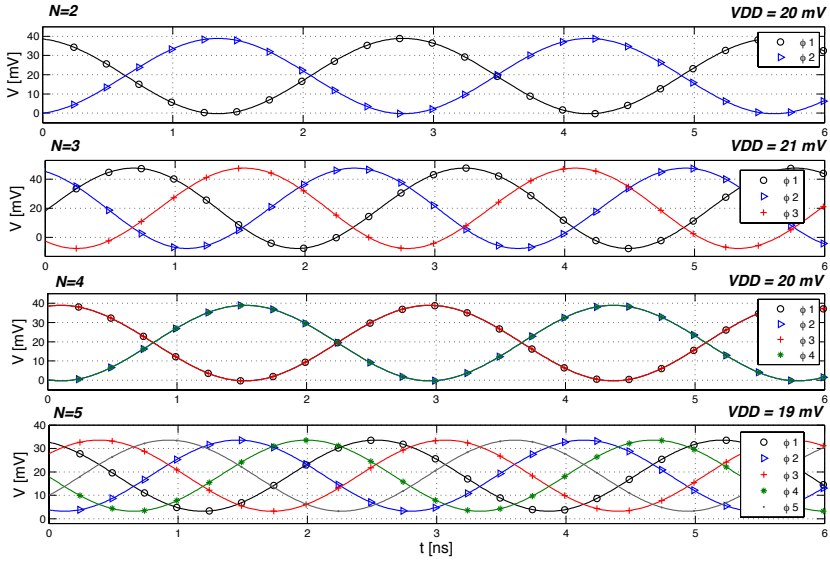


Figure 20: Simulated voltage waveforms at the gate terminal of each stage of the ESRO with $N = 2$, 3, 4, and 5.

Figure 21 shows the calculated values for the minimum supply voltage as a function of both the number of stages and the type of topology, IRO or ESRO, using the parameters of devices available in a 130 nm technology. The $V_{DD,min}$ value for the IRO was calculated from (2.10), while for the ESRO it was calculated from (2.25) The oscillation frequency of the ESRO was calculated from (2.17). For the IRO topology, zero-VT transistors with W/L = 250 μm/0.42 μm and L=100 nH ($Q \approx$8 at 500 MHz) were employed. For the ESRO, zero-VT transistors with W/L = 1000 μm/0.42 μm, L_1 = 22 nH ($Q_1 \approx 11$ at 500 MHz), and L_2 = 100 nH ($Q_2 \approx 8$ at 500 MHz) were used for the calculations. As can be readily noted, the ESRO is capable of starting up at a V_{DD} significantly lower than in the case of the IRO, but at the expense of an additional inductor per stage.

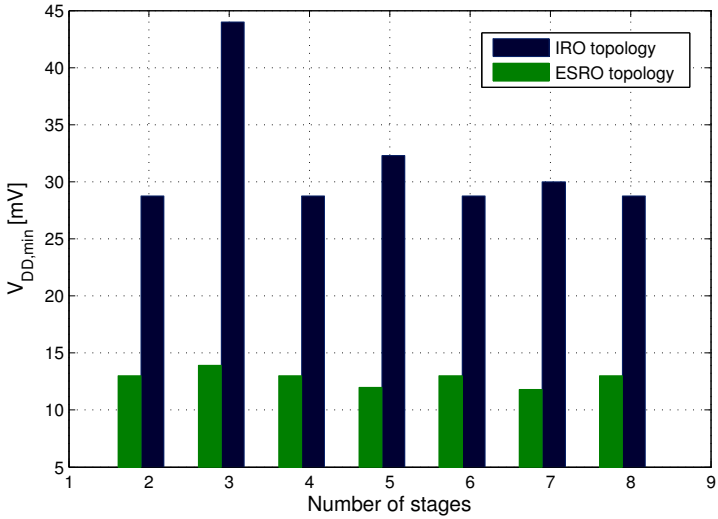


Figure 21: Calculated values for the minimum supply voltage for the starting up of the IRO and ESRO topologies versus number of stages.

2.2.3 The Effect of the Load on the Oscillating Frequency and Minimum Transistor Gain

For the sake of simplicity, the effect of the output load on the behavior of the ESRO is analyzed only for the two-stage ESRO shown

in Fig. 22 (a). It is worth noting that a two-stage ESRO is a cross-coupled oscillator that uses an inductive coupling inductor (L_2) between stages. Using the equivalent small-signal circuit of a single stage, as shown in Fig. 22 (b), the transfer function of a single stage considering the effect of the load is

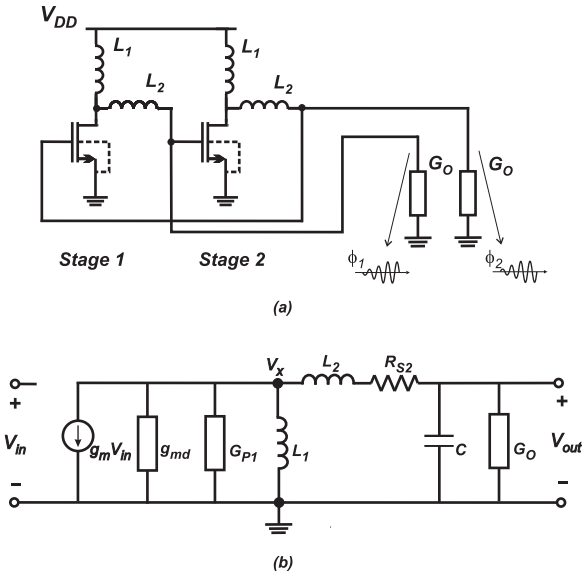


Figure 22: (a) Schematic diagram of the two-stage ESRO; (b) Simplified small-signal model of a single stage of the ESRO, with the load modeled as a conductance G_o.

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{\left(g_{md} + G_{P1} + \frac{1}{sL_1}\right)\left[(sC + G_o)(sL_2 + R_{s2}) + 1\right] + sC + G_o} \tag{2.28}$$

Following the same procedure adopted for calculating the oscillation frequency of the unloaded ESRO, and assuming $\phi = \pi$, the oscillation frequency is

$$\omega = \sqrt{\frac{G_o R_{S2} + 1}{(L_1 + L_2)C + L_1 (R_{S2} C + L_2 G_o)(g_{md} + G_{P1})}} \tag{2.29}$$

which reduces to

$$\omega = \sqrt{\frac{1}{(L_1 + L_2)C + L_1 L_2 G_o g_{md}}} \tag{2.30}$$

for negligible inductor losses. The greater-than-unity gain required for the starting up of the oscillations is achieved for

$$g_m > (g_{md} + G_{P1})\left(1 - L_2 C\omega^2 + G_o R_{S2}\right) + \frac{R_{S2}C}{L_1} + G_o\left(1 + \frac{L_2}{L_1}\right) \tag{2.31}$$

which can be written in terms of g_{ms} and g_{md} as

$$\frac{g_{ms}}{g_{md}} > 1 + \frac{n}{g_{md}}\left[(g_{md} + G_{P1})\left(1 - L_2 C\omega^2 + G_o R_{S2}\right) + \frac{R_{S2}C}{L_1} + G_o\left(1 + \frac{L_2}{L_1}\right)\right] \tag{2.32}$$

Finally, disregarding the inductor losses, assuming n=1 and substituting (2.30) into (2.32) we find the compact expression for the minimum transistor gain from

$$\frac{g_{ms}}{g_{md}} > 2 - \frac{L_2 C}{(L_1 + L_2)C + L_1 L_2 G_o g_{md}} + \frac{G_o}{g_{md}}\left(1 + \frac{L_2}{L_1}\right) \tag{2.33}$$

The effect of the output conductance G_o (which represents the load inserted by the stage following the oscillator) on both the oscillation frequency (equation (2.30)) and the minimum transistor gain (equation (2.33)) is shown in Fig. 23. Despite the strong influence of G_o on the minimum transistor gain required for oscillation, this effect can be reduced by increasing g_{md} through transistor widening.

2.3 THE ENHANCED SWING COLPITTS OSCILLADOR - ESCO

This section presents the analysis and discussion of a Colpitts oscillator valid for very low supply voltages. From the study on the previous ring oscillators it can be concluded that a good practice for ultra-low-voltage oscillators is the application of all the available voltage bias to the transistors and the boosting of the oscillation amplitude beyond the supply rails. For ULV applications, the conventional Colpitts oscillator illustrated in Fig. 24 presents some limitations, which will be discussed before analyzing the ESCO.

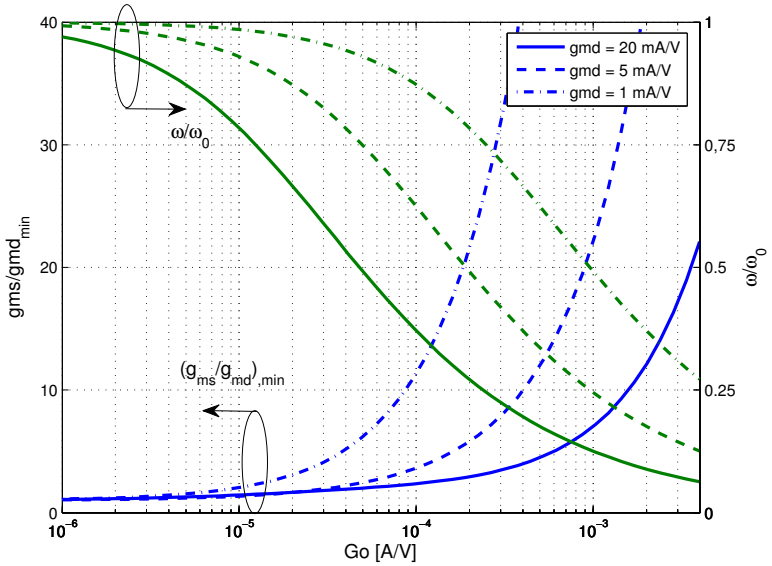


Figure 23: Calculated oscillation frequency (equation (2.30)) normalized to $\omega_0 = 1/\sqrt{(L_1 + L_2)C}$ and minimum transistor gain (equation (2.33)) in terms of the output conductance G_o. $L_1 = 9.5\ \mu$H, $L_2 = 950\ \mu$H (both with $Q = 80$) and $C = 3$ pF.

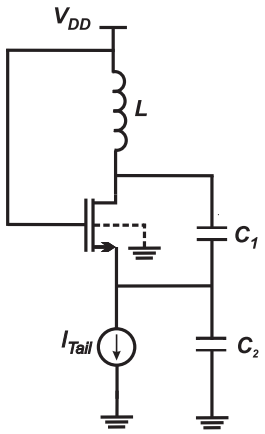


Figure 24: Conventional Colpitts oscillator.

When the voltage swing is large and the current source enters the triode region for a fraction of the period, the voltage drop across

the current source can be close to zero. Thus, the minimum voltage at the source and also at the drain clips around zero volts (ground level). Consequently, the maximum sinusoidal peak-to-peak voltage swing at the drain cannot exceed $2V_{DD}$ (supply-limited region), which is an important drawback of the Colpitts oscillator in Fig. 24.

In order to reduce the phase noise, in some studies the tail current source in Fig. 24 has been replaced by an inductor [41], [42], [43] and [44]. In [45], in addition to the inclusion of a second inductor, substrate bias is used in order to reduce the minimum V_{DD}.

In order to circumvent the limitations of the conventional Colpitts oscillator, the ESCO shown in Fig. 25 was used[43], [44]. This topology is capable of boosting the oscillation amplitude beyond the supply rails.

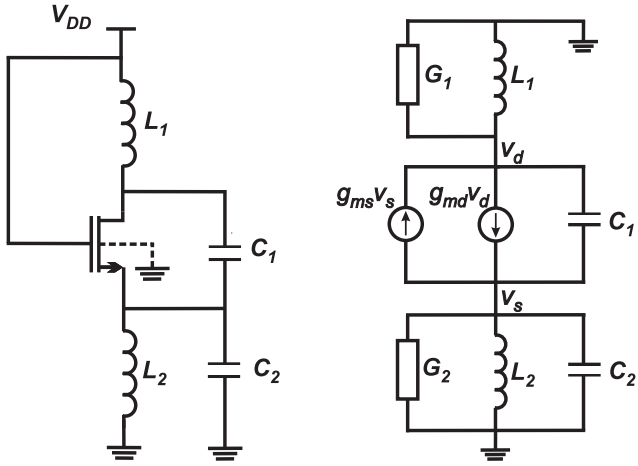


Figure 25: Schematic of the ESCO and its small-signal model.

2.3.1 Analysis

The small-signal model of the ESCO is shown in Fig. 25, where g_{ms} and g_{md} represent the source and drain transconductances. The transistor capacitance C_{gs} is absorbed in C_2. G_1 and G_2 model the losses of inductors L_1 and L_2, respectively.

2.3.1.1 Frequency of Oscillation

For the sake of simplicity, let us assume that the ESCO oscillation frequency is independent of both the losses and the transistor parameters. The oscillation frequency can be calculated (see Fig. 25) as the resonance frequency of the equivalent LC tank composed of the inductor L_1 and an equivalent capacitance C_{eq} given by

$$C_{eq} = \frac{C_1 C_2^{'}}{C_1 + C_2^{'}} \tag{2.34}$$

where

$$C_2^{'} = C_2 - \frac{1}{\omega^2 L_2} \tag{2.35}$$

is the capacitance equivalent to the L_2C_2–tank at the oscillation frequency ω, which is such that

$$\omega^2 L_1 C_{eq} = 1 \tag{2.36}$$

The value of the equivalent capacitance C_{eq} is found from (2.34), (2.35), and (2.36). After some algebra we have

$$C_{eq} = \frac{(C_1 + C_2)\,k_L + C_1 - \sqrt{[(C_1 + C_2)\,k_L - C_1]^2 + 4k_L C_1^2}}{2} \tag{2.37}$$

where $k_L = L_2/L_1$. In fact, two solutions can be found for the equivalent capacitance; however, only the lower capacitance, which is associated with the higher frequency of oscillation, is possible. The reason for this is that, for the lower oscillation frequency, the source and drain voltages are 180^o out-of-phase. Since the transistor voltage gain V_d/V_s is positive, the loop gain will be negative at the lower frequency; thus, the circuit cannot oscillate at the lower frequency. For the particular case of $L_1 = L_2$, (2.37) is simplified to

$$C_{eq} = C_1 + \frac{C_2}{2} - C_1\sqrt{1 + \left(\frac{C_2}{2C_1}\right)^2} \tag{2.38}$$

In order to find the requirements of the transistor parameters for oscillation, firstly, the voltage gain from drain to source will be

calculated.

2.3.1.2 Voltage Gain between Drain and Source Terminals

To calculate the common-gate voltage gain we can proceed as follows. Following an inspection of the small-signal equivalent circuit of Fig. 25 we obtain

$$-V_d(s)\left(G_1+\frac{1}{sL_1}\right)_{s=j\omega}=V_s(s)\left(G_2+\frac{1}{sL_2}+sC_2\right)_{s=j\omega} \tag{2.39}$$

where V_d and V_s are the small-signal voltages at the source and drain, respectively. Assuming that the Q values of the LC tanks are high at the frequency ω, the relationship between the source and drain voltages calculated from (2.39) is

$$\frac{V_d}{V_s}=a\cong-\frac{L_1}{L_2}\left(1-\omega^2L_2C_2\right)=\frac{C_2}{C_{eq}}-\frac{L_1}{L_2} \tag{2.40}$$

The value of a, calculated from (2.37) and (2.40), is given by

$$a=u+\sqrt{u^2+\frac{L_1}{L_2}} \tag{2.41}$$

where

$$u=\frac{C_1+C_2}{2C_1}-\frac{L_1/L_2}{2}=\frac{1}{2}\left(1+\frac{C_2}{C_1}-\frac{L_1}{L_2}\right) \tag{2.42}$$

The value of a in (2.41) is always greater than unity. Note that for $L_2\to\infty$ the value of a is

$$a_{L_2\to\infty}=1+\frac{C_2}{C_1} \tag{2.43}$$

which is the result for the conventional Colpitts oscillator. To achieve high swing with low supply voltages, the value of a must be relatively close to unity, *i.e.* $C_2/C_1 << 1$. In this case (2.41) can be approximated as

$$a_{C_2<<C_1}=1+\frac{C_2/C_1}{1+L_1/L_2} \tag{2.44}$$

Another interesting case is $L_1 = L_2$. In this case (2.41) reduces to

$$a_{L_1=L_2} = \frac{C_2}{2C_1} + \sqrt{1 + \left(\frac{C_2}{2C_1}\right)^2} \tag{2.45}$$

which, for small capacitive ratios, C_2/C_1, becomes

$$a_{L_1=L_2} \cong 1 + \frac{C_2}{2C_1} \tag{2.46}$$

A graphical interpretation of the voltage gain V_d/V_s can be obtained as follows. Disregarding the losses of the passive devices, the Kirchhoff's current law (KCL) for nodes V_d and V_s, leads to equations (2.47) and (2.48)

$$\frac{V_d}{V_s} = \frac{L_1}{L_2}\left(\omega^2 C_2 L_2 - 1\right) \tag{2.47}$$

$$\frac{V_d}{V_s} = 1 + \frac{C_2}{C_1}\left(1 - \frac{1}{\omega^2 C_2 L_2}\right) \tag{2.48}$$

These two equations, which give the relationship between the drain and source potentials in terms of the oscillation frequency ω, are shown in Fig. 26. As can be seen in the figure, for a specified L_1/L_2 ratio the curves intersect at two points. However, as stated at the beginning of this section, only the higher frequency, which results in a positive V_d/V_s ratio, is a valid solution.

Having calculated the value of a, in order to calculate the minimum transistor gain to start-up the oscillator, the circuit can be modeled as shown in Fig. 27 [46].

2.3.1.3 Minimum Transistor Gain Required for Oscillation Start-up

For the occurrence of oscillation, the transistor must be able to compensate the loss of the passive components. In other words, reflecting to the primary winding the conductance connected to the secondary winding in Fig. 27, the requirement for oscillation is written

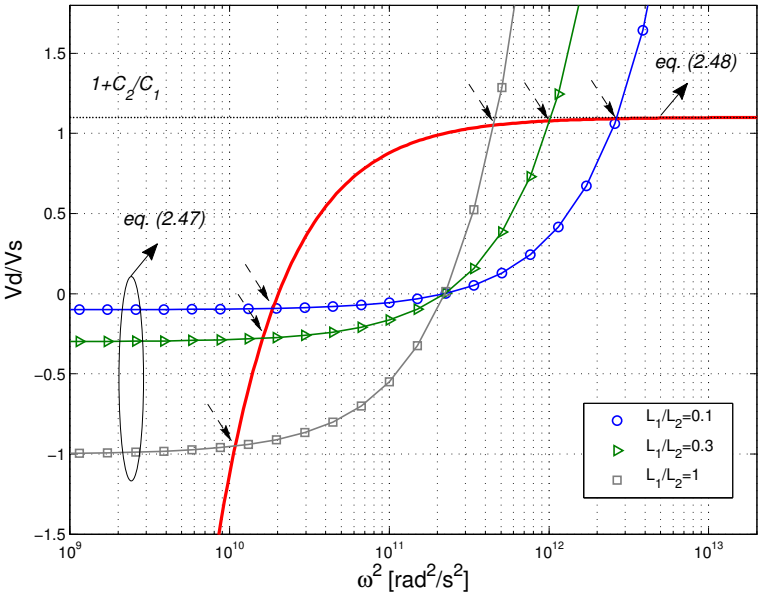


Figure 26: V_d/V_s ratio in terms of ω^2, for the cases where L_1/L_2 = 0.1, 0.3, and 1, with C_2/C_1=0.1.

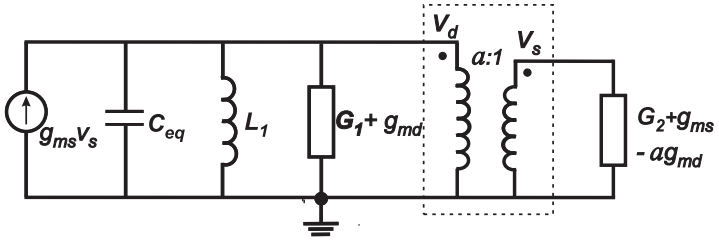


Figure 27: ESCO with capacitive divider modeled as a transformer

as

$$g_{ms}V_s = g_{ms}\frac{V_d}{a} > \left[G_1 + g_{md} + \frac{1}{a^2}(G_2 - ag_{md} + g_{ms})\right]V_d \qquad (2.49)$$

or equivalently

$$g_{ms} > ag_{md} + \frac{a^2 G_1}{(a-1)} + \frac{G_2}{(a-1)} \qquad (2.50)$$

From (2.50), the transistor gain g_{ms}/g_{md} can be calculated as

$$\frac{g_{ms}}{g_{md}} > a + \frac{a^2}{(a-1)}\frac{G_1}{g_{md}} + \frac{1}{(a-1)}\frac{G_2}{g_{md}} \tag{2.51}$$

The curves in Fig. 28 represent the minimum gain g_{ms}/g_{md} calculated from (2.51) for the case in which $G_1 = G_2 = G$.

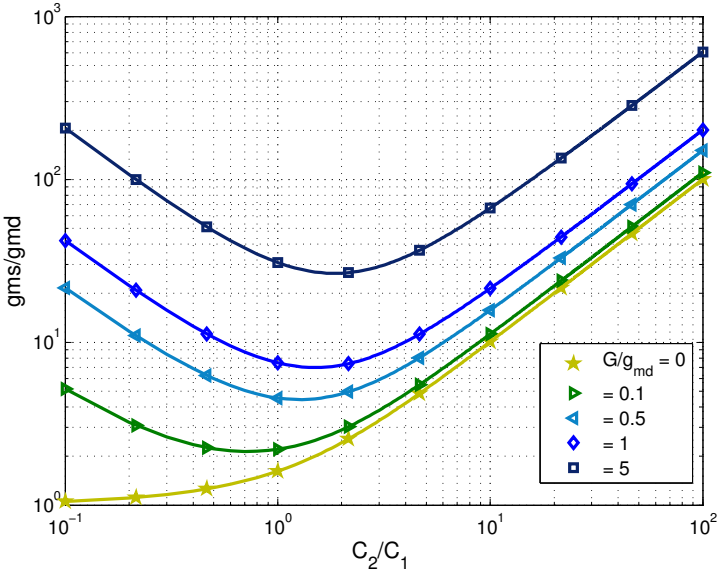


Figure 28: Minimum transistor intrinsic gain (to start up oscillations) versus C_2/C_1 ratio for $L_1 = L_2$, with G/g_{md} as a parameter.

As is clear from Fig. 28, there is an optimum value for the voltage gain a that minimizes the transconductance required for oscillation. The value a_{opt} that minimizes the right-hand side of (2.50) is

$$a_{opt} = 1 + \sqrt{\frac{G_1 + G_2}{G_1 + g_{md}}} \tag{2.52}$$

From (2.44) and (2.52), after selecting g_{md}, L_1 and L_2, the C_1/C_2 ratio can be determined, assuming that the quality factors of the in-

ductors are equal, *i.e.* $G_1/G_2 = L_2/L_1$, as

$$\frac{C_2}{C_1}|_{opt} = \left(1 + \frac{L_1}{L_2}\right)^{3/2} \sqrt{\frac{G_1/g_{md}}{1 + G_1/g_{md}}} \tag{2.53}$$

The substitution of (2.52) into (2.50) yields the optimized minimum value for the intrinsic gain

$$\frac{g_{ms}}{g_{md}} > 1 + 2\frac{G_1}{g_{md}} + 2\sqrt{\left(1 + \frac{L_1}{L_2}\right)\left(1 + \frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}} \tag{2.54}$$

From (2.54) it follows that the gain required for oscillation can be reduced for high values of g_{md} and low L_1/L_2 ratios.

Let us now consider some particular cases of interest. For the classical Colpitts oscillator, in which the transistor operates in saturation, G_2 and g_{md} can be neglected. Thus, (2.50) reduces to

$$g_{ms} > \frac{a^2 G_1}{(a-1)} \tag{2.55}$$

while (2.52) gives $a_{opt} = 2$. Consequently, the source transconductance necessary for oscillation is at least $4G_1$. Thus, the voltage gain g_{ms}/G_1 must be greater than 4 and, from (2.46), $C_1 = C_2$, which is the well-known result for the classical Colpitts oscillator [47]. In the hypothetical case of ideal inductors ($G_1 = G_2 = 0$) it follows from (2.50) that

$$\frac{g_{ms}}{g_{md}} > a \tag{2.56}$$

Thus, the open-loop gain (g_{ms}/g_{md} times $1/a$) must be greater than unity. It is important to note that g_{ms}/g_{md}, which is the intrinsic gain of the transistor operating in the common gate topology, is always greater than unity, as is shown in eq. (A.9) in Appendix A. For $C_2/C_1 << 1$, which is a practical implementation of the circuit, as will be demonstrated in the next chapter, it follows from (2.44) and (2.56) that

$$\frac{g_{ms}}{g_{md}} > a = 1 + \frac{C_2/C_1}{1 + L_1/L_2} \tag{2.57}$$

2.3.1.4 Minimum Supply Voltage Required for Oscillation Start-up

Assuming, as in the previous section, the dc values $V_S = V_B = 0$ and $V_G = V_D = V_{DD}$, for a fixed g_{md}, the minimum $V_{DS}(= V_{DD})$ is reached by combining the equation of the minimum transistor gain g_{ms}/g_{md} (equation (2.54)) and the expression for the drain-source voltage (V_{DS}) in Appendix A . Thus, for $G_1/G_2 = L_2/L_1$

$$V_{DD} = \frac{\phi_t^2}{2I_S} g_{md} \left(2\frac{G_1}{g_{md}} + 2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}} \right)$$
$$+\phi_t \ln\left(1 + 2\frac{G_1}{g_{md}} + 2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}} \right) \qquad (2.58)$$

For $C_2/C_1 << 1$, assuming, as in the previous section, that the MOSFET operates in the subthreshold region and neglecting the losses in the inductors, (2.44) and (2.58) can be combined to obtain the minimum supply voltage of the ESCO topology as

$$V_{DD,min} = \phi_t \ln(a) = \phi_t \ln\left(1 + \frac{C_2/C_1}{1 + L_1/L_2}\right) \qquad (2.59)$$

Theoretically, as (2.59) shows, the ESCO can oscillate at very low supply voltages. In practice, however, the unavoidable losses, the parasitic capacitance of the drain node and operation of the transistor in moderate or strong inversion will contribute to increasing the value of V_{DD} given by (2.59). Some simulated and experimental results for the minimum supply voltage, including losses and considering the transistor operation in moderate inversion, will be given in Section 3.

2.4 COMPARISON BETWEEN THE ULV TOPOLOGIES

In this chapter, the analysis of three oscillator topologies valid for the ultra-low-voltage operation was presented. The main results as well as some design characteristics are summarized in Table 4. Two of the topologies described, the enhanced swing Colpitts oscillator and the enhanced swing ring oscillator can operate with supply voltages below the thermal voltage. On the other hand, the inductive ring

oscillator is a very convenient topology for applications that require minimum dc voltages of the order of $2kT/q$ (two times the thermal voltage). The experimental and simulated results that verify the analysis developed in this section, are presented in the next chapter.

Table 4: Comparison between the IRO, ESRO and ESCO topologies.

	IRO	**ESRO**	**ESCO**
$^{*}V_{DD,min}/\phi_t$	$\ln(1+n)$	$\ln\left(1+\frac{nL_1}{L_1+L_2}\right)$	$\ln\left(1+\frac{C_2/C_1}{1+L_1/L_2}\right)$
$^{*}\omega_{osc}$	$1/\sqrt{LC}$	$1/\sqrt{C(L_1+L_2)}$	$1/\sqrt{C_{eq}L_1}$
Design optimization		$\frac{L_2}{L_1}\|_{opt} = \frac{1}{2}\left(\sqrt{1+\frac{4g_{md}}{G_P}}-1\right)$	$\frac{C_2}{C_1}\|_{opt} = \left(1+\frac{L_1}{L_2}\right)^{3/2}\sqrt{\frac{G_1/g_{md}}{1+G_1/g_{md}}}$
Design	Easiest:"ratio-less" design	Intermediate: L_1/L_2 ratio	Hardest: determine L_1/L_2 and C_2/C_1 ratios
Area	Intermediate, at least two inductors	Large, at least four inductors	Intermediate, two inductors and two capacitors

*Disregarding the inductor losses.

3 ULV OSCILLATORS - DESIGN AND EXPERIMENTATION

In order to validate the analysis of the ULV oscillators introduced in Chapter 2, this chapter presents the design and experimentation associated with the ESCO, IRO and ESRO topologies. To explore the practical minimum values for the supply voltage of oscillators, fully-integrated circuits as well as circuits using off-the-shelf devices, were implemented.

Due to their remarkable characteristics in relation to ULV circuits (see Section 1.2), all oscillators were designed with zero-VT transistors. Two types of transistors were employed, the off-the-shelf ALD1800A and the zero-VT transistor available in the IBM 130nm 8RF-DM integrated technology. This fabrication process, besides providing the active devices, allows the implementation of high quality passive devices.

3.1 DESIGN OF THE ENHANCED SWING COLPITTS OSCILLATOR - ESCO

In this section, two versions of the enhanced swing Colpitts oscillator are presented, a discrete version, using off-the-shelf inductors and capacitors, and a fully-integrated version.

3.1.1 Design of the ESCO using Off-the-Shelf Components

In order to demonstrate the feasibility of the operation of the ESCO with supply voltages under kT/q, an oscillator using off-the-shelf devices with high quality inductors and capacitors was implemented. In the first attempt, the ESCO was designed with ALD1800A [48], zero-VT transistors which cost a couple of dollars per device. In order to increase the transistor gain, the first prototype was built with a parallel association of 24 transistors, as shown in Fig. 29 (a) and started up from around 20 mV of supply voltage. However, due to the lower drive capability of the association compared with the transistor available in the 130 nm integrated process (as can be seen in Table 16 in Appendix B), and the high values of the intrinsic capacitances, it seemed appropriate to build a second prototype around customized transistors with large W/L in 130 nm technology.

Thus, the ESCO prototype shown in Fig. 29 (b) with a zero-VT

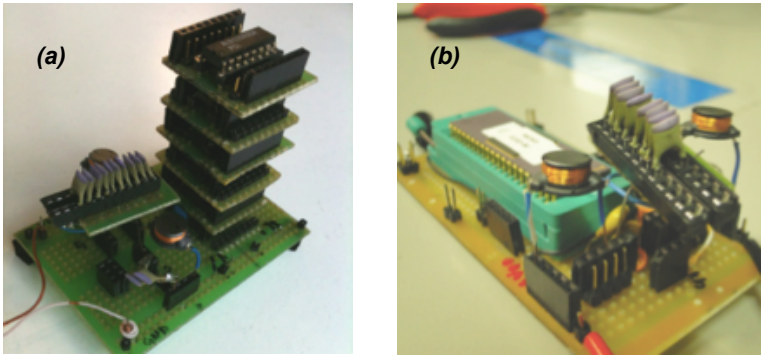


Figure 29: Photograph of the discrete ESCO prototypes: (a) built with off-the-shelf zero-VT transistor; (b) built with a customized zero-VT transistor in the 130 nm technology.

transistor in 0.13 μm CMOS technology with W/L=500x5 μm/0.42 μm was built. The main transistor parameters are shown in Appendix B.5. The oscillator circuit, together with the values for the components employed in the experiment, is shown in Fig. 30. The nominal inductances chosen were both equal to 10 mH with quality factors of around 90. Using equation (2.38) with $C_1 >> C_2$ the approximate value for C_2 was found ($\approx$ 440 pF) which provides an oscillation frequency of around 110 kHz. For the experiment, we employed nominal values of 3.6, 2.0, 1.8, and 1.54 nF for C_1. Transistor capacitances, measured for $V_G = V_D$ =20 mV and V_S=0, are negligible when compared with C_1 and C_2. The quality factors of the capacitors are around than 2,000. Passive devices were characterized at 100 kHz and their values, along with the parasitic losses, are given in Fig. 30.

With C_1 = 1.54 nF, the prototype shown in Fig. 30 oscillates at around 108 kHz. The experimental waveform of the drain voltage is shown in Fig. 31 for V_{DD}= 15 mV.

Circuit simulations were run for the ESCO in order to find the minimum supply voltage required for sustained oscillations. The values for the components are those shown in Fig. 30, except for C_1 and C_2, whose values were chosen so as to keep an oscillation frequency of the order of 110 kHz for a given C_2/C_1 ratio. The quality factor of the capacitors was around 2,000. The MOS transistor, previously described in this text, was the same for all simulations.

Figure 32 shows the simulation results for the minimum supply voltage of the ESCO required to ensure sustained oscillations. Note that, in this particular case, the losses of the passive components do

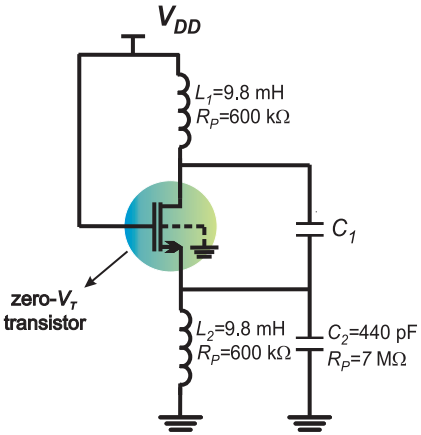


Figure 30: Schematic of the ESCO with values for the passive components characterized at 100 kHz. Values for C_1 are given in the text.

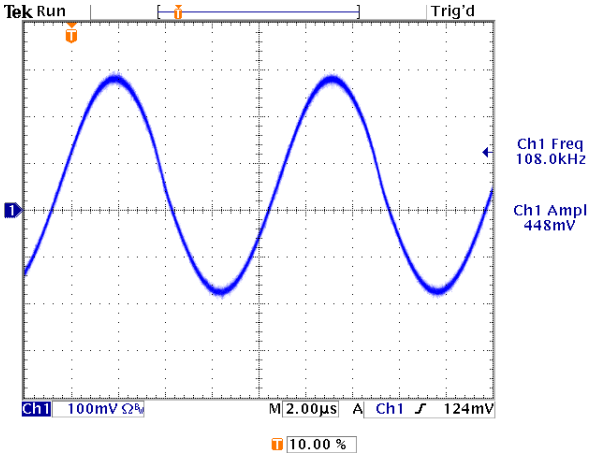


Figure 31: Experimental drain voltage of the ESCO of Fig. 30 for V_{DD}= 15 mV, C_1 =1.54 nF, C_2 =0.44 nF and temperature around 23°C.

not play an important role, except for very low C_2/C_1 ratios, below approximately 10^{-2}. Four experimental values, C_2/C_1=0.12, 0.22, 0.25, and 0.29, represented by triangle symbols, show acceptable agreement with the simulation results. Note that for C_2/C_1=0.12 circuit oscillations in the circuit prototype were sustained at a supply voltage of only 15 mV, with the simulation indicating a supply voltage of 8 mV. The dotted line indicates the theoretical limit for operation in weak inversion.

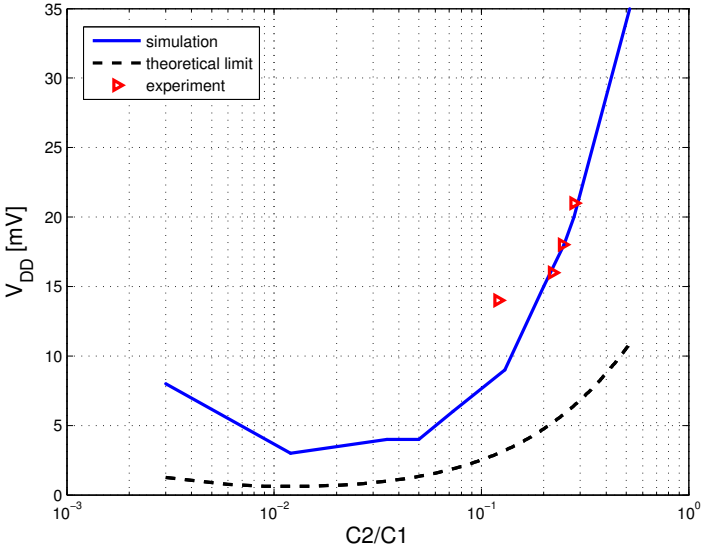


Figure 32: Minimum supply voltage for sustained oscillations versus C_2/C_1 of the ESCO in Fig. 30. Details for the values of C_1 and C_2 are given in the text.

Figure 33 illustrates the variation in the amplitude of the drain voltage in terms of the supply voltage. The curves represent the measured and simulated values and their close proximity can be observed.

The capability of the circuit to generate oscillations when powered by a thermoelectric generator attached to a human body was verified, as can be seen in Fig. 34. Using the prototype shown in Fig. 29 (a), built with the zero-VT transistor ALD1108A and with C_1 =2.6 nF, C_2 =520 pF and $L_1 = L_2$ =9.8 mH, the circuit oscillates at a dc voltage of 22 mV delivered by the thermoelectric generator [49] at a room temperature of 24°C.

3.1.2 Design of the Fully-Integrated ESCO

Based on the analysis presented in Chapter 2, a Colpitts oscillator was designed for operation at 800 MHz. High-quality integrated inductors (Q>10), with the inductances indicated in Fig. 35, were used. The oscillator employs a wide zero-VT transistor (W/L=300x5 μm/420 nm) to provide enough drive capability to compensate for the

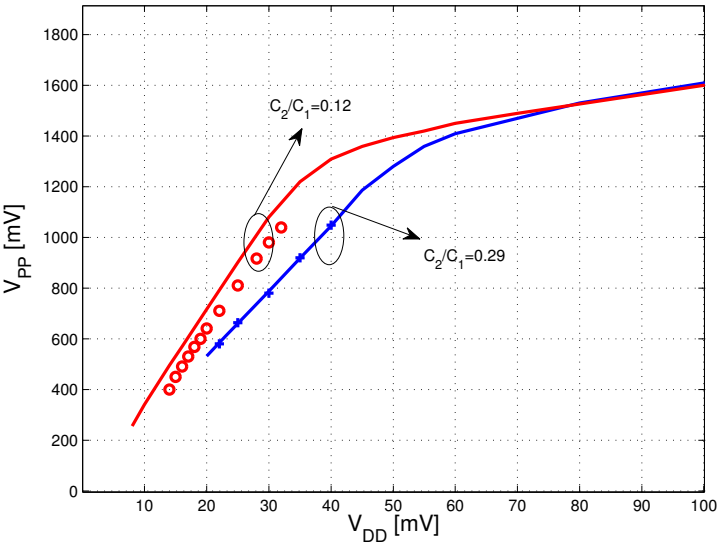


Figure 33: Simulated (solid lines) and experimental (symbols) peak-to-peak drain voltage versus supply voltage for $C_2/C_1 = 0.29$ and 0.12.

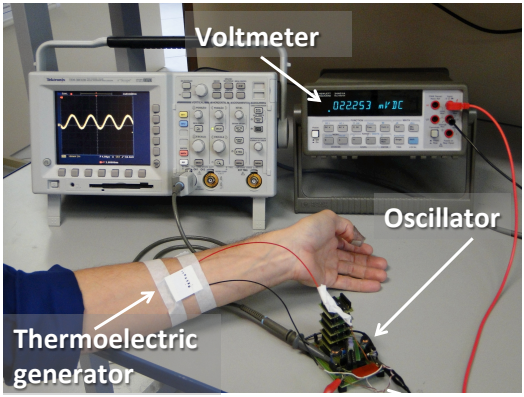


Figure 34: Photograph of the ESCO powered by a thermoelectric generator for $T \approx 24°C$.

inductor losses.

Once the inductors and transistor parameters are known, the capacitive feedback can be readily determined from (2.53), which, in

this design, yields an optimum capacitive ratio ≈ 0.7. From (2.36) and (2.37), after some adjustment to account for parasitic capacitances due to the layout, C_1 and C_2 values of 6 pF and 3.5 pF, respectively, were selected.

A schematic diagram of the oscillator and the voltage buffer is shown in Fig. 35. A tapered inverter chain was chosen for the buffer since it presents a small capacitive load to the oscillator. In Fig. 35 the inductor parameters (simulated at 800 MHz) and the MOSFET capacitances, extracted from Cadence EDA tools, are indicated. The layout of the circuit as well as the microphotograph of the chip implemented in the IBM 130 nm technology is shown in Fig. 36.

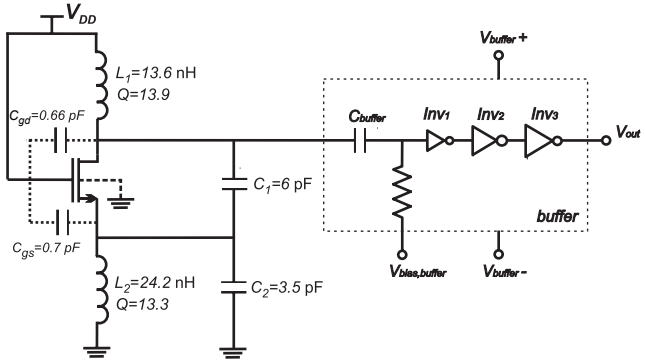


Figure 35: Schematic diagram of the fully-integrated ESCO design and the voltage buffer. Inductors were simulated at 800 MHz.

The setup used to test the oscillator is shown in Fig. 37. As can be seen in this figure, the circuit can oscillate at below 100 mV of supply voltage, starting up from around 86 mV, while the calculation based on (2.58) gives a minimum supply voltage of 56 mV. The main results obtained with the fully-integrated ESCO are summarized in Table 5. The calculated values were taken from the simulated parameters detailed in Fig. 35, without taking into account the parasitic elements due to the layout. The spectrum for the oscillator biased at V_{DD}=86 mV is shown in Fig. 38.

3.2 DESIGN OF THE INDUCTIVE RING OSCILLATOR - IRO

This section presents two fully-integrated versions of the inductive ring oscillator with seven and two stages, oscillating from 53 mV and 46 mV of supply voltage, respectively. Both circuits were imple-

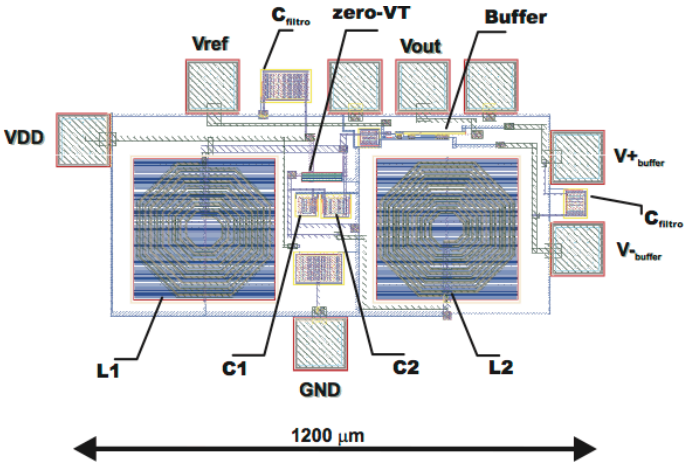


Figure 36: (a) Layout and (b) micrograph of the fully-integrated ESCO built in the IBM 130 nm technology.

Table 5: Summary of the main results obtained for the fully-integrated ESCO.

	Calculated	Simulated (post layout)	Experimental
f_{osc}	850 MHz	715 MHz	700 MHz
$V_{DD,min}$	56 mV	50 mV	86 mV

mented in the IBM 130 nm process.

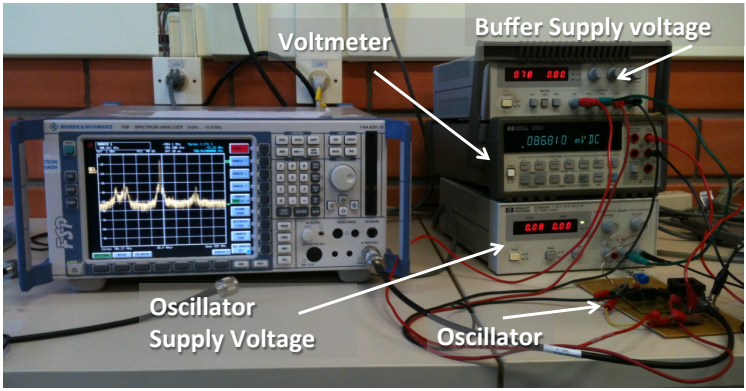


Figure 37: Setup used to test the fully-integrated ESCO.

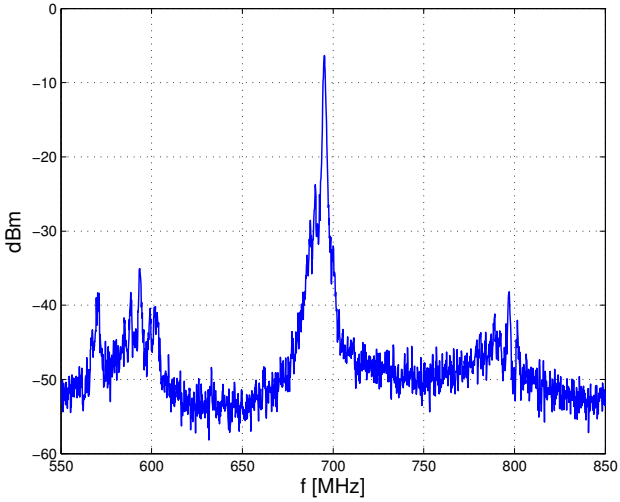


Figure 38: Experimental spectral diagram of the fully-integrated ESCO operating with V_{DD} = 86 mV.

3.2.1 Design of the Fully-Integrated Seven-Stage IRO

At the beginning of this study, in order to demonstrate the influence of the number of stages on the minimum supply voltage required for start-up and on the oscillation frequency, a seven-stage IRO using

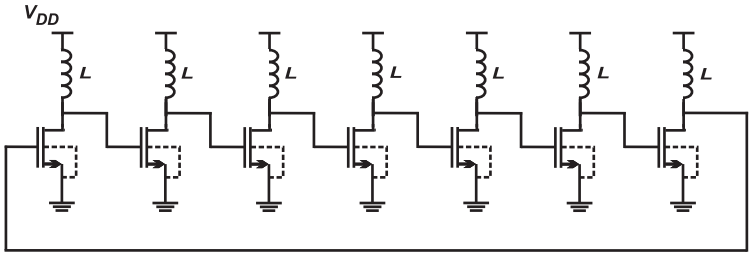


Figure 39: Schematic diagram of the seven-stage inductive ring oscillator.

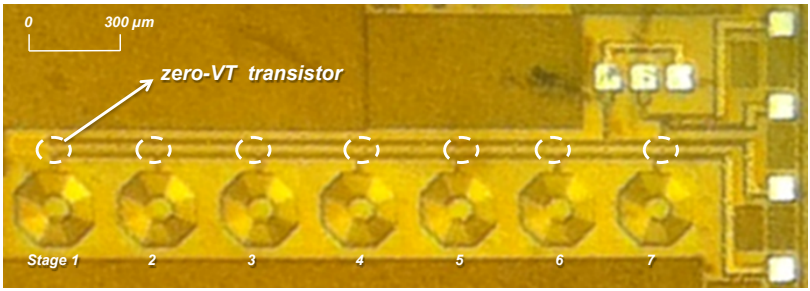


Figure 40: Micrograph of the seven-stage inductive ring oscillator in the 130 nm technology.

zero-VT transistors and inductors in the IBM 130 nm technology was designed. The schematic diagram and the layout are shown in Figs. 39 and 40, respectively.

A summary of the characteristics of the zero-VT transistor (W/L=30x5 μm/480 nm) and the inductor used in the oscillator are given in Table 6. The inductor was chosen so that the G_P value was as low as possible within the expected frequency range (500 to 800 MHz). In Table 6, V_T and g_{md} were obtained experimentally employing the procedures shown in Appendix B whereas the other parameters (capacitances and inductances) were taken from the simulator.

Using the values shown in Table 6, the oscillation frequency calculated from (2.5) is around 1 GHz, against 730 MHz obtained using the simulator. In fact, the parasitic capacitances introduced by the layout contributed to reducing the oscillation frequency to around 550 MHz, as the experimental spectral diagram in Fig. 41 shows. The minimum voltage required to start up the oscillator obtained with the experimental prototype was around 53 mV, against 50 mV calculated using (2.10) and the values in Table 6.

Table 6: Main characteristics of the inductor (at 550 MHz) and transistor (V_{DD}=40 mV) used in the integrated inductive ring oscillator.

Transistor		Inductor
g^*_{md} = 2.3 mA/V	C = 130 pF	L = 100 nH
V^*_T = 22 mV	C_{gd} = 70 pF	G_P = 0.3 mA/V

* Value obtained experimentally.

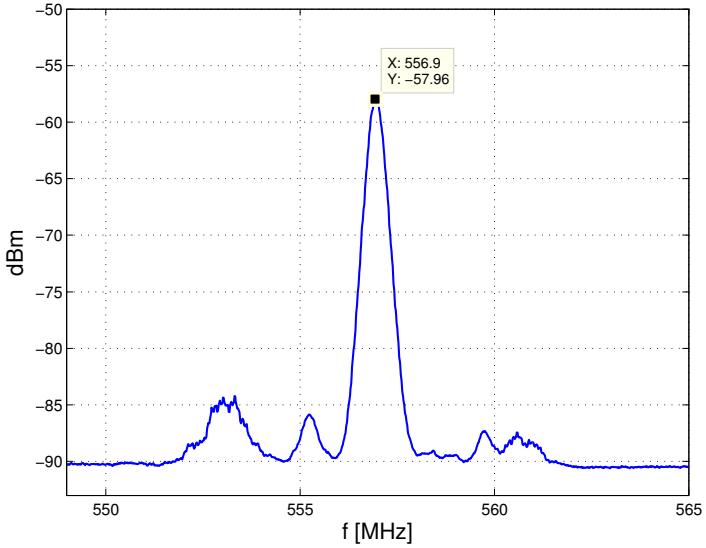


Figure 41: Spectral diagram of the seven-stage inductive ring oscillator, obtained experimentally for V_{DD}=70 mV.

In order to investigate the experimental variation in the output voltage magnitude with a variation in the supply voltage, both the experimental and simulation results were plotted in Fig. 42. Note that the output voltage is normalized to its value at a supply voltage of 100 mV. In order to measure the oscillator output by an instrument with an input impedance of 50 Ω, a voltage buffer composed by a triple-well transistor configured as a common-source was used. The absolute value of the oscillation amplitude can be seen in the next section (for the two-stage IRO design).

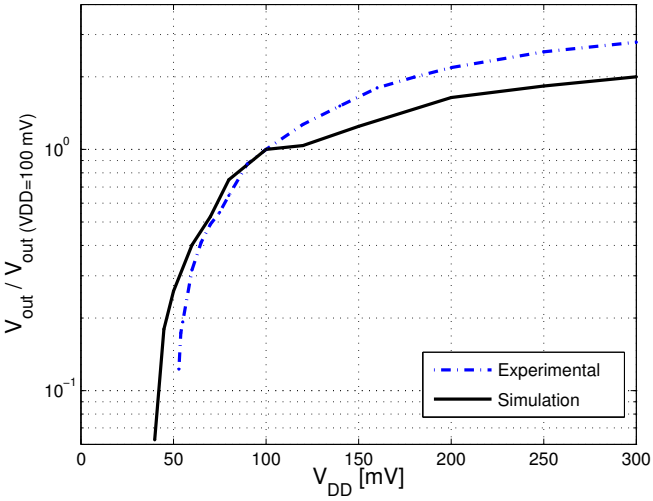


Figure 42: Normalized output voltage of the fully-integrated seven-stage inductive oscillator *vs.* supply voltage.

3.2.2 Design of the Fully-Integrated Two-Stage IRO

Based on the analysis presented in Chapter 2, a two-stage IRO that operates with supply voltages of less than 50 mV was designed. According to (2.8), the supply voltage is minimized when the phase shift between contiguous stages of the oscillator is equal (or close) to π. Such a phase shift can be obtained with either an even number of stages or an odd number of stages greater than 5, e.g., the seven-stage IRO described in Section 3.2.1. From (2.10), one can see that the minimum supply voltage has a strong dependence on the inductor losses. Thus, a high-Q ($Q \approx 8$) inductor at the oscillation frequency, approximately 500 MHz, was chosen. It is then possible to calculate (or determine through simulation) the W/L ratio of the zero-VT transistor to achieve the required capacitance for the specified oscillation frequency. The characteristics of both the transistor and the inductor used in each stage of the IRO are summarized in Table 7. Differences between the simulated and experimental values for the DC current at V_{DD}=50 mV are mainly attributed to the difference between the nominal and practical values for the threshold voltage.

Figure 43 shows the micrograph of the fully integrated two-

Table 7: Summary of device characteristics and the main simulated and experimental results for the fully integrated two-stage IRO.

Simulated Device Characteristics		**IRO results**	
Transistor	Inductor	Simulated	Experimental
W/L=30x6μm/0.42μm	L=108 nH	$V_{DD,min}$=38 mV	$V_{DD,min}$=46 mV
V_T=53 mV	Q=7.9	f_{osc}=467 MHz	f_{osc}=410 MHz
I_S=75 μA	f_{res}=1.1 GHz	I_{DC}=0.14 mA	I_{DC}=0.26 mA
g_{md}=2.06 mA/V			

*g_{md} and I_{DC} were obtained at V_{DD}= 30 mV and 50 mV, respectively.

** L was simulated at 460 MHz.

stage IRO implemented in the 130 nm technology. In order to measure the amplitude in each oscillator phase simultaneously, a symmetrical voltage buffer was designed. As shown in the schematic diagram in Fig. 44, the buffer is polarized by a dc current I_B. The degenerated common-source topology of each output of the buffer maintains an acceptable linearity for input signals of up to 300 mV peak-to-peak with a voltage gain of -1/3 at 400 MHz.

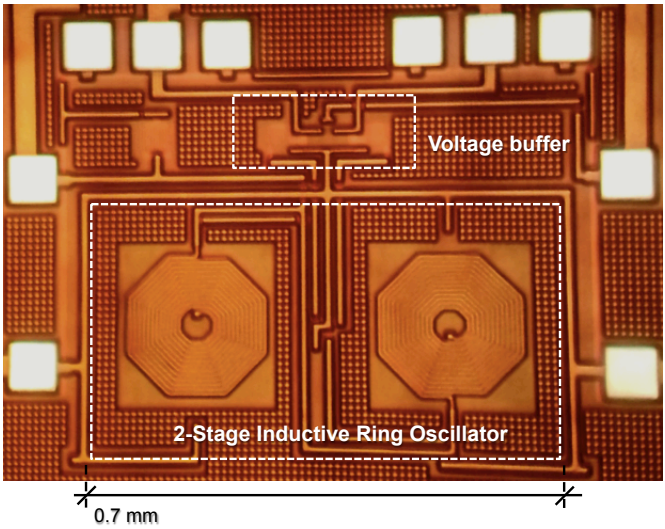


Figure 43: Micrograph of the two-stage IRO in a 130 nm technology.

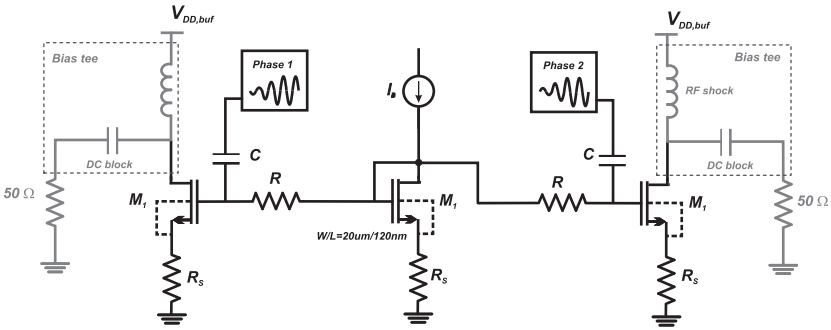


Figure 44: Schematic diagram of the voltage buffer.

Experimental measurements were performed in both the time and frequency domains. The experimental waveforms at each output of the voltage buffer, which has as inputs the two phases of the inductive ring oscillator were obtained using the oscilloscope Tektronix DSA 70804C and are shown in Figure 45. This figure shows the prototype oscillations at around 410 MHz when powered with a 45.3 mV supply.

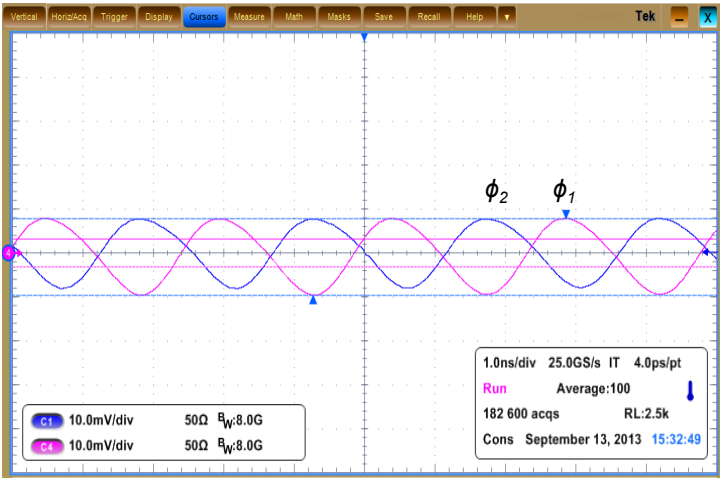


Figure 45: Experimental waveforms at the buffer outputs for V_{DD}=45.3 mV.

The variation in the amplitude and frequency of the IRO oscillator, in terms of the supply voltage, measured with the oscilloscope are shown in Fig. 46. The peak oscillator voltage is around 34 mV at V_{DD}=50 mV.

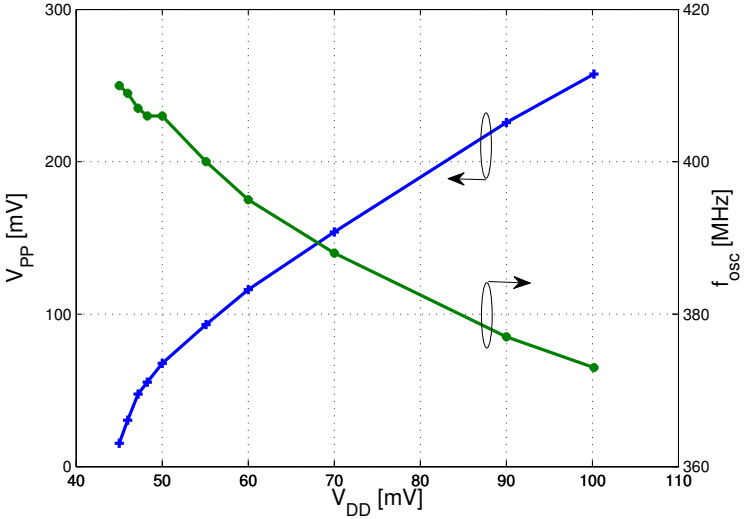


Figure 46: Experimental peak-to-peak output voltage and oscillation frequency of the two-stage IRO versus V_{DD}.

Figure 47 shows the oscillator under test with the spectrum analyzer Agilent MXA 9020A. The spectral diagram of the signal generated by the IRO for V_{DD} =50 mV is shown in Fig 48. The phase noise ($\mathcal{L}(f)$) measured with the application Agilent N9068A [50] was -108 dBc/Hz for V_{DD} = 50 mV, while for V_{DD} = 200 mV, $\mathcal{L}(f)$ = -130 dBc/Hz, both measured at Δf = 3 MHz.

The variations in the minimum supply voltage, oscillation frequency and dc power consumption (measured at $V_{DD} = V_{DD,min}$), for five samples of the oscillator, are shown in Fig. 49. As can be seen in the figure, the maximum variation between the five samples in terms of $V_{DD,min}$ was 2 mV, whereas the frequency deviation between the fastest and the slowest samples was less than 1%. It is worth noting the extremely low power consumption of the oscillator (below 20 μW) for all of the samples.

The main simulated and experimental results for the IRO are summarized in Table 7. Despite some differences in the minimum start-up voltage and in the oscillation frequency, the agreement between the simulated and experimental curves is quite good. Since the main goal of this study was to design oscillators operating with very low supply voltages for application in energy harvesting circuits, the

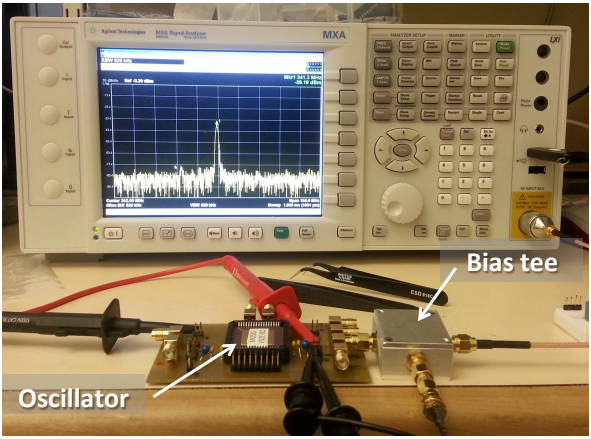


Figure 47: Photograph of the oscillator being tested by the spectrum analyzer Agilent MXA 9020A.

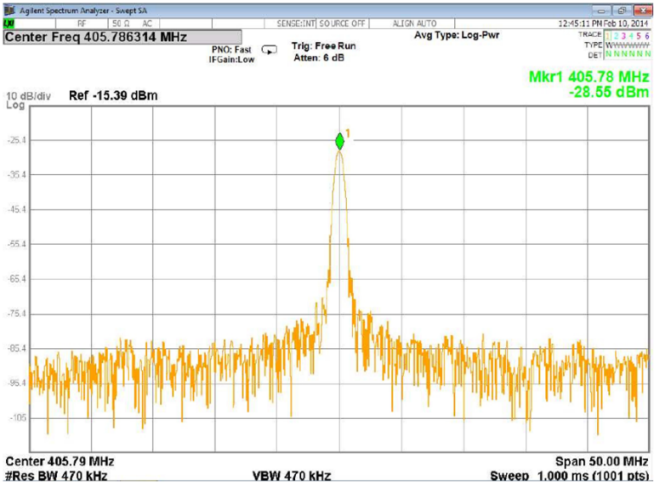


Figure 48: Spectral diagram of the two-stage inductive ring oscillator, obtained for V_{DD} = 50 mV.

accuracy of the oscillation frequency is not of major concern.

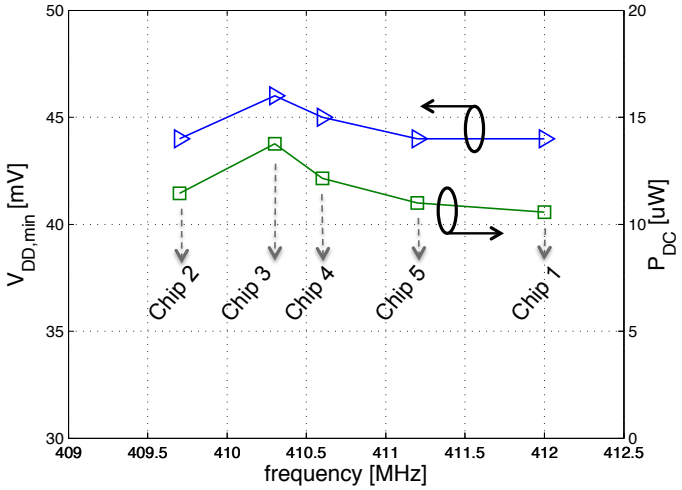


Figure 49: Comparison between five samples of the fully-integrated two-stage IRO, in relation to $V_{DD,min}$, f_{osc} and dc power consumption measured at $V_{DD} = V_{DD,min}$.

3.3 DESIGN OF THE ENHANCED SWING RING OSCILLATOR - ESRO

As shown in Chapter 2, due to the use of a second inductor in each stage, the ESRO topology can boost the oscillation amplitude beyond the supply rails even when operating with very small supply voltages. In order to demonstrate its ULV operation, the design and testing of the enhanced swing ring oscillator are described in this section. Two designs, one built with off-the-shelf inductors and the second fully-integrated, demonstrated operation at extremely low minimum supply voltages of 3.5 and 30 mV, respectively. The details of each design as well as the measurements taken with the two prototypes are given below.

3.3.1 Design of the ESRO using Off-the-Shelf Components

A prototype of a two-stage enhanced swing ring oscillator was built with off-the-shelf inductors and zero-VT transistors with an as-

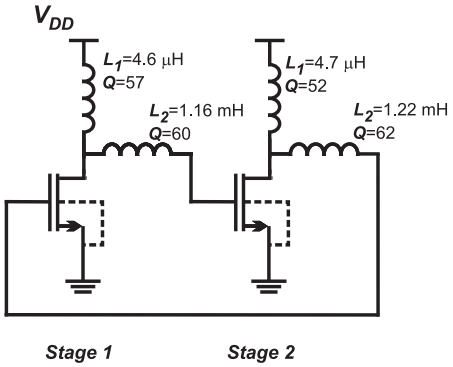


Figure 50: The two-stage ESRO with values for the passive components characterized at 1 MHz.

pect ratio W/L=300x5 μm/420 nm in the 0.13 μm CMOS process. The oscillator circuit, along with the values for the inductor parameters characterized at 1 MHz, are shown in Fig. 50.

Figure 51 shows the voltage at each output of the oscillator oscillating at around 1.1 MHz for supply voltage of 3.7 mV and 4.7 mV. Note the extremely high swing voltages at the outputs. The different magnitudes of the outputs are a consequence of the mismatch between inductors.

Figure 52 illustrates the variation in the amplitude of the gate voltage in terms of the supply voltage. The curves that represent the measured values are very close to those obtained for the simulated values. Simulation results in this paper were run in Spectre, the circuit simulator of Cadence.

Figure 53 shows a picture of the discrete prototype of the enhanced swing ring oscillator. In this experiment, the minimum start-up supply voltage was around 3.5 mV. It is interesting to note that the each output of the oscillator was loaded by an oscilloscope probe with R=1MΩ and C=2pF .

3.3.2 Design of the Fully-Integrated ESRO

Using the theoretical analysis detailed in Section 2, we designed a fully-integrated cross-coupled ESRO able to operate with supply voltages of around 30 mV. The inductors were designed so as to achieve a relatively high $K_L = L_2/L_1$ ratio (around 4), in order to reduce the g_{ms}/g_{md} ratio (see equation (2.24)) and, consequently,

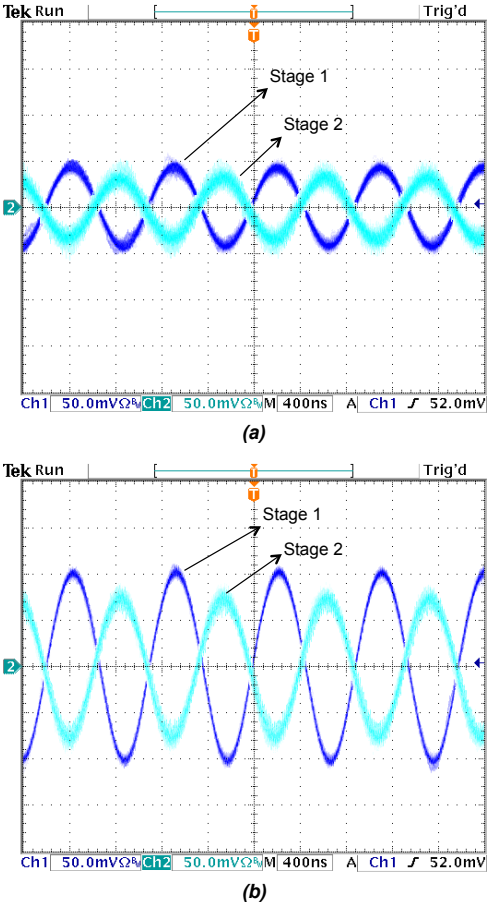


Figure 51: Experimental gate voltages of the two-stage ESRO with the parameter inductors given in Fig 50. (a) V_{DD} = 3.7 mV, (b) V_{DD} = 4.7 mV.

the minimum V_{DD} required for oscillation. Both inductors were also designed for a relatively high quality factor Q (around 8 at 400 MHz), which is close to the maximum value reached in the technology under consideration.

The theoretical optimum g_{md} was determined from (2.23), resulting in a value of around 13 mA/V after taking into account the inductor parameters in Table 8. In view of both the lack of accurate modeling for hand analysis and the parasitic elements due to the physical layout, we resorted to some fine-tuning through simulation. Subsequently, the aspect ratio W/L of the transistor was found to be

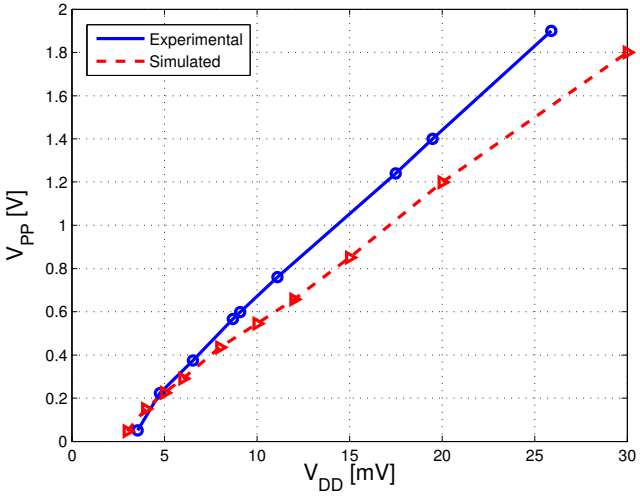


Figure 52: Simulated (dotted line) and experimental (solid line) peak-to-peak gate voltage *vs.* supply voltage of the two-stage ESRO.

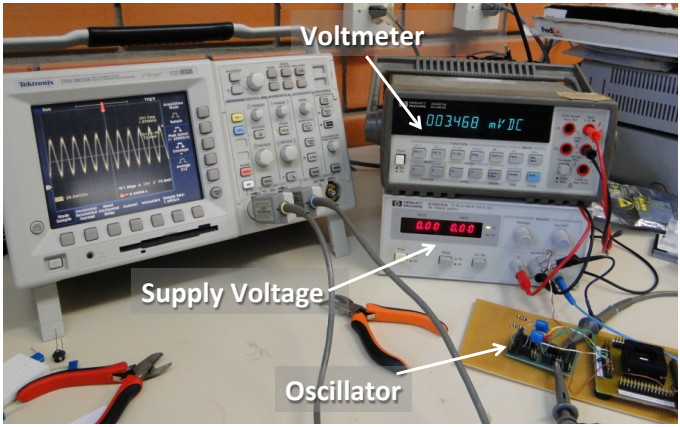


Figure 53: Picture showing the discrete prototype of the enhanced swing ring oscillator and test equipment.

25x20 μm/420 nm for the starting up of oscillations at the lowest supply voltage.

A summary of the characteristics of the components of each stage of the ESRO is given in Table 8. As can be seen, the measurements and the simulated results for the ESRO match very closely. Fig-

Table 8: Summary of device characteristics and the main simulated and experimental results for the fully integrated ESRO design.

Simulated Device Characteristics			**ESRO results**	
Transistor	Inductor L_1	Inductor L_2	Simulated	Experimental
W/L=25x20μm/0.42μm	L_1=19 nH	L_2=80 nH	$V_{DD,min}$=29 mV	$V_{DD,min}$=30 mV
V_T=46 mV	Q_1=8.7	Q_2=7.9	f_{osc}=410 MHz	f_{osc}=340 MHz
I_S=225 μA	f_{res1}=6.2 GHz	f_{res2}=1.2 GHz	I_{DC}=0.72 mA	I_{DC}=0.86 mA
g_{md}=7 mA/V				

*g_{md} and I_{DC} were obtained at V_{DD}= 30 mV and 50 mV, respectively.

** L_1 and L_2 were simulated at 400 MHz.

ure 54 shows the micrograph of the ESRO implemented in the 130 nm technology. In order to measure the two oscillator phases of the ESRO, again the voltage buffer shown in Fig. 44 was used.

In order to characterize the fully-integrated ESRO, the same setup used to measure the fully-integrated two-stage IRO in the time and frequency domains was applied. Figure 55 shows the waveforms at the buffer outputs. Despite the somewhat different amplitudes of the waveforms, a remarkable feature of this circuit is that it oscillates at around 340 MHz from a supply voltage as low as 30 mV.

The variations in the amplitude and frequency of the ESRO in terms of the supply voltage are illustrated in Fig. 56. For V_{DD}=50 mV the oscillator output peak voltage is around 145 mV. The minimum supply voltage for the starting up of oscillations is 30 mV at room temperature.

The measured spectral diagram of the signal generated by the fully-integrated ESRO for V_{DD} = 30 mV is shown in Fig 57. Assuming an offset frequency (Δf) of 3 MHz, the values for the oscillator phase-noise were -103 and -131 dBc/Hz for supply voltages of 30 and 100 mV, respectively.

3.4 COMPARISON BETWEEN THE DESIGNED CIRCUITS

Table 9 summarizes the main characteristics and results obtained with the implementation of the oscillators. It is interesting to note that, for both the ESRO and the ESCO, low ratios between the values for the energy storage devices, both capacitors and inductors, can

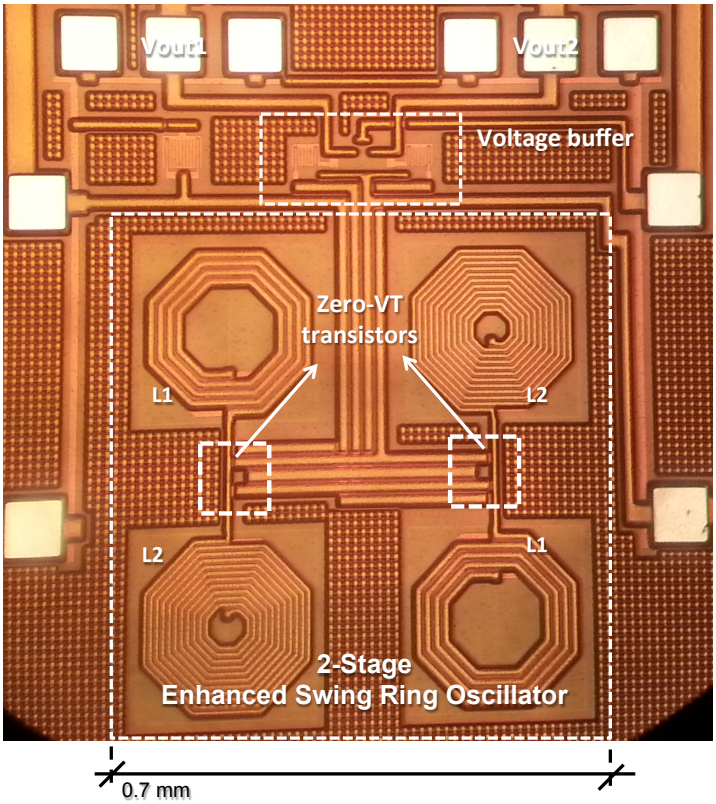


Figure 54: Micrograph of the two-stage ESRO in the 130 nm technology.

lead to very low $V_{DD,min}$, which is feasible with discrete components, but can be hard to achieve in integrated implementations.

To the best of our knowledge, the minimum supply voltages for the operation of the ESRO achieved in this study are the lowest reported to date for running either a fully integrated or an off-the-shelf oscillator. In Chapter 5, the remarkable characteristics of the ESRO operating from extremely low supply voltages will be applied to control charge pump circuits allowing the DC-DC boost conversion from very low voltage sources.

The experimental characteristics of the zero-VT transistors employed in the ULV oscillators are described in Appendix B.5.

Table 10 shows a comparison between some state-of-the-art oscillators and the fully-integrated two-stage IRO and ESRO designs. Despite the fact that the main motivation for this study is related to

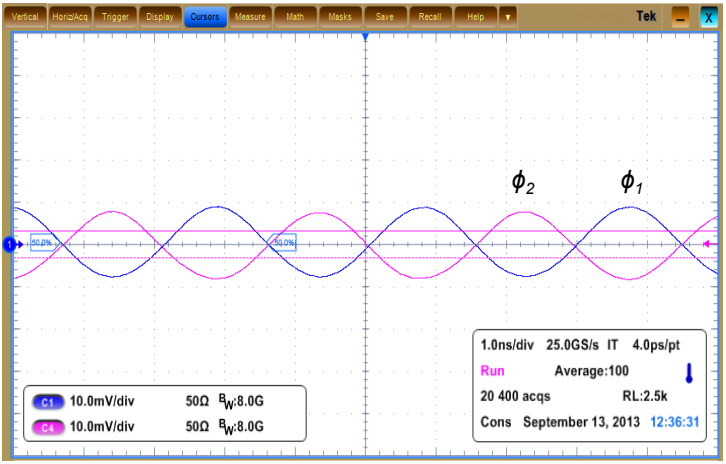


Figure 55: Waveforms at the output of the voltage buffer in which the inputs are the two phases of the ESRO, for V_{DD}=32 mV.

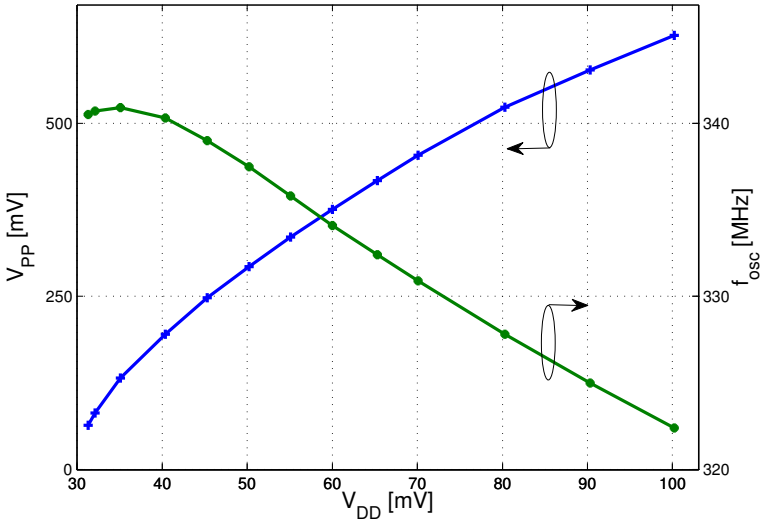


Figure 56: Experimental peak-to-peak output voltage and frequency of the two-stage ESRO in terms of V_{DD}.

energy harvesting, the data in the table show that the oscillators designed in this study present a remarkably low power consumption with acceptable phase noise characteristics, opening up new oppor-

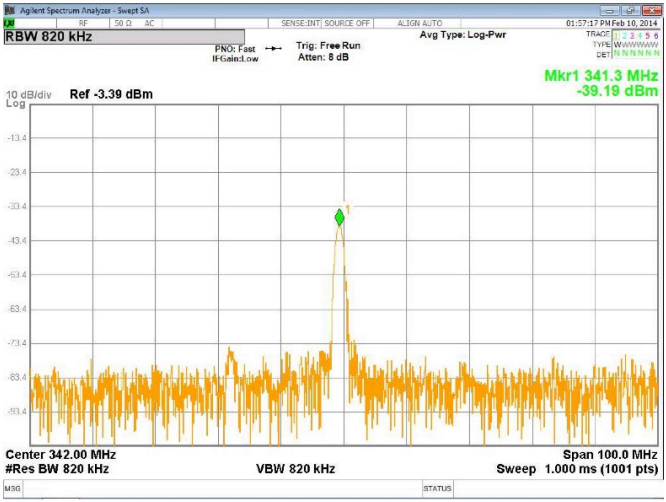


Figure 57: Spectral diagram of the two-stage ESRO for V_{DD} = 30 mV.

tunities for extremely low power RF applications.

In the table, the figure of merit (FoM), [44], is

$$FoM = 20\log\left(\frac{f_{osc}}{\Delta f}\right) - 10\log\left(\frac{P_{DC}}{1mW}\right) - \mathcal{L}(f) \tag{3.1}$$

where Δf is the offset frequency.

Table 9: Comparison between the ULV oscillators designed in this study.

	Devices		Exp. Results
	W/L=500x5μm/0.42μm		$V_{DD,min}$=15 mV
ESCO	L_1=9.8 mH	L_2=9.8 mH	f_{osc}=110 kHz
off-the-Shelf	$Q_1 \approx 90$	$Q_2 \approx 90$	V_P=320 mV
	C_1=1.54 nF	C_2=440 pF	
	*L simul. at 100 kHz; V_P meas. at V_{DD}=20 mV.		
	W/L=300x5μm/0.42μm		$V_{DD,min}$=86 mV
ESCO	L_1=13.6 nH	L_2=24.2 nH	f_{osc}=706 MHz
Fully-Integrated	$Q_1 \approx 13.9$	$Q_2 \approx 13.3$	I_{DC}=3 mA
	C_1=6 pF	C_2=3.5 pF	
	*L simul. at 800 MHz; I_{DC} meas. at V_{DD}=100 mV		
IRO 7-Stage	W/L=30x5μm/0.48μm		$V_{DD,min}$=53 mV
Fully-Integrated	L=100 nH	$Q \approx 8$	f_{osc}=550 MHz
			*L simul. at 550 MHz.
	W/L=30x6μm/0.42μm		$V_{DD,min}$=46 mV
IRO 2-Stage	L=108 nH	$Q \approx 7.9$	f_{osc}=410 MHz
Fully-Integrated			V_P=34 mV
			I_{DC}=0.26 mA
	*L simul. at 460 MHz; V_P, I_{DC} meas. at V_{DD}=50 mV		
	W/L=300x5μm/0.42μm		$V_{DD,min}$=3.5 mV
ESRO	L_1=4.6 μH	L_2=1.2 mH	f_{osc}=1.1 MHz
Off-the-Shelf	$Q_1 \approx 55$	$Q_2 \approx 60$	V_P=720 mV
	*L simul. at 1 MHz; V_P meas. at V_{DD}=20 mV		
	W/L=25x20μm/0.42μm		$V_{DD,min}$=30 mV
ESRO	L_1=19 nH	L_2=80 nH	f_{osc}=340 MHz
Fully-Integrated	$Q_1 \approx 8.7$	$Q_2 \approx 7.9$	V_P=145 mV
			I_{DC}=0.86 mA
	*L simul. at 400 MHz; V_P, I_{DC} meas. at V_{DD}=50 mV.		

Table 10: Comparison between oscillators designed in this study and state-of-the-art oscillators.

Ref.	$V_{DD,min}$	P_{DC}	$\mathcal{L}(f)^*$	Tech.	Freq.	FoM
[41]	0.5 V	0.6 mW	-119	0.18 μm	3.8 GHz	193
[44]	0.4 V	1.92 mW	-132	0.13 μm	4.9 GHz	193
[51]	1 V	4.2 mW	-127	0.13 μm	5.25 GHz	195
[52]	1 V	1.3 mW	-132	0.13 μm	4.9 GHz	196
IRO at $V_{DD} = 50mV$	50 mV	12.8 μW	-108	0.13 μm	405 MHz	169.5
ESRO at $V_{DD} = 30mV$	30 mV	15 μW	-103.5	0.13 μm	340 MHz	162
ESRO at $V_{DD} = 0.1V$	0.1 V	244 μW	-131	0.13 μm	323 MHz	181.6

*$\mathcal{L}(f)$ measured at Δf=3 MHz, except in [41] and [51] where $\mathcal{L}(f)$ was measured at Δf=1 MHz.

4 ULV STEP-UP CONVERTERS

In the previous chapters, the theory and the experimental results that support the operation of oscillators operating from extremely low voltage supplies have been presented without considering the main application of this thesis. In this chapter, the analysis of a ULV charge pump which, working together with the oscillators presented in Section 2, can boost voltages as low as the thermal voltage kT/q to the higher voltage levels (V_{DD} >500 mV) required to supply current electronic circuitry is described.

After a brief review of some ULV DC-DC converters, the topology proposed herein, which is based on the Dickson charge pump, is introduced. The mathematics of a circuit that operates down to extremely low voltages with expressions for the output voltage, power converter efficiency and input resistance is presented in the next sections.

4.1 ULV STEP-UP TOPOLOGIES

Converting input voltages of the order of the thermal voltage to dc voltages in the range of 0.5-1.0 V, typically required to power current electronic circuitry, is not an easy task. This is mainly because for supply voltages below 100 mV it is extremely difficult to generate oscillatory signals and simultaneously deal with the losses caused by the boost stage. In the past decade, in an attempt to reduce the minimum voltage required to start up the converter, many researchers have presented solutions employing topologies based on charge pumps or inductive boost (Fig. 58), or a combination of the two (Fig. 59).

The inductive boost converter topology shown in Fig. 58 (a) is widely used for voltage boosting because of its reasonable efficiency. However, for ULV applications, due to the low ratio of the ON current to the OFF current for low values of the peak-to-peak gate signals, the minimum operation voltage has been higher than 100 mV [53]. Also, the passive losses have a strong negative influence on the circuit performance. In fact, all of the fully-integrated inductive boost converters operate with at least 1 V of voltage supply [54], [55].

Another design challenge of the inductive boost topology operating under 100 mV is that for large transformation ratios (V_{out}/V_{in}), the duty-cycle must be extremely high. As an example, from the basics of the circuit [56], considering a continuous operating mode and

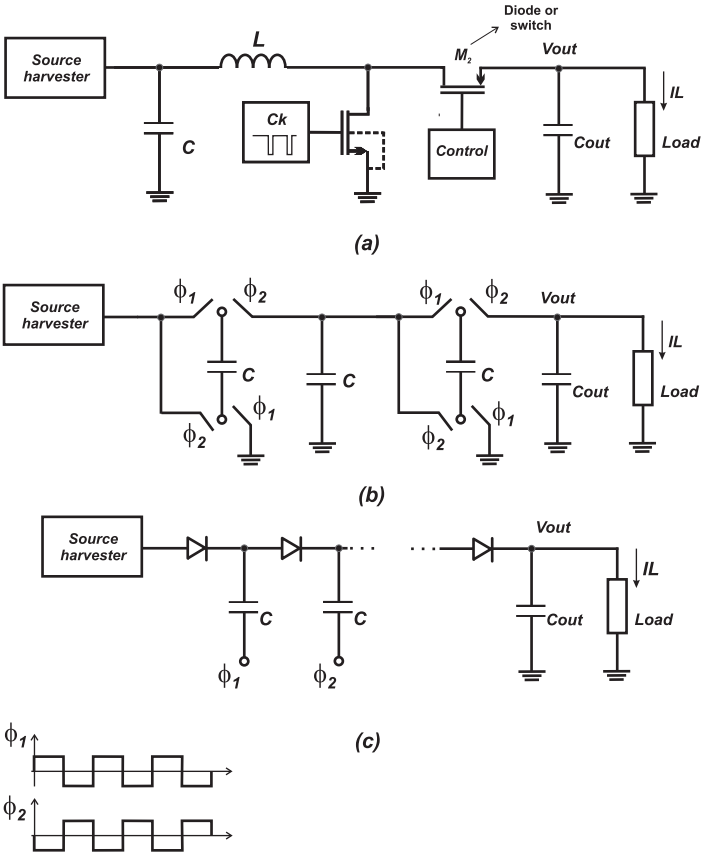


Figure 58: DC-DC converter topologies for ULV conversion. (a) inductive boost, (b) Fibonacci charge pump (c) Dickson charge pump.

a hypothetical lossless system, the duty-cycle D (ratio t_{on}/t_{off}) of the clock generator in Fig. 58 (a) is calculated as

$$D = 1 - \frac{V_{in}}{V_{out}} \tag{4.1}$$

resulting in $D = 0.95$ for values of V_{in}=50 mV and V_{out}=1 V, increasing the complexity of the control circuit and the quality requirements of the inductor and the switches. For similar reasons, the switched capacitor converters, such as the Fibonacci converter [57] shown in Fig. 58 (b), have not been used for ULV applications, with huge losses originating from the large number of stages and switches required.

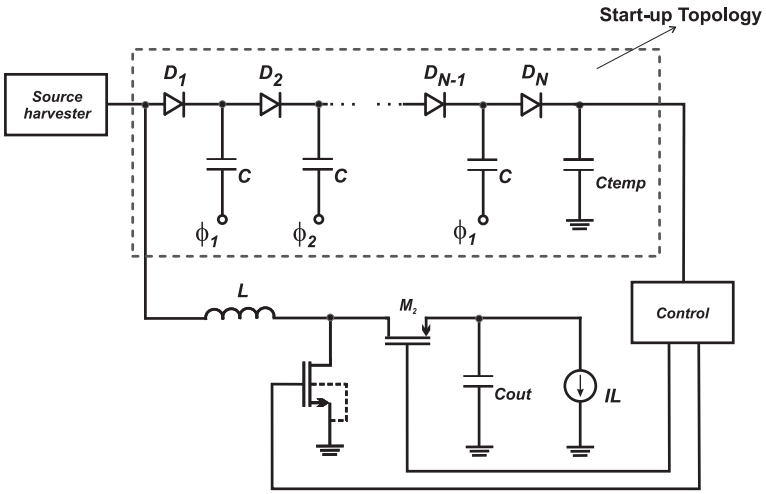


Figure 59: Hybrid topology composed of a charge pump and an inductive boost converter.

On the other hand, charge pump converters based on the topology introduced by John Dickson [58] have been employed in a wide variety of applications, even in the energy scavenging field. In fact, as has been demonstrated recently, the charge pump shown in Fig. 58(c) can operate from DC voltages below 100 mV even with clock signal amplitudes of the same order [10], [59]. However, the voltage drop across the diodes, particularly for a multiple-stage charge pump, which is required to elevate ULV references, adversely affects the efficiency and mitigates the output current, limiting the application of the topology to a start-up block in ULV applications. Despite the considerable efforts made over the past decade to improve the circuit efficiency, as demonstrated in [60] and [61], the applicability of the improvements achieved has not yet been demonstrated for ULV references.

The solution used to obtain high efficiency in the voltage conversion and a reduced start-up voltage has been the use of hybrid topologies: charge pump for the start-up and inductive boost for the permanent regime [10], [59], [62]. However, besides increasing the area and the number of off-chip components, the use of a second topology considerably increases the system complexity.

In the next sections, an analysis of the Dickson charge pump based on physical diode parameters, which allows us to explore the ULV design space of the converter, is described.

4.2 MODEL OF THE ULV DICKSON CHARGE PUMP

The basic operation of a charge pump can be understood with the help of the basic voltage doubler shown in Fig. 60 (a). During phase ϕ_1, switches S_1 and S_3 are "on", and capacitor C_1 is charged with $C_1 V_{DD}$. During phase ϕ_2, only S_2 is "on" and, ideally, $V_{out} = 2V_{DD}$. Considering the case in which a capacitor C_2 is a load, as shown in Fig. 60 (b), C_1 will share the stored charge with C_2, and $V_{out} = 2V_{DD}C_1/(C_1 + C_2)$. After a few cycles, some charge will be transferred to C_2 and ideally, $V_{out} \cong 2V_{DD}$.

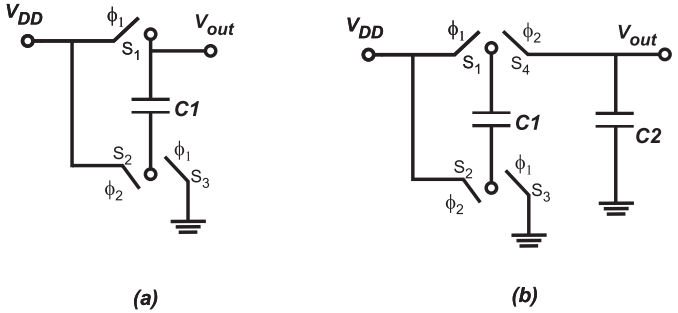


Figure 60: Basic voltage doubler [63].

A practical implementation of the multiplier shown in Fig. 60 is the Dickson charge pump (Fig. 61). For steady-state operation, assuming as an initial approximation that the forward voltage drop across each diode is the same, as shown in Fig. 61, the output voltage is given [58], [64] by

$$V_{out,ideal} = V_{in} + (N-1)\,2V_P - NV_d \tag{4.2}$$

where N is the number of diodes, V_d is the diode forward voltage drop and V_P is the peak voltage of V_ϕ.

Despite the result obtained in (4.2) gives us some idea regarding the converter output voltage, the conventional approach involving a constant diode forward voltage for the Dickson charge pump is not applicable for ULV operation since (4.2) does not provide any information on the dependence of V_d on the diode parameters and load current. Thus, in order to analyze the Dickson converter down to input voltages of the order of the thermal voltage kT/q or even less, a converter model, which includes both the load current and the more realistic exponential current-voltage characteristic of the diode, is in-

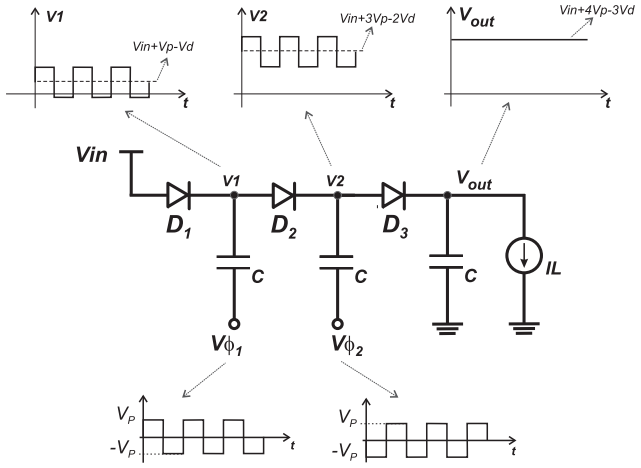


Figure 61: Dickson charge pump with the indication of the nodal voltages.

troduced herein.

4.2.1 The Output Voltage of the Dickson Converter

A schematic of the Dickson charge pump with the voltage waveform across the diodes considering steady-state operation is shown in Fig. 62. The voltage waveforms across D_1 and D_N differ from those across the intermediate diodes since one of the terminals of both the leftmost and rightmost diodes is connected to the dc nodes (V_{in} and V_{out}, respectively). For this reason, the forward voltage drops across D_1 and D_N are the same ($V_{d1} = V_{dN}$). For the other diodes, the forward voltage drop across them will be the same ($V_{d2} = \ldots = V_{dN-1}$). Thus, the dc output voltage of the converter is

$$V_{out} = V_{in} + (N-1)2V_P - 2V_{d1} - (N-2)V_{d2} \tag{4.3}$$

In order to calculate V_{d1} and V_{d2}, as in [25], [65], let us consider the steady-state operation and that both the output voltage and the load current are constants. Also, the diode is modeled by the Shockley equation (4.4), which can be applied to the MOSFET connected as a diode operating in weak inversion [25]. The diode current I_D is given by

$$I_D = I_{sat}\left(e^{V_D/n\phi_t} - 1\right) \tag{4.4}$$

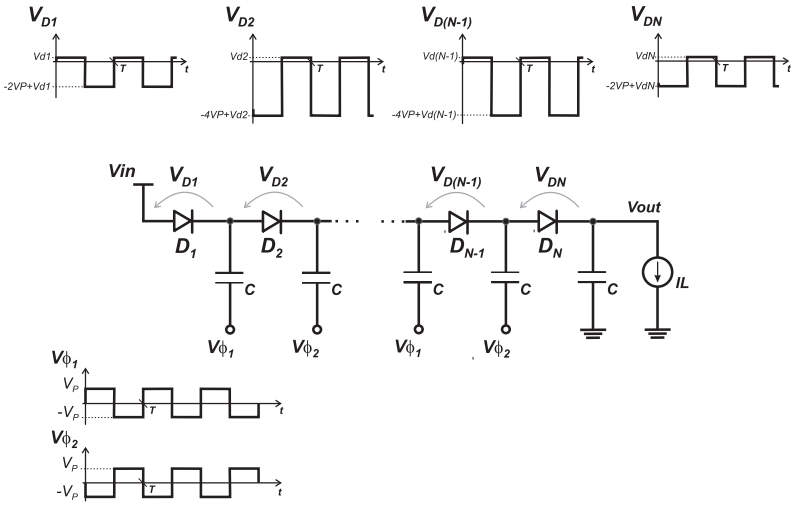


Figure 62: Dickson charge pump with the diode forward voltage drop indicated.

where I_{sat} is the diode saturation current, n is the diode ideality factor and V_D is the voltage across the diode. For the sake of simplicity, V_ϕ is considered as a square signal with amplitude V_P, as shown in Fig. 62. The average value of the diode current over a complete cycle of the oscillating signal is equal to the load current, I_L, *i.e.* [25]

$$I_L = \int_{-\frac{T}{2}}^{\frac{T}{2}} I_D dt \tag{4.5}$$

assuming that in steady-state operation the capacitor values are sufficiently high to keep the voltages at each node almost constant over each half-cycle, and thus the forward voltage drops V_{d1} and V_{d2} are calculated respectively, as

$$\left(1 + \frac{I_L}{I_{sat}}\right) T = \int_{-\frac{T}{2}}^{0} e^{\frac{V_{d1}}{n\phi_t}} dt + \int_{0}^{\frac{T}{2}} e^{\frac{V_{d1}-2V_P}{n\phi_t}} dt \tag{4.6}$$

$$\left(1 + \frac{I_L}{I_{sat}}\right) T = \int_{-\frac{T}{2}}^{0} e^{\frac{V_{d2}}{n\phi_t}} dt + \int_{0}^{\frac{T}{2}} e^{\frac{V_{d2}-4V_P}{n\phi_t}} dt \tag{4.7}$$

resulting in

$$V_{d1} = V_P - n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] \tag{4.8}$$

$$V_{d2} = 2V_P - n\phi_t \ln\left[\frac{\cosh(2V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] \tag{4.9}$$

Substituting the result of (4.8) and (4.9) in (4.3), the converter output becomes

$$V_{out} = V_{in} + 2n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] + (N-2)\, n\phi_t \ln\left[\frac{\cosh(2V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] \tag{4.10}$$

Simulations using the exponential diode model, performed with the Agilent ADS simulator, confirm the accuracy of (4.10). A comparison between the calculated and simulated output voltages, in terms of the normalized load current I_L/I_{sat}, is plotted in Fig. 63 with number of stages ranging from 2 to 10. In this figure V_{in}=30 mV, V_P=90 mV, ϕ_t=25.7 mV, and the parameters of the diodes are I_{sat}=40 μA, and n=1.

4.2.2 The Power Converter Efficiency - PCE

The PCE of the Dickson charge pump is the output power P_{out} divided by the input power P_{in}. The latter is the sum of the output power and the power loss P_{loss} due to the diodes [25]. Recalling that the voltage waveform across D_1 and D_N differ from those across the intermediate diodes (see Fig. 62), the power loss across the diodes will be $P_{d1} = P_{dN}$ and $P_{d2} = ... = P_{dN-1}$. In order to find P_{loss} we need to calculate P_{d1} and P_{d2}.

The power loss in $D1$ is given by

$$P_{d1} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{D1} I_{D1}\, dt = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{D1} I_{sat}\left(e^{V_{D1}/n\phi_t} - 1\right) dt \tag{4.11}$$

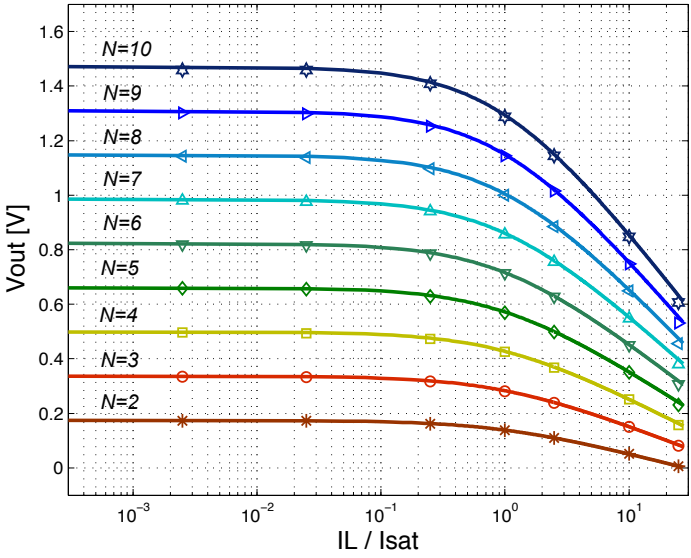


Figure 63: Calculated (solid line) and simulated (symbols) output voltage (V_{out}) *vs.* the load current normalized to the saturation current (I_L/I_{sat}), for N ranging from 2 to 10, V_{in}=30 mV and V_P=90 mV.

and considering the waveform of V_{D1} (shown in Fig. 62) results in

$$P_{d1} = \frac{1}{T}\int_{-\frac{T}{2}}^{0} V_{d1} I_{sat}\left(e^{\frac{V_{d1}}{n\phi_t}} - 1\right)dt + \frac{1}{T}\int_{0}^{\frac{T}{2}} (V_{d1} - 2V_P) I_{sat}\left(e^{\frac{V_{d1}-2V_P}{n\phi_t}} - 1\right)dt \tag{4.12}$$

Assuming $V_x = V_{d1} - V_P$, (4.12) can be re-written as

$$P_{d1} = \frac{1}{T}\int_{-\frac{T}{2}}^{0} (V_x + V_P) I_{sat}\left(e^{\frac{V_x+V_P}{n\phi_t}} - 1\right)dt + \frac{1}{T}\int_{0}^{\frac{T}{2}} (V_x - V_P) I_{sat}\left(e^{\frac{V_x-V_P}{n\phi_t}} - 1\right)dt \tag{4.13}$$

The solution of (4.13) is

$$P_{d1} = -I_{sat} V_x + \frac{I_{sat}}{2} e^{\frac{V_x}{n\phi_t}}\left[V_x\left(e^{\frac{V_P}{n\phi_t}} + e^{\frac{-V_P}{n\phi_t}}\right) + V_P\left(e^{\frac{V_P}{n\phi_t}} - e^{\frac{-V_P}{n\phi_t}}\right)\right] \tag{4.14}$$

$$P_{d1} = -I_{sat} V_x + I_{sat} e^{\frac{V_x}{n\phi_t}} \left[V_x \cosh\left(\frac{V_P}{n\phi_t}\right) + V_P \sinh\left(\frac{V_P}{n\phi_t}\right)\right] \tag{4.15}$$

From (4.8), the exponential term $e^{V_x/n\phi_t}$ can be written as

$$e^{\frac{V_x}{n\phi_t}} = e^{\frac{V_{d1}-V_P}{n\phi_t}} = \frac{1 + I_L/I_{sat}}{\cosh(V_P/n\phi_t)} \tag{4.16}$$

which, inserted into (4.15) gives

$$P_{d1} = I_L (V_{d1} - V_P) + (I_{sat} + I_L) V_P \tanh\left(\frac{V_P}{n\phi_t}\right) \tag{4.17}$$

Combining (4.8) with (4.17) results in

$$P_{d1} = (I_{sat} + I_L) V_P \tanh\left(\frac{V_P}{n\phi_t}\right) - I_L n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] \tag{4.18}$$

Following the same procedure to obtain (4.18), the power loss in D_2 is

$$P_{d2} = (I_{sat} + I_L) 2V_P \tanh\left(\frac{2V_P}{n\phi_t}\right) - I_L n\phi_t \ln\left[\frac{\cosh(2V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] \tag{4.19}$$

Since the total power loss, P_{loss}, due the diodes is $2P_{d1} + (N - 2)P_{d2}$, the total input power P_{in} is calculated as

$$P_{in} = P_{out} + P_{loss} \tag{4.20}$$

$$\begin{aligned} P_{in} = {} & I_L V_{out} + (I_{sat} + I_L) 2V_P \tanh\left(\frac{V_P}{n\phi_t}\right) - 2I_L n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] \\ & + (N-2)(I_{sat} + I_L) 2V_P \tanh\left(\frac{2V_P}{n\phi_t}\right) - (N-2) I_L n\phi_t \ln\left[\frac{\cosh(2V_P/n\phi_t)}{1 + I_L/I_{sat}}\right] \end{aligned} \tag{4.21}$$

The substitution of (4.10) in (4.21) results in

$$P_{in} = I_L V_{in} + (I_{sat} + I_L) 2V_P \left[\tanh\left(\frac{V_P}{n\phi_t}\right) + (N-2)\tanh\left(\frac{2V_P}{n\phi_t}\right)\right] \tag{4.22}$$

A comparison between the values for the calculated (4.22) and simulated (using ADS simulator) input power in Fig. 64 verifies the accuracy of the model developed

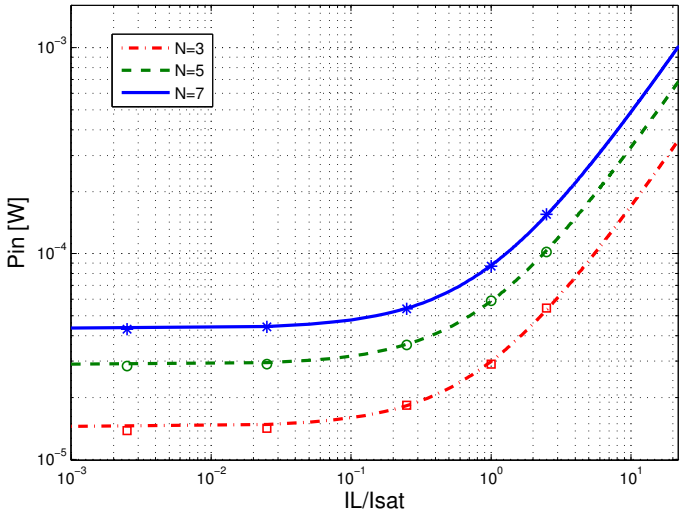


Figure 64: Calculated (line) and simulated (symbols) input power (P_{in}) *vs.* the load current normalized to the saturation current (I_L/I_{sat}), for N = 3, 5 and 7, V_{in}=30 mV, V_P=90 mV and $n\phi_t$=25.7 mV.

Finally, from (4.22), the power converter efficiency can be calculated as

$$PCE = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}$$

$$PCE = \frac{V_{in} + 2n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t)}{1+I_L/I_{sat}}\right] + (N-2)\,n\phi_t \ln\left[\frac{\cosh(2V_P/n\phi_t)}{1+I_L/I_{sat}}\right]}{V_{in} + \left(1+\frac{I_{sat}}{I_L}\right)2V_P\left[\tanh\left(\frac{V_P}{n\phi_t}\right) + (N-2)\tanh\left(\frac{2V_P}{n\phi_t}\right)\right]} \quad (4.23)$$

Figure 65 shows of the theoretical PCE (from equation (4.23)) in terms of the normalized load current I_L/I_{sat} and the amplitude V_P. As can be seen in the graphs, the power converter efficiency is strongly dependent on the load current and the amplitude of the signal. Also, we can note that for a given load current, the converter efficiency can be optimized according to the diode saturation current value.

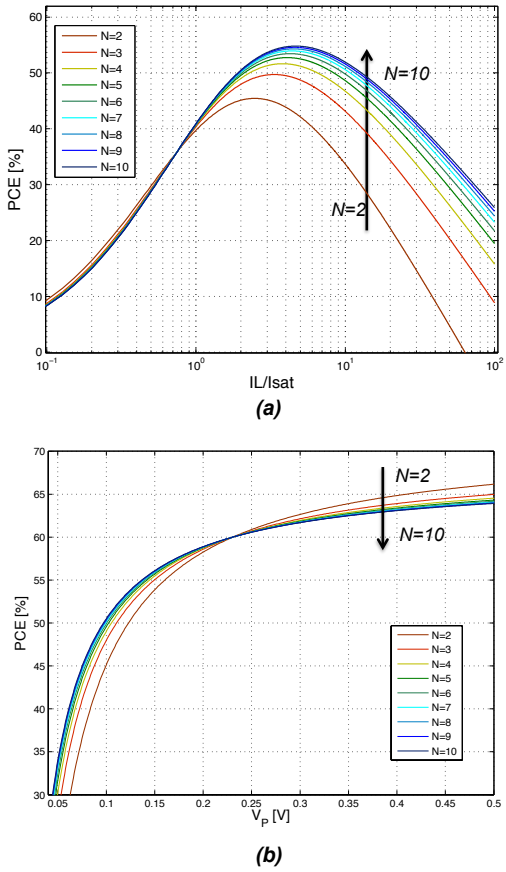


Figure 65: Theoretical (from equation (4.23)) PCE for N ranging from 2 to 10: (a) in terms of I_L/I_{sat} for I_{sat} = 40 μA, V_{in}=50 mV and V_P=$2V_{in}$; (b) in terms of V_P for I_{sat}= 40 μA, and I_L = $2I_{sat}$, and V_P = $2V_{in}$. In both graphs $n\phi_t$=25.7 mV.

4.2.3 The Equivalence between Square and Sine Signals

In the context of this study, where the converter will operate from an LC oscillator, it is convenient to adapt the model of the Dickson converter, obtained considering a square signal, for use with a sine wave signal. Taking the equivalence between a square wave of magni-

tude V_P and a sine wave of amplitude V_A, demonstrated in [25], where

$$I_0(V_A/n\phi_t) = \cosh(V_P/n\phi_t) \tag{4.24}$$

we can rewrite the Dickson models for the output voltage, input power and power converter efficiency for a sine wave as

$$V_{out} = V_{in} + 2n\phi_t \ln\left[\frac{I_0\left(V_A/n\phi_t\right)}{1+I_L/I_{sat}}\right] + (N-2)\, n\phi_t \ln\left[\frac{I_0\left(2V_A/n\phi_t\right)}{1+I_L/I_{sat}}\right] \tag{4.25}$$

$$P_{in} = I_L V_{in} + (I_{sat}+I_L)\, 2V_A\left[\frac{I_1\left(V_A/n\phi_t\right)}{I_0\left(V_A/n\phi_t\right)} + (N-2)\,\frac{I_1\left(2V_A/n\phi_t\right)}{I_0\left(2V_A/n\phi_t\right)}\right] \tag{4.26}$$

$$PCE = \frac{V_{in} + 2n\phi_t \ln\left[\frac{I_0(V_A/n\phi_t)}{1+I_L/I_{sat}}\right] + (N-2)\, n\phi_t \ln\left[\frac{I_0(2V_A/n\phi_t)}{1+I_L/I_{sat}}\right]}{V_{in} + \left(1+\frac{I_{sat}}{I_L}\right) 2V_A\left[\frac{I_1(V_A/n\phi_t)}{I_0(V_A/n\phi_t)} + (N-2)\,\frac{I_1(2V_A/n\phi_t)}{I_0(2V_A/n\phi_t)}\right]} \tag{4.27}$$

where $I_0(z)$ and $I_1(z)$ are the modified Bessel functions of the first kind, of order zero and one, respectively.

4.2.4 The Input Resistance of the Charge Pump

For design purposes, it is worth calculating the equivalent resistance seen by the oscillator $R_{in,cp}$. Thus, for a sine wave oscillator, disregarding the term related to the dc input voltage (V_{in}=0) in (4.26), according to the model shown in Fig. 66 $R_{in,cp}$ can be expressed as

$$R_{in,cp} = \frac{2V_A^2}{P_{in}^*}$$

$$R_{in,cp} = \frac{V_A^2}{(I_{sat}+I_L)\, V_A\left[\frac{I_1(V_A/n\phi_t)}{I_0(V_A/n\phi_t)} + (N-2)\,\frac{I_1(2V_A/n\phi_t)}{I_0(2V_A/n\phi_t)}\right]} \tag{4.28}$$

where P_{in}^* is the power delivered by the oscillator.

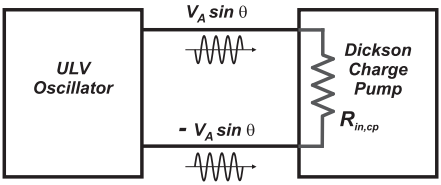


Figure 66: Model of the equivalent resistance of the charge pump seen by the oscillator.

4.3 DESIGN METHODOLOGY - DETERMINATION OF N AND I_{SAT}

Once the equations for the output voltage and the power converter efficiency have been derived, the values of N and I_{sat} which minimize the losses of the converter can be found. As shown in Fig. 67, for a specified output voltage and load current (*eg.* V_{out}=1V and I_L=1μA), there is an optimum number of stages that minimizes the converter losses and thus improves the converter efficiency. For this optimum N value, the value of I_{sat} such that V_{out}=1V is found. In Fig. 67, the ideality factor that fits the Shockley equation is n = 1.4, a value obtained with the zero-VT transistor employed as a diode, as will be seen in the next section. For the example of Fig. 67 where the specification is V_{out} =1V and I_L = 1μA, the highest PCE value (PCE = 29.7%) is obtained for N=11 and I_{sat} =400 nA.

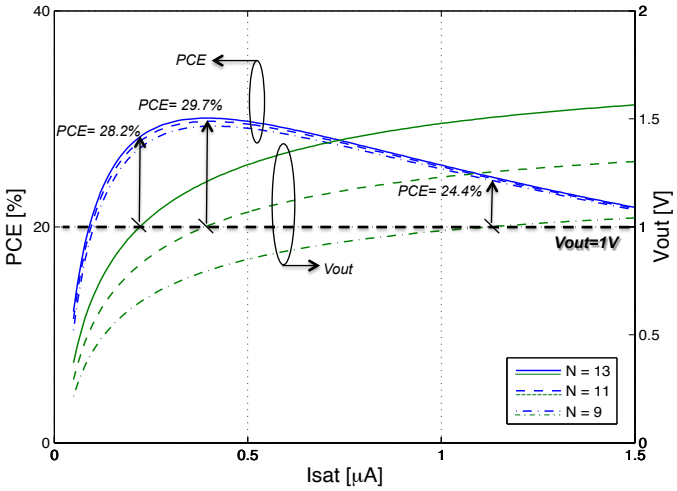


Figure 67: Calculated output voltage (eq. (4.25)), and power converter efficiency (eq. (4.27)) in terms of the diode saturation current I_{sat}, for numbers of stages of 9, 11 and 13. ϕ_t=25.7 mV.

5 DESIGN OF AND EXPERIMENTATION WITH THE ULV STEP-UP CONVERTERS

Based on the theoretical analysis of both the oscillators and the charge pumps operating at extremely low voltages, this chapter presents the design, implementation and testing of a three prototypes of a step-up converter: fully-integrated; integrated with external inductors; and discrete. The goal was to boost voltage levels of the order of, or lower than, kT/q.

The architecture of the step-up converters designed is shown in Fig. 68. Due to the remarkable characteristics of the enhanced swing ring oscillator, that is, (i) oscillating even when powered with very low supply voltages, (ii) boosting the output magnitude and (iii) generating two complementary phases, this topology was chosen to provide the ac signals required for the operation of the charge pump.

In order to reduce the voltage drop across the diodes, high drive capability diodes were employed, using diode-connected zero-VT transistors or Schottky diodes for the off-the-shelf design. The characteristics of each design will be described in this chapter. It should be noted that the oscillator and the converter in Fig. 68 are powered from the same source.

Using the measurement setup shown in Fig. 69, composed of the Keithley SourceMeter 2450, used for the power supply and to measure the dc current consumption of the circuits (I_{DC}), and the Keithley current source 6221, employed to emulate a load current (I_L), the converter output voltage and the input/output power were measured.

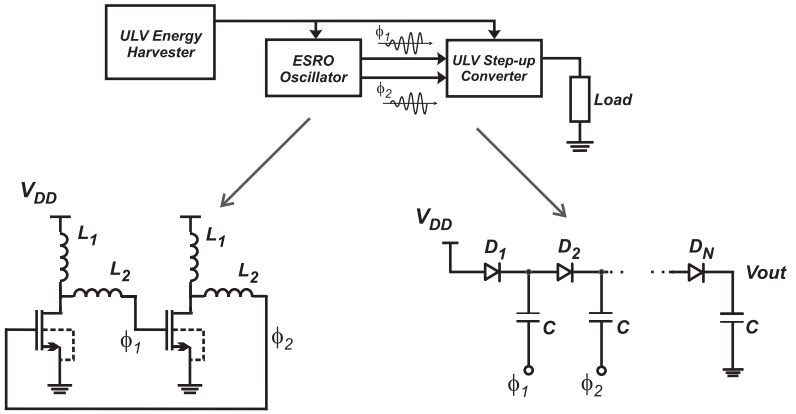


Figure 68: The proposed step-up ULV topology.

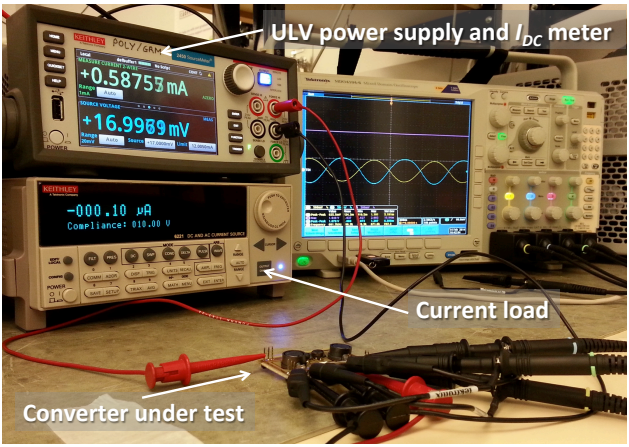


Figure 69: Setup employed to measure the characteristics of the step-up converters.

In order to measure the dc voltage at the converter output, the high-impedance voltmeter Agilent 34411A was used. For some of the measurements taken with the oscilloscope, each measured terminal under test was loaded by an oscilloscope probe with R = 10 MΩ and C= 3.3 pF.

The methodology to design the ULV step-up converters is based on the simplified flowchart shown in Fig. 70. From a specified oscillation frequency, the inductors can be initially selected in order to present a high L_2/L_1 ratio (at least 3) and at the same time provide the highest quality factor (for that frequency). With the aid of (2.23), the initial value of the transistor g_{md}, and thus the W/L ratio, can be found. With the value for the oscillator peak voltage (obtained by simulation or experimentally), from the specifications for the output voltage and load current, it is possible to find the best pair (number of stages of the charge pump and the diode saturation current) that minimizes the converter losses. To adjust the specifications of frequency and minimum start-up voltage, some interaction may be necessary in order to define the oscillator transistor aspect ratio and the value for the inductors. Also, due to the oscillator peak-amplitude being dependent on the equivalent load inserted by the converter, some interactions are necessary in order to define the W/L ratio of the transistor connected as a diode.

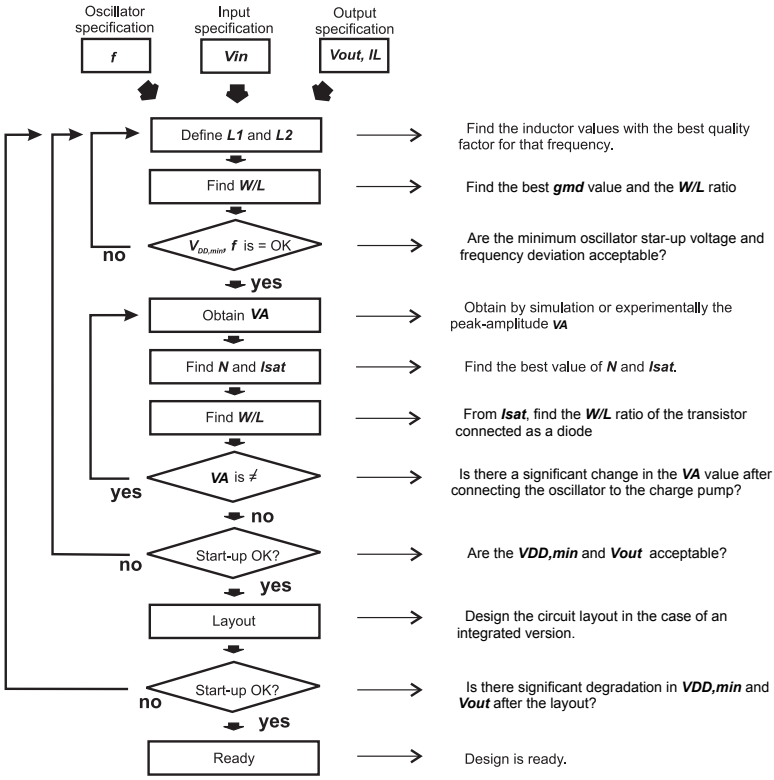


Figure 70: Flowchart used to design the ULV step-up converters.

5.1 THE IMPLEMENTED CHIP

In order to verify the voltage limits of the topology in an integrated version, the chip shown in Fig. 71 was designed in the IBM 130 nm CMOS technology. Two designs were implemented in the same chip: a fully-integrated one, built with inductors available in the technology, and another using external high-Q inductors. As indicated in Fig. 71, the implemented blocks in the chip are a fully-integrated ESRO, an eleven-stage Dickson charge pump, a pair of zero-VT transistors to be used in the external inductors-based design, a buffer to take the oscillator outputs and a voltage limiter to protect the diodes of the converter against over voltages.

In order to save chip area, the strategy adopted was the sharing

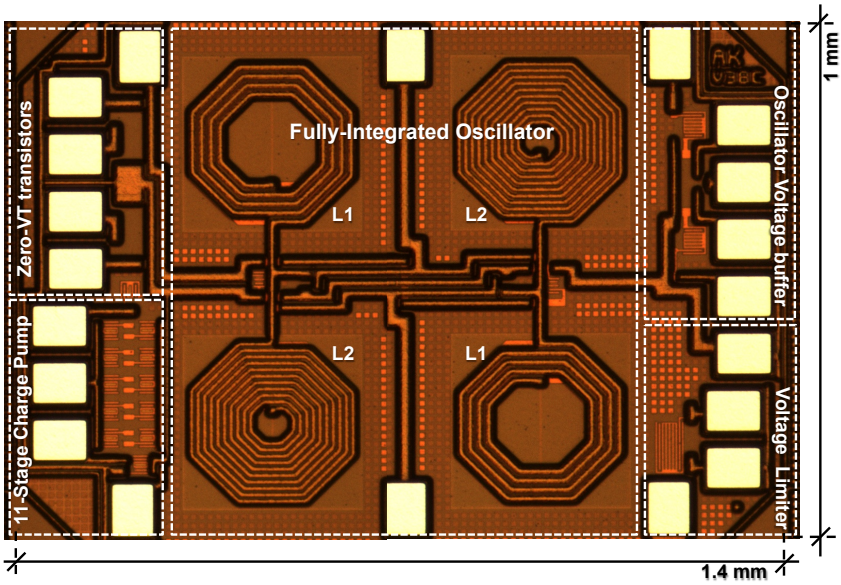


Figure 71: Micrograph of the chip implemented in the 130 nm technology.

of some blocks common to the two designs, such as the voltage limiter and the oscillator voltage buffer. Because of the similar specifications (as will be demonstrated in this chapter), the same 11-stage charge pump was employed in both designs. Thus, to test the two step-up converters, some blocks were connected externally.

5.2 THE FULLY-INTEGRATED CONVERTER DESIGN

Using the IBM 130 nm CMOS technology, the fully integrated step-up converter topology shown in Fig. 72 was designed and implemented. The main design goal was to generate a dc output of 1V at a current consumption of 1 μA with the minimum input dc voltage.

The design methodology followed the flowchart in Fig. 70. As regards the oscillator design, the inductors were designed to achieve a relatively high $K_L = L_2/L_1$ ratio (L_1 = 18 nH and L_2 = 66 nH), in order to reduce the minimum V_{DD} required for oscillation. Both inductors have a quality factor Q of around 8 at 500 MHz, which is close to the maximum value reached in the technology under consideration for that frequency. After the definition of the value for the inductors, a starting point for the calculation of the zero-VT transistor aspect ratio

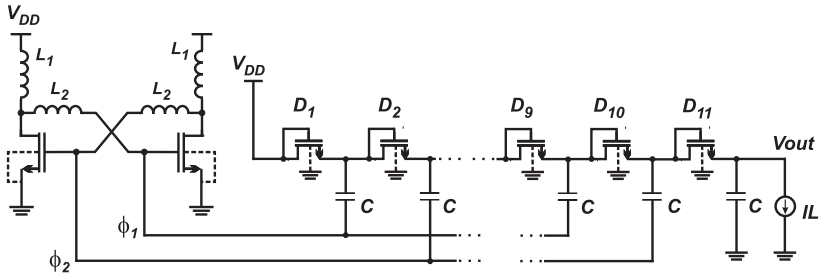


Figure 72: Schematic diagram of the fully-integrated step-up converter implemented with zero-VT transistors.

is equation (2.23), which gives the g_{md} value of the transistor that minimizes V_{DD}. Considering also the specified oscillation frequency, the W/L ratio of the zero-VT transistor must be calculated (or determined through simulation) to achieve the capacitance required to maintain the operation frequency. After some fine tuning by simulation the W/L ratio was 500 μm/0.42 μm.

The charge pump parameters were defined from the efficiency criteria presented in Section 4.3. As shown in Fig. 67, considering the above-mentioned specifications (V_{out}=1 V and I_L=1 μA), for a sine wave signal with an amplitude of 107 mV (simulated amplitude generated by the oscillator), the best number of stages is 11, with an ideal diode saturation current value of around 400 nA. Thus, considering the zero-VT transistor connected as a diode, as shown in Fig. 72, after some tuning by simulation, the transistor aspect ratio that matches the requirements for the output voltage and load current was W/L= 4.2 μm/0.42 μm, with I_{sat} = 550 nA. The I_D *vs.* V_D curve for the transistor operating as a diode is shown in Appendix B. The device characteristics of the fully integrated step-up converter design are summarized in Table 11.

The calculated efficiency of the designed Dickson converter in terms of the peak oscillator amplitude for I_L ranging from 0.1 μA to 1 mA, is shown in Fig. 73. As can be seen in the graph, for V_A < 200 mV the maximum efficiency is around 50%.

The layout of the ESRO and the eleven-stage Dickson charge pump, both designed in the IBM 130 nm technology, are shown in Fig. 74. As can be seen, wide metal lines were used in order to reduce the ohmic losses of the designed circuits.

For the fully integrated prototype shown in Fig. 71, the values for the dependence of the converter output voltage (V_{out}), the output power (P_{out}) and the power converter efficiency (PCE) on the supply

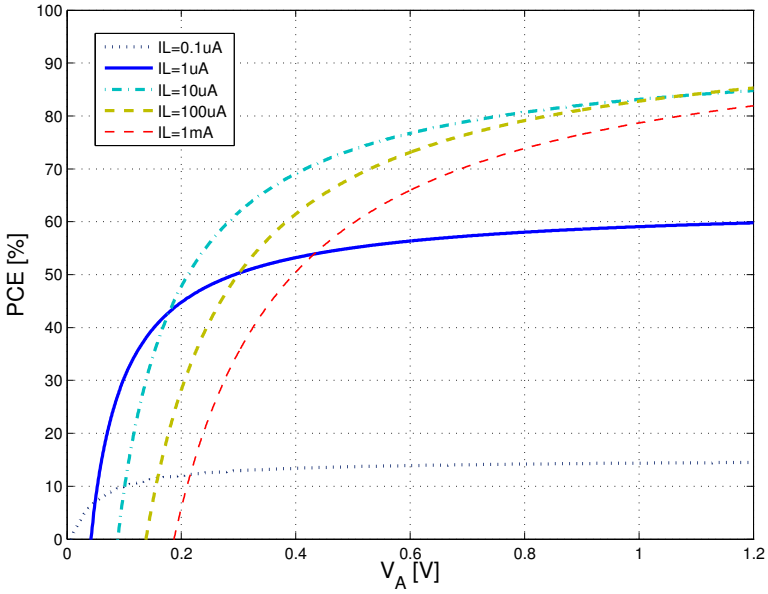


Figure 73: Calculated, from (4.27), PCE of the implemented eleven-stage Dickson converter ($N = 11$; I_{sat}=550 nA) in terms of the peak amplitude, for I_L ranging from 0.1 μA to 1 mA.

voltage ($V_{in} = V_{DD}$) were experimentally determined for the load current ranging from 10 nA to 5μA, as shown in Fig. 75.

Operating at a frequency of around 550 MHz, the fully-integrated prototype can start up from 73 mV of V_{DD}, generating around 400 mV at the output. As shown in Fig. 75, the target specification of 1V of output voltage and 1 μA of load current is obtained at $V_{DD} = 86$ mV.

From the curves in Fig. 75 (b) it is shown that, even when built with quality-factor inductors of around 8, the circuit can provide 5 μW at the output for an input voltage of around 108 mV.

The experimental and calculated V_{out} *vs.* I_L characteristics of the eleven-stage Dickson converter (considering only the charge pump without the oscillator) is shown in Fig. 76. To obtain the experimental points, the pulse pattern generator HP 81130A was used, which provided the two complementary square signals, with 50 MHz and peak amplitude $V_P = 2 * V_{DD}$, for V_{DD} of 25, 30 and 35 mV. The experimental waveforms of the signal provided by the pattern genera-

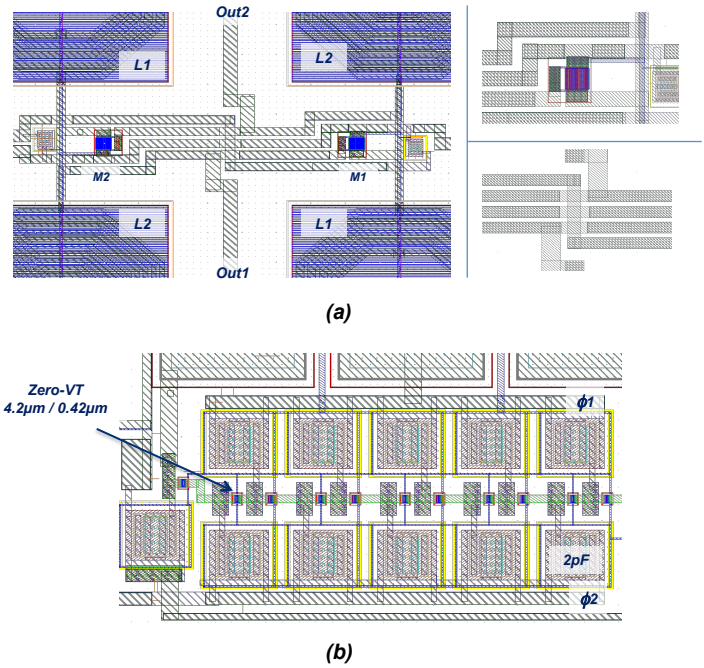


Figure 74: (a) Layout of the ESRO oscillator; (b) Layout of the eleven-stage Dickson converter, both designed in the 130 nm technology.

tor are shown in Fig. 76. The differences between the simulated and experimental results can be attributed to the mismatch between the Shockley diode model, assumed in the calculations, and the zero-VT transistor behavior operating as a diode.

5.3 THE CONVERTER DESIGN WITH EXTERNAL INDUCTORS

In order to decrease the minimum V_{DD} of the circuit shown in Fig. 72, to increase the output power capability and the converter efficiency, a second step-up converter was designed using external inductors with a quality factor of around 60, which is able to start up with less than 20 mV of V_{DD}. In an attempt to reduce the prototype area and the losses inserted by the connections between the chip and the external inductors, the chip was wire-bonded to the substrate using gold wires with a length of 1.5 mm. Figure 77 shows a photograph of the circuit board implemented to test the chip. The dimensions of

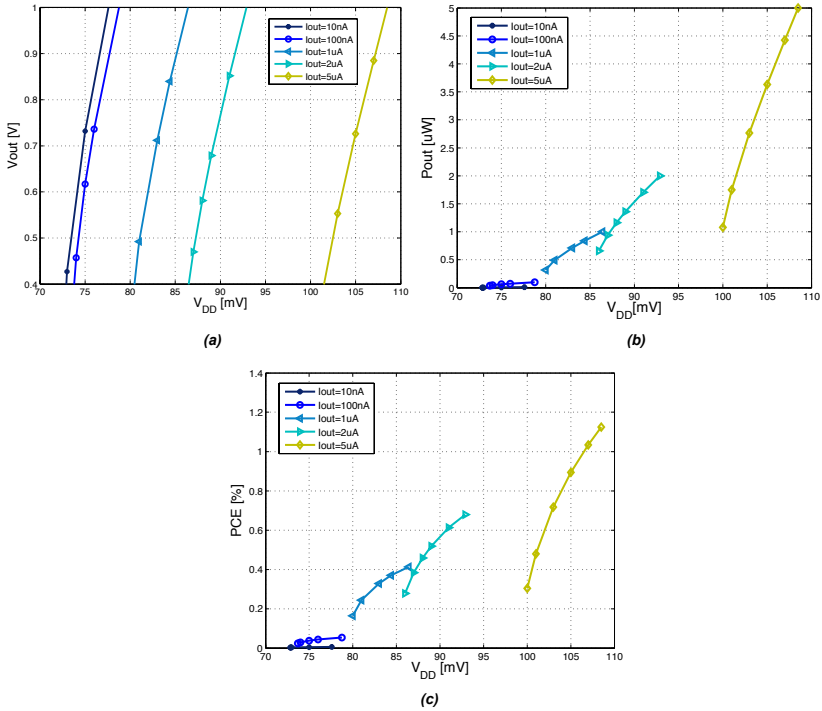


Figure 75: Experimental (a) output voltage, (b) output power, and (c) power converter efficiency of the fully-integrated converter for a load current ranging from 10 nA to 5 µA. All curves are plotted in terms of the supply voltage ($V_{DD} = V_{in}$).

the external inductors L_1 and L_2 were 2.5 mm x 2 mm and 3.4 mm x 1.6 mm, respectively. A photograph of the SMD inductors used in the design can be seen in Fig. 78. The zero-VT transistors of the oscillator as well as the Dickson charge pump (same converter implemented in the fully-integrated design) were integrated in the chip shown in Fig. 71.

A flowchart of the design method is shown in Fig. 70. From the high quality inductors (L_1=220 nH, L_2=595 nH, both with a quality factor of around 60 at 50 MHz), the aspect ratio of the zero-VT transistor found using the algorithm in Fig. 70 was 2000 μm/0.42 μm. In order to save chip area, and considering the same design target specification as that for the fully-integrated design (V_{out} = 1V at $I_L = 1\mu$A), the same eleven-stage charge pump converter (employed in the fully-

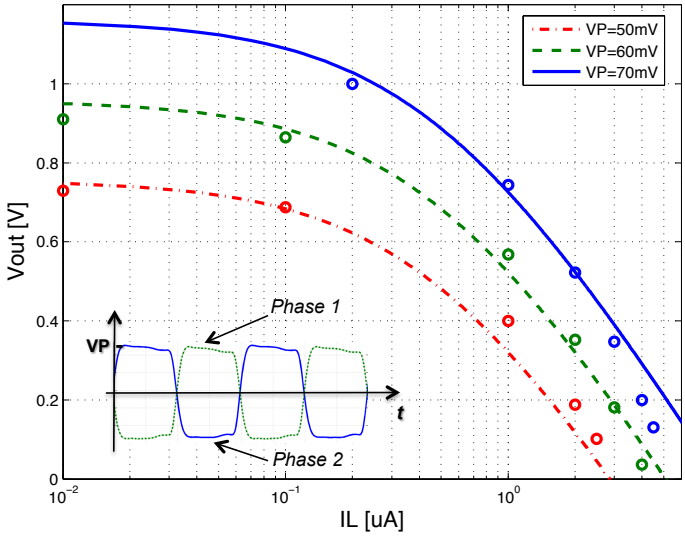


Figure 76: Calculated (lines) and experimental (symbols) of the integrated converter output voltage in terms of the load current for $V_P = 2V_{in}$.

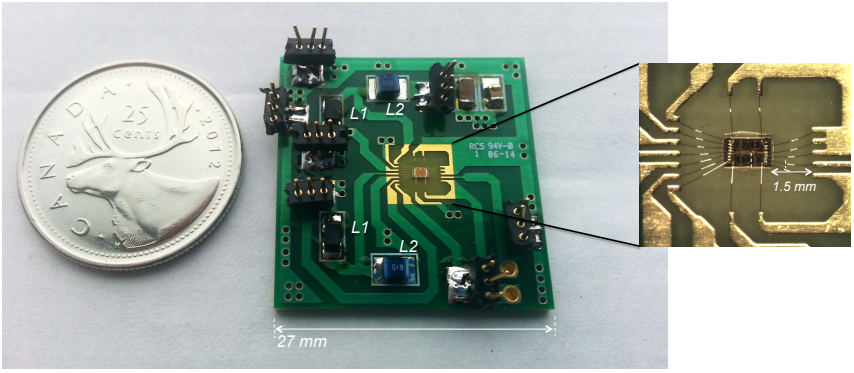


Figure 77: Photograph of the wire-bonded prototype implemented to test the step-up converter designed with external inductors.

integrated design) was adopted.

The layout of the wide zero-VT transistors (W/L=400x5μm/0.42μm) used in the oscillator, composed of a parallel association of 400 unitary transistors of W/L=5μm/0.42μm, is shown in Fig. 79.

The post-layout simulation of the step-up converter is shown

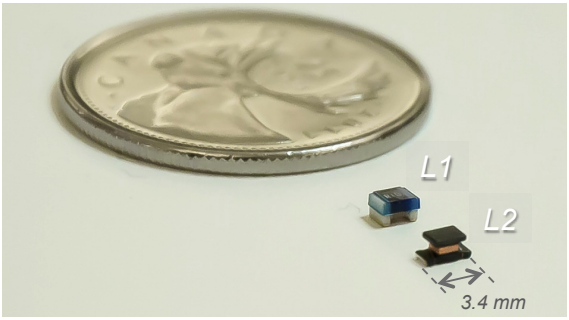


Figure 78: Photograph of the SMD inductors employed in the converter design.

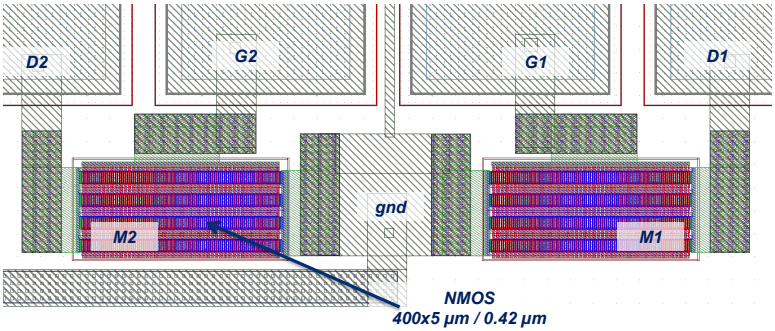


Figure 79: Layout of the zero-VT transistors used in the step-up converter designed with external inductors.

in Fig. 80. In Fig. 80 (a) the transient simulated characteristics for V_{DD}=24 mV and I_L=1 μA are shown. The minimum supply voltage to start up the converter (I_L = 0) simulated with the corners of the technology is shown in Fig. 80 (b). On comparing the simulations performed using the typical parameters (tt) with the experiments obtained employing the wire-bonded prototype (shown in Fig. 81) the results match very closely.

For the prototype shown in Fig. 77, the experimental curves for V_{out}, P_{out} and PCE *vs.* the supply voltage are shown in Fig. 81 (a), (b) and (c), respectively.

As can be seen, the condition I_L = 1 μA and V_{out} = 1 V is obtained at V_{DD} = 23 mV, while with V_{DD} = 37.7 mV the circuit can supply a load current of 5 μA, maintaining V_{out} = 1V. As was explained in Chapter 4, for low voltages the Dickson charge pump efficiency is affected by the oscillator peak amplitude. Thus, considering an eleven-

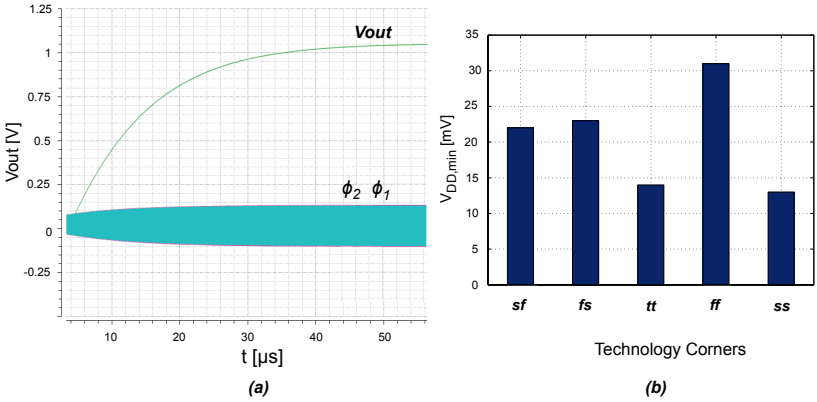


Figure 80: Post-layout simulation of the step-up converter with external inductors. (a) V_{out} for V_{DD}=24 mV and I_L=1 μA and (b) minimum supply voltage to start up the converter considering the corners of the technology.

stage converter, for an output voltage of 1V, the maximum oscillator amplitude will be lower than 100 mV, limiting the converter efficiency. This characteristic can be seen in the graph of Fig. 81 (d), where the maximum PCE was around 10 for an output voltage of 1V.

Also, as illustrated in Fig. 65, there is an optimum I_L/I_{sat} ratio that maximizes the converter efficiency. For the converter under test, the peak of the efficiency is obtained for I_L= 4 μA, corresponding to I_L/I_{sat}=7.3 (considering I_{sat} = 550 nA).

The transient nature of the circuit start-up for V_{DD}=40 mV and I_L=3 μA is shown in Fig. 82 (a). As can be seen, the circuit takes less than 2 ms to stabilize at around V_{out} = 1.1 V. The voltage at the two complementary oscillator outputs as well as at the converter output for V_{DD} = 30 mV and I_L = 1 μA, measured with the Tektronix MDO4104-6 oscilloscope, are shown in Fig. 82 (b). It should be noted that due to the oscilloscope probe impedance, the $V_{DD,min}$ deviated slightly in relation to the result shown in Fig. 81.

The main results obtained with the external inductor design are presented in Table 12.

5.4 THE OFF-THE-SHELF CONVERTER DESIGN

In order to demonstrate the possibility of boosting voltages below kT/q, a step-up converter which is able to raise the voltage level from 10 mV to 1V for a load current of 100 nA was designed. The

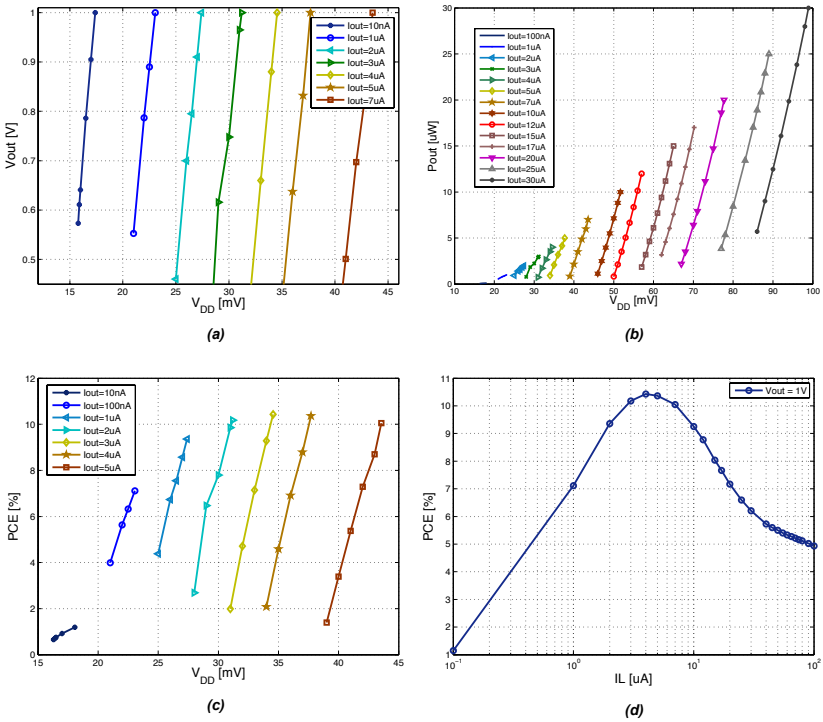


Figure 81: Experimental measurements for step-up converter with external inductors: (a) output voltage; (b) output power; and (c) power converter efficiency, in terms of the supply voltage ($V_{DD} = V_{in}$). (d) Power converter efficiency in terms of I_L , for V_{out}=1V.

schematic diagram of the two-stage ESRO connected to the Dickson converter is shown in Fig. 83. Using zero-VT transistors of the IBM 130 nm technology with W/L=1500 μm/420 nm for the oscillator, off-the-shelf inductors and Schottky diodes, the circuit can start up from V_{DD} = 3.8 mV, while providing a dc output voltage of 150 mV. The photograph of the prototype implemented with SMD passives is shown in Fig. 84. A micrograph of the oscillator transistors, mounted on the board using a plastic QFN package, is shown in the lower part of Fig. 84.

High-Q inductors (L_1 and L_2 in Fig. 83) were used to boost the oscillator output voltage. The inductor values characterized at 600 kHz were: L_1=9.5 μH, quality factor Q_{L1} ≈80, resonance frequency, f_{rL1} ≈150 MHz, L_2=950 μH, Q_{L2} ≈80, and f_{rL2} ≈2.1 MHz.

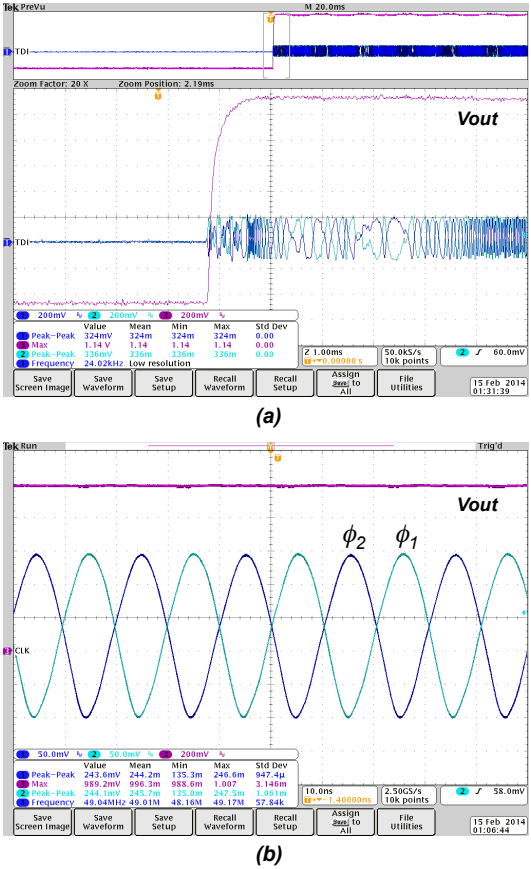


Figure 82: Oscilloscope waveforms of the step-up converter with external inductors. (a) Start-up for V_{DD} = 40 mV and I_L = 3 μA; (b) Steady-state operation for V_{DD} = 30 mV and I_L = 1 μA.

Based on Fig. 85, which represents equation (4.25), it is possible to define the number of stages that matches the design specifications for V_{out} and I_L/I_{sat}. As can be seen in the figure, the effect of the increment of the diode saturation current (which represents the decrement of I_L/I_{sat}), besides increasing the output voltage, is essential for decreasing the minimum peak amplitude for a required output voltage.

As a way to reduce the converter drop-out and to decrease the minimum voltage for starting up the oscillator a three-stage Dickson charge pump was built using commercial Schottky diodes with I_{sat}=90 nA and n=1. Schottky diodes were used due to their higher drive ca-

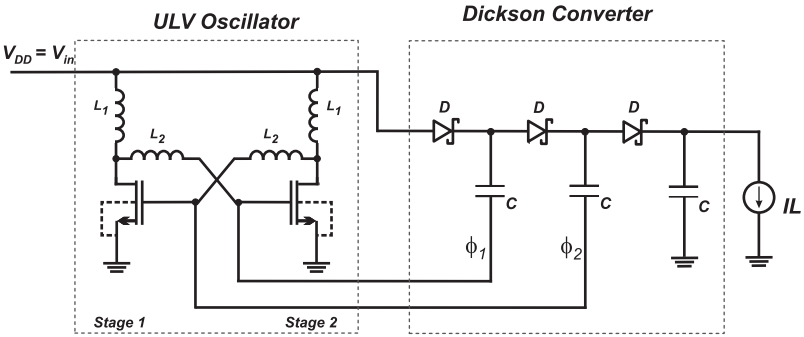


Figure 83: Schematic diagram of the off-the-shelf step-up converter.

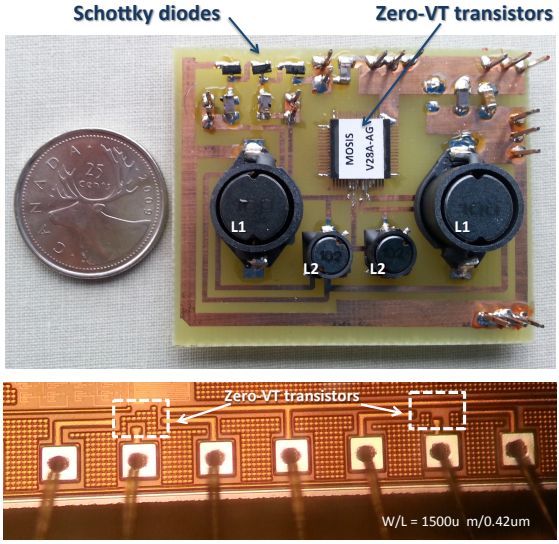


Figure 84: Photograph of the step-up converter prototype. The bottom part shows the micrograph of the zero-VT transistors implemented in the 130 nm process.

pability compared to standard pn-junction diodes whose saturation current is typically a few nA. Since the main role of the converter is to decrease the minimum operating voltage as much as possible, a small number of stages was selected (in order to reduce the diode losses), that is, the minimum sufficient to boost the output voltage to 1V. Thus, as Fig. 85 shows, for $N = 3$, the converter output reaches 1V, for an oscillator amplitude of 300 mV, a value appropriate for the

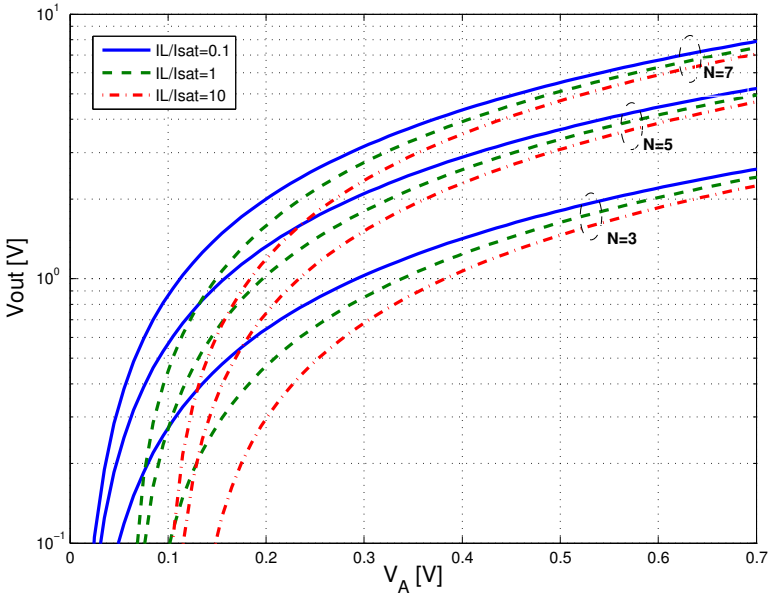


Figure 85: Calculated output voltage (from (4.25)) *vs.* peak amplitude V_A for I_L/I_{sat} = 0.1, 1, and 10 and N = 3, 5 and 7. For the calculations in this figure, V_{in} = 10 mV, ϕ_t = 25.7 mV and n = 1.

implemented oscillator, and a load current I_L/I_{sat}=0.1, or equivalently I_L=9 nA.

The data related to the dependence of the converter output voltage (V_{out}), the output power (P_{out}) and the power converter efficiency (PCE) on the supply voltage ($V_{in} = V_{DD}$) for load currents ranging from 10 nA to 8 μA, determined experimentally using the prototype shown in Fig. 84, are shown in Fig. 86. As can be seen, the converter can reach V_{out} = 1 V at V_{in} = 10 mV and I_L = 100 nA. Considering the case in which the load current is 1 μA, the capability to drive a load of 1μW is reached for V_{in} = 25 mV. Note that, with V_{DD} smaller than 95 mV, the system can drive a load of 10 μW.

The transient characteristics of the converter are illustrated in Fig. 87, for V_{DD} = 25 mV and I_L = 120 nA (Fig. 87 (a)), and for V_{DD} = 11 mV and I_L = 110 nA (Fig. 87 (b)).

A comparison between the experimental output voltage obtained with the prototype shown in Fig. 84 and that calculated from (4.25) can be seen in Fig. 88. For the calculation of V_{out}, the value

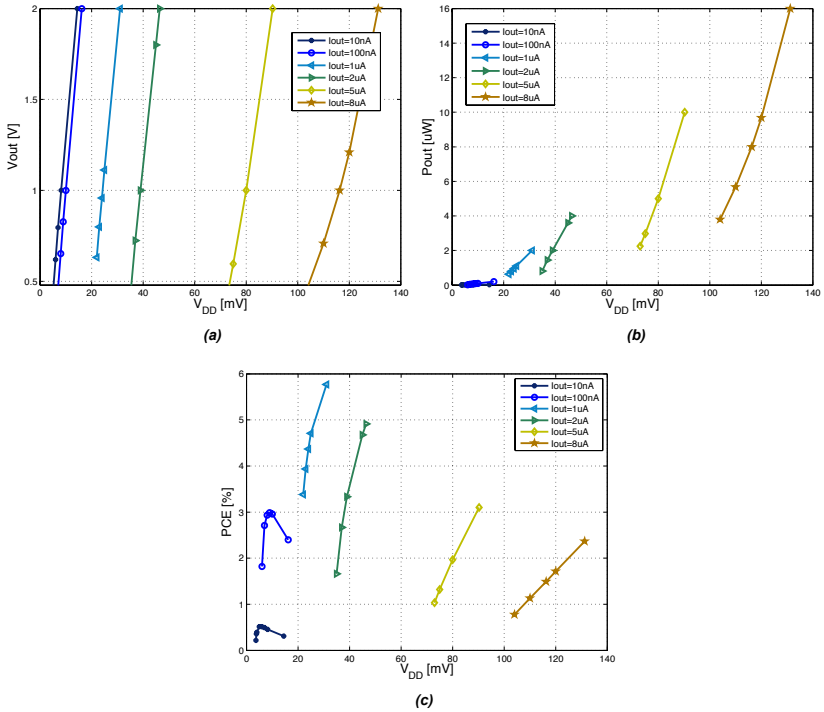


Figure 86: Experimental (a) output voltage, (b) output power and (c) power converter efficiency of the off-the-shelf converter for load currents ranging from 10 nA to 8 µA. All curves are plotted in terms of the supply voltage ($V_{DD} = V_{in}$).

of V_P was taken as the average value of the amplitudes of the two oscillator outputs, since the oscillator presented slightly unbalanced outputs, as shown in Fig. 87. Since the measured values of V_A and V_{out} in Fig. 88 were obtained with the oscilloscope, due to the load inserted by the oscilloscope probe (as previously mentioned), the output voltage was slightly different to that presented in Fig. 86.

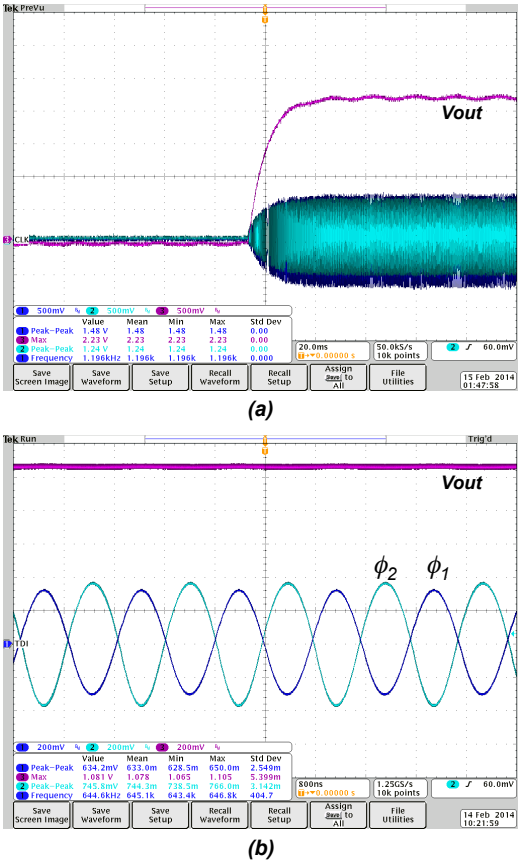


Figure 87: Waveforms of the off-the-shelf design. (a) for V_{DD} = 25 mV and I_L = 120 nA; (b) for V_{DD} = 11 mV and I_L = 110 nA.

5.5 COMPARISON BETWEEN THE CONVERTER DESIGNS

5.5.1 Comparison between the Implemented Designs

In this study, three versions of the topology shown in Fig. 68 for ultra-low voltage operation were implemented. The design space was explored considering the frequency of operation and the area, demonstrating the possibility of boosting extremely low voltages with a fully-integrated, semi-integrated, and an off-the-shelf design.

The main parameters of the devices employed in the three de-

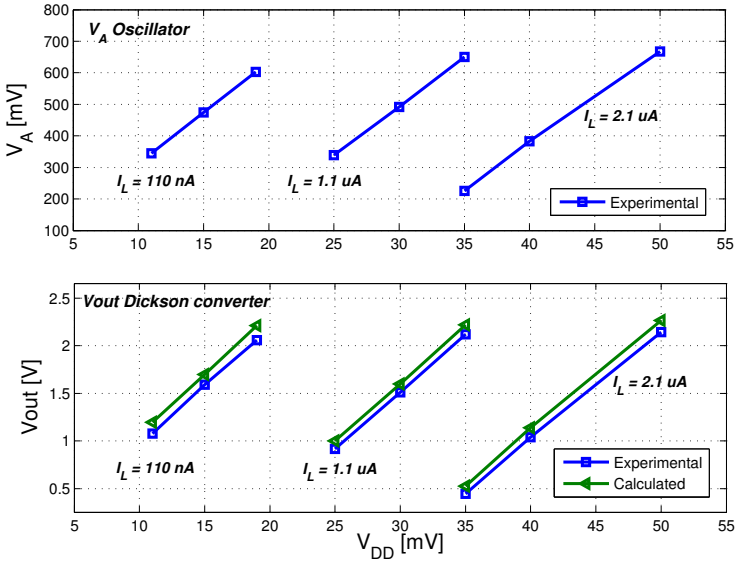


Figure 88: Oscillator peak voltage and converter output voltage *vs.* supply voltage. The experimental values were measured from the prototype shown in Fig. 84 and the calculated V_{out} was obtained from (4.25).

signs are summarized in Table 11. A comparison of the designs implemented is given in Table 12.

5.5.2 Comparison with Some State-of-the-Art Designs

In recent years several topologies and techniques have been proposed in order to start up DC-DC converters with less than 100 mV using, for example, a mechanical switch [33], a post-fabrication tuned oscillator [28] or an external transformer [59]. The minimum voltage required to start up the converters in [28], [33], [59] is around 35 mV, including the extra cost associated with the use of external devices, such as inductors and capacitors. A comparison between previous state-of-the-art research and our study with regards to the minimum start-up voltage and the design characteristics is shown in Table 13. A second comparison between studies of the same nature as that reported herein, composed of either voltage multipliers or charge pumps, is given in Table 14.

Table 11: Characteristics of the devices employed in the ULV step-up converters implemented in this thesis.

	Oscillator		Charge Pump
Fully-Integrated Design	W/L=500μm/0.42μm V_T = 46 mV g_{md} = 7.08 mA/V n = 1.2	$^*L_1$ = 18.8nH $^*Q_1$ = 8.7 $^*L_2$ = 66 nH $^*Q_2$ = 8.1	W/L=4.2μm/0.42μm $^*I_{sat}$ = 550 nA $^*n$ = 1.4 $^*C$ = 2 pF
External Inductor Design	W/L=2000μm/0.42μm V_T = 32 mV g_{md} = 19 mA/V n = 1.1	L_1 = 220 nH Q_1 = 58 L_2 = 594 nH Q_2 = 67	W/L=4.2μm/0.42μm $^*I_{sat}$ = 550 nA $^*n$ = 1.4 $^*C$ = 2 pF
Off-the-Shelf Design	W/L=1500μm/0.42μm V_T = 24 mV g_{md} = 20.5 mA/V n = 1.2	L_1 = 9.8 μH Q_1 = 100 L_2 = 980 μH Q_2 = 55	Schottky diode I_{sat} = 90 nA n = 1 C = 2.2 nF

* Value obtained by simulation.

Table 12: Experimental results for the ULV step-up converters implemented in this study.

	Fully Integrated Design	External Inductor Design	Off-the-Shelf Design
f_{osc}	550 MHz	50 MHz	600 kHz
Area*	1 mm^2	20 mm^2	660 mm^2
Characteristcs at start-up (I_L = 10nA)	$V_{DD,min}$=73 mV I_{DC}=2 mA	$V_{DD,min}$=15.8 mV I_{DC}= 0.5 mA	$V_{DD,min}$=3.8 mV I_{DC}=0.13 mA
Characteristcs at V_{DD} = 50 mV, V_{out}=1 V	-	I_L = 9.37μA PCE = 9.41 %	I_L=2.77μA PCE = 2.8 %
Characteristcs at V_{DD} = 100 mV, V_{out}=1V	I_L = 3.27 μA PCE = 1 %	I_L = 30.6 μA PCE = 6.2 %	I_L=6.61μA PCE = 1.9 %
Characteristcs at V_{out}=1V, I_L=1 μA	$V_{DD,min}$=86 mV I_{DC}=2.8 mA	$V_{DD,min}$=23 mV I_{DC}=0.61 mA	$V_{DD,min}$=24.5 mV I_{DC}=0.92 mA

* Area of the IC with PADs + area of the external devices.

As can be seen in Tables 13 and 14, the proposal described in this thesis allows a very important reduction in the minimum operational voltage of electronic step-up converters to be achieved. To the best of our knowledge, the results presented herein represent the low-

est supply voltage ever reported for a step-up converter in a conventional CMOS technology, at room temperature.

Table 13: Comparison between state-of-the-art converter designs. Designs I, II and III refer to fully-integrated, integrated with external inductors and off-the-shelf designs, respectively.

Ref.	$V_{DD,min}$	Topology	Process	Characteristics
[10]	95 mV	Dickson + Inductive boost	65 nm	Post-layout tuning + External inductor and capacitor
[28]	40 mV	Inductive boost	0.13 μm	External transformer
[33]	35 mV	Inductive boost	0.13 μm	Mechanical switch + External inductor and capacitor
[59]	80 mV	Dickson + Inductive boost	65 nm	Post-layout tuning + External inductor and capacitor
[62]	50 mV	AC/DC multiplier +Inductive boost	65 nm	External inductor and capacitor
[66]	600 mV	Inductive boost	0.13 μm	External capacitors or previously charged batteries
[67]	600 mV	Switched capacitor	-	Fully integrated
[68]	270 mV	Switched capacitor	0.13 μm	Fully integrated
[69]	100 mV	AC/DC multiplier	0.18 μm	Fully integrated (simulated results)
Design I	73 mV	Dickson	0.13 μm	Fully integrated
Design II	15.8 mV	Dickson	0.13 μm	Integrated with external inductors
Design III	3.8 mV	Dickson	0.13 μm	Off-the-shelf-devices

Table 14: Details of the design of the charge pumps and AC/DC multipliers described in Table 13.

Ref.	V_{out}/V_{in}	I_L	N	f_{osc}	Topology
[10]	460mV/95mV	10.5 nA	20	330 kHz	Dickson
[59]	500mV/80mV	4 nA	30	200 kHz	Dickson
[62]	300mV/50mV	500 nA	12	30 MHz	AC/DC multiplier
[69]	1.3V/150mV	10 μA	-	200 MHz	AC/DC multiplier
[69]	1.02V/90mV	100 μA	4	50 MHz	Dickson
Design I	1V/86mV	1 μA	11	550 MHz	Dickson
Design II	1V/23mV	1 μA	11	50 MHz	Dickson
Design III	1V/10mV	100 nA	3	600 kHz	Dickson

6 SUMMARY AND CONCLUSIONS

6.1 SUMMARY

In order to investigate the minimum supply voltage for MOSFET oscillators, three topologies were studied. Based on a ring topology with a LC load, the inductive ring oscillator - IRO is theoretically capable of operating with one half of the voltage supply limit of digital circuits, but the enhanced swing ring oscillator - ESRO and the enhanced swing Colpitts oscillator ESCO, do not present a hard limit for the minimum supply voltage. Theoretical expressions derived for the oscillation frequency, minimum transistor gain and minimum supply voltage to start up the oscillators generate a theoretical framework suitable to design oscillators operating at very low voltages.

To check the operation of the oscillators at ultra-low-voltages, six prototypes were implemented. Four fully-integrated designs, fabricated using the IBM 130 nm technology, generate oscillations from voltage supplies as low as 86, 53, 46 and 30 mV employing the ESCO, IRO (seven stages), IRO (two stages) and ESRO arrangements, respectively. Using zero-VT transistors fabricated in the same process and off-the-shelf passives, two prototypes employing the ESCO and ESRO topologies can start up from voltage supplies of 15 and 3.5 mV. It is worth noting the high magnitude swing presented for those designs. Considering the two ESRO prototypes, a peak-to-peak amplitude of 500 mV at the oscillator outputs is obtained for supply voltages of 77 and 8 mV, employing a fully-integrated and an off-the-shelf designs, respectively.

The application of energy harvesting also was addressed in this study. Based on the physical parameters of the diode and on the load current, expressions for the output voltage, input resistance and the power converter efficiency were derived for the Dickson charge pump, generating the theoretical basics to design boost converters operating from voltages as low as the thermal voltage.

The possibility of boosting ultra-low-voltages to higher voltage levels necessary to supply the current electronics has been verified in this thesis. Built upon the Dickson charge pump and on the ULV ESRO, three prototypes of step-up converters were implemented. For input dc voltage levels of 86 and 23 mV, a fully integrated prototype, and another integrated prototype except for the external inductors, respectively, can generate a dc level of 1V for a load current of 1 μA. For

a load current of 100 nA, a prototype built with off-the-shelf devices can reach 1 V at the output for an input voltage of 10 mV.

Until the writing of this manuscript, this study generated 3 journal papers (two of then published and one waiting for the revising process), seven papers published in proceedings of international conferences and six works presented in workshops in the United States, Mexico and Brazil. Also, the paper "10 mV - 1 V Step-up converter for energy harvesting applications" received the best paper award of the 27th SBCCI that was held in Aracaju, Brazil.

6.2 CONCLUSIONS

In this thesis, oscillators and boost converters operating at ultra-low voltage have been described. Using an exponential law for the non-linear device (diode and MOSFET), it was found that the minimum supply voltage for the proper operation of these circuits can be below the Meindl limit for logic inverters.

The proper operation of electronic circuits is dependent on the voltage gain. Voltage gain, as a consequence of the nonlinearity of transistors, requires a minimum supply voltage to emerge with the necessary strength. For ideal MOS transistors ($n = 1$) operating in weak inversion in the common-source configuration, the intrinsic gain equals unity for V_{DS} =(ln2)kT/q, but the intrinsic gain of the common-gate configuration is always greater than unity. MOSFET oscillators, when appropriately designed, can operate with supply voltages well below (ln2)kT/q. To this end, one option is the use of the MOSFET in the common-gate configuration, as in the case of the enhanced swing Colpitts oscillator. A second option is the use of the transistor in the common-source topology and boost the voltage gain with an appropriate LC circuit, as in the case of the enhanced swing ring oscillator.

The use of zero-VT MOSFET for the operation of ULV analog circuits is proposed herein. Experimental prototypes built with off-the-shelf passive devices and those which are fully-integrated start up oscillations from voltages as low as 3.5 and 30 mV, respectively. To the best of our knowledge, this thesis presents the lowest supply voltage for oscillators ever reported.

The operation of oscillators with supply voltages below the thermal voltage has been shown to be an alternative for harvesting energy from very-low-voltage sources. Based on the enhanced swing ring oscillator and on the Dickson charge pump, the possibility of

generating a dc level of 1 V at an input voltage as low as 10 mV was experimentally verified. To the best of our knowledge, this study presents the lowest supply voltage for step-up converters ever reported.

The results reported in this thesis, besides verifying the operation of analog circuits well below the supply voltage limit for digital circuits, the Meindl limit, open new opportunities concerning ULV and ULP electronics. As was demonstrated herein, there is plenty of room for ultra-low-voltage CMOS electronics below the Meindl limit for logic.

ANNEX A – THE TRANSISTOR MODEL

The MOSFET model used throughout this study is based on the Unified Current Control Model (UICM) [70], [71], [72], which represents the device behavior in all regimes of operation. In this model the current I_D is written as a combination of the forward (I_F) and reverse (I_R) currents as

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{A.1}$$

where i_f and i_r are the normalized forward and reverse currents, respectively, I_S is the specific current, defined as $I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L}$, μ is the effective mobility, C'_{ox} is the oxide capacitance per unit area, n is the slope factor, ϕ_t is the thermal voltage and W/L is the aspect ratio of the transistor.

The relation between the voltages and currents is given by

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1 \right) \right] \tag{A.2}$$

$$V_P = \frac{V_G - V_T}{n} \tag{A.3}$$

where V_P is the pinch-off voltage and V_T is the threshold voltage. Voltages are referenced to bulk. The differentiation of the drain current (I_D) with respect to V_S, V_D, and V_G allows us to write

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = \frac{2I_S}{\phi_t} \left(\sqrt{1 + i_f} - 1 \right) \tag{A.4}$$

$$g_{md} = \frac{\partial I_D}{\partial V_D} = \frac{2I_S}{\phi_t} \left(\sqrt{1 + i_r} - 1 \right) \tag{A.5}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{g_{ms} - g_{md}}{n} \tag{A.6}$$

The drain-source voltage V_{DS} can be expressed in terms of i_f and i_r

using (A.2).

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \tag{A.7}$$

The resulting expression for V_{DS} can be written in terms of the transconductances making use of (A.4) and (A.5), which yields

$$\frac{V_{DS}}{\phi_t} = \frac{\phi_t}{2I_S}(g_{ms} - g_{md}) + \ln\frac{g_{ms}}{g_{md}} \tag{A.8}$$

Now, considering weak inversion operation only, (A.8) can be written as

$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}} \tag{A.9}$$

The simplified small signal model of the MOSFET is shown in Fig. 89 [72].

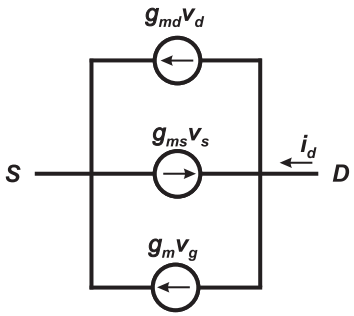


Figure 89: Small signal model of the MOSFET. The bulk is ac grounded.

ANNEX B – CHARACTERIZATION OF THE ZERO-VT TRANSISTOR

In this appendix an experimental characterization of some zero-VT transistors used in this study is presented.

B.1 I_D $VS.$ V_{DS} CHARACTERISTICS

The I_D *vs.* V_{DS} characteristics of the zero-VT transistor with W/L=2500 μm/420 nm, with V_{GS} ranging from -200 to 250 mV, are shown in Fig. 90 in the linear and logarithmic scales.

B.2 EXTRACTION OF V_T, I_S AND N

The main characteristics of the MOS transistor (V_T, I_S, and n) used in calculations throughout this paper were extracted employing a procedure based on the transconductance-to-current ratio (g_m/I_D). Details on the extraction are given in [72] and [73], but briefly V_T, I_S, and n are extracted from I_D - V_G measurements obtained with the circuit shown in the lower part of Fig. 91.

As demonstrated in [72] and [73], V_T is the gate voltage at which the condition $g_m/I_D = 0.53.(g_m/I_D)_{max}$ holds for $V_{DS} = \phi_t/2$. Also, the specific current $I_S = 1.163.I_D^*$, I_D^* being the drain current determined when $V_G = V_T$. Since $(g_m/I_D)_{max} = 1/n\phi_t$, the slope factor n is easily extracted from the peak of the g_m/I_D curve and the temperature. Even though n decreases slightly with increasing gate voltage, it has been assumed that, for the calculations in this paper, n can be considered independent of V_G.

The simulated variations in the values of V_T and I_{SQ} for four W/L ratios are shown in Table 15. The sheet normalization current I_{SQ} is defined as $I_{SQ} = I_S/(W/L)$. The values in the table were extracted from the g_m/I_D procedure.

B.3 EXTRACTION OF THE TRANSCONDUCTANCES

The transistor transconductances can be extracted using a procedure based on the I_D x V_D curve obtained with the circuit in the

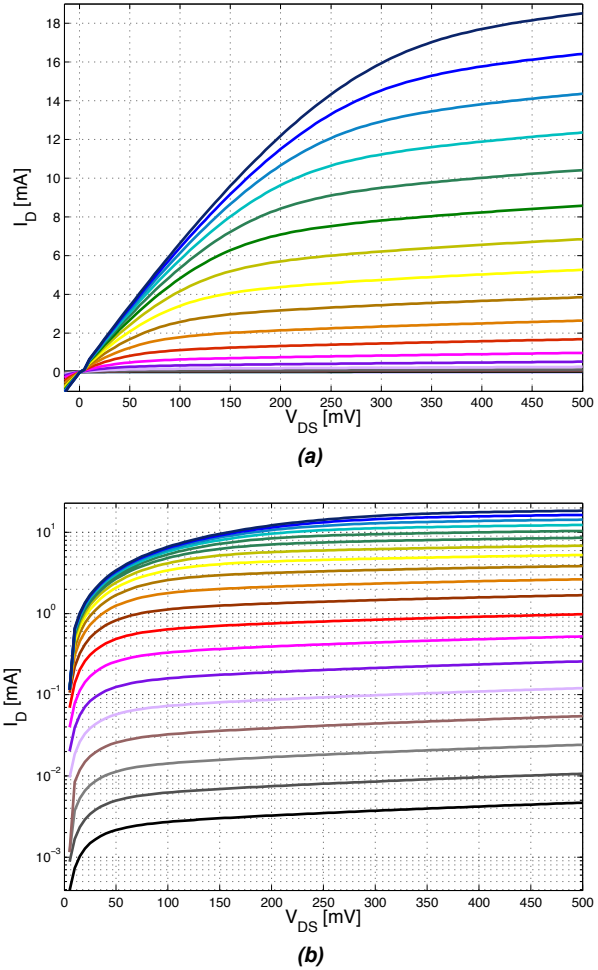


Figure 90: I_D *vs.* V_{DS} ($V_S = V_B$) for a zero-VT transistor for V_{GS} ranging from -200 to 250 mV, with an interval of 25 mV. (a) linear characteristics; (b) logarithmic characteristics.

bottom part of Fig. 92.

Considering the dc polarization used in the oscillators presented herein, for a given V_G value ($V_G = V_{DD}$), the drain transconductance, $g_{md} = \partial I_D/\partial V_D$, can be obtained for the condition $V_G = V_D = V_{DD}$. Due to the transistor symmetry, the source transconductance is equal to g_{md} at V_{DS}=0, that is g_{ms}=$g_{md}|_{VDS=0}$.

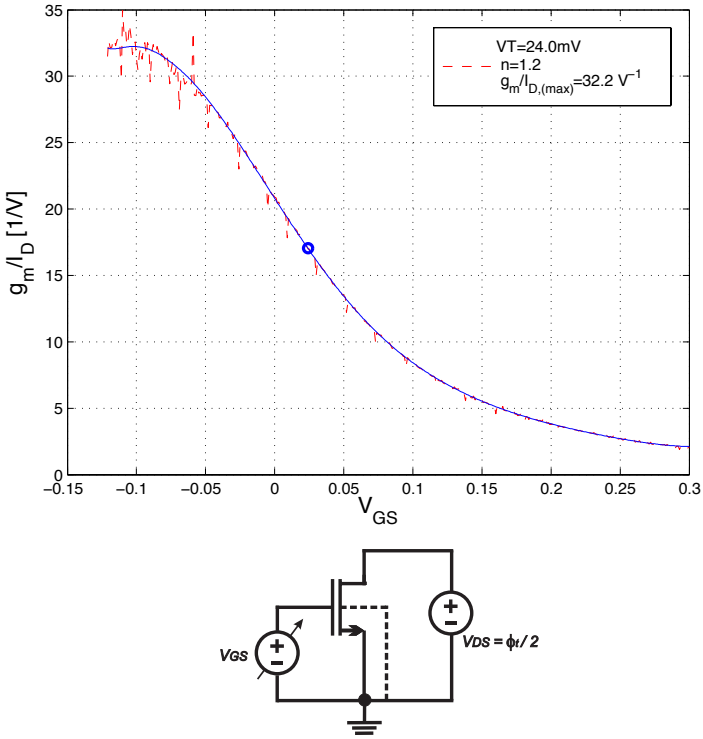


Figure 91: Experimental g_m/I_D curve and the circuit configuration for extracting the main static MOSFET parameters. To obtain this figure, a zero-VT transistor with W/L=1500 μm/420 nm was used.

Table 15: Simulated values for V_T and $I_{SQ} = I_S/(W/L)$ of the zero-VT transistor, for some W/L aspect ratios.

W/L	3μm/420nm	6μm/840nm	12μm/1.68μm	48μm/6.72μm
V_T	88 mV	41.3 mV	16.4 mV	-5.9 mV
I_{SQ}	126 μA	175 μA	204.5 μA	230.4 μA

This procedure was used to determine the behavior of the source and drain transconductances (which were used in the design of the oscillators), and the experimental transconductances of the drain and source as well as the voltage gain in the common-gate configuration (g_{ms}/g_{md}) of the zero-VT transistor with W/L=1500 μm/420 nm in terms of V_{DD} are shown in Fig. 92.

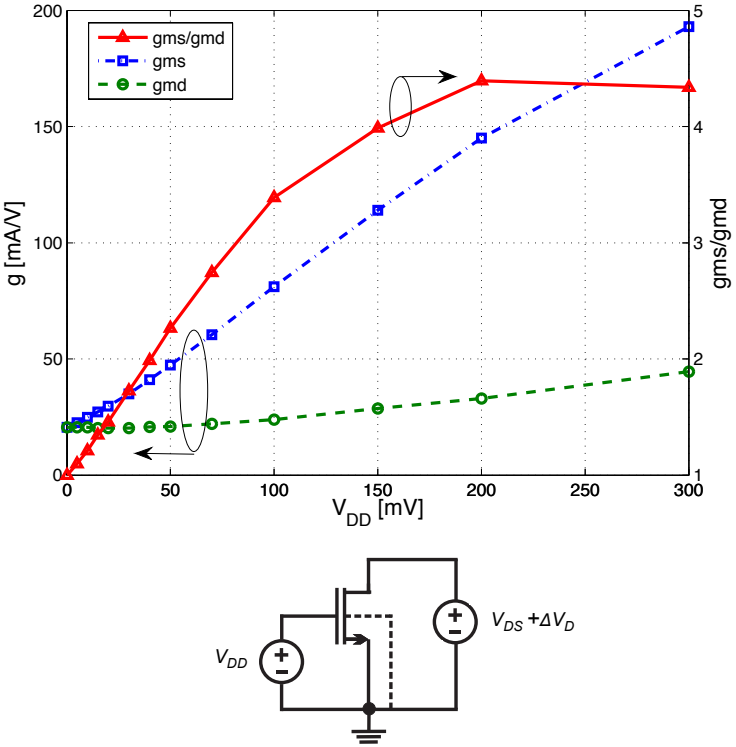


Figure 92: Experimental drain and source transconductances of the zero-VT transistor with W/L=1500 μm/420 nm, for V_{DD} = 0 to 300 mV.

In this regard, it should be noted that the drain transconductance of the zero-VT transistor operating at low voltages with $V_G = V_D$ is almost bias-independent. To demonstrate this, let it us consider the transistor model described in Appendix A, biased at $V_S = V_B$ and $V_G = V_D = V_{DD}$. Assuming that n=1, (A.2) can be written as

$$\frac{-V_T}{\phi_t} = \left[\sqrt{1+i_r} - 2 + \ln\left(\sqrt{1+i_r} - 1\right)\right] \qquad \text{(B.1)}$$

Thus, the reverse inversion level (i_r) is, at least for low voltages, almost independent of the gate voltage. If, in addition, the value for V_T is exactly zero, the solution of (B.1) corresponds to $i_r = 3$, and the value

of g_{md} calculated from (A.5) is

$$g_{md} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_r}-1\right) = \frac{2I_S}{\phi_t} \tag{B.2}$$

Therefore, in a first-order approximation, the g_{md} value is dependent only on the specific current I_S, defined in Appendix A, and the thermal voltage ϕ_t. Equation (B.2) can be used for a back-of-the-envelope calculation of g_{md}.

B.4 CHARACTERIZATION OF THE ZERO-VT AS A DIODE

A comparison between the zero-VT and the standard transistors, both connected as a diode (bottom part of Fig. 93) is shown in Fig. 93. As can be seen in the graphs, for low V_D, the zero-VT MOSFET, when connect as a diode, presents a saturation current more than two orders of magnitude higher than the conventional transistor available in the IBM 130nm process for the same area.

The experimental characterization of the zero-VT transistor with W/L=2500μm/420nm connected as a diode, for V_S ranging from 0 to -200 mV, is shown in Fig. 94.

B.5 CHARACTERIZATION OF THE ZERO-VT TRANSISTORS EMPLOYED IN THIS STUDY

The experimental characterizations of some zero-VT transistors used in the designs described in this thesis are shown in Table 16.

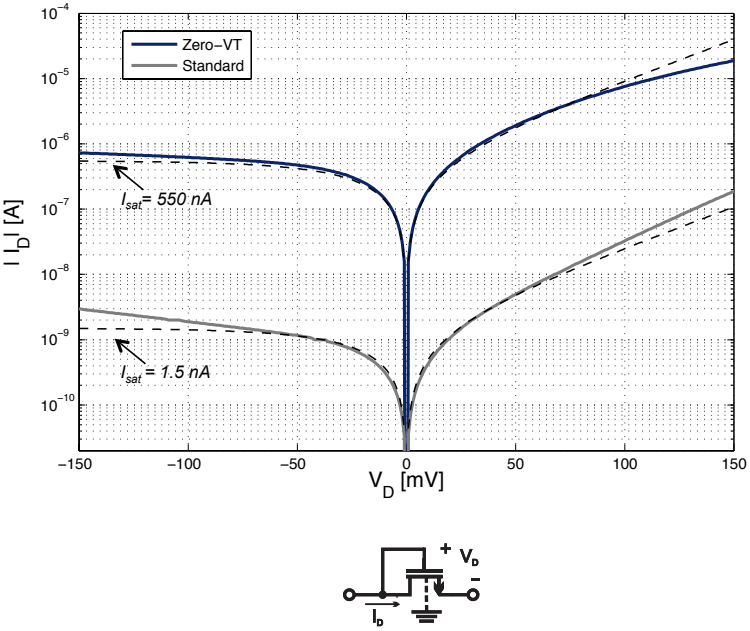


Figure 93: Simulated I_D *vs.* V_D characteristics of the standard and zero-VT transistors available in the 130 nm technology, both connected as diodes with W/L=4.2μm/420nm. The dashed line represents the ideal Shockley behavior given by $I_D = I_{sat}(e^{V_D/n\phi_t} - 1)$, considering n=1.4 for both transistors.

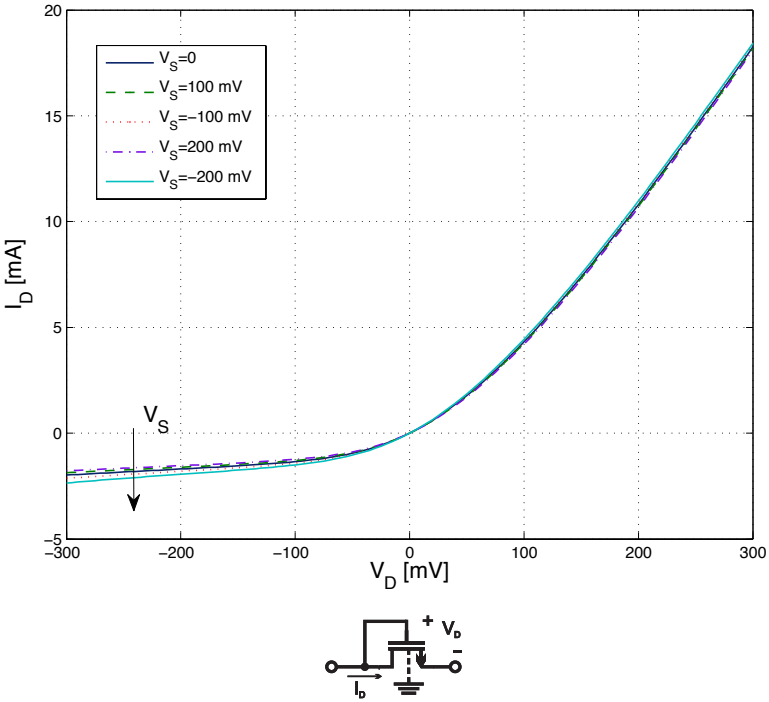


Figure 94: Experimental I_D *vs.* V_D characteristics of the zero-VT transistor with W/L=2500μm/420nm.

Table 16: Experimental characterization of the zero-VT transistors.

Transistor	Experimental Characteristics		Application
ALD 1108A	V_T = 59 mV	$^{*}g_{md}$=315μA/V	
24 MOSFETs	I_S = 11.2 μA		ESCO - off
	n = 1.6		
W = 30 x 5 μm	V_T = 22 mV	$^{*}g_{md}$=2.3mA/V	IRO - FI
L = 480 nm	I_S = 44 μA	$^{**}g_{md}$=2.6mA/V	7-stage
	n = 1.2		
W = 500 x 5 μm	V_T = -10 mV	$^{*}g_{md}$=24mA/V	
L = 420 nm	I_S = 277 μA	$^{**}g_{md}$=26mA/V	ESCO - off
	n = 1.2		
W = 300 x 5 μm	V_T = 24 mV	$^{*}g_{md}$=20.5mA/V	ESCO - FI
L = 420 nm	I_S = 450 μA	$^{**}g_{md}$=23.9mA/V	ESRO - off
	n = 1.2		Converter - off
W = 30 x 6 μm	V_T = 53 mV	$^{*}g_{md}$=2mA/V	IRO - FI
L = 420 nm	I_S = 71 μA	$^{**}g_{md}$=2.5mA/V	2-stage
	n = 1.2		
W = 25 x 20 μm	V_T = 46 mV	$^{*}g_{md}$=7.08mA/V	
L = 420 nm	I_S = 225 μA		ESRO - FI
	n = 1.2		
W = 400 x 5 μm	V_T = 32 mV	$^{*}g_{md}$=19mA/V	Converter
L = 420 nm	I_S = 489 μA	$^{**}g_{md}$=21mA/V	with external
	n = 1.1		inductors

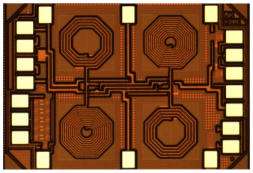
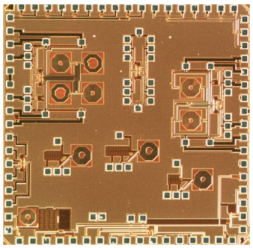
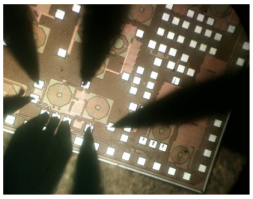
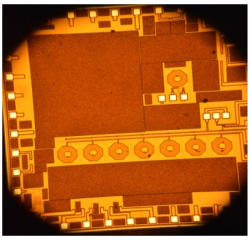
* at V_{DD}= 10 mV; ** at V_{DD}= 100 mV

FI - refers to the fully-integrated design

off - refers to the off-the-shelf design

ANNEX C – DESIGNED CHIPS

Table 17: Chips designed during the doctoral research.

Die Microphotograph	*Characteristics*	*Implemented Circuits*	*Charac. Lab*
	**Chip 4 - Polystim / CMC** ▪ Submitted: July 2013 ▪ Chip area: 1.2 mm^2 ▪ Package: - CFP 24 - LCC 28	▪ Fully Integrated step-up converter; ▪ Semi-integrated step-up converter, wire-bonded with external inductors; ▪ Zero-VT - W/L=2000µm / 0.42µm.	▪ Polystim - Polytechnique Montreal
	**Chip 3 - LCI multi project run** ▪ Submitted: Feb. 2013 ▪ Chip area: 16 mm^2 ▪ Package: - LCC 68	▪ Fully Integrated 2-stage IRO; ▪ Fully Integrated 2-stage ESRO; ▪ Zero-VT - W/L=500µm / 0.42µm; - W/L=180µm / 0.42µm.	▪ LCI – UFSC ▪ Polystim - Polytechnique Montreal
	**Chip 2 - LCI multi project run** ▪ Submitted: Aug. 2012 ▪ Chip area: 16 mm^2 ▪ Package: - QFN 64	▪ Fully Integrated ESCO; ▪ Zero-VT - W/L=1500µm / 0.42µm - Used in the off-the-shelf ESRO - Used in the off-the-shelf step-up converter.	▪ LCI – UFSC ▪ Polystim - Polytechnique Montreal
	**Chip 1 - LCI multi project run** ▪ Submitted: May 2011 ▪ Chip area: 16 mm^2 ▪ Package: - DIP 40	▪ Fully Integrated 7-stage IRO; ▪ Zero-VT - W/L=2500µm / 0.42µm - Used in the off-the-shelf ESCO.	▪ LCI – UFSC

ANNEX D – PUBLICATIONS

A list of papers submitted or published during the doctoral research period is shown given below.

D.1 JOURNAL PAPERS

- M. B. Machado, M. C. Schneider, and C. Galup-Montoro, "Fully integrated inductive ring oscillators operating at V_{DD} below $2kT/q$," submitted to *Springer Analog Integrated Circuits and Signal Processing Journal*, in October 2013.

- M. B. Machado, M. C. Schneider, and C. Galup-Montoro, "On the minimum supply voltage for MOSFET oscillators," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 62, no. 2, pp. 347-357, Fev. 2014.

- C. Galup-Montoro, M. C. Schneider and M. B. Machado, "On the ultra-low-voltage operation of CMOS analog circuits: amplifiers, oscillators, and rectifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59. No.12, pp. 932-36, Dec. 2012.

D.2 CONFERENCE PAPERS

- M. B. Machado, M. Sawan, M. C. Schneider, and C. Galup-Montoro, "10 mV - 1V Step-up converter for energy harvesting applications," in Proc. of *27th Symposium on Integrated Circuits and Systems Design*, (SBCCI), Aracaju, Brazil, Sept. 2014.

  The paper received the best paper award of the 27th SBCCI.

- M. B. Machado, M. C. Schneider, M. Sawan, and C. Galup-Montoro, "Fully integrated 86 mV - 1V step-up converter for energy harvesting applications," in Proc. *12th IEEE International New Circuits and Systems Conference*, (NEWCAS), Trois-Rivières, Canada, Jun. 2014.

- M. B. Machado, M. C. Schneider, and C. Galup-Montoro, "Design of a fully integrated Colpitts oscillator operating at V_{DD}

below $4kT/q$," in Proc. *5th IEEE Latin American Symp. on Circ. and Systems* (LASCAS), Santiago, Chile, Feb. 2014.

- C. Galup-Montoro, M. C. Schneider, L. Carli, and M. B. Machado, "Introductory ultra-low-voltage electronics," in Proc. *7th IEEE Argentine School of Technology and Applications* (EAMTA), Buenos Aires, p. 1-8, 2013.

- M. B. Machado, M. C. Schneider, C. Galup-Montoro, "Analysis and design of ultra-low-voltage inductive ring oscillators for energy-harvesting applications," in Proc. *4th IEEE Latin American Symp. on Circ. and Systems* (LASCAS), Cusco, Peru, Feb. 2013.

- F. R. Sousa, M. B. Machado and C. Galup-Montoro, "A 20 mV Colpitts Oscillator powered by a thermoelectric generator," in Proc. *IEEE International Symposium on Circuits and Systems* (ISCAS), Seoul, Korea, pp. 2035-2038, May 2012.

- M. B. Machado, O. F. Siebel, M. C. Schneider, C. Galup-Montoro, "MOSFET threshold voltage: definition, extraction, and applications," in Proc. *The Nanotechnology Conference and Expo* (Nanotech), Boston, USA, pp. 710-713, Jun. 2011.

D.3 WORKSHOP PRESENTATIONS

- C. Galup-Montoro, M. C. Schneider and M. B. Machado, "Modeling and parameter extraction of zero-VT MOSFETs for ultra-low-voltage operation," *MOS Modeling and Parameter Extraction Working Group* (MOS-AK/GSA) , San Francisco, USA, Dec. 2012.

- C. C. Santos Junior, D. Deoti, R. M. da Ponte, M. B. Machado, and M. C. Schneider, "Zero-threshold-voltage MOSFETs: a survey," *12th Microelectronics Students Forum*, (SForum), Brasilia, DF, Aug. 2012.

- M. B. Machado, M. C. Schneider and A. Arnaud, "A battery charge monitor topology for implantable medical devices," in Proc. *IBERCHIP XVIII Workshop*, Playa del Carmen, Mexico, pp. 126-130, Feb. 2012.

- C. Galup-Montoro, M. C. Schneider and M. B. Machado, "On the minimum supply voltage for CMOS analog circuits: rectifiers

and oscillators," *MOS Modeling and Parameter Extraction Working Group* (MOS-AK/GSA), Washington DC, USA, Dec. 2011.

- M. B. Machado, T. Oliveira, M. C. Schneider, C. Galup-Montoro, "Direct determination of MOSFET parameters from the I_D versus V_S curve at low V_{DS}," *MOS Modeling and Parameter Extraction Working Group* (MOS-AK/GSA), San Francisco, USA, Dec. 2010.

REFERENCES

[1] Y. Zhang, et al., "A Batteryless 19 μW MICS/ISM-band energy harvesting body sensor node SoC for ExG application," *IEEE J. of Solid-State Circuits*, vol. 48, no.1, pp. 199-213, Jan. 2013.

[2] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, A. P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE J. of Solid-State Circuits*, vol. 45, no. 4, pp. 804-816, Apr. 2010.

[3] G. Chen, M. Fojtik, K. Daeyeon, D. Fick, J. Park, M. Seok, M.-T. Chen, Z. Foo, D. Sylvester, and D. Blaauw, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in *IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers* (ISSCC), pp. 288-289, Feb. 2010.

[4] S. Ethier, M. Sawan, "Exponential current pulse generation for efficient very high-impedance multisite stimulation," *IEEE-Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 30-38, Feb. 2011.

[5] J. Olivo, S. Carrara, G. De Micheli, "Energy harvesting and remote powering for implantable biosensors," *IEEE Sensors J.*, vol.11, no.7, pp. 1573-1586, Jul. 2011.

[6] R.J.M. Vullers, R. van Schaijk, I. Doms, C. Van Hoof, R. Mertens, "Micropower energy harvesting," *Solid-State Electronics*, vol. 53, no. 7, pp. 684-693, Jul. 2009.

[7] J. Rabaey, *Low Power Design Essentials*. Springer, New York, 2009.

[8] E. Macci, *Ultra low-Power Electronics and Design*. Springer, New York, 2004.

[9] R. J. M. Vullers, R. V. Schaijk, H. J. Visser, J. Penders, C. V. Hoof, "Energy harvesting for autonomous wireless sensor networks," *IEEE Solid-State Circuits Mag.*, vol. 2, no. 2, pp. 29-38, 2010.

[10] P. H. Chen, K. Ishida, K. Ikeuchi, X. Zhang, K. Honda, Y. Okuma, Y. Ryu, M. Takamiya, T. Sakurai, "Startup techniques for 95 mV step-up converter by capacitor pass-on scheme and V_{TH}-tuned oscillator with fixed charge programming," *IEEE J. of Solid-State Circuits*, vol. 47, no. 5, pp. 1252-1260, May 2012.

[11] J. F. Randall, *Designing indoor solar products*, Wiley, 2005.

[12] C. J. Love, S. Zhang, and A. Mershin, "Source of sustained voltage difference between the xylem of a potted Ficus benjamina tree and its soil," PLoS ONE, vol. 3 no. 8, e2963, Aug. 2008.

[13] V. Leonov, T. Torfs, P. Fiorini, C. Van Hoof, "Thermoelectric converters of human warmth for self-powered wireless sensor nodes," *IEEE Sensors J.*, vol. 7, no. 5, pp. 650-657, May 2007.

[14] S. Wolfson Jr, S. Gofberg, P. Prusiner, and L. Nanis, "The bioautofuel cell: A device for pacemaker power from direct energy conversion consuming autogenous fuel," Trans. Amer. Soc. Artif. Internal Organs, vol. 14, pp. 198–203, 1968.

[15] S. Kerzenmacher, J. Ducrée, R. Zengerle, F. Von Stetten, "Energy harvesting by implantable abiotically catalyzed glucose fuel cells," *Journal of Power Sources*, vol. 182, no. 1, pp. 66-75, Jul. 2008.

[16] S. Kerzenmacher, J. Ducrée, R. Zengerle, F. Von Stetten, "An abiotically catalyzed glucose fuel cell for powering medical implants: reconstructed manufacturing protocol and analysis of performance," *Journal of Power Sources*, vol. 182, no. 1, pp. 66-75, Jul. 2008.

[17] B. I. Rapoport, J. T. Kedzierski, and R. Sarpeshkar, "A glucose fuel cell for implantable brain-machine interfaces," PLoS One, vol. 7 no. 6, e38436, Jun. 2012.

[18] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: a tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 3-29, Jan. 2012.

[19] J. D. Meindl and A. J. Davis, "The fundamental limit on binary switching energy for terascale integration TSI," *IEEE J. of Solid-State Circuits*, vol. 35, no. 10, pp. 1515-1516, Oct. 2000.

[20] R. Swanson and J. Meindl, "Ion-implanted complementary MOS transistors in low-voltage Circuits," *IEEE J. of Solid-State Circuits*, pp. 146-153, Apr. 1972.

[21] A. Bryant et al. "Low-power CMOS at $V_{DD} = 4kT/q$," Device Research Conference, pp. 22-23, Notre Dame, IN, Jun. 2001.

[22] N. Lotze, and Y. Manoli, "A 62 mV 0.13 μm CMOS standard-cell-based design technique using Schmitt-trigger logic," *IEEE J. of Solid-State Circuits*, vol. 47, no. 1 pp. 47-60, Jan. 2012.

[23] L. C. C. Marques, "Switched-MOSFET technique for programmable filters operating at low-voltage supply," PhD. Dissertation, Dept. Elect. Eng. Federal University of Santa Catarina, UFSC, SC, 2002.

[24] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*: Regular Papers, vol. 54, no. 1, pp. 153-166, Jan. 2007.

[25] A. J. Cardoso, L. G. de Carli, C. Galup-Montoro, and M. C. Schneider, "Analysis of the rectifier circuit valid down to its low-voltage limit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no.1, pp. 106-112, Jan. 2012.

[26] *ECT310 datasheet*, Enocean Co., available on-line at: http://www.enocean.com.

[27] *LTC3108 datasheet*, Linear Technology Co., available on-line at: http://www.linear.com.

[28] J.-P. Im, S.-W. Wang, S.-T. Ryu, G.-H. Cho, "A 40 mV transformer-reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting," *IEEE J. of Solid-State Circuits*, vol. 47, no. 12, pp. 3055-3067, Dec. 2012.

[29] Oscillator with super low supply voltage, On-line available http://www.dicks-website.eu/fetosc/enindex.htm, accessed April 16, 2012.

[30] R. Gonzalez, B. M. Gordon, and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," *IEEE J. of Solid-State Circuits*, vol. 32, no. 8, Aug. 1997.

[31] IBM Foundry and Manufacturing Services Education, "Design kit and technology training CMOS8RF," V1700, Oct. 2010.

[32] C. Galup-Montoro, M. C. Schneider, and M. B. Machado, "Ultra-low-voltage operation of CMOS analog circuits: amplifiers, oscillators, and rectifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59. no. 12, pp. 932-36, Dec. 2012.

[33] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage," *IEEE J. of Solid-State Circuits*, vol. 46, no. 1, pp. 333-341, Jan. 2011.

[34] T. Niiyama, P. Zhe, K. Ishida, M. Murakata, M. Takamiya, T. Sakurai, "Dependence of minimum operating voltage (VDD_{min}) on block size of 90-nm CMOS ring oscillators and its implications in low power DFM," in *International Symposium on Quality Electronic Design* (9th ISQED), pp.133-136, Mar. 2008.

[35] O. Momeni, E. Afshari, "High power terahertz and millimeter-wave oscillator design: A systematic approach," *IEEE J. of Solid-State Circuits*, vol.46, no.3, pp.583-597, March 2011.

[36] Li Guansheng, E. Afshari, "A low-phase-noise multi-phase oscillator based on left-handed LC-ring," *IEEE J. of Solid-State Circuits*, vol. 45, no. 9, pp. 1822-1833, Sep. 2010.

[37] R. Sujiang, H. C. Luong, "Design and analysis of varactor-less interpolative-phase-tuning millimeter-wave LC oscillators with multiphase outputs," *IEEE J. of Solid-State Circuits*, vol. 46, no. 8, pp. 1810-1819, Aug. 2011.

[38] J. Savoj, B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase/frequency detector," *IEEE J. of Solid-State Circuits*, vol. 38 no.10, pp. 13-21, Jan. 2003.

[39] A. Rofougaran, J. Rael, M. Rofougaran, A. Abidi "A 900 MHz CMOS LC-oscillator with quadrature outputs," in *IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers* (ISSCC), pp. 392-393, 1996.

[40] M. I. Disman, W. A. Edson, "Simultaneous asynchronous oscillations in class-C oscillators," *IRE*, vol. 46, no. 5, pp. 895-903, May 1958.

[41] K. Kwok and H. C. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer feedback," *IEEE J. of Solid-State Circuits*, vol. 40, no. 3, pp. 652- 660, Mar. 2005.

[42] H.-H Hsieh; L. -H. Lu, "A high-performance CMOS voltage-controlled oscillator for ultra-low-voltage operations," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 467-473, Mar. 2007.

[43] F. Farhabakhshian, T. Brown, K. Mayaram, and T. S. Fiez, "A 475 mV, 4.9 GHz enhanced swing differential Colpitts VCO in 130 nm CMOS with an FoM of 192 dBc/Hz," in *IEEE Custom Integrated Circuits Conf.* (CICC), pp. 1-4, 2010.

[44] T. W. Brown, F. Farhabakhshian, A. G. Roy, T. S. Fiez, and K. Mayaram, "A 475 mV, 4.9 GHz enhanced swing differential Colpitts VCO with phase noise of -136 dBc/Hz at a 3 MHz offset frequency," *IEEE J. of Solid-State Circuits*, vol. 46, no. 8 pp. 1782-1795, Aug. 2011.

[45] S.-L. Jang, Chein-Feng Lee, "A low voltage and power LC VCO implemented with dynamic threshold voltage MOSFETS," *Microw. Wireless Compon. Lett.*, vol. 17, no. 5, pp. 376-378, May 2007.

[46] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Krieger Publishing Company, Malabar, FL, 1971.

[47] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, Boston, 2001.

[48] *ALD110800 datasheet*, Advanced linear Devices Co., available on-line at: http://www.aldinc.com/pdf/ALD110800.pdf, on Aug. 2012.

[49] *Introduction to thermoelectrics & design manual*, Tellurex Co., available on-line at: http://www.tellurex.com/technology/design-manual.php, on Jul. 2011.

[50] *Phase noise measurement application N9068A*, Agilent Co., available on-line at: http://cp.literature.agilent.com/litweb/pdf/5989-5354EN.pdf.

[51] Z. Li and K. K. O, "A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator," *IEEE J. of Solid-State Circuits*, vol. 40, no. 6, pp. 1296–1302, Jun. 2005.

[52] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. of Solid-State Circuits*, vol. 43, no. 12, pp. 652–660, Dec. 2008.

[53] A. Richeli, A. Comensoli, Zs. M. Kovacs-Vajna, "A DC/DC boosting technique and power management for ultra low-voltage energy harvesting applications," *IEEE Trans. Ind. Electron*, vol. 59, no. 6, pp. 2701-2708, Jun. 2012.

[54] A. Richelli, L. Colalongo, M. Quarantelli, M. Carmina, Zs. M. Kovacs-Vajna, "A fully integrated inductor-based 1.8-6-V step-up converter," *IEEE J. of Solid-State Circuits*, vol. 39, no. 1, pp. 242-245, Jan. 2004.

[55] M. Wens, K. Cornelissens, M. Steyaert, "A fully integrated 0.18 μm CMOS DC-DC step-up converter, using a bondwire spiral inductor," in *IEEE European Solid-State Circuits Conf.* ESSCIRC, 2007.

[56] M. K. Kazimierczak, "Pulse width modulation DC-DC power converters," Wiley, 2008.

[57] F. Ueno, T. Inoue, I. Oota, I. Harada, "Emergency power supply for small computer systems," in *IEEE Int. Symp. on Circ. and Systems* (ISCAS), vol. 2, pp.1065-1068, Jun. 1991.

[58] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. of Solid-State Circuits*, vol. SC.-11 no. 3, pp. 374-378, Jun. 1976.

[59] P.-H. Chen, X. Zhang, K. Ishida, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "An 80 mV startup dual-mode boost converter by charge-pumped pulse generator and threshold voltage tuned oscillator with hot carrier injection," *IEEE J. of Solid-State Circuits*, vol. 47, no. 11, pp. 2554-2562, Nov. 2012.

[60] R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, P. L. Rolandi, "Power efficient charge pump in deep submicron standard CMOS technology," *IEEE J. of Solid-State Circuits*, vol. 38, no. 6, pp. 1068-1071, Jun. 2003.

[61] G. Palumbo, D. Pappalardo, M. Gaibotti, "Charge-pump circuits: power-consumption optimization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.49, no.11, pp. 1535-1542, Nov. 2002.

[62] P.-S. Weng, H.-Y Tang, P.-C. Ku, and L.-H. Lu, "50 mV-input batteryless boost converter for thermal energy harvesting," *IEEE J. of Solid-State Circuits*, vol. 48, no. 4, pp. 1031-1041, Apr. 2013.

[63] L. Pylarinos, "Charge Pumps: An Overview," available on line at: http://www.eecg.toronto.edii/ kphang/ece1371/chargepumps.pdf.

[64] F. Pan, T. Samaddar, *Charge Pump Circuit Design*. Mc-Graw-Hill, New York, 2006.

[65] J. P. Curty , N. Joehl , F. Krummenacher , C. Dehollain and M. Declercq "A model for u-power rectifier analysis and design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2771-2779, Dec. 2005.

[66] E. J. Carlson, K. Stunz and B. P. Otis, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. of Solid-State Circuits*, vol. 45 no. 4, pp. 741-750, Apr. 2010.

[67] I. Doms, P. Merken R. Mertens C. Van Hoof, "Integrated capacitive power-management circuit for thermal harvesters with output power 10 to 1000 μW," in *IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers* (ISSCC), San Francisco, pp. 300-301, Feb. 2009.

[68] Y. C. Shih, B. P. Otis, "An inductorless DC-DC converter for energy harvesting with a 1.2 μW bangap-referenced output controller," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 832-836, Dec. 2011.

[69] G. Bassi, L. Colalongo, A. Richelli, Zs. M. Kovacs-Vajna, "100 mV-1.2 V fully-integrated DC-DC converters for thermal energy harvesting," *IET Power Electronics*, vol. 6, no. 6, pp. 1151-1156, Jul. 2013.

[70] A. I. A. Cunha, M. C. Schneider, C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. of Solid-State Circuits*, vol. 33, no. 10, pp. 1510-1519, Oct. 1998.

[71] C. Galup-Montoro, M. C. Schneider, *MOSFET Modeling for Circuit Analysis and Design*. International Series on Advances in Solid State Electronics and Technology. World Scientific, 2007.

[72] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010.

[73] A. I. A. Cunha, M. C. Schneider, C. Galup-Montoro, C. D. C. Caetano and M. B. Machado, "Unambiguous extraction of threshold voltage based on the ACM model," in *Nanotech 2005, Workshop on Compact Modeling* (WCM), Anaheim, USA, pp. 139-141, May 2005.