Phase Synchronism Loops of Carrier and Data

Antonio D. Reis [1, 2], Jose F. Rocha [2], Atilio S. Gameiro [2], Jose P. Carvalho [1]

[1]*Dep. Física / G. F.A. Telecom., Universidade da Beira Interior, 6201-001 Covilhã, Portugal*
[2]*Dep. Electrónica e Telecomunicações / I. T., Universidade de Aveiro, 3810 Aveiro, Portugal Phone:*
+351 275 319 700   e-mail: adreis@ubi.pt

Abstract- This work presents a Phase Lock Loop for Carrier Wave (CPLL) and a Phase Lock Loop for Data Bits (DPLL). Each one of these devices is constituted by a phase comparator, a loop gain, a low pass filter and a voltage controlled oscillator. The objective is to study these synchronizers and evaluate their performance in presence of noise. We measure the output jitter UIRMS (Unit Intervals Root Mean Square) versus input SNR (Signal Noise Ratio).
Keywords- Synchronism, Digital Communication Systems.

Introduction – The CPLL (Carrier Phase Lock Loop) and the DPLL (Data Phase Lock Loop) are actually very much used in various systems of Electronics and Telecommunications. The CPLL improves the quality, rigor and precision of the Electronics and Telecommunications Systems, which use the radiofrequence carrier, as in particular the Radio and Television. In equal mode, the DPLL improves the   quality, rigor and precision of the Electronics and Telecommunications Systems, which use the band base data, as in particular the transmission by fiber optic.

We study four CPLLs (analog_c, hybrid_c, combinational_c, sequential_c) and four DPLLs (analog_d, hybrid_d, combinational_d, sequential_d).

The Carrier PLL and the Data PLL - The CPLL is constituted by a carrier phase comparator Ckf, a loop gain Ka, low pass filter LPF and voltage controlled oscillator VCO. The DPLL is also constituted by a data phase comparator Dkf, loop gain Ka, low pass filter LPF and voltage controlled oscillator VCO.   The difference between the CPLL and the DPLL is only in the phase comparator. While the Ckf is only able to synchronize with an input regular wave the Dkf is able to synchronize with an input pseudo- random data [1].

An illustrative representation of the CPLL consists of an unipolar antenna that receives the radiofrequence signal, followed of the CPLL (Fig.1a). An illustrative representation of the DPLL consists of a fiber optic that receives the optical signal, followed of the DPLL (Fig.1b).
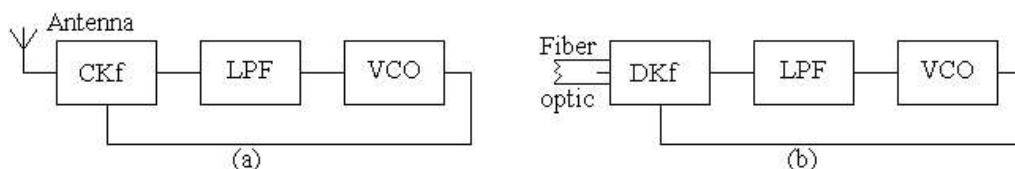

Fig1: Configurations of a system with CPLL (a) and a system with DPLL (b)

Various old electronics and telecommunications systems are based in filters and resonant circuits, but now are being substituted by modern systems based on CPLLs and DPLLs [1].

Results, discussion and conclusions
We tested, in terms of output jitter UIRMS versus input SNR, four CPLLs and four DPLLs. We verified that generally the output jitter UIRMS decreases gradually when the input SNR increases.

References
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