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A 68000-based produce sorting microcomputer : graduate clinical research master's report

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Graduate Clinical Research
Master's Report

A 68000-Based Produce Sorting
Microcomputer

by

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Preface

This report discusses in great detail the various research, design, and development stages of the Produce Sorting Microcomputer developed for HAGAN ENGINEERING Inc. The two-semester Clinical Research project has been approved by the graduate committee at the School of Engineering at the University of the Pacific and fulfills the requirements towards a Master Degree in Electrical Engineering.

The project was selected based on its complexity, feasibility, the time span it required to complete, and its relevance to the area of real-time-microcomputer design. In addition, the design constraints and specifications were to be dictated solely by HAGAN ENGINEERING Inc. and all further modifications were to be discussed and approved by HAGAN. These limitations created a professional industry-like atmosphere, which is one of the goals of the Clinical Research Program.

A brief User's Manual will accompany the MC68000 board; it will contain all the vital information about the system that a programmer or a technician might need to understand the system. The manual will contain the complete circuit schematic, a parts list, general design features, and all the software properties of the system (memory map, interrupt tables, register map).

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1.1 Introduction

The objective behind the design of the MC68000 project was to provide HAGAN ENGINEERING Inc. with a controller board that is able to monitor and control several produce sorting lanes simultaneously, with the MC68000 C.P.U. being the only processor available in the entire system. One of the specifications of the project is to design an open system that is not bound by any specific I/O device or transducer. Consequently, the terms 'monitor and control' above will not be defined in terms of external monitoring or controlling circuits. The MC68000 board was designed to serve as a general purpose controller that could communicate with several types of I/O devices. This was made possible by the various combinations of signals made available through the connectors on the board. Finally, the design was to be laid out on a printed circuit board for commercial use.

Note: A copy of the complete circuit diagram is included in appendix A (a reduced copy and a real size one). It should be referred to throughout the following design discussions.

1.2 Design Features

Full speed operation at 8 MHz.

8K Words of Battery-Backed RAM for User Code Development or data storage.

8K Words of ROM for Monitor storage.

Full data bus, 8 address lines, and control circuitry available in EIA Standard RS-485 via two separate 26 pin dual-in-line connectors.

8 Data and Address lines, 3 I/O lines, and control circuitry available in buffered TTL levels via a 26-pin DIP connector for general

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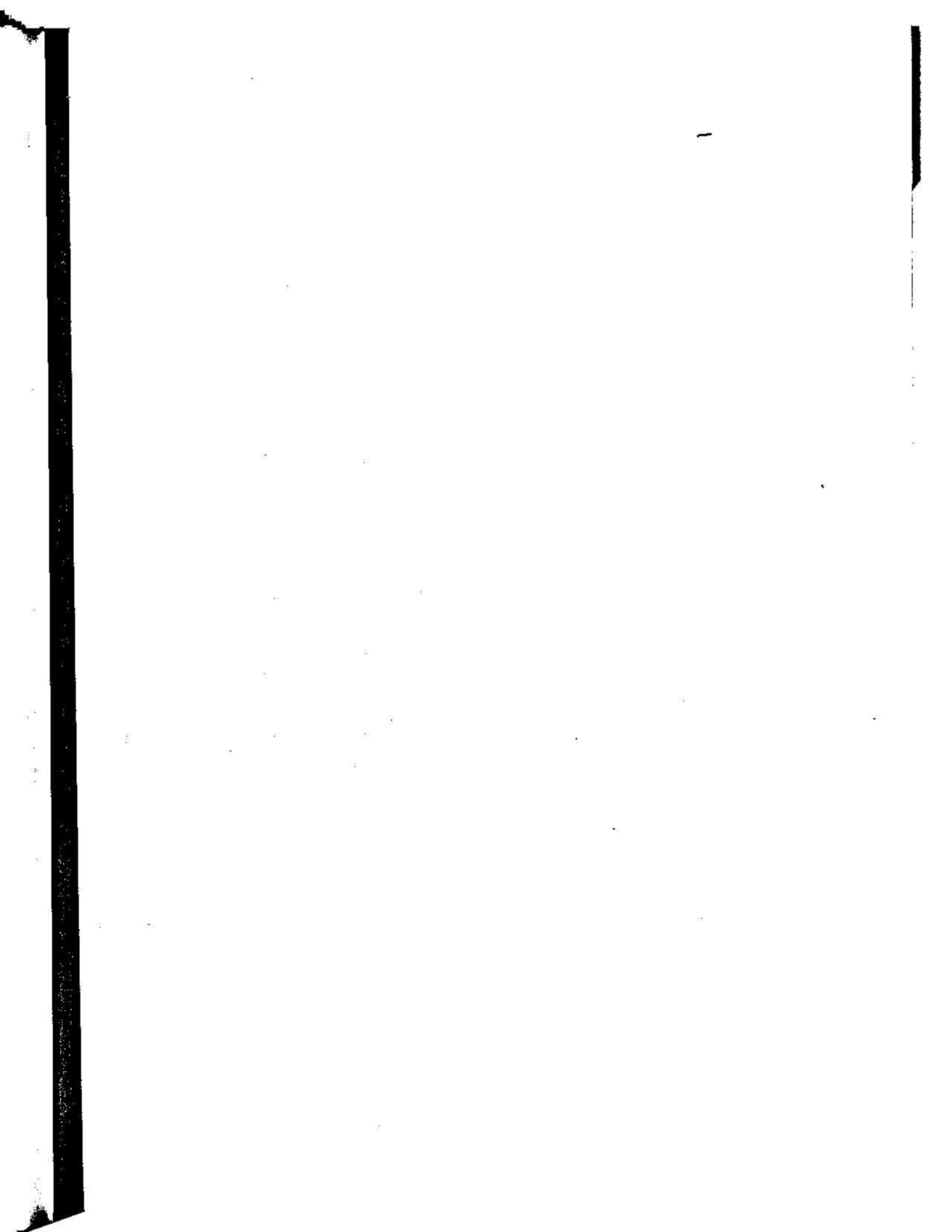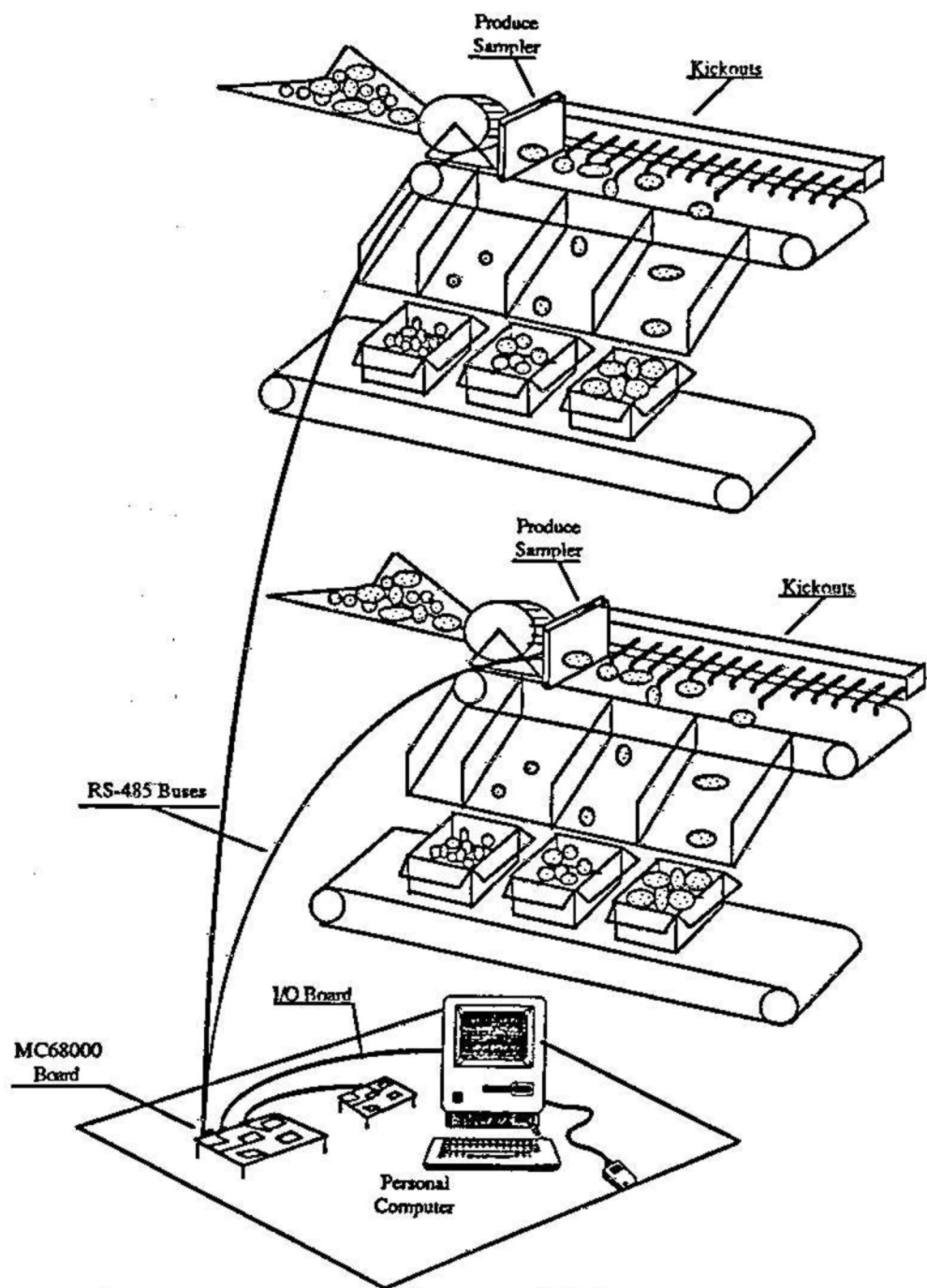
Figure 1 68000 Typical Application
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2.0 System Memory

The following section discusses in detail the timing of the MC68000 processor within the board, its relationship with asynchronous devices, and the memory configuration on the MC68000 board. These explanations should serve the user as a guide to connecting asynchronous peripherals to the system through connectors J1, J2, and J3.

2.1 The MC68000 Read Cycle

The MC68000 machine cycle consists of a minimum of four clock cycles and is divided into eight states labeled S0 to S7 (see figure 3 next page). All machine cycles start in state S0 with the clock high and end in state S7 with the clock low. Of course the machine read cycle may be extended (up to 1.6 seconds in the case of this MC68000 design) by the insertion of wait states (each with a duration of one half clock cycle) between clock states S4 and S5, allowing the MC68000 to operate with a mixture of both fast and slow interface components.

At S0 of the read cycle, all signals are negated with the exception of R/W which remains high for the rest of the read cycle. In State S1, the address on A01 to A23 becomes valid and remains so until state S0 of the following cycle. In state S2 the address strobe, AS*, goes low indicating that the content of the address bus is valid. The timing of LDS* and UDS* are the same as AS*, and their falling edges can be used to initiate a memory access. After the falling edge of AS* (and the Data Strobe Lines), if the

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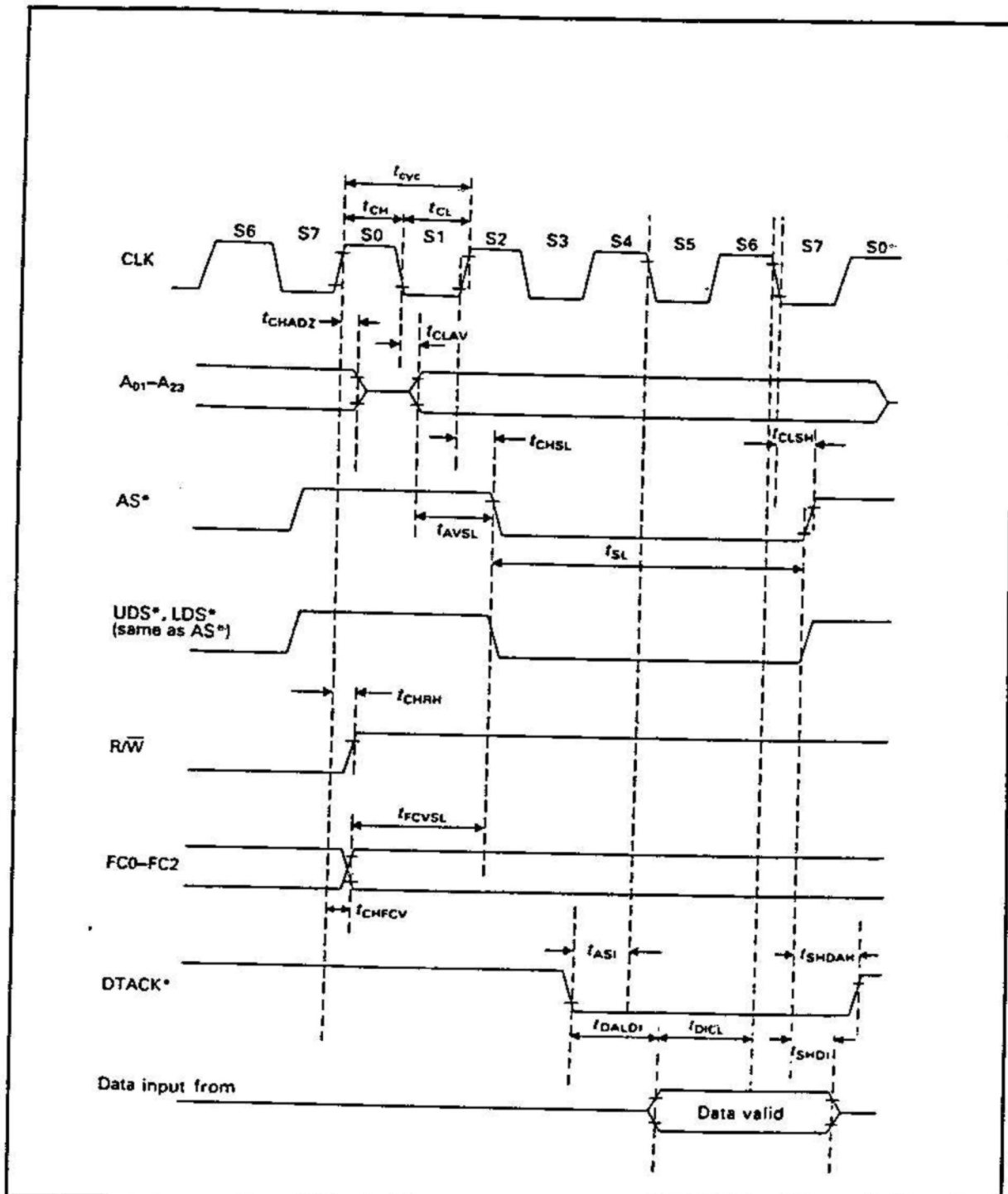
Figure 3 MC68000 Timing Diagram

DTACK* does not go low at least 20ns before the end of state S4, wait states are introduced between S4 and S5 until DTACK* is asserted. If the DTACK* line is not asserted by the component being read within the next 1.6 seconds, the processor is reset by the external watch dog timer on the board.

During the final state, S7, of the current bus cycle (after the assertion of DTACK*) both AS* and LDS*/UDS* are negated (unasserted) and the data is latched into the MC68000 internally. DTACK* must be negated after the strobes have been negated.

2.2 Timing Relationship

The following timing parameters pertain to the MC680008L 8MHz CPU by Motorola Inc. Please refer to Figure 3, above.

The address bus is floated within 80ns (Max) of the start of S0. The new address is placed on the bus no more than 70 ns (Max) after the start of S1. The address strobe, AS*, is asserted no less than 30ns after the address has stabilized.

R/W is set high at the beginning of a read cycle no more than 70 ns (Max) after the start of S0, and stays high for the remainder of the current cycle.

The key parameter governing the DTACK* handshake from the peripheral is its setup-time, 20ns (min.), before the falling edge of S4. If DTACK* satisfies this timing, the next state will be S5, otherwise wait states will be inserted until DTACK* is asserted . In order to avoid the

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insertion of a wait state, DTACK* must be asserted at least 20ns before the next clock input.

During state S7, both address and data strobes are negated within 70ns (Max) of the falling edge of the clock. In order to meet the data hold-time of the MC68000, the contents of the data bus must be stable for at least 0 ns after the rising edge of the strobes. In other words, the data may become invalid concurrently with the rising edge of AS* or LDS/UDS*.

Note: The MC68000 Board has a watchdog timer that resets the MC68000 processor if the timer is not strobed by AS* within 1.6 sec. Therefore, all read and write cycles can hold the bus (i.e., keep DTACK* inactive) no longer than 1.6 sec. This feature is provided to avoid a bus freeze in case of an erroneous bus cycle.

2.3 Peripheral Compatibility

Figure 4 (next page) relates the essential features of the MC68000 timing diagram to those of a peripheral that will be placed directly on the bus without needing wait states (All the memory components placed on the MC68000 Board operate with zero wait states).

From the falling edge of S0 to the falling edge of S6, three full clock cycles take place, a total time of $3*t_{cyc}$ (The processor latches the data at the end of state S6). During this time, the value on the address bus become valid (70ns), the peripheral is accessed (t_{AA}), and the data setup-time is met (15ns). Thus, the total time for this action is given by 70ns + 15ns + t_{AA}.

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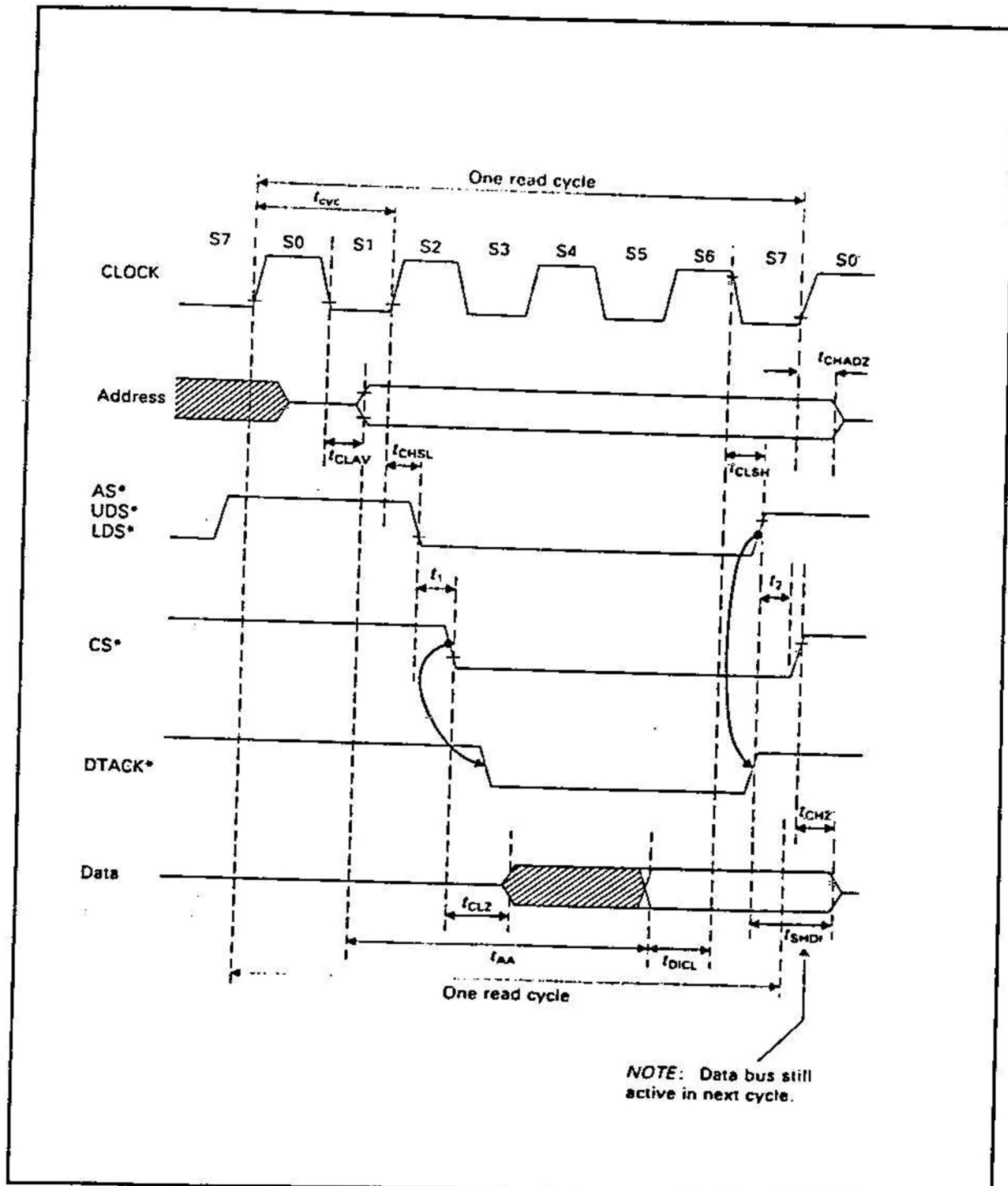
Figure 4   MC68000 /Peripheral Timing Diagram

Putting the two equations together we get:

$$3 * t_{cyc} > 70ns + 15ns + t_{AA}$$

or

$$t_{AA} < 3 * 125 - 70 - 15 \quad \Rightarrow t_{AA} < 290ns$$

Therefore, the peripheral must have an access time of less than 290ns to work with the MC68000L8 at 8 MHz without any wait states.

Note: The data from the peripheral must stay valid until the AS* (Chip Select) is negated.

2.4 MC68000 Board Memory Configuration

The MC68000 Board has 16K Bytes of ROM available for storing a Monitor program and permanent data. The 16K Bytes of ROM are configured as two 8K Bytes in parallel to form an 8K Word (16bit/Word) memory space. The ROMs have an access time of 150nsec, which makes it possible to use them without any wait states.

The same configuration applies to the two 8K Bytes of RAM used in the design to provide an 8K Word space for downloading programs. The RAMs have an access time of 100ns making it possible to operate them without any wait states.

2.5 Memory Map

The complete memory map of the system is shown in table 1 (next page). It should be noted that ROM starts at address 0F, eliminating the choice of dynamic programming of the exception vectors. In other words,

Table 1 MC68000 Board Memory Map

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	ADDRESS	DEVICE	SPACE
0	0	0	0	0	0	0	0	0	0	0	0	0	X	0	0	0	0	0	X	X	X	X	00 0000	ROM	8K
1	1	1	1	1	1	1	1	1	1	1	1	1	X	0	0	0	0	0	X	X	X	X	00 3FFF	ROM	
0	0	0	0	0	0	0	0	0	0	0	0	0	X	1	0	0	0	0	X	X	X	X	00 8000	RAM	8K
1	1	1	1	1	1	1	1	1	1	1	1	1	X	1	0	0	0	0	X	X	X	X	00 BFFF	RAM	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	0	1	0	0	0	X	X	X	X	01 0000	901CS	24 REG.
1	1	1	1	1	X	X	X	X	X	X	X	X	X	0	1	0	0	0	X	X	X	X	01 003F	901CS	
0	0	0	0	0	0	0	0	X	X	X	X	X	X	1	1	0	0	0	X	X	X	X	01 8000	HEADCS	256 WORDS
1	1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	0	0	0	X	X	X	X	01 81FF	HEADCS	
0	0	0	0	0	0	0	0	X	X	X	X	X	X	0	0	1	0	0	X	X	X	X	02 0000	BOARDCS	256 BYTES
1	1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	1	0	0	X	X	X	X	02 01FF	BOARDCS	
0	0	0	0	0	0	0	0	0	0	0	0	0	X	1	0	1	0	0	X	X	X	X	02 8000	N.C.	32K
1	1	1	1	1	1	1	1	1	1	1	1	1	X	1	0	1	0	0	X	X	X	X	02 FFFF	N.C.	
0	0	0	0	0	0	0	0	0	0	0	0	0	X	0	1	1	0	0	X	X	X	X	03 0000	N.C.	32K
1	1	1	1	1	1	1	1	1	1	1	1	1	X	0	1	1	0	0	X	X	X	X	03 7FFF	N.C.	
0	0	0	0	0	0	0	0	0	0	0	0	0	X	1	1	1	0	0	X	X	X	X	03 8000	N.C.	32K
1	1	1	1	1	1	1	1	1	1	1	1	1	X	1	1	1	0	0	X	X	X	X	03 FFFF	N.C.	

the interrupt vectors will have to be programmed in ROM and a jump to RAM would have to be placed after the vectors for software development that uses exceptions. This scheme was adopted in order to save additional circuitry that would have been needed to select the ROM at Power up then select RAM eight clock cycles later.

2.6 Battery Backup

A 165mAh 3V Lithium battery is used in conjunction with a Maxim 695 to detect brownouts, power-ups, and power-downs. Any time the power falls below 4.65V, both RAM chips are disabled via their chip-enables, power to the RAM VCC is re-routed to the 3V battery, and the processor is reset. At power-up, the Max695 holds the reset line low for 200ms after valid power levels are restored. This gives the MC68000 plenty of time beyond its required 100ms initialization period. It also guarantees sound RAM data and prevents the processor from erroneously writing to RAM.

The current required by the memories is 50µA maximum. Therefore, the current supplied by the battery can be up to 2 * 50µA + 1µA, or 101µA (The Max 695 leaks 1µA Max in power-down mode).

A 165mAh fully charged Lithium battery should be able to supply this current for 1633 hours, or over 60 days.

3.0 MC68901 Multifunction Peripheral

The MC68901 directly interfaces with the MC68000 microprocessor via the asynchronous bus structure. Both vectored and polled interrupt

schemes are supported with the M.F.P. providing unique vector number generation for each of its 16 interrupt sources. The MC68901 offers the following functions to the MC68000 board:

- Eight Individually Programmable I/O Pins with Interrupt Capability.
- 16-Source Interrupt Controller with Individual Source Enable and Masking.
- Four Timers, Two of which are Multi-Mode Timers.
- Single-Channel Full-Duplex Universal Synchronous/Asynchronous Receiver-Transmitter.

3.1 The M.F.P. in the MC68000 Board

The MC68901's I/O functions are available on the MC68000 board via connectors on the board, and are described in detail below (refer to the circuit diagram in appendix A for details):

- All seven I/O lines are available at connector J4 as TTL level inputs. The main purpose of this connector is to provide the user with seven external interrupt lines. Consequently, the lines have optional pull-up resistors connected to them. The I/O lines on J4 could be used as input bits, however the user should provide proper buffering of the TTL lines since no on-board buffering is provided for these lines.

  Timer A and Timer B are also available at J4 as general purpose Event Counters/Pulse Measurement Timers.

Note: In no circumstance should any of the lines on J4 be used as outputs. These lines are not buffered and are to be used as inputs only; connecting them as output lines to an off-board device could permanently damage the

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MC6890L Refer to J1 for output lines.

• Connector J1 has I/O bit 7 (I/O7) connected to it as a buffered TTL level output bit. This line could be used as output because it is buffered. J1 also has I/O5 and I/O6 available as input bits, as in J4, but with no pull-up resistors.

Note: Bits I/O5 and I/O6 on J1 should be used as inputs only since they are not buffered.

• The serial communication channel on the MC68901 is converted to EIA Standard RS-485 and connected to connector J6. The Serial channel clock input is a 2.4576MHz from which any desired baud rate can be programmed via timer D and the internal frequency divider in the M.F.P.

• The MC68901 Timers A, B, C, and D are general purpose 8-bit timers that can generate periodic interrupts, measure elapsed time, and count signal transitions. Timer D is used as a programmable baud rate generator.

• The MC68901 has an interrupt level 7 assigned to it by the MC68000. This is the highest priority level on the MC68000. This guarantees immediate processing of all the prioritized interrupts generated by the MC68901.

3.2 Addressing The MC68901

The MC68901 has a base address of 010000H, and contains 24 registers that are directly addressable, simplifying programming. The register map is shown in table 2 on the following page.

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Hex Address	Abbreviation	Register Name
10001	GPDR	General Purpose I/O Data Register
10003	AER	Active Edge Register
10005	DDR	Data Direction Register
10007	IERA	Interrupt Enable Register A
10009	IERB	Interrupt Enable Register B
1000B	IPRA	Interrupt Pending register A
1000D	IPRB	Interrupt Pending register B
1000F	ISRA	Interrupt In-Service Register A
10011	ISRB	Interrupt In-Service Register B
10013	IMRA	Interrupt Mask Register A
10015	IMRB	Interrupt Mask Register B
10017	VR	Vector Register
10019	TACR	Timer A Control Register
1001B	TBCR	Timer B Control Register
1001D	TCDCR	Timers C and D Control Register
1001F	TADR	Timer A Data Register
10021	TBDR	Timer B Data Register
10023	TCDR	Timer C Data Register
10025	TDDR	Timer D Data Register
10027	SCR	Synchronous Character Register
10029	UCR	USART Control Register
1002B	RSR	Receiver Status Register
1002D	TSR	Transmitter Status register
1002F	UDR	USART Data Register

Table 2   MC68901 Register Map

4.0 I/O Connectors

The MC68000 Board has seven I/O connectors that are discussed in detail below.

4.1 Connector J1

Connector J1 has 8 Address and 8 Data lines, 3 I/O lines, and 4 control lines for asynchronous communication with the MC68000. J1 is configured to communicate with an I/O board with asynchronous communication capabilities. The four control lines are R/W, LDS*, BOARDCS*, and IODACK*. These lines are used in conjunction with the address and data lines to give access to 256 bytes of I/O space. The 3 I/O lines are discussed in detail in section 3.1 above.

Note: IODACK* is to be held high at all times for proper board operation unless a valid read/write cycle is in progress through J1. IODACK* is the data acknowledge line for the I/O board.

4.2 Connectors J2 and J3

J2 and J3 are the main data input source for the board. Together, they provide 16 data lines, 8 address lines, and control lines, all in EIA standard RS-485. J2 and J3 are configured as read-only buses. The control lines HEADACK* and HEADCS* are needed to establish read-only asynchronous communication. RS-485 communication protocol requires two differential lines for each TTL line. Consequently, the 26 TTL lines are converted to 52 transmission and reception lines at the connectors. Every

line is split into two, namely X and Y (i.e., D01 becomes D01X and D01Y) where Y is the low line and X is the high line.

The main reasons the RS-485 Standard was adopted in this design are the noise immunity offered by the transceivers (Common Mode Output Voltage Range of -12.0 Volts to +12.0 Volts with an input sensitivity of +/- 200mV over this range), the high speed at which they are able to communicate (10 Mbs), the multipoint communication scheme they offer due to their three-state output capabilities, and the long distances at which they are able to perform these functions (up to 4000ft). As a result, the MC68000 board is able to communicate at high speed with several produce sorting lanes located at various locations throughout a produce sorting company without the worry of communication noise.

In a typical application, the MC68000 reads sampled raw data from J2 and J3, and sends feedback control signals for produce sorting and boxing through J1, which would normally be connected to an I/O board that uses the same communication standards.

Note: The only constraint on the MC68000 board as far as J2 and J3 are concerned, is that every read cycle must be no longer than 1.6 sec, otherwise the processor will be reset by the watchdog timer.

4.3 Connector J4

Connector J4 was discussed in detail in section 3.1 along with the operation of the MC68901 Multifunction Peripheral.

4.4 Connector J5

J5 is the power connector with pins 1 and 3 as Ground signals and pin 2 as 5 Volts. The board uses a single 5V power supply. Power requirements are discussed in section 5.0, below.

4.5 Connector J6

J6 is the RS-485 Serial communication connector. Four lines are available: Transmit lines X&Y, and receive lines X&Y. The baud rate is programmable via Timer D, which uses a base clock frequency of 2.4576MHz.

4.6 Connector J7

J7 is the reset connector. A cable attaches to J7 and is connected to a normally-open SPST switch which is placed on the casing of the board.

5.0 Power Requirements

The majority of the integrated circuits used on the MC68000 board are low power CMOS devices. Consequently, the power requirements are lower than they would have been if TTL LS and HMOS devices had been used. The maximum power requirement for the board is 1.3 Amperes at 5 Volts in the event an HMOS MC68000 CPU is used. If a CMOS CPU 68HC000 is used, the maximum power requirement would drop to 1.1 Amperes. In either case, a standard 1.5 Amps power supply at 5 Volts would serve the board well.

6.0 Board Prototyping and Testing

An Augat wire-wrap breadboard system was used to prototype and test the MC68000 design initially. The system development consisted of modular building and testing of the microcomputer parts as suggested by the time table in appendix C. The system peripherals were the first parts to be tested in order to insure compatibility with the MC68000 and proper functioning. The first prototype included reset circuitry, the RS-485 line drivers and receivers, the system clocks, and the serial drivers. No parts proved to be incompatible or defective.

The second phase consisted of testing the processor, reset circuitry, ROMs, and various glue parts. A simple infinite loop program was written to test the circuit which gave expected results by displaying the correct repetitive waveforms on all address and data lines. At this time the final address decoding was implemented using a single 74HCT138 3/8 decoder. The address decoding was tested by writing to all the assigned memory blocks and observing the corresponding waveforms.

The last part of testing the basic microcomputer consisted of installing the two 6264LP-10 Random Access Memories, and the corresponding glue parts. An elaborate test program was written to test every bit in the RAM by using the stack as a pointer to the memory location to be tested and writing a different data Long word to every location. Initial results of the tests revealed a bus error every time the processor accessed RAM via the user stack also located in RAM. However, a different test

program revealed a positive RAM test if the stack is not used. It was later discovered that for proper processor operation the stack is to be initialized at a long word boundary (i.e., at an even address). The initial test program was re-run with a correct stack address and the the RAM test was completed successfully.

The last phase of the test consisted of assembling the compete board, with the MC68901 Multifunction Peripheral, RS-485 line transceivers, and bus buffers. A test program was written to test the complete features of the board. The test proved satisfactory. A copy of the program can be found in appendix D.

7.0 Printed Circuit Board Design

The Final stage of the design procedure was to implement the MC68000 board on a 4-layer high density printed circuit board for commercial use. To accomplish this task, the DOUGLAS CAD/CAM™ PROFESSIONAL SYSTEM (D.P.S.) electronic design and manufacturing system was used on an Apple® Macintosh™ personal computer. The D.P.S. is a professional software system that is acquired in three separate packages. Each of three packages is crucial to developing a professional PCB and will be discussed in detail in the following sections.

7.1 The D.P.S. CAD/CAM™ Schematic Program

The Schematic program was used during the initial stages of the design. This is a schematic capture program with the ability to simulate

SSI and MSI circuitry dynamically. The program comes with libraries that contain hundreds of digital and analog parts that are normally used in electrical and computer engineering design. Integrated circuits that were needed in the MC68000 design which were not available but which were needed in the design had to be created using a graphics program then transferred to the Schematic libraries. The complete circuit diagram is shown in appendix A. A reduced size copy is included, along with a four page detailed copy. Following completion of the circuit diagram, Schematic generated a report containing all the pin-to-pin connection listings, the complete parts list, and the instructions for the Autorouter program (the third part of D.P.S). The report is included in appendix L. Before continuing with the PCB development, several design modifications took place, in part due to design optimization and in part by HAGAN's request.

7.2 The D.P.S. CAD/CAM™ Layout Program

Layout is used in the second phase of the PCB development. After the final schematic diagram is completed, Layout is used in conjunction with the Schematic report to place the integrated circuit footprints on the PCB. The report is used to check off every part that has already been placed on the board in order to avoid its placement more than once.

Layout has the ability to generate multilayered boards with high density component spacing. The program comes with a built in footprint library of the most popular ICs. Other IC footprints can be easily created with Layout and stored in the library.

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After placement of all the parts, the board outlines are set and a silk screen file is created. The silk screen file is usually printed on the PCB over the solder mask in white epoxy ink. This file usually contains the name of all components, their orientation, and any information that needs to be on the PCB itself. The silk screen file does not effect the tracing or routing of the board.

The MC68000 board was designed with four layers: A component layer, a solder layer, a ground layer, and a power layer. Appendix E shows the footprints that were created with Layout. It can be seen that all holes of the same size are printed with a distinct pattern. This scheme is used to make automated Printed Circuit Board manufacturing feasible. The silk screen created for the board is shown in appendix F.

7.3 The D.P.S. CAD/CAM™ Autorouter

The Autorouter is the final and most crucial part of the CAD/CAM package in that it establishes all the interconnections on the PCB, including Power and Ground connections. Autorouter is a program that requires preset instructions (usually included in the Schematic report) according to which it will route the board. The router routes the board by making several passes (as many as instructed in the report from the Schematic program) through the pin-to-pin connection list in the report. For every one of these connections or nodes, the router attempts to place a trace in such a way that it follows the criteria given in the instructions of the Schematic report. The criteria can be changed for each pass through

the node list. They can also be changed for selected nodes in the list. Usually, several experimental runs need to be made on a board before the best Autorouter instruction set is established, otherwise the Autorouter will route a certain percentage of the nodes and will leave the rest unconnected. The unrouted nodes are then listed in a new report that is generated by Autorouter. It is then up to the user to either re-run the program with a new instruction set or route the remaining nodes manually. Another way of routing a board would consist of first manually placing the traces known to have presented some difficulty to the program, then running the program on the board with the manual traces included. In this case the user has to flag all the pre-routed nodes in the report list to prevent Autorouter from routing them again.

Several runs were made on the MC68000 board in order to optimize the Autorouter's instruction set for a higher percentage of the routed nodes. It took Autorouter about 5 hours on the Apple® Macintosh Plus™ (or Apple® Macintosh SE™) to complete each run. The first run yielded 83% of the nodes routed. With subsequent runs the percentage was increased gradually by modification of the instruction set. At 92% a plateau was reached where it was realized that node pre-routing was necessary if the board was to be routed with its present size and component density. Since the most inefficient routing done by Autorouter was on the memory components, a pre-routed file (Barrier file) was created with all the memory components interconnected (see appendix G). Finally, after some instruction modifications, Autorouter routed the complete board (100% of

the traces) in four passes. The development time was greatly reduced when the Apple® Macintosh IIX™ was used which decreased the Autorouter runs to 1.5 hours instead of the 5 hours required on the Apple® Macintosh Plus™.

The final routed files consist of the component side traces, the solder side traces, the power plane traces, and the ground plane traces. All four layers are shown in Appendices H, I, J, and K respectively.

7.4 Photoplotting and PCB Manufacturing

Following the completion of the board design, the routing files were sent electronically (via Modem) to Douglas Company, where they were photoplotted with a high precision laser. The artwork was received from Douglas five working days later and was ready to be submitted to a PCB manufacturer. After consulting with several PCB companies, the film was given to a PCB manufacturer who produced the 4-layer board in two weeks.

8.0 PC Board Cost

A parts list including prices is given in appendix B. The printed circuit board cost will be $33.69 if it is manufactured in quantities greater than 100. The fully populated MC68000 Board will cost around $127.41 excluding labor (i.e., assembling and testing).

9.0 PC Board Testing

After receiving the 68000 PCB, it was checked for shorts and missing traces. Several vias were found to have shorted the ground plane to the power plane due to Autorouter's handling of the barrier file. This problem was corrected by inserting an instruction in the Schematic report that clears the vias on all four layers. The holes on the PCB were drilled out and connecting wires were placed instead which cleared all the shorts.

Three traces were missing from the board, the ground and power shorting bars of the 74HCT04 and the RESET line of the MC68901. The missing lines were corrected on the D.P.S. files and were soldered on the Board.

After all the corrections were made the MC68000 PCB ran and executed all the test programs that the prototype had previously run.

Appendix A
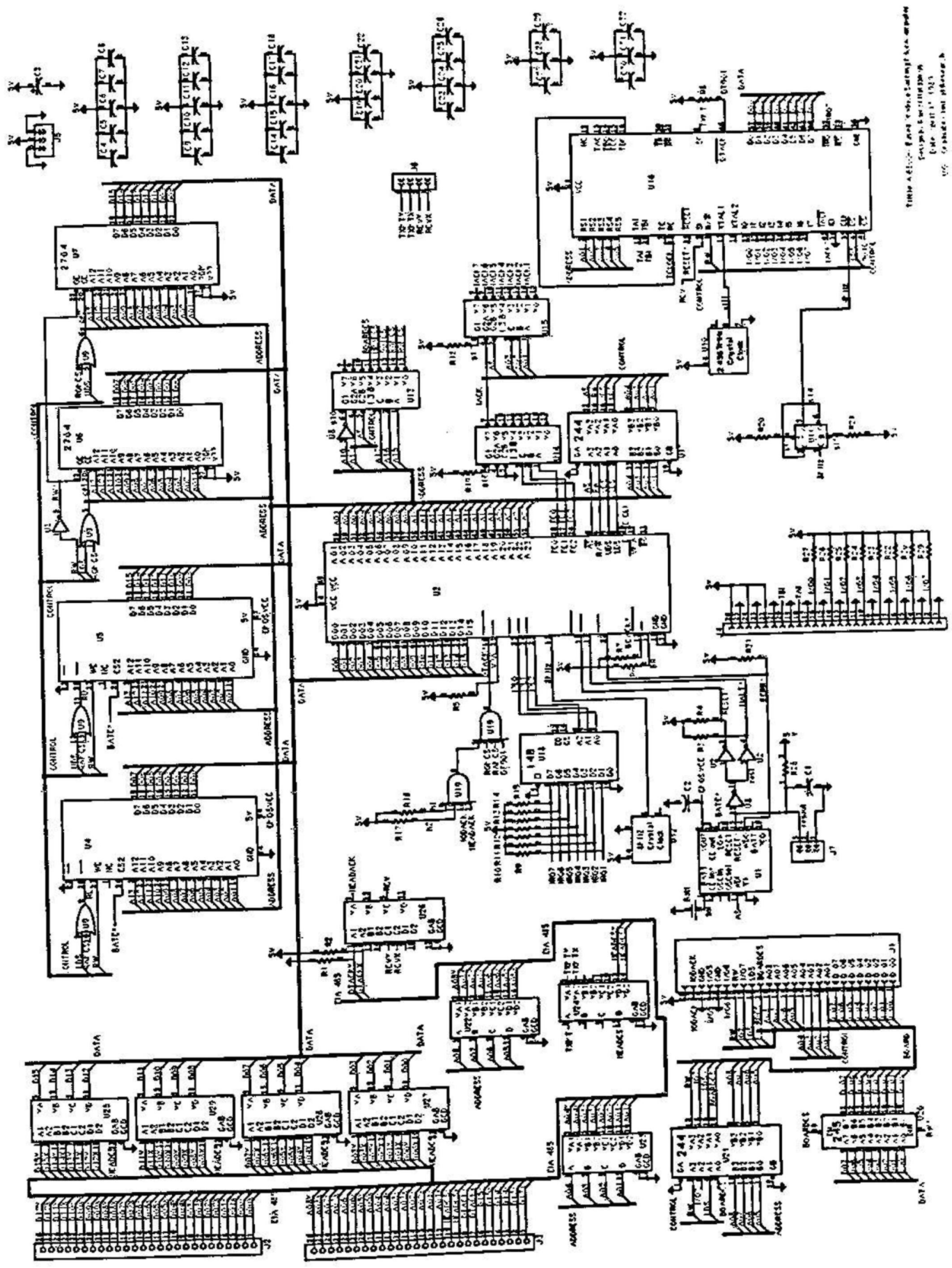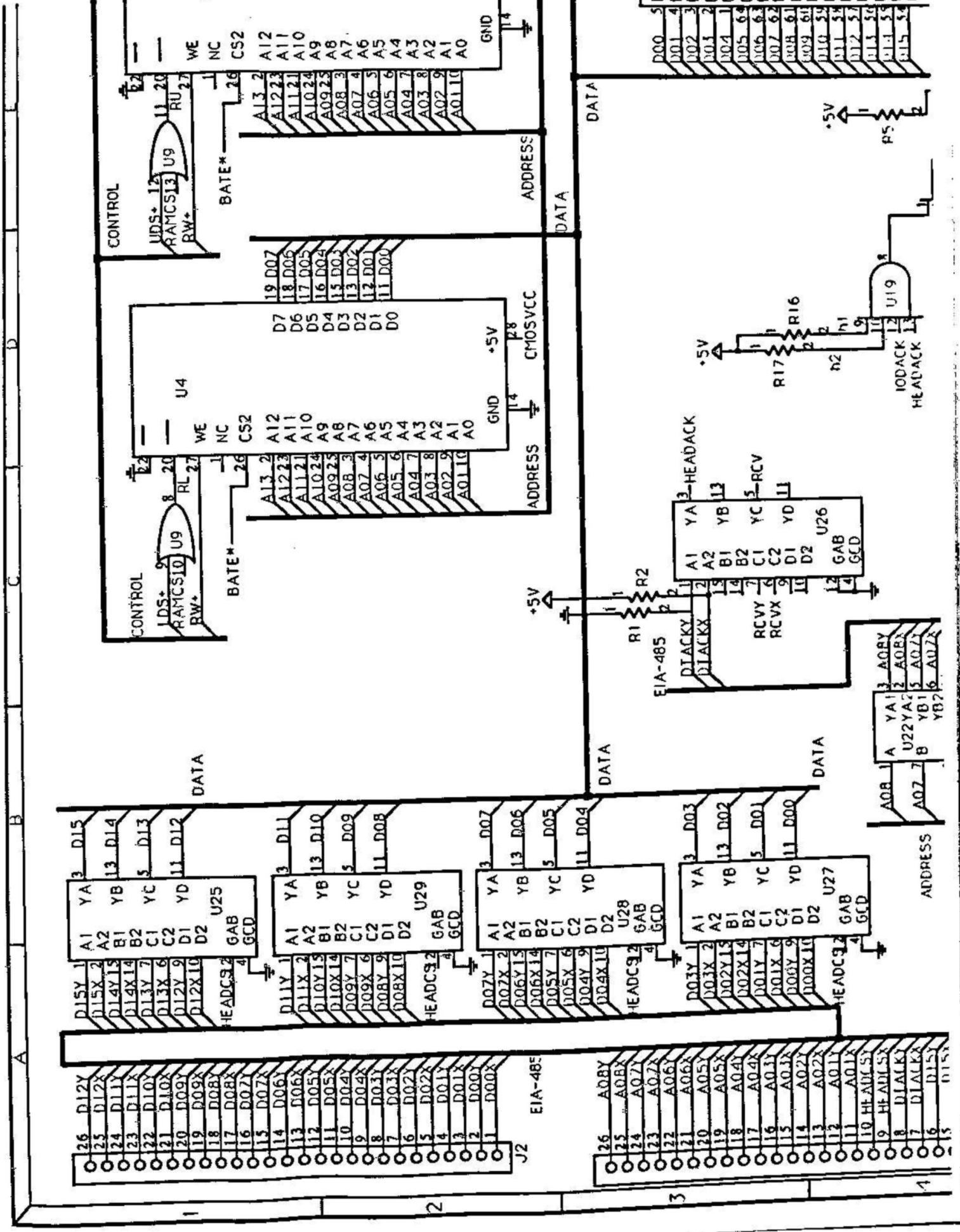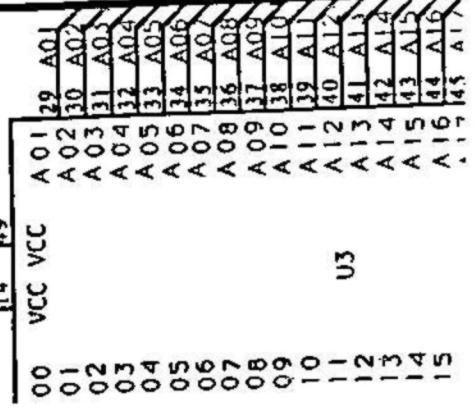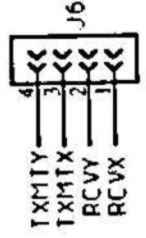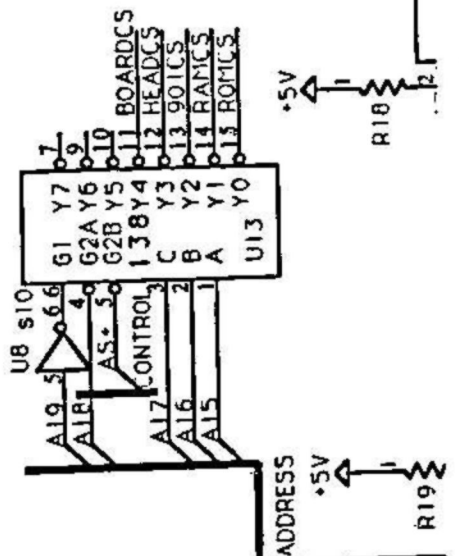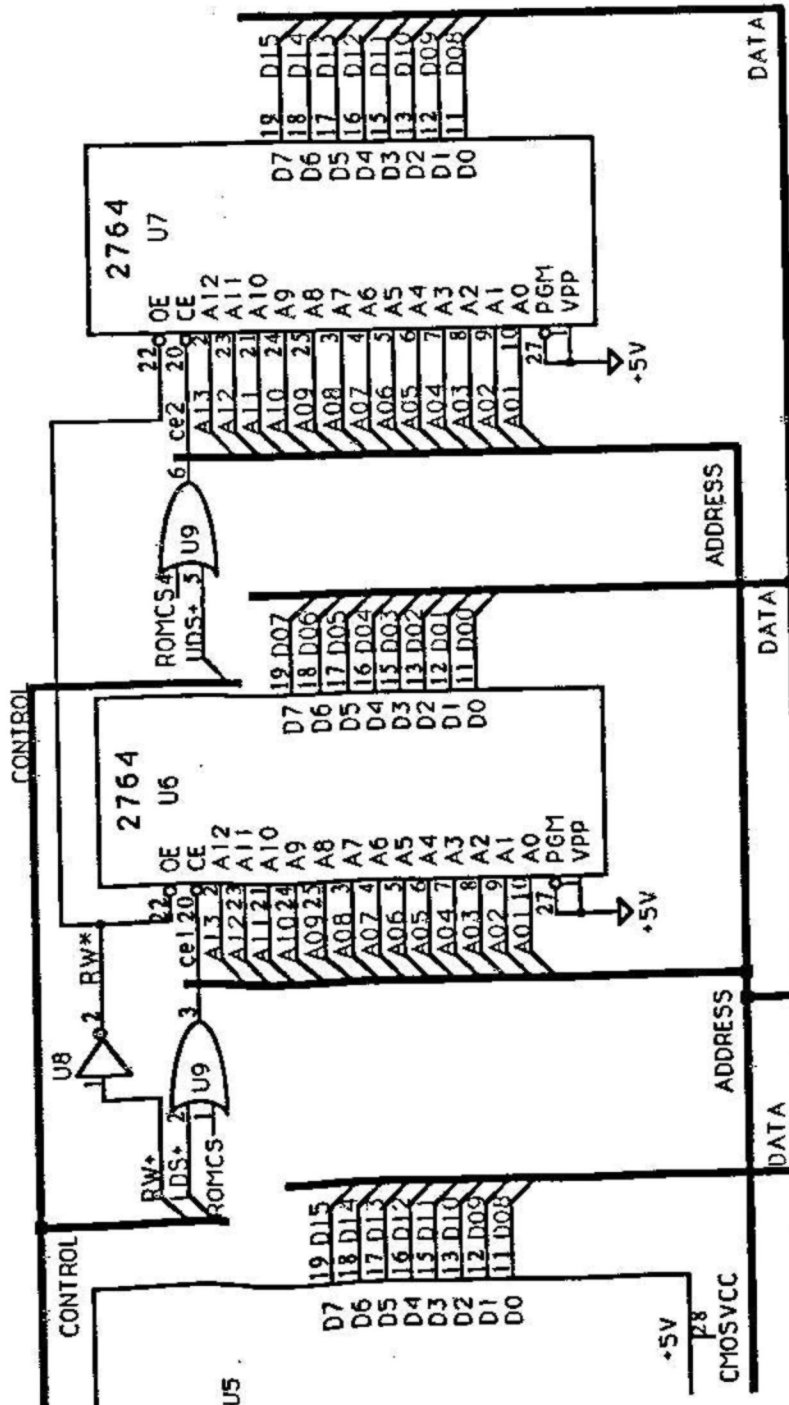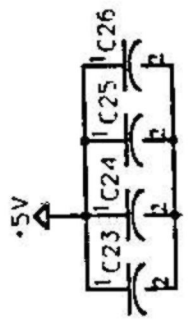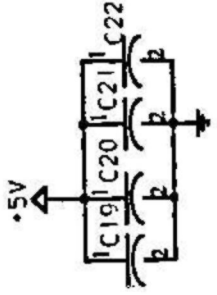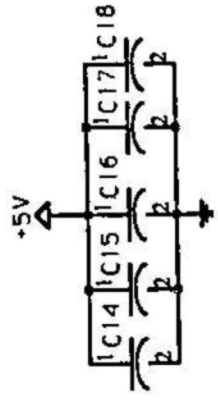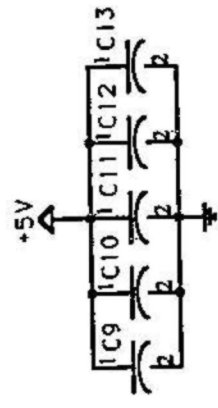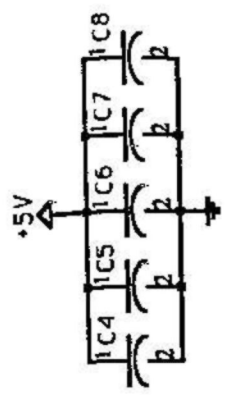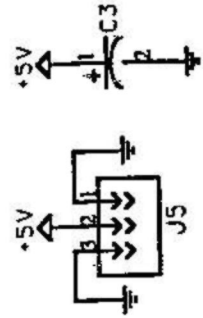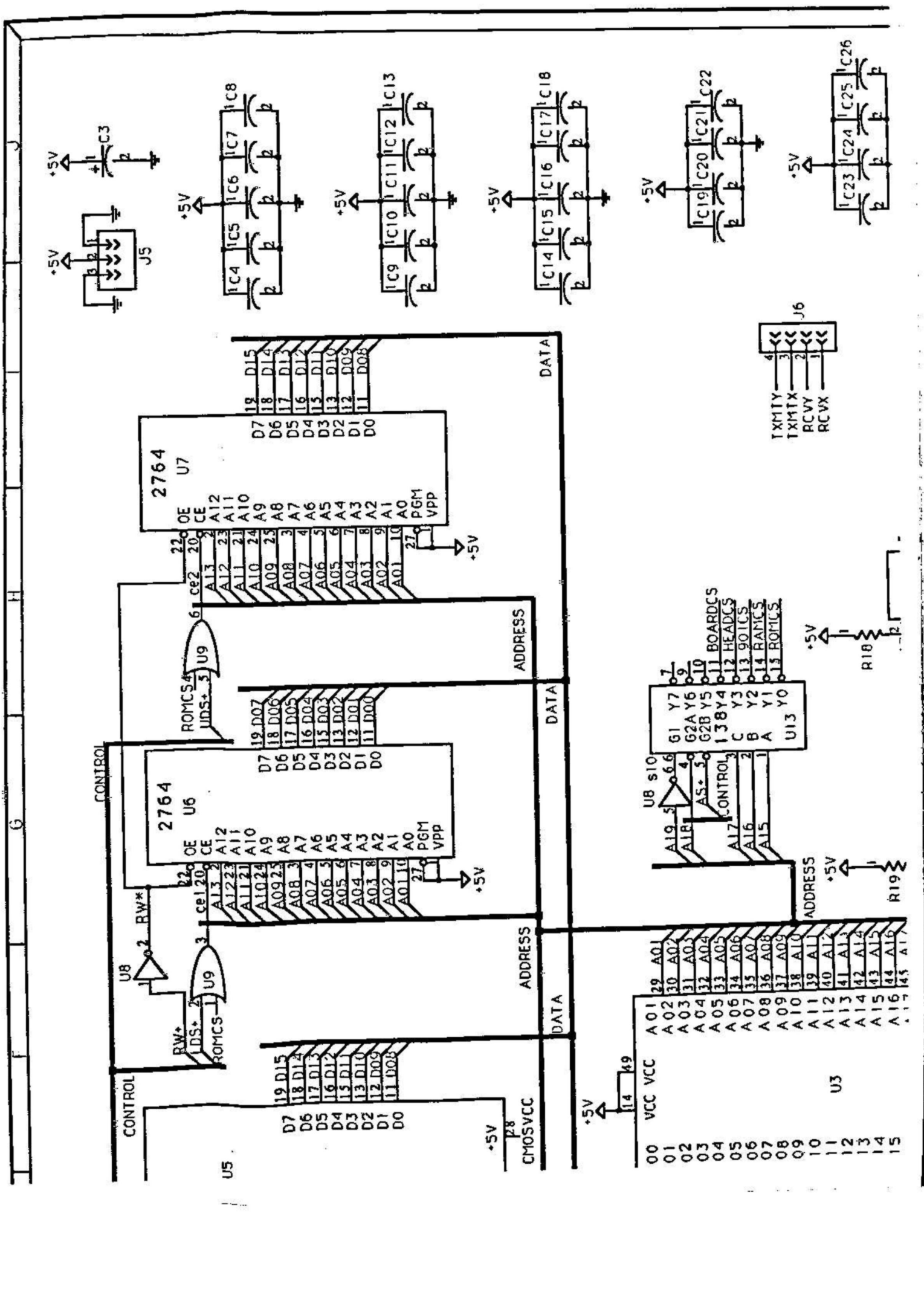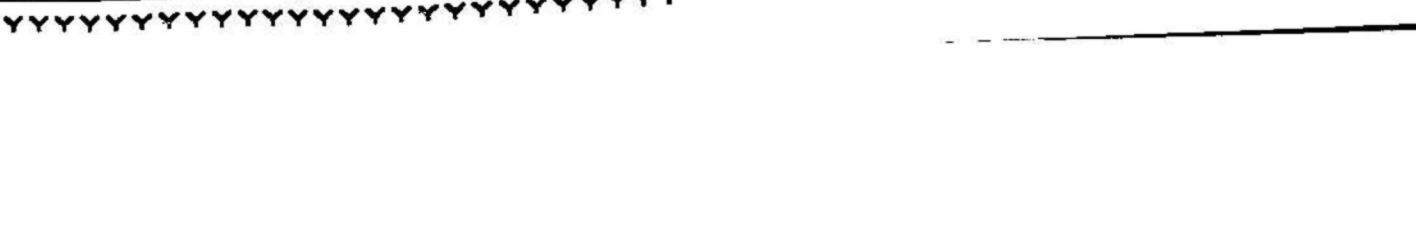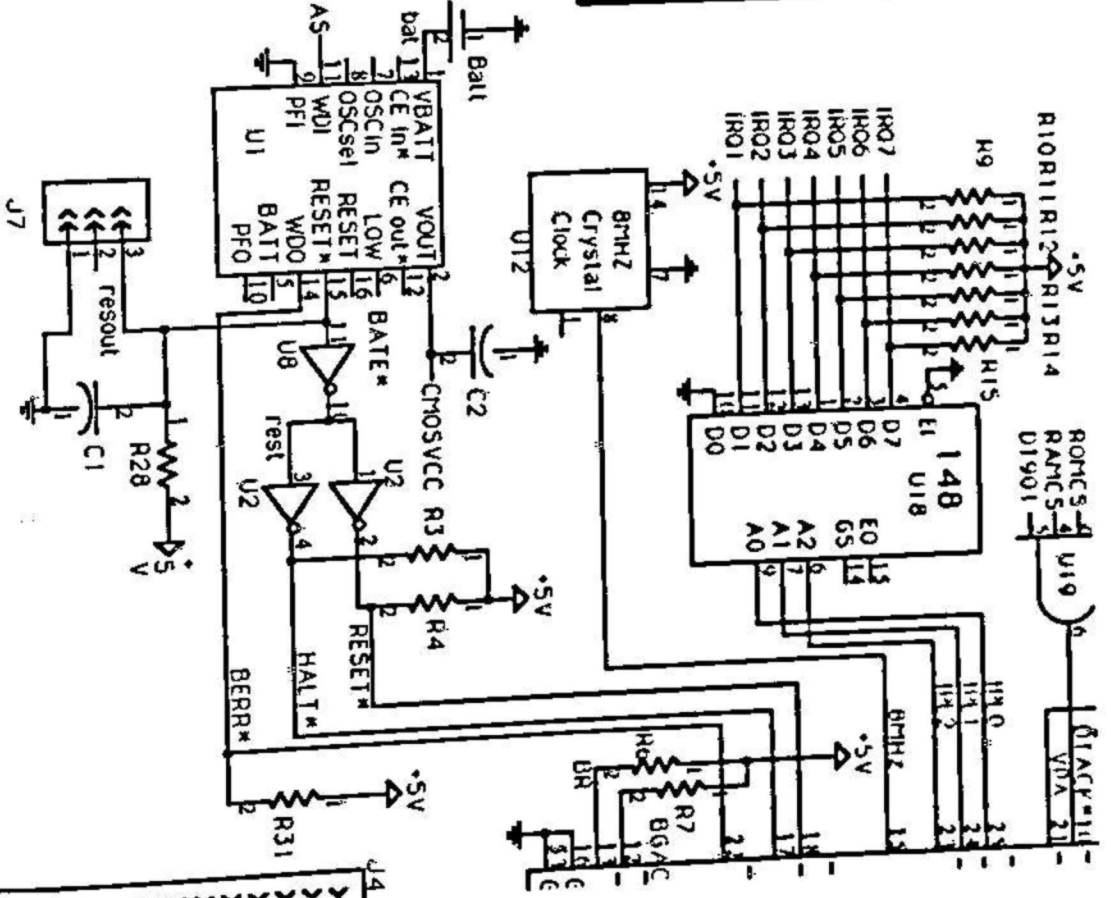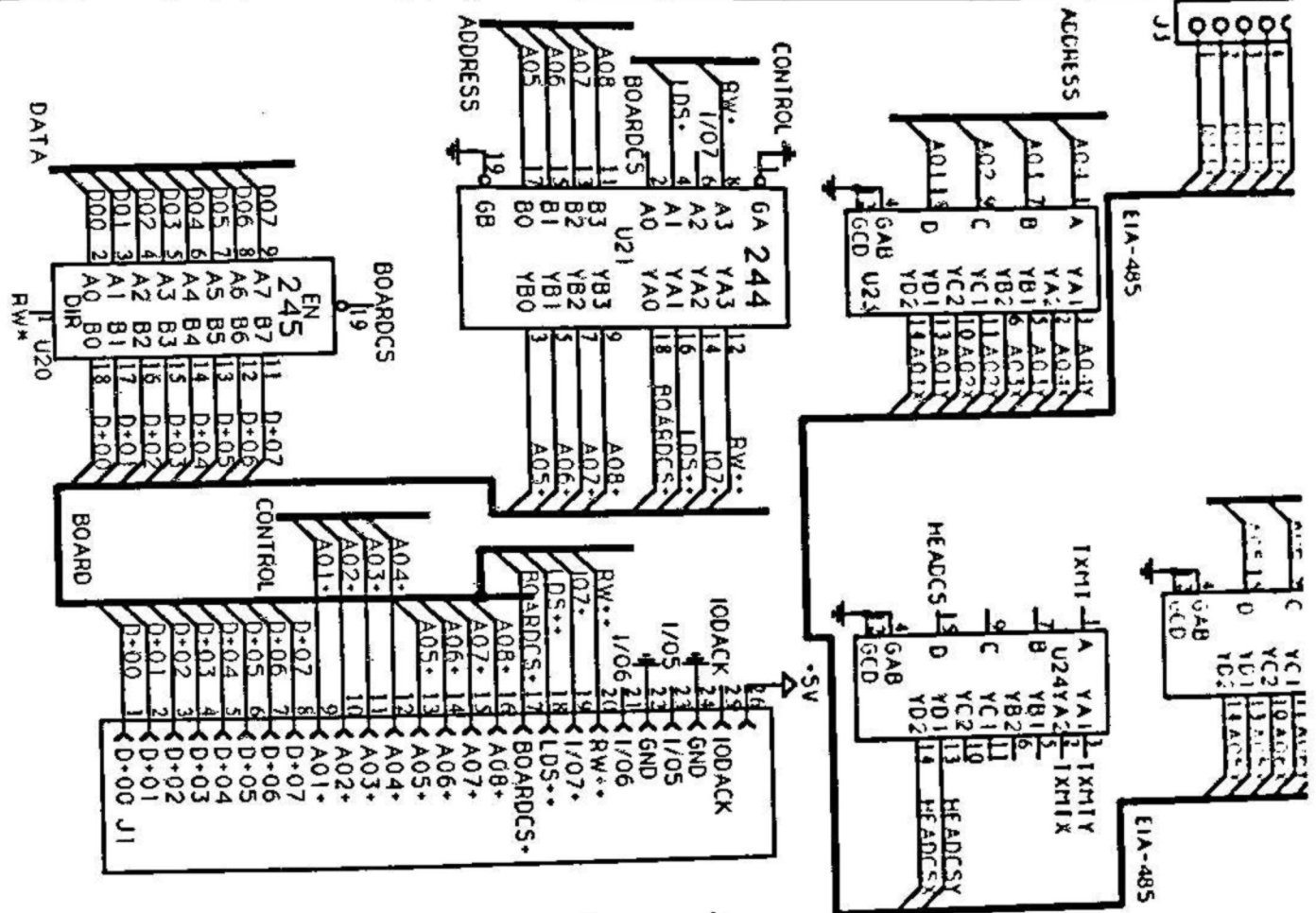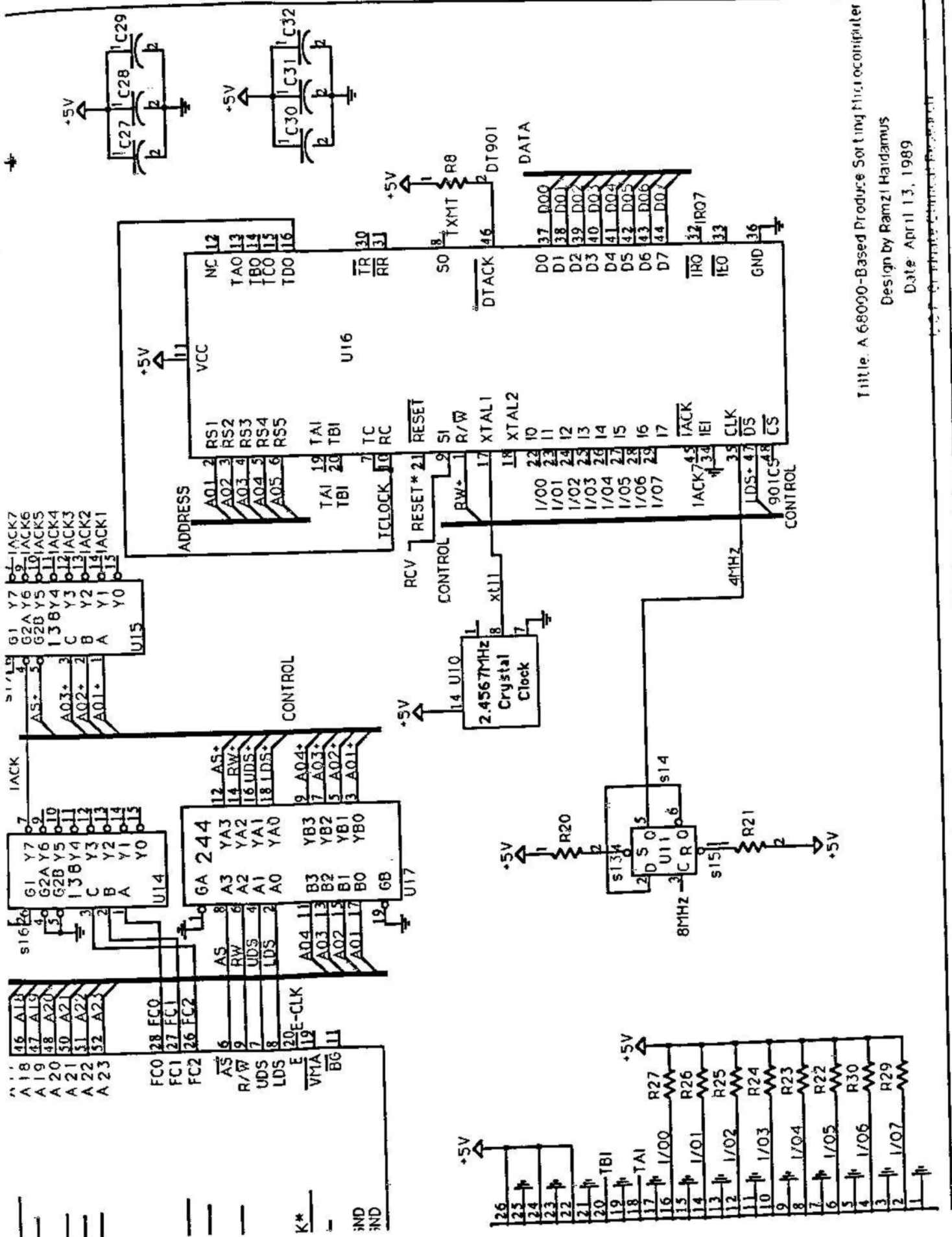
Title: A 68000-Based Produce Sorting Microcomputer

Design by Ramzi Haidamus

Date April 13, 1989

Appendix B

Part Description	Quantity	Unit Price	Cost	Source
100 µF Capacitor Axial/Polarized	1	.15	.15	Bourns
.1µf capacitor 100volts	32	.15	4.80	Bourns
Lithium Battery BR2325	1	3.95	3.95	Reovac
Socket for BR2325	1	.79	.79	Reovac
Right angle male double row DIP 26 Pins	4	.95	3.80	Jameco
4.7k Resistors 1/4 Watt Carbon	32	.05	1.60	Bourns
Hex Inverter w/ open collector	1	.19	.19	Texas Instruments
MC68000L8 8MHz CPU	1	9.95	9.95	Motorola
6264LP-10 CMOS RAM 100ns access	2	10.95	21.90	Texas Instruments
27C64-15 CMOS 8K ROM 150ns access	2	5.95	11.90	Texas Instruments
74HCT04 Inverter	1	.19	.19	Texas Instruments
74HCT32 OR Gate	1	.19	.19	Texas Instruments
74HCT74 Dual D Flip Flop	1	.29	.29	Texas Instruments
8MHz Oscillator TTL output	1	3.95	3.95	Texas Instruments
74HCT138 3/8 Decoder	3	.39	1.17	Texas Instruments
74HCT244 Octal Tri State noninverting Buffer	2	.59	1.18	Texas Instruments
74LS148 8-Line to 3-Line Priority Encoder	1	.99	.99	Texas Instruments
74HCT20 4-Input NAND Gates	1	.17	.17	Texas Instruments
74HCT245 Octal Bus Noninverting Transceiver	1	.69	.69	Texas Instruments
A96172 Quad EIA-485 Line drivers w/ 3-state output	3	2.95	8.85	Fairchild
A96173 Quad EIA-485 Line receivers w/3 state output	5	2.95	14.75	Fairchild
14 Pin low profile solder socket	5	.12	.60	Advanced
16 Pin low profile Solder Socket	13	.13	1.69	Advanced
20 Pin low profile Solder Socket	3	.19	.57	Advanced
28 Pin low profile Solder Socket	4	.27	1.08	Advanced
48 Pin low profile Solder Socket	1	1.69	1.69	Advanced
64 Pin low profile Solder Socket	1	2.14	2.14	Advanced
2.4576 MHz Oscillator TTL Output	1	7.40	7.40	ITT
68901LC Multi-Function Peripheral for 68000	1	5.00	5.00	Motorola
MAX695CPE Microprocessor Supervisory IC	1	4.00	4.00	MAXIM
TOTAL PARTS COST			93.72	
PARTS + BOARD = 93.72 + 33.39			127.11	HAGAN

MC68000 Board Parts List

Appendix C

DATE TASK	September			October			November			December			January		February		March	
	7	14	28	5	19	26	2	16	30	7	21	31	7	21	7	21	7	21
68000 Research																		
68901/230 Research																		
Peripheral Research																		
68000 Design																		
Order & receive Parts																		
Test Peripherals																		
Build & test Basic 68000																		
Test 68000 + peripherals																		
Learn P.C program																		
Design 68000 on P.C																		
Final Report																		

▨▨▨ Dependent on previous tasks

▨▨▨ Independent from previous tasks

Time Table for the 68000 project

Appendix D

```
                          1 "68000"
                          2
                          3
                          4 * This incredible program has been written to test the
                          5 * functions of the 68901 MFP  in the 68000 based system
                          6 * All IO pins are tested along with the timers.   Inerrupts
                          7 * will be tested later
                          8
        (00010000)        9 MFPBASE    EQU    00010000H
        (00010001)       10 GPDR       EQU    MFPBASE+01H     ;GENERAL PURPOSE IO REGISTER
        (00010003)       11 AER        EQU    MFPBASE+03H     ;ACTIVE EDGE REGISTER
        (00010005)       12 DDR        EQU    MFPBASE+05H     ;DATA DIRECTION REGISTER
        (00010007)       13 IERA       EQU    MFPBASE+07H     ;INTERRUPT ENABLE REGISTERS
        (00010009)       14 IERB       EQU    MFPBASE+09H     ;
        (0001000B)       15 IPRA       EQU    MFPBASE+0BH     ;INTERRUPT PENDING REGISTERS
Er      (0001000D)       16 IPRB       EQU    MFPBASE+0DH
        (0001000F)       17 ISRA       EQU    MFPBASE+0FH     ;INTERRUPT IN-SERVICE REGISTERS
        (00010011)       18 ISRB       EQU    MFPBASE+11H
        (00010013)       19 IMRA       EQU    MFPBASE+13H     ;INTERRUPT MASK REGISTERS
        (00010015)       20 IMRB       EQU    MFPBASE+15H
        (00010017)       21 VR         EQU    MFPBASE+17H     ;VECTOR REGISTER
        (00010019)       22 TACR       EQU    MFPBASE+19H     ;TIMER CONTROL REGISTERS
        (0001001B)       23 TBCR       EQU    MFPBASE+1BH
        (0001001D)       24 TCDCR      EQU    MFPBASE+1DH
        (0001001F)       25 TADR       EQU    MFPBASE+1FH     ;TIMER DATA REGISTERS
        (00010021)       26 TBDR       EQU    MFPBASE+21H
        (00010023)       27 TCDR       EQU    MFPBASE+23H
        (00010025)       28 TDDR       EQU    MFPBASE+25H
        (00010027)       29 SCR        EQU    MFPBASE+27H     ;SYNCHRONOUS CHARACTER REGISTER
        (00010029)       30 UCR        EQU    MFPBASE+29H     ;USART CONTROL REGISTER
        (0001002B)       31 RSR        EQU    MFPBASE+2BH     ;RECEIVER STATUS REGISTER
        (0001002D)       32 TSR        EQU    MFPBASE+2DH     ;TRANSMITTER STATUS REGISTER
        (0001002F)       33 UDR        EQU    MFPBASE+2FH     ;USART DATA REGISTER
                         34
                         35 *
                         36 *
                         37 *
                         38 *                   VECTOR ASSIGNMENTS
                         39 *
                         40                                   ;GPDR VECTORS
        (0040)           41 I0VEC      EQU    40H
        (0041)           42 I1VEC      EQU    41H
        (0042)           43 I2VEC      EQU    42H
        (0043)           44 I3VEC      EQU    43H
        (0046)           45 I4VEC      EQU    46H
        (0047)           46 I5VEC      EQU    47H
        (004E)           47 I6VEC      EQU    4EH
        (004F)           48 I7VEC      EQU    4FH
        (004D)           49 TIMERAVEC  EQU    4DH             ;TIMER A VECTOR
        (0048)           50 TIMERBVEC  EQU    48H             ;TIMER B VECTOR
        (0045)           51 TIMERCVEC  EQU    45H             ;TIMER C VECTOR
        (0049)           52 TR_ERRVEC  EQU    49H             ;TRANSMIT ERROR
        (004A)           53 TR_EMPVEC  EQU    4AH             ;TRANSMIT BUFFER EMPTY
        (004B)           54 RC_ERRVEC  EQU    4FH             ;RECEIVE ERROR
        (004C)           55 RECVEC     EQU    4CH             ;RECEIVER BUFFER FULL
                         56
                         57
```

LOCATION OBJECT CODE LINE   SOURCE LINE

```
                (0000)    58 NULL      EQU   0
                (000D)    59 CR        EQU   0DH
                (000A)    60 LF        EQU   0AH
                (0020)    61 SPACE     EQU   20H
                (003A)    62 COLON     EQU   3AH
                (0008)    63 BACKSPACE EQU   8
                          64
                          65          ORG 0
                          66
000000 0000 BFFE          67          DC.L 00000BFFEH
000004 0000 0500          68          DC.L 000000500H
                          69
                          70          ORG 0500H
                          71
000500 13FC 0000          72 INIT:     MOVE.B #0,IERA        ;DISABLE INTERRUPTS
000504 00010007
000508 13FC 0000          73          MOVE.B #0,IERB
00050C 00010009
000510 13FC 0040          74          MOVE.B #40H,VR         ;SET VECTOR REGISTER
000514 00010017
000518 13FC 0001          75          MOVE.B #01H,TADR       ;SET TIMER A TO DIVIDE BY 1
00051C 0001001F
000520 13FC 000C          76          MOVE.B #0CH,TACR       ;PRESCALER DIVIDE BY 50
000524 00010019
000528 13FC 0003          77          MOVE.B #3,TDDR         ;TIMER D DIVIDE BY 6
00052C 00010025
000530 13FC 0061          78          MOVE.B #61H,TCDCR      ;TIMER D DIVIDE BY 4 TO GET
000534 0001001D
                          79                                 ;4800 BAUD, TIMER C DIVIDE
                          80                                 ;BY 100 FOR FUN
000538 13FC 0098          81          MOVE.B #98H,UCR        ; UART 8 BITS, NO PARITY,
00053C 00010029
                          82                                 ; 2 STOP BITS, DIVIDE BY 16
000540 13FC 0001          83          MOVE.B #1,RSR          ;ENABLE RECEIVER
000544 0001002B
000548 13FC 0005          84          MOVE.B #5,TSR          ;ENABLE TRANSMITTER
00054C 0001002D
000550 13FC 00FF          85          MOVE.B #0FFH,DDR       ;ALL BIT ARE OUTPUT
000554 00010005
000558 207C               86          MOVEA.L #GPDR,A0       ;MFP IO PORT ADDRESS
00055A 00010001
00055E 227C               87          MOVEA.L #RSR,A1
000560 0001002B
000564 247C               88          MOVEA.L #TSR,A2
000566 0001002D
00056A 267C               89          MOVEA.L #UDR,A3
00056C 0001002F
000570 103C 0041          90          MOVE.B #41H,D0         ;LOAD AN "A"
000574 143C 0000          91          MOVE.B #0,D2           ;CLEAR PORT COUNTER
                          92
000578                    93 LOOP
000578 4EB9 0000          94          JSR    OUTCHR
00057C 0590
00057E 5202               95          ADDQ.B #1,D2           ;INCREMENT COUNTER
000580 1082               96          MOVE.B D2,[A0]         ;INCREMENT PORT
000582 4EB9 0000          97          JSR    INCHARTST
000586 059C
```

LOCATION OBJECT CODE LINE   SOURCE LINE

```
0005B8  6702         98              BEQ.S   AGAIN
0005BA  1013         99              MOVE.B  [A3],D0
0005BC  4EF8 0578    100 AGAIN:      JMP LOOP
000590               101 OUTCHR:
000590  1212         102             MOVE.B  [A2],D1        ;READ TRANSMITTER
000592  0801 0007    103             BTST    #7,D1          ;IS BUFFER EMPTY
000596  67FB         104             BEQ.S   OUTCHR         ;WAIT FOR TRANSMISION
000598  1680         105             MOVE.B  D0,[A3]        ;SEND CHARACTER
                     106
00059A  4E75         107             RTS                    ;RETURN FROM SUBROUTINE
00059C               108 INCHARTST:
00059C  1211         109             MOVE.B  [A1],D1        ;READ RECEIVER
00059E  0201 0080    110             AND.B   #80H,D1
0005A2  4E75         111             RTS
```

Errors=   0

Appendix E
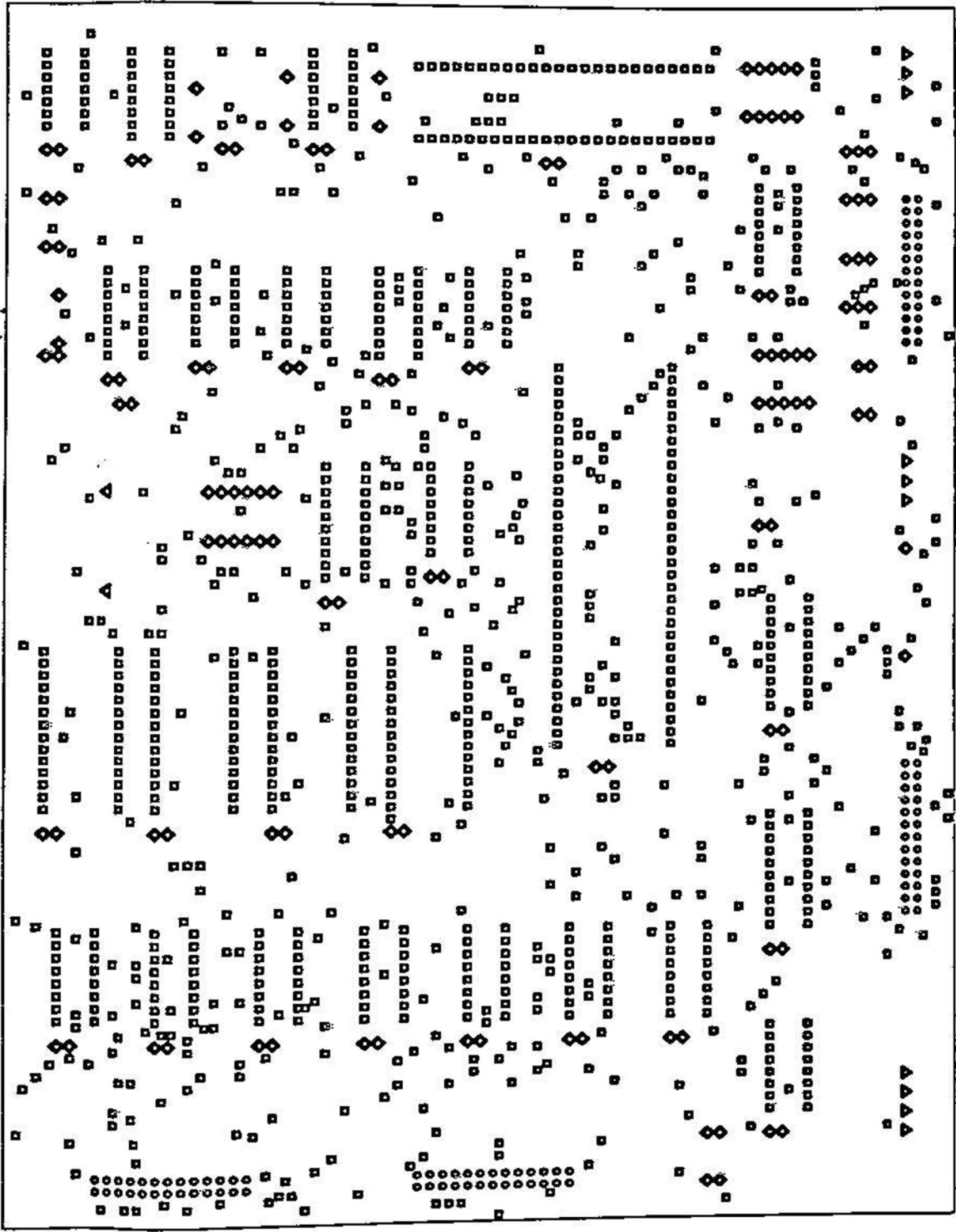
68 TRESKIPOI

Appendix F

R3 R4
C1
R28
C31 U1
C2
Batt
R31 R18 R17 R16
C17 U17
C13 U13

C7 U7
C3 U5
C6 U6
C4 U4

C32 U2
C15 U15
R18
C10 U10
R20
C11 U11
R21

C8 U8
C19 U19
C14 U14
C9 U9

C30 U3

R11 R12 R13 R14 R15
J7
R25 R27 R26
R22 R23 R24
J4
R5 C8 R6 R7 R9 R10 U18
R30 R29

C16

U16

C12 U12
J5
C9

C20 U20
C1 U1

J1
C21 U21
J6

C29 U29
C28 U28
C27 U27
C25 U25
C23 U23
C22 U22
C26 U26
R1
C24 U24

J2
J3
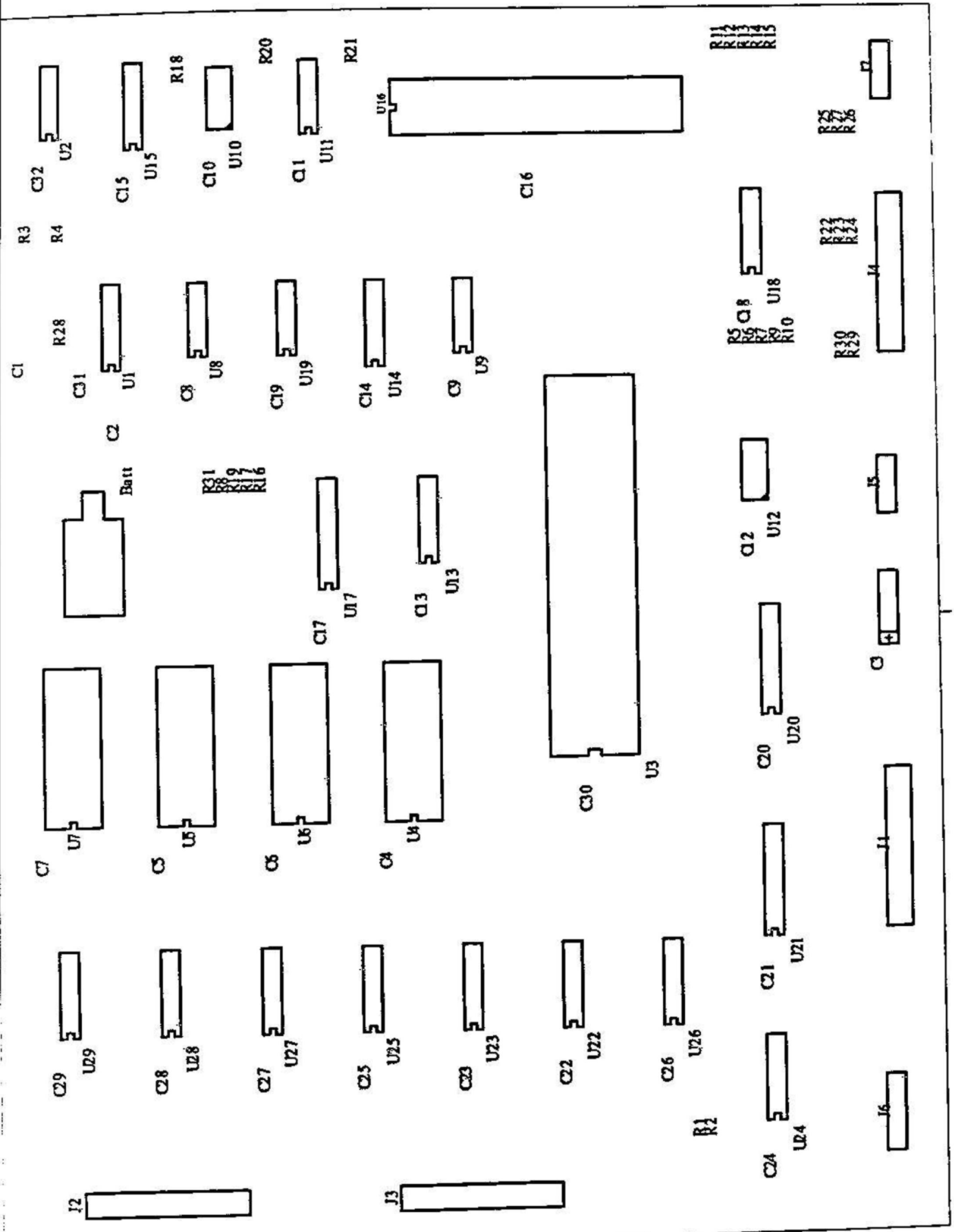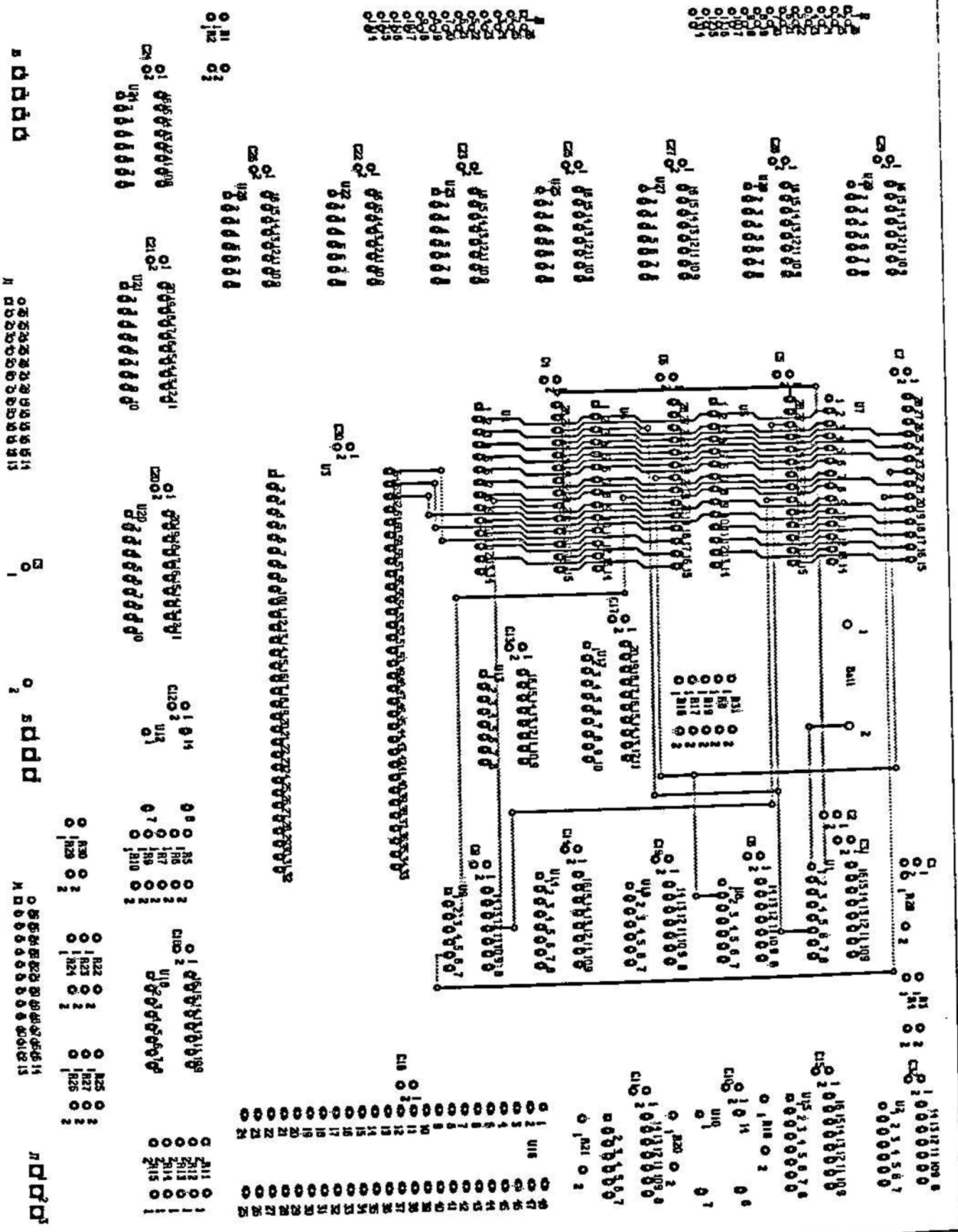
Appendix G

Appendix H

Appendix I

Appendix J

Appendix K

Appendix L

NETLIST

```
+5V        C3-1 C4-1 C5-1 C6-1 C7-1 C8-1 C9-1 C10-1 C11-1 C12-1
C13-1 C14-1 C15-1 C16-1 C17-1 C18-1 C19-1 C20-1 C21-1 C22-1 C23-1
C24-1 C25-1 C26-1 C27-1 C28-1 C29-1 C30-1 C31-1 C32-1 J1-26 J4-22
J4-24 J4-26 J5-2 R2-1 R3-1 R4-1 R5-1 R6-1 R7-1 R8-1 R9-1 R10-1 R11-1
R12-1 R13-1 R14-1 R15-1 R16-1 R17-1 R18-1 R19-1 R20-1 R21-2 R22-1
R23-1 R24-1 R25-1 R26-1 R27-1 R28-2 R29-1 R30-1 R31-1 U1-3 U2-14
U3-14 U3-49 U6-1 U6-27 U6-28 U7-1 U7-27 U7-28 U8-14 U9-14 U10-14
U11-14 U12-14 U13-16 U14-16 U15-16 U16-11 U17-20 U18-16 U19-14 U20-20
U21-20 U22-16 U23-16 U24-16 U25-16 U26-16 U27-16 U28-16 U29-16
D03Y       J2-8 U27-1
D04X       J2-9 U28-10
D10X       J2-21 U29-14
D15        U3-54 U5-19 U7-19 U25-3
D14        U3-55 U5-18 U7-18 U25-13
D13        U3-56 U5-17 U7-17 U25-5
D12        U3-57 U5-16 U7-16 U25-11
D11        U3-58 U5-15 U7-15 U29-3
D10        U3-59 U5-13 U7-13 U29-13
D08        U3-61 U5-11 U7-11 U29-11
D09        U3-60 U5-12 U7-12 U29-5
s10        U8-6 U13-6
h2         R17-2 U19-10
RW+        U4-27 U5-27 U8-1 U16-1 U17-14 U21-8
HEADCS     U13-12 U24-15 U25-12 U27-12 U28-12 U29-12
HEADACK    U19-13 U26-3
LDS++      J1-18 U21-16
UDS        U3-7 U17-4
RAMCS      U9-13 U9-10 U13-14 U19-4
ROMCS      U9-4 U9-1 U13-15 U19-2
UDS+       U9-12 U9-5 U17-16
RW         U3-9 U17-6
4MHz       U11-5 U16-35
8MHz       U3-15 U11-3 U12-8
901CS      U13-13 U16-48
A01        U3-29 U4-10 U5-10 U6-10 U7-10 U16-2 U17-17 U23-15
A01+       J1-9 U15-1 U17-3
A01X       J3-11 U23-14
A01Y       J3-12 U23-13
A02        U3-30 U4-9 U5-9 U6-9 U7-9 U16-3 U17-15 U23-9
A02+       J1-10 U15-2 U17-5
A02X       J3-13 U23-10
A02Y       J3-14 U23-11
A03        U3-31 U4-8 U5-8 U6-8 U7-8 U16-4 U17-13 U23-7
A03+       J1-11 U15-3 U17-7
A03X       J3-15 U23-6
A03Y       J3-16 U23-5
A04        U3-32 U4-7 U5-7 U6-7 U7-7 U16-5 U17-11 U23-1
A04X       J3-17 U23-2
A04Y       J3-18 U23-3
A05        U3-33 U4-6 U5-6 U6-6 U7-6 U16-6 U21-17 U22-15
A05+       J1-13 U21-3
A05X       J3-19 U22-14
A05Y       J3-20 U22-13
A06        U3-34 U4-5 U5-5 U6-5 U7-5 U21-15 U22-9
```
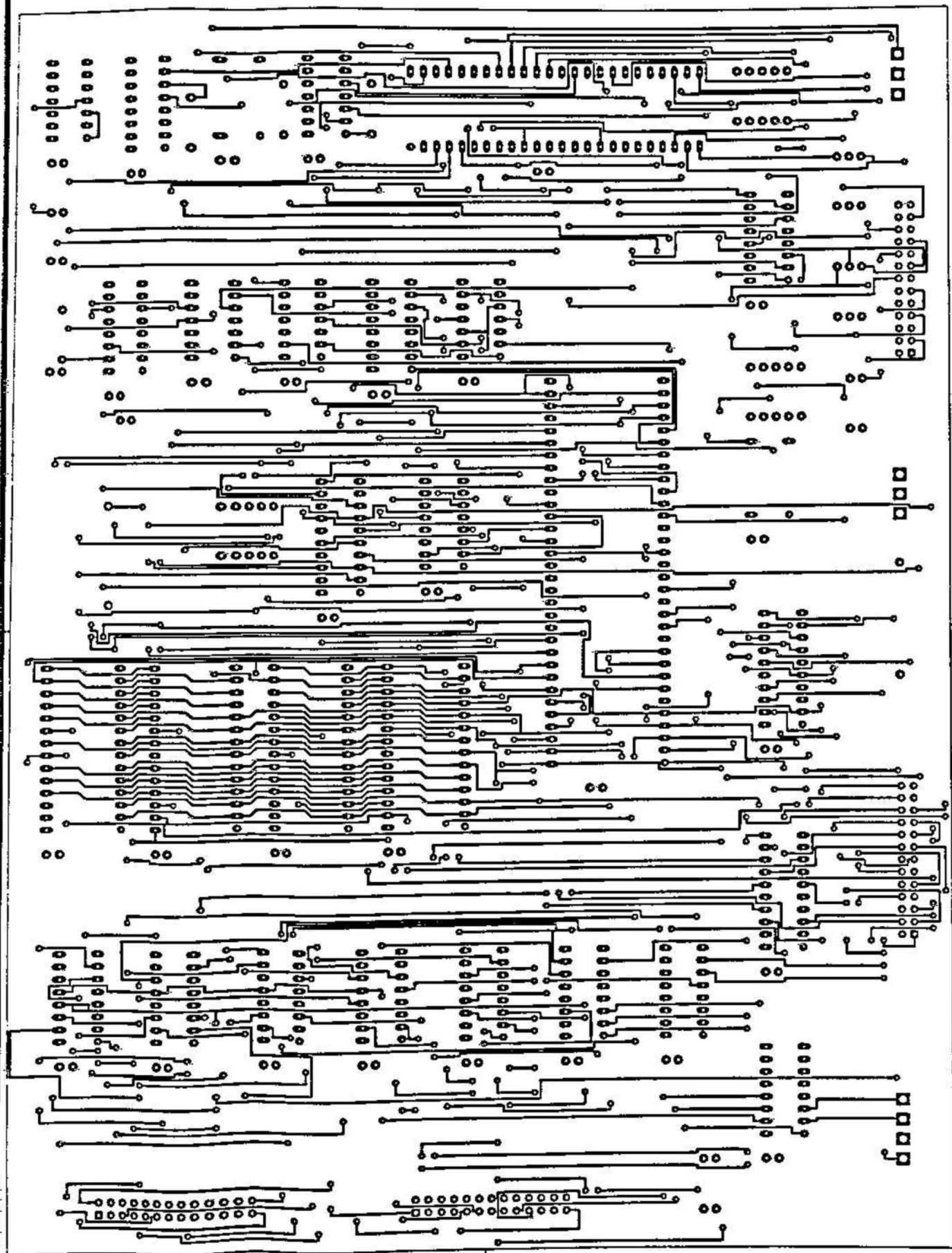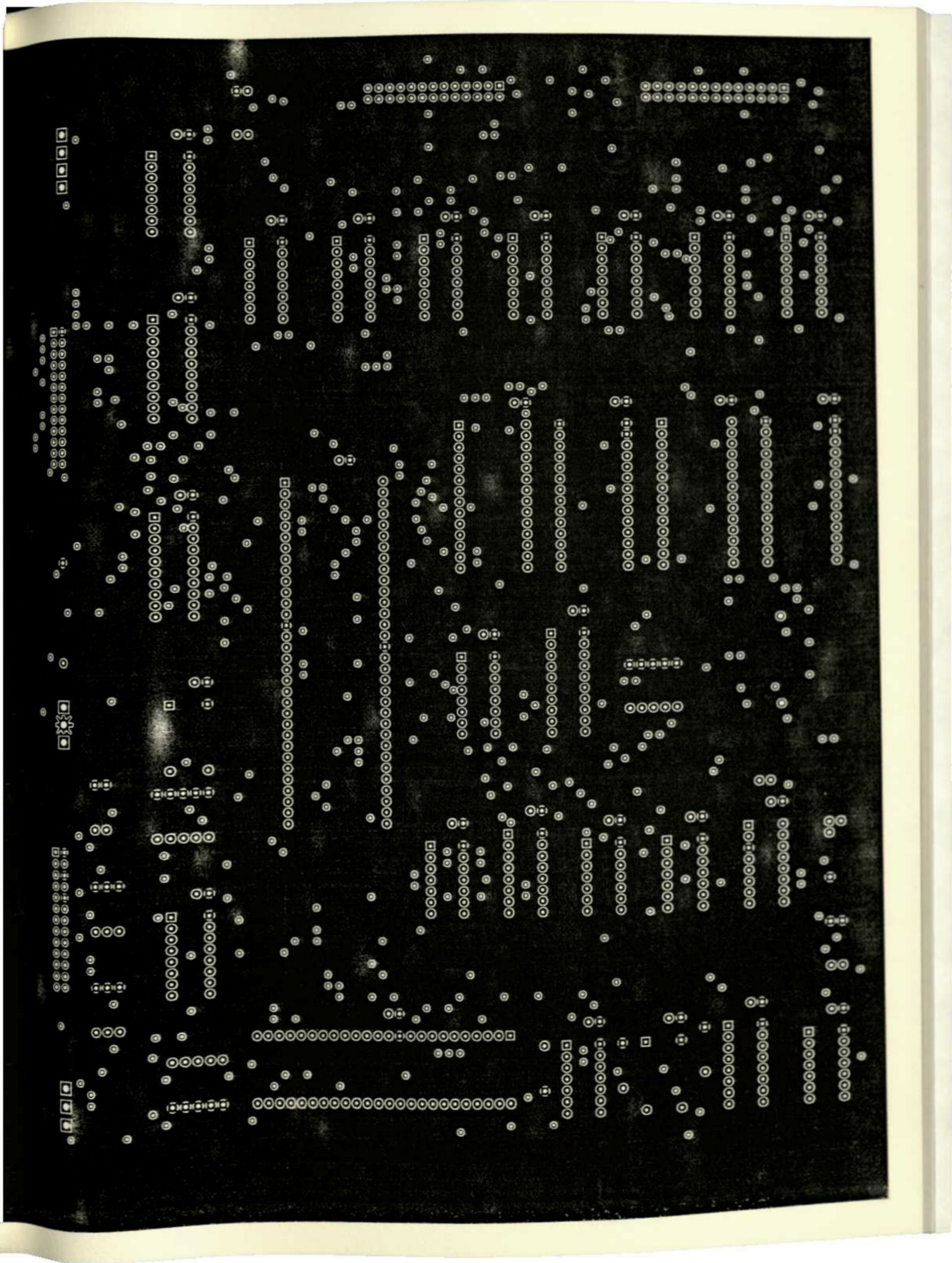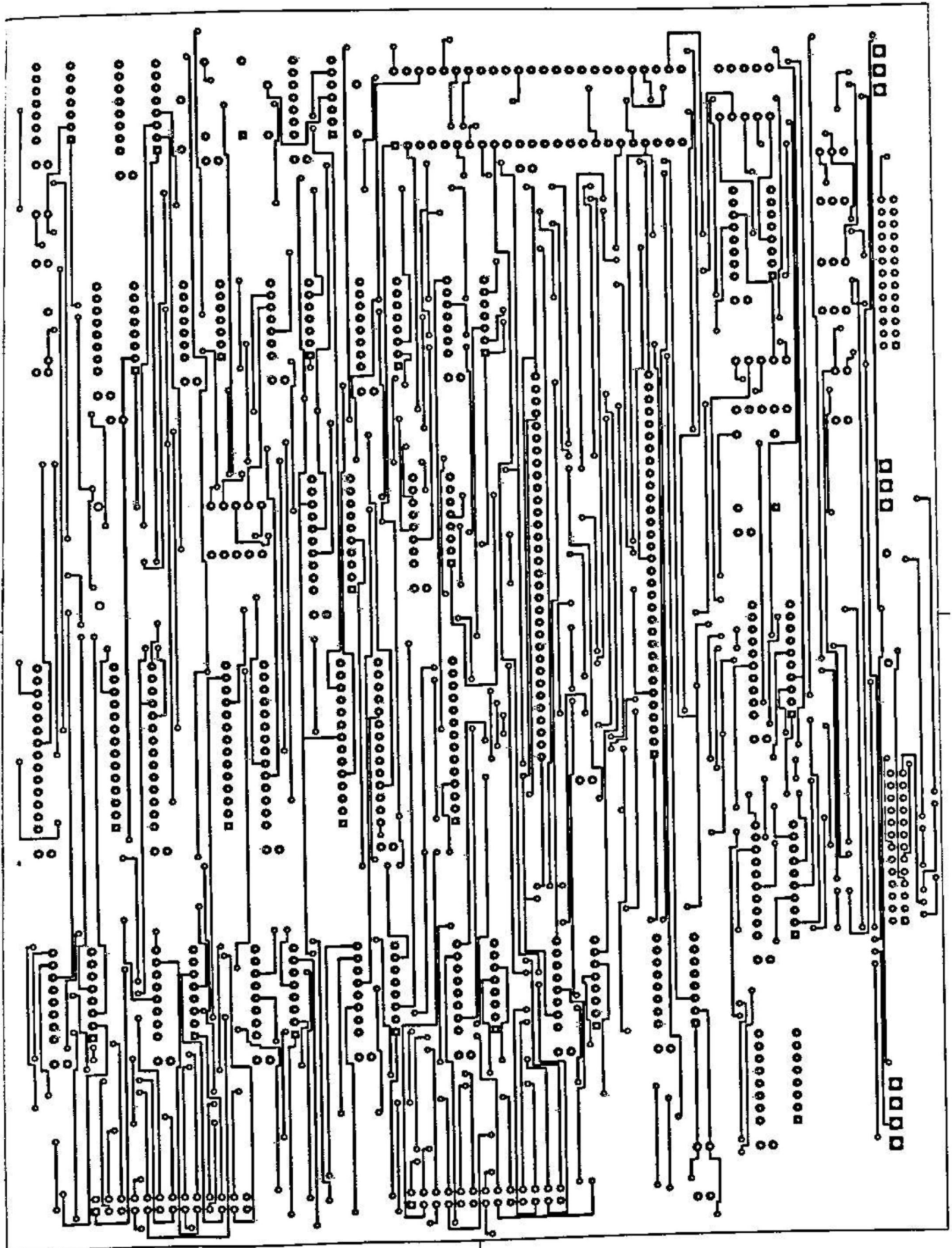
```
A06+        J1-14 U21-5
A06X        J3-21 U22-10
A06Y        J3-22 U22-11
A07         U3-35 U4-4 U5-4 U6-4 U7-4 U21-13 U22-7
A07+        J1-15 U21-7
A07X        J3-23 U22-6
A07Y        J3-24 U22-5
A08         U3-36 U4-3 U5-3 U6-3 U7-3 U21-11 U22-1
A08+        J1-16 U21-9
A08X        J3-25 U22-2
A08Y        J3-26 U22-3
A09         U3-37 U4-25 U5-25 U6-25 U7-25
A10         U3-38 U4-24 U5-24 U6-24 U7-24
A11         U3-39 U4-21 U5-21 U6-21 U7-21
A12         U3-40 U4-23 U5-23 U6-23 U7-23
A13         U3-41 U4-2 U5-2 U6-2 U7-2
A15         U3-43 U13-1
A16         U3-44 U13-2
A17         U3-45 U13-3
A18         U3-46 U13-4
A19         U3-47 U8-5
AS          U1-11 U3-6 U17-8
AS+         U13-5 U15-5 U17-12
BATE*       U1-6 U4-26 U5-26
BERR*       R31-2 U1-14 U3-22
BGACK*      R7-2 U3-12
BOARDCS     U13-11 U20-19 U21-2
BOARDCS+    J1-17 U21-18
BR          R6-2 U3-13
CMOSVCC     C2-2 U1-2 U4-28 U5-28
D+00        J1-1 U20-18
D+01        J1-2 U20-17
D+02        J1-3 U20-16
D+03        J1-4 U20-15
D+04        J1-5 U20-14
D+05        J1-6 U20-13
D+06        J1-7 U20-12
D+07        J1-8 U20-11
D00         U3-5 U4-11 U6-11 U16-37 U20-2 U27-11
D00X        J2-1 U27-10
D00Y        J2-2 U27-9
D01         U3-4 U4-12 U6-12 U16-38 U20-3 U27-5
D01X        J2-3 U27-6
D01Y        J2-4 U27-7
D02         U3-3 U4-13 U6-13 U16-39 U20-4 U27-13
D02X        J2-5 U27-14
D02Y        J2-6 U27-15
D03         U3-2 U4-15 U6-15 U16-40 U20-5 U27-3
D03X        J2-7 U27-2
D04         U3-1 U4-16 U6-16 U16-41 U20-6 U28-11
D04Y        J2-10 U28-9
D05         U3-64 U4-17 U6-17 U16-42 U20-7 U28-5
D05X        J2-11 U28-6
D05Y        J2-12 U28-7
D06         U3-63 U4-18 U6-18 U16-43 U20-8 U28-13
D06X        J2-13 U28-14
D06Y        J2-14 U28-15
D07         U3-62 U4-19 U6-19 U16-44 U20-9 U28-3
```

```
D07X       J2-15 U28-2
D07Y       J2-16 U28-1
D08X       J2-17 U29-10
D08Y       J2-18 U29-9
D09X       J2-19 U29-6
D09Y       J2-20 U29-7
D10Y       J2-22 U29-15
D11X       J2-23 U29-2
D11Y       J2-24 U29-1
D12X       J2-25 U25-10
D12Y       J2-26 U25-9
D13X       J3-1 U25-6
D13Y       J3-2 U25-7
D14X       J3-3 U25-14
D14Y       J3-4 U25-15
D15X       J3-5 U25-2
D15Y       J3-6 U25-1
DT901      R8-2 U16-46 U19-5
DTACK*     U3-10 U19-6
DTACKX     J3-7 R2-2 U26-2
DTACKY     J3-8 R1-2 U26-1
FC0        U3-28 U14-1
FC1        U3-27 U14-2
FC2        U3-26 U14-3
Ground     Batt-1 C1-1 C2-1 C3-2 C4-2 C5-2 C6-2 C7-2 C8-2 C9-2
           C10-2 C11-2 C12-2 C13-2 C14-2 C15-2 C16-2 C17-2 C18-2 C19-2 C20-2
           C21-2 C22-2 C23-2 C24-2 C25-2 C26-2 C27-2 C28-2 C29-2 C30-2 C31-2
           C32-2 J1-22 J1-24 J4-1 J4-3 J4-5 J4-7 J4-9 J4-11 J4-13 J4-15 J4-17
           J4-19 J4-21 J4-23 J4-25 J5-1 J5-3 J7-1 R1-1 U1-4 U1-9 U2-7 U3-16
           U3-53 U4-14 U4-22 U5-14 U5-22 U6-14 U7-14 U8-7 U9-7 U10-7 U11-7 U12-7
           U13-8 U14-4 U14-5 U14-8 U15-8 U16-34 U16-36 U17-1 U17-10 U17-19 U18-5
           U18-8 U18-10 U19-7 U20-10 U21-1 U21-10 U21-19 U22-4 U22-8 U22-12
           U23-4 U23-8 U23-12 U24-4 U24-8 U24-12 U25-4 U25-8 U26-4 U26-8 U26-12
           U27-4 U27-8 U28-4 U28-8 U29-4 U29-8
HALT*      R3-2 U2-4 U3-17
HEADCSX    J3-9 U24-14
HEADCSY    J3-10 U24-13
I/O0       J4-16 R27-2 U16-22
I/O1       J4-14 R26-2 U16-23
I/O2       J4-12 R25-2 U16-24
I/O3       J4-10 R24-2 U16-25
I/O4       J4-8 R23-2 U16-26
I/O5       J1-23 J4-6 R22-2 U16-27
I/O6       J1-21 J4-4 R30-2 U16-28
I/O7       J4-2 R29-2 U16-29 U21-6
IACK       U14-7 U15-4
IACK7      U15-7 U16-45
IO7+       J1-19 U21-14
IODACK     J1-25 U19-12
IPL0       U3-25 U18-9
IPL1       U3-24 U18-7
IPL2       U3-23 U18-6
IRQ1       R9-2 U18-11
IRQ2       R10-2 U18-12
IRQ3       R11-2 U18-13
IRQ4       R12-2 U18-1
IRQ5       R13-2 U18-2
IRQ6       R14-2 U18-3
```

```
IRQ7        R15-2 U16-32 U18-4
LDS         U3-8 U17-2
LDS+        U9-9 U9-2 U16-47 U17-18 U21-4
RCV         U16-9 U26-5
RCVX        J6-1 U26-6
RCVY        J6-2 U26-7
RESET*      R4-2 U2-2 U3-18 U16-21
RL          U4-20 U9-8
RU          U5-20 U9-11
RW*         U6-22 U7-22 U8-2 U20-1
RW++        J1-20 U21-12
S00002      U19-8 U19-1
TAI         J4-18 U16-19
TBI         J4-20 U16-20
TCLOCK      U16-7 U16-10 U16-16
TXMT        U16-8 U24-1
TXMTX       J6-3 U24-2
TXMTY       J6-4 U24-3
VPA         R5-2 U3-21
bat         Batt-2 U1-1
ce1         U6-20 U9-3
ce2         U7-20 U9-6
h1          R16-2 U19-9
resout      C1-2 J7-3 R28-1 U1-15 U8-11
rest        U2-3 U2-1 U8-10
s13         R20-2 U11-4
s14         U11-2 U11-6
s15         R21-1 U11-1
s16         R19-2 U14-6
s17         R18-2 U15-6
xtl1        U10-8 U16-17
```

PARTS

Batt	Battery RC805 Battery	BR2325
C1	Capacitor RC100 Cap	$.1\mu f$
C2	Capacitor RC100 Cap	$.1\mu f$
C3	Capacitor RC900 Cap+	$100\mu f/16V$
C4	Capacitor RC100 Cap	$.1\mu f$
C5	Capacitor RC100 Cap	$.1\mu f$
C6	Capacitor RC100 Cap	$.1\mu f$
C7	Capacitor RC100 Cap	$.1\mu f$
C8	Capacitor RC100 Cap	$.1\mu f$
C9	Capacitor RC100 Cap	$.1\mu f$
C10	Capacitor RC100 Cap	$.1\mu f$
C11	Capacitor RC100 Cap	$.1\mu f$
C12	Capacitor RC100 Cap	$.1\mu f$
C13	Capacitor RC100 Cap	$.1\mu f$
C14	Capacitor RC100 Cap	$.1\mu f$
C15	Capacitor RC100 Cap	$.1\mu f$
C16	Capacitor RC100 Cap	$.1\mu f$
C17	Capacitor RC100 Cap	$.1\mu f$
C18	Capacitor RC100 Cap	$.1\mu f$
C19	Capacitor RC100 Cap	$.1\mu f$
C20	Capacitor RC100 Cap	$.1\mu f$

C21	Capacitor RC100 Cap	.1μf			
C22	Capacitor RC100 Cap	.1μf			
C23	Capacitor RC100 Cap	.1μf			
C24	Capacitor RC100 Cap	.1μf			
C25	Capacitor RC100 Cap	.1μf			
C26	Capacitor RC100 Cap	.1μf			
C27	Capacitor RC100 Cap	.1μf			
C28	Capacitor RC100 Cap	.1μf			
C29	Capacitor RC100 Cap	.1μf			
C30	Capacitor RC100 Cap	.1μf			
C31	Capacitor RC100 Cap	.1μf			
C32	Capacitor RC100 Cap	.1μf			
J1	26 Pin Connector DIP26 CONCT26				
J2	26 Pin Connector DIP26 PIN26				
J3	26 Pin Connector DIP26 PIN26				
J4	26 Pin Connector J26H J26H				
J5	3 Pin Plug 3PLUG 3PLUG				
J6	4 pin Plug 4PLUG J6				
J7	3 Pin Plug 3PLUG 3PLUG				
R1	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R2	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R3	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R4	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R5	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R6	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R7	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R8	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R9	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R10	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R11	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R12	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R13	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R14	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R15	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R16	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R17	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R18	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R19	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R20	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R21	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R22	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R23	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R24	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R25	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R26	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R27	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R28	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R29	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R30	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
R31	Resistor RC400 RES	$4.7k\Omega$	Pacom	1/4 Watt Carbon Film
U1	MAX691 DIP16 MAX691		MAXIM	
U2	74HCT05 DIP14 NOT		Texas Instruments Plastic Package	
U2	74HCT05 NOT			
U3	MC68000L8 DIP64 68000		Motorola	
U4	MCM6164P55 DIP28 6164		Motorola Plastic Package	
U5	MCM6164P55 DIP28 6164		Motorola Plastic Package	
U6	TMS 2764-20JL DIP28 2764		Texas Instruments Ceramic Package	
U7	TMS 2764-20JL DIP28 2764		Texas Instruments Ceramic Package	

```
U8    74HCT04   DIP14 NOT            Texas Instruments Plastic Package
U8    74HCT04        NOT
U8    74HCT04        NOT
U9    74HCT32        OR-2
U9    74HCT32   DIP14 OR-2           Texas Instruments Plastic Package
U9    74HCT32        OR-2
U9    74HCT32        OR-2
U10   2.4576MHz Oscillator OSC14 2.4576 Crystal  ITT
U11   74HCT74   DIP14 DFF            Texas Instruments Plastic Package
U12   8MHz Oscillator OSC14 8Mhz Crystal    ITT
U13   74HCT138  DIP16 138            Texas Instruments Plastic Package
U14   74HCT138  DIP16 138            Texas Instruments Plastic Package
U15   74HCT138  DIP16 138            Texas Instruments Plastic Package
U16   MC68901L  DIP48 MC68901          Motorola  Plastic Package
U17   74HCT244  DIP20 244            Texas Instruments Plastic Package
U18   74LS148   DIP16 148          Texas Instruments Plastic Package
U19   74HCT21   DIP14 AND-4           Texas Instruments Plastic Package
U19             AND-4
U20   74HCT245  DIP20 245
U21   74HCT244  DIP20 244            Texas Instruments Plastic Package
U22   A96172   DIP16 422 DRIVER        Fairchild Plastic Package
U23   A96172   DIP16 422 DRIVER        Fairchild
U24   A96172   DIP16 422 DRIVER        Fairchild
U25   A96173   DIP16 422 RECEIVER       Fairchild Plastic Package
U26   A96173   DIP16 422 RECEIVER       Fairchild
U27   A96173   DIP16 422 RECEIVER       Fairchild
U28   A96173   DIP16 422 RECEIVER       Fairchild
U29   A96173   DIP16 422 RECEIVER       Fairchild
```

ROUTER

* Set Spacing on all layers
GRID = 25
WIDTH = 12
TOLERANCE = 5

* Set Solder side
LAYER 0
VERT = 10
HORZ = 1
BEND = 8

* Set Component side
LAYER 1
VERT = 1
HORZ = 10
BEND = 8

* Set colors
LAYER 0 RED
LAYER 1 GREEN

* Select all layers again
LAYER ALL
BURY 0

* Name the files

```
REPORT RouteReport.68
LOAD LABEL "68000 Layout"
LOAD BARRIER 0,1 "68000 BAR"
LOAD BARRIER 2,3 "68000 BAR GRND"
SAVE 0,1 "68000.TRCS.0.1"
SAVE 2,3 "68000.GRND.2.3"

* Indicate prerouted nodes
JUMPER U4-10 TO U5-10 TO U6-10 TO U7-10
JUMPER U4-9 TO U5-9 TO U6-9 TO U7-9
JUMPER U4-8 TO U5-8 TO U6-8 TO U7-8
JUMPER U4-7 TO U5-7 TO U6-7 TO U7-7
JUMPER U4-6 TO U5-6 TO U6-6 TO U7-6
JUMPER U4-5 TO U5-5 TO U6-5 TO U7-5
JUMPER U4-4 TO U5-4 TO U6-4 TO U7-4
JUMPER U4-3 TO U5-3 TO U6-3 TO U7-3
JUMPER U4-25 TO U5-25 TO U6-25 TO U7-25
JUMPER U4-24 TO U5-24 TO U6-24 TO U7-24
JUMPER U4-21 TO U5-21 TO U6-21 TO U7-21
JUMPER U4-23 TO U5-23 TO U6-23 TO U7-23
JUMPER U4-2 TO U5-2 TO U6-2 TO U7-2
JUMPER U4-11 TO U6-11
JUMPER U4-12 TO U6-12
JUMPER U4-13 TO U6-13
JUMPER U4-15 TO U6-15
JUMPER U4-16 TO U6-16
JUMPER U4-17 TO U6-17 TO U3-64
JUMPER U4-18 TO U6-18 TO U3-63
JUMPER U4-19 TO U6-19 TO U3-62
JUMPER U5-11 TO U7-11
JUMPER U5-12 TO U7-12
JUMPER U5-13 TO U7-13
JUMPER U5-15 TO U7-15
JUMPER U5-16 TO U7-16
JUMPER U5-17 TO U7-17
JUMPER U5-18 TO U7-18
JUMPER U5-19 TO U7-19
JUMPER U6-22 TO U7-22 TO U8-2
JUMPER U4-26 TO U5-26 TO U1-6
JUMPER U4-28 TO U5-28 TO U1-2 TO C2-2
JUMPER U4-20 TO U9-8
JUMPER U5-20 TO U9-11
JUMPER Batt-2 TO U1-1
JUMPER U6-20 TO U9-3
JUMPER U7-20 TO U9-6

* Show the Rats nest
DRAW RAT

* Report
PRINT Routed by Ramzi's Method
CHECK
DRAW

* Route Ground planes
TITLE "Ground Planes"
SHORTBAR 95
PLANE 2 ONLY Ground
```

```
SHORTBAR 96
PLANE 3 ONLY +5V

DRAW

* No Traces on ground planes
 LAYER 2,3 OFF
LAYER 0,1 ON

* 1st Pass
ORTHO ON
CLEARANCE 100
PITCH 100
THRU 20
*Route
TITLE 1ST PASS
ROUTE

DRAW RAT


* 2ND Pass
ORTHO OFF
TITLE 2ND PASS
ROUTE
BEEP
BEEP
BEEP

* 3RD Pass
CLEARANCE 0
PITCH 25
TITLE 3RD PASS
ROUTE

DRAW RAT

* LAST PAST
BEND 3
THRU 3
LAYER 0
VERT = 2
HORZ = 1
LAYER 1
VERT = 1
HORZ = 2

TITLE LAST PASS
ROUTE
BEEP
BEEP
BEEP
DRAW

PAUSE 4
CYAN
DRAW RAT
```

```
PAUSE 5
END

***DONE***
```

Appendix M

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