Complementary Metal-Oxide Semiconductor and Memristive Hardware for Neuromorphic Computing

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The ever-increasing processing power demands of digital computers cannot continue to be fulfilled indefinitely unless there is a paradigm shift in computing. Neuromorphic computing, which takes inspiration from the highly parallel, low-power, high-speed, and noise-tolerant computing capabilities of the brain, may provide such a shift. Many researchers from across academia and industry have been studying materials, devices, circuits, and systems, to implement some of the functions of networks of neurons and synapses to develop neuromorphic computing platforms. These platforms are being designed using various hardware technologies, including the well-established complementary metal-oxide semiconductor (CMOS), and emerging memristive technologies such as SiO_x-based memristors. Herein, recent progress in CMOS, SiO_x-based memristive, and mixed CMOS-memristive hardware for neuromorphic systems is highlighted. New and published results from various devices are provided that are developed to replicate selected functions of neurons, synapses, and simple spiking networks. It is shown that the CMOS and memristive devices are assembled in different neuromorphic learning platforms to perform simple cognitive tasks such as classification of spike rate-based patterns or handwritten digits. Herein, it is envisioned that what is demonstrated is useful to the unconventional computing research community by providing insights into advances in neuromorphic hardware technologies.

1. Introduction

Conventional computing that involves storing data in, and retrieving it from, memory results in numerous interactions between the slow memory and the fast processors. In addition, the data movement between memory and processor produce a bottleneck that is limited by the available bandwidth in the computing platform used.[1–3] This significantly affects the computation speed, in particular when a large amount of data is to be processed in a short time. Furthermore, the excessive data movement in conventional sequential- and parallel-processing computers results in very high power consumption. Even though supercomputers with highly parallel processing capabilities are presently used to satisfy the high throughput of computationally complex tasks, they are extremely power hungry.[4]

The prevalence of big data and a need for low-power and high-speed processing in everyday life and edge computing devices demands a shift to computers with elevated capabilities but with low power consumption. This may be achieved through unconventional computing methods,[5] among

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which neuromorphic computing is a promising approach, where engineering inspirations are taken from the noise-tolerant, parallel, low-power, and high-speed signal processing abilities of biological brains.[6]

Neuromorphic computing was coined by Mead,[7] when he envisioned that while exploiting the similarities between semiconductor physics and biological neural systems, one may develop brain-inspired computing platforms. Ever since, neuromorphic research has evolved and researchers are implementing various technologies, from conventional semiconductors, as proposed by Mead,[8–12] to memristive systems,[2,13,14] to hybrid CMOS–memristive designs[15,16] to develop neuro-mimicking platforms for replicating experimental results observed in biology[14,17] or for neuro-inspired platforms used in computing systems.[18–20]

In this article, as shown in **Figure 1**, we provide an overview of neuromorphic computing with CMOS, SiO_x-based memristive, and mixed CMOS–memristive technologies. Our work covers neuro-mimicking designs, which are able to replicate some known aspects of biological neurons and synapses. We also use these neuro-mimicking components to show they can be used in simple cognitive tasks such as spike-based pattern classifications or image sensing. In addition, we use memristive devices to perform more complex classification tasks such as classifying Modified National Institute of Standards and Technology (MNIST) hand-written digits using networks developed mainly from memristive weight elements, where these elements show good performance despite device variations and nonidealities.

Mostafa Rahimi Azghadi completed his Ph.D. in 2014 in neuromorphic VLSI design at Adelaide University, Australia, achieving two doctoral research medals. His main research interests include neuromorphic computing and hardware implementation of learning for spiking and deep neural architectures. Dr. Rahimi is currently a tenured senior lecturer with James Cook University, Australia.

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2. Neuromorphic Components Design

In this section we discuss some previously published as well as some new results on CMOS and memristive neuromorphic neurons and synapses. These designs are toward one of the main goals of neuromorphic engineering, i.e., replicating the underlying principles of neural systems, with the hope to understand them better and discover the use of technology for artificial neural components. Using these components, we will then, in the next section, design systems that perform neuromorphic learning and computation, which are essential purposes of neuromorphic systems.

2.1. CMOS Synapse and Neuron Design

Silicon technology that has reached maturity in the past 40 years has been widely used in neuromorphic computing, from the early works of Mead's team such as the Mahowald and Douglas silicon neuron[21] to cooperation between Mead's students and the wider neuromorphic community in constructing CMOS implementations of various neuron models.[22] In addition, synaptic plasticity, which is believed to play an essential role in learning and memory in the brain, has also been implemented in CMOS in various forms. These range from detailed biophysical models[23,24] to computational rate- and timing-based synapse models.[25–27]

When implementing CMOS-based neuronal and synaptic models, one could design a circuit that utilizes the above-threshold[23]

or subthreshold[28] region of the operation of transistors to implement various mathematical expressions, which are mainly devised by computational neuroscientists.[29] One of the main advantages of analog CMOS designs for neuron and synapse circuits is that the designer can produce almost any behavioral characteristics of the neuron or synapse, which has been approximated and mapped through a mathematical model. In that case, the designer will route together transistors, and in some cases capacitors (which can be realized using transistors), to realize those rules.

In the following sections we discuss the design and implementation of some previous neuron and synapse circuits implemented using CMOS technology and discuss their behaviors, which closely mimic the observations in biological experiments.

2.1.1. CMOS Synapse Design

Here, we describe the design of an analog synaptic circuit that closely mimics some of the known behavioral characteristics of synapses in the visual cortex and hippocampus.[30,31] The circuit that is shown in **Figure 2**a has been designed and fabricated in CMOS to implement the triplet spike timing-dependent plasticity (STDP) rule proposed in a previous study.[32] STDP is a recognized synaptic plasticity rule that alters the synaptic weight based on the timing differences between pre- and postsynaptic spikes. If a presynaptic spike arrives before a postsynaptic one, it can result in potentiation, whereas a reverse spiking order may cause depression. Triplet STDP, on the other hand,
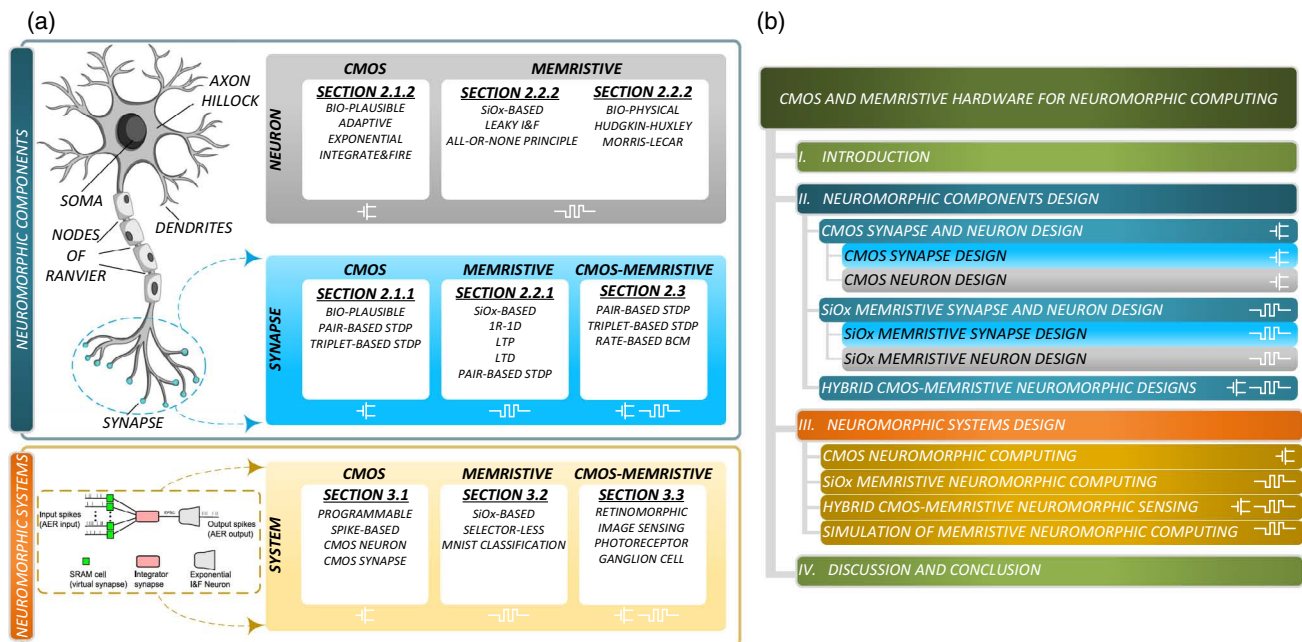
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Figure 1. The structure of the article at a glance. a) The article is composed of discussions on CMOS, memristive, and hybrid CMOS–memristive neuromorphic components and systems. b) The tree structure of the article outline is shown.

considers not only the timing differences between pre- and post-synaptic spikes, but it takes into account the timing difference between a pair of pre- or a pair of postsynaptic spikes in the presence of a post- or presynaptic spike, respectively.[32]

Our newly proposed STDP circuit that resembles, but is simpler than a previous design presented in a previous study,[33] is capable of reproducing the outcome of a wide range of synaptic plasticity biological experiments, including spike pair, triplet, and quadruplet performed in the hippocampus, as shown in a previous study.[30] In addition, it can mimic frequency-dependent pairing experiments performed in the visual cortex, as shown in a previous study.[31] There are three different circuit parts shown in Figure 2a that each correspond to a different feature of a computational model which represents the triplet STDP rule proposed in a study by Pfister et al.[32] Here, the red middle part implements the pair-based dynamics of STDP. With the addition of two side parts, shown in blue, extra pre-pre or post-post interaction dynamics are added up to the base-line pair-based dynamics (shown in red). For more details on the circuit and its functionality, please refer to the study by Azghadi et al.[33]

Figure 2b, c shows measurement results from the circuit in (a), which was fabricated using a 1-poly 6-metal 0.18 μm Austria Micro Systems (AMS) CMOS process. In this circuit, the synaptic weight is represented by the charge stored in the weight capacitor, C_W. Here, the top purple trace in (b) shows the change in the synaptic weight due to a pre-post-pre triplet of spikes, when only the pair-based STDP (red part) of the circuit is active. In contrast, the bottom trace demonstrates the synaptic weight change in the results of the same spike combination and timings but when the complete triplet circuit, i.e., all red and blue parts, is active. Similarly, in the top purple trace in (c), the synaptic weight potentiation as a result of the pair-based pre-post interaction is shown

to be smaller compared with the triplet-based weight change. The higher potentiation of the triplet-based STDP is due to the additional post-pre-post interaction, which is activated through the blue triplet parts of the circuit. This figure shows the first physical implementation of a very large-scale integration (VLSI) synaptic device that accounts for higher-order STDP rules.

2.1.2. CMOS Neuron Design

A CMOS-based circuit design of an adaptive exponential integrate and fire (IF) neuron circuit[22,34] is shown in **Figure 3**a. The circuit is composed of several parts including an input differential pair integrator low-pass filter (ML1-ML3), a second low-pass filter (MG1-MG6) which implements spike frequency adaption, a noninverting amplifier with current-mode positive feedback for address event representation (AER) (MA1-MA6), and a reset block (MR1-MR6) for resetting the neuron and implementing the required refractory period. Figure 3b shows measurement results from the neuron fabricated in a 0.35 um AMS CMOS process.[18] Here, the silicon neuron's membrane voltage stored on C_{men} is shown in response to a constant current injection (I_{in}). This closely resembles the spiking behavior of cortical neurons measured in response to somatically injected currents.[35] As the figure shows, the neuron can be controlled to exhibit behaviors similar to biology.

2.2. SiO$_x$ Memristive Synapse and Neuron Design

Memristive and resistive random access memory (RRAM) devices have been extensively used to implement synapse and neuron circuits for neuromorphic devices, circuits, and systems.[36]
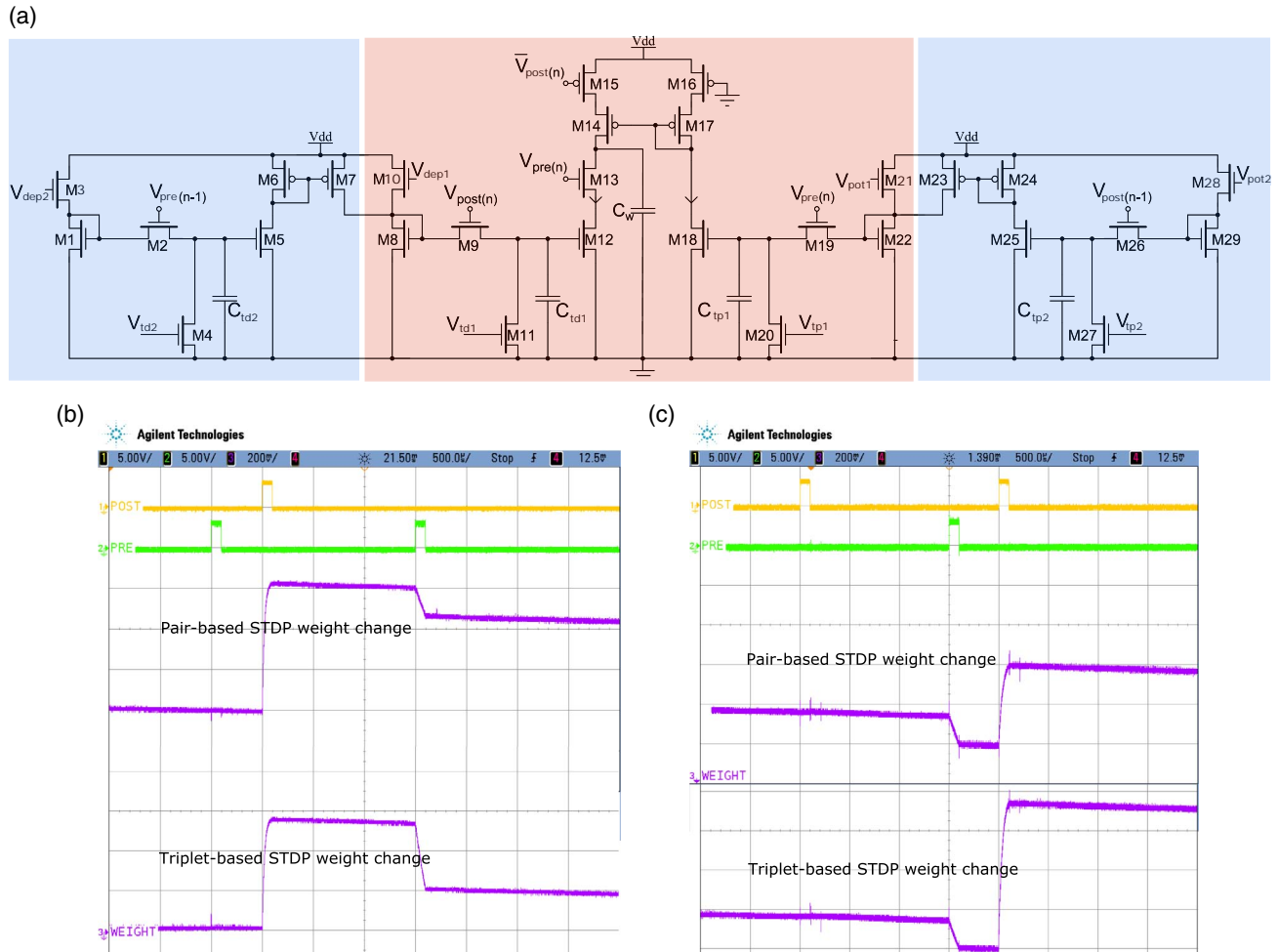
(a)

(b)

(c)

Figure 2. A synapse circuit implemented in CMOS to realize triplet-based STDP a) can modify synaptic weight based on pair-based STDP (top traces in [b,c]) when only its pair-based (red) part is activated, whereas it shows triplet-based weight change dynamics (bottom traces in [b,c]) when all its parts, i.e., the triplet depression (left blue) and triplet potentiation (right blue), work in conjunction with the pair-based (red) part. Note that a pre-post-pre spike triplet b) can result in a higher synaptic depression in triplet STDP interactions (bottom trace), whereas it shows a lower depression (top trace) in the pair-based spike interaction, due to considering only the post-pre pair, and not the pre-post-pre triplet. Similarly, in the case of post-pre-post spiking in (c), higher potentiation is expected when considering the triplet combination (bottom trace), whereas lower potentiation is elicited when only a pre-post pair is considered (top trace).

In this article, we focus mainly on silicon oxide (SiO_x) memristive devices for neuromorphic computing.

SiO_x is commonly used as a gate dielectric for metal-oxide-semiconductor field-effect transistors (MOSFETs) due to its stable physical and chemical characteristics, i.e., relative dielectric constant: 3.9, energy gap: 9 eV, dielectric strength 13.5 MV cm^{-1}, and thermal stability >1050 °C.[37] In addition to its excellent insulating properties, CMOS compatibility, and controllability, SiO_x-based resistive switching phenomena have recently been demonstrated in vacuum[38] and in ambient atmospheric conditions,[39] indicating that this traditionally passive material can be utilized as an active memory element (memristor), controlled by an external electrical field.[40,41]

Furthermore, the microstructure plays a crucial role in air-stable resistance switching in pure silicon oxide. The columnar structure in sputtered silicon oxide films provides preferential parts for filaments formation.[42] The control of the interface

roughness between the bottom electrode and the switching layer affects both the switching voltages and endurance.[43] Apart from the intrinsic CMOS compatibility, switching properties of silicon oxide-based RRAMs compare favorably against other more commonly used RRAM materials. We direct readers to the extensive review.[39] These features make SiO_x an attractive material for neuromorphic computing.

Many different mechanisms could govern the resistance switching in silicon oxide. Generally, the filamentary resistance switching mechanisms are classified into those that are intrinsic to the oxide material—commonly known as valance change or intrinsic switching mechanisms—and those that involve metallic diffusion from electrochemically active electrodes (e.g., silver or copper) or metal doping to form metallic filaments—commonly known as electrochemical metalization, conductive bridge, or extrinsic switching mechanisms.[44]
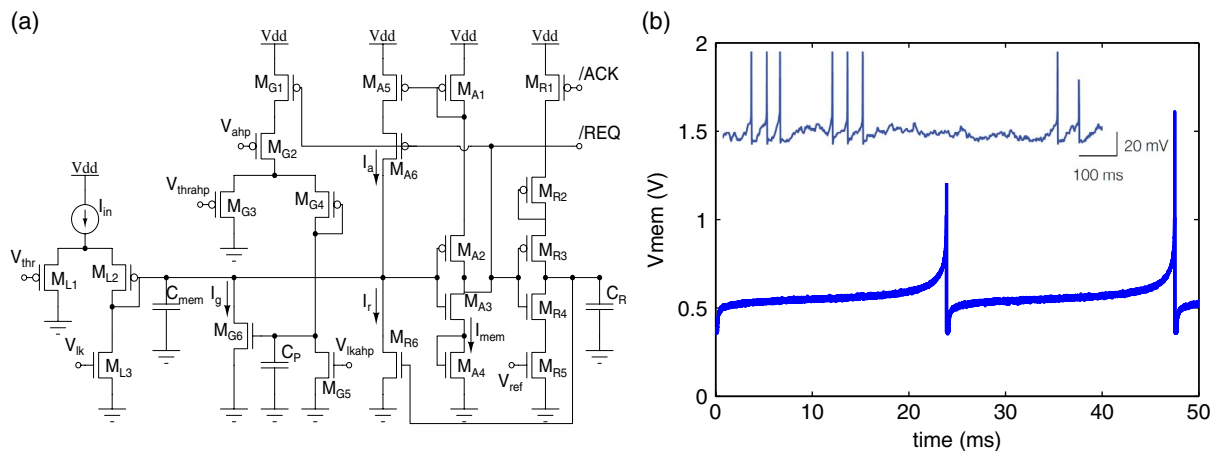
Figure 3. a) A neuron circuit implemented in CMOS (Adapted with permission.[34] Copyright 2014, IEEE.) is capable of reproducing b) the spiking behavior similar to that of biological neurons (Adapted with permission.[18] Copyright 2015, ACM). The inset shows the spiking behavior of neurons measured in response to somatically injected currents, whereas the spiking behavior of the neuron is also in result of increasing I_{in}.

Here, we only focus on intrinsic switching in silicon oxide that can further be subdivided into air-stable switching and air-sensitive switching.[39] The first type has been studied with devices with exposed oxide surfaces and also in bulk and porous oxides.[45–47] Air-sensitive switching occurs only in vacuum as the oxidation of conductive filaments occurs in an oxidizing ambient. The second type, air-stable switching, is possible either in oxygen-rich or nonoxidizing environments, as conductive filaments form far from surfaces and are more critically affected by the oxide microstructure.[42,43,48] The taxonomy of resistance switching in SiO_x-based RRAMs is shown in **Figure 4**.

2.2.1. SiO$_x$ Memristive Synapse Design

SiO_x memristive devices are used to implement both STDP[49,50] and synaptic weights in physical implementations of artificial neural networks.[15,51] STDP is often regarded as a key local learning rule in biological systems, modulating synaptic weights in accordance with the degree of temporal overlap between pre- and postsynaptic action potentials. It has been shown that memristive devices can implement a pulse timing-dependent change of resistance by suitably overlapping voltage pulses.[52] Most realizations use bipolar resistance switching, but unipolar SiO_x-RRAMs can perform STDP plasticity by controlling set and reset processes.

In this case, the STDP response is generated using identical square voltage pulses, where the post-synaptic pulse is modified by a capacitor and converted into a triangular pulse before being applied to an RRAM device. The purpose of pulse modification is to achieve the desired device response to leading and trailing pulse edge slopes. The concept is described in detail in a previous study.[50] **Figure 5** shows the results of the implementation of STDP-like response in unipolar SiO_x-RRAM devices. In this figure, (a) shows a nonidentical STDP-mimicking pulse set up. If a square pulse and a triangular pulse are below threshold there is no change in device resistance if a single pulse is applied. However, if the sum of these two pulses is above the threshold it is possible to adjust device resistance. In these examples the square pulse is a presynaptic spike and the triangle pulse is a

postsynaptic spike. The presynaptic spike arrives earlier than the postsynaptic spike; the resulting sum is a slow leading edge above the threshold. This leads to a decrease in resistance (increase in conductance—set process). The postsynaptic spike arrives earlier than the presynaptic spike; the resulting sum is a slow trailing edge above the threshold. This causes an increase in resistance (decrease in conductance—reset process). Figure 5b shows the percentage of the expected successful operation, i.e., if a conductance decrease or increase is expected for a specific Δt, does that happen or not on the actual device? Figure 5c,d shows the resulting STDP synaptic weight (conductance) changes in response to Δt values in the range from -600 to $+800\,\mu s$.

All the above memristive synapse results are for air-stable devices. However, one-diode-one-resistor (1D–1R) air-sensitive test structures can also be used for vacuum-type SiO_x-based synapse device demonstration, as shown in **Figure 6**. In this figure, (a) demonstrates a secondary electron microscopy (SEM) image of the top-down view of the fabricated device, whereas (b) shows a cross-section image of the 1R device, including its layer information. The synapse device structure and characteristics of this 1D–1R design have been described in detail in a previous study.[53]

To fabricate this device, the active SiO_x memory layer is deposited to a thickness of 40 nm using plasma-enhanced chemical vapor deposition (PECVD). The reactive ion etch (RIE) step then clears out the SiO_x layer inside the hole and creates a SiO_x sidewall where the memory device is formed (Figure 6b). The active memory area of the 1 R device is $2 \times 2\,\mu m^2$ and the overall size including metal interconnects is $21.9 \times 21.9\,\mu m^2$. The overall size of the 1D device is $41 \times 19\,\mu m^2$.

Figure 6c shows an endurance of sequential long-term potentiation (LTP) and long-term depression (LTD) behaviors using nonidentical pulses in 1D–1R architecture with different voltage increment steps for potentiation and depression: 0.1 V (top), 0.2 V (middle), and 0.3 V (bottom). For depression, the pulse height modulates from 11 to 17 V with 10 μs pulse width; for potentiation, the pulse height changes from 4.0 to 10 V with 10 μs pulse width. Such flexible artificial control built with synaptic devices could provide a suitable platform for a broad weight
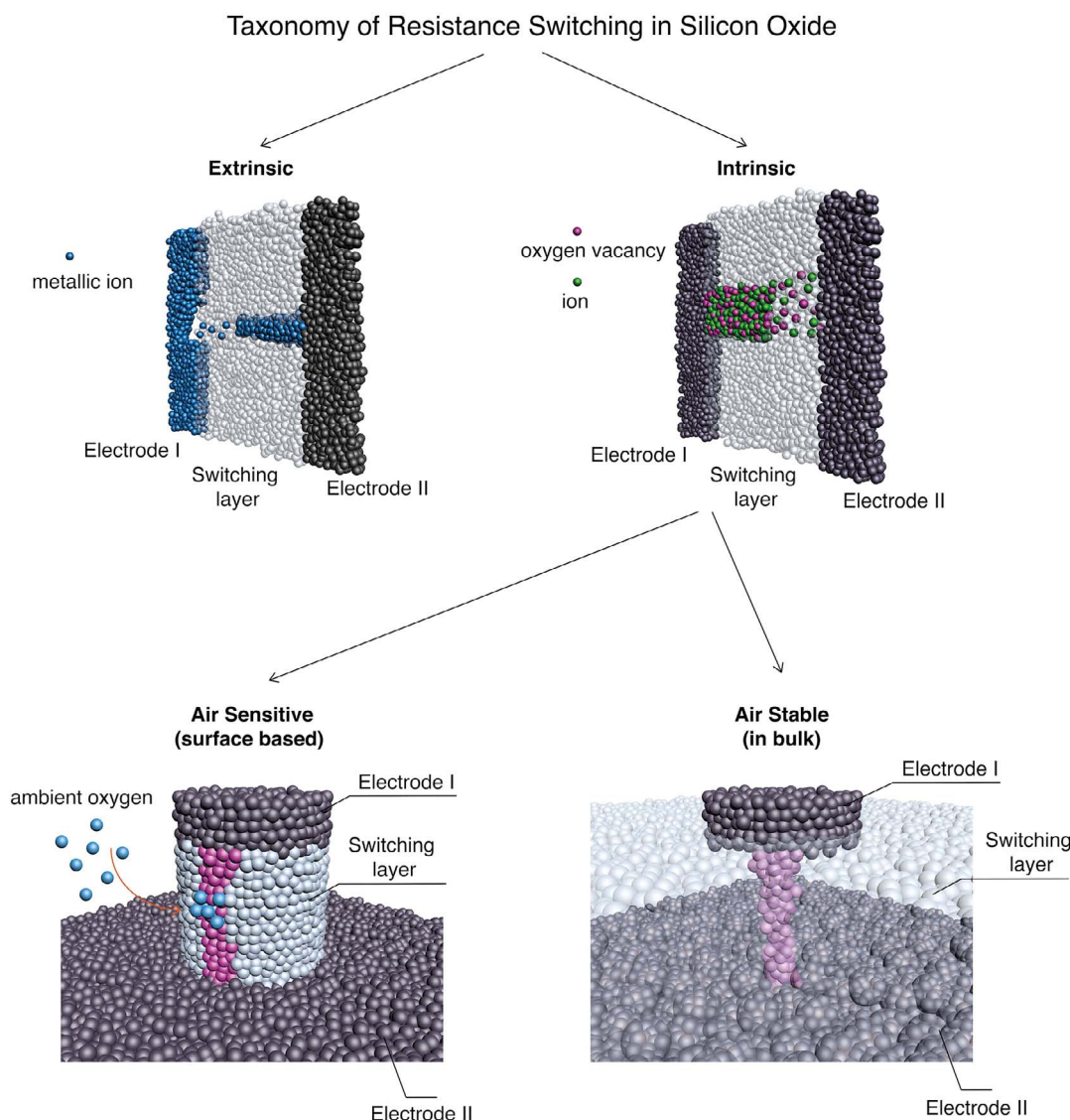
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Figure 4. Taxonomy of resistance switching in silicon oxide. Upper LHS: Schematic of extrinsic resistance switching. Upper RHS: Schematic of intrinsic resistance switching. Lower LHS: Air-sensitive resistance switching: typically, electroforming and resistance switching occur only in devices with an exposed oxide surface and not in bulk devices. This is attributed to re-oxidation of surface-based silicon filaments by an oxidizing ambient. Lower RHS: Air-stable resistance switching. This type of switching occurs in ambient (oxidizing) conditions and is defined by the microstructure of the oxide material. Switching voltages are typically lower for air-sensitive switching. Reproduced with permission.[39] Copyright 2018, John Wiley and Sons.

range of computing applications. Some of the advantages that SiO_x-based synaptic devices provide over other resistive switching materials include a higher dynamic range (10^4) and the potential to achieve as many as 10–60 multilevel states (dependant on the stability, e.g., retention and endurance) in both LTP and LTD by changing the increment/decrement of the voltage step, as shown here.

Figure 6d,e shows that the SiO_x-based 1D–1R synaptic device can mimic STDP. These figures show a total of ten different conductance levels of the device, when positive and negative spike timing differences, as well as spike widths, are used, to emulate the potentiation and depression window behavior of STDP, observed in experimental[30,49] and computational experiments.[32]

2.2.2. SiO_x Memristive Neuron Design

Memristive and RRAM devices are more commonly used to implement synaptic weight plasticity in spiking neural networks (SNNs) or represent weights in artificial neural networks. However, unipolar SiO_x-RRAMs have also been considered for modeling aspects of the electrical activity of the neuron. It has been demonstrated that specific operational procedures could lead to the generation of controlled voltage transients that resemble spike-like responses seen in biological neurons. Additionally, the integration and thresholding capabilities that are crucial for neuronal functionality have also been demonstrated. Further, redox-based resistance switching models can
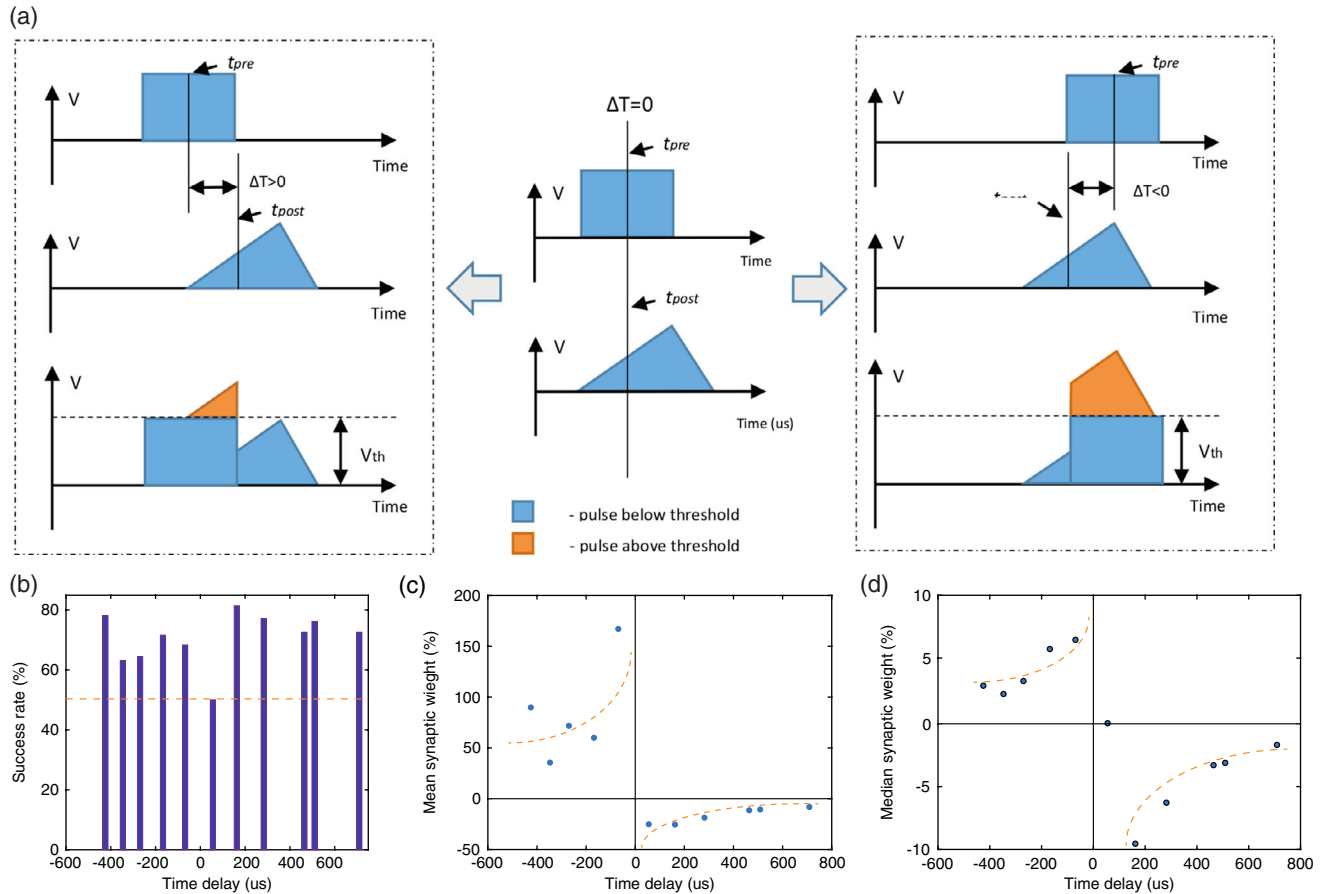
Figure 5. a) Illustration of the experimental setup to test STDP-like behavior: Non-identical pre- and postvoltage pulses and the resulting overlapping voltage across the device. b) The plot demonstrates successful device operations (conductance increase or decrease depending on time delays). Plots demonstrate STDP-like behavior for c) mean and d) median change in device conductance. Dotted lines serve as a visual guide. Adapted under the terms of the CC BY license.[50] Copyright 2018, The Authors, published by Frontiers Media.

be related to the Hodgkin–Huxley (HH)[54] conductance model by analyzing the equivalent electrical circuits[55] and are found to be very similar.

Figure 7 shows the thresholding, spiking, and integration capabilities of SiO_x RRAM-based neurons. The main idea is to control the competing set and reset processes (the former being field driven, the latter current driven) by stressing devices with appropriate current inputs. A constant current bias is used to test thresholding and spiking functionality, whereas current pulses are used to implement integration.

The unipolar switching in SiO_x-RRAM devices is utilized to generate voltage transients (resembling voltage spikes) by applying a constant current bias. By applying currents larger than the reset current, the device is put in the metastable state, fluctuating between the low resistance state (LRS) and the high resistance state (HRS). As a result, the voltage spiking is measured at the output of the device. If the input current is lower than a threshold (reset) current, the resistance states are stable; therefore, no voltage spiking is observed. Figure 7a shows threshold spiking behaviour. Furthermore, the integration functionality is demonstrated by applying a train of excitatory current pulses while changing the timing between the pulses. A much smaller

current pulse senses the voltage across the device. Figure 7b–f shows the obtained results. The frequency of input current pulses controls the rate of voltage spiking. The results resemble the leaky IF (LIF) model. A more in-depth analysis of the results and the experimental setup can be found in a previous study.[55]

In addition to the neuron spiking behavior shown in Figure 7, a simple one-resistor-one-resistor (1R–1R) test structure can be used for air-stable type SiO_x-based neuron device demonstration, as shown in **Figure 8**. The detailed neuron device structure and characteristics have been described in previous studies.[38,56] For this neuron design, two device structures have been fabricated: a) SiO_x/HfO_x stacking bilayer as shown in Figure 8a,b and b) vanadium electrode (V)/SiO_x single layer shown in Figure 8d. For the SiO_x/HfO_x stacking bilayer structure, the SiO_2 layer of 30 nm thickness was sputtered and HfO_2 of 1 nm thickness (confirmed by the transmission electron microscopy (TEM) image, as shown in Figure 8a) was deposited using atomic layer dDeposition (ALD) at 250 °C. The TaN layer of 170 nm that serves as a top electrode WAS deposited also through sputtering. For the V/SiO_x single-layer structure, vanadium electrode of 200 nm and SiO_2 layer of 6 nm was deposited by sequentially sputtering without a vacuum break.
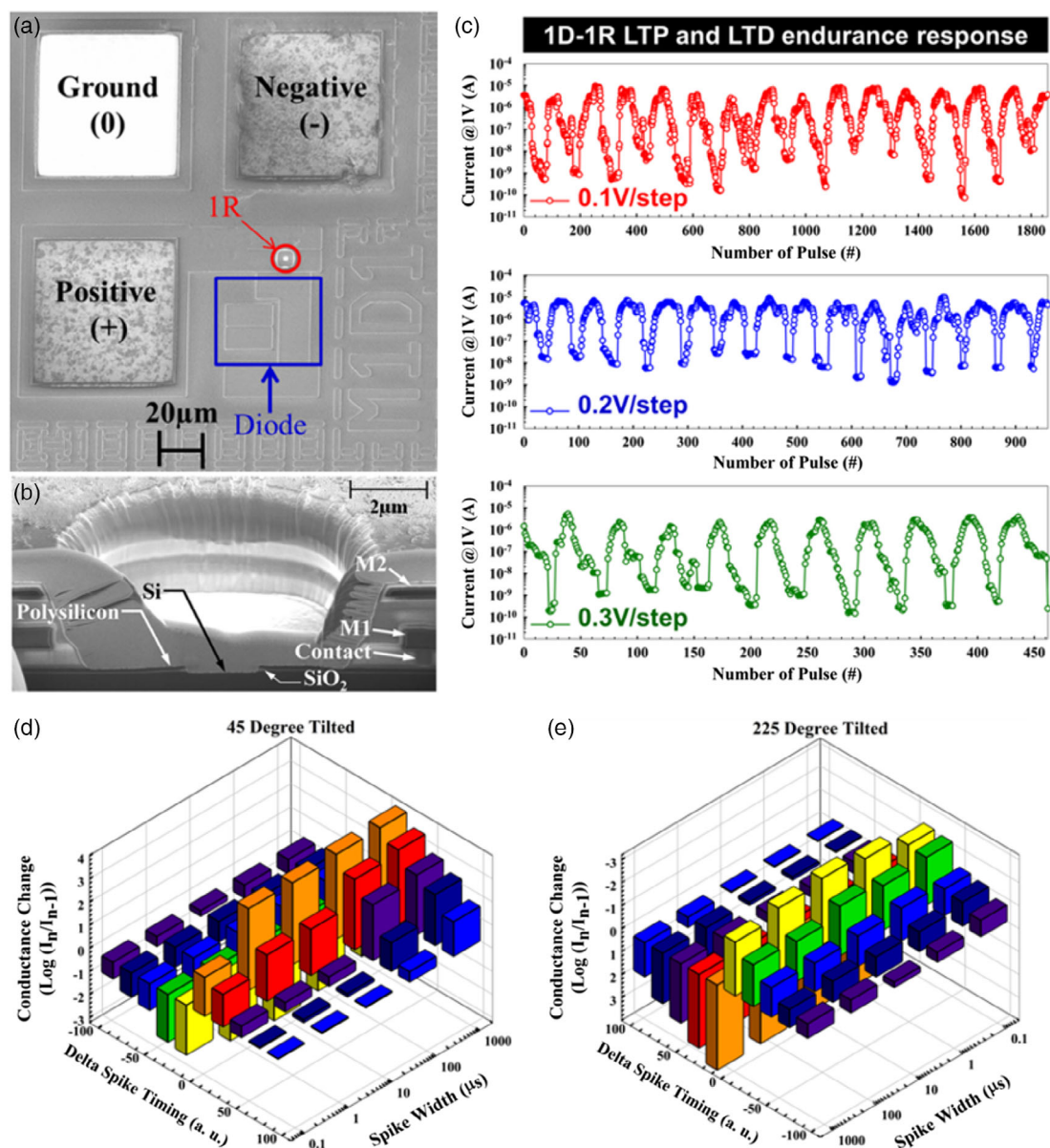
Figure 6. SiO$_x$-based 1 R–1 D synaptic device. The device structure is shown in SEM images shown in a) for top view and b) cross-sectional view. c) The device shows great controllability to increase and decrease its conductance in response to pulse amplitude modulation. d) The device is used to demonstrate ten different conductance change behaviors as a result of an STDP experiment, where positive and negative spike timing difference as well as spike widths are used. Here, (e) shows the same data as (d) but in the reversed order. a,b,d,e) Reproduced under the terms of the CC BY license.[53] Copyright 2016, The Authors, published by Springer Nature.

The SiO$_x$/HfO$_x$ stacked structure exhibits excellent reliable threshold switching in air with an ultralow operation voltage (<0.5 V) (Figure 8b). The nonlinearity/selectivity of this device is about 180, which can stably operate at 0.3 V threshold voltage, whereas the holding voltage is 0.1 V, as shown in Figure 8c. The self-compliance current is also observed here, which is due to the internal filament limitation.[57] Figure 8d shows the other SiO$_x$-based threshold switching structure formed by V/SiO$_x$ single-layer stacking. The nonlinearity and selectivity of this device is about 102, which can stably operate at 1.2 V, where

the device threshold voltage is 1.1 V. Note that an electroforming process is necessary before any operation.[38,56]

One of the promising features of these two threshold switching devices is that they are able to demonstrate the all-or-none principle in neuronal behavior. It means that, if a neuron responds at all, then it must respond completely. Also, it means that a greater intensity of stimulation does not produce stronger spiking but can increase firing frequency.[58,59] Figure 8e shows the schematic of the simple 1R–1R test circuit and its actual experimental setup to realize the all-or-none principle
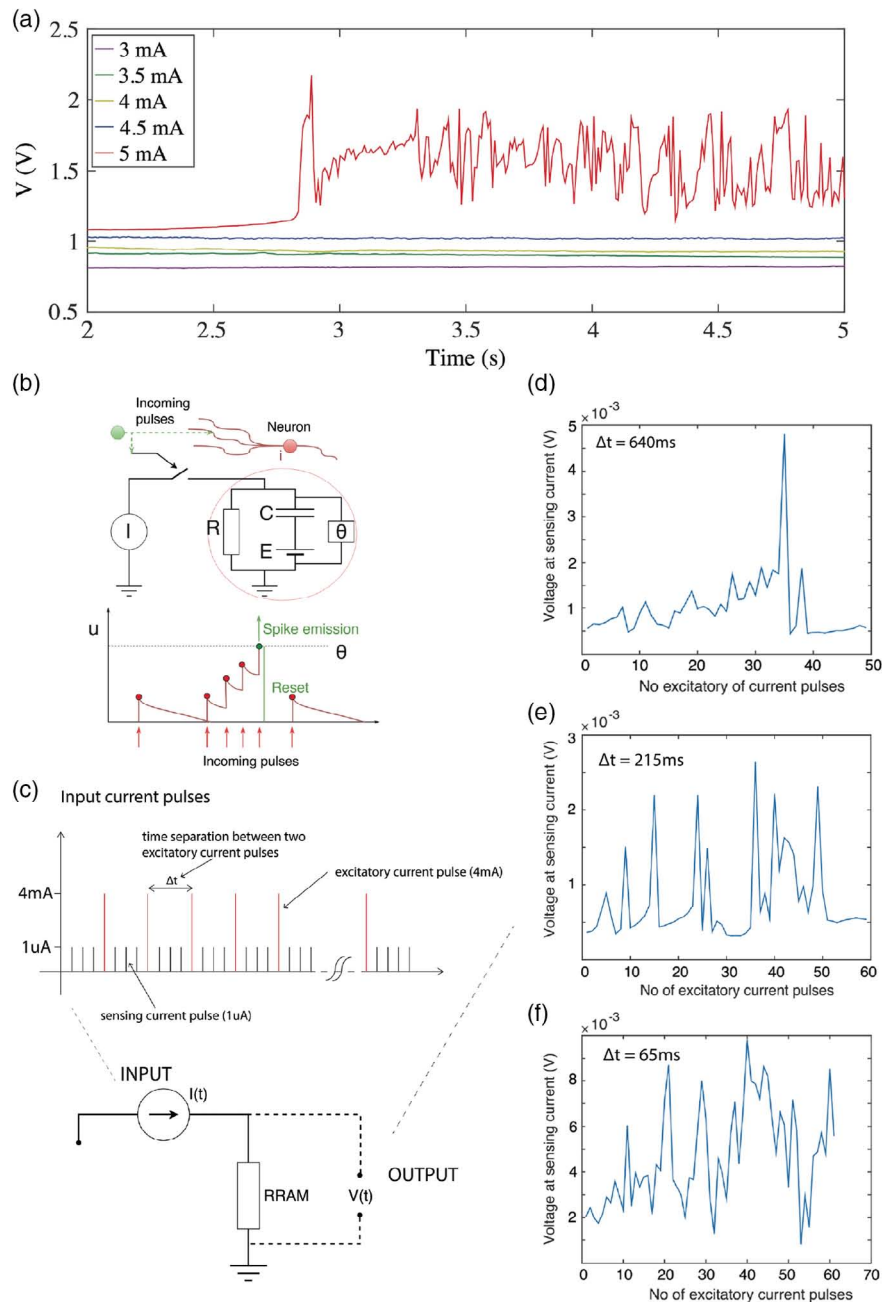
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Figure 7. a) Voltage transients (spikes) do not occur until the constant current of 5 mA is applied (current threshold). b) Schematic of the LIF neuronal model. The lower figure shows the integration of input current pulses over time. Theta is the voltage threshold for spiking. c) Excitatory current pulses (4 mA) are applied to the device, and small current pulses (1 μA) are used for sensing the voltage across the device. Device voltage response is shown for pulse time separations of d) 640 ms, e) 215 ms, and f) 65 ms. These demonstrate that spiking occurs for the smaller number of pulses if the separation between input current pulses is shorter. Adapted under the terms of the CC BY license.[55] Copyright 2016. The Authors, Published by Frontiers Media.

biomimetically. By applying the green input pulse shape as shown in Figure 8e and measuring the voltage between the resistance and the measurement instrument (Agilent DSO9254A), we can distinguish the all-or-none principle, as shown in Figure 8f in blue color. When the applied voltage (CH2, 2 V) is below the threshold voltage (note to the voltage divider setting, which is 0.4 V for the SiO_x/HfO_x stacked structure and 1.1 V for V/SiO_x structure), there are no spikes firing. However, when the

applied voltage is at or above the threshold voltage (3.7 V), a sequential and repeatable 1.2 V output spike (peak-to-peak voltage) with 25 μs period is generated.

The above memristive neurons only replicate the threshold-based spiking IF behavior of neurons. However, biophysical neurons are considered to provide richer dynamical behavior and more computational complexity in comparison with their bioplausible counterparts such as IF and LIF neurons.
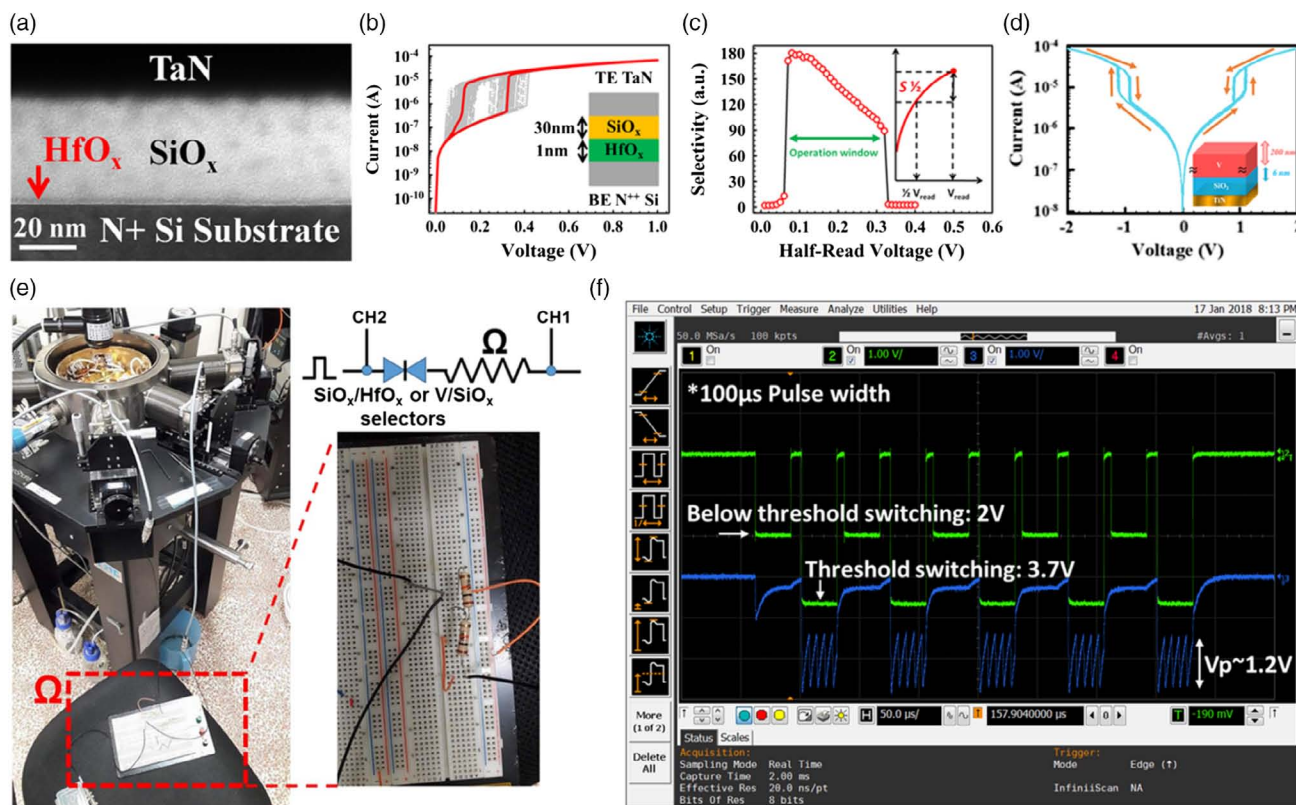
Figure 8. SiOₓ-based 1R–1R neuron device. a) TEM cross-section image of metal–insulator–semiconductor (MIS) structure: TaN/30 nm-SiOₓ/1 nm-HfOₓ/N + Si substrate. b) 100 times *I–V* threshold switching of MIS device in air. c) Threshold switching in the air for selectivity and nonlinearity of the stacking bilayer structure shown in (a). d) Typical *I–V* threshold switching of vanadium electrode/6 nm-SiOₓ/TiN structure. e) Experimental setup for a simple neuron circuit by the SiOₓ-based threshold switching selector. f) The screenshot of measurement instrument (Agilent DSO9254A) and measured voltage results in CH1 (green line) and CH2 (blue line). Pulses with 100 µs width are used here. When CH1 is below the firing threshold (e.g., at 2 V), there is no firing observed, whereas if threshold switching occurs (e.g., input pulse amplitude > 3.7 V), the neuron firing begins on CH2 (damping Vp 1.2 V). a,b) Adapted with permission.[38] Copyright 2018, The Royal Society of Chemistry.

HH neuron[54] and its simplified version such as Morris–Lecar (ML)[60] are members of the biophysical neuron family and due to their neurocomputational properties, nonbiomimetic CMOS circuits are not capable of reproducing their dynamics efficiently in terms of energy and area. The introduction of memristor devices has transformed the design of HH neuron circuits,[61,62] whose design progress slowed due to the lack of built-in stochasticity in CMOS circuits for building more realistic brain-plausible neuromorphic platforms.[63,64]

We have previously shown that the known functionalities of HH[65] and ML[66] neuron models can be simulated using behavioral memristive models. **Figure 9** shows two different panels, each describing one bioinspired memristive neuron circuit diagram, memristive channel characteristics, and bifurcation behaviors at different frequencies, for a different neuron model. In the top panel of Figure 9, (a) shows the basic circuit schematic for the HH neuron memristor-based circuit model with memristive behavior of sodium and potassium channels. A voltage-gated potassium (sodium) channel is emulated by positively (negatively) biased memristor devices coupled with a membrane capacitor. In this panel, (b) shows the tonic spiking behavior of memristive HH neuron and potassium (K⁺) and sodium (Na⁺) channels for HH model. In the bottom panel,

(c) shows the ML neuron model circuit diagram and the behavior of potassium and calcium channels for the ML memristive circuit model in response to a 2.5 V sinusoidal input voltage at different frequencies. The otassium channel memristor *I–V* curve is shown at 5 Hz, 50 Hz, and 5 kHz (from left to right). The calcium channel memristor *I–V* is displayed at 100 Hz, 500 Hz, and 50 kHz (from left to right). The scaled ML neuron bifurcation behavior for different current stimulus is shown in Figure 9d. The membrane voltage, calcium channel's current, potassium channel's current, and state variables (M, N) have been also displayed for the stimulus currents of 60 and 100 µA.

In the last two sections, we presented a number of designs implementing synaptic and neuronal functionalities such as LTP, LTD, and STDP for memristive synapses and all-or-none and threshold spiking behavior for memristive neurons. Except for the simulation-based HH and ML memristive neuron models discussed, all other designs explained using SiOₓ structures. In addition to the design presented earlier, SiOₓ-based devices have been extensively used in other neuromorphic systems, specifically for synaptic behavior demonstration. Here, we provide a comparison of various SiOₓ-based memristive synaptic devices discussing their functionalities and physical/switching structures, as shown in **Table 1**.
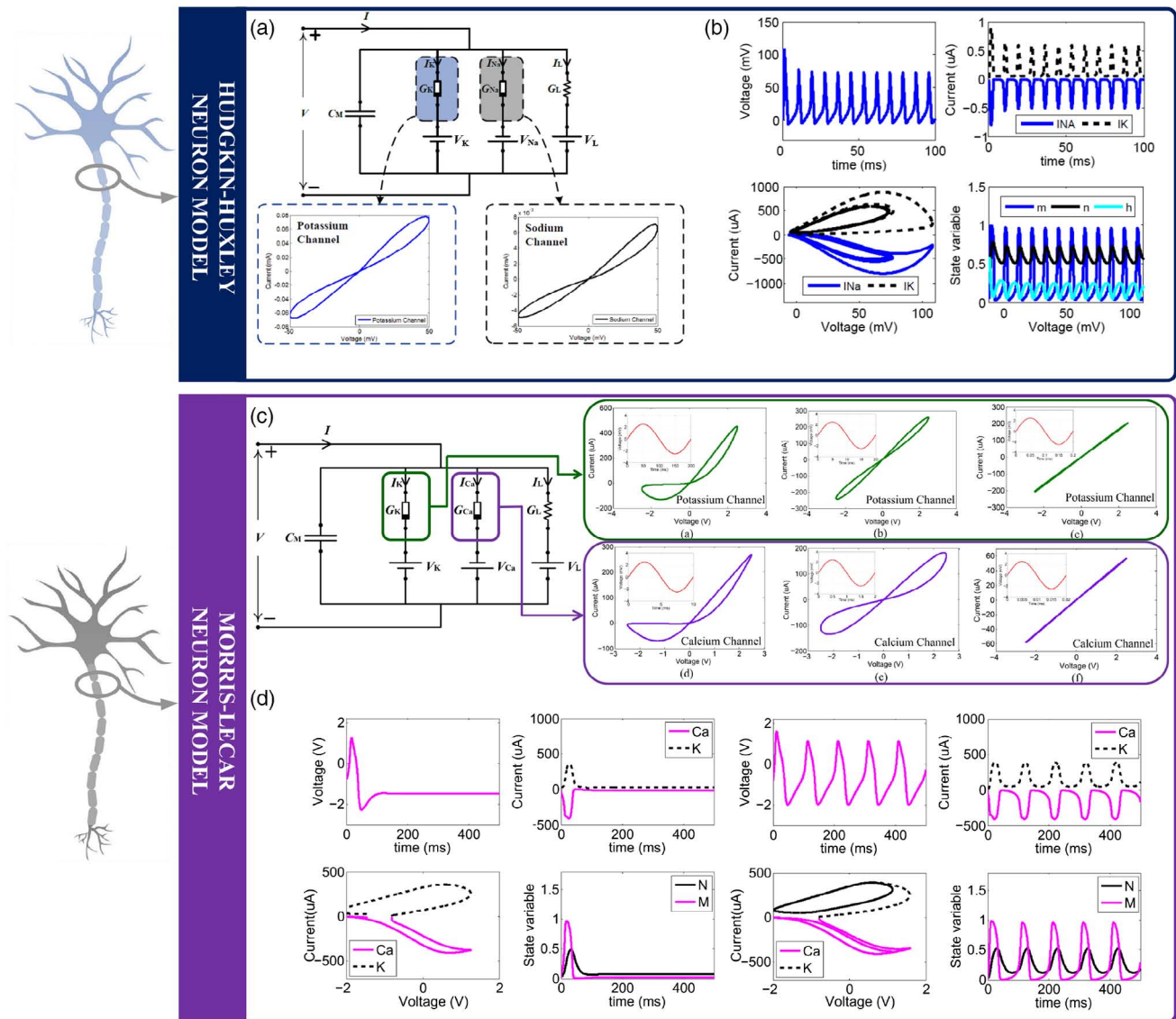
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Figure 9. Bioinspired memristive neuron circuit diagrams, memristive channel characteristics, and bifurcation behaviors at different frequencies, for HH (top panel) and ML (bottom panel) neuron models. Adapted with permission.[65,66] Copyright 2016 and 2017, IEEE.

As Table 1 shows, various techniques have been used to implement different devices with diverse layer stacks, deposition methods, switching polarity, switching type, and SiO_x thicknesses.

These designs that operate at different set/reset voltages, as low as 0.5 V and as high as 10–15 V, offer various degrees of functionality and on/off ratios. Some of these devices also present a

Table 1. Comparison of switching characteristics and parameters of SiO_x-based resistive switching devices.

	Device stacks	Deposition method	Switching polarity	SiO_x thickness	Set [V]	Reset [V]	On/Off ratio	Multi level	LTP /LTD	STDP
Gao et al.[67]	$LiCoO_2$/porous SiO_x	Thermal	Bipolar	150 nm	4	−4	$<10^6$	Yes	Yes	–
Zarudnyi et al.[50]	SiO_x	Sputtering	Unipolar	37 nm	3.7	2.5	$<10^2$	–	–	Yes
Wang et al.[69]	SiO_x/TaO_x	Ion beam	Bipolar	1, 2, 4 nm	0.5	−0.5	$<10^3$	–	Yes	Yes
Acevedo et al.[70]	$LCMO/SiO_2$	Native	Bipolar	2 nm	5	−5	$<10^2$	Yes	–	–
Chen et al.[68]	SiO_x	PVD	Bipolar	100 nm	1	−1	<10	Yes	Yes	–
Chang et al.[53]	SiO_x	PECVD	PECVD unipolar	40 nm	4–10	−15	$<10^2$	Yes	Yes	Yes
Mehonic et al.[42,51]	$Mo/SiO_x/Ti/Au$	Reactive sputtering	Bipolar	35 nm	−1	1	$<10^4$	Yes	Yes	Yes

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multilevel structure, which is useful in implementing neuromorphic computing systems. It is worth noting that, not all designs, except for two of our previous works[51,53] are able to implement the three investigated synaptic plasticity functionalities, i.e., LTP and LTD, and STDP.

Note that in Gao's study,[67] a porous silicon oxide structure has been used. The main function of SiO_x here is to facilitate lithium-ion migration in forming a conductive path, with well-controlled lithium ions in the SiO_x layer. These features enhance neuromorphic computing performance, i.e., LTP and LTD, similar to those observed in the SiO_x device developed in a previous study.[68] In the work by Wang et al.,[69] an opposite SiO_x functionality is used to enhance the resistive switching characteristics for analog resistance modulation. The SiO_x here was found to have a denser microstructure compared with the TaO_x layer. This microstructural attribute could lead to the retardation of oxygen diffusion in the SiO_x layer. Also, the diffusion constant is 1–6 orders of magnitude lower than that in the substoichiometric TaO_x. Therefore, in their proposed device, the diffusion rate of oxygen ions is expected to decrease in SiO_x. As a result, the resistive switching in the cell is likely to take place in the more stoichiometric and insulating SiO_x layer that is in series with the substoichiometric and more conductive TaO_x layer (valence change-type memristor). Similarly, in Acevedo's study,[70] it is reported that SiO_x drives the observed resistive switching behaviors by taking and releasing oxygen ions to and from the nearby manganite layer. These results confirm that the combination of two active oxides (stacked structure) improves the neuromorphic functionalities compared with the single-oxide structures, as shown in Table 1. However, some materials (such as $LiCoO_2$ or LCMO) may not be fully CMOS compatible.

2.3. Hybrid CMOS–Memristive Neuromorphic Designs

Although neuronal and synaptic behaviors have been replicated using memristors, as discussed in the previous sections, silicon and CMOS-based neuron designs have shown more convenient implementation processes and better functionalities.[22] Unlike neurons, synaptic behaviors and functionalities are more conveniently implemented using memristive devices. Therefore, one may choose to use memristive devices to implement synaptic learning in a neuromorphic system, whereas all other components of the system are implemented using analog and digital CMOS.[15] This requires seamless integration of CMOS and memristive technologies in a hybrid design, so the benefits of both domains are achieved in the final system.

There have been many previous hybrid CMOS–memristor neuromorphic designs in the literature.[15,71–73] In most of these systems, the neuron and interfacing circuitry are designed in CMOS, whereas synapses implementing targeted synaptic plasticity rules, such as STDP, are realized using one or a few memristors, which are programmed through shared or individual CMOS circuits. Here, we show a hybrid CMOS–memristor neuromorphic synapse that implements rate-based synaptic plasticity in the form of the Bienenstock Cooper Munro (BCM)[74] rule, as a neuromorphic component. In addition, in Section 3.3, we show a hybrid system implementing spike-based image sensing.[16]

In a previous work,[15] we proposed a hybrid CMOS–memristor neuromorphic synapse that was shown to be capable of reproducing a number of biological experiments including pair-based, triplet, and quadruplet, similar to the CMOS circuit shown in Figure 2a. The hybrid synapse circuit that is connected to a presynaptic and a postsynaptic neuron is shown in **Figure 10**a. Here, we show for the first time that this circuit can generate BCM-like behavior, which is observed in biological experiments.[75] Figure 10b shows the weight modifications achieved using the circuit in (a), driven by random pre- and post-synaptic Poissonian spike trains. This experiment is composed of ten trials. In each trial, a random presynaptic spike train with the rate ρ_{pre} along with a random postsynaptic spike train with the rate ρ_{post}, both of a 10 s duration, are applied to the bimemristive hybrid synapse. The rates of pre- and postsynaptic spike trains are considered equal and are swept over the range
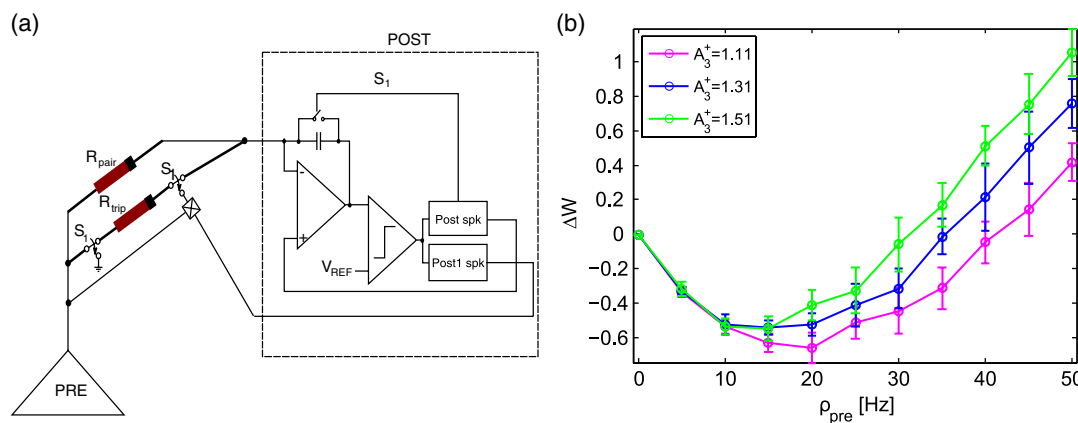

Figure 10. a) A hybrid CMOS–memristor neuromorphic synapse connected to CMOS pre- and postsynaptic devices (Adapted with permission.[15] Copyright 2017, IEEE). The crossed square in the synapse circuit is representative of a multiplication/rectification circuit. In addition, S_1 is a digital signal that activates two switches in the synapse and one in the neuron, to implement the correct timings required for the STDP rule.[15] b) The hybrid synapse is able to reproduce a BCM-like weight modification behavior,[74,75] by modifying A_3^+, a triplet STDP potentiation parameter, which dictates the amplitude of potentiation due to the interaction between a postsynaptic spike, with its two immediate previous postsynaptic and presynaptic spikes.[32]

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of 0–50 Hz. Figure 10b shows the average weight change and their standard deviations over the ten trials. This figure shows the main characteristic of the BCM rule, which is turning LTD to LTP at a specific spike rate, i.e., the BCM threshold. Additionally, this figure shows the sliding threshold feature of the BCM rule, which can alter the frequency at which LTD turns to LTP. This turning threshold as shown in a previous study[32] can be controlled using the STDP parameters. Here we have utilized the triplet potentiation amplitude, A_3^+, to slide the threshold toward lower or higher depression.[15]

Although previous CMOS circuits implementing triplet STDP have also shown the ability to realize BCM behavior, they occupy a large silicon real estate, mainly due to the large capacitances required to store the synaptic weight and provide time constants required for triplet STDP dynamics. However, the proposed memristor-based hybrid circuit, compared with its CMOS counterparts, occupies up to a ten times smaller chip area.[15] This feature makes it a promising component for large-scale neuromorphic systems with spike-based learning capabilities and encourages designers to benefit from hybrid designs in more applications, such as neuromorphic image sensing.

3. Neuromorphic Systems Design

In Section 2, we discussed the design and implementation of various CMOS, memristive, and hybrid CMOS–memristive neuromorphic circuits that were designed and implemented to realize neuronal or synaptic behaviors. We showed that the devices and circuits designed are able to replicate some known functionalities and behaviors of biological systems, such as LTP, LTD, STDP, triplet STDP, all-or-none spiking, threshold spiking, HH and ML neuron channel characteristics, and bifurcation behaviors. In this section, we utilize several of the designed circuits developed and explained earlier to implement neuromorphic computing systems applied to spike-based as well as artificial neural network learning. We also discuss the design and implementation of a hybrid CMOS–memristor neuromorphic sensing system.

3.1. CMOS Neuromorphic Computing

A neuromorphic system can be implemented completely using digital[76,77] or using a mix of analog and digital CMOS technology.[18,27] If the system is implemented in digital, the behaviors of neurons and synapses are approximated and the spiking and AER structure of the system is realized in digital architectures.[8,76,78] However, if the system is designed in mixed analog–digital domain, the synaptic and neuronal behaviors are replicated closely in analog, whereas AER and interfacing are realized using digital technology.[9]

Most of the previous CMOS-based neuromorphic systems include fixed learning and neuron circuits, where an array of analog synaptic cells implementing a fixed learning rule, such as STDP[28] or SDSP,[25] is connected to an array of IF neurons. These implementations offer great biomimicing properties because their components closely mimic biological experiments; however, they can only be used with the learning rules implemented in their hardware. Some neuromorphic systems, such

as those described in a previous study,[18] provide more flexibility by giving the user the ability to describe the network structure as well as the required learning rule in software, whereas the neuron and synapse components are implemented in analog hardware. The AER and spike transmission in these systems use digital technology and are usually implemented on field programmable gate arrays (FPGAs)[79] that facilitate programmability and reproduction.[76]

Here, we describe the operation and use of such a hardware–software system[18] that uses CMOS circuits providing programmable synaptic learning. This programmability gives the user the freedom to explore any arbitrary spike-based learning rule. The design that is shown in **Figure 11**a is composed of a) an asynchronous static random access memory (SRAM) array that can be programmed as virtual synapses, connected to b) an array of CMOS synapses, which integrate a current proportional to the weight stored in their corresponding SRAM cells, to feed into c) IF neurons similar to the neurons explained in Figure 3, which receive/transmit spikes from/to other neurons/synapses in a set network, through d) asynchronous control and interfacing circuits that manage the AER communication. All analog components on the chip are tuned by biases received from e) a bias generator circuit.

Figure 11b shows an example SNN that has been implemented on the chip shown in (a). The chip receives AER input spikes, which contain information on a) the address of the postsynaptic neuron, b) the address of the programmable SRAM-based virtual synapse connected to this neuron, c) the type and address of the physical integrator synapse, and d) the new five-bit weight value that will be written to the addressed virtual synapse (SRAM cell). The AER output spikes, in contrast, only show the address of the postsynaptic neuron that generated them.

Using the network shown in Figure 11b, two UP and DOWN rate-based spike patterns (shown at the top of Figure 11c), with 20% correlation (6 fixed common input spike trains shown with red circles, from the total 30), are learned through triplet STDP,[32] to be classified unsupervised. The four panels in the figure show the output neuron firing rate during learning. In the first trial, learning has not happened yet; hence, the output neuron fires with a similar rate for both UP and DOWN patterns. As the learning progresses, at each trial either the UP or DOWN spike-based pattern is randomly selected to be applied to the network. Also, a new Poissonian spike train is generated for each of the 18 active synaptic inputs for either UP or DOWN. It is seen that after 20 trials, the output neuron successfully distinguishes between the two patterns, showing a higher firing rate for UP patterns. The figure shows the results for 20 runs, each including 20 trials. For each run, the initial synaptic weights, the order in which UP and DOWN patterns are applied to the network over 20 trials, as well as the definition (spike timing intervals and distribution) of UP and DOWN patterns are randomized. Note that the learning rule used for this classification, implemented in software to program the SRAM virtual synapses on the chip, provides the same functionality as the circuit shown in Figure 2a. We have shown that this classification task can achieve 100% accuracy, even in the presence of 87% (i.e., 26 common input spike trains) correlation between the two patterns.
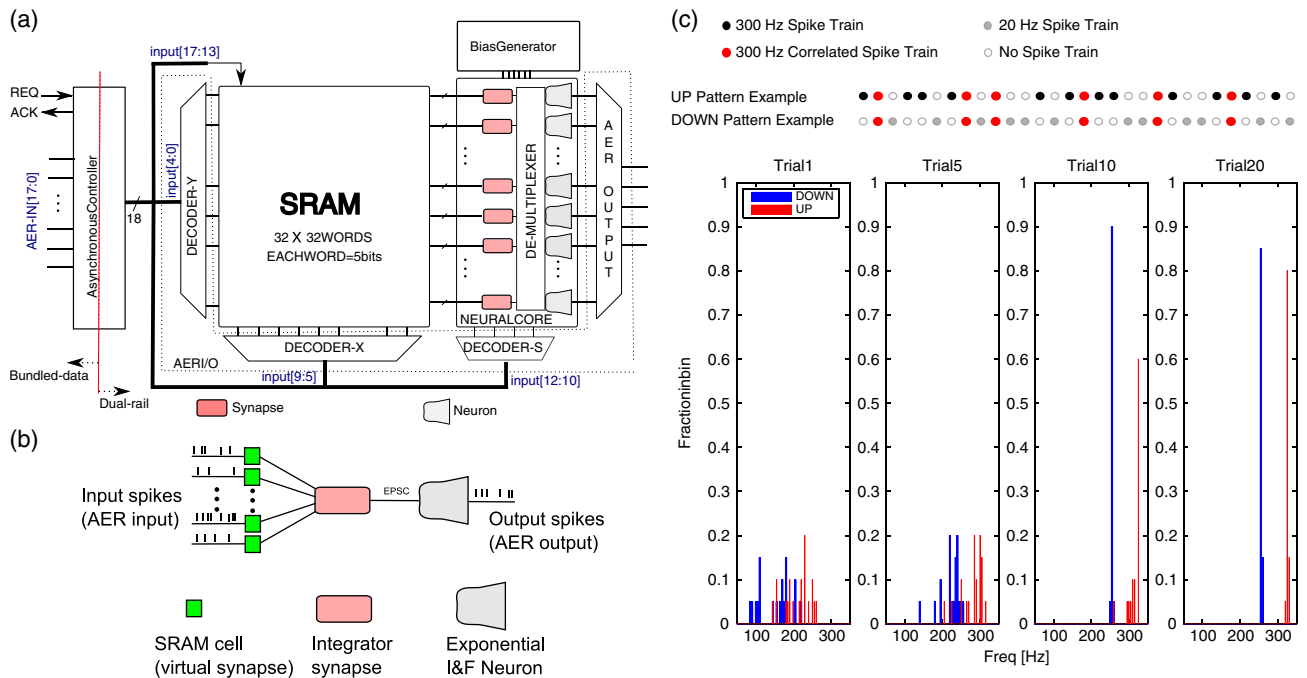
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Figure 11. a) A programmable neuromorphic chip implements a b) simple perceptron network to learn unsupervised to detect c) 20% correlated rate-based patterns. a) Adapted with permission.[34] Copyright 2014, IEEE. b,c) Adapted with permission.[18] Copyright 2015, ACM.

3.2. SiO$_x$ Memristive Neuromorphic Computing

SNN and artificial neural network systems that utilize memristors as their learning components or simply as a programmable element have been researched extensively.[15,19,80–83] Here, we mainly focus on neuromorphic systems that utilize SiO$_x$ memristive devices for learning, where memristors are used as weight elements. We also show simulation results of neuromorphic learning using spike-based learning and STDP, realized using ideal memristor models. However, there exist challenges in the use of memristive devices as learning components, which should be considered in neuromorphic learning systems design. Here, we show and discuss some of these challenges that mainly arise from the unavoidable device nonidealities.

In addition to the ability to replicate STDP-like behavior for spike-based learning (shown in Figure 5), memristive and RRAM crossbars offer the execution of vector-matrix multiplication in the analog domain.[19] When voltage pulses are applied on one side of the programmed RRAM crossbar, and current is sensed on the orthogonal terminals, this system provides approximate vector matrix multiplications (multiply and accumulate [MAC]) operations in constant time steps using Kirchhoff's and Ohm's laws.[84] This approach promises speed and power efficiency improvements of many orders of magnitude compared with conventional CMOS systems.[19] However, there exist obstacles on the way of utilizing memristive devices as STDP-enabling synaptic devices or MAC operation facilitators.

The main obstacle to realizing the full potential of RRAM crossbars is the number of both device-level and system-level nonidealities. These include device-to-device and cycle-to-cycle variabilities, a limited number of resistance states or a narrow

operational range of resistance modulation, nonlinearity of both voltage–current characteristics and pulse response of devices, and high line resistances in crossbar arrays. Despite these, SiO$_x$-RRAM devices have been used to implement weights in physical neural networks, in which multiple weight values (memristive resistance states) are required.[51]

Figure 12a,b shows the feasibility of achieving multiple resistance states in intrinsic SiO$_x$-RRAM devices by controlling the reset process (i.e., varying the reset voltage) during voltage sweeps. Stable resistance states are achieved as devices reset gradually from the LRS to the HRS. However, for practical applications, pulse operation is preferred. In this case, the gradual reset dynamics is highly dependent on voltage amplitude and pulse width, as clearly shown in Figure 12c,d. Programming curves that gradually switch devices from the LRS to the HRS (see for instance Figure 12d) are typically called LTD and are akin to synaptic functionality. As these figures show, the memristive devices could be challenging for implementation of distinct resistance levels required for learning and inference in artificial neural networks. In addition, other nonidealities such as device failure and fabrication yield are present that can affect the network performance.

We have studied extensively the effects of various memristors' nonidealities on inference accuracy, using the MNIST handwritten digits dataset,[51] where the neural network weights are represented as memristive device-resistant states, as shown in **Figure 13**. **Figure 14** shows examples of the impact of yield and device failure on inference accuracy, as well as that of varying the number of resistance states with different schemes to map device resistance onto ANN weights, as shown in Figure 13.
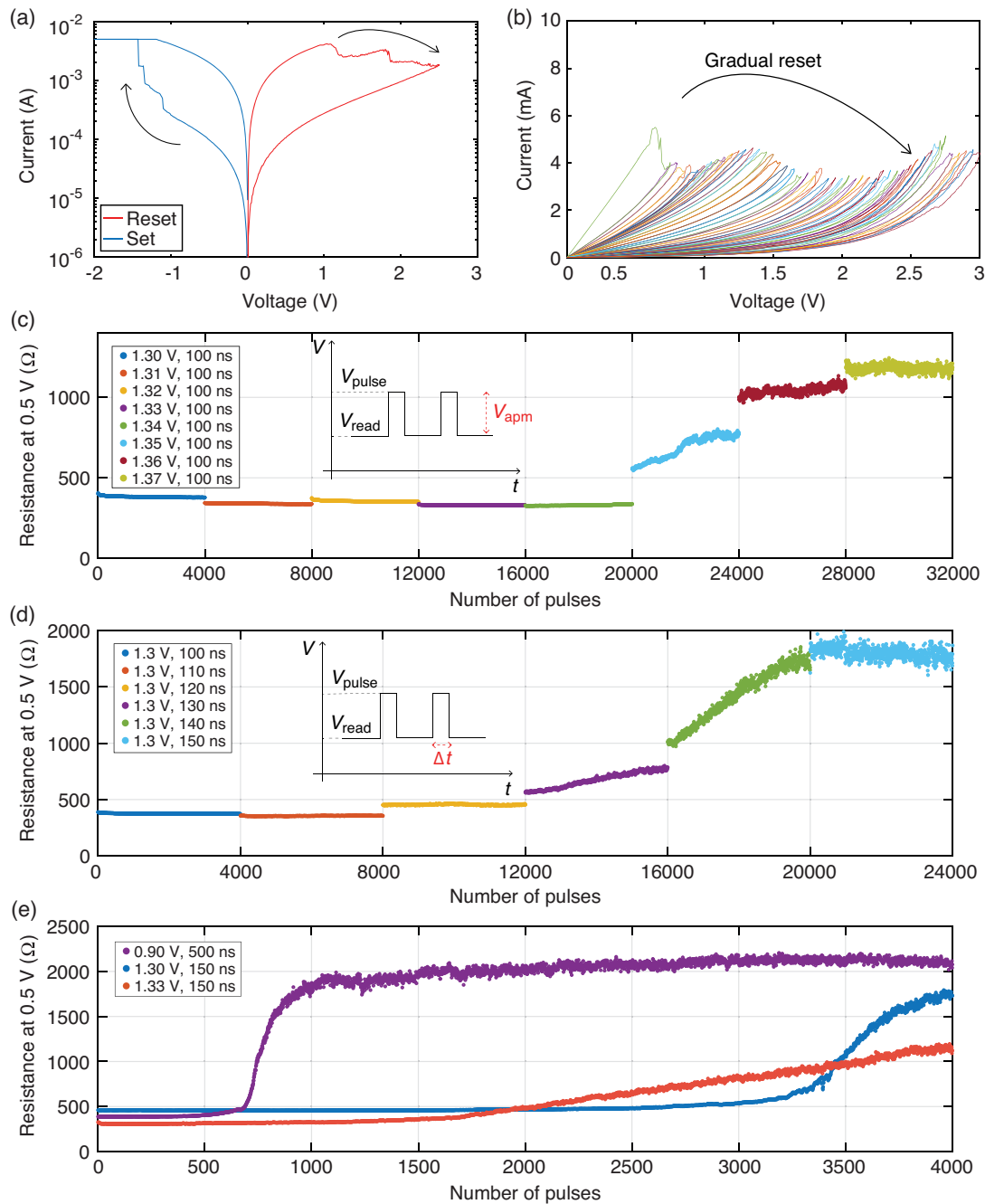
Figure 12. a) *I–V* curves demonstrate a typical bipolar resistance switching. b) Adjustment of reset voltage shows a gradual reset process achieving multiple stable resistance states. Dynamics of resistance increase (LTD) is highly dependent on both pulse amplitude and pulse width. This is demonstrated in (c) and (d) receptively. e) Three very different LTD curves are obtained from the same RRAM device by changing the pulse amplitude and width. Reproduced under the terms of the CC BY license.[51] Copyright 2019. The Authors, published by Frontiers Media.

From these figures, it is evident that higher-device nonidealities result in lower inference accuracy in the implemented classification task for MNIST. The figure also suggests that small-device nonidealities (<10%) do not significantly affect the performance of the implemented SiO$_x$-based neuromorphic system, which uses memristors as programmable weights, whereas learning happens through supervised backpropagation (BP).[51]

In a similar study to the one explained earlier, we developed another SiO$_x$-based memristor neuromorphic learning platform, in which a three-layer neural network (shown in **Figure 15**a) was designed and trained for the classification of MNIST dataset (784 × 64 × 10) and topology patterns (TP) of the atmosphere effect (256 × 64 × 7).[38] Note that the experimental LTP and LTD property of the synaptic devices was used to devise a

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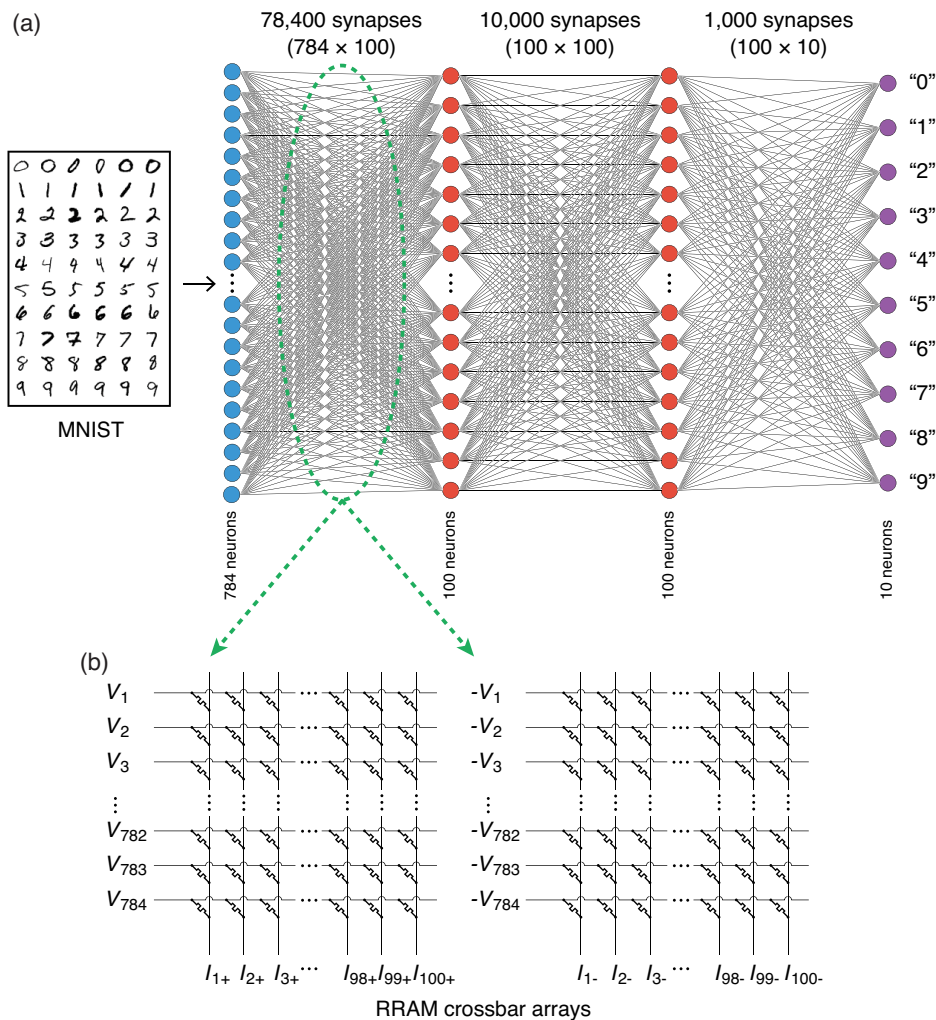**SYSTEMS**
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Figure 13. a) The structure of the implemented ANN for MNIST classification task. b) The network weights at each layer are mapped to a two-*x*bar structure. Here, the network has two hidden layers. Reproduced under the terms of the CC BY license.[51] Copyright 2019. The Authors, published by Frontiers Media.
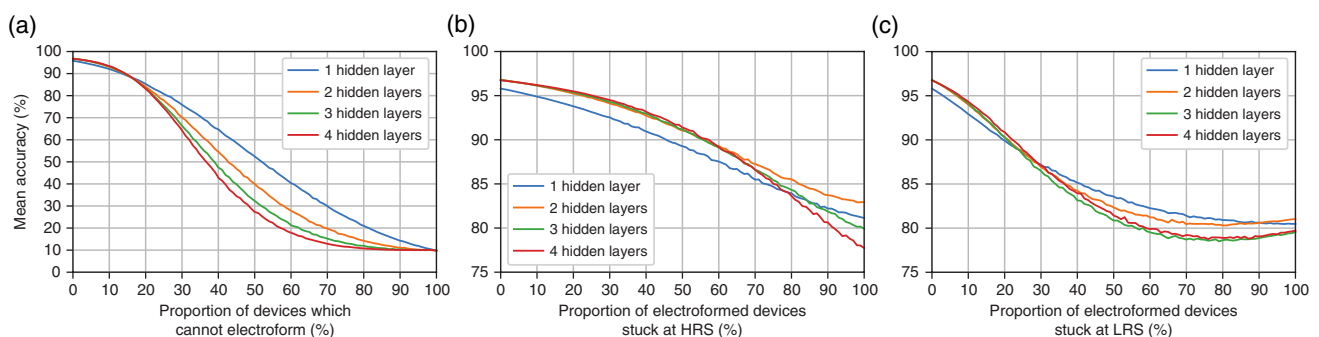

Figure 14. The decrease in inference accuracy of RRAM-based ANNs from a) the effect of un-electroformed devices, b) devices failed at HRS, and c) devices failed at LRS. Adapted under the terms of the CC BY license.[51] Copyright 2019. The Authors, published by Frontiers Media.

function of synaptic weight (W) with respect to the input pulse numbers.[85] During the training process, the feedback error of network weights obtained from the BP algorithm was modulated using the function. Then, the deviation between the output and the target signal was minimized in the learning process. We found that the network learning performance relied heavily on the linearity and accuracy of the weight resistance tuning process that was developed for the memristive network.
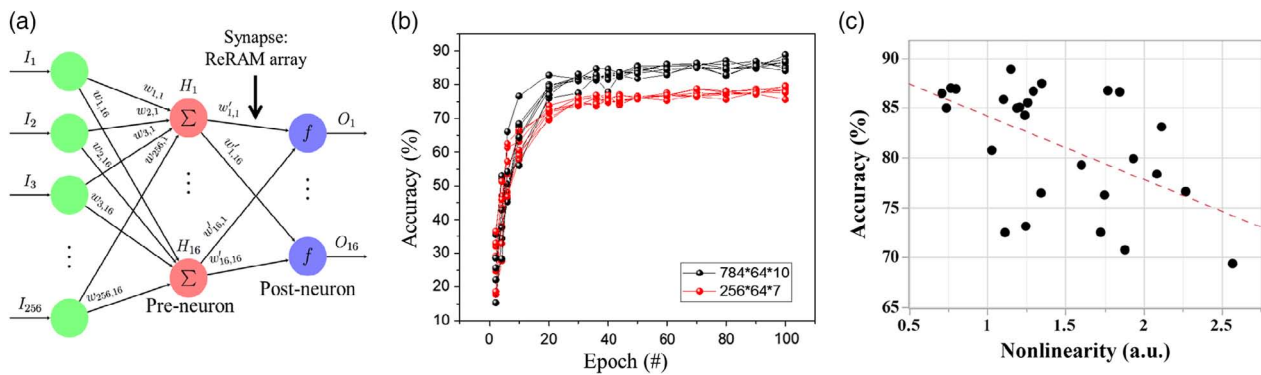
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Figure 15. a) The structure of the simulated neural network is shown. It learns through BP algorithm and supervised training. b) The actual network sizes are $256 \times 64 \times 10$ and $256 \times 64 \times 7$, which achieved different accuracy levels after 100 learning epochs for various device-to-device variation levels (each curve), averaged around 89% and 80%, for the two network sizes for MNIST and TP classification. Note that the convergence speed was similar in both network sizes and for various device variation levels. c) Correlation between LTP and LTD nonlinearity effect and the simulated accuracy is shown.

Figure 15b shows that the best learning accuracies achieved for MNIST and TP are around 89% and 80%, respectively. The figure also shows that there is no clear difference between various device-to-device variation cases. Furthermore, the accuracy correlation with LTP and LTD nonlinearity (as defined in a previous study[85]) is shown in Figure 15c. It is shown that the implemented neuromorphic learning system that uses SiO_x-based weight reaches a simulated accuracy of up to 90%, but the accuracy decreases with the increase in nonlinearity by a slope of 6.

The promising neural network learning results shown in Figure 15 were achieved using the simple SiO_x-based metal–insulator–metal (MIM) structure in place of the network weight elements, in a crossbar structure. In addition, it has been shown[86,87] that such MIM devices simplify memory array design if used in a crossbar architectures. However, the leakage through the sneak paths inevitably induced while accessing MIM crossbar networks may cause weight variation issues detrimental to the development of reliable memristor-based neuromorphic learning and computation.[88] To mitigate the sneak paths currents, a diode or a selector device is usually positioned in series with a memristor cell to form a 1D–1R or 1S–1R structure.[89,90] These configurations considerably increase fabrication and circuit design complexity and cost.

To address this problem, in **Figure 16**, we have developed a selectorless memristor, which does not require a 1D or 1S series connection. This is achieved using simple high-k/low-k bilayer stacks (as shown in Figure 16b). The intrinsic selectorless property (or the nonlinear *I–V* characteristics, as shown in Figure 16a) can be realized by inserting an ultra low-k layer (e.g., SiO_x layer or graphite oxide layer).[91] The main benefit here is that the ultra low dielectric constant layer provides nonlinearity intrinsically by carrier transport formulation design, specifically in Poole–Frenkel defect cases.[92]

Here we use this selectorless memristor to demonstrate neuromorphic learning. Figure 16a shows typical bipolar resistive switching *I–V* characteristics during DC voltage sweeps for HfO_x single layer (H11) and HfO_x (7 nm)/graphite (5 nm) stacked (H7G5) bilayer selectorless memristive devices. The sneak path current in H7G5 device can be avoided by taking advantage of nonlinearity in the self-rectifying *I–V* characteristics

of this device. The *I–V* characteristics shows that the H11 has a higher sneak path current at LRS. Therefore, the H7G5 structure can be used that shows the self-rectifying behavior, where the LRS current is suppressed and sneak paths current can be eliminated.

Figure 16b shows the TEM image of the H7G5 stacked selectorless memristor device. The device structure and fabrication processes have been fully described in a previous study.[93] The immunity to the sneak path currents introduced through the nonlinearity of the selectorless devices introduced here mitigates the potential weight variability in neuromorphic learning and computing applications. Moreover, the selectorless device introduced can result in larger crossbar sizes, as shown in the figure. This results in a larger number of wordlines, which in turn means a bigger network suitable for extended computing demands.

Figure 16c shows LTP (top) and LTD (bottom) behaviors using identical pulses method to examine the conductance flexibility and modulation in H7G5 devices. For depression, the pulse height is -0.7 V with 50 μs pulse width; for potentiation, the pulse height is 1.54 V lasting for 100 μs. Figure 16d shows the simulation accuracy results obtained using H11 and H7G5 selectorless devices mapped into the three-layer neural network shown in Figure 15a for classifying the handwritten digits MNIST dataset. As the figure shows, the best classification accuracy achieved using the network composed of the H7G5 devices is around 85%, which is far better than that of the network using H11 devices (30%). This network uses selectorless RRAM devices as their weight elements, which suppress the sneak path current without the need for additional transistors compared with previous designs.

In all aforementioned learning experiments performed using SiO_x devices, neural networks were simulated with realistic device models, where learning occured through machine learning approaches such as BP. In these networks, the memristive devices were mainly used as weight elements, which are programmed to represent a certain resistance state. Therefore, no unsupervised learning through neural-inspired algorithms such as STDP, similar to that shown in Figure 11c, occured. However, it has been shown that memristive devices can be used to perform unsupervised learning through synaptic plasticity mechanisms used in neuromorphic systems. In the next section, we
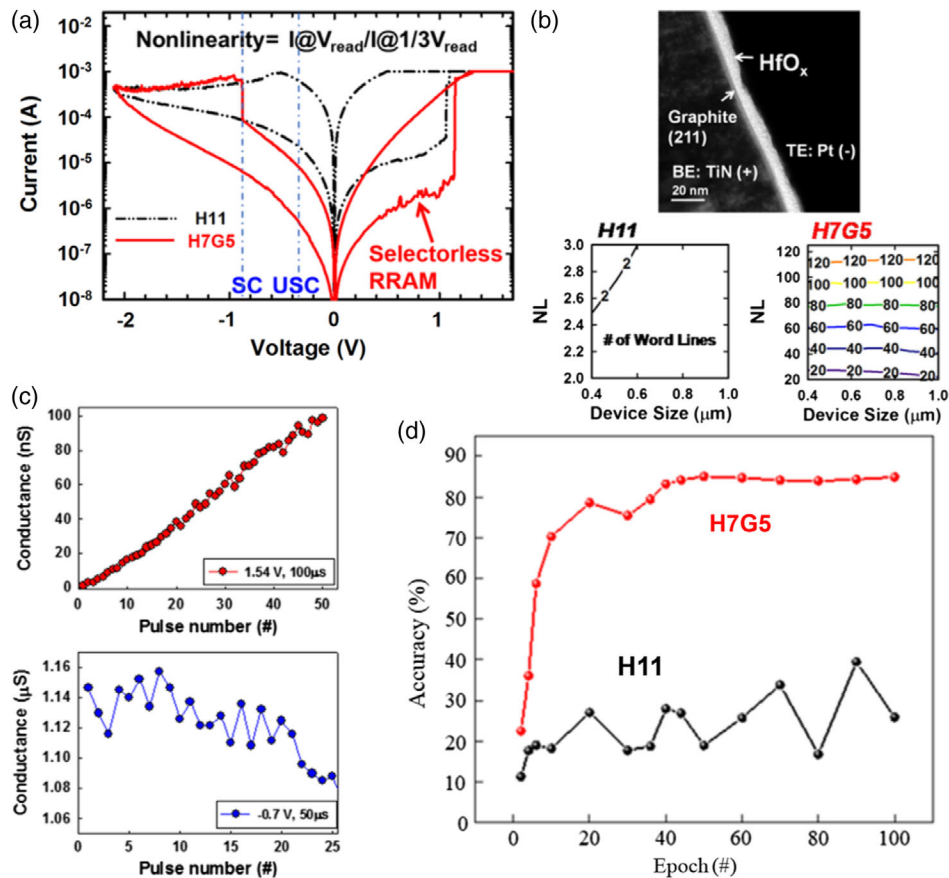
Figure 16. a) *I–V* characteristics of bipolar resistive switching operation in HfO_x single-layer memristor (H11) and selectorless HfO_x (7 nm)/graphite (5 nm) stacked memristor (H7G5) (Adapted under the terms of the CC BY license.[91] Copyright 2019. The Authors, published by Springer Nature). b) TEM image of a sample H7G5 stacked device is shown at the top (Adapted with permission.[93] Copyright 2019, The Royal Society of Chemistry.) and crossbar array size calculation based on measured nonlinearity and memory window with various device sizes (0.4, 0.6, 0.8, 1 µm) on H11 and H7G5 devices are shown at the bottom. c) The LTP/LTD behaviors using identical pulses are shown for H7G5 devices. d) Neural network simulation accuracy using BP algorithm and supervised training is shown. The accuracy is around 85% for H7G5% and 30% for H11. A similar network to that shown in Figure 15a was used.

provide simulation results of a memristive neuromorphic system that uses STDP for unsupervised learning of simple patterns.

3.3. Hybrid CMOS–Memristive Neuromorphic Sensing

The use of memristors as a processor of input sensory information has rapidly gained traction but has only had limited success in the frontend generation of sensory data. For example, in previous studies,[16,94] both works use memristive meshes for spatiotemporal smoothing of information as a way to reduce noise through averaging. The resistive power dissipation and lack of equal set/reset processing speeds have made it too difficult to justify the additional fabrication steps required to implement thin-film metal-oxide memristors in the back-end-of-the-line (BEOL) for CMOS integration.

In the circuit shown in **Figure 17**a, we present a novel memristor–CMOS image circuit that utilizes temporal storage of information in RRAM to block signals in the absence of temporal change in light intensity. This circuit is an extension and improvement on what is presented in the image sensing circuit from a previous study,[16] which relied on the use of a

separate match line for voltage comparisons to a constant reference. A constant reference means that an output was generated at the source of a transistor M3 when input intensity exceeded some threshold; that is to say, there was no detection of temporal difference of intensity, and therefore light adaptation was a mechanism of DC thresholding. We draw inspiration from dynamic vision sensors here, but rather than using a capacitance to block DC content, we rely on the identical signals generated from the application of a read pulse to a pair of identically programmed memristors at two consecutive points in time to block the output. The voltage and memristor state X read-out are shown in Figure 17b, and the use of the match line alone in a spike-based programming scheme is shown in Figure 17c. The output signal from the image-sensing circuit is passed through a subthreshold amplitude-to-frequency converter which generates voltage spikes, in a manner similar to that of the retinal ganglion cells,[95,96] the schematic of which is shown in Figure 17d, and array-based architecture of image sensor interfacing to subthreshold cell circuits in Figure 17e. The final spiking output results are shown in Figure 17f for a given input of light intensity change. The chip is fabricated in the SK Hynix
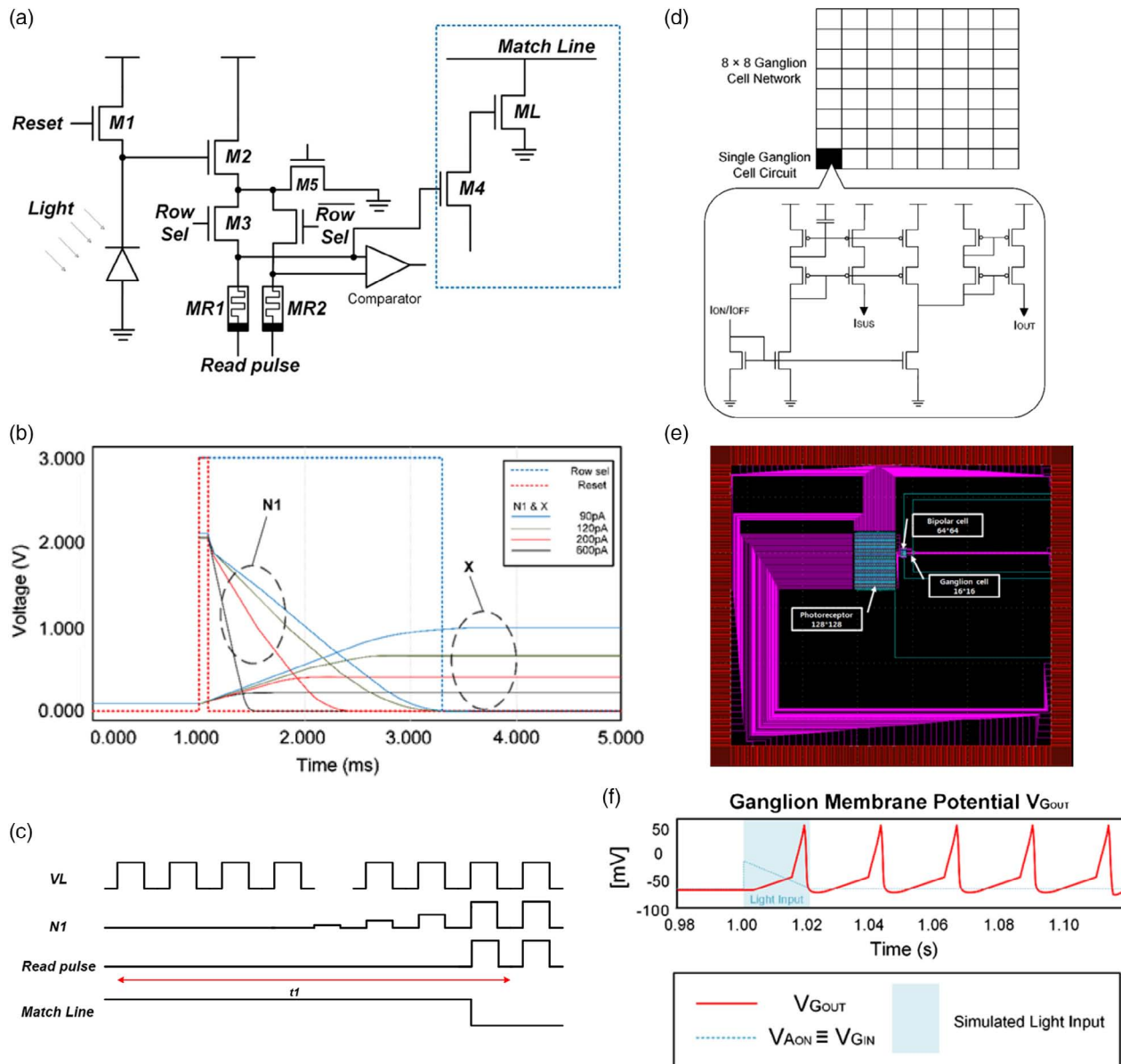
Figure 17. a) The schematic structure of the CMOS–RRAM photoreceptor. b) Photoreceptor cell output and state response. c) Photoreceptor cell pulsing. d) Circuit schematic of a ganglion cell-inspired subthreshold CMOS amplitude-to-frequency converter. The ganglion cell circuit accepts current as input from the previous image-sensing stage and will only generate an output where there has been a change in intensity, to achieve retina-like power optimization. e) Retinal network CMOS chip layout. The full flow of photocurrent commencing at a 128 × 128 array of photoreceptor cells, which are averaged to a 64 × 64 bipolar cell network to produce a graded action potential and are subsequently converged to a 16 × 16 retinal ganglion cell network for fast spike generation. f) Experimental results of the RRAM–CMOS retinomorphic architecture. e,f) Reproduced with permission.[16] Copyright 2018, IEEE.

180 nm process, $V_{DD} = 1.8$ V and $V_{th} = 0.4$ V. Here, $V_{G_{OUT}}$ is the voltage-converted current output, whereas $V_{A_{ON}}$ and $V_{G_{IN}}$ are the voltage-converted inputs from the preceding stage. Note that the response is shifted negatively to replicate a biologically plausible resting membrane potential.

3.4. Simulation of Memristive Neuromorphic Computing

Biophysical neuron models, such as those developed for HH and ML neurons, have shown memristive behavior in their footprint.[97,98] There exist only a few experimental implementations[62,99] of memristor-based biophysical neurons due to the high complexity of the neuronal dynamics and bifurcation behaviors. To the best of our knowledge, there is no memristive biophysical neuron-based network, which has been tested for any type of application. To address this challenge, one approach is to develop and utilize simulation frameworks for memristive neuromorphic networks. Significant research[64,100–102] has been conducted on simulating memristive networks, where experimental implementation cannot be conducted due to the network

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size, complexity, technology limitations, etc. The simulation analysis can provide insight into the dynamical behavior of the equivalent memristive circuit model of various neuron models and the learning behavior and performance of their network.

We have developed and simulated simple crossbar structured memristive networks to validate the functionality of the

biologically-inspired ML and HH memristive neurons (that were shown in Figure 9), in a simple pattern classification task. **Figure 18**a shows the STDP learning mechanism for two coupled HH neurons with memristive synapses in a small-scale crossbar structure. Figure 18b shows the membrane voltage of pre- and postsynaptic HH neurons connected by a memristive synapse for
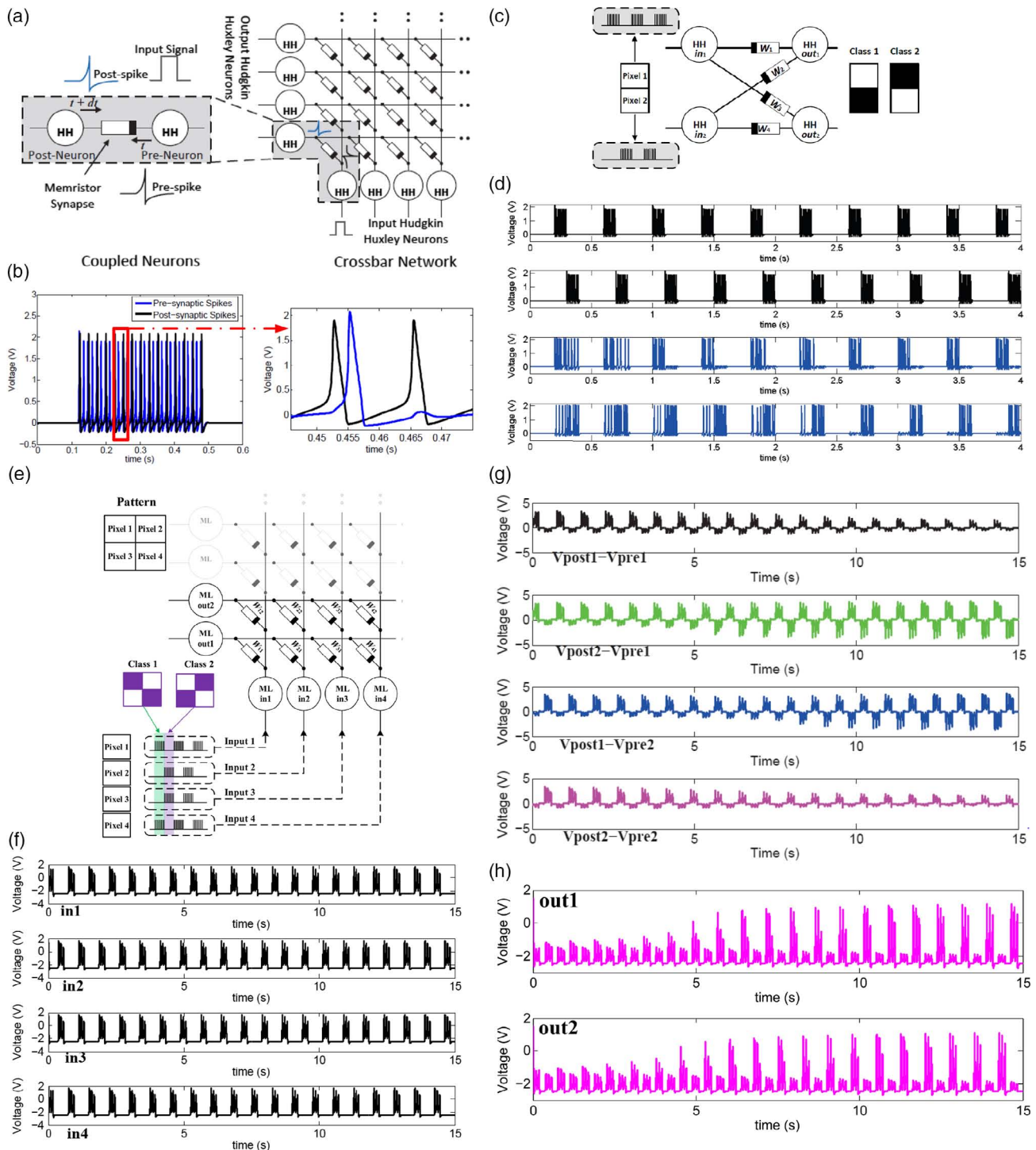

Figure 18. Simple patterns are classified by HH and ML memristive neurons, connected through crossbar structures of memristive synapses, following STDP learning, through overlapped input spikes. Adapted with permission.[65,66] Copyright 2016 and 2017, IEEE.

a 15 µA stimulus current. Figure 18c shows a 2×2 two-layer perceptron network with HH neurons and memristor synapses, where the inputs are two classes of two-pixel images. The classification results of the two-pixel input patterns performed by the 2×2 memristive network are shown in Figure 18d. Here, the membrane voltages of the presynaptic (black) and postsynaptic (blue) memristive HH neurons are shown. Initially, postsynaptic neurons spike without any specific pattern, and it takes some times for them to follow the input patterns. The learning is unsupervised and the winner neuron follows one of the patterns based on its initial weight vector. When the class 2 image is assigned to postsynaptic neuron 1, the weight of memristive synapse 1 increases due to STDP. As post-synaptic neuron 1 spikes after presynaptic neuron 1 (a black pixel makes a neuron spike), the weight of memristive synapse 1 increases. Also, the weight of memristive synapse 2 decreases as postsynaptic neuron 2 is inactive whereas presynaptic neuron 1 spikes.

Figure 18e shows a 4×2 two-layer perceptron network with ML memristive neurons and memristive synapses. In this case, inputs are two classes of four-pixel images. Four presynaptic neurons' membrane voltages are shown in Figure 18f, which show their spiking activity, after applying the input spike trains. LTD and LTP phenomena are shown in Figure 18g during the classification in the memristive network on the synaptic devices. Finally, Figure 18h shows postsynaptic neurons' membrane voltages and the results show successful classification of the two classes of input patterns, where after 5 s, neuron 1 fires for one pattern, whereas neuron 2 fires for the other pattern.

4. Discussion and Conclusions

Neuromorphic computing is a far-reaching field that encompasses the hardware implementation of basic artificial neural networks, through to biologically plausible spike-based systems. In both cases, learning and inference are the cornerstones of building functional large-scale networks that facilitate tasks that are fundamentally tied to neural cognition.

We have shown how CMOS and memristive systems have become highly pervasive in neuromorphic computing as they mimic the functional primitives of SNNs and artificial neural networks alike and reproduce neuronal and synaptic models at the device/physics level. While various RRAM switching mechanisms are available, we have focused on the use of filamentary-based switching and joule-heating modulation in SiO_x memristors to construct substantially simplified neurons and synaptic circuits when compared with their purely CMOS counterparts. In essence, the integration of nanoscale nonvolatile devices in the BEOL has completely removed reliance on physically disparate volatile DRAM or SRAM arrays, where information transfer is thwarted by restricted bus sizes.

The von Neumann bottleneck in conventional computing systems is alleviated by leveraging analog domain in-memory computing in memristive crossbar systems capable of spike-based and nonspiking training and inference, both supervised and unsupervised. This was demonstrated in both oxygen migration of hafnium-oxide devices and filamentary growth within SiO_x memristors, which may be integrated with active CMOS arrays or passive arrays by exploiting highly nonlinear characteristics

that exhibit diode-like suppression of sneak paths currents. As cognitive neuroscientists better understand that learning mechanisms that occur within our neural systems, having a fundamental physical device-level primitive enables an optimized mode of implementation that can be used to successfully demonstrate more complex learning rules and higher-order behaviors such as triplet-based, quadruplet-based STDP, and beyond.

In-memory processing has also been demonstrated in similar analog domain form by implementing multibit flash cells, but these are bottlenecked by the lower-limit technology nodes that floating-gate transistors are fabricated in, and memristive devices appear to be the prime candidates for moving beyond such limitations. An alternative in both array-based computing and biological spike generation has been shown in the form of subthreshold analog circuits such as those shown in this article, which take advantage of ultralow power consumption but suffer from extremely high RC delays which are introduced from high drain-to-source equivalent resistance values when the channel has not been fully inverted due to low voltages applied at the gate.

Neuromorphic engineering is not limited to drawing inspiration from the processing that occurs within the brain and can be broadened to any biological process. We have demonstrated neuromorphic vision sensing by developing a RRAM-based adaptive image sensor, which is equally important as a method to optimize the frontend procurement of information that is transmitted to the processor. The notion that event-based processing strips input data of redundancy and that the retina implements ultralow power processing through adaptive vision are replicated in our sensory neuromorphic RRAM–CMOS integrated system. The realization of fully optimized systems may require similar approaches in integrating neuromorphic processing with front-end neuromorphic sensing.

The advantages of RRAM-based neuromorphic computing are naturally counterbalanced by the requirement to convert read-out currents into digital domain information for interfacing with computing systems, and this requires the use of analog-to-digital converters (ADCs) which partially offset the power, speed, and area advantages of purely RRAM neuromorphic systems. Current integration techniques use active resistive switching layers above higher-level metal layers for any technology process, which enables us to take advantage of vertical real estate of a chip and relax the burden of planar topological area. The same methodology has been applied in using FinFET technology to reduce the impact of electron traps in creating channels with a larger cross-sectional area for CMOS scaling below 5 nm feature sizes. There is a continued need to explore the effect of noise associated with analog computing and quantization effects on precision but with the silver lining that neural networks can be designed to be robust to minor errors, signal fluctuations and nonidealities, making them optimal candidates for applications in soft computing.

In addition, retention degradation (i.e., time-dependent RRAM state decay) and its impact should be considered in neuromorphic computing, as it is done in previous works such as a study by Wu et al.[103] At a temperature of 85 °C, stacked TaO_x devices have shown retention times of over 10 years.[104] Though when baking at higher temperatures, a 12% degradation in classification on the MNIST dataset is observed, and most degradation

occurs after 10^4 s.[105] As a result, a refresh operation is required in practical applications to maintain the accuracy.

To further improve retention, electrical design at the state level (e.g., compliance current limiters) should be fine tuned. From a structural and architectural perspective, oxygen exchange layer (OEL) and one transistor-one resistor (1T–1R) cells are needed to mitigate stochastic oxygen vacancy generation, annihilation, and overshooting pulses. The use of stacked-layer structures and thin-film plasma treatment are also helpful to eliminate the defective states recovery. At the board level, a passive heat sink is a common practical solution to prevent thermal throttling during heavy workload cycles.

It should also be noted that semi-volatile devices, such as WO_x from previous studies,[106,107] which display millisecond retention characteristics, may also be leveraged as LIF neurons. This enables devices to reproduce time-dependent spiking adaptations which have been observed in pyramidal neurons and is useful in reservoir computing, thus efficiently processing temporal information.[108]

At this stage, researchers have a strong idea of the architecture of biological cells within sensory systems such as the retina and, to some extent, the brain as well. However, what is lacking is a unified account of the computation that takes place within biological sensors and how they process, filter, and store information before transmitting them to the brain. As neuroscientists converge toward a better understanding of the biological processing that takes place across the nervous system, CMOS and memristive researchers will be able to continue to cooperate in building large-scale systems to both better understand the cognitive circuits in performing functional and behavioral tasks such as pattern recognition and higher-order interpretation and introduce the low-power and highly adaptive advantages of biological processes to conventional computing.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

complementary metal-oxide semiconductors, memristors, neuromorphic computing, resistive random access memory, unconventional computing

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