TALK **THURSDAY 12.15PM**

Digital, analog, and memristive implementation of spike-based synaptic plasticity

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Synaptic plasticity is believed to play an essential role in learning and memory in the brain. To date, many plasticity algorithms have been devised, some of which confirmed in electrophysiological experiments. Perhaps the most popular synaptic plasticity rule, or learning algorithm, among neuromorphic engineers is the Spike Timing Dependent Plasticity (STDP). The conventional form of STDP has been implemented in various forms by many groups and using different hardware approaches. It has also been used for applications such as pattern classification. However, a newer form of STDP, which elicits synaptic efficacy modification based on the timing among a triplet of pre- and post-synaptic spikes, has not been well explored in hardware.

We have investigated and designed a number of STDP and TSTDP electronic circuits using different hardware approaches, including analog, digital, and memristors. All these implementations are able to completely and with a minimal error replicate the outcome of a wide range of biological experiments. They have also been verified to reproduce a spike rate-based synaptic plasticity behavior similar to the Bienenstock Cooper Munro (BCM) rule. We have used a number of these implementations in a spiking neural architecture comprising of different types of neurons to perform cognitive tasks such as pattern classification and unsupervised character recognition.

Our electronic implementations of the TSTDP rule can be used in large-scale analog, digital, or memristive neural architectures, to improve their synaptic plasticity capabilities. This will result in more biophysically faithful neuromorphic systems providing a better medium for neuroscience research.