



# VU Research Portal

## Processor Architecture, by S. Lavington

Tanenbaum, A.S.

### **published in**

Computer Architecture News  
1978

### **document version**

Publisher's PDF, also known as Version of record

[Link to publication in VU Research Portal](#)

### **citation for published version (APA)**

Tanenbaum, A. S. (1978). Processor Architecture, by S. Lavington. *Computer Architecture News*, 6(6), 31-31.

### **General rights**

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal ?

### **Take down policy**

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

### **E-mail address:**

[vuresearchportal.ub@vu.nl](mailto:vuresearchportal.ub@vu.nl)

S. H. Lavington,  
Processor Architecture,  
NCC Publications, Manchester, 1976, 126pp

This slim volume provides a cursory introduction to the subject of computer architecture. It is too short to be of much use to computer science students and too elementary to be of much use to computer science professionals, but it might be of interest to electrical engineering students whose primary interest was not computers, but who nevertheless wished to learn a little bit about computer architecture in as painless a way as possible. In particular, about half the book is devoted to a discussion of a hypothetical minicomputer, which is intentionally simple enough to be built by the students from scratch as an exercise.

There are five chapters, covering basic concepts (what a stored program computer is, word length, etc), CPU design (gates, adders, timing signals, etc.), the order code for the hypothetical mini, the i/o structure for the hypothetical mini, and large computer systems. There are also five appendices: binary numbers, binary addition, CPU configurations, references, and answers to some of the problems. There is also an excellent index, ten percent as long as the book itself!

The first chapter begins immediately with the design of the hypothetical mini, called the SM104 in chapter 3. Much of the chapter deals with the components of the system such as main store, ALU, and the various registers, and their interconnections. There is also a section explaining that "primitive" instructions such as load accumulator are carried out as sequences of yet more primitive micro-operations. The obvious way to describe this would be in terms of a hypothetical interpreter, i.e. a microprogram. Unfortunately there is no mention of the idea of interpretation here.

Chapter two is concerned with gates, flip flops, serial adders, ripple adders, synchronous and asynchronous computers, timing and control signals and the like. It is questionable whether such topics really belong in a book on processor architecture, since these matters are all transparent to the programmer.

The next chapter describes the order code for the SM104 in detail. It is a 16 bit mini, with one accumulator, 4 index registers, and 16 instructions. There is a nice discussion of design criteria for an architecture on page 41, starting with the sentence: "The processor architecture should en-

able the most used programming tasks to be performed most easily."

It is thus disappointing that the mini is rather old fashioned. If the author had started out with the concept of interpretation in mind, he could have nicely shown how an attractive instruction set could have been implemented by interpretation using a very simple hardware base. As it is, the reader is left with the feeling that minicomputers necessarily have dreadful architectures for reasons of cost.

The fourth chapter introduces i/o using the paper tape reader as an example. Then the difference between polling and interrupts is covered. Then comes a long discussion on how the SM104 does i/o, including 3 pages about how to bootstrap it into operation. Lastly there is a section on technology (TTL vs. ECL vs. MOS), but very superficial.

The last chapter is far and away the best. In it, the interaction of block structured languages and the stack, cache memories, virtual memory, The MU5, and capabilities are mentioned. There is also a section on 0,1,2, and 3 address machines, in which it is claimed that the PDP-10 is a one address machine, the IBM 370 a two address machine, and the CDC Cyber a three address machine. Depending on whether or not one considers registers to be addresses or not, this is misleading at best.

In many ways the book (published in 1976) is already seriously dated. The use of an instruction set with a 4 bit opcode, 2 index bits, and 10 bit address field for the example machine is hardly modern. Also there are numerous quotes throughout the book that give one a feeling it was written quite a while ago. For example, "The control store is normally read only, but changes to its contents can be made manually," (page 34); "It is difficult on a small machine to provide a store protection system which is fool-proof without being unduly restrictive," (page 59); "As an indication of the cheapness and compactness, though, an 8 bit MOS microprocessor module is available which gives all the functions of a simple ALU for a price of about £150," (page 78).

In short, the book might be useful in an electrical engineering laboratory where students were to build the SM104 machine, but for other purposes it is too superficial and outmoded already.

Andrew S. Tanenbaum  
Amsterdam, The Netherlands