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To my parents

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Nomenclature

PWM: Pulse Width Modulation

True-PWM-Pole: True PWM Zero Voltage Switching Pole inverter

NPC: Neutral-Point-Clamped inverter

ARCPI: Auxiliary-Resonant-Commutated-Pole-Inverter

ACRLI: Actively-Clamped-Resonant-DC Link-Inverter

DPM: Discrete-Pulse-Modulation

ZVS: Zero-Voltage-Switching

ZCS: Zero-Current-Switching

SVM: Space-Vector-Modulation

FFM: Fundamental-Frequency-Modulation

C_1, C_2: DC link capacitors

C_m: clamping capacitor

C_f: output filter capacitor

C_{r1}, C_{r2}, C_{r3}, C_{r4}: resonant capacitors

C_s: snubber capacitor

d: instantaneous duty ratio

d_1, d_2, d_3, d_4: instantaneous duty ratios of cell 1, 2, 3, 4

f_m: fundamental output frequency

f_c: switching frequency

G: self-balancing constant

i_{cm}: instantaneous clamping capacitor charging current

$i_{cm \cdot rms}$: instantaneous clamping capacitor rms current

i_{lrprms}: instantaneous resonant inductor rms current from diode to switch commutation

i_{lrnrms}: instantaneous resonant inductor rms current from switch to diode commutation

i_{lrrms}: instantaneous resonant inductor rms current

i_o: instantaneous inverter output current

i_n: instantaneous current out of the neutral point

i_{load}: instantaneous output filter inductor current

$I_{o \cdot rms}$: inverter output rms current

I_p: inverter output peak current

I_{TQ}: device actual turn-off current

I_{rr}: freewheeling diode reverse recovery current

k: auxiliary transformer ratio

L_{r14}, L_{r23}: resonant inductors

L_f: filter inductor

L_s: snubber inductor

mod(t): modulating sinusoidal reference

M: index of sub-harmonic modulation/number of inverter levels

p: number of switching cells

P_o: output power

P_s: snubber loss

Q: quality factor

R: resonant loop equivalent resistance

R_o: load resistance

SW: NPC leg switching function

SW_1: switching function of cell 1

SW_2: switching function of cell 2

T: switching cycle

V_{dc}: DC link voltage

V_{s1}: device blocking voltage of switch S_1

v_o: instantaneous inverter output voltage

$V_{o\cdot rms}$: inverter output rms voltage

v_{cr1}: instantaneous voltage of resonant capacitor C_{r1}

v_{cm}: clamping voltage during dynamics

v_{cs}: instantaneous auxiliary capacitor C_s voltage

v_{d1}, v_{d2}: DC link capacitor voltages during dynamics

v_{AO}: direct inverter output voltage during dynamics

Z_o: resonant impedance

θ: leading angle of output voltage versus output current

δ: declining factor of output low-pass filter

σ: snubber loss factor

ω_m: inverter output fundamental angle frequency

ω_c: sub-harmonic carrier angle frequency

Δv_{AO}: direct inverter output voltage variation to clamping voltage perturbation

Δi_{load}: load current variation to clamping voltage perturbation

Δi_{cm}: clamping capacitor charging current variation to clamping voltage perturbation

$\Delta i_{cm \cdot dc}$: DC component of Δi_{cm}

Δi_n: i_n variation to neutral potential perturbation

Δi_{ndc}: DC component of Δi_n

Abstract

This thesis deals with the soft switching techniques applied to multilevel inverters for high frequency high voltage and high power conversion. The following subjects are studied to this end:

1. Multilevel inverter operation. After the brief inspection of the conventional high power converter structures employing device association or converter association, fundamentals and problems of the multilevel inverters evolved from cell association are examined. Clamping voltage stability of the capacitor clamping inverter and the neutral potential stability of the diode clamping inverter are explored in details.

2. Multilevel inverter commutation. Major snubbers used in two-level and multilevel inverters are reviewed. The problems associated with these snubbers are outlined. Further, soft switching techniques reported for two-level inverters are assessed.

The transformer connection True-PWM-Pole technique is proposed and tested. It is then utilized and tested in three level capacitor clamping inverter and the Neutral-Point-Clamped (NPC) inverter. This technique along with the Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI) are both extended to the multilevel case (M>3), the topologies are demonstrated.

Auto-transformer connection and capacitor connection True-PWM-Poles are also discussed.

3. New multilevel inverter topology. A new diode clamping multilevel inverter free of series association of the clamping diodes is introduced, analyzed and tested. It's shortcoming is unveiled. Clamping, snubbing and soft switching of this new inverter are shortly treated.

With this investigation, the basic aspects in regard to soft switching of multilevel inverters are outlined.

Resumo

Esta tese apresenta técnicas de comutação suave aplicadas a inversores com múltiplos níveis para aplicações de alta freqüência, alta tensão e alta potência. Os seguintes assuntos são estudados com esta finalidade:

1. Operação dos inversores com múltiplos níveis. Após breve análise das estruturas de alta potência convencionais que empregam associação de interruptores ou associação de conversores, examinam-se os fundamentos e problemas dos inversores com mútliplos níveis. A estabilidade da tensão de grampeamento do inversor com grampeamento capacitivo e a estabilidade do potencial de neutro do inversor com diodo de grampeamento são exploradas em detalhe.

2. Comutação dos inversores com múltiplos níveis. A maioria dos circuitos de ajuda à comutação (*snubbers*) utilizados nos inversores com dois níveis e com múltiplos níveis é revisada. Os problemas associados a estes *snubbers* são delineados. Além disso, analisam-se as técnicas de comutação suave conhecidas para inversores com dois níveis.

A técnica *True-PWM-Pole* com conexão de transformador é proposta e testada, sendo então utilizada e ensaiada em um inversor com tres níveis com grampeamento capacitivo e em um inversor com grampeamento no ponto neutro (*NPC - Neutral-Point-Clamped*). Esta técnica e o inversor com pólo de comutação auxiliar grampeado (*ARCPI - Auxiliary-Resonant-Commutated-Pole-Inverter*) são estendidos aos casos de múltiplos níveis (M>3) e suas topologias são apresentadas.

Discutem-se também as conexões de auto-transformador e de capacitor para a técnica *True-PWM-Pole*.

3. Nova topologia de inversor com múltiplos níveis. Um novo inversor com múltiplos níveis com grampeamento a diodos, sem necessidade de associação série dos diodos de grampeamento é introduzida, analisada e testada, sendo também apresentadas as suas deficiências. Analisam-se ainda o grampeamento, a estratégia de ajuda à comutação (*snubbing*) e a comutação suave deste novo inversor.

Com esta investigação, os aspectos básicos relativos à comutação suave de inversores com múltiplos níveis são apresentados.

Chapter 1. Fundamentals of Multilevel Inverters

Abstract: This chapter reviews the existing approaches for implementing high power converters. The fundamentals of multilevel inverter circuits, including voltage synthesizing, modulation as well as their specific problems are then discussed. Commutation issues of these circuits are specifically treated which will be the main subject of this thesis.

1.1. Implementation of High Power Converters

The power electronics community has witnessed in the last decade continuous advance in the ratings as well as the switching characteristics of the power semiconductor devices. Most remarkably, the 3.3kV, 1.2kA IGBT modules and the 6kV, 6kA GTO thyristors have entered the market, and the development targets for the near future are the 4.5kV IGBT module and the 9kV-12kV GTO thyristor [1]. However, high power electronics, typically traction drives and supplies or utility applications [2] [3] [4], call for switching operation involving higher voltage or current with adequate performance. To meet this demand, devices, switching cells or converters have been associated as solutions.

1.1.1. Device Association

Parallel association: Converter current handling capability can be raised by paralleling two or more IGBT modules together [5] [6]. The major problem of this association is the unequal current sharing due to the module parameters deviations as well as the construction and thermal coupling issues. Moreover, high current operation demands bulky setup with voluminous power connections evoking problems with stray inductances. In practice, GTO thyristors can not be associated in parallel, which will lead to unequal current distribution [7].

Series association: Series association of GTOs has been a proven technique for high voltage operation in railway interties [7], STATic CONdenser (STATCON) [8] and self-commutated AC/DC converter [9] applications. It is further enabled with the possibility to supply the gate units directly from the main circuit rather than a low voltage supply at the ground level [9] [67]. By device screening, gate units adaptation, precise gate turn-off timing [9] or hard gate drive [7] [10], voltage sharing can be well ensured. Series association of

IGBTs is also under investigation [11] [12]. A distinguished advantage of series association is the redundancy it offers by adding one more device in the ring, as well as the individual device life time extension as a result of voltage stress reduction.

1.1.2. Converter Association

In the case of device association, either parallel or series, the converter waveforms as well as the di/dt or dv/dt rates of change do not benefit from the multiple devices. In converter association, however, multilevel waveforms are synthesized while the di/dt or dv/dt rates remain unchanged. Converter association can be realized in one of the following approaches.

DC side in parallel/ AC side in parallel by transformer: As shown in Fig. 1.1(a), the secondary voltages are imposed and the secondary current ripple is high. To limit this ripple the leakage inductance has to be located at the secondary side, which is not favorable for transformer construction [14]. This configuration is found at the supply side of locomotive drives [3]. But it is not recommended for STATCON application due to the harmonic currents flowing through the inverters and the transformer secondaries [8].

DC side in parallel/AC side in series by transformer: As shown in Fig. 1.1(b), currents at both sides are imposed. The low ripple secondary current results in lower converter losses and magnetic losses. Railway interties [3] and also STATCON [8] [13] have employed such configuration. Transformer leakage inductance can be located at either side.

DC side in parallel/AC side in parallel by Current-Sharing reactor: As shown in Fig. 1.1(c), spontaneous current sharing is achieved through this configuration [15]. Obviously, the number of converters is limited to two.

DC side in parallel/AC side in parallel by separate reactor: As shown in Fig. 1.1(d), by paralleling converter subsystem, this structure is characteristic of its homogeneous modular construction, operation redundancy as well as the reduced current ripple of the summing current. It has been widely utilized especially in industrial drive areas [7].

DC side in series/AC side in series by transformer: As shown in Fig. 1.1(e), again currents at both sides are imposed allowing for lower losses. Such configuration can be found in DC/AC/DC converter applications [16] [17].

DC side in series/AC side in parallel by transformer: As shown in Fig. 1.1(f), voltages of the secondary sides are imposed forcing each converter working independently. The structure enables high voltage operation with reduced harmonics in the summing current [18].

AC side connected to open winding: In this case, the DC side can be either in parallel [19], as shown in Fig. 1.1(g), or series or separated [20]. Chokes to suppress zero sequence voltage are necessary. Again, the number of converters is limited to two.

DC side isolated (H-bridge cascade inverter): As shown in Fig. 1.1(h), the most salient merit of this configuration is the possibility of direct connection to high voltage system, allowing for elimination of the heavy transformer. However, each DC side must be isolated from the other. Literature review shows that this type of inverter has been constructed as broadcasting amplifier by ABB [21] and as high precision current supply for plasma physics by JET [22] more than a decade ago. It has in the recent years been recommended for other applications including industrial drives [23] [24], traction [25], active filtering [26] and especially static VAR compensator [27] [28].

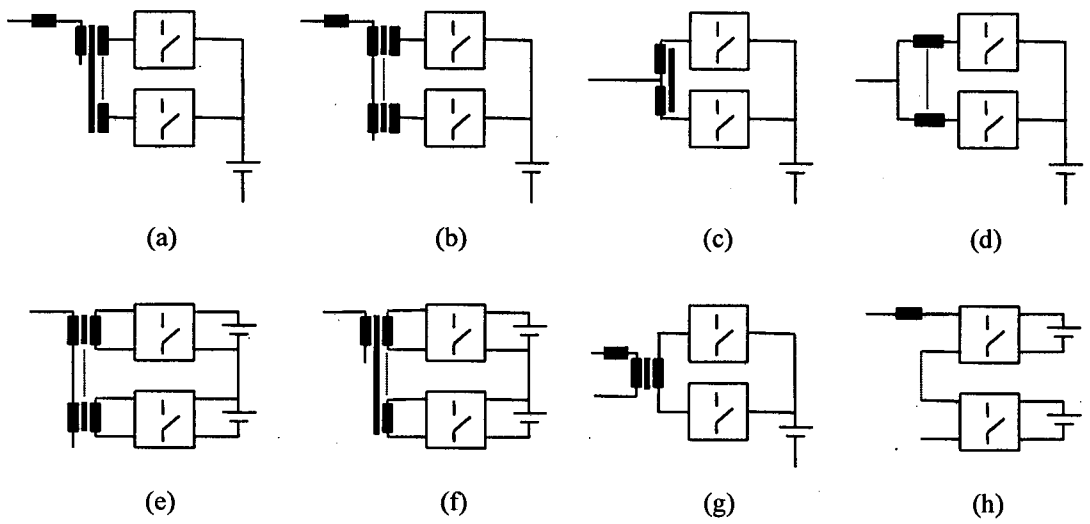


Fig. 1.1. Different circuits resulted from converter association.

1.1.3. Cell Association

Parallel association: As shown in Fig. 1.2(a), the cellular structure allows for feeding high current with greatly reduced ripple [29]. In particular, assuming a non-zero impedance of the voltage source at the switching frequency, current sharing becomes inherent [30]. An alternative technique was also recently explored [31], as shown in Fig. 1.2(b). Direct reactor-less paralleling of cells has also been reported in engineering application, which enhances the current capacity but without reducing the ripple [70].

Series association: Explorations on the series association of cells in the past two decades have given birth to two major structures: the diode clamping multilevel inverter [32]-

[37], and the capacitor clamping multilevel inverter [38] [39]. Except for the three level diode clamping inverter (Neutral-Point-Clamped—NPC) which has now been increasingly accepted by the industry for high voltage high power applications, other circuits of the family are still under investigations.

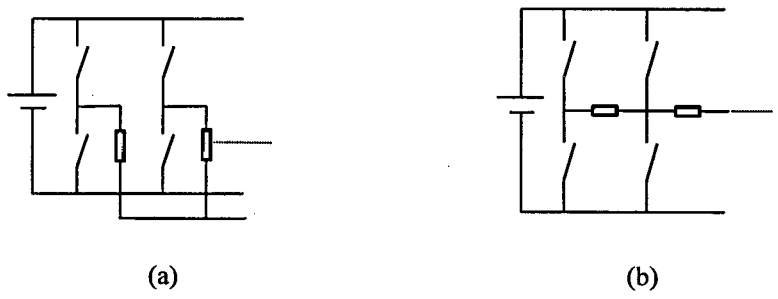


Fig. 1.2. Different circuits resulted from parallel association of cells.

1.2. Diode Clamping Multilevel Inverter

The idea of diode clamping was first established in three level's case, which is now known as the NPC inverter [32][33]. It was then extended to any level by different researchers [34]-[37]. Fig. 1.3 shows a five level inverter leg, which can be regarded as being set-up by four two level switching cells in quasi-series: C_1, S_1, S_1'; C_2, S_2, S_2'; C_3, S_3, S_3' and C_4, S_4, S_4'. Switches S_1, S_2, S_3 and S_4 in the up-arm and also switches S_1', S_2', S_3' and S_4' in the down-arm can be regarded in quasi-series. By timing the switching actions of the corresponding switches in different cells, an output waveform with five level is obtained, while terminal dv/dt remains the same value as each single device sees in the cells.

1.2.1. Voltage Synthesizing

Suppose that the DC link voltage is equally distributed among the four storage capacitors, then a staircase output waveform with reference to the DC capacitor neutral point could be synthesized as shown in Fig. 1.4 according to Table1.1. Note that the eight switches give only five switching states and five output voltage levels are produced. The switching of each cell is conditioned by the others as following:

- An outer switch can only be turned on when the inner switch is in conduction.
- An inner switch can only be turned off when the outer switch is not in conduction.

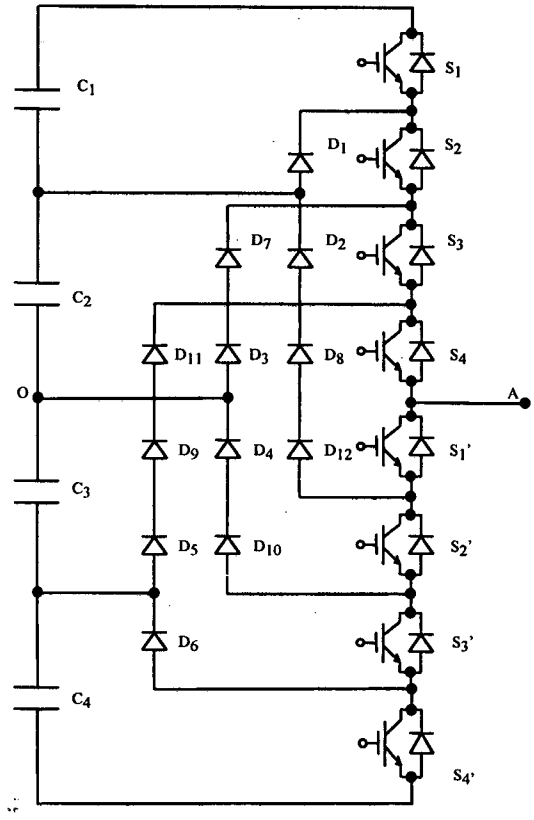


Fig. 1.3. A five level diode clamping inverter leg, consisting of (5-1) storage capacitors, (5-1)×2 switches and a total of (5-1)×(5-2) clamping diodes.

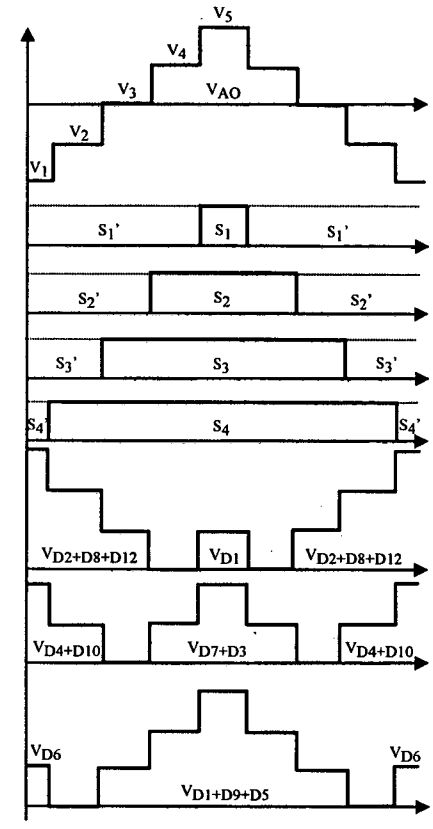


Fig. 1.4. Switching sequence with the resulting output waveform and the blocking voltages across the clamping diodes.

Table 1.1. Diode clamping five level inverter switches combinations

Output V_{AO} Levels	switches combinations							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
V_5=1/2 V_{dc}*	1	1	1	1	0	0	0	0
V_4=1/4 V_{dc}	0	1	1	1	1	0	0	0
V_3=0	0	0	1	1	1	1	0	0
V_2=-1/4 V_{dc}	0	0	0	1	1	1	1	0
V_1=-1/2 V_{dc}	0	0	0	0	1	1	1	1

* V_{dc} stands for the total DC link voltage.

1.2.2. Modulation

Fundamental-Frequency-Modulation (FFM): For large power applications where device rating is a major factor limiting the obtainable maximum power, full utilization of the

device will be interesting [14]. The FFM has been deemed the best solution in this case. Additional benefit of FFM is the low switching loss (snubber loss) and high efficiency, at the expense of slow response. Bulky filters are always used to ensure low interfacing THD.

Sub-harmonic PWM modulation: The increased power rating and improved switching performance of turn-off devices together with advanced circuit techniques have been creating increasing possibilities using PWM in high power applications. This can be found in most of the high power drive applications [20].

The idea of multilevel PWM has been well established that suits well the PWM modulation of a M-level diode clamping multilevel inverter [40]. The pattern shown in Fig. 1.5 is for the case of a five level inverter leg, where the reference signal intersects with the four carriers generating the four PWM signals for the four switching pairs. The down trace illustrates the output voltage with reference to the DC neutral potential of the leg. Several different dispositions of the carriers have been studied exhibiting different harmonic results [40]. Engineering applications of sub-harmonic PWM modulation for single phase and three phase NPC inverter have been reported [3] [41].

Space-Vector-Modulation: Space-Vector-Modulation (SVM) has been extensively reported to offer superior performance in comparison to conventional PWM techniques (natural sampling or regular sampling etc.), in terms of the reduced harmonics, optimized switching sequence and increased voltage transfer ratio [42]-[44]. It has also been a major approach to realize PWM pattern in NPC inverter [18], [45]-[47] by industry. In a complex plane, a NPC inverter can be represented by 27 switching states located at the corners of triangular patterns, among which 19 of them are independent states and the remaining 8 are redundant states, as shown in Fig. 1.6. PWM commands can be created by sampling the desired voltage vector at a constant sampling frequency, such sampling is then approximated by a sequence of three vectors defined at the corners of the sub-triangle where the desired voltage vector is located. Such approximation leads the output value to the set-point within the next sampling period.

The resultant switching sequence of SVM is essentially similar to that obtained by sub-harmonic PWM when adding a zero sequence component to the sinusoidal reference in a three phase system [48]. In principal, SVM can also be applied to a M-level (M>3) inverter. A M-level three phase system will be able to work with M^3 switching states, among which 1+3M(M-1) states are distinctive states. No engineering results have been reported.

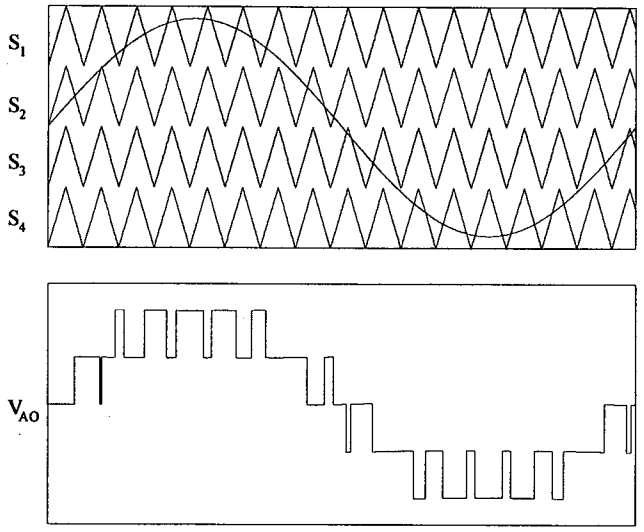


Fig. 1.5. Multilevel PWM method for a diode clamping multilevel inverter leg.

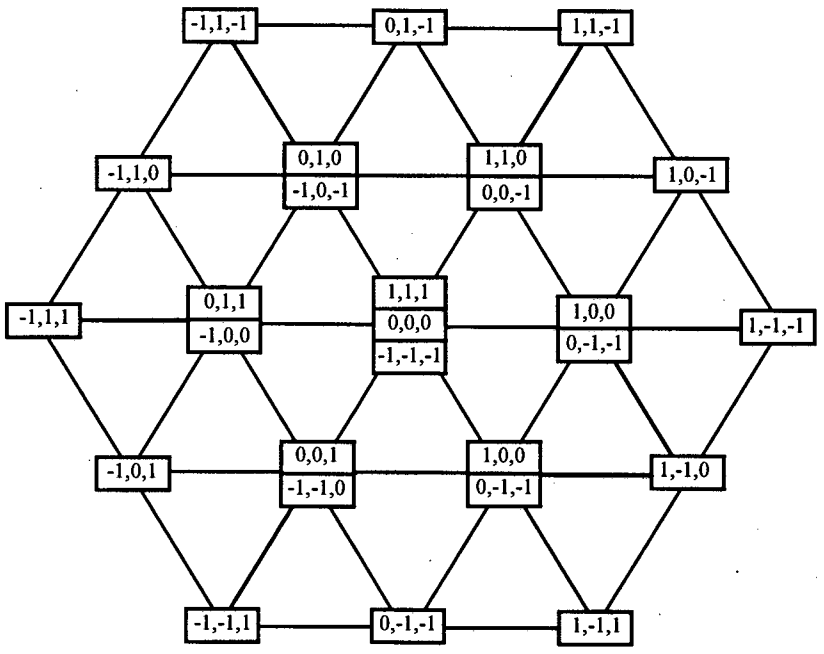


Fig. 1.6. Space vector diagram of the 27 switching states of a NPC inverter.

Closed loop modulation: In addition to the open loop schemes reviewed above, closed loop schemes like hysteresis current control [49] or delta voltage control [23] have also been investigated, which allow the generation of multilevel gating sequences inherently in the

closed loop. In particular, hysteresis current control has been used to supply high precision current for the saddle coils in plasma research [22].

1.2.3. Potential Drift and DC Supply Structures

Drift mechanism: The M-1 storage capacitors at the DC link gives M-2 floating potentials which may drift if the net average currents flowing into the given potentials are not zero. Potential drift will cause output waveform distortion and further some devices will be subjected to destructive voltage stress. For the five level case shown in Fig. 1.3, two situations can be identified [50] [51]:

- When the load current is not pure-reactive, level V_4 will decrease and level V_2 will increase. Both converge to level V_3 which keeps stable. Eventually a five level inverter will become a three level one, while the neutral potential (level V_3) doesn't drift.
- On the other hand, when the load current is pure-reactive, either lagging or leading, the net average charge flows into each level over a switching cycle is zero. Ideally all voltage levels V_2, V_3 and V_4 are always stable.

DC supply structures: To enable active power processing, the following approaches have been proposed but no engineering results have been reported.

- Use regulated DC sources in the places of the storage capacitors [52], which requires complex AC/DC circuitry.
- Use regulation circuitry to enforce the energy flow between the neighboring capacitors, which is applicable for both unidirectional or bi-directional operation [35] [53].
- Use back-to-back system where charges from both sides compensate each other [50], which is feasible only when input/output voltages are equal. Otherwise very complex control of the AC/DC converter will be required [54] [55].

Note that when pure reactive power is processed, potential drift may still happen due to unequal capacitor leakage currents, unequal device switching delays as well as asymmetrical charging during transience operation etc. Thus active control over each potential is still necessary in this case [56] [57] [58].

1.2.4. Neutral Potential Control of the NPC Inverter

Neutral potential self-balancing: When switching function of each NPC leg is quarter-wave symmetric, typically when sub-harmonic modulation is utilized, the neutral potential is

found to be self-balancing when the load is not pure reactive [59] [60]. Neutral potential deviation causes DC current component flowing in the neutral line rejecting the deviation.

However, under space vector modulation, when the two states of the middle vector are not duly distributed during the local switching cycle [45], the neutral potential will become unstable and the self-balancing property will be lost.

Neutral potential control: In the case of space vector modulation, neutral potential control can be achieved in principle by making use of the redundant states of the middle vectors in a three phase system [45]-[47], [61]-[62]. The redundant state of a middle vector tends to complement the charging/discharging flowing into the neutral potential resulted from the other state of the same vector.

Depending on the extent of asymmetry resulted mainly from different gating/switching delays, load transience, load unbalance etc. in a practical system, the need for active neutral potential control may arise even when sub-harmonic PWM modulation is used. Such control can be realized by superimposing a zero sequence DC component equally to the three phase references according to the neutral potential deviation direction as well as the system operation mode [63]-[64]. So that the net charge to the neutral potential during a third of the fundamental cycle is altered without affecting the line voltage. Note that such action of suppressing is a low frequency behavior.

1.2.5. Other Operation Problems

Cell coupling: The complex structure of the diode clamping multilevel inverter results in complex coupling among the commutating cell and the non-commutating cells through the parasitic inductances and capacitances. Refer to Fig. 1.3, when a negative current flowing through S_1', S_2', D_{10} and D_4 to the neutral potential, the turn-off of S_2' will then lead to the discharging of the parasitic capacitances of S_3' and S_4', due to the demagnetization of parasitic inductance of the neutral bus.

Indirect clamping of inner switches: Except for the two lateral switches, all the inner switches are not directly clamped. Refer to Fig. 1.3, for the switching cell of C_2, S_2 and S_2', it is S_2 in series with D_1 rather than S_2 directly that is clamped by D_3 and D_7 to the storage capacitor C_2. Similarly, it is S_2' in series with D_4, D_{10} rather than S_2' directly that is clamped by D_2, D_8 and D_{12} to C_2. Due to this indirect clamping, the discharged state will hold and

unequal blocking voltage distribution will happen. An inner switch always sees higher voltage than the outer one and the center switches will be mostly stressed.

The unequal voltage distribution is a structural shortcoming of the NPC inverter [18] [19] [65] and is common for the diode clamping family. The voltage difference between the neighboring switches is directly related to the clamping bus parasitic inductance and therefore can be minimized by introducing advanced manufacturing techniques [68]-[70].

Series connection of clamping diodes: As shown in Fig. 1.3 and Fig. 1.4 that appropriate number of fast diodes must be put in series in each clamping path to withstand the corresponding voltage stress. The diversity of the turn-on/turn-off characteristics and the stray capacitances of these fast diodes may cause dynamic voltage distribution problems. In the same sense, different blocking characteristics of these diodes may cause static voltage distribution problems. The use of grading resistance for static voltage sharing and snubbing capacitance for dynamic voltage sharing lead to lossy and voluminous solution. A new structure [37] free of this problem will be discussed in Chapter 8 of this thesis.

Snubbing difficulty: Aside from the two lateral buses, all the inner clamping buses in a M-level system (M>3) carry currents that are bidirectionally controlled which causes difficulty in offering polarized damping for turn-on snubbing reactors. Non-polarized snubber is especially inefficient [66]. Solutions to this problem must be found before GTOs can be employed in this structure for any practical applications.

1.3. Capacitor Clamping Multilevel Converter

While the NPC inverter was proposed in the late 70's, the capacitor clamping inverter was also introduced [38]. However, this technique had received little international attention until the introduction of the " Imbricated Cells" [39]. A five-level capacitor clamping inverter leg is shown here in Fig. 1.7. Similarly, this leg can be regarded as the quasi-series association of four switching cells: C_4, S_4 and S_4'; C_3, S_3 and S_3'; C_2, S_2 and S_2'; C_1, S_1 and S_1'. Besides, switches S_1, S_2, S_3 and S_4 of the up-arm and switches S_1', S_2', S_3' and S_4' of the down-arm can be regarded in quasi-series association. By timing the switching sequence of the corresponding switches in different cells, a terminal output of five level is obtained.

1.3.1. Voltage Synthesizing

In a five level diode clamping inverter leg, switching action of one switching cell is dependent on the other cells and the eight switches give only five different switching states producing five level output. However, in a capacitor clamping inverter leg, suppose that each clamping voltage is stable, the operation of each switching cell is independent of the others. From the eight switches 16 different switching states are available producing the five level output. This redundancy can be witnessed from Table 1.2.

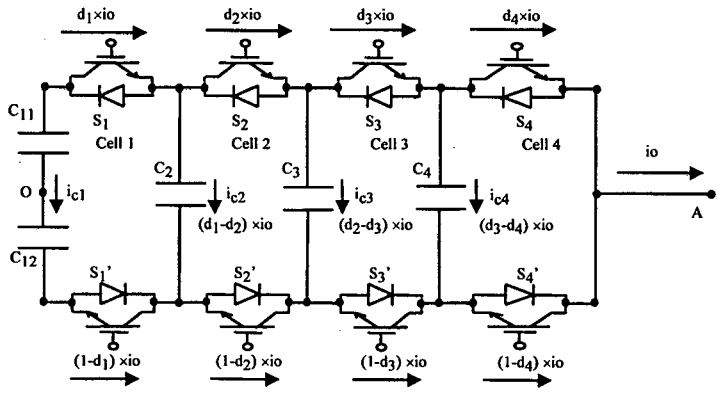


Fig. 1.7. Diagram of a capacitor clamping 5-level inverter leg consisting of (5-1)× 2 switches and (5-1) storage capacitors.

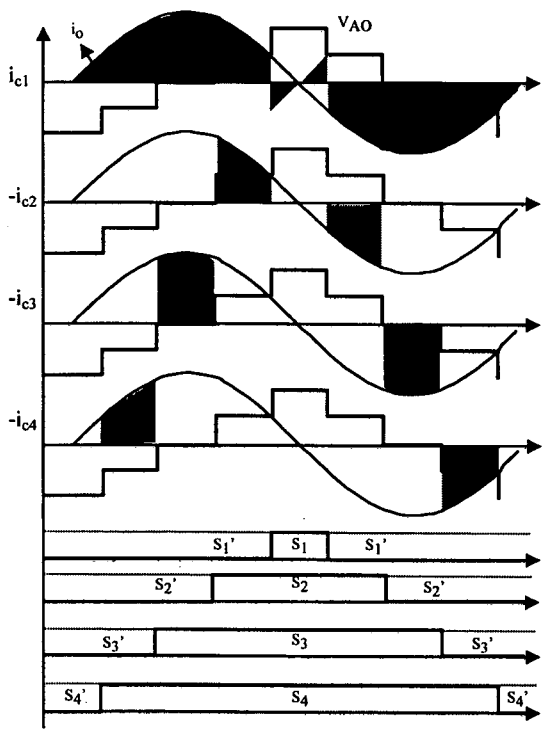


Fig. 1.8. Voltage synthesizing of the capacitor clamping five level inverter under fundamental frequency modulation.

In comparison with the diode clamping multilevel inverter where one state corresponds to one level, the multiple states for each level in capacitor clamping inverter allows performance optimization for the given criteria. Fig. 1.8 shows an illustrative voltage synthesizing under fundamental frequency modulation pattern.

Table 1.2. Capacitor clamping five level converter switches combinations

Output V_{AO}	Switches Combinations							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
1/2 V_{dc}	1	1	1	1	0	0	0	0
1/4 V_{dc}	1	1	1	0	0	0	0	1
	1	1	0	1	0	0	1	0
	1	0	1	1	0	1	0	0
	0	1	1	1	1	0	0	0
0	1	1	0	0	0	0	1	1
	1	0	1	0	0	1	0	1
	1	0	0	1	0	1	1	0
	0	1	1	0	1	0	0	1
	0	1	0	1	1	0	1	0
	0	0	1	1	1	1	0	0
-1/4 V_{dc}	1	0	0	0	0	1	1	1
	0	1	0	0	1	0	1	1
	0	0	1	0	1	1	0	1
	0	0	0	1	1	1	1	0
-1/2 V_{dc}	0	0	0	0	1	1	1	1

V_{dc} stands for the total DC link voltage.

1.3.2. Modulation

Steady state clamping voltage distribution: As shown in Fig. 1.7, when the load current during each switching cycle is supposed to be constant, the duty cycle for each cell must be set equal. Steady state voltage distribution across each capacitor is then guaranteed due to the zero average current flow through each capacitor during each switching cycle .

Output voltage harmonics: For a leg with p cells, assuming an identical duty cycle applied to each cell, a set of gating signals phase shifted by $2\pi/p$ will produce an output voltage where the harmonics up to p times of the switching frequency are zero [71].

Clamping capacitor RMS current stress [72]: When duty cycle and phase shift are both defined, the instantaneous RMS stress is dependent on duty cycle and load power factor. Maximum RMS stress happens when only reactive power is processed. Phase shift can also be optimized for RMS current stress, rather than output voltage harmonics.

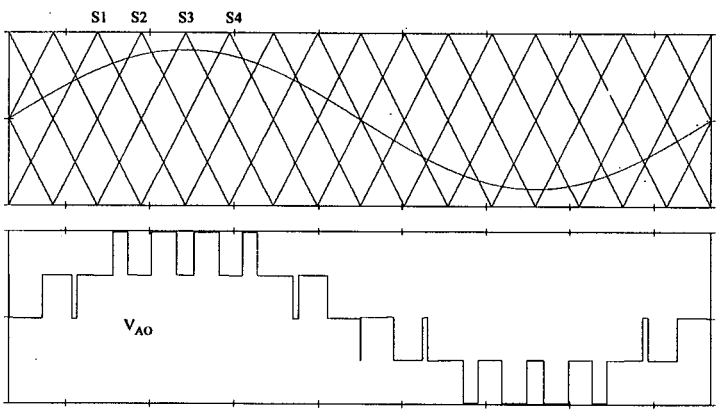


Fig. 1.9. PWM modulation pattern for five level capacitor clamping leg.

Sub-harmonic PWM modulation: Fig. 1.9 shows a typical sub-harmonic PWM modulation pattern where the phase shift has been optimized for output voltage harmonics. Four carriers phase shifted by 90 degrees are compared with a sinusoidal modulating reference producing the four gating signals for the four cells. When the modulating reference is higher than the carrier, the corresponding switch is turned on.

1.3.3. Dynamic Clamping Voltage Distribution

Success of the capacitor clamping inverter depends largely on the stability of each clamping voltage, especially during dynamics. Unequal distribution of the clamping voltage causes output distortion, and will subject the switches to destructive voltage stress.

With the modulation pattern defined in Fig. 1.9, and when the load is not pure reactive, it has been verified that each clamping voltage will tend to converge at its nominal value no matter what are the initial conditions, as a result of the self-balancing mechanism inherent with the inverter [74].

1.4. Snubbing Techniques for Multilevel Inverters

A snubber network serves such multifarious functions as to limit the device di/dt and dv/dt rates of change, to transfer the switching stress, to suppress the turn-on/turn-off spikes as well as to control the EMI, etc. For GTO, excessive voltage or current rates of change are not allowed by the device itself. When high capacity IGBT is concerned, snubbed operation is still favored [99]. Enormous energy will otherwise be accumulated during hard switching, making device derating inevitable to avoid fatal junction temperature in operation [100].

1.4.1. Dissipative/Regenerative Snubbers for Two-Level Inverters

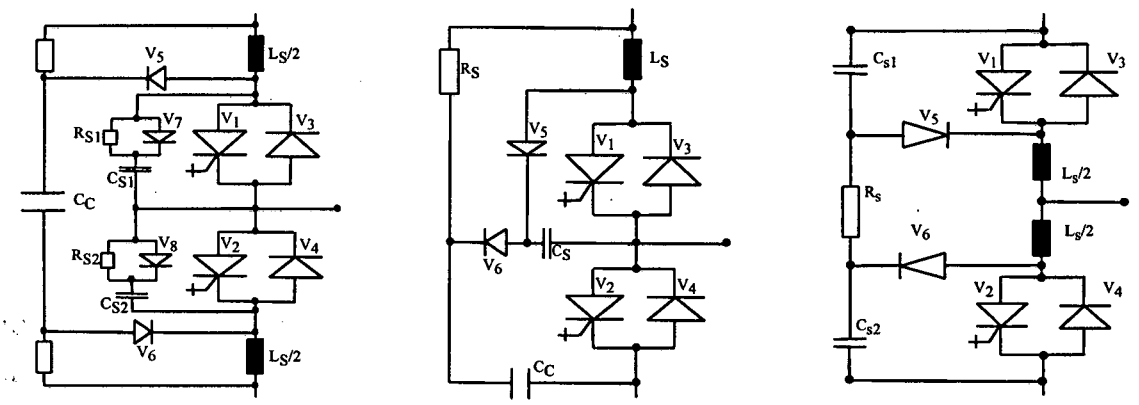
Dissipative snubbers: Dissipative snubbers can be distinguished between conventional and low-loss snubbers as summarized below. One snubber differs the other in the ways of discharging the snubber capacitor or demagnetizing the snubber inductor [75].

- *Conventional snubber:* The mostly used conventional snubber [76] [77] is shown in Fig. 1.10(a). An additional clamping capacitor ($2C_s<C_c<5C_s$) is installed for the turn-off circuitry so that to simplify the low-inductance designing task. Snubber loss is high which is the major factor limiting the switching frequency.
- *Low-loss asymmetrical snubber:* Snubber loss can be reduced by about 60% by using only one snubbing capacitor, as shown in Fig. 1.10(b) [78]-[80]. Snubbing of the down switch is achieved by a longer path including C_c, V_6 and C_s, typically $5C_s<C_c<10C_s$. The large storage capacitor suppress the voltage spikes but also necessarily increases the path inductance. An option is to use distributed capacitors for C_c. With either a clamping capacitor or a storage capacitor in the network, the switching of one inverter leg can be influenced by the other due to the coupling introduced by common inductance.
- *Low-loss symmetrical snubber*: The large clamping/storage capacitor as well as the resulted mutual coupling are absent in a symmetrical low-loss circuit, as shown in Fig. 1.10(c) [81]-[83]. The price paid for the space savings is the less tightly controlled device voltage stress, typically 1.5 times instead of 1.2 times with the asymmetrical one.

The presence of the turn-on snubber in the discharging path of the turn-off snubber makes a small resistance reasonable for R_s, typically 0.3Ω. Thus the actual snubbing capacitance is nearly doubled, depends on the impedance encountered in the current path

to the remote capacitor. Typically 1.5 times is attainable in practice. This effect reduces the local capacitor to nearly half of the value needed for the device. As a result, the snubber loss is also nearly halved.

Regenerative snubbers: Regenerative snubbers developed in the past can be broadly classified into passive recovery schemes and active recovery schemes as will be reviewed shortly below.



(a) conventional snubber (b) low-loss asymmetrical snubber (c) low-loss symmetrical snubber

Fig. 1.10. Major dissipative snubbers for two-level inverter.

- *Passive recovery schemes:* Typical passive recovery schemes have been to replace the discharging resistors in the dissipative snubbers with a coupling transformer as have been proposed in [76] [84]. The principal problem with transformer recovery is the lower efficiency and low maximum GTO switching frequency due to the core reset time limit, which is dependent on the transformer turns ratio. To avoid saturation, core reset by introducing a proper resistor in series with the transformer in order to dissipate the energy associated with the magnetizing current, or in the other instance, by opening the freewheeling path with an active switch have been studied [85] [86].

  Other schemes of this category are to replace the discharging resistors with storage capacitors which accumulate the snubber energy and will then be sent back to the load during the turn-off process, as was proposed in [87]. The additional current during turn-on together with the complexity of this circuit has been the major drawbacks of this scheme.
- *Active recovery schemes:* The general idea of a typical active recovery scheme is to replace the dissipative resistors in the dissipative snubbers with choppers which feed back the

recovered snubber energy to the DC link, as have been proposed in [88]-[89]. An example [88] is shown in Fig. 1.11, where C_3, L_c and D_1 work as an inverting step up/down chopper. A general trade-off exists in the designing among over voltage, over current of the devices and settling time of the snubber components as can be found in any other snubbers. Experiment on a 1.5MVA system proves that a open loop control of the chopper offers good dynamics. A regenerative snubber is also installed for the chopper [87]. Normally, three phases share the chopper(s).

The power rating and in-turn the complexity of the chopper is actually proportional to the inverter switching frequency. It may therefore be appropriate to state that the success of chopper recovery is limited to low frequency operation.

- *Snubber energy recovery for GTOs in series:* Series connection of GTOs are the state of the art technique for implementing large capacity utility inverters. The efficiency, however, is far lower than the conventional line commutated ones due to the snubber loss. Energy recovery becomes hence interesting. Collective [90] and individual [9] recovery schemes have been tested recently, and the latter one, as shown in Fig. 1.12, has been used in a 300MW AC/DC converter [9]. Regenerative circuit is provided for each GTO, and the recovered energy is fed back through the series connected diode rectifiers to the DC link.

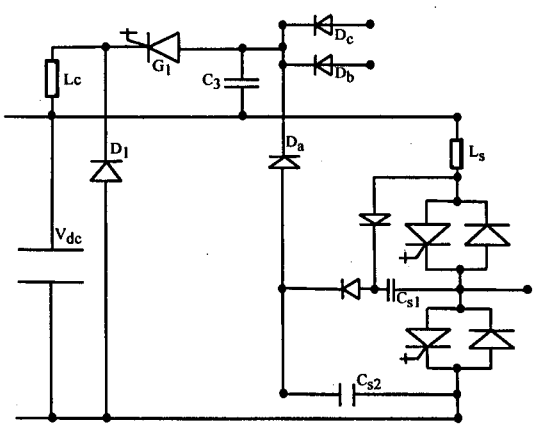


Fig. 1.11. Chopper recovery scheme for the asymmetrical low loss snubber. D_b and D_c interface the two other phases [88].

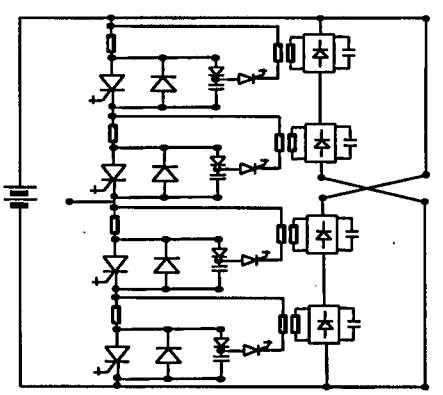


Fig. 1.12. Method of snubber energy regeneration for GTOs in series, which has been used in a 300MW AC/DC converter [9].

1.4.2. Dissipative /Regenerative Snubbers for Multilevel Inverters

As far as the snubbing of multilevel inverters are concerned, the NPC inverter has received the most attention from industry and research community. The snubbing of the

capacitor clamping inverter seems not a different issue but has not been reported yet. The following content reviews solely the existing work on NPC inverter.

Dissipative snubbers: The fact that an NPC inverter leg consists of two cells in series association simplifies the problem of snubber arrangement for it.

- *Low-loss asymmetrical snubber:* Fig. 1.13(a) shows a low-loss asymmetrical snubber for NPC inverter, which has been employed by Siemens AG in a 3MVA GTO (2.5KV, 3KA) liquid cooled 300 Hz drive system [18][19]. The two low-loss snubbers work for C_1, V_1, V_3 cell and C_2 ,V_2, V_4 cell respectively, in the same principle as in a two-level inverter. The prolonged snubbing paths for the two inner switches (V_{12}, C_{s3}, V_{22} , C_{s1} for V_3, V_{16}, and C_{s2}, V_{23}, C_{s4}, V_{13} for V_{15}, V_2) call for particular construction attention.

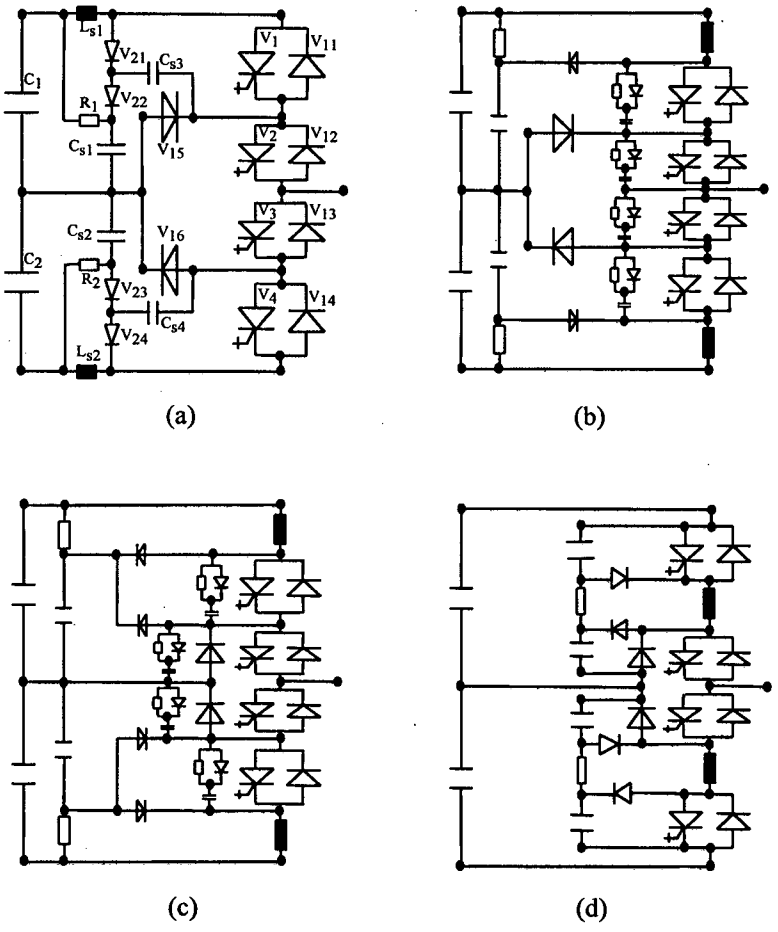


Fig. 1.13. Different dissipative snubber arrangements for NPC inverter.

- *Conventional snubbers:* Fig. 1.13(b) shows an arrangement using conventional snubber for NPC inverter which has been used for traction converters in Europe [75]. The four turn-off snubbers directly mounted for each switch may give rise to serious coupling between the

cells. Aside from the outer blocking device discharging when its neighboring inner device is turned-off, the outer blocking device can further undergo a unnecessary voltage dip (associated loss) when the other outer device is turned-off. With the modified arrangement shown in Fig. 1.13(c), the two cells are decoupled.

- *Symmetrical low-loss snubber:* As shown in Fig. 1.13(d), the symmetrical low-loss snubber can also be applied to NPC inverter working in the same way as in the two-level case [91]. Note that two-device modules are no longer applicable due to the reactor position.

Regenerative snubbers: Any dissipative snubbers that are used in NPC inverter can theoretically be modified into regenerative ones [92] [93]. A successful example has been reported recently [65] [94], by extending the idea in [89], as shown in Fig. 1.14. In this circuit, L_{s1} serves as the turn-on snubber for G_1 and G_3 while L_{s4} for G_2 and G_4. For turn-off, C_{s3} and C_{s1} for G_3 while C_{s2} and C_{s4} for G_2. L_{a3} and L_{a2} limit the turn on discharging of C_{s3} and C_{s2}. The outstanding benefit of this snubber is the recharging paths established by C_{s2} and C_{s3} for the outer switches turn-off snubbers C_{s4} and C_{s1}. The problem of indirect clamping is thus mitigated. This circuit has been used in a 10MVA back-back GTO (6-inch 6KV/6KA) system for rolling mill drives by Mitsubishi Corp. of Japan. The whole 24 GTOs share the four choppers and the reported efficiency reaches 97%.

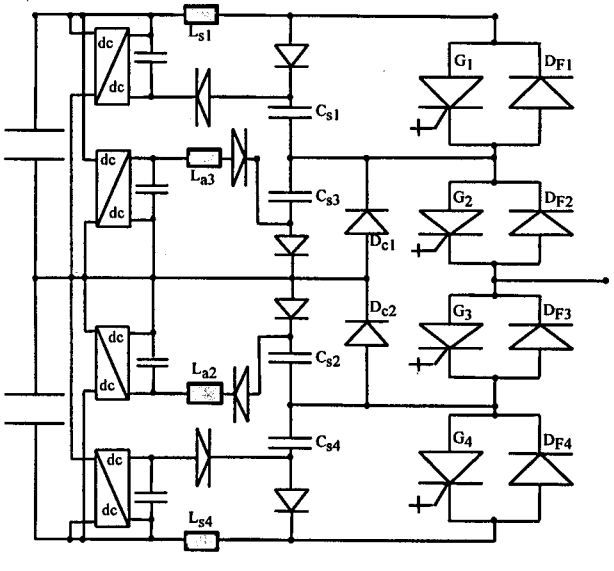


Fig. 1.14. A regenerative Snubber Circuit for NPC Inverter.

1.4.3. Snubber Problems

Snubber loss: All dissipative snubbers reviewed above consist of energy storage components, which have to be discharged or demagnetized periodically. Snubber loss of an inverter leg is given by (1.1) [75]:

$$P_S = \{\sigma \cdot \frac{1}{2} \cdot C_S \cdot V_{dc}^2 + \frac{1}{2} \cdot L_S \cdot (I_{TQ}^2 + I_{rr}^2)\} \cdot f_c \qquad (1.1)$$

where

C_S: Turn-off snubber capacitance

I_{TQ}: Actual turn-off current

I_{rr}: Free-wheeling diode reverse recovery current

V_{dc}: DC link voltage

L_s: Turn-on snubber inductance

f_c: Switching frequency

σ: Loss factor (σ=3 for the conventional snubber and σ=1 for the low loss snubbers)

The snubber loss is square proportional to the current switched and the voltage blocked, and is proportional to the frequency operated. With a low-loss snubber, it may occupy 1%-2% of the whole power installed for a 300-400 Hz system. In high power high performance applications, this large amount of heat transfer becomes highly objectionable resulting in low efficiency, limited frequency, and moreover, significant cooling and construction difficulties.

Regenerative snubber allows for improvement in efficiency. However, frequency increase will necessarily be limited by the complexity of the recovery circuits.

Voltage/current overshoots: Most snubbers, dissipative or regenerative, use a polarized series inductor for voltage transfer during turn-on, and a polarized parallel capacitor for current transfer during turn-off. The turn-on and turn-off snubbers are not independent of each other, instead, each is involved in the operation of the other.

- The energy accumulated in the series inductor during turn-on will be transferred to the parallel capacitor during turn-off in a damped resonance across the device causing voltage overshoot.
- The energy accumulated in the parallel capacitor during turn-off will be transferred to the series inductor during turn-on in another damped resonance through the device causing current overshoot.

When inductor or capacitor with higher values are used for optimizing the switching loss, the voltage/current overshoots and also the snubber loss are amplified accordingly. The result of such overshoots is the derating of the switches, typically by 40%-60% in the nominal voltage and around 20% in the nominal current depending on the thermal condition.

Turn-on and turn-off snubber interactions can be decoupled by a specific arrangement [95]-[96], as shown in Fig. 1.15. Obviously, the large electrolytic capacitors for voltage overshoot limiting lead to voluminous and expensive solution.

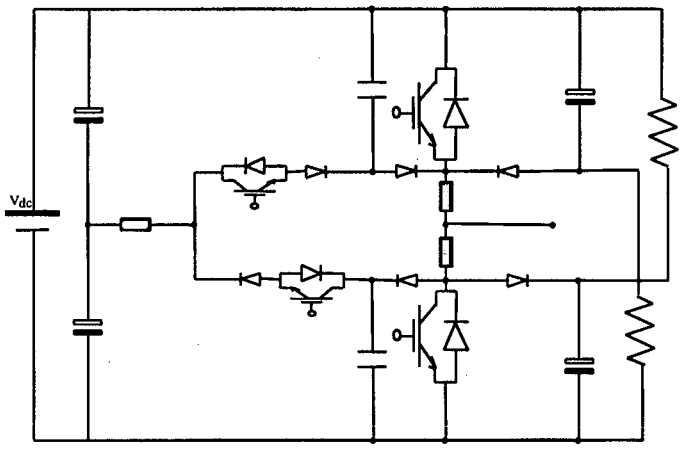


Fig. 1.15. Snubber circuit free of voltage/current overshoots across/through the main switches.

Snubbing diode issues: The need for a snubbing diode in the turn-off snubber gives rise to the following problems [98]:

- Forward recovery of the snubbing diode contributes to the first turn-off voltage spike during the rapid decreasing of the anode current, which is known as V_{DSP} for GTO.
- Additional construction inductance in the snubbing path due to the mounting of the snubbing diode causes another term to the first turn-off voltage spike.
- Reverse recovery of the snubbing diode interacts with the parasitic inductance of the discharging resistor and causes a negative voltage spike (third turn-off voltage spike).
- In the case of asymmetrical snubber, snubbing diodes in a non-commutating leg can become pre-flooded when the common potential is lifted due to the common inductance voltage stress caused by a commutating leg. The pre-flooded diodes will be subjected to very high stress if the switch is turned on at such moment [80].

Turn-on snubber loss: Turn-on snubber inductor in the power circuit is required by all snubbers, which causes considerable steady state loss.

Snubbing complexity for devices in series: Each device in a cascading string requires individual turn-off snubber [7], which is always oversized to assist equal voltage sharing. Energy recovery calls for circuitry of great complexity [9] [90].

Prolonged snubbing path in diode clamping multilevel inverter: All the switching arms, except for the up-arm of the up-most cell and the down-arm of the down-most cell, are normally composed of several switches and several diodes in series for either the forward path or the freewheeling path. The internal inductances as well as the mounting inductances of these additional switches or diodes in the forward or freewheeling path will necessarily aggravate the voltage spike problem.

Prolonged snubbing path in capacitor clamping inverter: All the switching cells, except for the inner-most one, always involve a clamping capacitor in the snubbing path. Similarly, the internal inductance as well as the mounting inductance of this clamping capacitor will add to the voltage spike problem.

1.5. Conclusions

- When adequate capacity and performance of an installation can not be fulfilled with the use of single device, associations of devices, converters and cells have been developed. The series association of cells has led to new topologies including the diode clamping multilevel inverter and the capacitor clamping multilevel inverter, both promise high voltage operation with reduced harmonics without necessitating heavy magnetics.
- Snubbed operation is needed for GTOs and is favored by high capacity IGBTs. The use of snubber leads to objectionable problems, which become more pronounced for multilevel inverters. Frequency increase with regenerative snubber is limited by the complexity of the recovery circuitry. The pursuit for an advanced solution replacing snubbers in multilevel inverters for high frequency operation constitutes the major objective of this thesis.

Chapter 2. True-PWM-Pole Two-Level Inverter

Abstract: This chapter reviews the state of the art of the soft switching inverter circuits for high power applications. The transformer connection True-PWM-Pole inverter is analyzed in details as an alternative for the Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI), results of which are verified with a 5kW half bridge prototype. Topology variations including auto-transformer and capacitor connection True-PWM-Poles are discussed.

2.1. Soft Switching Inverter Circuits Review

Switching process defines the operation condition of the device and holds essentially the most critical position in power electronics. The different switching types as well as the representative soft switching inverter circuits [101] [102] are reviewed briefly.

2.1.1. Different Types of Switching

Besides hard switching which is characteristic of turn-off with full load current and turn-on under full voltage, other three types of switching are identified as follows [102]-[104]. Typical switching waveforms are illustrated in Fig. 2. 1.

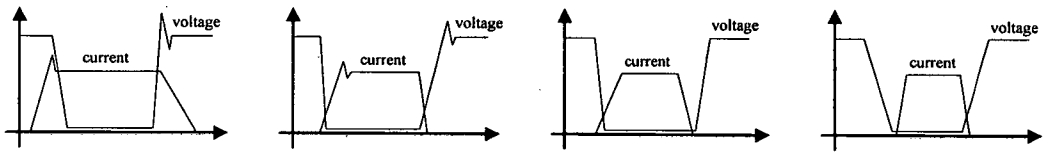
Inductive turn-on/capacitive turn-off: An inductor is in series with the device to reduce the turn-on loss while a capacitor is in parallel with the device to reduce the turn-off loss. The savings in device losses are penalized by the troubles imposed by the trapped energy in the reactive elements.

Inductive turn-on/zero current turn-off: An inductor is in series with the device to reduce the turn-on loss while the turn-off occurs at zero current with zero loss by external circuit means. Turn-off voltage spike due to the rapid voltage transition from the inductor to the device after the device turn-off and the associated loss during the device reverse recovery are characteristic of this switching type. Series inductor in the main path as well as the charge dump of the parasitic capacitance during turn-on (Power FETs) reduce the efficiency.

Capacitive turn-off /zero voltage turn-on: A capacitor is in parallel with the device to reduce the turn-off loss while the turn-on occurs at zero voltage by external circuit means. Turn-on current spike due to the rapid current transition from the capacitor to the anti-parallel

diode as well as the associated loss during diode forward recovery are characteristic of this switching type. Demagnetization of parasitic inductance during turn-off leads to voltage spike.

Logically, a forth switching type characteristic of zero voltage turn-on and zero current turn-off should exist [105]. For the case of inverter it has not yet been investigated probably due to the greater complexity and less practical interests.



(a) Hard turn-on, hard turn-off

(b) Inductive turn-on, capacitive turn-off

(c) Inductive turn-on, zero current turn-off

(d) Capacitive turn-off, zero voltage turn-on

Fig. 2.1. Switching waveforms for different switching types.

All snubbers are of the first switching type with *Inductive turn-on/capacitive turn-off.* Among the two soft switching types, the second type of switching with *inductive turn-on/zero current turn-off* has been popular with all the forced commutated thyristor circuits during the 1960s and 1970s [106]-[108], it is called today Zero-Current-Switching (ZCS) for short. For gate-controlled devices, the third switching type with *Capacitive turn-off/zero voltage turn-on* has been extensively explored and has been abbreviated as Zero-Voltage-Switching (ZVS). Recent work [109] [110] have suggested the use of the second switching type for IGBTs due to the growth in the turn-off switching loss as the junction temperature increases.

When zero voltage switching is concerned, aiding network may be configured on per-phase or per-inverter basis. Per-phase positioning yields the variant of the resonant pole inverter family, while per-inverter positioning yields the resonant link family. The resonant pole family generally has more elements but individual phase works autonomously. In comparison, the resonant link family suffers from severe coupling between phases.

2.1.2. Resonant DC Link Inverter Circuits

Perhaps the most mature circuit of this family is the Actively-Clamped-Resonant-DC - Link-Inverter (ACRLI) [111], due to its low component count and high development status, as depicted in Fig. 2.2. However, the discrete nature of the resonant DC link requires that the low frequency output voltage has to be synthesized following a Discrete-Pulse Modulation

(DPM) [112]. And a resonant link frequency that is four to six times as fast as the operating frequency of the PWM inverter is required to attain comparable load harmonics level or control bandwidth performance. DPM inverters need to compensate for the inferior resolution by imposing greater number of pulses onto the load. Presently available ACRLI inverters are rated in excess of 200 kVA with link frequency up to 70-100kHz. For inverter ratings exceeding 300 kVA, the size, cost and cooling of the resonant inductor become limiting issues [113] [114]. Main device blocking voltage is clamped to about 1.3-1.5 times the DC voltage.

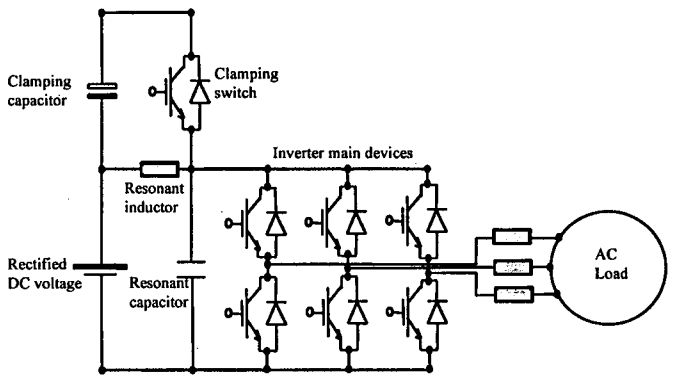


Fig. 2.2. Actively-clamped-resonant-DC-link-inverter (ACRLI).

ACRLI in PWM operation was explored [115], but was not preferred [116]. In the meanwhile, the considerable amount of PWM resonant DC link circuits [117]-[119], [146] etc. need yet to be examined further for high power applications.

2.1.3. Resonant Pole Inverter Circuits

The resonant pole family is generally realized by loading the inverter inductively at the switching frequency, regardless of the actual load current condition. A variety of circuits have been studied for this purpose during the past decade [120] [121]. Among which the Auxiliary -Resonant-Commutated-Pole-Inverter (ARCPI) [122], as shown in Fig. 2.3, has been deemed the most plausible in high power application area [123] [147], due to its small power auxiliary circuitry and full PWM capability. The phase plane of the resonance and the relevant waveforms for a switching cycle are shown in Fig. 2.4 and Fig. 2.5 respectively. The control of the ARCPI consists of these two critical issues:

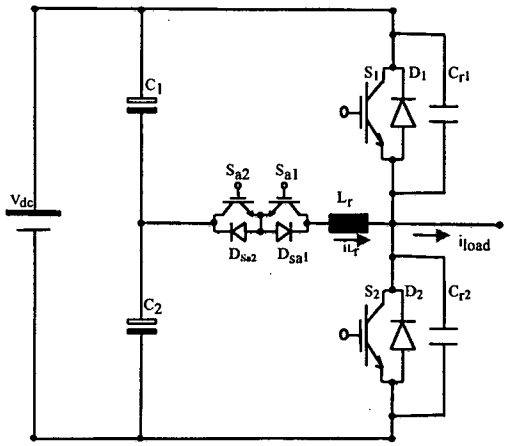


Fig. 2.3. Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI).

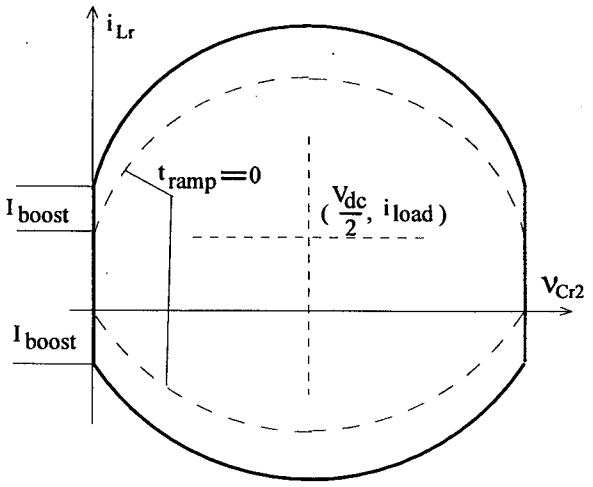


Fig. 2.4. Phase plane representation of the resonance between L_r and C_{r2} during a switching cycle.

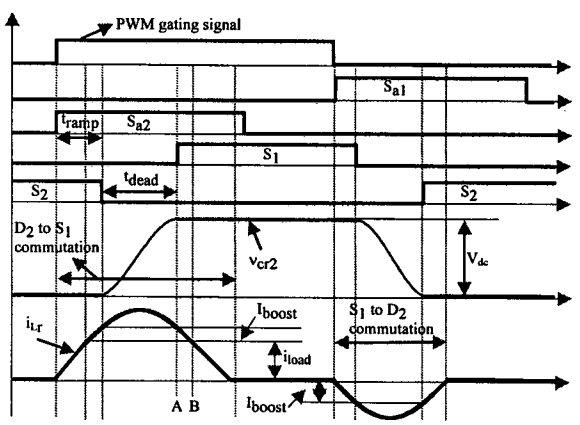


Fig. 2.5. Relevant waveforms of the ARCPI during a switching cycle.

t_{ramp} Control: For diode to switch commutation, before turning-off the triggered main switch, the corresponding auxiliary switch must be turned on in advance so that the auxiliary switch current is allowed to ramp up until the triggered main switch carries an adequate current valued at I_{boost}. Such ramp stage guarantees that the pole voltage will swing to the rail level taking into account the uncertainties especially the losses in the resonance process [81] [124]. Without this stage, resonant capacitors can not be fully charged or discharged at the end of the resonance, and considerable loss will be caused if a switching action is imposed [125].

Consequently, to maintain always an adequate level of I_{boost}, the ramp time t_{ramp} must be controlled to follow the load current. *Precise measurements of the load current as well as the*

resonant inductor current become therefore mandatory, which will increase the cost and reduce the reliability [126]. As the I_{boost} current is always small (5-10 A) and the resonant inductor current ramps up very fast, this control is hard to be implemented [127]. Diode reverse recovery current will enhance the commutation but it can not be counted on.

Zero voltage switching is further affected by the DC center tap potential. Generally, in inverter applications including motor drives, the center tap potential is self regulating at ½ V_{dc} due to the equalization of charge in and out of the respective phases as the direction of each phase current alternates between positive and negative. However, when low frequency high output current is supplied, significant drift is likely to happen during a sustained interval [128]. Hence t_{ramp} must also be controlled to compensate for this drift. Zero voltage switching will be lost if I_{boost} remains unchanged.

t_{dead} Control: As shown in Fig. 2.5, after turning-off the main switch, the opposite main switch must be turned on between instant A, where the resonant capacitor gets fully charged and the anti-parallel diode starts conducting, and instant B, where the resonant inductor current decreases to the load current level and the anti-parallel diode stops conducting, as expressed in (2.1).

$$\frac{2}{\omega_0} a\cos\left[\frac{I_{boost}Z_0}{\sqrt{(\frac{V_{dc}}{2})^2+(I_{boost}Z_0)^2}}\right] \le t_{dead} \le \frac{2}{\omega_0} a\cos\left[\frac{I_{boost}Z_0}{\sqrt{(\frac{V_{dc}}{2})^2+(I_{boost}Z_0)^2}}\right] + I_{boost}\frac{2L_r}{V_{dc}} \qquad (2.1)$$

where $\omega_0 = \frac{1}{\sqrt{2C_rL_r}}$ is the resonant frequency, $Z_0 = \sqrt{\frac{L_r}{2C_r}}$ is the resonance impedance.

From (2.1), both intervals are not related to the load current and t_{dead} can ideally be set to constant over the whole output period. However, the following uncertainties will be influential and the preset constant t_{dead} can go outside the actual range of instants A and B.

- Variation of the parasitic resistance due to heating effects.
- Variations of the input DC voltage as well as its center tap potential.

As a result, voltage status of each main switch must be supervised to secure more robust zero voltage switching without regard to any circuit parameter variations [128] [129].

Mathematical analysis for the ARCPI is given in Appendix 2.1.

2.2. True-PWM-Pole Inverter Circuit and Operation

With a view to reduce the control complexities of the ARCPI, a True-PWM-Pole inverter [130] using transformer connection, as shown in Fig. 2.6, is studied as an alternative.

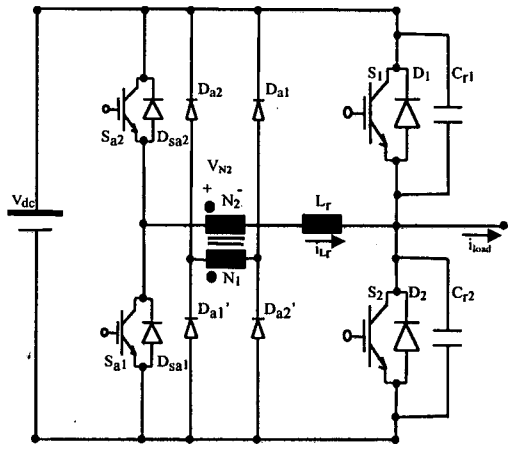


Fig. 2.6. Transformer connection True-PWM-Pole inverter scheme.

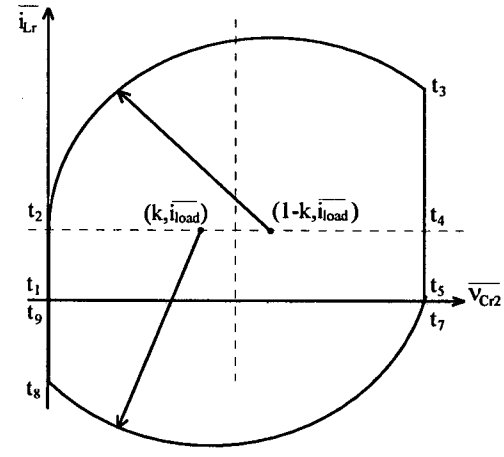


Fig. 2.7. Phase plane diagram of the resonance between L_r and C_{r2} during a switching cycle.

Prior to discussion of the commutation process, the following conditions are assumed:

- Positive load current i_{load} is flowing and remains constant during the commutation.
- Transformer ratio k is set to ensure sufficient energy for the pole voltage swinging to the rail level in the presence of commutation losses, as will be discussed in subsection 2.4.
- Construction parasitics, switching transience and transformer imperfections are neglected.
- Main switch turn-off and auxiliary switch turn-on happen at the same instant as decided by the PWM scheme, while the main switch turn-on happens until the detected voltage across the switch declining to zero. Conduction interval of the auxiliary switch is constant covering the maximum commutation duration as will be discussed in subsection 2.4.

With reference to the phase plane diagram of the resonance shown in Fig. 2.7, the relevant commutation waveforms in Fig. 2.8, and the commutation step diagrams in Fig. 2.9, the commutation of the inverter leg during one switching cycle consists of the next steps:

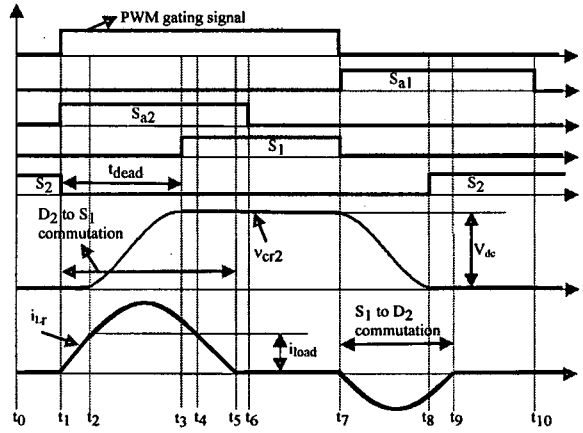


Fig. 2.8. Relevant commutation waveforms of the True-PWM-Pole inverter during a switching cycle.

Step 1 (t_0-t_1): Circuit steady state. Freewheeling diode D_2 carries the load current.

Step 2 (t_1-t_2): S_2 is turned off and S_{a2} is turned on at t_1, leading to conduction of D_{a2} and D_{a2}'. N_2 sees a positive voltage of kV_{dc} which joins the DC link voltage V_{dc} enforcing current decreasing in D_2 .

Step 3 (t_2-t_3): i_{Lr} rises to the load current level at t_2 leading to blocking of D_2. Resonance among L_r, C_{r2} and C_{r1} is initiated. C_{r2} is charged while C_{r1} discharged. Recovery current of D_2 enhances the charging current and therefore facilitates the commutation process.

Step 4 (t_3-t_4): v_{Cr2} rises to V_{dc} at t_3 leading to conduction of D_1. Then S_1 is turned on at zero voltage. Rapid current transfer from C_{r2} and C_{r1} to D_1 may cause oscillation.

Step 5 (t_4-t_5): i_{Lr} falls to load current at t_4. D_1 then stops conduction and S_1 starts carrying current.

Step 6 (t_5-t_7): i_{Lr} extinguishes at t_5 allowing for turn-off of S_{a2} at t_6. Circuit reaches another steady state. S_1 carries load current.

Step 7 (t_7-t_8): S_1 turned off and S_{a1} is turned on at t_7, which initiates a resonance between L_r and C_{r1}, C_{r2}. N_2 sees a negative voltage of kV_{dc} after turn-on of S_{a1} and conduction of D_{a1} and D_{a1}'. C_{r1} is charged and C_{r2} is discharged.

Step 8 (t_8-t_9): v_{Cr1} rises to V_{dc} at t_8 leading to conduction of D_2. Then S_2 is turned on at zero voltage. Rapid current transition from C_{r1} and C_{r2} to D_2 may cause oscillation due to stray/internal inductances of the paths .

Step 9 (t_9-t_{10}): i_{Lr} falls to zero at t_9 allowing for turn-off of S_{a1} at t_{10}. Circuit returns to the original steady state. D_2 carries load current (same to *Step 1*).

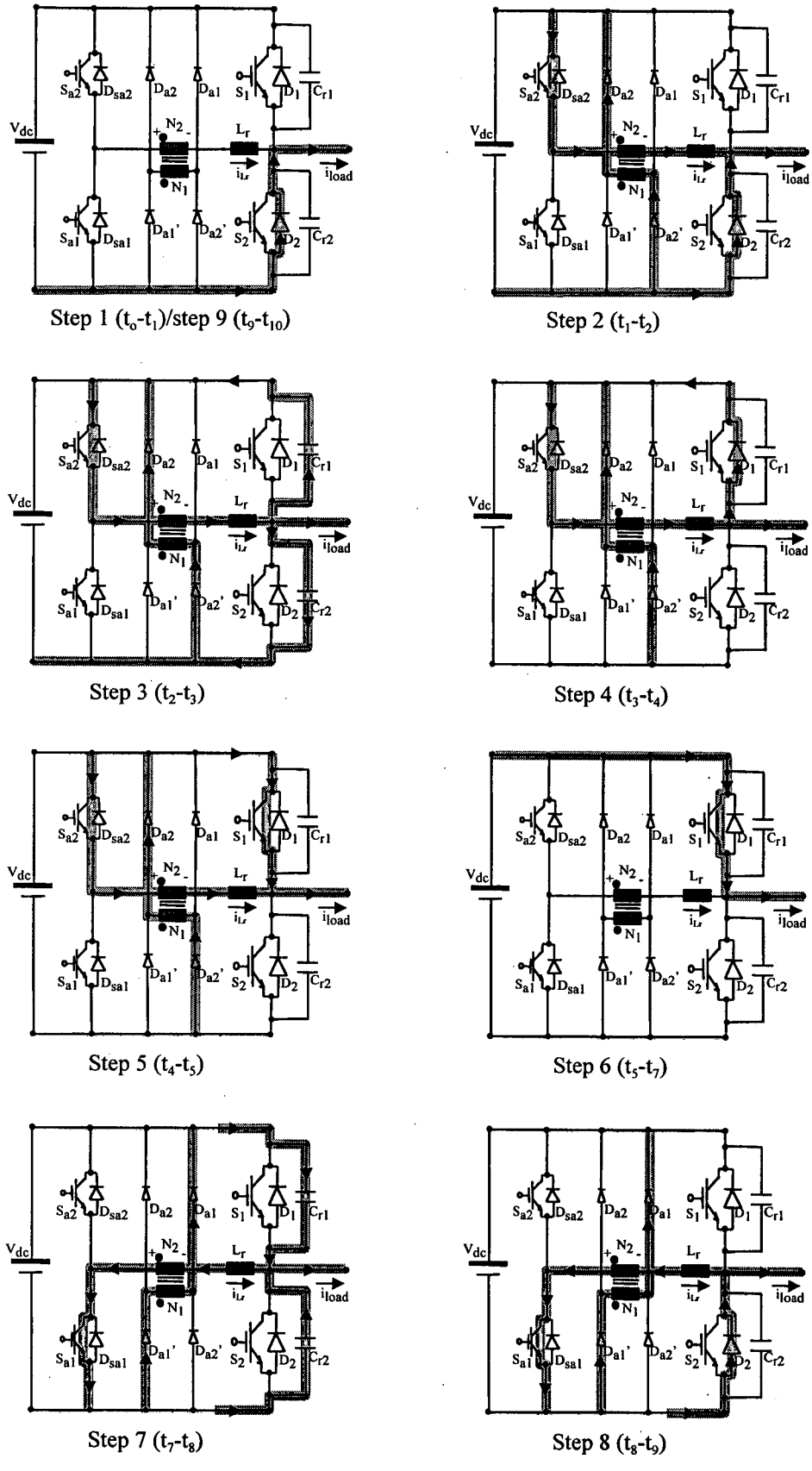


Fig. 2.9. Commutation step diagrams of the True-PWM-Pole inverter during a switching cycle.

In summary, for the True-PWM-Pole inverter circuit, the main switch works with zero voltage turn-on and capacitive turn-off, whereas the main freewheeling diode works with zero voltage turn-on and zero current turn-off. Superior to the conventional snubber, the capacitive turn-off loss of the main switch can be minimized by optimizing the resonant capacitor to this end. Meanwhile, depending on its forward recovery property, the snap-on of the main freewheeling diode does not introduce any considerable loss.

Moreover, all the auxiliary devices work with zero current turn-off. And yet voltage is only reapplied after turn-on of the opposite auxiliary switch and no voltage spike can occur. By comparison, although the auxiliary devices in the ARCPI block half the DC link voltage, they suffer from turn-off spike which calls for the use of additional snubbers [131].

Besides, despite the bridge configuration, the turn-on of the auxiliary switch is actually snubbed by the resonant inductor since the opposite freewheeling diode carries no current beforehand and its reverse recovery is negligible. Transformer excitation is reset to zero after each commutation and no magnetic accumulation can happen.

In particular, by designing the transformer ratio less than 1/2, an auxiliary voltage source valued at (1-k)V_{dc} which is higher than $V_{dc}/2$ becomes available which delivers sufficient energy for the resonant pole to swing to the rail voltage. Thus the "boost" stage and the associated control complexities with the ARCPI are no longer necessary in this case. The auxiliary switch can be simply turned on at the same instant as the main switch is turned off. Losses incurred from the extra turn-on/turn-off actions of the switch are further avoided.

2.3. True-PWM-Pole Inverter Commutation Analysis

The following assumptions are made in the analysis:

- Resonance angle frequency $\omega_0 = \frac{1}{\sqrt{2C_r L_r}}$, resonance impedance $Z_0 = \sqrt{\frac{L_r}{2C_r}}$, switching cycle T, quality factor $Q = \frac{\omega_o L_r}{R}$ is infinite neglecting losses in the resonance process.
- Unit current $\bar{i} = iZ_o / V_{dc}$, unit voltage $\bar{v} = v / V_{dc}$, unit time $\bar{t} = t\omega_0$.

2.3.1. Total Commutation Duration

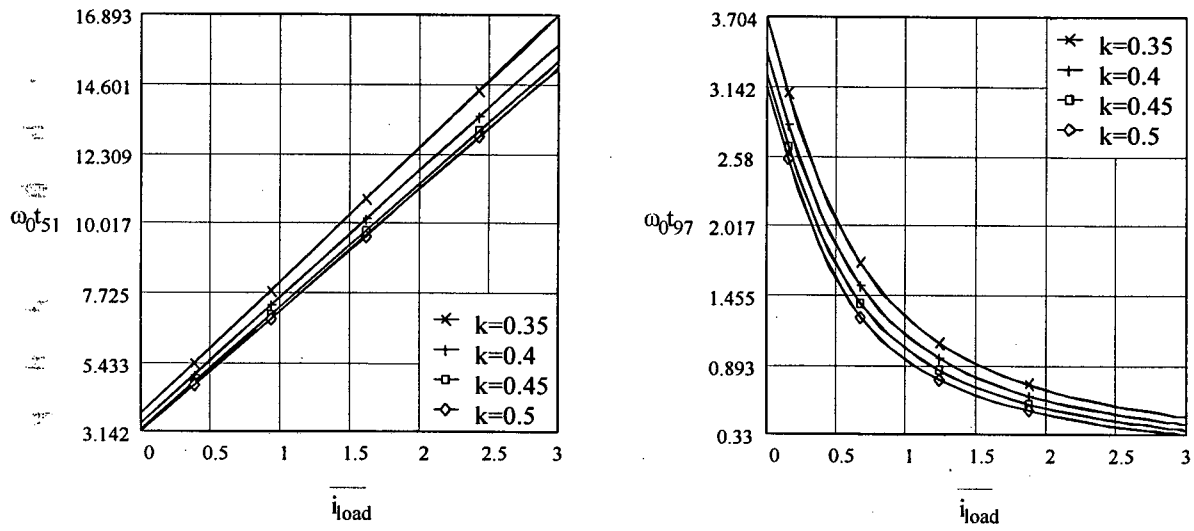
For diode to switch (D_2 to S_1) commutation, the unit value of the total commutation duration $t_{51}=t_5-t_1$ is given by (2.2):

$$\omega_o t_{51} = \frac{\overline{i_{load}}}{(1-k)} + (\pi - a\cos\frac{k}{1-k}) + \frac{\sqrt{1-2k}}{k} + \frac{\overline{i_{load}}}{k} \tag{2.2}$$

For switch to diode (S_1 to D_2) commutation, the unit value of the total duration $t_{97}=t_9-t_7$ is given by (2.3):

$$\omega_o t_{97} = \pi - a\cos\frac{k}{\sqrt{(1-k)^2+\overline{i_{load}}^2}} - a\cos\frac{(1-k)}{\sqrt{(1-k)^2+\overline{i_{load}}^2}} + \sqrt{1-2k+\overline{i_{load}}^2} - \overline{i_{load}} \tag{2.3}$$

Equations (2.2) and (2.3) are graphically shown in Fig. 2.10(a)(b).



(a) Diode to switch commutation

(b) Switch to diode commutation

Fig. 2.10. Variations of commutation durations t_{51} and t_{97} with load current and transformer ratio.

Obviously, for diode to switch commutation, the total duration increases with the load current. On the contrary, for switch to diode commutation, the total duration will decrease with the load current. Both will increase with decreased transformer ratio.

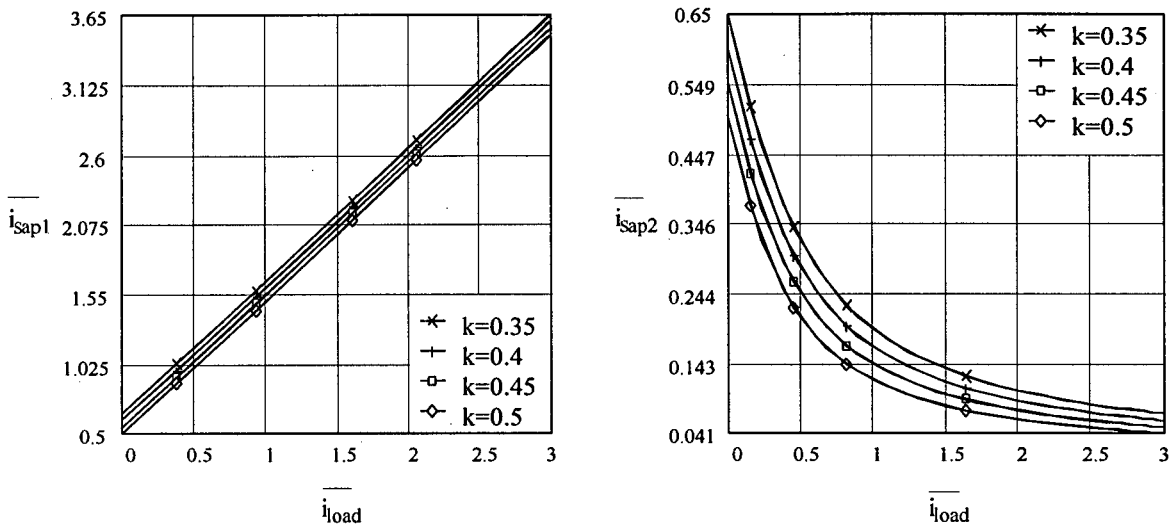
2.3.2. Auxiliary Switch Peak Current Stress

For diode to switch (D_2 to S_1) commutation, the unit value of the auxiliary switch (S_{a2}) peak current i_{sap1} can be represented by (2.4):

$$\overline{i_{sap_1}} = (\overline{i_{load}} + 1 - k) \tag{2.4}$$

For switch to diode (S_1 to D_2) commutation, the unit value of the auxiliary switch (S_{a1}) peak current i_{sap2} can be represented by (2.5):

$$\overline{i_{sap_2}} = (\sqrt{(1-k)^2 + \overline{i_{load}}^2} - \overline{i_{load}}) \tag{2.5}$$



(a) Diode to switch commutation

(b) Switch to diode commutation

Fig. 2.11. Variations of the auxiliary switch peak currents with load current and transformer ratio.

(2.4) and (2.5) are represented in Fig. 2.11(a)(b). For diode to switch commutation, the peak current of the corresponding auxiliary switch increases with the load current. For switch to diode commutation, however, it will decrease with the load current. Both will increase with reduced transformer ratio.

2.3.3. Auxiliary Switch RMS Current Stress

The resonant inductor RMS current stress over switching period resulted from diode to switch commutation $\overline{i_{Lprms}}$ can be expressed by (2.6):

$$(\overline{i_{Lrprms}})^2 = \frac{1}{T}\int_0^{L_1}[(1-k)\bar{t}]^2 d\bar{t} + \frac{1}{T}\int_0^{L_2}[\overline{i_{load}} + (1-k)\sin(\bar{t})]^2 d\bar{t} + \frac{1}{T}\int_0^{L_3}[\sqrt{1-2k} - k\bar{t}]^2 d\bar{t} \quad (2.6)$$

where:

$$L_1 = \overline{i_{load}} / (1-k)$$

$$L_2 = \pi - acos(\frac{k}{1-k})$$

$$L_3 = (\overline{i_{load}} + \sqrt{1-2k}) / k$$

Similarly, the resonant inductor RMS current resulted from switch to diode commutation $\overline{i_{Lrnrms}}$ is expressed by (2.7):

$$(\overline{i_{Lrnrms}})^2 = \frac{1}{T}\int_0^{J_1}[\overline{i_{load}} + (k-1)\sin(\bar{t}) - \overline{i_{load}}\cos(\bar{t})]^2 d\bar{t} + \frac{1}{T}\int_0^{J_2}[-\sqrt{1-2k+(\overline{i_{load}})^2} + \overline{i_{load}} + k\bar{t}]^2 d\bar{t} \quad (2.7)$$

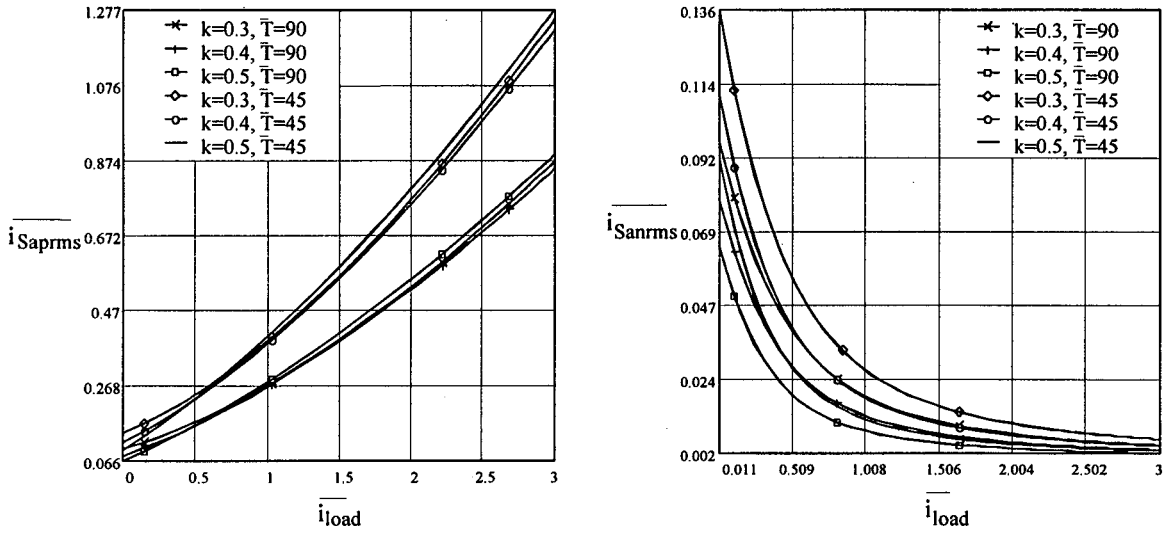
where:

$$J_1 = \pi - acos\frac{k}{\sqrt{(1-k)^2 + (\overline{i_{load}})^2}} - acos\frac{1-k}{\sqrt{(1-k)^2 + (\overline{i_{load}})^2}}$$

$$J_2 = (\sqrt{(1-k)^2 + (\overline{i_{load}})^2} - \overline{i_{load}}) / k$$

The auxiliary switch RMS current during diode to switch commutation $\overline{i_{Saprms}}$ and switch to diode commutation $\overline{i_{Sanrms}}$ are equal to $\overline{i_{Lrprms}}$ and $\overline{i_{Lrnrms}}$ respectively, which are shown in Fig. 2.12 (a)(b). The resonant inductor RMS current can then be described by (2.8):

$$\overline{i_{Lrrms}} = \sqrt{\overline{i_{Lrprms}}^2 + \overline{i_{Lrnrms}}^2} \quad (2.8)$$



(a) diode to switch commutation

(b) switch to diode commutation

Fig. 2.12. Auxiliary switch RMS currents related to the load current, transformer ratio and switching cycle.

An auxiliary switch is subject to the diode to switch commutation current or the switch to diode commutation current alternatively at the fundamental frequency in accordance with the load current direction. From Fig. 2.12, for diode to switch commutation, the auxiliary switch RMS current increases with the load current. Nevertheless, for switch to diode commutation, it will decrease with the load current. Both will increase with reduced transformer ratio or reduced switching cycle.

2.4. True-PWM-Pole Inverter Designing

2.4.1. Transformer Ratio k

When losses in the resonance process (device conduction loss, resonant inductor loss and resonant capacitor loss etc.) are considered, the actual phase plane becomes compressed, as shown in Fig. 2.13. To guarantee that the pole voltage can still reach the rail level which ensures zero voltage switching in this case, the transformer ratio k should meet (2.9):

$$V_{dc}(1-k)-\frac{V_{dc}}{2} \geq \frac{V_{dc}}{2}\frac{\pi}{4Q} \tag{2.9}$$

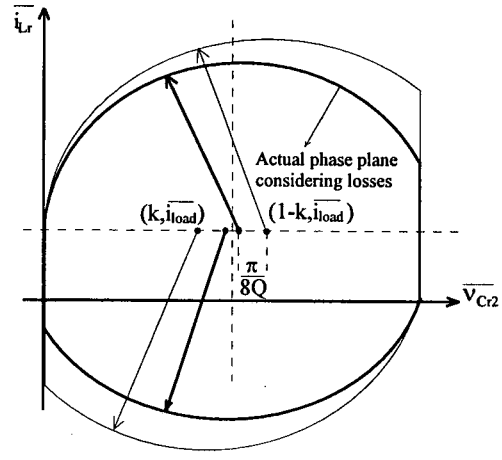


Fig. 2.13. Actual phase plane for the resonance after considering the losses in the process.

where $Q=\frac{\omega_o L_r}{R}$ and R represents the equivalent resistance in the resonance loop. Equation (2.9) can be simplified to (2.10):

$$k \leq \frac{1}{2} - \frac{\pi}{8Q} \tag{2.10}$$

When the transformer ratio is set less than ½ according to (2.10) taking into account the losses in the resonance process, zero voltage switching is then guaranteed without any additional measurements or control complexities. Such extra freedom in transformer ratio is deemed the most distinguished feature the True-PWM-Pole offers over the ARCPI.

2.4.2. Resonant Frequency ω_o

The resonant frequency should be set by optimizing the RMS current stress of the auxiliary switch according to Fig. 2.12(a) based on the switching frequency of the system.

2.4.3. Resonant Capacitor C_r and Resonant Inductor L_r

The resonant capacitance should be optimized for the main switch turn-off loss [132]. Based on the resonant frequency and the resonant capacitance, the resonant inductance is then decided.

2.4.4. Auxiliary Switch Gating Signal Width and Minimum PWM ON/OFF Time

The minimum width of the auxiliary switch gating signal must be set above the maximum value of the commutation duration, as demonstrated in Fig. 2.10(a). In the same sense, the inverter minimum PWM ON/OFF time (t_7-t_1 in Fig. 2.8) should also be set above this value.

2.4.5. Rating of the Auxiliary Switch

Due to the zero current switching in the auxiliary circuitry and due also to the high switching frequency with respect to the thermal inertia of the device, the rating of the auxiliary switch should be chosen according to its RMS stress as illustrated in Fig. 2.12(a). However, auxiliary switch peak current illustrated in Fig. 2.11(a) should not exceed the device peak output current rating, which is normally 25% higher than the device peak switching current in the case of IGBT.

Aside from the transformer ratio that is attributed to ensure zero voltage switching, designing of the resonant parameters is always a compromise among the many factors such as switching loss, device rating and duty cycle loss (DC voltage utilization) etc. Practical designing should be oriented to serve the specific designing purpose where one particular requirement may outweigh the others.

2.5. True-PWM-Pole Inverter Experimentation

A proof-of-concept 5kW IGBT half bridge inverter, as shown in Fig. 2.14, has been built modulated with normal sub-harmonic sinusoidal PWM modulation. The specifications of the prototype are shown in Table 2.1. Designing results of the resonant and transformer parameters according to sub-section 2.4 are shown in Table 2.2.

Table 2.1. Prototype specifications

DC input voltage	V_{dc}=420V	Output voltage	$V_{o.rms}$ =106V	Modulation index	M=0. 78
Output power	P_o=5kW	Load current	$I_{o.rms}$ =42.5A	Switching frequency	f_c=6.5kHz

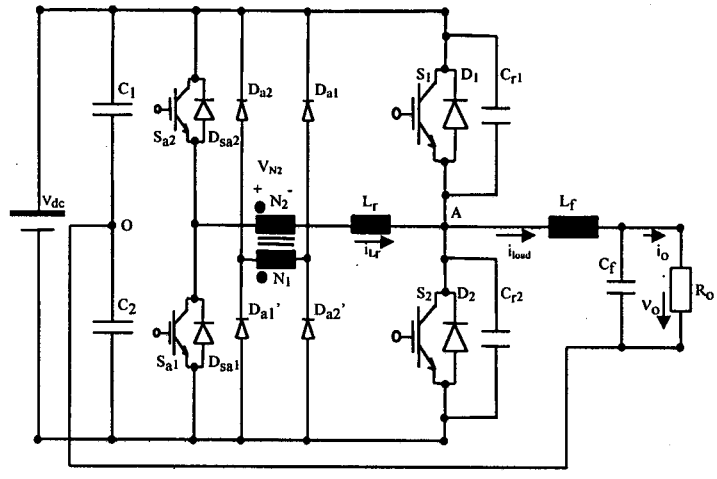


Fig. 2.14. Diagram of the 5kW IGBT half bridge inverter.

Table 2.2. Resonant and transformer designing results

Resonant capacitor	*1.* Capacitance: C_r=0.1uF, *2.* Type: low-loss polypropylene, *3.* Estimated maximum turn-off loss 4W.
Resonant inductor	*1.* Inductance: L_r=12uH, *2.* Structure: 36 turns 15AWG copper wire wound on air core bobbin, *3.* Current rate of change 20A/uS.
Auxiliary Transformer	*1.* Transformer ratio: k =0.4, *2.* Structure: Two in parallel each made up of 60 turns Litz wire (7 strands 24AWG) in the primary and 24 turns Litz wire (15 strands 24AWG) in the secondary wound on E65/29 ferrite core, *3.* Allowed equivalent resonant loop resistance around 1.95Ω.

As a result of the above designing, the resultant maximum commutation duration is 12.7uS according to Fig. 2.10(a). The maximum peak and RMS currents of the auxiliary switch are 89.5A and 21.5A respectively according to Fig. 2.11(a) and Fig. 2.12(a). Thus the auxiliary switch gating signal width is set at 14.4uS and the minimum/maximum PWM widths are set at 16.8uS and 136.8uS respectively. Dead time of 2.4uS is inserted interlocking the two main switches.

Two SEMIKRON IGBT modules (SKM50GB123D, 1200V/50A) are employed as the main and auxiliary switches, four ultra-fast HFA30TA60C (600V/30A) work as the auxiliary diodes. Two storage capacitors C_1 and C_2 each rated at 350V/3300uF form the DC center tap. A low-pass filter (L_f=1.45mH, C_f=12uF) is installed at the output.

Besides, four SEMIKRON SKH10 intelligent driver are used for driving of the main and auxiliary IGBTs. Each driver is interfaced by an external zero voltage detecting circuit to

the gate terminal of the IGBT module, which releases the gating signal when the detected voltage becomes zero. The details of which are described in Chapter 5.

Fig. 2.15 shows the output load side voltage and filter inductor current waveforms. Fig. 2.16 shows the ZVS commutation process of the main switch S_1 during switching cycle. Further in Fig. 2.17, the details of turn-on at i_{load}=56A are shown. For a predicted dv/dt of 111V/uS (averaged over t_2-t_3) and di/dt of 20A/uS, the experimental values are about 114V/uS and 18A/uS respectively. And in Fig. 2.18, the details of turn-off at i_{load}=56A are shown. For a predicted dv/dt of 307V/uS (averaged over t_7-t_8), the experimental value is about 277V/uS. The first voltage spike of about 120V appears due to the stray inductance in the turn-off snubbing path (prolonged loop for measurement objective). Fig. 2.19 shows the main switch turn-on at zero load current.

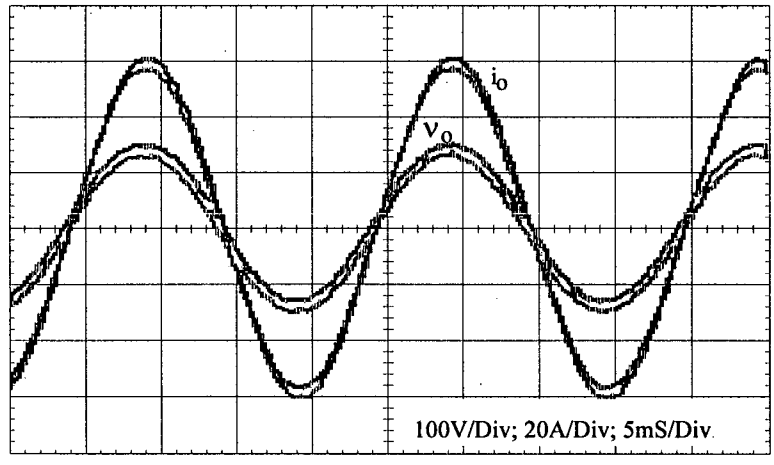


Fig. 2.15. Experimental output voltage and filter inductor current.

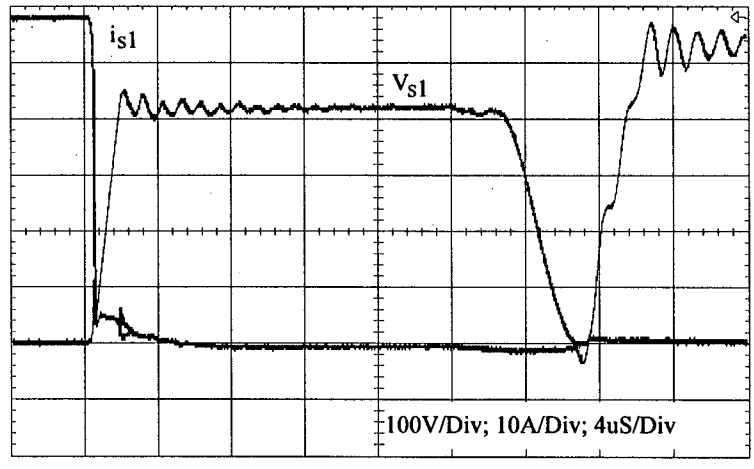


Fig. 2.16. Experimental commutation process of the main switch (S_1)

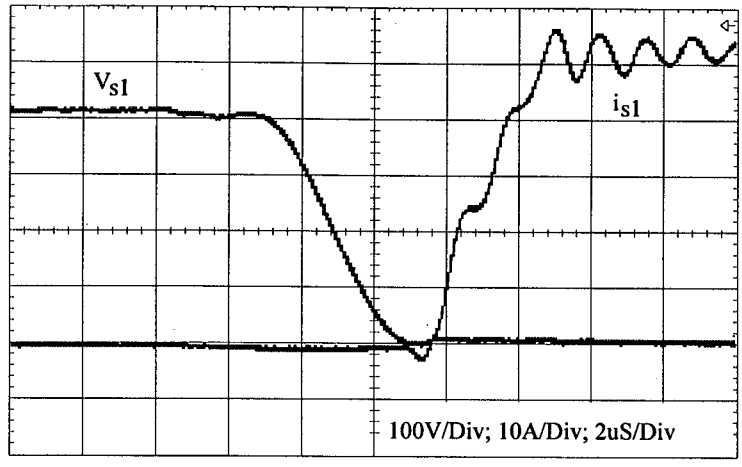


Fig. 2.17. Experimental zero voltage switching process of the main switch (S_1).

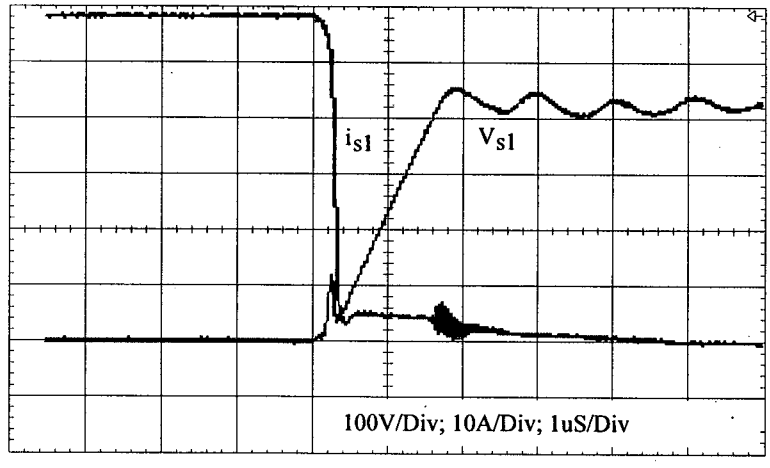


Fig. 2.18. Experimental capacitive turn-off of the main switch (S_1).

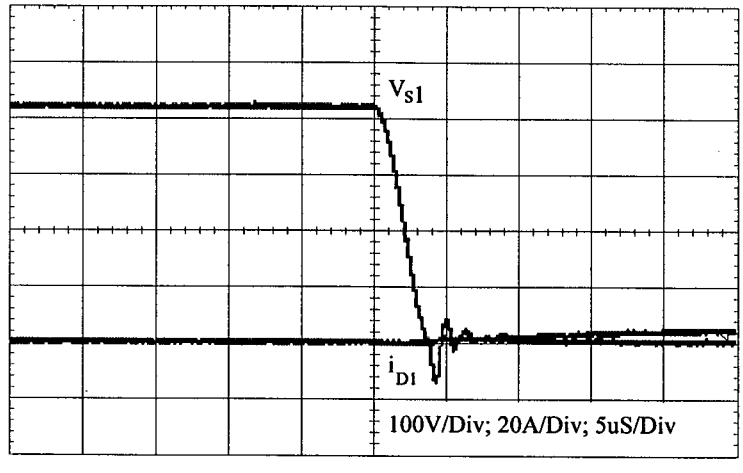


Fig. 2.19. Experimental commutation process of the main switch (S_1) at zero load current.

Fig. 2.20 shows the commutation process of the auxiliary switch (S_{a2}) at i_{load}=20A. For the predicated commutation duration of 7.2uS according to Fig. 2.10(a), and the predicted peak current of 47.8A according to Fig. 1.11(a), the experimental values are 6.7uS and 40.5A respectively. The turn-on is inductive and no reverse recovery current from the opposite diode is seen. In the meanwhile, no turn-off voltage spike is generated. The voltage protrusion afterwards occurs due to the dynamic charging/discharging of the floating middle potential of the auxiliary leg.

Fig. 2.21 shows the commutation process of the auxiliary diode at the transformer primary side. The turn-off spike suggests the introduction of simple snubbing to the diodes in practice.

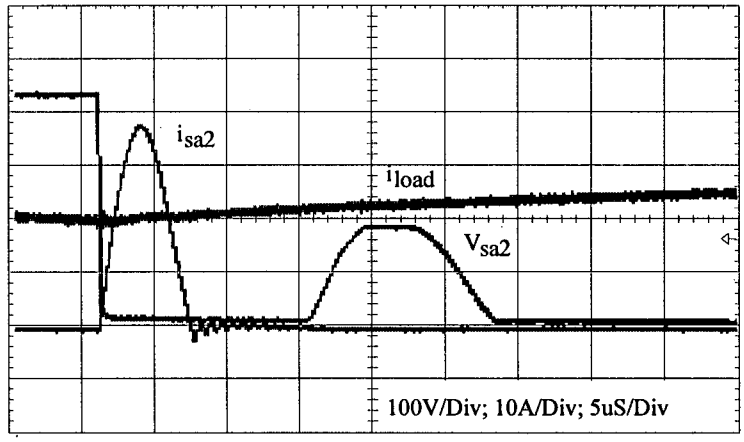


Fig. 2.20. Experimental inductive turn-on and zero current turn-off of the auxiliary switch (S_{a2}).

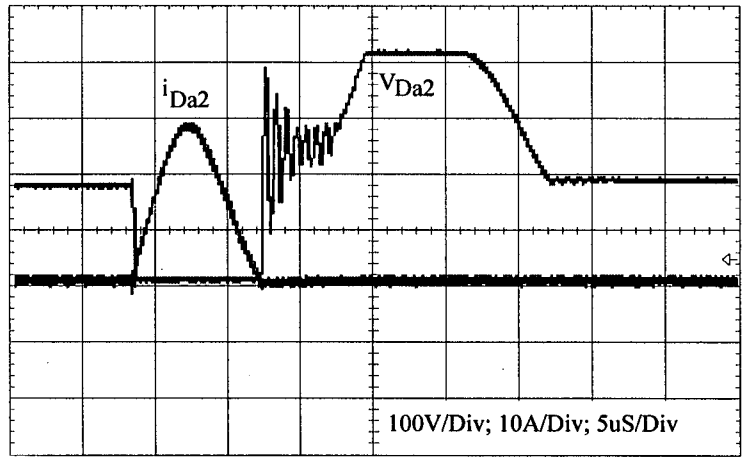


Fig. 2.21. Experimental commutation process of the auxiliary diode (D_{a2}).

Fig. 2.22 shows the resonant inductor current in relation to the load current and the main device voltage. Fig. 2.23 shows the details for switch to diode commutation at i_{load}=26A. For the predicted commutation duration of 2.25uS and the predicted peak current of 14.2A, the experimental values are about 2uS and 10A respectively. In the meantime, Fig. 2.24 shows the details for diode to switch commutation at i_{load}=18A. The experimental commutation duration and peak current are about 6.2uS and 46A, which are in accordance with the predicted values of 7.3uS and 50.8A according to Fig. 10(a) and Fig. 11(a) respectively.

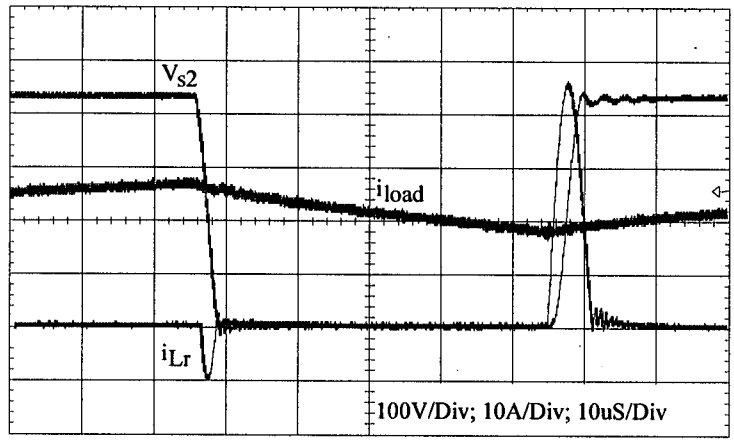


Fig. 2.22. Experimental relationship among the resonant inductor current, load current and main device voltage (S_2).

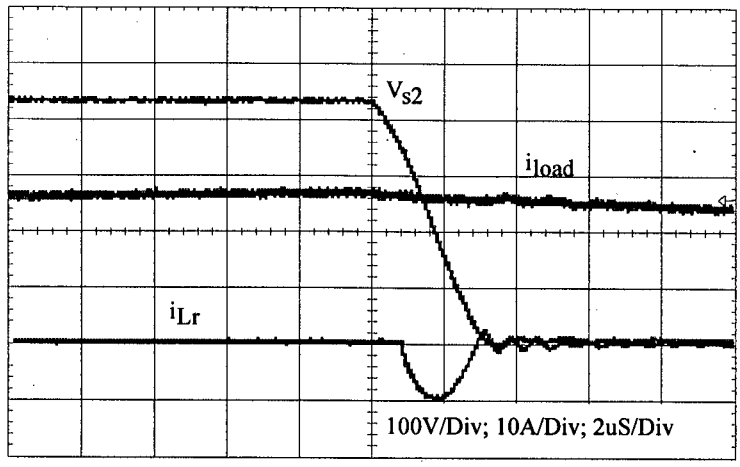


Fig. 2.23. Resonant inductor current in relation to the load current and the main device voltage (S_2) during switch to diode commutation ($S_1$to D_2).

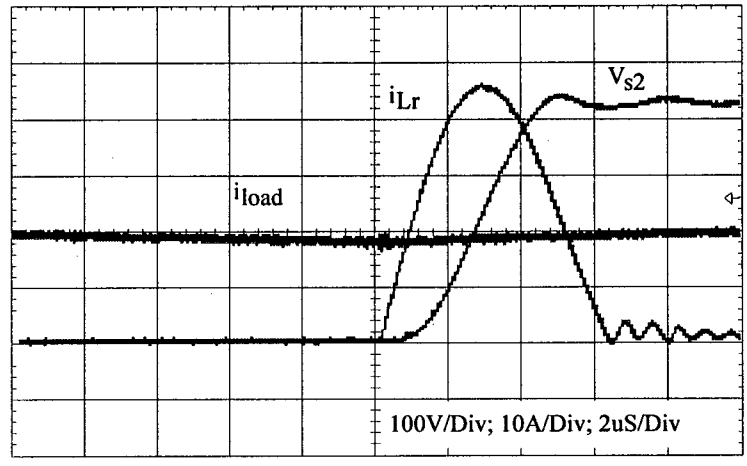


Fig. 2.24. Resonant inductor current in relation to the load current and the main device voltage (S_2) during diode to switch commutation (D_2 to S_1).

2.6. True-PWM-Pole Inverter Variations

The fundamental idea of the True-PWM-Pole inverter is to introduce a bi-directional voltage source in the resonance path which joins the DC link voltage to establish the auxiliary voltage supply for the resonance. Besides transformer, this bi-directional voltage source can also be formed by auto-transformer, or by capacitor as discussed below.

2.6.1. Normal Auto-Transformer Connections

Two auto-transformer connections [130] [133] [134] are shown in Fig. 2.25.

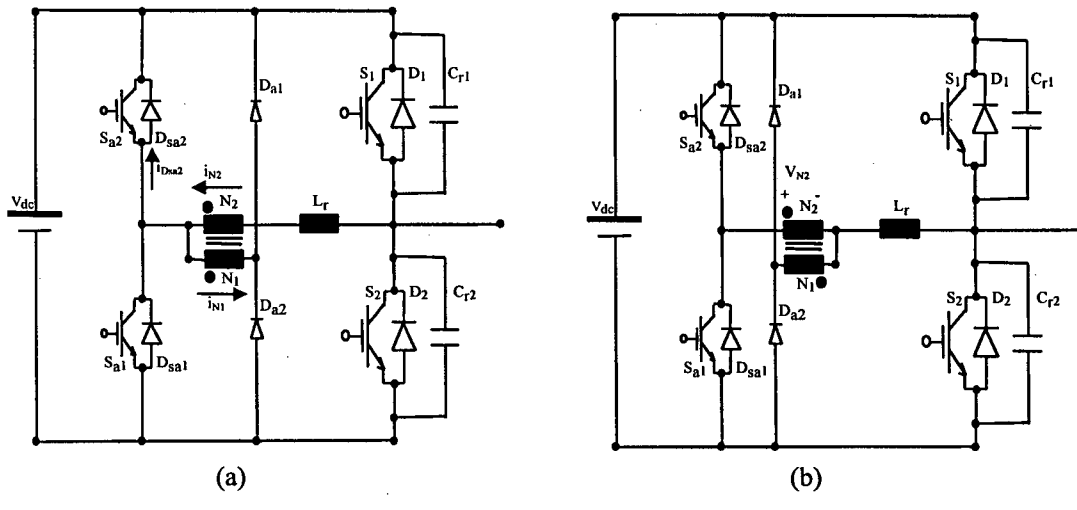


Fig. 2.25. Two variations of the True-PWM-Pole inverter with auto-transformer connection.

At the first glance, the auto-transformer connection offers attractive properties over its transformer connection counterpart. The current flowing through the auxiliary switch is now (1-k) times of that with the transformer connection, which allows for further reduction of the auxiliary switch rating. In the case of Fig. 2.25(b), the auto-transformer primary voltage rating as well as the secondary current rating are further nearly halved.

Nevertheless, auto-transformer connection causes freewheeling current flow during steady state in the auxiliary circuitry, which results in considerable steady state loss in the auxiliary circuitry. Moreover, the auxiliary switches will operate with hard switching.

Fig. 2.26 shows the relevant experimental waveforms based on Fig. 2.25(a) when D_1 to S_2 commutation happens. Due to the freewheeling current flowing through L_r, N_2 and D_{sa2} prior to the commutation (t_1), the resonant inductor current does not return to zero after the commutation (t_2). Instead, this residual current flows through L_r, N_2 and S_{a1}, causing hard switching of the auxiliary switch S_{a1} (t_3).

Upon turn-off of S_{a1},the opposite freewheeling diode D_{sa2} starts conduction, which forces the current decreasing in the resonant inductor. In the meanwhile, a voltage is reflected on the auto-transformer primary side due to the current decreasing in the secondary side, which forces D_{a2} into conduction carrying a increasing current. The two currents add to each other and the resulted net flux changes at a rate which maintains the voltages on the both sides.

The secondary current reverse direction at t_4. Afterwards, when the summing current in D_{sa2} declines to zero (t_5), both currents get equal and flow steadily through D_{a2}, N_1, N_2 and L_r until the next switching action. The auto-transformer flux can not be reset to zero.

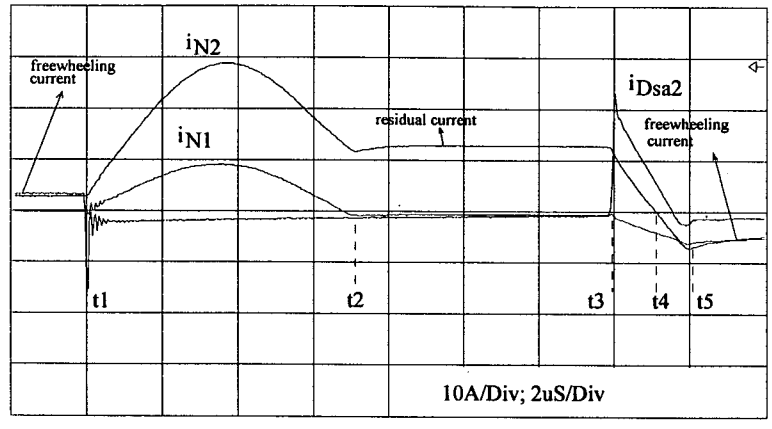


Fig. 2.26. Experimental waveforms of the currents in the two windings and the auxiliary freewheeling diode (D_{sa2}) when auto-transformer is used in the True-PWM-Pole inverter (Refer to Fig. 2.25(a)).

The current spike at t_1 indicates the reverse recovery of the freewheeling diode D_{sa2}.

Similar phenomena have also been observed for the circuit of Fig. 2.25(b). As a result, auto-transformer may be used in the True-PWM-Pole inverter only after adequate measures are taken which prevent the flowing of the freewheeling current.

2.6.2. Modified Auto-Transformer Connections

From the above analysis, the freewheeling current is resulted from the residual current and each one becomes aggravated by the other. The residual current is primitively the auto-transformer magnetizing current. Such being the case, the following measures can be taken to eliminate the freewheeling current and the residual current flowing.

1. By breaking up the freewheeling current path, which leads to the transformer connection True-PWM-Pole.
2. By de-coupling the interaction between the freewheeling current and the residual current, which can be realized by making the auxiliary switch a unidirectional one.

Based on the second measure, the four schemes shown in Fig. 2.27 are obtained. The resonant inductor current rating in the two schemes of Fig. 2.27(a)(b) is further halved. However, the equivalent resonant inductor and resonant capacitor are reduced. For the case of Fig. 2.27(a), the reduction coefficient is 1/(1+k), and for the case of Fig. 2.27(b), this coefficient is k/(1+k), which means that for a given dv/dt or di/dt, the required inductance and capacitance are increased. Moreover, the auto-transformer primary in Fig. 2.27(a) and the auto-transformer secondary in Fig. 2.27(b) now block the full DC voltage. The state equations for the commutation resonances of the two schemes are given in Appendix 2.2.

The idea of unidirectional auxiliary switch has been verified in a 5kW half bridge IGBT inverter prototype. The topology for experimentation is shown in Fig. 2.27(c), two series diodes used are APT15D60K(600V15A). Other components are the same with the transformer connection True-PWM-Pole prototype (L_r=15uH, rather than 12uH). Fig. 2.28 and Fig. 2.29 show the relevant waveforms when S_2 carries current and is turned on and off.

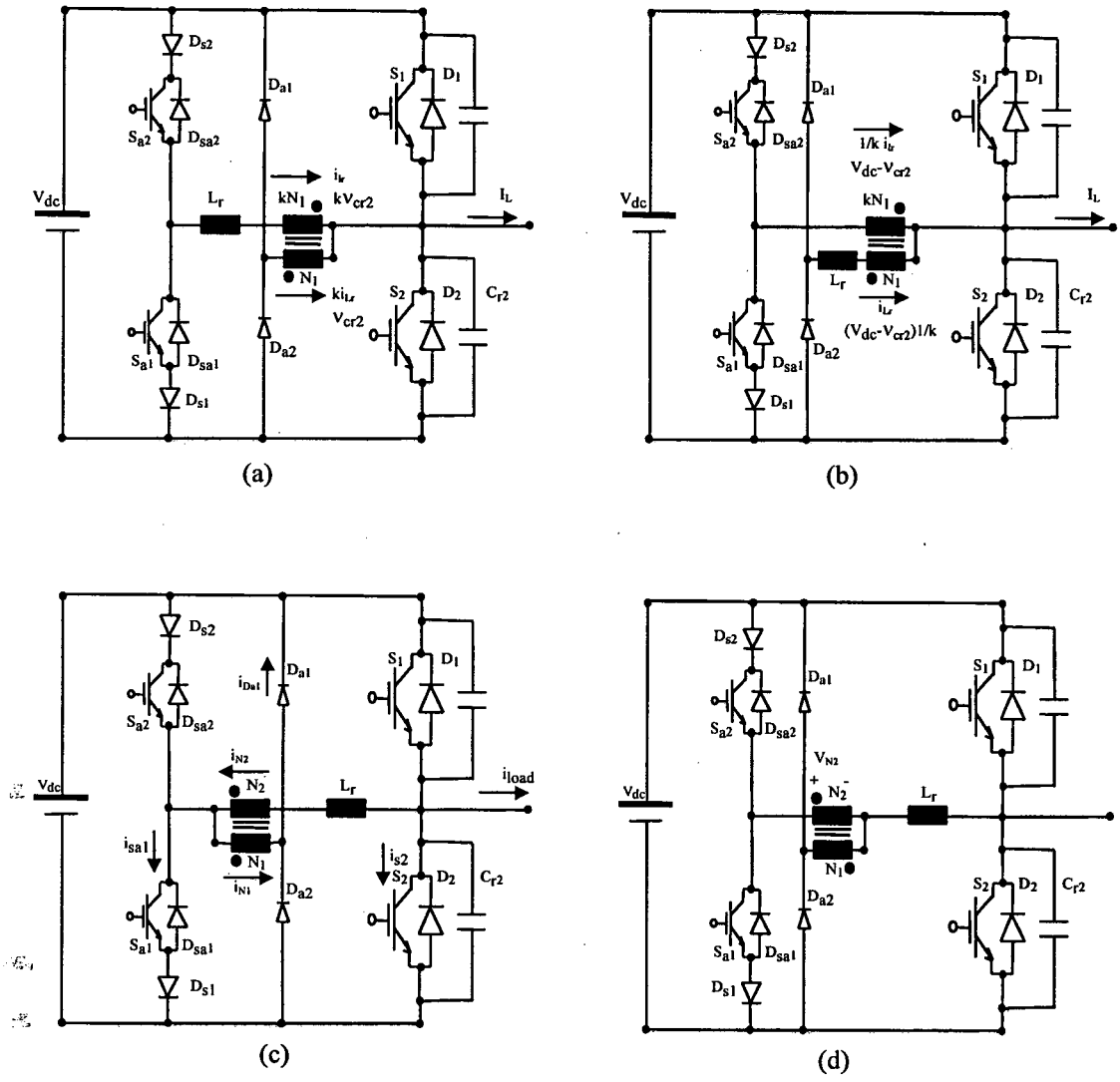


Fig. 2.27. Topology variations of the modified auto-transformer connection True-PWM-Pole.

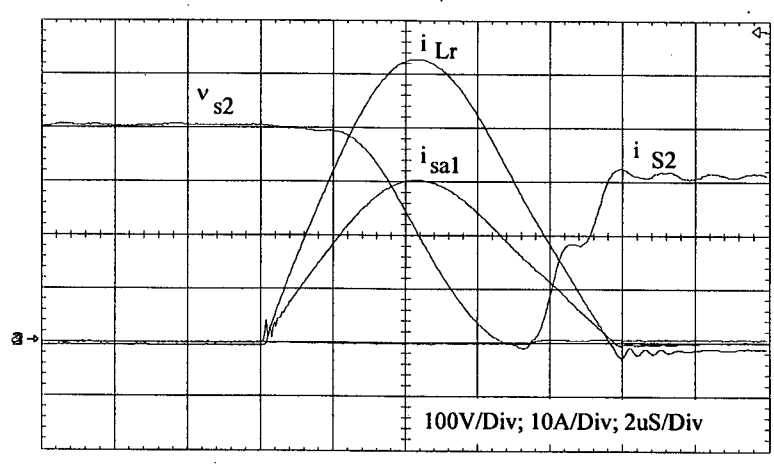


Fig. 2.28. Relevant experimental waveforms when S_2 is turned on carrying the load current.

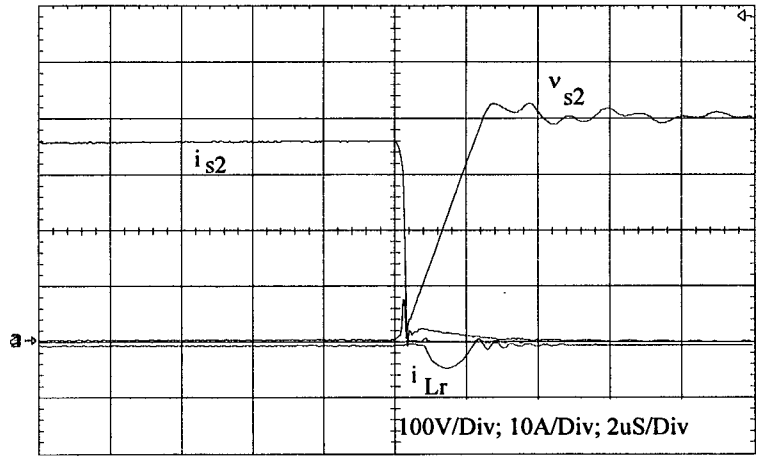


Fig. 2.29. Relevant experimental waveforms when S_2 is turned off from carrying the load current.

The relevant auxiliary switch commutation waveforms are shown in Fig. 2.30. Obviously, the auxiliary switch turns on and off at zero current. However, a reverse voltage spike appears across the series diode right after the resonant current is reset to zero. The reverse voltage spike is resulted from the interaction among the stray capacitances of the auxiliary devices and the resonant inductance, forced by the auto-transformer secondary voltage which does not reset instantly. The details of the reverse voltage spike is shown in Fig. 2.31. This spike can be suppressed by a simple RCD snubber across the series diode.

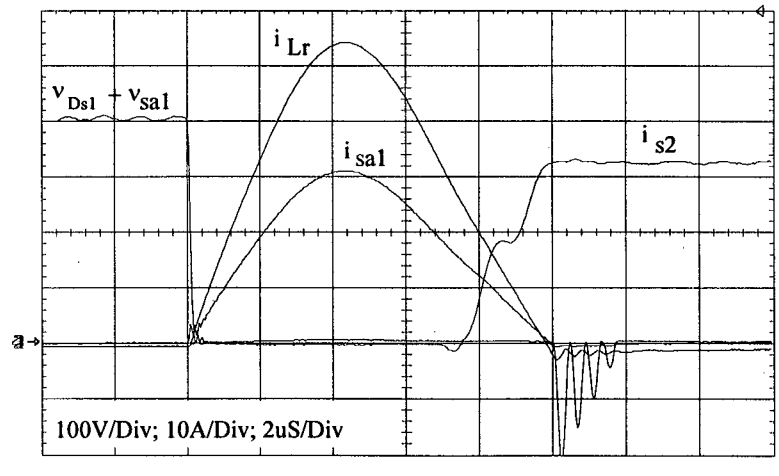


Fig. 2.30. Relevant experimental auxiliary switch S_{a1} waveforms when S_2 is turned on carrying the load current.

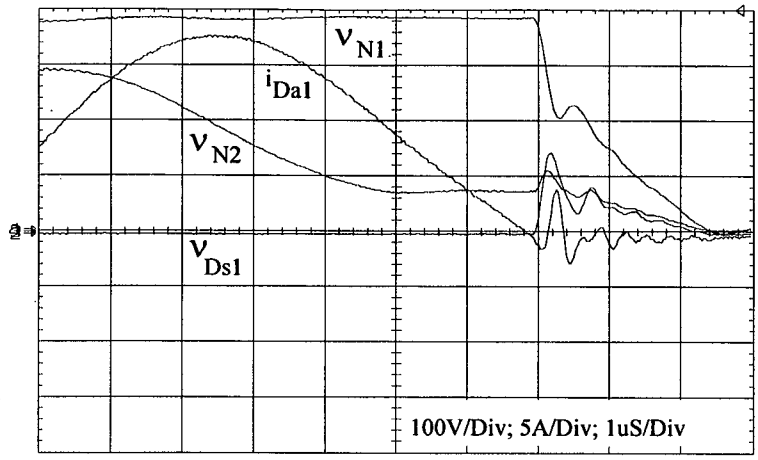


Fig. 2.31. Experimental details of the reverse voltage spike resulted from the auxiliary switch S_{a1} turn-off during D_1 to S_2 commutation.

When the modified auto-transformer connection circuits are compared with the transformer connection circuit, the auxiliary switch current stress is nearly halved while an extra simple RCD snubber is needed for the series diode. Other benefits including the auto-transformer voltage/current stress reduction or the resonant inductor current stress reduction are possible with its variations, which are also tested in the laboratory.

2.6.3. Capacitor Connection

Capacitor can be used in the place of the transformer or auto-transformer to attain a True-PWM-Pole inverter, as shown in Fig. 2.32. This circuit resembles the traditional series current commutation circuit [108], which has recently been considered for use in the boost converter with turn-off device [135].

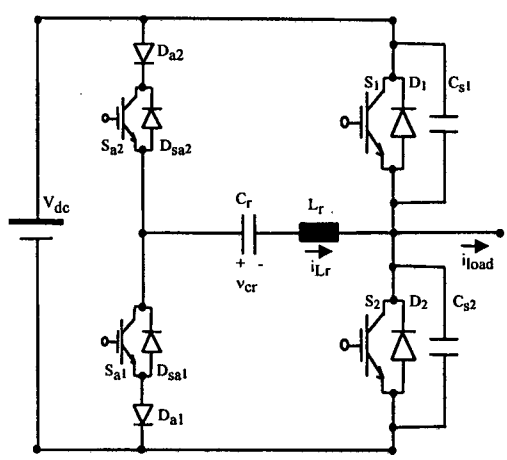


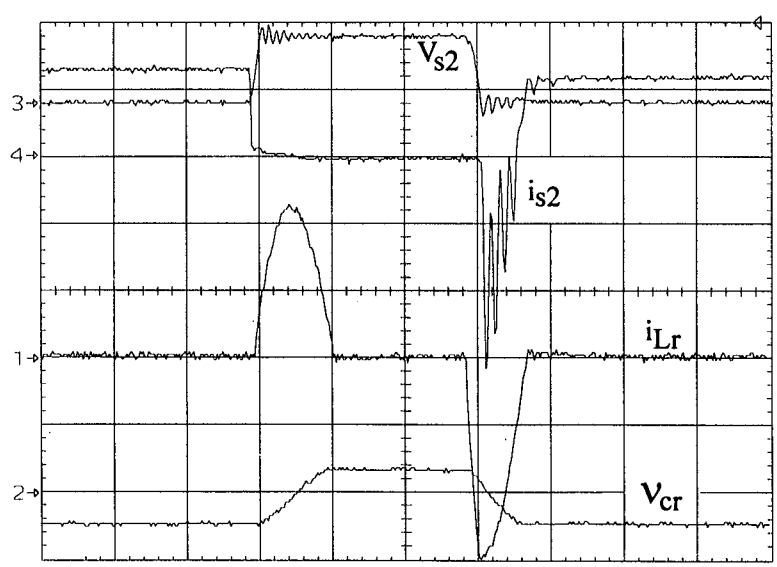
Fig. 2.32. New True-PWM-Pole inverter with capacitor replacing the transformer or auto-transformer.

Control and operation sequence of this new pole inverter are all the same with the transformer connection True-PWM-Pole. Fig. 2.33 (a)(b) show the experimental turn-on and turn-off processes of S_2 when the load current is carried by S_2 and D_2 respectively.

Similar to the transformer or auto-transformer connections where the secondary voltage alternates direction naturally after each commutation, the capacitor voltage in this case changes its direction after each commutation as a result of the charging/discharging by the resonant current. However, the capacitor voltage always adds to the DC link voltage forcing the resonance, rather than subtracts from, like the transformer connection, which leads to more than sufficient resonant current. In Fig. 2.34, the experimental capacitor (v_{cr}) voltage in relation to the load current under the given circuit parameters is illustrated. The key issue in designing of this inverter is to find the capacitance for C_r which is a compromise among resonant current, capacitor (C_r) voltage and commutation duration. Certain loss must be assumed in the resonant loop to avoid iterative capacitor voltage increment, as is the McMurray inverter [107].

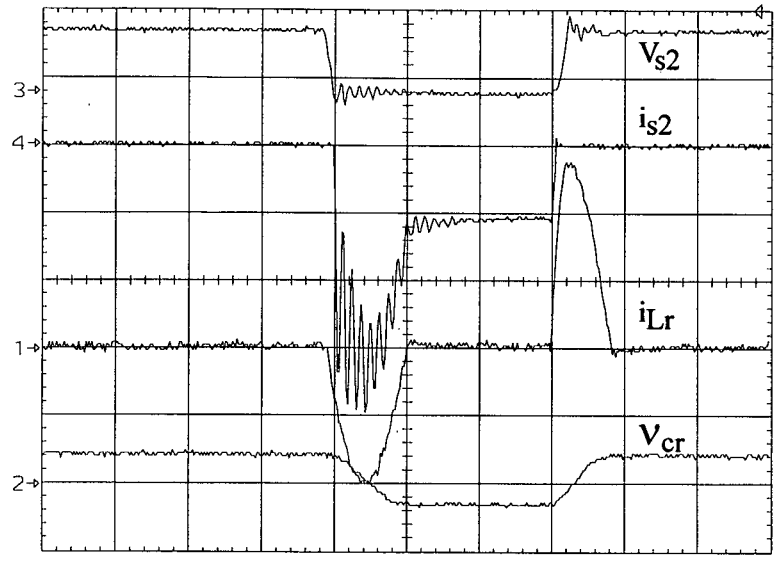
When this circuit is compared with the transformer connection True-PWM-Pole inverter, the troubles associated with magnetics (manufacturing labor, loss etc.) are avoided, at the expense of the fairly pronounced resonant current. Both ensure zero voltage switching in the main circuit and zero current switching in the auxiliary circuit without any extra measuring or controlling.

Mathematical analysis of the commutation resonance is given in Appendix 2.3.



100V/Div; 10A/Div; 10uS/Div

(a) commutation processes when S_2 carries current



100V/Div; 10A/Div; 10uS/Div

(b) commutation processes when D_2 carries current

Fig. 2.33. Experimental S_2 commutation processes when S_2 or D_2 carries current.

(C_{s1}=C_{s2}=0.1uF, L_r=7.5uH, C_r=2uF)

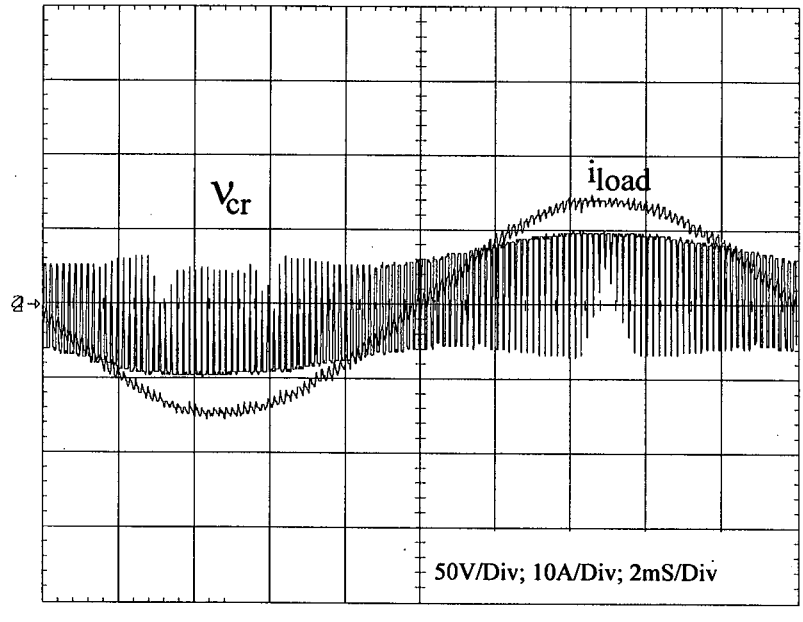


Fig. 2.34. Experimental capacitor (C_s) voltage related to the load current.

(C_{s1}=C_{s2}=0.1uF, L_r=7.5uH, C_r=2uF)

2.7. Conclusions

- Resonant pole inverter solves the problems of the conventional snubber associated with snubber interaction, series inductor and snubbing diode etc. The auxiliary circuitry works with simultaneous zero current switching, which is a significant advantage over the regenerative snubber.
- Transformer connection True-PWM-Pole inverter avoids the control complexities of the ARCPI, while zero voltage switching for the main switch and zero current switching for the auxiliary switch are always guaranteed. The auxiliary switch current stress is comparable to the ARCPI circuit while its voltage stress is clamped to the DC rail voltage. Experimental results from a 5kW half bridge prototype agrees well with the analysis.
- The normal True-PWM-Pole inverter suffers from such problems as freewheeling current and residual current in the auxiliary circuit, primitively due to the magnetizing current of the auto-transformer, which renders this scheme not practically applicable. Experimental results showing the problems of this structure are explained.
- The modified auto-transformer connection True-PWM-Pole inverter solves the above problems by introducing a diode in series with each auxiliary switch. The auxiliary switch current stress is halved in the modified auto-transformer connection True-PWM-Pole circuits. Further reduction of the auto-transformer voltage/current rating or the resonant inductor current rating are possible with its variations. Also, experimental results from a 5kW prototype verifies these solutions.

Appendix 2.1. Mathematical analysis of the ARCPI

Refer to Fig. 2.3, Fig. 2.4 and Fig. 2.5, the commutation duration, peak current stress and quasi-rms current stress (over switching cycle) can be mathematically analyzed. The base values used are: unit current $\bar{i} = iZ_o / V_{dc}$, unit voltage $\bar{v} = v / V_{dc}$, unit time $\bar{t} = t\omega_0$. Throughout the analyses, the unit value of I_{boost} current is assumed to be 20%.

1. Total commutation duration

For diode to switch commutation, the total commutation duration is given by (2.1A):

$$\overline{t_{ds}} = 2a\cos\frac{\overline{i_{boost}}}{\sqrt{\frac{1}{4}+\overline{i_{boost}}^2}} + 4[\overline{i_{load}} + \overline{i_{boost}}] \tag{2.1A}$$

For switch to diode commutation, the total commutation duration is given by (2.2A):

$$\overline{t_{sd}} = 2a\cos\frac{\overline{i_{boost}} + \overline{i_{load}}}{\sqrt{\frac{1}{4}+[\overline{i_{boost}} + \overline{i_{load}}]^2}} + 4\overline{i_{boost}} \tag{2.2A}$$

(2.1A) and (2.2A) are represented in Fig. 2.1A.

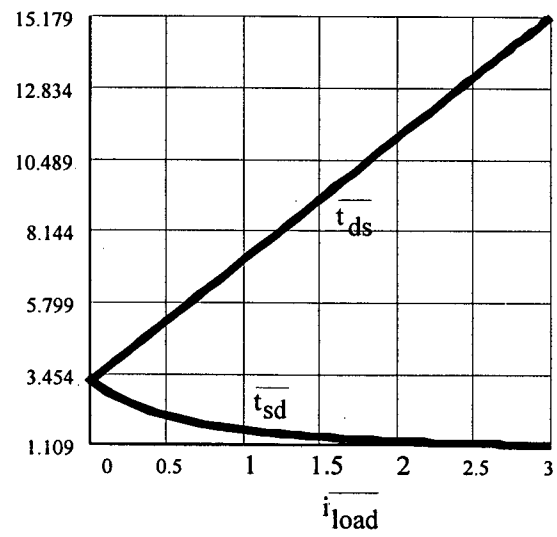


Fig. 2.1A. Total commutation durations versus load current for diode to switch commutation and switch to diode commutation.

2. Auxiliary device peak current stress

For diode to switch commutation, the auxiliary switch peak current is given by (2.3A):

$$\overline{i_{sap1}} = \overline{i_{load}} + \sqrt{\frac{1}{4} + \overline{i_{boost}}^2} \tag{2.3A}$$

For switch to diode commutation, the auxiliary switch peak current is given by (2.4A):

$$\overline{i_{sap2}} = -\overline{i_{load}} + \sqrt{\frac{1}{4} + (\overline{i_{boost}} + \overline{i_{load}})^2} \tag{2.4A}$$

(2.3A) and (2.4A) are represented in Fig. 2.2A.

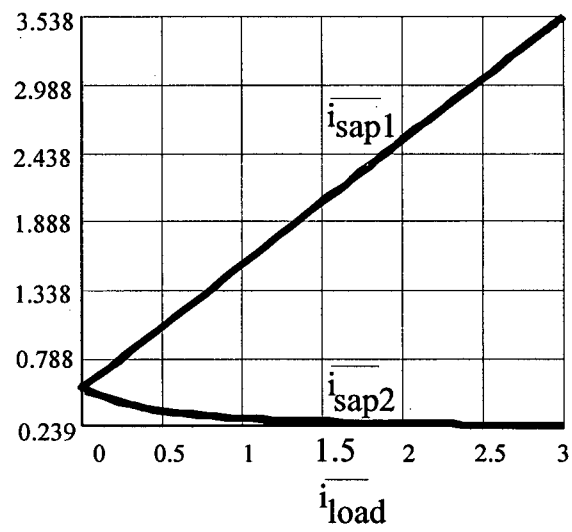


Fig. 2.2A. Auxiliary switch peak currents versus load current for diode to switch commutation and switch to diode commutation.

3. Auxiliary switch RMS current stress

For diode to switch commutation, the auxiliary switch RMS current is given by (2.5A):

$$\overline{i_{saprms}} = \sqrt{\frac{2}{\bar{T}} \int_0^{2(\overline{i_{load}} + \overline{i_{boost}})} \frac{1}{4}\bar{t}^2 d\bar{t} + \frac{1}{\bar{T}} \int_0^{2a\cos\frac{\overline{i_{boost}}}{\sqrt{\frac{1}{4}+\overline{i_{boost}}^2}}} (\overline{i_{load}} + \frac{1}{2}\sin\bar{t} + \overline{i_{boost}}\cos\bar{t})d\bar{t}} \tag{2.5A}$$

For switch to diode commutation, the auxiliary switch RMS current is given by (2.6A):

$$\overline{i_{sanrms}} = \sqrt{\frac{2}{\overline{T}}\int_0^{2\overline{i_{boost}}} \frac{1}{4}\bar{t}^2 d\bar{t} + \frac{1}{\overline{T}}\int_0^{2a\cos\frac{\overline{i_{boost}}+\overline{i_{load}}}{\sqrt{\frac{1}{4}+(\overline{i_{boost}}+\overline{i_{load}})^2}}} (\overline{i_{load}} - \frac{1}{2}\sin\bar{t} - (\overline{i_{load}} + \overline{i_{boost}})\cos\bar{t})d\bar{t}}$$

(2.6A)

(2.5A) (2.6A) are represented in Fig. 2.3A.

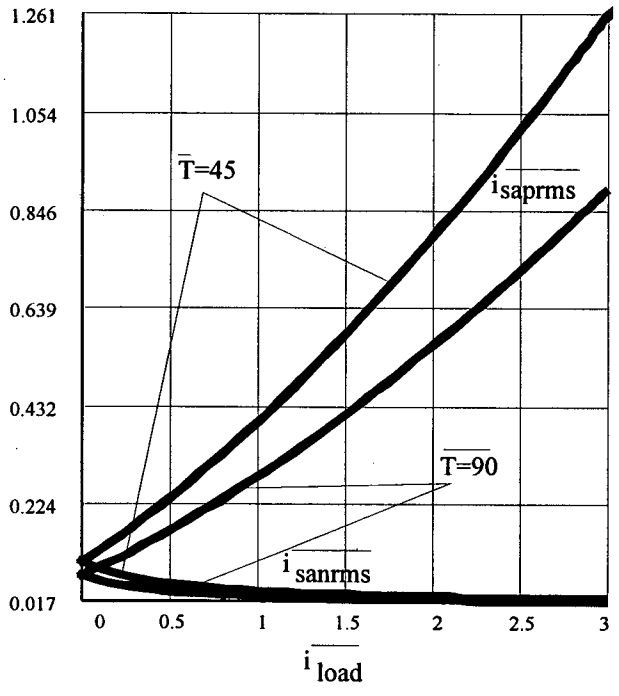


Fig. 2.3A. Auxiliary switch RMS currents versus load current for diode to switch commutation and switch to diode commutation.

Resonant inductor average current during one switching cycle can be similarly obtained.

By comparison with Fig. 2.10, Fig. 2.11 and Fig. 2.12 regarding the True-PWM-Pole case, the ARCPI is almost equal to the True-PWM-Pole in terms of the commutation durations and the auxiliary switch current stresses.

Appendix 2.2. State equations for the modified True-PWM-Pole schemes

1. For the case of Fig. 2.27(a), the state equations for the resonance between L_r, C_{r1} and C_{r2} are given by (2.7A):

$$\frac{L_r}{1+k}\frac{di_{Lr}}{dt} = \frac{V_{dc}}{1+k} - v_{Cr2}$$

$$\frac{2C_{r2}}{1+k}\frac{dv_{Cr2}}{dt} = i_{Lr} - \frac{I_L}{1+k} \tag{2.7A}$$

2. For the case of Fig. 2.27(b), the state equations for the resonance between L_r, C_{r1} and C_{r2} are given by (2.8A):

$$\frac{kL_r}{1+k}\frac{di_{Lr}}{dt} = \frac{V_{dc}}{1+k} - v_{Cr2}$$

$$\frac{2kC_{r2}}{1+k}\frac{dv_{Cr2}}{dt} = i_{Lr} - \frac{kI_L}{1+k} \tag{2.8A}$$

From the above equations, the phase plane for each commutation resonance can be obtained which facilitates the mathematical analysis as well as further physical understanding.

Appendix 2.3. Analysis of the commutation resonance in the capacitor connection inverter (diode to switch commutation)

1. S_2 turned off and S_{a2} turned on, D_2 current decreasing until blocking

$$i_{Lr} = \frac{V_o - V^*}{Z_r}\sin(\omega_r t) \tag{2.9A}$$

$$v_{cr} = V^* \cos(\omega_r t) \tag{2.10A}$$

where $\omega_r = \frac{1}{\sqrt{L_r C_r}}$, $Z_r = \sqrt{\frac{L_r}{C_r}}$ and V^* is the initial voltage of C_r.

2. Commutation resonance, C_{s2} charged and C_{s1} discharged

$$i_{Lr} = I_L \frac{C_p}{C_r}\cos(\omega_r' t) + \frac{V_o - V^{**}}{Z_r'}\sin(\omega' t) + I_L \frac{C_p}{C_s} \tag{2.11A}$$

$$v_{cs} = (V_o - V^{**})\frac{C_p}{C_s}\cos(\omega_r' t) - I_L \frac{C_p^2}{C_r C_s} Z_r' \sin(\omega_r' t) - I_L \frac{C_p + C_s}{C_s^2} t + V^{**} \tag{2.12A}$$

$$v_{cr} = (V_o - V^{**})\frac{C_s}{C_r}\cos(\omega_r' t) - I_L \frac{C_p C_s}{C_r^2} Z_r' \sin(\omega_r' t) + I_L \frac{C_p}{C_r C_s} t + V^{**} + (V_o - V^{**})\frac{C_s}{C_r} \tag{2.13A}$$

where $C_s = C_{s1} // C_{s2}$, $C_p = \frac{C_r C_s}{C_r + C_s}$, $\omega_r' = \frac{1}{\sqrt{L_r C_p}}$, $Z_r' = \sqrt{\frac{L_r}{C_p}}$, and I_L is the load current, V^{**} is the initial voltage of C_r.

3. L_r fully demagnetized, C_r charged

$$i_{Lr} = I^{***}\cos(\omega_r t) - \frac{V^{***}}{Z_r}\sin(\omega_r t) \tag{2.14A}$$

$$v_{cr} = V^{***}\cos(\omega_r t) + I^{***} Z_r \sin(\omega_r t) \tag{2.15A}$$

where V^{***} is the initial voltage of C_r and I^{***} is the initial current of L_r.

Commutation from switch to diode can be analogously analyzed.

Chapter 3. Operation of the Three Level Capacitor Clamping Inverter

Abstract: This chapter deals with the major operation problems of the three level capacitor clamping inverter, including clamping voltage stability, clamping capacitor stress, and output spectrum etc. Experimental results from a half bridge inverter verify the analysis.

3.1. Basic Operation Problems

A half bridge three level capacitor clamping inverter, as shown in Fig. 3.1, consists of two two-level switching cells, namely, C_1, C_2, S_1, S_4 (cell 1) and C_m, S_2, S_3 (cell 2), which can be treated separately in the modulation point of view. When the two cells share a given switching frequency, the control signal of one cell can be distinguished from the other by the duty cycle and the phase shift relationships, which will decide the next aspects of operation:

- Clamping voltage steady state stability.
- Output voltage spectrum.
- Clamping capacitor stress.
- Clamping voltage dynamic stability.

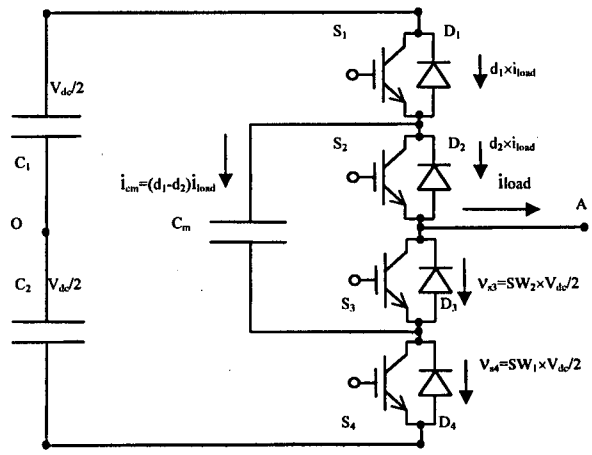


Fig. 3.1. Configuration of a half bridge three level capacitor clamping inverter.

3.2. Clamping Voltage Steady State Stability

Referring to Fig. 3.1, steady state stability of the clamping voltage is decided by the current flowing through the clamping capacitor. Stability will be guaranteed as far as this current can be averaged to zero during each switching cycle. When the load current is

supposed to be constant during a switching cycle, the average current flowing through the clamping capacitor during that switching cycle will be given by (3.1):

$$i_{cm} = (d_1 - d_2) \cdot i_{load} \tag{3.1}$$

where d_1 and d_2 are the instantaneous duty cycle of cell 1 and cell 2 respectively. Obviously, *$i_{cm}=0$ or $d_1=d_2=d$ will ensure the steady state stability during the local switching cycle.*

3.3. Output Voltage Spectrum

It has been concluded that a set of control signals phase shifted by $2\pi / p$ (p is the number of cells) will produce an output voltage where the harmonics up to p times of the switching frequency are zero [74]. In a two cell's case, when v_{cm} is supposed to be equal to $V_{dc}/2$, the output voltage is given by (3.2):

$$v_{AO} = v_{S3} + v_{S4} - \frac{V_{dc}}{2} = sw_2 \cdot \frac{V_{dc}}{2} + sw_1 \cdot \frac{V_{dc}}{2} - \frac{V_{dc}}{2} \tag{3.2}$$

where SW_1 and SW_2 are the switching functions of cell 1 and cell 2. When SW_1 or $SW_2=1$, the down switch (S_4 or S_3) is in blocking state.

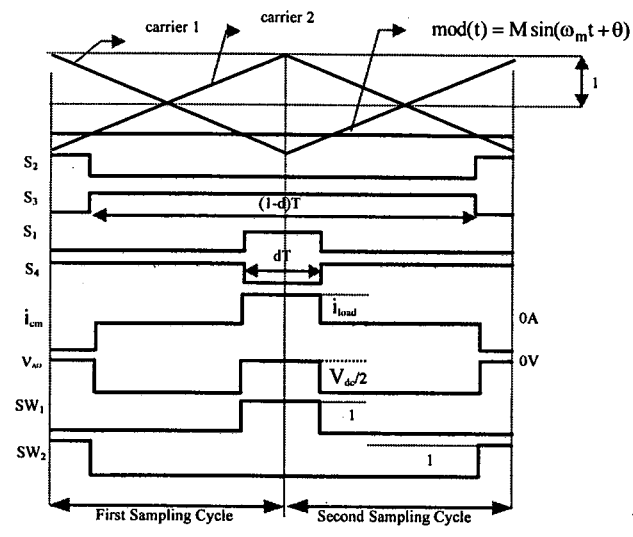


Fig. 3.2. Sub-harmonic PWM modulation pattern of the main circuit and the associated waveforms.

Control signals fulfilling the conditions of equal duty cycle and π phase shift can be generated by intersecting a sinusoidal modulating reference with two π phase shifted bipolar triangle carriers, as shown in Fig. 3.2. Assuming that the modulating reference starts from the coordinate zero, the two natural sampling PWM series SW_1 and SW_2 can be expressed in Fourier form as given by (3.3) and (3.4) respectively [136][137]:

$$
\begin{aligned}
sw_1 = {} & \frac{1}{2} + \frac{M}{2} sin(\omega_m t) + \sum_{m=1,3,5...}^{\infty} (-1)^{\frac{m+1}{2}} \frac{2J_0^{\frac{mM\pi}{2}}}{m\pi} sin(m\omega_c t - \frac{\pi}{2}) \\
& + \sum_{m=1,3,5..}^{\infty} \sum_{n=\pm 2,\pm 4,..}^{\pm\infty} \frac{2J_n^{\frac{mM\pi}{2}}}{m\pi} sin(\frac{m\pi}{2}) \cos[(m\omega_c t + n\omega_m t) - m\pi] \\
& + \sum_{m=2,4,..}^{\infty} \sum_{n=\pm 1,\pm 3,..}^{\pm\infty} \frac{2J_n^{\frac{mM\pi}{2}}}{m\pi} \cos(\frac{m\pi}{2}) sin[(m\omega_c t + n\omega_m t) - m\pi]
\end{aligned}
\tag{3.3}
$$

$$
\begin{aligned}
sw_2 = {} & \frac{1}{2} + \frac{M}{2} sin(\omega_m t) - \sum_{m=1,3,5...}^{\infty} (-1)^{\frac{m+1}{2}} \frac{2J_0^{\frac{mM\pi}{2}}}{m\pi} sin(m\omega_c t - \frac{\pi}{2}) \\
& - \sum_{m=1,3,5..}^{\infty} \sum_{n=\pm 2,\pm 4,..}^{\pm\infty} \frac{2J_n^{\frac{mM\pi}{2}}}{m\pi} sin(\frac{m\pi}{2}) \cos[(m\omega_c t + n\omega_m t) - m\pi] \\
& + \sum_{m=2,4,..}^{\infty} \sum_{n=\pm 1,\pm 3,..}^{\pm\infty} \frac{2J_n^{\frac{mM\pi}{2}}}{m\pi} \cos(\frac{m\pi}{2}) sin[(m\omega_c t + n\omega_m t) - m\pi]
\end{aligned}
\tag{3.4}
$$

where M is the modulation index, ω_m is the sinusoidal modulating reference frequency, ω_c is the triangle carrier frequency, and $J_n^{(\frac{mM\pi}{2})}$ is the Bessel function of the first kind and n order of argument $\frac{mM\pi}{2}$. Substitution from (3.4) and (3.3) in (3.2), the output voltage of the half bridge three level capacitor clamping inverter is given by (3.5):

$$
v_{AO} = V_{dc} \frac{M}{2} sin(\omega_m t) + V_{dc} \sum_{m=2,4,..}^{\infty} \sum_{n=\pm 1,\pm 3,..}^{\pm\infty} \frac{2J_n^{\frac{mM\pi}{2}}}{m\pi} \cos(\frac{m\pi}{2}) sin[(m\omega_c t + n\omega_m t) - m\pi] \tag{3.5}
$$

From (3.5), the following conclusions are obtained regarding the output spectrum under π phase shifting condition:

- *The triangle carrier frequency components together with its cross modulation harmonics are canceled.*
- *Among the cross modulation harmonics families, m=1,3,5..families are canceled.*
- *No even harmonics exist in the spectrum.*

3.4. Clamping Capacitor Stress

When control signals for the two cells are with equal duty cycle and are π phase shifted, the RMS current stress through the clamping capacitor will be dependent on the load current together with the duty cycle of the local switching cycle, which is given by (3.6) and (3.7):

$$i_{cm.rms}(t) = i_{load}(t)\sqrt{2(1-d(t))}\ ;\ \text{when } d>0.5 \tag{3.6}$$

$$i_{cm.rms}(t) = i_{load}(t)\sqrt{2d(t)}\ ;\quad \text{when } d<0.5 \tag{3.7}$$

where $i_{cm.rms}(t)$ is the quasi-instantaneous RMS current stress through the clamping capacitor which is solved over switching cycle, and d(t) is the duty cycle of the two cells. Moreover:

$$d(t) = \frac{1+\mathrm{mod}(t)}{2} \tag{3.8}$$

So that substitution for (3.6) and (3.7) yields (3.9):

$$i_{cm.rms}(t) = i_{load}(t)\sqrt{1-|\mathrm{mod}(t)|} \tag{3.9}$$

Eq. (3.9) is represented in Fig. 3.3. From which, the following conclusions are drawn as regards the clamping capacitor stress:

- *The maximum RMS current equals the peak load current.*
- *Maximum RMS current occurs when pure reactive power is transferred.*

Similarly, the voltage ripple across the clamping capacitor is obtained in (3.10):

$$\Delta v_{cm}(t) = \frac{Ti_{load}(t)}{C_m} \frac{(1 - |\text{mod}(t)|)}{2} \tag{3.10}$$

where $\Delta v_{cm}(t)$ is the voltage ripple amplitude.

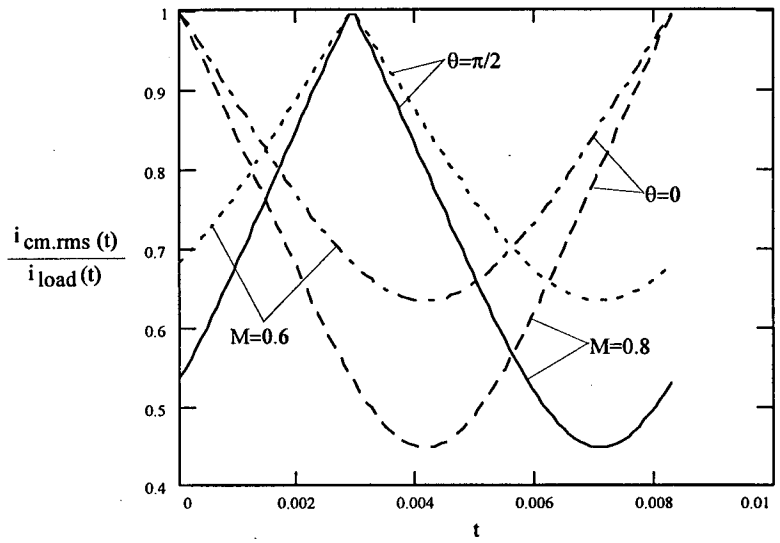


Fig. 3.3. Clamping capacitor current stress related to load current and load power factor.

$i_{load}(t) = I_p sin(\omega_m t)$, mod$(t) = Msin(\omega_m t + \theta)$, $\omega_m = 2\pi \times 60$.

3.5. Clamping Voltage Dynamic Stability

Dynamic stability refers to the ability of the clamping voltage to return to its nominal value after a perturbation with no specific control over it, i.e., the self-balancing ability.

3.5.1. Self-Balancing under Ideal Condition

Assume that for some reason, expected or unexpected, typically during the start-up process, the clamping voltage arrives at a value other than $V_{dc}/2$, then the output voltage can be expressed by (3.11):

$$v_{AO} = sw_2 v_{cm} + sw_1\left(\frac{V_{dc}}{2} - v_{cm}\right) - \frac{V_{dc}}{2} \tag{3.11}$$

which can be rearranged as (3.12):

$$v_{AO} = \frac{V_{dc}}{2}(sw_1 + sw_2 - 1) + (sw_1 - sw_2)(\frac{V_{dc}}{2} - v_{cm}) \tag{3.12}$$

The second part of (3.12) represents the output voltage response to the clamping voltage variation. Substitution from (3.3) and (4.4) in (3.12), the output voltage variation is given by (3.13):

$$\Delta v_{AO} = (\frac{V_{dc}}{2} - v_{cm})\{\sum_{m=1,3,5...}^{\infty} (-1)^{\frac{m+1}{2}} \frac{4J_0^{\frac{mM\pi}{2}}}{m\pi} sin(m\omega_c t - \frac{\pi}{2})$$
$$+ \sum_{m=1,3,5..}^{\infty} \sum_{n=\pm2,\pm4,..}^{\pm\infty} \frac{4J_n^{\frac{mM\pi}{2}}}{m\pi} sin(\frac{m\pi}{2}) \cos[(m\omega_c t + n\omega_m t) - m\pi]\} \tag{3.13}$$

Assume a load impedance of $z_j\angle\theta_j$ at the harmonic frequency of j, the corresponding load current variation can be written by (3.14):

$$\Delta i_{load} = (\frac{V_{dc}}{2} - v_{cm})\{\sum_{m=1,3,5...}^{\infty} (-1)^{\frac{m+1}{2}} \frac{4J_0^{\frac{mM\pi}{2}}}{m\pi} \frac{1}{z_{m\omega_c}} sin(m\omega_c t - \frac{\pi}{2} - \theta_{m\omega_c})$$
$$+ \sum_{m=1,3,5..}^{\infty} \sum_{n=\pm2,\pm4,..}^{\pm\infty} \frac{4J_n^{\frac{mM\pi}{2}}}{m\pi} \frac{1}{z_{m\omega_c+n\omega_m}} sin(\frac{m\pi}{2}) \cos[(m\omega_c t + n\omega_m t) - m\pi - \theta_{m\omega_c+n\omega_m}]\} \tag{3.14}$$

When this load current variation is reflected back to the clamping capacitor, the resultant charging current variation will be given by (3.15):

$$\Delta i_{cm} = \Delta i_{load}(sw_1 - sw_2) \tag{3.15}$$

Substitution from (3.3) (3.4) and (3.14) in (3.15), the result of which will be a substantially complicated expression and may not allow for any physical insight. However, when the clamping voltage balancing is particularly concerned, only the DC component in Δi_{cm} is of interest and this fact simplifies the task. The DC component in the charging current variation can finally be written by (3.16):

$$\Delta i_{cm.dc} = (\frac{V_{dc}}{2} - v_{cm})G \tag{3.16}$$

where:

$$G = \frac{1}{2}\sum_{m=1,3,5...}^{\infty}\{[(-1)^{\frac{m+1}{2}}\frac{4J_0^{\frac{mM\pi}{2}}}{m\pi}]^2\frac{1}{z_{m\omega_c}}\cos(\theta_{m\omega_c})\}$$
$$+\frac{1}{2}\sum_{m=1,3,5..}^{\infty}\sum_{n=\pm2,\pm4,..}^{\pm\infty}\{[\frac{4J_n^{\frac{mM\pi}{2}}}{m\pi}\sin(\frac{m\pi}{2})]^2\frac{1}{z_{m\omega_c+n\omega_m}}\cos(\theta_{m\omega_c+n\omega_m})\} \tag{3.17}$$

This DC charging current can be related to the clamping voltage variation by (3.18):

$$(\frac{V_{dc}}{2} - v_{cm})G = c_m\frac{dv_{cm}}{dt} \tag{3.18}$$

The clamping voltage dynamics is given in the end by (3.19):

$$v_{cm} = \frac{V_{dc}}{2} + [v_{cm}(0) - \frac{V_{dc}}{2}]e^{-\frac{\frac{1}{C_m}}{G}t} \tag{3.19}$$

where $v_{cm}(0)$ denotes the initial value of the clamping voltage, C_m is the capacitance of the clamping capacitor and C_m/G is the time constant for the first order dynamics.

The self-balancing mechanism analyzed above is illustrated in Fig. 3.4. For a given perturbation Δv_{cm}, the output voltage will vary correspondingly (Δv_{AO}) which results in load current variation Δi_{load}. The resulted charging/discharging current variation Δi_{cm} for the clamping capacitor will give rise to voltage component $\Delta\Delta v_{cm}$, which tends to cancel the original perturbation and the clamping voltage is finally maintained at its nominal value.

The foregoing discussion supports the next conclusions with regard to the self-balancing ability under ideal condition:

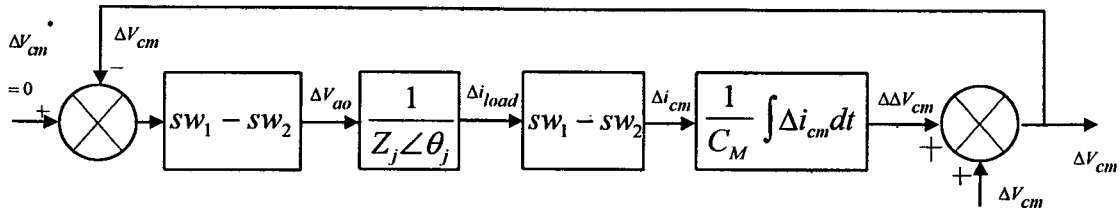


Fig. 3.4. Self-balancing mechanism of the three level capacitor clamping inverter.

- *Clamping voltage drift leads to components of odd multiples of the triangle carrier frequency and their cross-modulation harmonics at the output, according to (3.13), which essentially determines the self-balancing ability.*
- *Clamping voltage dynamic stability depends on the sign of constant G expressed by (3.17). G will always be positive if* $\theta \neq \pm\pi/2$, *i.e., non-pure-inductive/capacitive load will ensure the clamping voltage stability, regardless of its initial conditions. This is satisfied with normal inverter load.*
- *Clamping voltage response exhibits typical one order performance. The duration of the dynamics is dependent on the time constant (Cm/G) of this dynamics, which is further decided by: clamping capacitance, modulation index and load properties.*

3.5.2. Self-Balancing under Non-ideal Condition

Practical circuit contains various non-ideal conditions [138] which potentially lead to asymmetrical operation of the two cells and the clamping voltage may drift as a result. Among them, deviation from ideal trigger timing deserves the most treatment.

In an extreme case, duty cycle of one switching cell is always higher than the other for one load current direction, and is always lower for the other direction. Both tend to over-charge (discharge) the clamping capacitor. However, while the clamping capacitor being over-charged (discharged), a discharging (charging) current arises simultaneously due to the self-balancing mechanism counteracting the current of the first case. *Dependent on the extent of the asymmetry, there exists a new operation point other than the nominal value at which the net current flow to the clamping capacitor is averaged to zero during each switching cycle.* This conclusion is verified by PSPICE simulation, the results of which are shown in Fig. 3.5(a)(b).

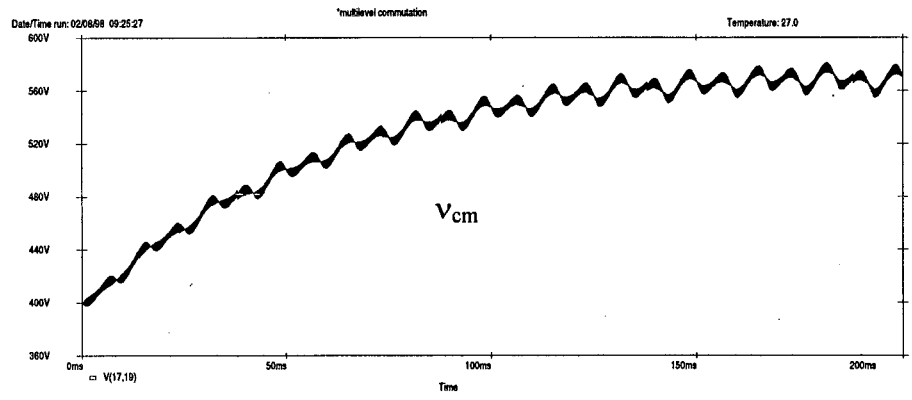
For this simulation, the half bridge three level capacitor clamping inverter is modulated by sub-harmonic PWM pattern, as shown in Fig. 3.2. Parameters/specifications are shown in Table 3.1. Duty cycle difference for the case of Fig. 3.5(a) is 0.01 (-0.01) and for the case of

Fig. 3.5(b) is –0.01 (0.01). The clamping voltage is balanced at 560V and 240V respectively after the first order dynamics. PSPICE program for this simulation is listed in Appendix 3.1.

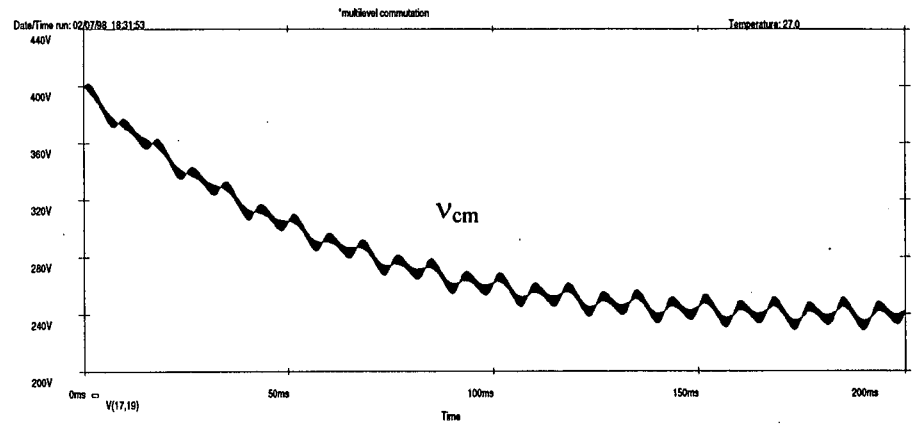
Table 3.1. Circuit parameters/specifications for simulation of self-balancing under non-ideal condition

Input voltage	V_{dc}=800V	Output Filter	L_f=0.1mH C_f=4uF	Modulation index	M=0.8	Load resistance	R_o=1Ω
Clamping capacitance	C_m=680uF	Operating frequency	f_c=10kHz	Fundamental Frequency	f_m=60Hz	Initial clamping voltage	$v_{cm}(0)$=400 V

Besides the extreme case discussed above, dead time causes no clamping voltage drift because it is symmetrical for the two cells. Dead time effect for one cell is canceled by the same effect for the other cell during the switching cycle.



(a) Duty cycle difference 0.01 for the positive current, -0.01 for the negative current



(b) Duty cycle difference –0.01 for the positive current, 0.01 for the negative current

Fig. 3.5. Clamping voltage self-balancing under non-ideal operation conditions.

3.5.3. Self-Balancing in Three Phase System

For a three phase system, as shown in Fig. 3.6, generally the same procedure in sub-section 3.5.1 can be followed. For any initial deviations $\Delta v_{cma,cmb,cmc}$ of the three clamping voltages, the corresponding load current variation in each individual phase must be solved which is then reflected back to each clamping capacitor determining its charging/discharging current variation. For this purpose, the corresponding voltage variation between the two neutral points O and O' is of the principal importance.

When three sinusoidal modulating waves with $2\pi/3$ mutual phase shift are applied for the three phases intersecting the same carrier wave, the resulted switching functions can be expressed by (3.20):

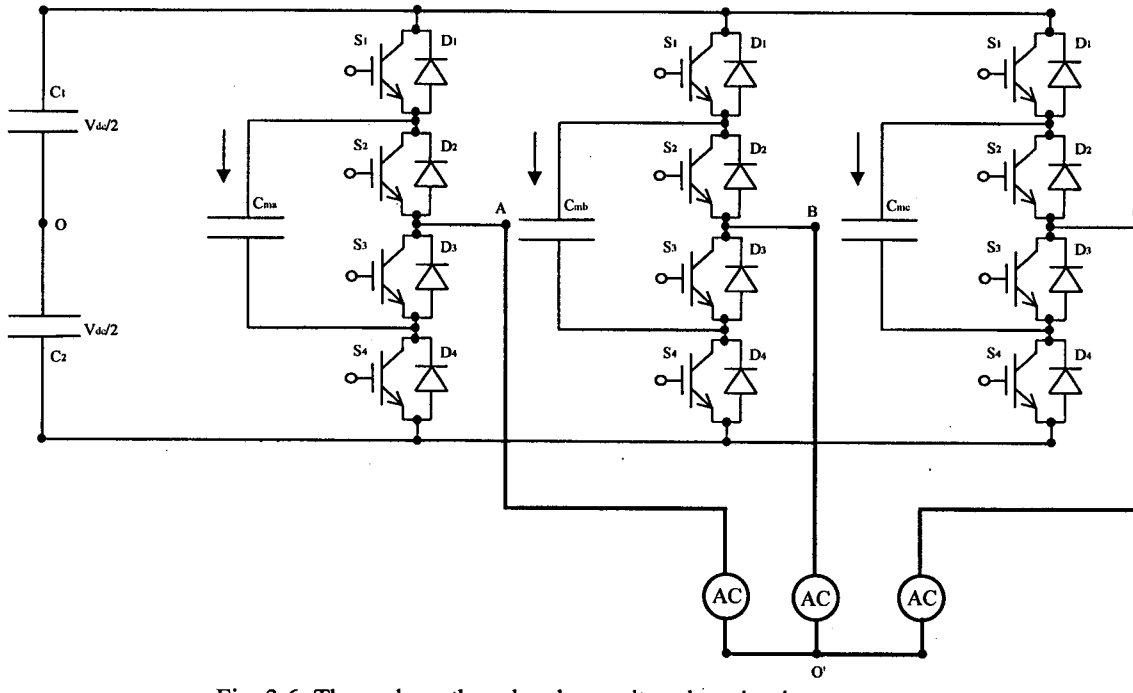


Fig. 3.6. Three phase three level capacitor clamping inverter system.

$$(sw_1 - sw_2)_{a,b,c} = \sum_{m=1,3,5...}^{\infty} \frac{4}{m\pi}(-1)^{\frac{m+1}{2}} J_0^{\frac{mM\pi}{2}} \sin(m\omega_c t - \frac{\pi}{2}) + \sum_{m=1,3,5..}^{\infty} \sum_{n=\pm 2,\pm 4,..}^{\pm\infty} \frac{4}{m\pi} \sin(\frac{m\pi}{2}) \cos[(m\omega_c t + n\omega_m t) - n\varphi_{a,b,c}] \tag{3.20}$$

where $\varphi_{a,b,c}$=0, $-2\pi/3$, $2\pi/3$ for phase A, B and C. From (3.20) and (3.12), voltage variation between each phase terminal and the DC link neutral potential is given by (3.21):

$$\Delta v_{AO,BO,CO} = (SW_1 - SW_2)_{a,b,c} \Delta v_{cma,cmb,cmc} \tag{3.21}$$

Afterwards voltage variation between the two neutral points is expressed by (3.22):

$$\Delta v_{o'o} = \frac{1}{3}(\Delta v_{AO} + \Delta v_{BO} + \Delta v_{CO}) \tag{3.22}$$

From (3.21) and (3.22), load voltage variation of each individual phase can be obtained and the same procedure in sub-section 3.5.1 can then be followed for the reflected charging/discharging current variation of each clamping capacitor. This procedure is not detailed here and only the conclusions are given as following:

1. *When clamping voltages in three phases are not equal (say, perturbation of clamping voltage in one phase during normal operation), the odd multiples of the triangular carrier frequency and their cross modulation harmonics enforce the self-balancing, which is similar to the half bridge case. The three clamping voltages will firstly get equal and then move to the nominal value synchronously.*
2. *When clamping voltages in three phases are equal (say, start up process), the cross modulation harmonics of the odd multiples of the triangular carrier frequency (odd multiples of the triangular carrier frequency are canceled) enforce the self-balancing. The three clamping voltages move to the nominal value directly and synchronously.*

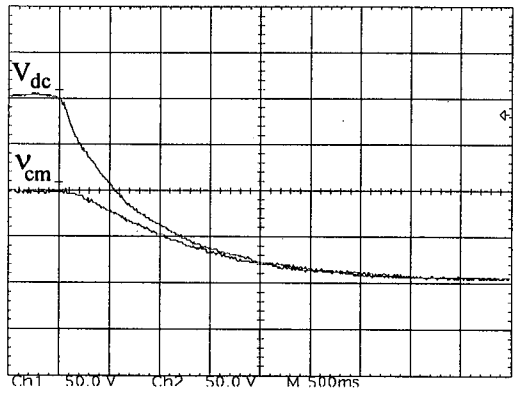
3.6. Experimental Verification

Basic experimental verification of the self-balancing ability is conducted on a small scale prototype. Refer to Fig. 3.1, the prototype parameters and specifications are given in Table 3.2, and the results are shown in Fig. 3.7. For Fig. 3.7(a) (b), the DC supply is opened and the clamping voltage is monitored. For Fig. 3.7(c) (d), the DC supply is closed and the clamping voltage is monitored.

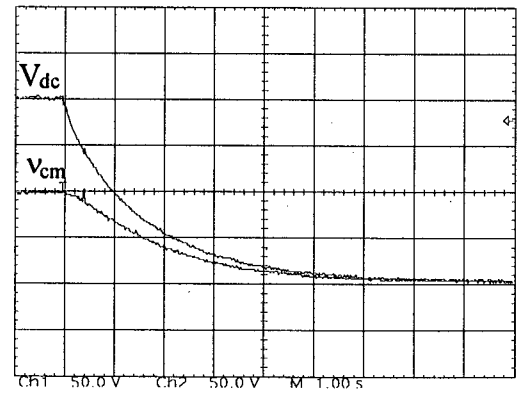
Table 3.2. Prototype parameters/specifications for experimental verification of the self-balancing

Input voltage	V_{dc}=200V	Output Filter	L_f=1.45mH C_f=12uF	Modulation index	M=0.62
Clamping capacitance	C_m=1650uF	Operating frequency	f_c=6.5kHz	Fundamental frequency	f_m=50Hz

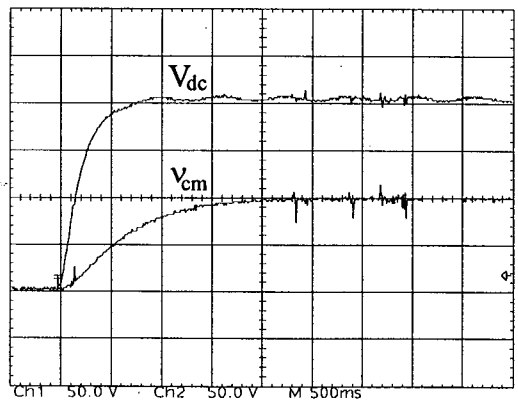
From the experimental results shown in Fig. 3.7, in both cases, the clamping voltage responds to the DC supply voltage change with first order characteristic and no resonance or overshoot is caused. However, longer time is taken to reach steady state when the load is lighter for either step-down or step-up, which means that the time constant of the dynamics runs inversely proportional to the load resistance. This result is in line with (3.19).



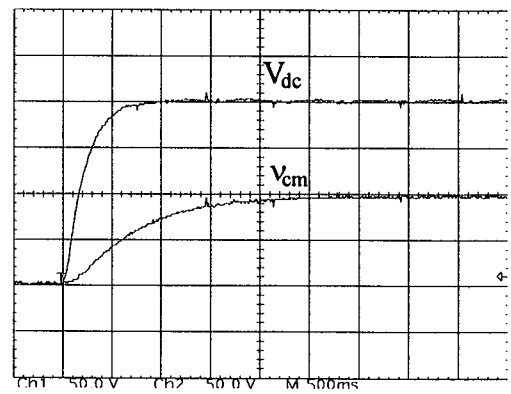
(a) Ro=3Ω



(b) Ro=7.5Ω



(c) Ro=3Ω



(d) Ro=7.5Ω

Fig. 3.7. Basic experimental verification of the self-balancing ability of the half bridge three level capacitor clamping inverter.

3.7. Conclusions

- Gating relationship of the two cells is associated with the clamping voltage stability, clamping capacitor stress and the output spectrum etc. While equal duty cycle is required for steady state stability, phase shift implies a compromise between clamping capacitor

stress and output spectrum. With π phase shift, the output spectrum is optimal and maximum RMS current of the load current value happens when the load is pure reactive.

- Clamping voltage is self-balancing under the given gating pattern with non-pure reactive load. Time constant of the first order dynamics is dependent on clamping capacitance, modulation index and the load properties.
- Dependent on the extent of non-ideals, typically resulted gating or switching mismatches, clamping voltage is balanced to a new operation point other than the nominal value, due to the self-balancing mechanism counteracting such non-ideals.

Appendix 3.1. PSPICE program for simulation under non-ideal situation

```
*Self-balancing under non-ideal situation

* pulse pattern generation
v1 1 0 pulse (-10 10 .1u 50u 50u .1u 100u)
e2 2 0 value {-v(1)}
vmod 5 0 sin(0 8 60 0 0 0)
vdri 42 0 pulse (0.2 -0.2 8.34m 0.1u 0.1u 8.34m 16.8m)  * duty cycle difference
esu1 6 0 table {v(1)-v(5)+v(42)} (-1e-2,10) (1e-2,0)
esd1 10 0 table {v(6,0)} (2,10) (3,0)
esu2 7 0 table {v(2,5)} (-1e-2,10) (1e-2,0)
esd2 11 0 table {v(7,0)} (2,10) (3,0)

*main circuit
su3 16 24 6 0 sswitch
ds3 24 17 dmod
du3 17 16 dmod
su4 17 25 7 0 sswitch
dsu4 25 18 dmod
du4 18 17 dmod
sd1 18 26 11 0 sswitch
dsd1 26 19 dmod
dd1 19 18 dmod
sd2 19 27 10 0 sswitch
dsd2 27 20 dmod
dd2 20 19 dmod

*device model
.model sswitch vswitch(ron=0.01 roff=1e6 von=4 voff=2)
.model dmod d(is=2e-15 bv=1500 tt=0 cjo=1p)

*DC link supply
vc2 16 40  400
vc22 40 20 400

*flying capacitance
c3 17 19 680u ic=400

*load and filter
lload 18 41 0.1mH
rload 41 40 1
cload 41 40 4uF

.tran 10u 600m 0 10u uic
.options vntol=10m abstol=10m reltol=0.1 itl5=0
.probe i(lload) i(c3) v(17,19)
.end
```

Chapter 4. True-PWM-Pole Three Level Capacitor Clamping Inverter

Abstract: This chapter proposes a transformer connection True-PWM-Pole three level capacitor clamping inverter. Besides the detailed description of the circuit configuration and operation, the specific features of this configuration are highlighted. Several topology variations for multilevel case are illustrated shortly in the end.

4.1. Circuit Configuration

The proposed circuit is shown in Fig. 4.1. It consists of a main half bridge three level capacitor clamping inverter circuit and two auxiliary branches. The first auxiliary branch (S_{a1}, S_{a4}) assists the commutation of the first switching cell (S_1, S_4) and forms the first pole; whereas the second auxiliary branch (S_{a2}, S_{a3}) assists the commutation of the second switching cell (S_2, S_3) and forms the second pole. The two poles can be regarded independent from each other so far as the clamping capacitor voltage is maintained at $V_{dc}/2$.

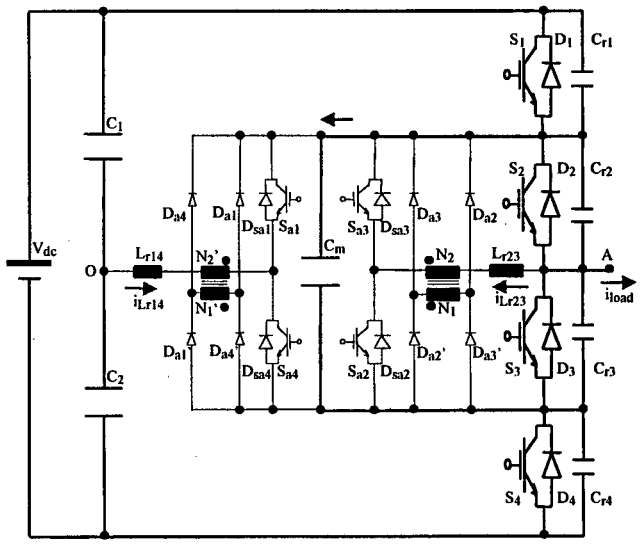


Fig. 4.1. The proposed True-PWM-Pole three level capacitor clamping inverter.

4.2. Circuit Operation

Prior to discussion of the commutation process, the following conditions are assumed:

- Positive load current i_{load} is flowing and remains constant during the commutation.
- Capacitors C_1 and C_2 are treated as voltage sources during the commutation. Clamping capacitor voltage is stabilized at $V_{dc}/2$.
- Transformer ratios are set to ensure sufficient energy for the pole voltage to swing to the rail level in the presence of commutation losses, as discussed in Chapter 2.
- Circuit parasitics, device switching transients and transformer imperfections are neglected.
- Main switch turn-off and auxiliary switch turn-on happen at the same instant decided from the modulation scheme discussed in Chapter 3, while the main switch turn-on happens until the detected voltage across the switch declining to zero. Conduction interval of the auxiliary switch is universally constant covering the maximum commutation duration as discussed in Chapter 2.

Refer to the theoretical waveforms for the entire switching cycle shown in Fig. 4.2, and the commutation step diagrams for the first sampling cycle shown in Fig. 4.3, the commutation of the half bridge inverter during the first sampling cycle consists of the next steps:

Step 1 (t_0-t_1): Circuit steady state. D_4 and S_2 carry load current discharging the clamping capacitor C_m. Output Voltage V_{AO}=0.

Step 2 (t_1-t_2): S_2 turned off and S_{a2} turned on at t_1, which starts a resonance between L_{r23} and C_{r2}, C_{r3}. N_2 sees a voltage of $kV_{dc}/2$ after turn-on of S_{a2} and conduction of D_{a2} and D_{a2}'. C_{r2} is charged and C_{r3} is discharged.

Step 3 (t_2-t_3): v_{Cr2} rises to $V_{dc}/2$ at t_2 leading to conduction of D_3. Then S_3 is turned on at zero voltage. Snap on of D_3 may cause oscillation due to its forward recovery as well as stray/internal inductances of the paths.

Step 4 (t_3-t_5): i_{Lr23} falls to zero at t_3 allowing for turn-off of S_{a2} at t_4. Circuit reaches another steady state. D_4 and D_3 carry load current. Clamping capacitor C_m is floating. And output voltage V_{AO}=-$V_{dc}/2$.

Step 5 (t_5-t_6): S_4 is turned off and S_{a4} is turned on at t_5, leading to conduction of D_{a4} and D_{a4}'. N_2' sees a voltage of $kV_{dc}/2$ which joins $V_{dc}/2$ enforcing current decreasing in D_4 .

Step 6 (t_6-t_7): i_{Lr14} rises to the load current level at t_6 leading to blocking of D_4. Resonance among L_{r14}, C_{r4} and C_{r1} is initiated. C_{r4} is charged while C_{r1} discharged. Recovery current of D_4 enhances the charging current and therefore facilitates the commutation process.

Step 7 (t_7-t_8): v_{Cr4} rises to $V_{dc}/2$ at t_7 leading to conduction of D_1. Then S_1 is turned on at zero voltage. Rapid current transfer from C_{r4} and C_{r1} to D_1 may cause oscillation.

Step 8 (t_8-t_9): i_{Lr14} falls to load current at t_8. D_1 stops conduction and S_1 starts carrying the load current.

Step 9 (t_9-t_{11}): i_{Lr14} extinguishes at t_9 allowing for turn-off of S_{a4} at t_{10}. Circuit reaches another steady state. S_1 and D_3 carry load current charging the clamping capacitor C_m. Output voltage V_{AO}=0.

In addition, the remaining two commutations in the second sampling cycle (D_3 to S_2 and S_1 to D_4) can be analogously inferred.

To summarize, for the proposed circuit, the main switch work with zero voltage turn-on and capacitive turn-off, whereas the main freewheeling diode work with zero voltage turn-on and zero current turn-off. Superior to the conventional snubber, the capacitive turn-off loss of the main switch can be minimized by optimizing the resonant capacitor to this end. Meanwhile, depending on its forward recovery property, the snap-on of the main freewheeling diode does not introduce any considerable loss.

Moreover, all the auxiliary devices work with zero current turn-off. And yet voltage is only reapplied after turn-on of the opposite auxiliary switch. Besides, despite of the bridge configuration, the turn-on of the auxiliary switch is actually snubbed by the resonant inductor since the opposite freewheeling diode carries no current beforehand and thus its reverse recovery is negligible. Transformer excitation is reset to zero after each commutation and no magnetic accumulation can happen.

In particular, by designing a transformer ratio less than 1/2, an auxiliary voltage of $(1-k)V_{dc}/2$ higher than $V_{dc}/4$ becomes available which delivers sufficient energy for the resonant pole to swing to the rail voltage. Thus the "boost" stage and the associated control complexity is no longer necessary.

Designing aspects of the two poles have been discussed in Chapter 2. Detailed implementation of a 3kW prototype will be presented in Chapter 5.

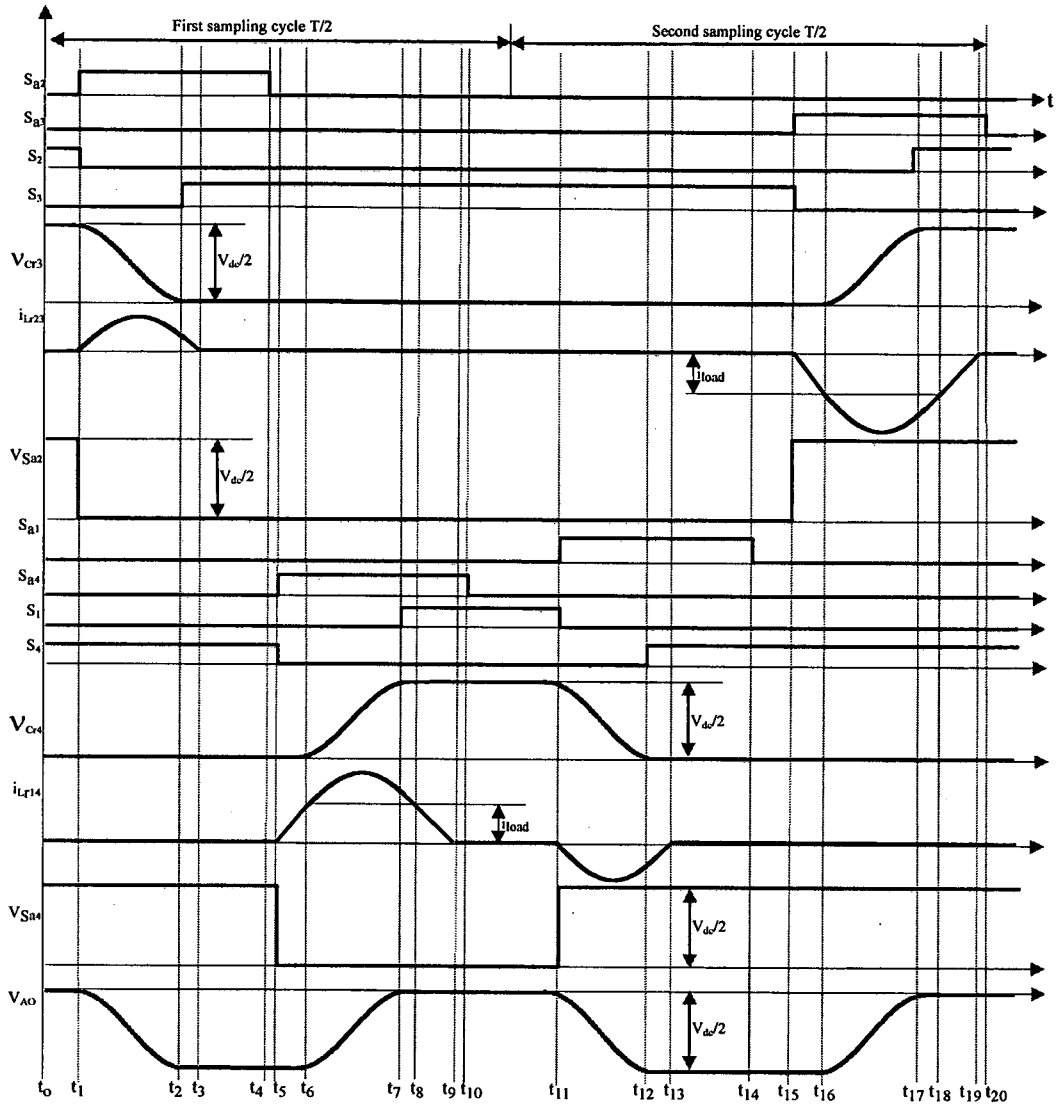
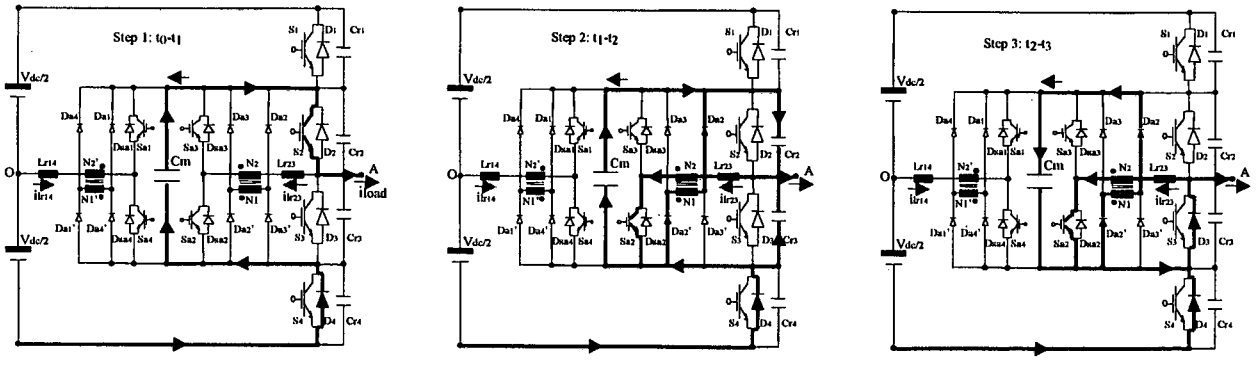


Fig. 4.2. Theoretical commutation waveforms for the proposed True-PWM-Pole three level capacitor clamping inverter in a entire switching cycle.



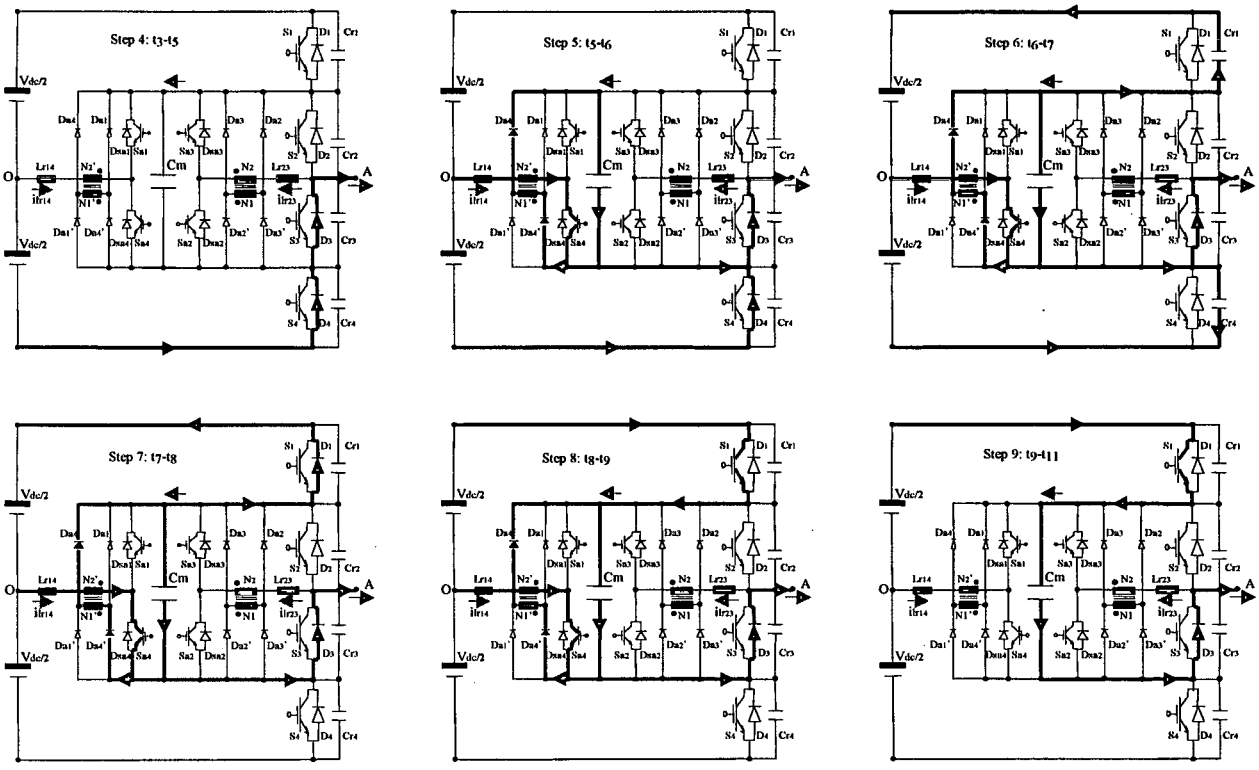


Fig. 4.3. Operation step diagrams for the first sampling cycle.

4.3. Specific Features

4.3.1. Clamping Voltage Stabilization

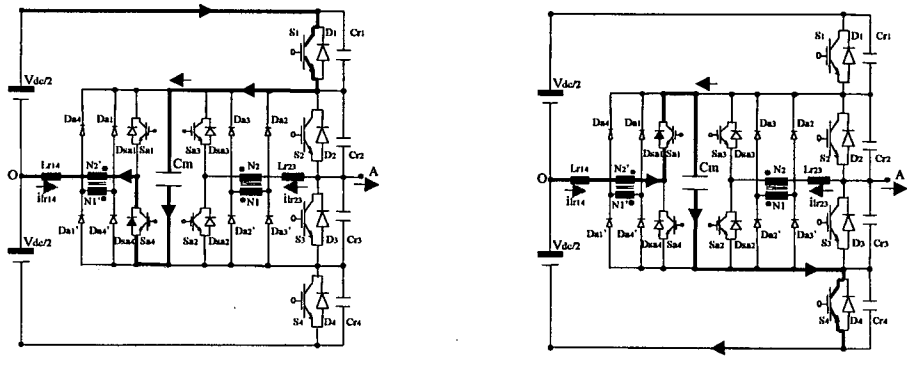
The self-balancing ability of the clamping voltage under the given modulation pattern verified in Chapter 3 is strongly subjected to load properties. Destructive clamping voltage variation may arise due to such reasons as load change (load open, reactive load for example) or triggering failure etc. Active control of the clamping voltage necessitates detection of the clamping voltage as well as the load current direction, which tends to complicate the system.

The proposed True-PWM-Pole three level capacitor clamping inverter posses charging/discharging paths for the clamping capacitor whenever perturbation occurs. When the clamping voltage gets below the nominal value, it will be charged by the up-capacitor ($V_{dc}/2$) through S_1, D_{sa4}, N_2' and L_{r14} when S_1 is gated, as shown in Fig. 4.4(a); or by the down-capacitor ($V_{dc}/2$) through S_4, $D_{sa1}$and L_{r14} when S_4 is gated, as shown in Fig. 4.4(b). In the meantime, when the clamping voltage gets above the nominal value, it will be discharged to the up-capacitor ($V_{dc}/2$) through D_1, Lr_{14}, N_2'and S_{a4} when S_{a4} is gated, as shown in Fig. 4.4(a);

or to the down-capacitor ($V_{dc}/2$) through S_{a1}, N_2', L_{r14} and D_4 when S_{a1} is gated, as shown in Fig. 4.4(b).

In other words, the charging paths are always existing except for the gating space interval between S_1 and S_4. However, the discharging paths become available only when the auxiliary switches S_{a1} or S_{a4} are gated.

Taking into account the magnetic losses and the conduction losses in the charging/discharging paths, the charging/discharging processes are a damped second order resonance involving the clamping capacitance, resonant inductor and the auxiliary transformer, which guarantees the clamping voltage to be stabilized at $V_{dc}/2$.



(a) (b)

Fig. 4.4. Charging (discharging) paths for the Clamping voltage through the auxiliary circuitry.

This feature in clamping voltage stabilization is lost when any of the modified auto-transformer connection True-PWM-Pole circuits is employed. The unidirectional auxiliary switch offers only discharging paths preventing the clamping voltage from being higher than the nominal value.

Note that when two storage capacitors are used in the DC side, this feature remains true only when the neutral potential is stable.

4.3.2. Normal Auto-Transformer Connection of the Second Pole

As discussed in Chapter 2, even though the normal auto-transformer connection True-PWM-Pole promises attractive properties in terms of the auxiliary switch current stress, auto-transformer primary voltage stress and the auto-transformer secondary current stress, the freewheeling current flowing in the auxiliary circuitry during non-commutation interval renders it not applicable and the transformer connection is preferred. The modified auto-transformer connections need extra snubbing for the series diode.

For the proposed three level inverter, the second pole (S_2, S_3, S_{a2} and S_{a3}) is a normal two-level structure and transformer connection or modified auto-transformer connection is inevitable. The first pole (S_1, S_4, S_{a1} and S_{a4}), however, is quite distinctive from a normal two-level structure. Because of the existence of the clamping capacitance, no freewheeling current can expect to flow through either the auxiliary switch or the auxiliary diode, if the normal auto-transformer connection is used.

As shown in Fig. 4.5, suppose that after the commutation for turn-off of S_4, a residual current flows through Lr_{14}, N_2', S_{a4}, C_m and D_1. The clamping capacitance C_m will then get discharged and a voltage difference between C_1 and C_m will arise, which tends to resist the residual current until it returns zero.

Such being the case, the phenomenon discussed in Chapter 2 no longer exists in this specific configuration. And the normal auto-transformer connection True-PWM-Pole becomes practically applicable for the first pole. This alternative was also tested in a 3kW prototype with essentially the same result as the transformer connection except for the auxiliary switch current stress which is nearly halved.

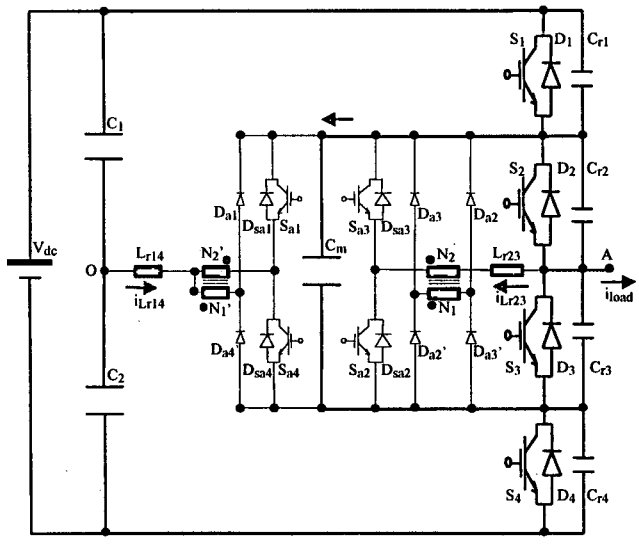


Fig. 4.5. Modified configuration of the True-PWM-Pole three level capacitor clamping inverter, with transformer connection for the second pole and normal auto-transformer connection for the first pole.

4.4. Topologies for Multilevel case (M>3)

Transformer connection True-PWM-Pole zero voltage switching scheme can be extended to multilevel case (M>3). Fig. 4.6 demonstrates a four level True-PWM-Pole capacitor clamping inverter, where S_{1a}, S_{1a}' and S_1, S_1'; S_{2a}, S_{2a}' and S_2, S_2'; S_{3a}, S_{3a}'and S_3, S_3'

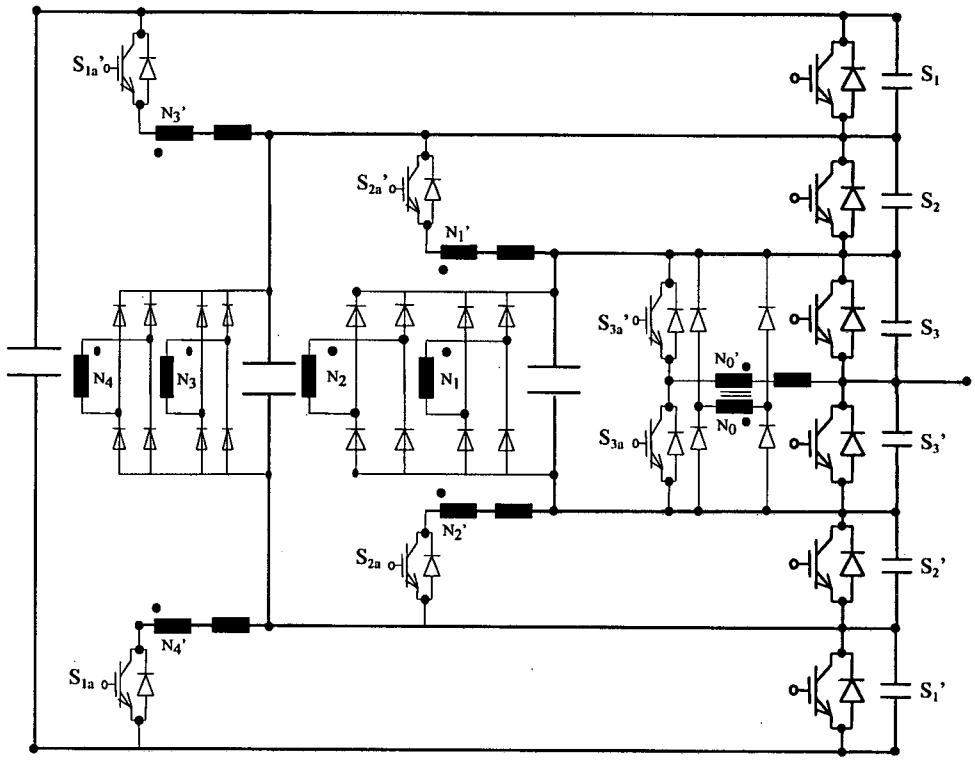


Fig. 4.6. Transformer connection True-PWM-pole zero voltage switching scheme extended to multilevel capacitor clamping inverter (M>3), example of four level case.

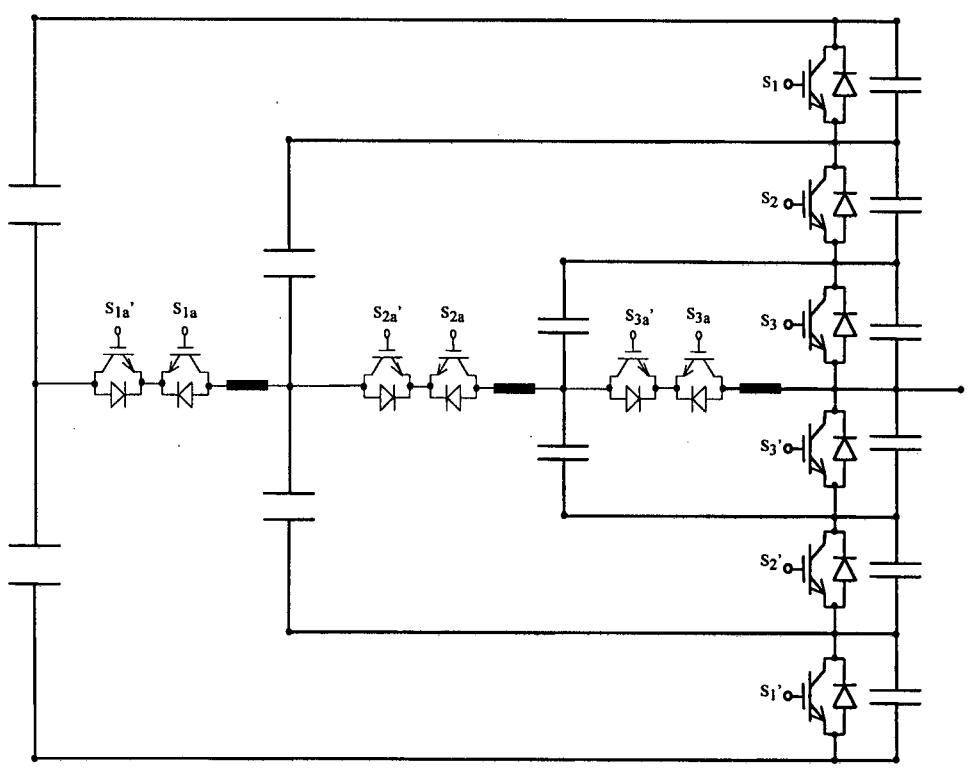


Fig. 4.7. ARCPI zero voltage switching scheme extended to multilevel capacitor clamping inverter (M>3), example of four level case.

form three poles. Each pole is independent of the others provided that the clamping capacitor voltages are stable.

The operation of each pole is the same as the normal transformer connection True-PWM-Pole except for the separate inductor and discrete auxiliary switch. The auxiliary switch blocks the same voltage as the main switch which enhances its applicability.

In addition, the Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI) is also extensible to multilevel case (M>3). A four level case is shown in Fig. 4.7, where S_{1a}, S_{1a}' and S_1, S_1'; S_{2a}, S_{2a}' and S_2, S_2'; S_{3a}, S_{3a}'and S_3, S_3' form three poles each work independently. All auxiliary switches block half of the main switch voltage.

4.5. Conclusions

- The proposed transformer connection True-PWM-Pole three level capacitor clamping inverter achieves zero voltage switching of the main devices and zero current switching of the auxiliary devices, without provoking any voltage/current spikes across the main or the auxiliary switches, without yet requiring any additional current monitoring or controlling.
- The proposal features a interesting second merit in stabilizing the clamping voltage, due to the existence of the charging/discharging paths established by the auxiliary devices for the clamping capacitor. In the meanwhile, due to the clamping capacitor involved in the resonant current paths, the normal auto-transformer connection True-PWM-Pole becomes applicable in this case without the problems of the freewheeling current and the residual current, which achieves the same property as the modified auto-transformer connection True-PWM-Pole without any voltage spike across the auxiliary switch.
- Both transformer connection True-PWM-Pole and ARCPI schemes are extensible to multilevel case (M>3) with the same performance as in the two-level case. The True-PWM-Pole extension requires considerable magnetics and diodes, while in the case of ARCPI extension, center-taped storage capacitors must be used and additional monitoring and controlling become necessary.

Chapter 5. Designing and Experimentation of the True-PWM-Pole Three Level Capacitor Clamping Inverter

Abstract: This chapter addresses a proof-of-concept 700V supply 3kW half bridge IGBT transformer connection True-PWM-Pole three level capacitor clamping inverter prototype. Hardware details and relevant experimental results are presented.

5.1. Prototype Specifications

A scaled laboratory prototype, as shown in Fig. 5.1, has been set up. The specifications of which are shown in Table 5.1.

Table 5.1. Prototype specifications

DC input voltage	V_{dc}=700V	Output voltage	$V_{o.rms}$=140V	Modulation index	M=0.62
Output power	P_o=3kW	Load current	$I_{o.rms}$=21.5A	Switching frequency	f_c=6.5kHz

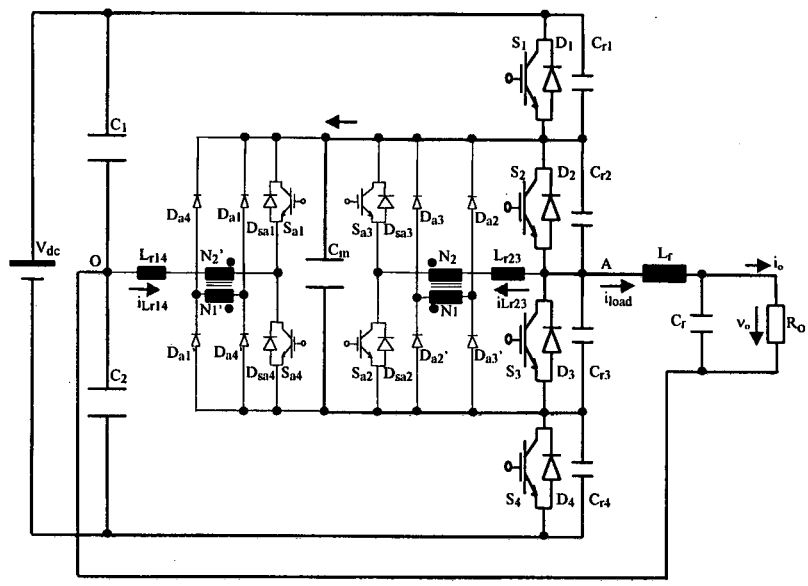


Fig. 5.1. Circuit Diagram of the 3kW half bridge laboratory prototype.

5.2. Main Circuit Designing

5.2.1. Power Supply

Three 300V/5A DC supplies are associated in series. An iron laminated 15mH inductor is put in series with the supply to suppress the ripple current.

5.2.2. DC link Capacitor

The designing criterion in the laboratory case is the DC voltage ripple across it. The capacitance is given by (5.1):

$$C_1 = \frac{TI_p}{\Delta V_{dc}} \tag{5.1}$$

where ΔV_{dc} is the peak to peak voltage ripple, T is the switching period and I_p is the load peak current. When maximum ΔV_{dc} is set to be 3V, this gives C_1=C_2= 1536uF.

In practice, the DC link capacitance should be designed for transience de-coupling between the utility side and the load side. Depending on the configuration of the rectifier side and the control of the whole system, the result can be quite different. The capacitors in use are C_1=C_2=3300uF, each with a nominal voltage of 350V.

5.2.3. Clamping Capacitor

Sizing of this capacitor is two-fold. On the one hand, higher capacitance allows for less voltage ripple, according to (3.10). And on the other hand, smaller capacitance reduces the clamping voltage transience duration, according to (3.19). Voltage ripple should be the major designing criterion in practice. Further, capacitor internal inductance and in particular its heat capacity to process the RMS current given in (3.9) must be taken into full account.

The actual capacitance used is 2750uF consisting of two 5500uF capacitors in series each with a nominal voltage of 250V.

5.2.4. Output Filter

The primary designing objective is to have the dominant harmonic component at the inverter output reduced to a given extent. From (3.5), for the given modulation index of 0.62, the dominant output voltage harmonic is calculated to be 0.35 of the fundamental component.

To keep the THD less than 5%, the dominant harmonic component need to be less than 3%. With a second order low-pass filter, the cut-off frequency ω_b can hence be decided by (5.2):

$$\omega_b = \frac{1}{\sqrt{L_f C_f}} = 2\pi(2f_c - f_m)10^{(20\lg 0.03 - 20\lg 0.35)/40} \tag{5.2}$$

where f_c is the switching frequency and f_m is output fundamental frequency.

Another designing objective is to avoid possible resonance at the output, especially in a closed loop system. For this purpose, the declining factor given by (5.3) must be considered.

$$\delta = \frac{1}{2R_o}\sqrt{\frac{L_f}{C_f}} \tag{5.3}$$

Define δ=0.65 and combine (5.2) and (5.3), the result will be L_f=0.37mH and C_f=4.5uF. The actual values used in the prototype are L_f=1.45mH and C_f=12uF.

A practical output filter designing, besides the preceding considerations, should also take into account such other factors as load short circuit protection, load inrush limiting, low frequency voltage stress etc.

5.2.5. Main Switches

The main switches S_1-S_4 used are two Non-Punch-Through IGBT modules SKM50GB123D. Ratings and the main electrical and thermal characteristics of which (including the inverse diodes) are shown in Table 5.2.

5.3. Resonant Circuit Designing

5.3.1. Resonant Components and Auxiliary Transformer

According to sub-section 2.4, the results of the designing are presented in Table 5.3.

5.3.2. Auxiliary Switches (S_{a1}-S_{a4})

According to Fig. 2.11(a) and Fig. 2.12(a), for load with peak current of 30A, the maximum peak and RMS currents of the auxiliary switch are 54.2A and 8.4A respectively. Blocking voltage of the auxiliary device is the same with the main device.

Devices used in the prototype as auxiliary switch are SKM50GB123D, the same as the main switch.

Table 5.2. IGBT module SKM50GB123D characteristics

symbol	conditions	values
Ic	Tcase=25°C/80°C	50A/34A
Icm	Tcase=25°C/80°C	100A/68A
Vces		1200V
Tj		-55°C- +150°C
Vcesat	Vge=15V, Ic=50A, Tj=25°C / 150°C	4.5V/3.5V(max.)
tdon/tr	Vcc=600V,Vge=15V, Ic=50A, Rgon=Rgoff=3.3Ω ,Tj=125°C	80nS/150nS
tdoff/tf	Vcc=600V,Vge=15V, Ic=50A, Rgon=Rgoff=3.3Ω ,Tj=125°C	250nS/150nS
VF(diode)	IF=50A, Vge=0V, Tj=150°C	2.9V
Qrr(diode)	Tj=125°C	10uC
trr(diode)	Tj=125°C	250nS
Rthjc	per IGBT	0.31°C / W
Rthjc	per DIODE	0.9°C / W
Rthch	per module	0.05°C / W
Lce		20nH

Table 5.3. Resonant components and transformer designing results

Resonant capacitor	*1*. Capacitance: C_r=0.1uF, *2*. Type: low-loss polypropylene, *3*. Estimated maximum turn-off loss 1W.
Resonant inductor	*1*. Inductance: L_r=15uH, *2*. Structure: 36 turns 15AWG copper wire wound on air core bobbin, *3*. Current rate of changing 14A/uS.
Transformer	*1*. Transformer ratio: k =0.4, *2*. Structure: 60 turns twisted wire (7 strands 24AWG) in the primary and 24 turns twisted wire (15 strands 24AWG) in the secondary wound on E65/29 ferrite core, *3*. Allowed equivalent loop resistance around 2.2Ω.

5.3.3. Auxiliary Diodes (D_{sa1}-D_{sa4}, D_{sa1}'-D_{sa4}')

The current stress of the auxiliary diodes is k times of that in the auxiliary switch. The blocking voltage of the auxiliary diodes is the same with the main device.

Components used in the prototype are HFA30TA60C in TO-220AC case, ratings and characteristics are given as following :

I_{FAV}=30A, V_{RWM}=600V, V_{FM}=1.2V, R_{thjc}=0.85 ° C / W and $t_{rr.max}$=60nS.

5.4. Thermal Designing

Thermal designing takes account of merely the conduction losses of the main devices. Switching losses of the main devices as well as the switching/conduction losses of the auxiliary devices are neglected. This simplification is reasonable in the prototype case.

For calculation of the conduction loss in the inverter instance, a conduction loss model has been recommended, which represents the device as a constant voltage drop in series with a nonlinear resistive element during conduction [139]. This nonlinear element is further simplified to a linear element so that a closed form solution can be reached. Conduction loss of the four devices is then given by (5.4):

$$P_{loss-on} = 4(P_{on-s} + P_{on-D}) \tag{5.4}$$

where:

$$P_{on-s} = \frac{1}{2} I_p V_{ce.o}(\frac{1}{\pi} + \frac{M}{4}\cos\theta) + I_p^2 R_{ce}(\frac{\sqrt{3}}{8\sqrt{\pi}} + \frac{M}{3\pi}\cos\theta) \tag{5.5}$$

$$P_{on-D} = \frac{1}{2} I_p V_{Fo}(\frac{1}{\pi} - \frac{M}{4}\cos\theta) + I_p^2 R_{ak}(\frac{\sqrt{3}}{8\sqrt{\pi}} - \frac{M}{3\pi}\cos\theta) \tag{5.6}$$

Device models for the IGBT and the reverse diode are given in (5.7) and (5.8) respectively:

$$V_{cesat} = V_{ce.o} + IR_{ce} \tag{5.7}$$

$$V_F = V_{F.o} + IR_{ak} \tag{5.8}$$

Where $V_{ce.o}$ and $V_{F.O}$ are the IGBT and reverse diode voltage drops at zero current, and R_{ce} and R_{ak} are the resistive elements of IGBT and diode. From SEMIKRON data-sheet [140], $V_{ce.o} \leq 1.5+0.002(Tj-25°)$, $R_{ce}=0.025+0.0001(Tj-25°)$, $R_{ak}(125°)=22m\Omega$ and $V_{F.O}(125^{O})=1.2V$.

According to (5.5) and (5.6), assume a modulation index M=0.62, load power factor $\cos\theta = 1$, load peak current Ip=30A and junction temperature Tj=125°, the loss distribution and the total loss are calculated to be: P_{on-s}=17.9W, P_{on-D}=4.04W, $P_{loss-on}$=87.8W.

Then, for a given junction temperature upper limit, the required thermal resistance of the heat-sink is given by (5.9) (four devices share a heat-sink):

$$R_{thha} = \frac{T_{j\max} - T_a - 2(P_{on-s} + P_{on-D})R_{thch} - P_{on-s}R_{thjc.s}}{P_{loss-on}} \tag{5.9}$$

where: T_{jmax} is the given maximum junction temperature.

Ta is the operation ambient temperature.

$R_{thjc.s}$ is the junction to case thermal resistance per IGBT.

$R_{thjc.D}$ is the junction to case thermal resistance per diode.

R_{thch} is the case to heatsink contact thermal resistance.

R_{thha} is the heatsink to ambient thermal resistance.

Setting Tjmax=125°C and substituting the known parameters into (5.9), one will get: R_{thha}=1.05°C/W.

For the prototype, a 200mm square heat-sink is mounted vertically on a wooden base accommodating the two main IGBT modules (with thermal compound). The two auxiliary IGBT modules (with thermal compound) together with the four diodes (with thin mica insulation layer and thermal compound) are mounted on another heat-sink of the same size assembled on the same base.

5.5. IGBT Driving Designing

5.5.1. Main IGBT Module Driving

Intelligent single IGBT driver SEMIDRIVER SKHI10 is used for each main IGBT device. The main feature of this driver is summarized as following:

- Improved output buffer enabling switching current up to 400A at 20kHz.
- Built-in soft turn-off mechanism enabling high DC bus voltage operation.
- Built-in DC/DC converter (4kV insulation) easing the driving supply arrangement.
- Information transfer (driving, protecting) by ferrite transformer offering high dv/dt immunity (75kV/uS).
- Optional input signal level: 15V/5V.
- External fault reset.

Electrical specifications and settings of the SKHI10 driver actually used is given in Table 5.4.

Table 5.4. Specifications and settings of SKHI10 driver

Electrical Characteristics (Ta=25°C)		
symbol	Term	Value
Vs	supply voltage	15V
Is	supply current(max.)	0.5A
VG(on)	turn-on gating voltage	15V
VG(off)	turn-off gating voltage	-8V
td(on)	input-output turn-on propagation time	1uS
td(off)	input-output turn-off propagation time	1uS
td(error)	error input-output propagation time	1uS
VCEsat	Vce reference for fault indication	5.2V
Rgon	internal turn-on gate resistor	22Ω
Rgoff	internal turn-off gate resistor	22Ω
tmin	fault indication delay time (Rce=18kΩ,Cce=330pF)	1.5uS
Error logic	fault indication outlet (pin J3 shorted)	low-logic

5.5.2. Auxiliary IGBT Module Driving

Intelligent medium power double IGBT driver SEMIDRIVER SKHI23/12 is used for each auxiliary IGBT driving. The major features of this driver are:

- Output buffer enabling switching 200A at 20kHz.
- Soft turn-off enabling higher DC bus voltage.
- Built-in DC/DC converter for driving power supply.
- Ferrite transformer information delivering enabling high dv/dt immunity.
- Built-in adjustable interlock circuit.

- Optional input signal level: 15V or 5V.
- Automatic fault reset when both inputs are zero.

Electrical specifications and settings of the driver are summarized in Table 5.5:

Table 5.5. Specifications and settings of SKHI23/12 driver

Electrical Characteristics (Ta=25 °C)		
symbol	Term	Value
Vs	supply voltage	15V
Is	supply current(max.)	0.5A
VG(on)	turn-on gating voltage	15V
VG(off)	turn-off gating voltage	-8V
td(on)	input-output turn-on propagation time	1.4uS
td(off)	input-output turn-off propagation time	1.4uS
td(error)	error input-output propagation time	1.4uS
VCEsat	Vce reference for fault indication	5.2V
Rgon	internal turn-on gate resistor	22Ω
Rgoff	internal turn-off gate resistor	22Ω
tmin	fault indication delay time (Rce=18kΩ,Cce=330pF)	1.5uS
Error logic	fault indication outlet (pin J2 shorted)	low-logic
tTD	interlock time (RTD1,RTD2 not installed)	10uS

5.5.3. Zero Voltage Detecting

According to Chapter 2, each main device voltage must be detected so that it is turned on at the moment when the voltage across it is zero.

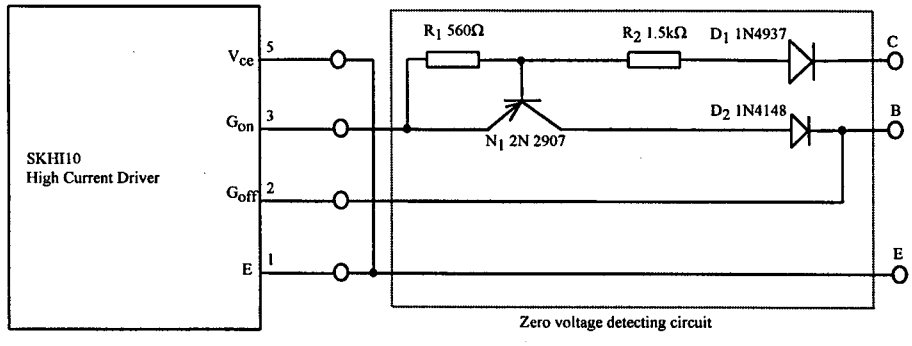


Fig. 5.2. Zero voltage detecting circuit in the prototype.

The circuit used in the prototype is shown in Fig. 5.2. The PWM turn-on command at G_{on} can only reach the output terminal B when the device collector voltage V_{CE} declining to near zero (threshold decided by R_1 and R_2). PWM turn-off command at G_{off} is sent directly to the output terminal B.

Note that the turn-on signal property (turn-on resistance etc.) of the driver would be altered with the adding of the zero voltage detecting circuit. However, dissimilar to hard-switching where turn-on performance (diode reverse recovery di/dt) is significantly affected by the turn-on signal property, the turn-on performance under zero voltage switching is not affected to any considerable extent.

Protection function of the SKHI10 driver must be disabled to avoid false failure indication during the commutation resonance. Device protection is then partly assumed by the zero voltage detecting circuit. Characteristics of the protection, however, are changed.

5.6. Control Designing

5.6.1. Control Requirements

- To generate the main switch gating signals according to the PWM modulation strategy indicated in Fig. 3.2. A dead time must be introduced between the complementary signals (S_1 and S_4, S_2 and S_3). The minimum/maximum pulse width must be set higher than the auxiliary switch gating signals.
- To generate the auxiliary switch gating signals according to Fig. 4.2, the width of which should be set according to Fig. 2.10(a).
- To give distinguishable fault memory as well as manual reset.

The control circuit designed is shown in Appendix 5.2 and is explained below.

5.6.2. Control Diagram

Clock signal generator U1: To use 2^{14} addresses generating the 50Hz output, the clock frequency should be: $f_{clock}=(1/50)/\ 2^{14}=833kHz$. The VCO embedded in CD4046 is used to generate this clock, where R1=10kΩ and C1=202pF. R2 and R3 serve to convert the CMOS 15V output to TTL 5V for the next stage, R2=10kΩ and R3=4.7kΩ.

Address counters U2/U3: Two CD4040s are cascaded to generate the 2^{14} address signals.

Gating signals generator U4: An EPROM 27256M is used to generate the eight switching signals, the BASIC program is listed in Appendix 5.1. According to Fig. 2.10, the maximum commutation duration is 11.3uS. Based on which, the auxiliary switch gating signal width is set at 14.4uS and the minimum/maximum PWM pulse widths are set at 28.8uS and 124.8uS respectively, with a modulation index of 0.62. Dead time of 2.4uS is inserted. Note that C24-C31 are imperative to suppress the EPROM output noise, each valued at 15nF.

Signal level converter U11/U12: Two SN7406s are used to convert the 5V signal back to 15V so that to enhance the noise immunity when the switching signals are delivered to the drivers. Resistors R4-R11 each valued at 2.2kΩ are pull-up resistors for SN7406s.

Fault trip-off U5/U6: Six OR gates are used to enable shut-down in the case of fault.

Auxiliary devices fault memory U7: The double drivers for the auxiliary devices are built with a automatic reset after fault, which is not favored in terms of fault identification. Thus external fault memory U7 is offered as a remedy.

Fault summing and manual reset U9/U10: The whole prototype will be shut down in the case of any individual device fault. Fault memory can only be removed with manual reset button. This designing enhances operation safety of the prototype. Resistors R12-R17 each valued at 2.2kΩ are external pull-up resistors for the fault indications from the drivers. Capacitors C2-C7 each valued at 100pF provide noise immunity for the fault indications.

5.7. Experimental Results

Fig. 5.3 shows the output load side voltage and filter inductor current waveforms. Fig. 5.4 shows the three level output voltage V_{AO}. Fig. 5.5 shows the ZVS commutation process of the main switch S_3 during switching cycle. Further in Fig. 5.6, the details of turning-on at i_{load}=21A are shown, for a predicted dv/dt of 90V/uS (averaged over $t_{12} - t_{11}$) and di/dt of 14A/uS, the experimental values are about 90V/uS and 13A/uS respectively. And in Fig. 5.7, the details of turning-off at i_{load}=24A are shown, for a predicted dv/dt of 152V/uS (averaged over $t_7 - t_6$), the experimental value is about 146V/uS.

Besides the commutation processes of the switch, the main freewheeling diode commutation processes are also shown in Fig. 5.8 and Fig. 5.9.

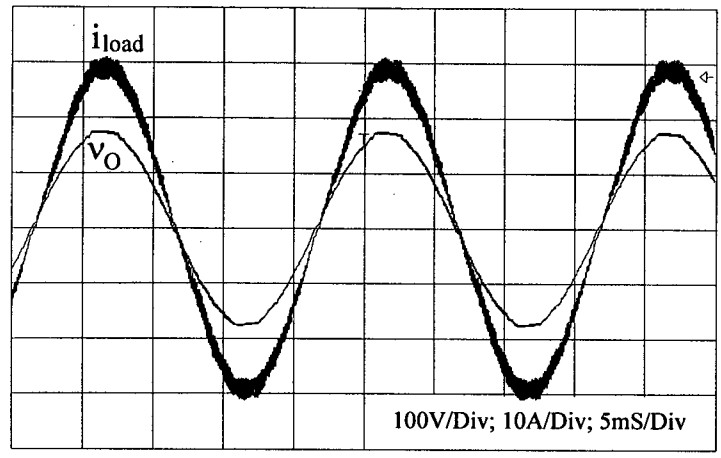


Fig. 5.3. Experimental output voltage and filter inductor current.

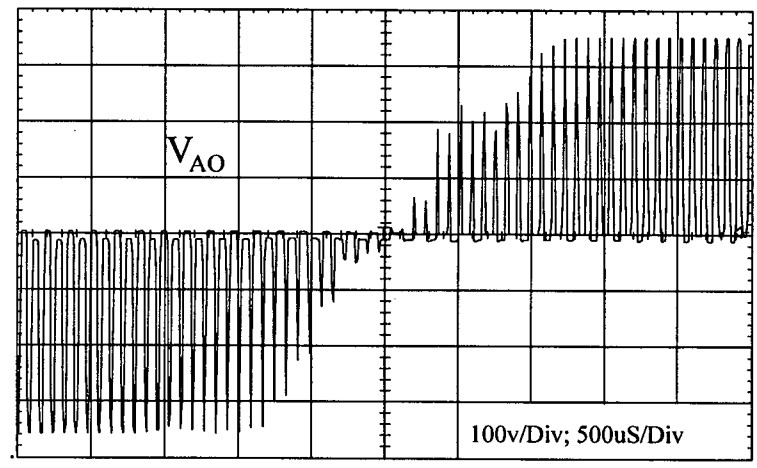


Fig. 5.4. Experimental inverter output voltage.

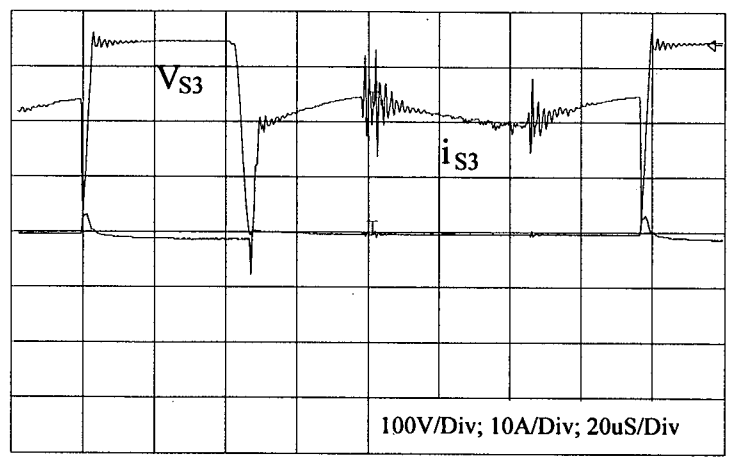


Fig. 5.5. ZVS commutation of the main switch (S_3).

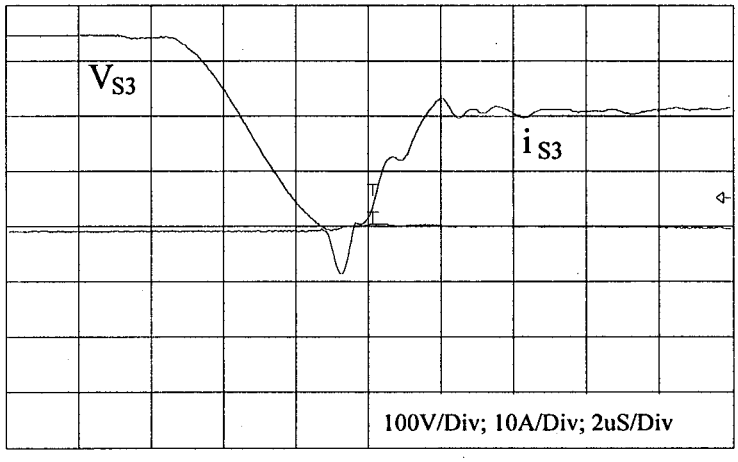


Fig. 5.6. Extended turn-on process of S_3.

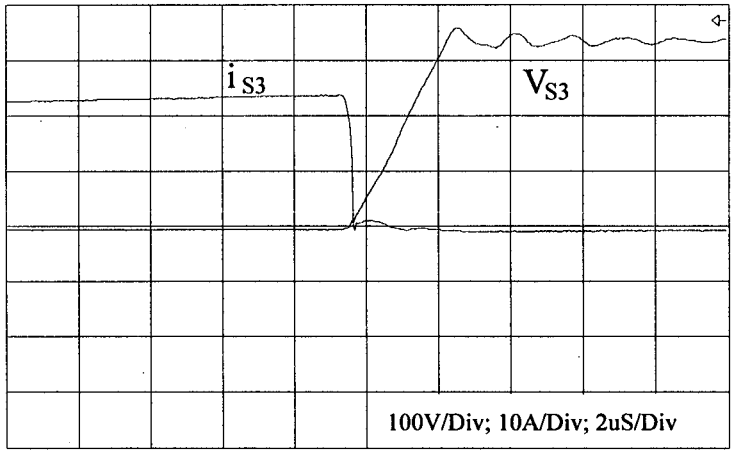


Fig. 5.7. Extended turn-off process of S_3.

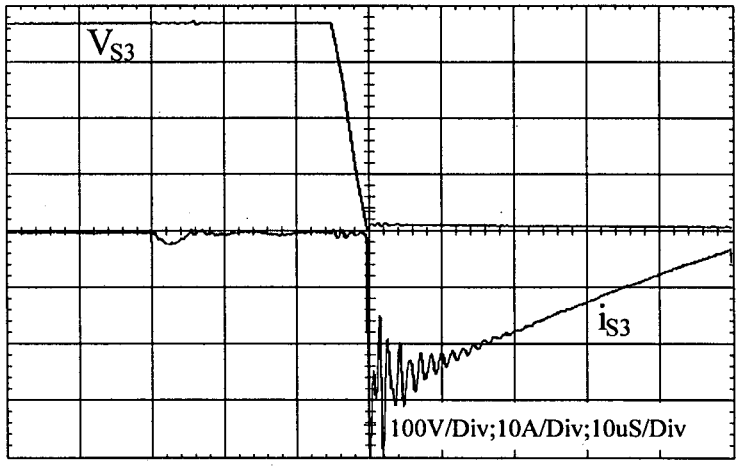


Fig. 5.8. Turn-on process of D_3 (L_f=0.45mH, C_f=12uF).

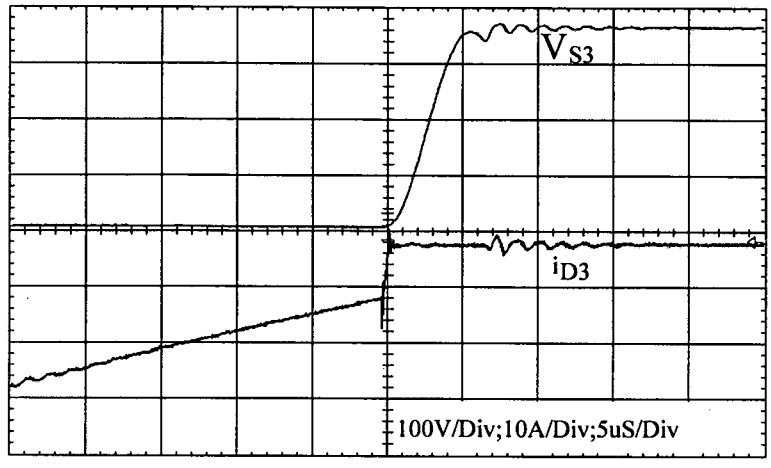


Fig. 5.9. Turn-off process of D_3 (L_f=0.45mH, C_f=12uF).

Fig. 5.10 shows the ZCS commutation process of the auxiliary switch (S_{a3}/D_{sa3}) at i_{load}=22A. For the predicated commutation duration of 9.8uS according to Fig. 2.10(a), and the predicated peak current of 46.3A according to Fig. 2.11(a), the experimental values are 9.5uS and 46.5A respectively.

Fig. 5.11 shows the resonant inductor current waveform when i_{load}=0A. For the predicated commutation duration of 5.9uS and the predicted peak current of 24.1A, the experimental values are about 5.5uS and 23.5A respectively. In the meantime, Fig. 5.12 shows the resonant inductor current waveform when i_{load}=22A. The experimental commutation duration and peak current are about 9.5uS and 46.5A, which are in accordance with the predicted values of 9.8uS and 46.3A according to Fig. 2.10(a) and Fig. 2.11(a).

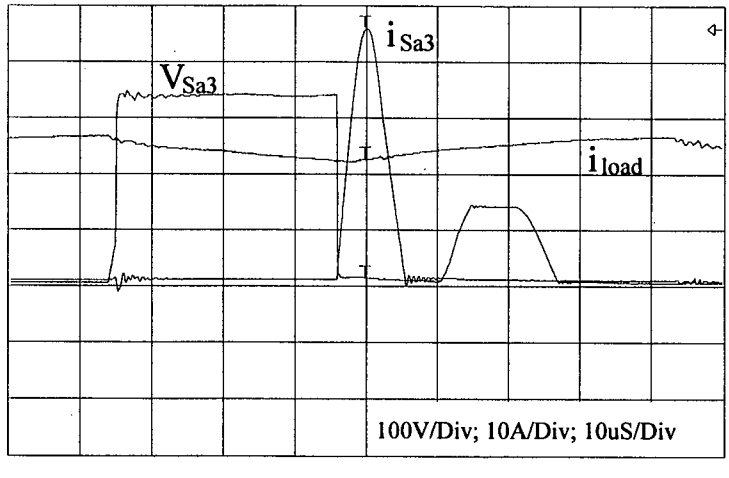


Fig. 5.10. ZCS commutation of the auxiliary switch (S_{a3}).

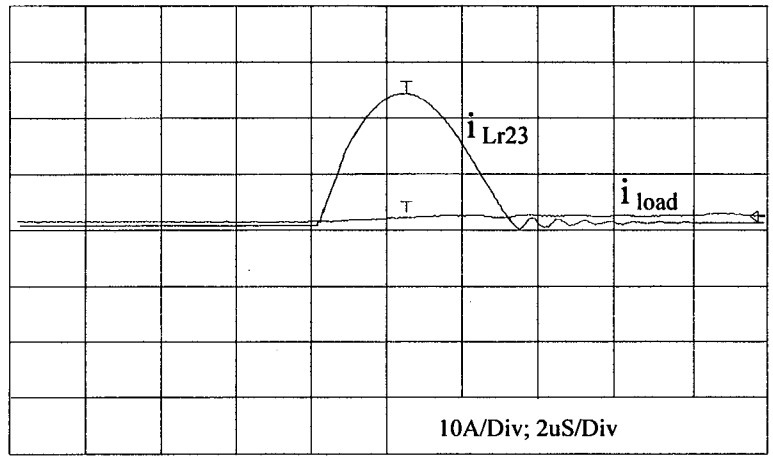


Fig. 5.11. Resonant inductor current waveform at i_{load}=0A.

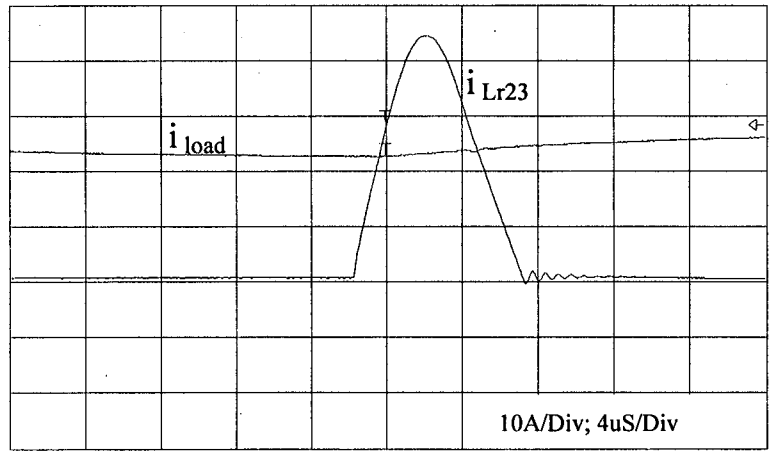


Fig. 5.12. Resonant inductor current waveform at i_{load}=22A.

5.8. Conclusions

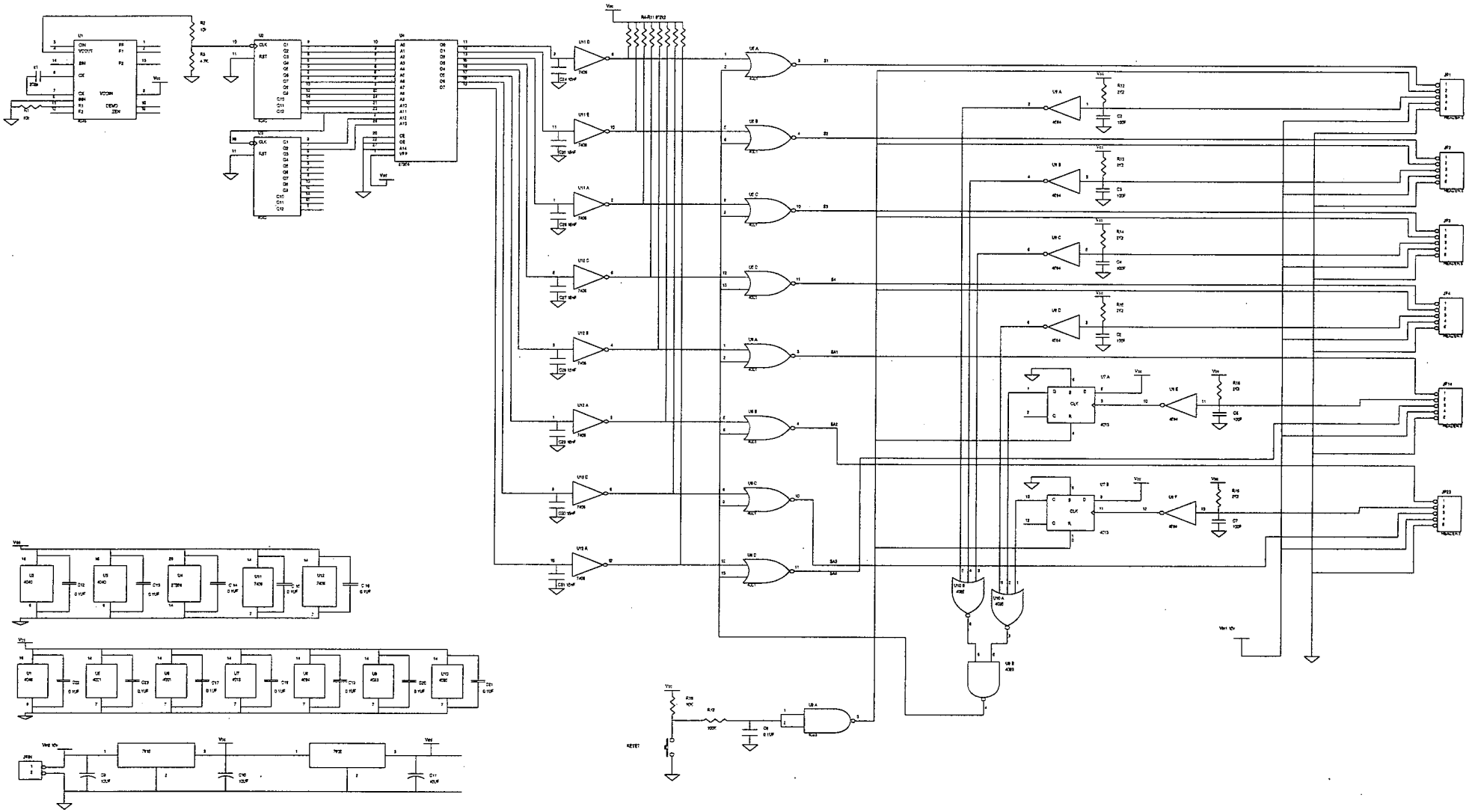
The foregoing presentation of the experimentation justifies the following conclusions:

- The proposed scheme ensures zero voltage turn-on and capacitive turn-off of the main switches, without causing any voltage/current spikes across these switches.
- The proposed scheme ensures inductive turn-on and zero current turn-off of the auxiliary switches, without causing any voltage spike.
- Main freewheeling diode works with zero voltage turn-on and zero current turn-off. Oscillation may occur during the diode forward recovery process due to the fast current transfer from the snubbing capacitors to the diode
- Characteristic curves presented in Chapter 2 regarding the commutation duration, resonant inductor peak current and resonant inductor RMS current are verified by the 3kW half bridge prototype.

Appendix 5.1. BASIC program for generating the gating signals in EPROM 27256M

```
970  U = 1   'DATA OUTPUT LINES COUNTER
980  OPEN "A:SPWM.DAT" FOR OUTPUT AS #1
990  PRINT #1, ":10";   'FIRST DATA OUTPUT LINE FORMAT
1000 PRINT #1, "000000";   'FIRST DATA OUTPUT LINE FORMAT
1010 FOR I = 0 TO 127: 'SELECT SWITCHING CYCLE
1020 RA1 = 0: RA2 = 0: RA3 = 0: RA4 = 0   'DEAD TIME/AUXILIARY COMMAND COUNTER
1030 FOR K = 128 * I TO 127 + 128 * I:  'SELECT ADDRESSES
1040 IF 0 <= K - I * 128 AND K - I * 128 <= 64 THEN VB = K - I * 128 ELSE VB = 128 - (K - I * 128)
'TRINGLE VB GENERATOR
1050 VA = 64 - VB   'TRINGLE WAVE VA GENERATOR
1060 PI = 3.14159
1070 VC = 32 + 20 * SIN(2 * PI * K / 16384)   'MODULATING WAVE GENERATOR
1080 IF VC > VA THEN SI1 = 1 ELSE SI1 = 0
1090 IF SI1 = 1 THEN RA1 = RA1 + 1 ELSE RA1 = RA1
1100 SI4 = 1 - SI1
1110 IF VC < VA AND 64 <= K - I * 128 AND K - I * 128 <= 127 THEN RA4 = 1 + RA4 ELSE RA4 = RA4
1120 IF VC < VB THEN SI3 = 1 ELSE SI3 = 0
1130 IF SI3 = 1 THEN RA3 = RA3 + 1 ELSE RA3 = 0
1140 SI2 = 1 - SI3
1150 IF VC > VB AND 64 <= K - I * 128 AND K - I * 128 <= 127 THEN RA2 = 1 + RA2 ELSE RA2 = RA2
1160 IF 1 <= RA1 AND RA1 <= 2 THEN DA4 = 1 ELSE DA4 = 0  'DEAD TIME
1170 IF 1 <= RA2 AND RA2 <= 2 THEN DA3 = 1 ELSE DA3 = 0  'DEAD TIME
1180 IF 1 <= RA3 AND RA3 <= 2 THEN DA2 = 1 ELSE DA2 = 0  'DEAD TIME
1190 IF 1 <= RA4 AND RA4 <= 2 THEN DA1 = 1 ELSE DA1 = 0  'DEAD TIME
1200 IF 1 <= RA1 AND RA1 <= 12 THEN SA4 = 1 ELSE SA4 = 0  'AUXILIARY SIGNAL WIDTH
1210 IF 1 <= RA2 AND RA2 <= 12 THEN SA3 = 1 ELSE SA3 = 0  'AUXILIARY SIGNAL WIDTH
1220 IF 1 <= RA3 AND RA3 <= 12 THEN SA2 = 1 ELSE SA2 = 0  'AUXILIARY SIGNAL WIDTH
1230 IF 1 <= RA4 AND RA4 <= 12 THEN SA1 = 1 ELSE SA1 = 0  'AUXILIARY SIGNAL WIDTH
1240 S1 = SI1 - DA4: S2 = SI2 - DA3: S3 = SI3 - DA2: S4 = SI4 - DA1  'MAIN SWITCH COMMAND
1250 A = SA4 * 2 ^ 7 + SA3 * 2 ^ 6 + SA2 * 2 ^ 5 + SA1 * 2 ^ 4 + S4 * 2 ^ 3 + S3 * 2 ^ 2 + S2 * 2 ^ 1 + S1 * 2
^ 0
'   PRINT #1, S1; SA1; S2; SA2; S3; SA3; S4; SA4; VC; VA; VB; K; A
1260    IF K = U * 16 THEN
1270    U = U + 1
1280      IF TOTAL < 255.5 THEN
1290        IF TOTAL < 15.5 THEN
1300        PRINT #1, "00"; HEX$(TOTAL)
1320        ELSE
1330        PRINT #1, "0"; HEX$(TOTAL)
1350        END IF
1360      ELSE
1370      PRINT #1, HEX$(TOTAL)
1390      END IF
1400    TOTAL = 0
1420    PRINT #1, ":"; HEX$(K / (U - 1));
1430      IF K < 16 THEN
1440      PRINT #1, "000";
1450      ELSE
1460        IF K < 256 THEN
1470        PRINT #1, "00";
1480        ELSE
1490          IF K < 4096 THEN
1500          PRINT #1, "0";
1510          END IF
1520        END IF
```

```
1530      END IF
1540    PRINT #1, HEX$(K); "00";
1550    END IF
1560 TOTAL = TOTAL + A
1570    IF A < 15.5 THEN
1580    PRINT #1, "0"; HEX$(A);
1590    ELSE
1600    PRINT #1, HEX$(A);
1610    END IF
1620  NEXT K
1630  NEXT I
1640    IF TOTAL < 256 THEN
1650    PRINT #1, "0"; HEX$(TOTAL);
1660    ELSE
1670    PRINT #1, HEX$(TOTAL);
1680    END IF
1690 CLOSE
1700 END
```



Appendix 5.2: Control diagram of the True-PWM-Pole half-bridge three level capacitor clamping inverter.

Chapter 6. Operation of the Neutral-Point-Clamped (NPC) Inverter

Abstract: This Chapter explores the neutral potential stability of the Neutral-Point-Clamped (NPC) inverter. Steady state stability, dynamic state stability along with the stability under non-ideal conditions are studied. The analyses are verified by PSPICE simulations.

6.1. Sub-Harmonic PWM Modulation of the NPC Inverter

Fig. 6.1 shows the half bridge NPC inverter circuit. The output potential is connected to positive, zero and negative when S_1 and S_2, S_2 and S_3 or S_3 and S_4 are ON respectively. The principle of sub-harmonic PWM modulation is shown in Fig. 6.2. By intersecting a sinusoidal reference mod(t) with two vertically shifted triangle carriers, a three level voltage v_{AO} with sinusoidal envelop is obtained at the output, which is expressed by (6.1):

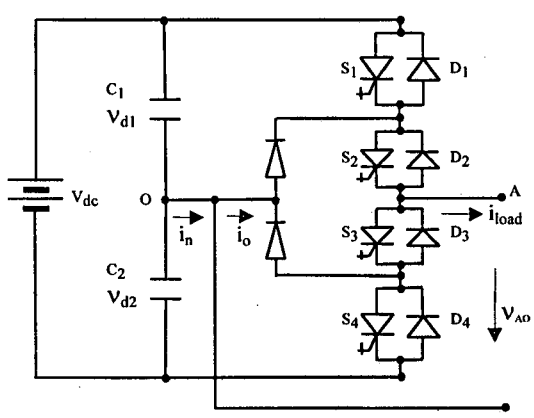


Fig. 6.1. Half bridge NPC inverter configuration.

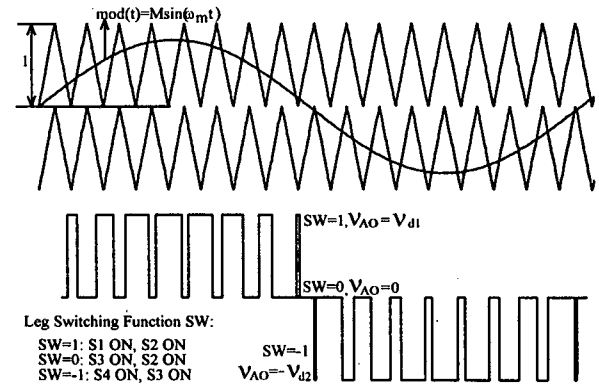


Fig. 6.2. Sub-harmonic PWM modulation for NPC inverter.

$$v_{AO} = \frac{(1+sw)sw}{2} v_{d1} - \frac{(sw-1)sw}{2} v_{d2} \tag{6.1}$$

(6.1) can be rearranged as (6.2):

$$v_{AO} = \frac{sw}{2}(v_{d1} + v_{d2}) + \frac{sw^2}{2}(v_{d1} - v_{d2}) \tag{6.2}$$

6.2. Neutral Potential Steady State Stability

Under steady state, $v_{d1}=v_{d2}=V_{dc}/2$, the output voltage v_{AO} is simplified to (6.3):

$$v_{AO} = sw\frac{V_{dc}}{2} \tag{6.3}$$

where the leg switching function sw can be given in Fourier form by (6.4):

$$sw = \sum_{k} A_k sin(k\omega_m t) \tag{6.4}$$

$$k \in K = 1,3,5,...$$

where A_k is the amplitude of the kth order harmonic, ω_m is the fundamental frequency. Then the load current i_{load} is written as (6.5):

$$i_{load} = \frac{V_{dc}}{2}\sum_{k}\frac{A_k}{Z_k}sin(k\omega_m t - \theta_k) \tag{6.5}$$

$$k \in K=1,3,5,...$$

where $Z_k \angle \theta_k$ is load impedance at harmonic order of k.

On the other hand, the current flowing out of the neutral potential i_n is given by (6.6):

$$i_n = i_o - i_{load} = i_{load}(1 - sw^2) - i_{load} = -sw^2 i_{load} \tag{6.6}$$

Substitution from (6.4) and (6.5) in (6.6), i_n is further expressed by (6.7):

$$i_n = \frac{V_{dc}}{4}\{\sum_k\sum_l A_k A_l \cos[(k-l)\omega_m t] - \sum_k\sum_l A_k A_l \cos[(k+l)\omega_m t]\}\sum_k \frac{A_k}{Z_k} sin(k\omega_m t - \theta_k) \tag{6.7}$$

$$k, l \in K, L = 1,3,5...$$

When the neutral point potential is concerned, only the DC component in i_n is of interest, which is given by (6.8):

$$i_{n.dc} = \int_0^{2\pi} i_n d(\omega_m t) \tag{6.8}$$

From perpendicular property, integration (6.8) equals zero. *This result implies the neutral point potential will be stable under normal sub-harmonic modulation, because of the zero current flowing from the neutral potential during the fundamental cycle.*

6.3. Self-Balancing under Ideal Condition

When dynamic state is concerned, suppose that the neutral potential diverges from zero after a perturbation, the output voltage will then be given by (6.2). While the first part represents the steady state voltage output, the second part of this expression, represents the output voltage variation ΔV_{AO} resulted from the neutral potential drift, which is rewritten in (6.9):

$$\Delta v_{AO} = \frac{sw^2}{2}(v_{d1} - v_{d2}) \tag{6.9}$$

Substitution from (6.4) in (6.9), Δv_{AO} can be detailed by (6.10):

$$\Delta v_{AO} = \frac{v_{d1} - v_{d2}}{4}\{\sum_k \sum_l A_k A_l \cos[(k-l)\omega_m t] - \sum_k \sum_l A_k A_l \cos[(k+l)\omega_m t]\} \tag{6.10}$$

$$k, l \in K, L = 1,3,5\ldots$$

From (6.10), even numbered harmonics appears at the output after the perturbation. In the meanwhile, the load current response to this variation, recorded as Δi_{load}, is given by (6.11):

$$\Delta i_{load} = \frac{v_{d1} - v_{d2}}{4}\{\sum_k \sum_l \frac{A_k A_l}{z_{k-l}} \cos[(k-l)\omega_m t - \theta_{k-l}] - \sum_k \sum_l \frac{A_k A_l}{z_{k+l}} \cos[(k+l)\omega_m t - \theta_{k+l}]\} \tag{6.11}$$

$$k, l \in K, L = 1,3,5\ldots$$

where $z_j \angle \theta_j$ is the load impedance at harmonic order of j.

On the other hand, the current variation flowing out of the neutral potential is inferred to be given by (6.12):

$$\Delta i_n = \Delta i_o - \Delta i_{load} = \Delta i_{load}(1 - sw^2) - \Delta i_{load} = -sw^2 \Delta i_{load} \tag{6.12}$$

where Δi_o is the neutral path current variation. When the neutral point potential variation is especially concerned, only the DC component of Δi_n is of interest, which is given by (6.13):

$$\Delta i_{n.dc} = \int_0^{2\pi} \Delta i_n d(\omega_m t) \tag{6.13}$$

Based on perpendicular property, $\Delta i_{n.dc}$ can be simplified to (6.14):

$$\Delta i_{n.dc} = \frac{v_{d2} - v_{d1}}{16} \{ \sum_k \sum_l \frac{(A_k A_l)^2}{z_{k-l}} \cos\theta_{k-l} + \sum_k \sum_l \frac{(A_k A_l)^2}{z_{k+l}} \cos\theta_{k+l} \} \tag{6.14}$$

$$k, l \in K, L = 1,3,5\ldots$$

(6.14) demonstrates that the sign of $\Delta i_{n.dc}$ is always dependent on the sign of $(v_{d2} - v_{d1})$, the value of which is further dependent on the part within the bracket. This result means that after perturbation, a corresponding variation arises simultaneously in the current flowing out of the neutral point, which rejects the perturbation.

From (6.14), the following conclusions can be drawn concerning the self-balancing ability in the half-bridge NPC inverter under ideal condition:

- Self-balancing exists so long as the load is not pure reactive ($\theta_{k-l} \neq \pm\frac{\pi}{2}, \theta_{k+l} \neq \pm\frac{\pi}{2}$).
- Time constant of the dynamics is dependent on the following components:
    1. Modulation index: The higher the longer.
    2. Load impedance amplitude and angle: The greater the longer.
    3. DC link capacitances: The larger the longer.

Fig. 6.3 illustrates the mathematical process conducted above. The output voltage response (Δv_{AO}) to the perturbation (v_{d1}-v_{d2}) leads to load current variation (Δi_{load}), which when reflected back to the neutral potential (Δi_n), rejects the original perturbation. So that the neutral potential is kept constant.

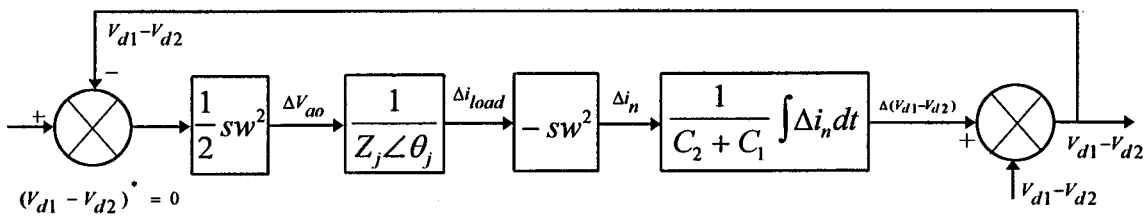


Fig. 6.3. Illustration of the self-balancing mechanism in the NPC inverter.

The self balancing ability has been verified by PSPICE simulation. Refer to Fig. 6.1 and Fig. 6.2, the circuit specifications and parameters for the simulation are given in Table 6.1. The simulation result is shown in Fig. 6.4. For a initial state drift of 100V, the neutral potential recovers to its steady state after about 400mS. The dynamics exhibits typical one-order system characteristic which is similar to the case of the capacitor clamping inverter. Appendix 6.1 gives the PSPICE program for this simulation.

Table 6.1. Specifications/parameters for PSPICE simulation of the self-balancing under ideal condition

DC link voltage	V_{dc}=800 V	Filter parameters	L_f=0.1mH C_f=4uF	Operation frequency	f_c=10kHz	Modulation index	M=0.4
DC link capacitances (uF)	C_1=4000 C_2=4000	Load resistance	R_o=1Ω	Fundamental frequency	f_m=100Hz	Initial voltages (V)	v_{d1}=300 v_{d2}=500

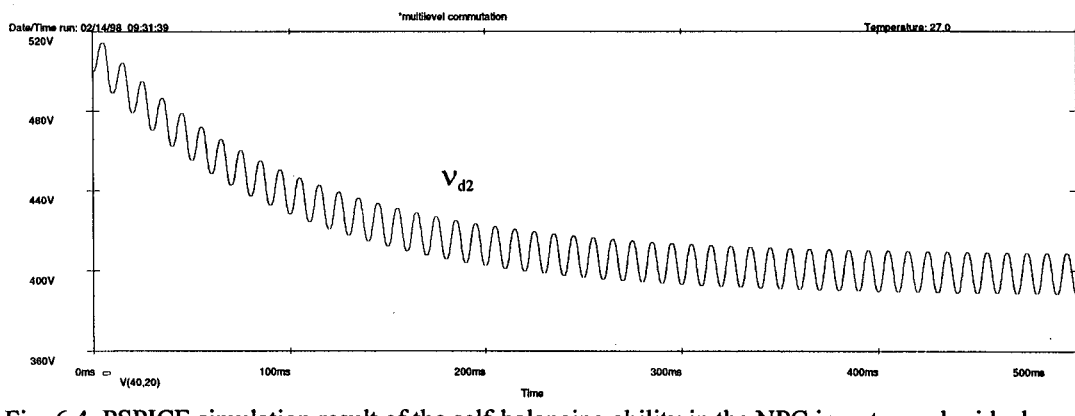


Fig. 6.4. PSPICE simulation result of the self-balancing ability in the NPC inverter under ideal condition.

6.4. Self-Balancing under Non-Ideal Condition

Analysis in section 6.3 has been conducted neglecting any circuit non-ideals which are always inevitable in practical circuit operation. For the half bridge NPC circuit concerned, asymmetrical charging/discharging during the positive/negative output voltage semicycle will lead to neutral potential drift. Such asymmetry can most probably be resulted from gating/switching diversities or load transience etc.

In an extreme case, DC component involved in the sinusoidal reference causes consistant charging/discharging unbalance over the neutral potential. However, while the neutral potential drifts away from zero, the self-balancing mechanism is activated simultaneously which tends to recover the drifted neutral potential. *Up to certain extent depending on the load properties, modulation index, DC link capacitances etc., the neutral point potential will be stabilized at an new operation point other than zero where new balance is reached.* This conclusion has been verified with PSPICE simulations. Circuit specifications and parameters for the simulations are shown in Table 6.2. Simulation results are shown in Fig. 6.5 and Fig. 6.6, which corresponds to DC biases of 0.5V and –0.5V to the reference respectively (carrier amplitude 10V, reference peak 4V). For the initial voltages of 400V across C_1 and C_2, v_{d1} and v_{d2} are eventually balanced at 280V and 520V after the first order dynamics, which means a neutral potential drift of 120V. PSPICE program for this simulation is listed in Appendix 6.2.

Similar to the case of the capacitor clamping inverter, dead time does not affect the self-balancing ability of the neutral potential. The influence in one semicycle is cancelled by the same influence in the other semicycle.

Table 6.2. Circuit specifications/parameters for simulation of self-balancing under non-ideal condition

DC link voltage	V_{dc}=800 V	Filter parameters	L_f=0.1mH C_f=4uF	Operation frequency	f_c=10kHz	Modulation index	M=0.4
DC link capacitances (uF)	C_1=4000 C_2=4000	Load resistance	R_o=1Ω	Fundamental frequency	f_m=100Hz	Initial voltages (V)	v_{d1}=400 v_{d2}=400

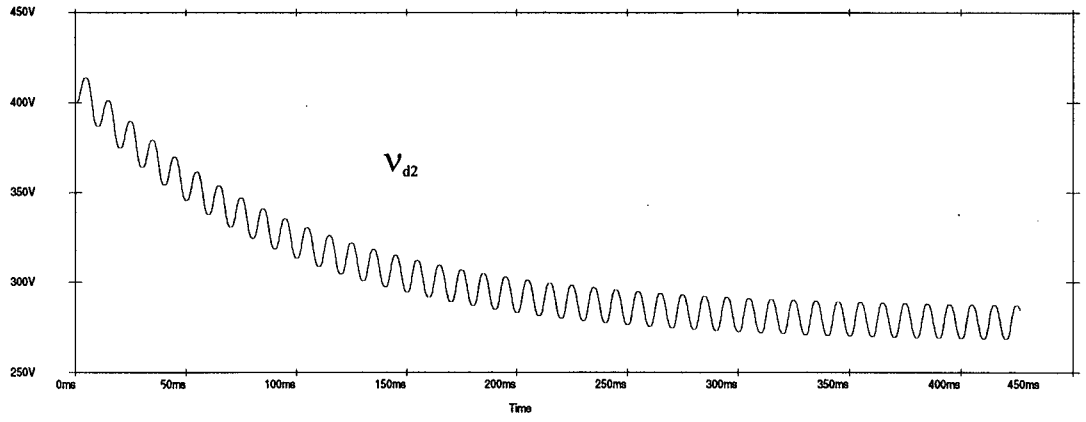


Fig. 6.5. Simulation result of the self-balancing ability under non-ideal condition, positive bias 0.5V.

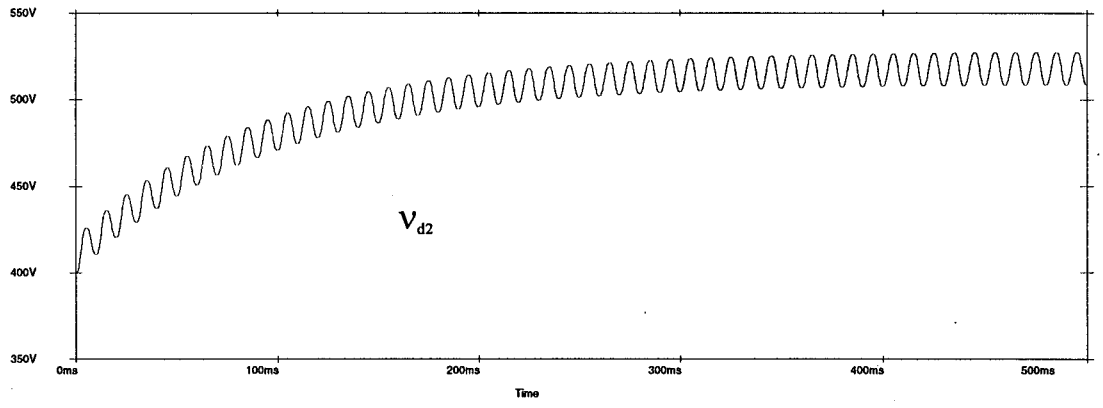


Fig. 6.6. Simulation result of the self-balancing ability under non-ideal condition, negative bias 0.5V.

6.5. Self-Balancing in Three Phase NPC Inverter System

For a three phase system, actually the same mathematical procedure as the half bridge case can be followed except for that the load neutral potential now must be included to the analysis. With a primitive perturbation at the neutral potential, a variation in the current flowing into the neutral potential will arise simultaneously, which is given by (6.15) [60]:

$$\Delta i_{n.dc} = \frac{3(v_{d2} - v_{d1})}{16}\left\{\sum_k \frac{\cos\theta_k}{Z_k}\left(\sum_l 2A_l A_{k+l} - \sum_l^{k-l} A_l A_{k-l}\right)^2\right\} \tag{6.15}$$

$k \in K=2,4,8,10,14,...$ $l \in L=1,3,5...$

From (6.15), for any perturbation of the neutral potential, the resultant neutral point current variation always has an appopriate sign that rejects the original perturbation and keeps the neutral potential from drift.

6.6. Conclusions

1. Neutral potential of the NPC inverter is self-balancing under the sub-harmonic PWM modulation with non-pure reactive load. The time constant of the first order dynamics is dependent on the load properties, modulation index and the DC link capacitances etc.
2. Depending on the extent of asymmetry, typically resulted from gating or switching mismatches, the neutral potential will be balanced to an new operation point other than zero, due to the self-balancing mechanism counteracting such asymmetry once it arises.

Appendix 6.1. PSPICE simulation program for self-balancing under ideal condition

```
*Self-balancing under ideal condition
*triggering signals generating
v1 1 0 pulse (0 10 .1u 50u 50u .1u 100u)
e2 2 0 value {v(1)-10}
vmod 5 0 sin(0 4 100 0 0 0)
esu1 6 0 table {v(1)-v(5)} (-1e-2,10) (1e-2,0)
esd1 10 0 table {v(6,0)} (2,10) (3,0)
esu2 7 0 table {v(2)-v(5)} (-1e-2,10) (1e-2,0)
esd2 11 0 table {v(7,0)} (2,10) (3,0)

*main circuit
su3 16 24 6 0 sswitch
ds3 24 17 dmod
du3 17 16 dmod
su4 17 25 7 0 sswitch
dsu4 25 18 dmod
du4 18 17 dmod
sd1 18 26 10 0 sswitch
dsd1 26 19 dmod
dd1 19 18 dmod
sd2 19 27 11 0 sswitch
dsd2 27 20 dmod
dd2 20 19 dmod
dc1 40 17 dmod
dc2 19 40 dmod

*device models
.model sswitch vswitch(ron=0.01 roff=1e6 von=4 voff=2)
.model dmod d(is=2e-15 bv=1500 tt=0 cjo=1p)

*DC link initial voltages
vdc 16 20 800
c2 16 40  4000u ic=300
c22 40 20 4000u ic=500

*load parameters
lload 18 41 .1m
rload 41 40 1
cload 41 40 4u

.tran 2u 600m 0 2u uic
.options vntol=1m itl4=100 abstol=1m reltol=0.1 itl5=0
.probe v(40,20) i(dc1) i(dc2)
.end
```

Appendix 6.2. PSPICE simulation program for self-balancing under non-ideal condition

```
*PSPICE simulation under non-ideal condition
*triangle carriers and sinusoidal reference
v1 1 0 pulse (0 10 .1u 50u 50u .1u 100u)
e2 2 0 value {v(1)-10}
vmod 5 0 sin(0 4 100 0 0 0)
*sinusoidal reference bias
erro 42 0 value {-0.5}
*triggering signals generating
esu1 6 0 table {v(1)-v(5)-v(42)} (-1e-2,10) (1e-2,0)
esd1 10 0 table {v(6,0)} (2,10) (3,0)
esu2 7 0 table {v(2)-v(5)-v(42)} (-1e-2,10) (1e-2,0)
esd2 11 0 table {v(7,0)} (2,10) (3,0)

*main circuit
su3 16 24 6 0 sswitch
ds3 24 17 dmod
du3 17 16 dmod
su4 17 25 7 0 sswitch
dsu4 25 18 dmod
du4 18 17 dmod
sd1 18 26 10 0 sswitch
dsd1 26 19 dmod
dd1 19 18 dmod
sd2 19 27 11 0 sswitch
dsd2 27 20 dmod
dd2 20 19 dmod
dc1 40 17 dmod
dc2 19 40 dmod

*device models
.model sswitch vswitch(ron=0.01 roff=1e6 von=4 voff=2)
.model dmod d(is=2e-15 bv=1500 tt=0 cjo=1p)

*DC link initial voltages
vdc 16 20 800
c2 16 40  4000u ic=400
c22 40 20 4000u ic=400

*load parameters
lload 18 41 .1m
rload 41 40 1
cload 41 40 4u

.tran 2u 600m 0 2u uic
.options vntol=1m itl4=100 abstol=1m reltol=0.1 itl5=0
.probe v(40,20) i(dc1) i(dc2)
.end
```

Chapter 7. True-PWM-Pole Neutral-Point-Clamped (NPC) Inverter

Abstract: This chapter introduces a transformer connection True-PWM-Pole NPC inverter. After a brief review of the existing work, the proposed circuit and its operation are discussed. The True-PWM-Pole and the ARCPI are then further extended to the diode clamping multilevel inverter (M>3). Experimental results from a 3kW half bridge True-PWM-Pole NPC inverter are given finally.

7.1. Review of the Existing Work

Literature review shows that several previous publications have associated the NPC inverter with soft switching. Earlier work may be traced back to the thyristor times when auxiliary network must be established to assist the turn-off of the thyristor switches. Fig. 7.1 shows the thyristor three state inverter (NPC) assisted by the McMurray commutation network [33], which can be regarded as zero current switching NPC inverter in the present meaning. Auxiliary thyristors A_1 and A_2 assist the main thyristors S_1 and S_3 while A_3 and A_4 assist S_2 and S_4. However, auxiliary thyristors A_1 and A_4 have to block the whole DC link voltage, rather than half of it as the main thyristors do.

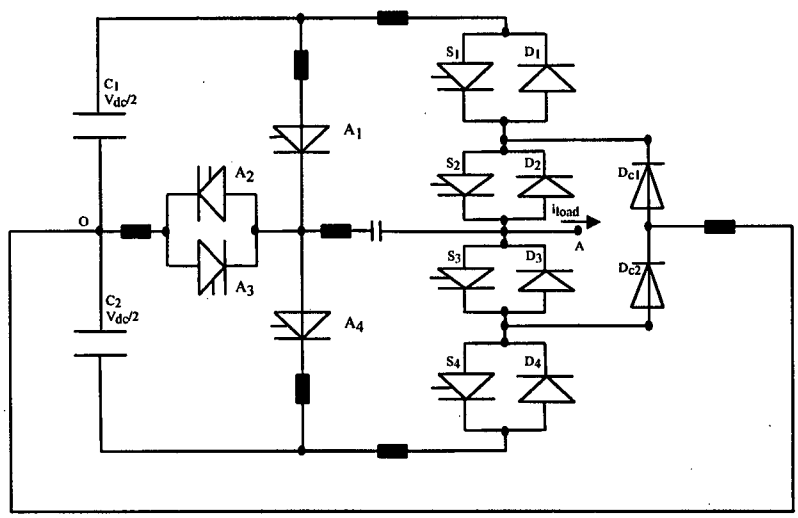


Fig. 7.1. Circuit diagram of the three state thyristor inverter.

Besides zero current switching, both resonant DC link [142] and resonant pole [143] zero voltage switching methods have been considered for the NPC inverter. In the ARCPI NPC inverter [143], as shown in Fig. 7.2, A_1 and A_2 assist the commutations of S_3 and S_1, while A_3 and A_4 assist S_4 and S_2. C_{r23} serves as snubbing capacitor for the center main switches S_2 and S_3. All the auxiliary switches A_1-A_4, however, have to see 3/4 of the DC link voltage, rather than ½ by the main switches.

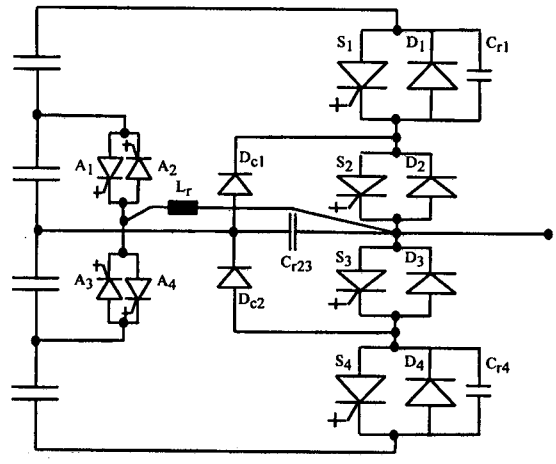


Fig. 7.2. Circuit diagram of the ARCPI NPC inverter.

Note that when the NPC structure is utilized for insulated DC/DC conversion, soft switching has been successfully achieved [144] [145] which promises wide application in high voltage area. The operation of which resembles the phase-shifted resonant bridge [103].

7.2. Proposed Circuit Configuration

The proposed transformer connection True-PWM-Pole NPC inverter circuit is shown in Fig. 7.3, which consists of the NPC main inverter circuit and two auxiliary branches. The first auxiliary branch (S_{a1}, S_{a3}) assists the commutation of the first switching cell (S_1, S_3) and forms the first True-PWM-Pole; whereas the second auxiliary branch (S_{a2}, S_{a4}) assists the commutation of the second switching cell (S_2, S_4) and forms the second True-PWM-Pole.

Provided that the NPC neutral potential is stable, and in particular, the coupling between the two poles can be neglected, the operation of the two True-PWM-Poles are then actually independent from each other and each pole works as in the two level case.

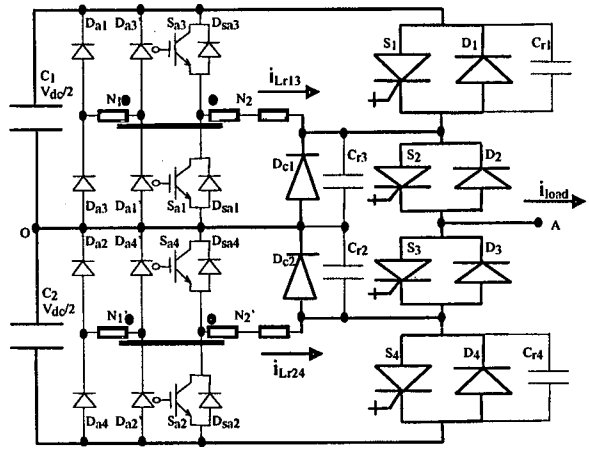


Fig. 7.3. The proposed True-PWM-Pole NPC inverter circuit.

7.3. Circuit Operation

According to the switching state of the main NPC inverter shown in Table 7.1, when the first pole is active, the second pole will be at rest (S_2 ON, S_4 OFF and $v_{cr4}=V_{dc}/2$, $v_{cr2}=0$). Four commutation processes can hence be distinguished:

Table 7.1. Switching State of the main NPC Inverter

Switching State / Output Voltage V_{AO}	S_1	S_2	S_3	S_4
$V_{dc}/2$	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF
$-V_{dc}/2$	OFF	OFF	ON	ON

(a) Positive load current, $D_{c1}+S_2$ to S_1+S_2 commutation;

(b) Positive load current, S_1+S_2 to $D_{c1}+S_2$ commutation;

(c) Negative load current, D_2+D_1 to S_3+D_{c2} commutation;

(d) Negative load current, S_3+D_{c2} to D_2+D_1 commutation.

For simplicity, only commutation details for processes (c) and (d) are detailed in the following. For which the next assumptions are made first:

(a) NPC neutral potential is stable during normal operation. Load current is constant during the commutation interval.

(b) Main switch turn-off and auxiliary switch turn-on happen at the same instant. Main switch turn-on signal is released when the detected voltage from the voltage monitor installed for

each main switch declines to zero. Auxiliary switch conduction duration covers the whole commutation interval.

(c) Transformer ratio is set to ensure the pole voltage swinging to the rail value during the commutation, as discussed in Chapter 2.

Refer to the relevant theoretical waveforms shown in Fig. 7.4 and the operation step diagrams shown in Fig. 7.5 and Fig. 7.6, the commutations proceed in the following steps.

Process(c): Negative load current, D_2+D_1 to S_3+D_{c2} commutation:

Step1 (t_0-t_1): Circuit steady state. D_2+D_1 carries the load current. Output voltage V_{AO}=V_{dc}/2.

Step2 (t_1-t_2): Turn on S_{a1} and turn off S_1 at t_1 simultaneously, which causes the conduction of D_{a1} and D_{a1}', magnetization of L_{r13} and current decreasing in D_1. Voltage of kV_{dc}/2 is reflected on N_2 setting-up a voltage source of V_{dc}(1-k)/2 forcing the resonance followed.

Step3 (t_2-t_3): D_1 is blocked at t_2 when i_{lr13} rises to the load current level. After which C_{r1} is charged while C_{r3} is discharged.

Step4 (t_3-t_4): C_{r1} is fully charged to V_{dc}/2 at t_3. D_{c1} begins conduction. And S_3 gating signal is released.

Step5 (t_4-t_5): L_{r13} current reaches load current at t_4, after which S_3+D_{c2} begins carrying current.

Step 6 (t_5-t_6): Current through/voltage across N_2 extinguish at t_5. S_3+D_{c2} carries the full load current. S_{a1} gating signal can be withdrawn. Circuit then reaches another steady state. The output voltage V_{AO}=0.

Process(d): Negative load current, S_3+D_{c2} to D_2+D_1 commutation:

Step7 (t_6-t_7): Turn on S_{a3} and turn off S_3 at t_6 simultaneously which causes conduction of D_{a3} and D_{a3}'. Voltage of kV_{dc}/2 is therefore established on N_2 resulting in a voltage source of V_{dc}(1-k)/2 forcing the resonance. Load current moves from S_3+D_{c2} to D_2 charging C_{r3} and discharging C_{r1}.

Step8 (t_7-t_8): C_{r1} gets fully discharged at t_7 after which current flowing in C_{r1} and C_{r3} transfers immediately to D_1. S_1 gating signal is then released.

Step9 (t_8-t_9): Voltage across/current through L_{r13} dies out at t_8, from which instant D_2+D_1 carries the full load current. S_{a3} gating signal can then be withdrawn. Circuit arrives at the original steady state. Output voltage $V_{AO}=V_{dc}/2$.

To summarize, in the proposed circuit, the main switches work with soft turn-on (zero voltage switching) and snubbed turn-off, while the main diodes (freewheeling and clamping) work with zero current turn-off and zero voltage turn-on. Unlike the case in the conventional snubber where the snubbing capacitance is limited by the snubber loss, the parallel capacitance in the present case can be optimized for the switch turn-off loss. However, the main diode is characteristic of snap-on which is similar to the system assisted with conventional snubber. The loss accrued in such process is dependent on the wiring inductance and the diode forward recovery property.

In the meantime, all the auxiliary devices including both switches and diodes work with soft turn-off (zero current switching). Moreover, despite the bridge configuration of the auxiliary devices, the turn-on of these devices are actually snubbed by the resonant inductor. Upon turn-on of an auxiliary switch, the opposite freewheeling diode carries no current and therefore its reverse recovery contribution can be neglected. Transformer excitation are reset to zero after each commutation and causes no magnetic accumulation. In particular, the extra freedom in synthesizing the auxiliary voltage source for the resonance offered by the transformer greatly simplifies the control.

Designing of the auxiliary branches has been discussed in Chapter 2.

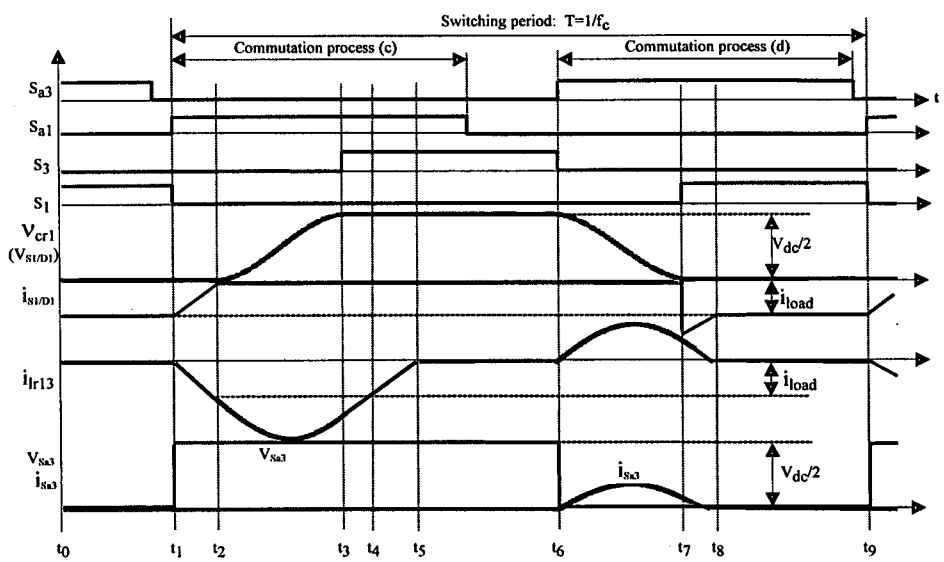
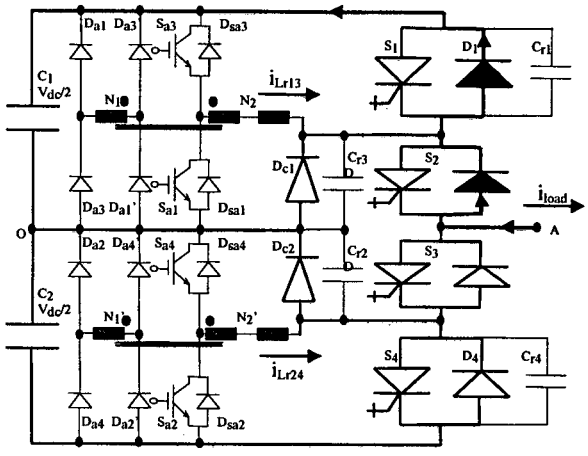
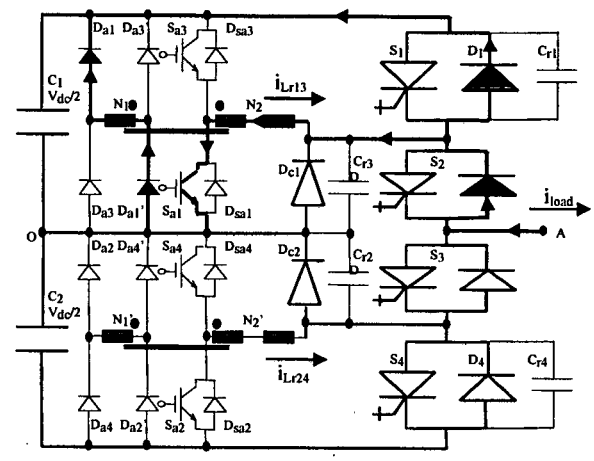


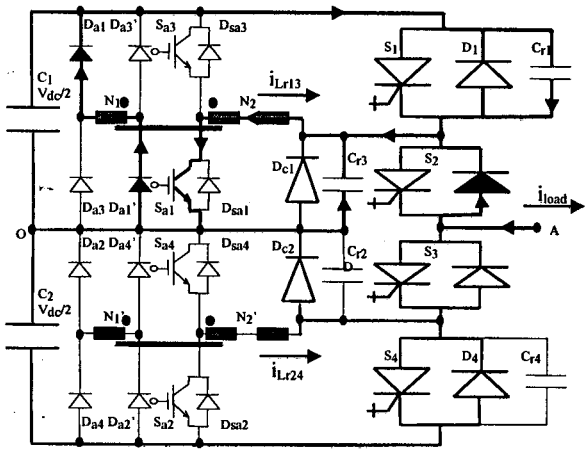
Fig. 7.4. Switching sequence of the main and the auxiliary switches and the relevant waveforms.



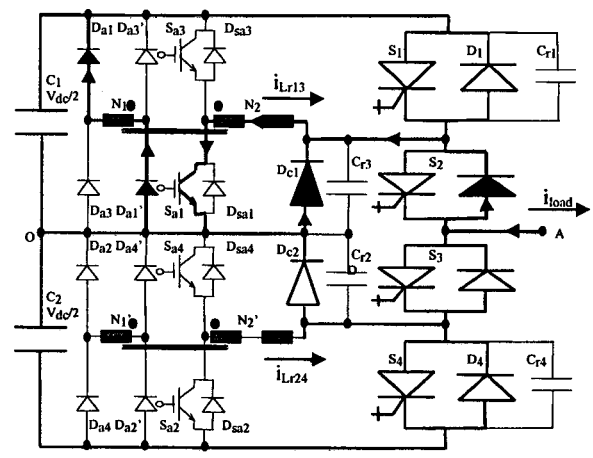
step 1: t_o-t_1 (step 9: t_8-t_9)



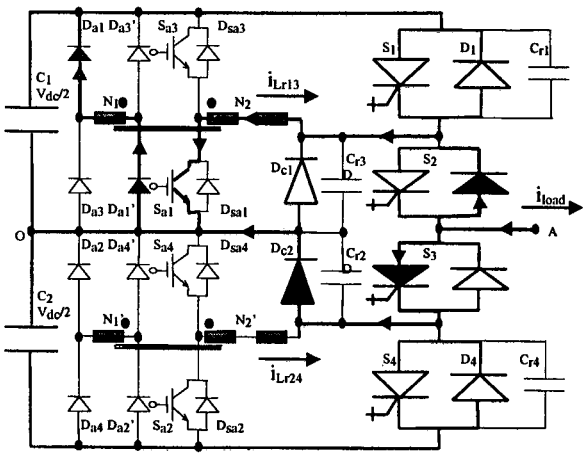
step 2: t_1-t_2



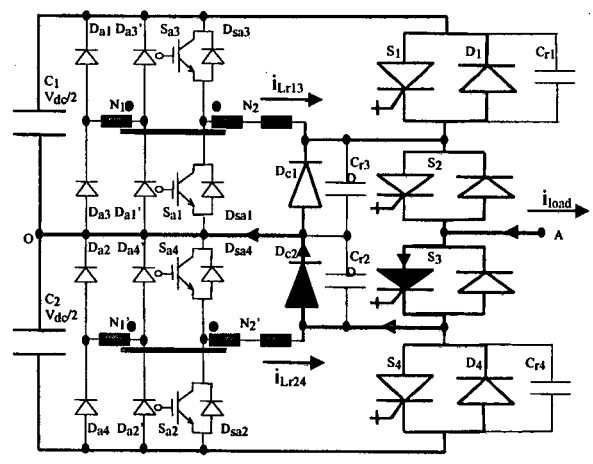
step 3: t_2-t_3



step 4: t_3-t_4

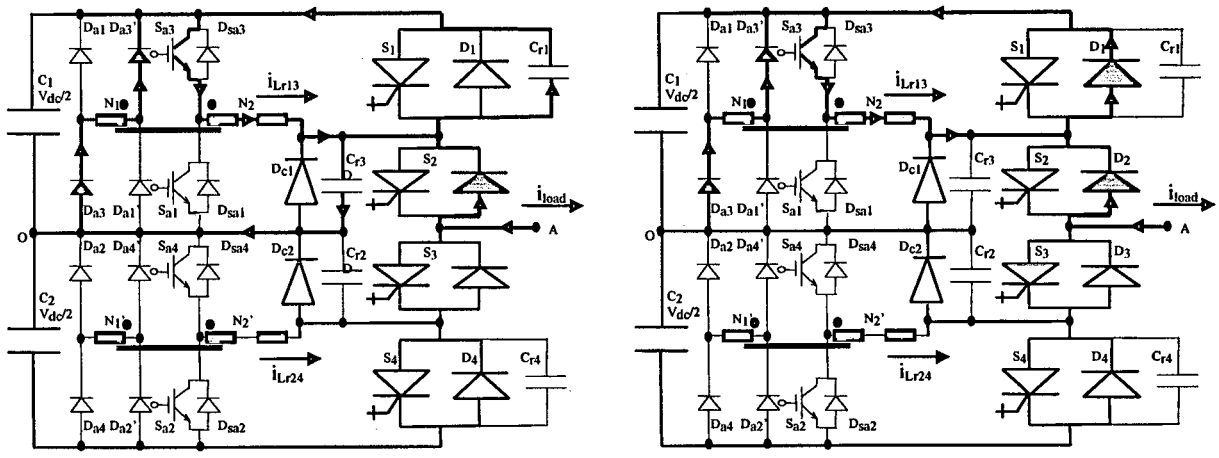


step 5: t_4-t_5



step 6: t_5-t_6

Fig. 7.5. Operation step diagrams for commutation process (c) D_1+D_2 to S_3+D_{C2} commutation.



step 7: t_6-t_7 step 8: t_7-t_8

Fig. 7.6. Operation step diagrams for commutation process (d) S_3+D_{C2} to D_1+D_2 commutation.

7.4. Topologies for Multilevel Case (M>3)

Zero voltage switching for multilevel diode clamping inverter (M >3) can be achieved by installing an auxiliary network based on either the whole multilevel leg or each two level switching cell of it.

7.4.1. Zero Voltage Switching on the Per-Leg Basis

Both True-PWM-Pole and ARCP methods are applicable for multilevel case. For the True-PWM-Pole method, the auxiliary branch is established by the same multilevel leg as the main leg, as shown in Fig. 7.7, where the commutations of S_1, S_2, S_3, S_1', S_2', and S_3' are assisted by S_{a1}, S_{a2}, S_{a3}, S_{a1}', S_{a2}' and S_{a3}' respectively and three True-PWM-Poles are formed. Transformer ratio should be set less than 1/6 to ensure zero voltage switching.

In the case of ARCP method, the auxiliary branch can be established by the sub-circuit of a M+1 level leg, as shown in Fig. 7.8. The commutations of S_1, S_2, S_3, S_1', S_2', and S_3' are assisted by S_{a1}, S_{a2}, S_{a3}, S_{a1}', S_{a2}' and S_{a3}' respectively and three ARCP poles are formed. Each main switching cell and its corresponding auxiliary switching cell work in the same way as in the two level case.

In this approach, all the poles share the same resonant inductor and transformer. However, resonant current always flows through three devices in series. In addition, all the inner auxiliary switches are indirectly clamped as the main switches.

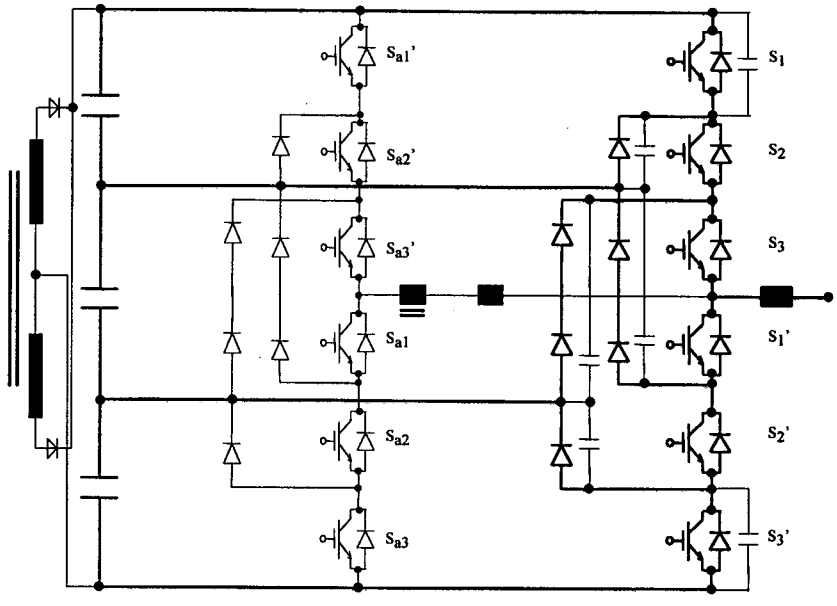


Fig. 7.7. A transformer connection True-PWM-Pole four level diode clamping inverter leg. The auxiliary switches block 1/3 of the DC link voltage, same as that by the main switches.

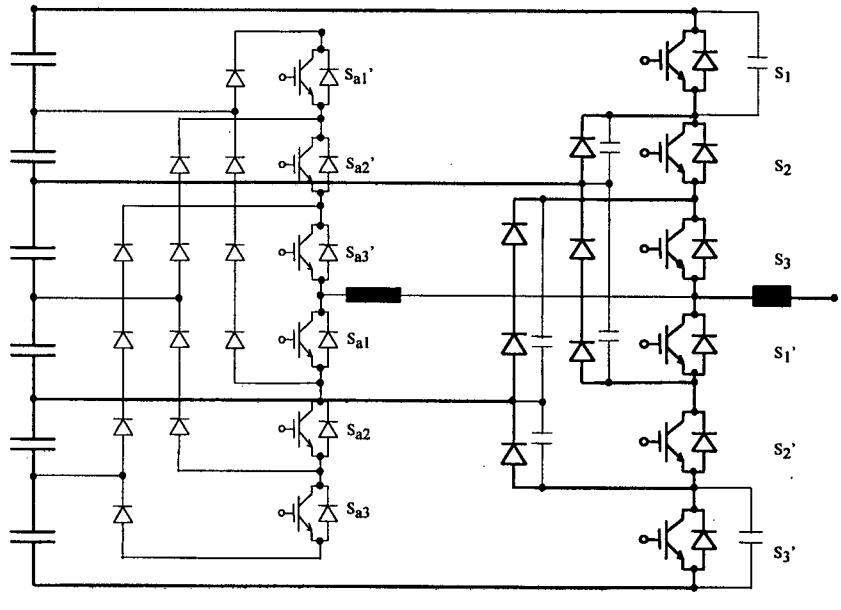


Fig. 7.8. An ARCP four level diode clamping inverter leg. The auxiliary switches block 1/6 of the DC link voltage, half of that by the main switches.

7.4.2. Zero Voltage Switching on the Per-Cell Basis

Zero voltage switching of the diode clamping multilevel inverter can also be achieved based on each two level switching cell with True-PWM-Pole or ARCPI methods. In this approach, individual two level auxiliary branch is installed for each switching cell, as shown in Fig. 8. 11 for the case of True-PWM-Pole and Fig. 8.12 for the case of ARCP.

In comparison with the previous approach, each pole has its own resonant inductor. However, resonant current flows through only one auxiliary switch, which avoids the problem of indirect clamping in the auxiliary network.

7.5. Experimentation

The experimental IGBT half bridge prototype, as shown in Fig. 7.9, employs a sinusoidal modulating signal and two vertically shifted carriers for the main circuit modulation, as discussed in Chapter 6. The neutral potential is not actively controlled and instead is stabilized counting on the inherent self-balancing mechanism. Specifications and parameters are given in Table 7.2:

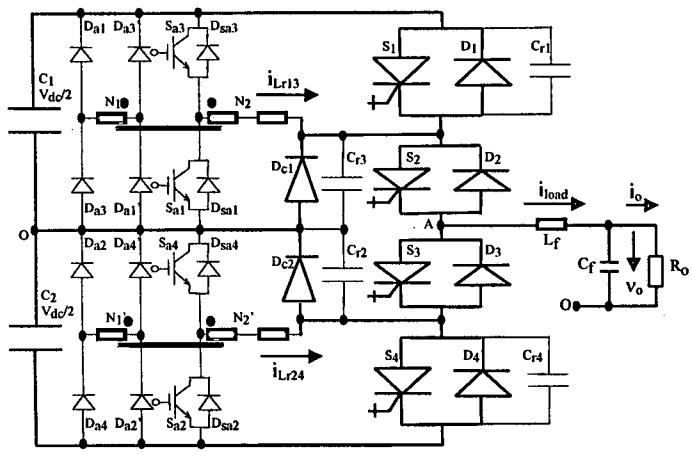


Fig. 7.9. Circuit diagram of the 3kW half bridge laboratory prototype.

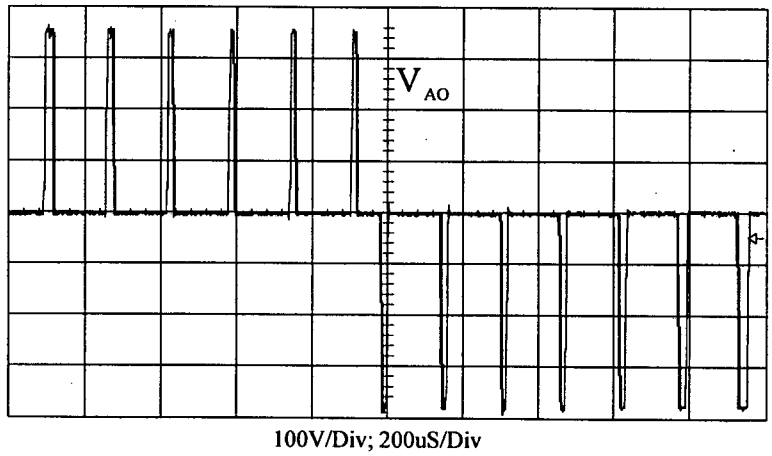
Table 7.2. Prototype specifications and parameters

Specifications	P_o=3.2kW, V_{dc}=720V, $V_{o.rms}$=140V, $I_{o.rms}$=22.8A
Parameters	k=0.45, T=153.6uS, C_r=0.1uF, L_r=15uH, M=0.62

Four IGBT modules (SKM50GB123D,1200V/50A) are employed as the main and auxiliary switches. Eight ultra-fast HFA30TA60C (600V/30A) diodes work as the auxiliary diodes. Two storage capacitors C_1 and C_2 each rated at 360V/3300uF form the center tap. Output second order filter: L_f=6.5mH, C_f=12uF. For each main switch, a zero voltage detecting circuit as discussed in Chapter 5 is installed.

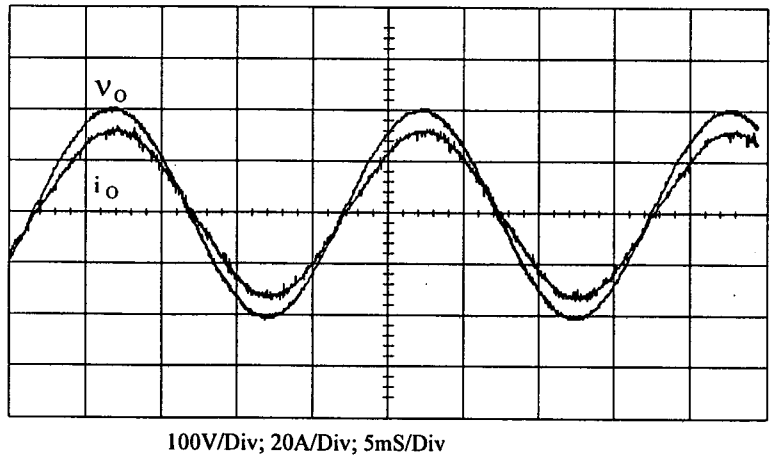
Under the given conditions, the maximum commutation duration is calculated to be 9.4uS. The width of the auxiliary switch gating signal is set at 12uS, and the Minimum/Maximum pulse widths are set at 14.4uS and 96uS respectively. Dead time of 2.4uS is introduced between the gating signals for the two main switches in each switching cell. Gating signals for the main and auxiliary switches are created in EPROM 27256M. Appendix 7.1 lists the BASIC program.

Fig. 7.10 shows the three level output of the inverter. Fig. 7.11 shows the output voltage and current after filtering. Fig. 7.12(a)- (d) show the typical four commutation processes.



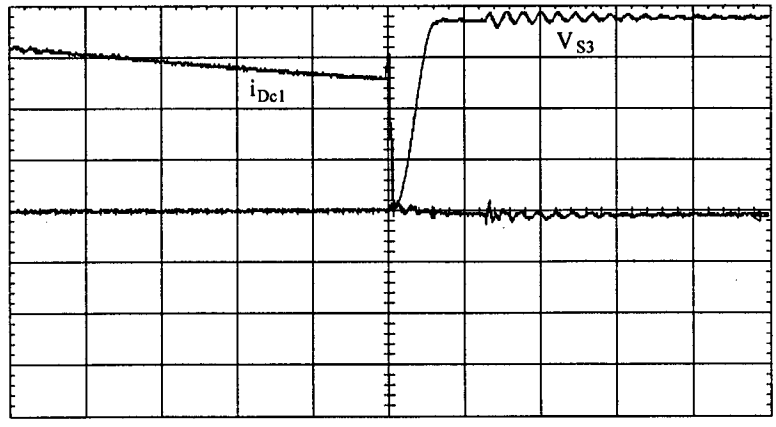
100V/Div; 200uS/Div

Fig. 7.10. The three level output of the NPC inverter.



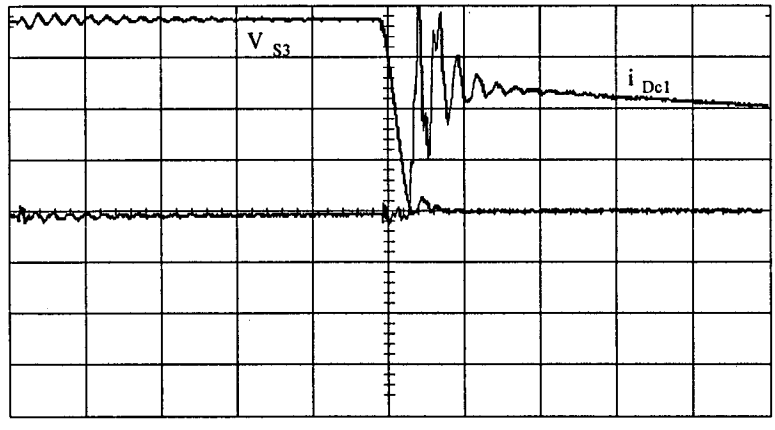
100V/Div; 20A/Div; 5mS/Div

Fig. 7.11. Output voltage/current after filtering.



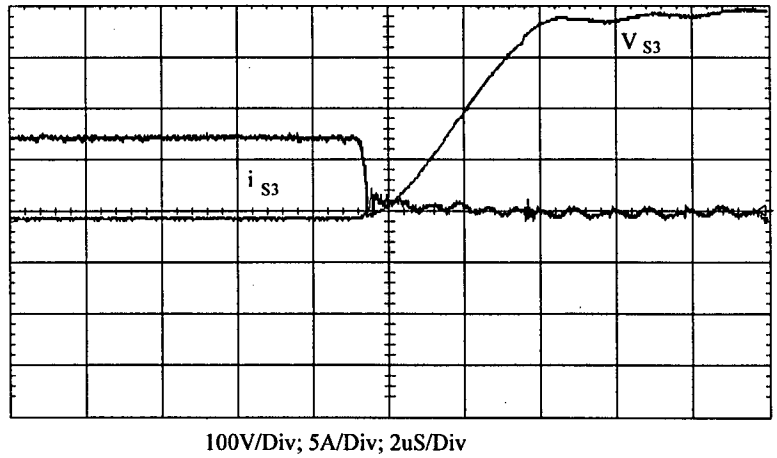
100V/Div; 5A/Div; 10uS/Div

(a) Positive load current , D_{c1} to S_1 commutation



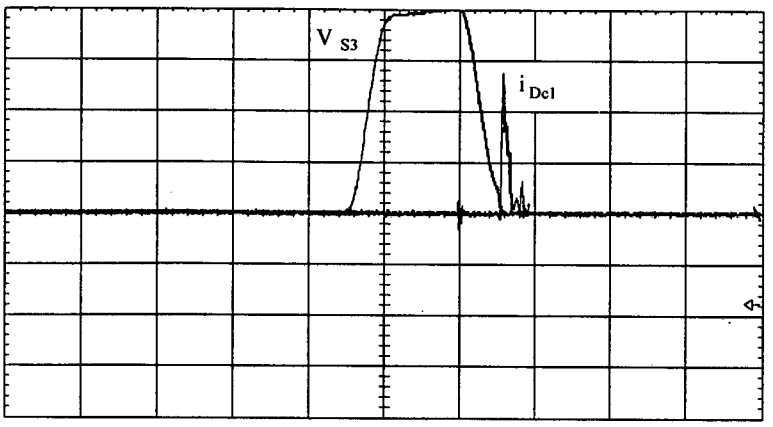
100V/Div; 5A/Div; 10uS/Div

(b) Positive load current, S_1 to D_{c1} commutation



100V/Div; 5A/Div; 2uS/Div

(c) Negative load current, S_3 to D_1 commutation

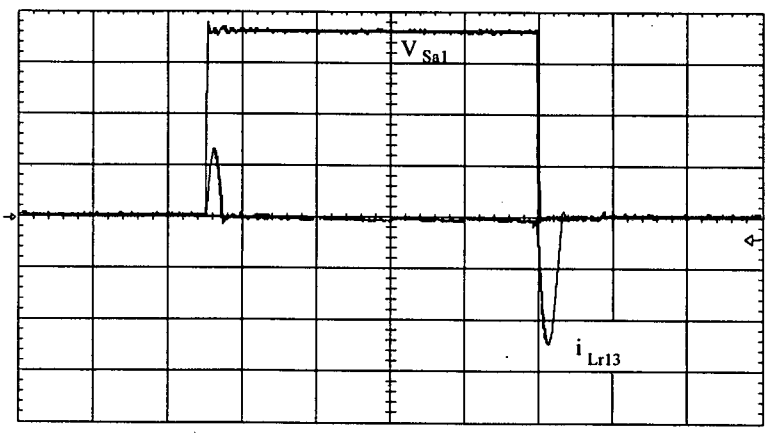


100V/Div; 5A/Div; 10uS/Div

(d) Negative load current, D_1 to S_3 commutation

Fig. 7.12. Four typical commutation processes of the first resonant pole.

Fig. 7.13 shows the auxiliary switch voltage and resonant inductor current waveforms at load current i_{load} =8A. For switch to diode commutation, with a theoretical commutation duration of 4.6uS and a resonant peak current of 17.5A, the experimental values are 4.1uS and 14.5A respectively. For diode to switch commutation, with a theoretical commutation duration of 7.3uS and a resonant peak current of 32.5A, the experimental values are 7uS and 27A respectively.



100V/Div; 10A/Div; 20uS/Div

Fig. 7.13. Auxiliary switch voltage and resonant inductor current.

7.6. Conclusions

The foregoing analysis and experimentation justify the following conclusions:

- The proposed scheme ensures zero voltage turn-on and capacitive turn-off of the main switches, without causing any voltage/current spikes across these switches.
- The proposed scheme ensures inductive turn-on and zero current turn-off of the auxiliary switches, without causing any voltage spike.
- Main freewheeling diode works with zero voltage turn-on, zero current turn-off. Oscillation may occur during the diode forward recovery process due to the fast current transfer from the snubbing capacitors to the diode
- Characteristic curves presented in Chapter 2 regarding the commutation duration, resonant inductor peak current and resonant inductor RMS current is verified.
- Both transformer connection True-PWM-Pole and ARCPI schemes are extensible to multilevel diode clamping multilevel inverter, achieved either on the per-cell basis or on the per-leg basis. The per-cell circuit requires multiple magnetics, its resonant current flows through only one auxiliary device. In comparison, unique magnetics are used in the per-leg circuit, however, the resonant current flows through multiple auxiliary devices.

Appendix 7.1. BASIC program for generating the gating signals in EPROM27256

```
970  U = 1   'DATA OUTPUT LINES COUNTER
980  OPEN "A:SPWMNPC.DAT" FOR OUTPUT AS #1
990  PRINT #1, ":10";  'FIRST DATA OUTPUT LINE FORMAT
1000  PRINT #1, "000000";  'FIRST DATA OUTPUT LINE FORMAT
1010 FOR I = 0 TO 127: 'SELECT SWITCHING CYCLE
1020 RA1 = 0: RA4 = 0
1030 FOR K = 128 * I TO 127 + 128 * I:  'SELECT ADDRESSES
1040 IF 0 <= K - I * 128 AND K - I * 128 <= 64 THEN VA = K - I * 128 + 64 ELSE VA = 128 - (K - I * 128)
+ 64'TRINGLE VB GENERATOR1050 VB = -64 + VA   'TRINGLE WAVE VA GENERATOR
1050 VB = VA - 64
1060 PI = 3.14159
1070 VC = 64 + 40 * SIN(2 * PI * K / 16384) 'MODULATING WAVE GENERATOR

1080 IF VC > 64 AND VA <= VC AND VC <= VA + 2 AND 64 <= K - I * 128 AND K - I * 128 <= 127
THEN MMP = 0 ELSE MMP = MMP + 1
1090 IF VC > 64 AND 1 <= MMP AND MMP <= 12 THEN MINP = 1 ELSE MINP = 0
1100 IF VC > VA AND 0 <= I AND I <= 63 AND MMP >= 1 THEN SI1 = 1 ELSE SI1 = 0
1110 SJ1 = SI1 OR MINP
1120 SJ3 = 1 - SJ1
1130 IF 1 <= MMP AND MMP <= 2 AND SJ1 = 1 AND VC > 64 THEN DA3 = 1 ELSE DA3 = 0
1140 IF 1 <= MMP AND MMP <= 10 AND SJ1 = 1 AND VC > 64 THEN SA3 = 1 ELSE SA3 = 0

1150 IF SJ1 = 0 AND 0 <= I AND I <= 63 AND VC > 64 AND 0 <= K - I * 128 AND K - I * 128 <= 63 THEN
RA1 = RA1 + 1 ELSE RA1 = RA1
1160 IF 1 <= RA1 AND RA1 <= 2 THEN DA1 = 1 ELSE DA1 = 0
1170 IF 1 <= RA1 AND RA1 <= 10 THEN SA1 = 1 ELSE SA1 = 0


1180 IF VB <= VC AND VC <= VB + 2 AND 0 <= K - I * 128 AND K - I * 128 <= 63 THEN MMN = 0 ELSE
MMN = MMN + 1
1190 IF VC < 64 AND 1 <= MMN AND MMN <= 12 THEN MINN = 1 ELSE MINN = 0
1200 IF VC < VB AND MMN >= 1 THEN SI4 = 1 ELSE SI4 = 0
1210 SJ4 = SI4 OR MINN
1220 SJ2 = 1 - SJ4
1230 IF 1 <= MMN AND MMN <= 2 AND SJ4 = 1 AND VC < 64 THEN DA2 = 1 ELSE DA2 = 0
1240 IF 1 <= MMN AND MMN <= 10 AND SJ4 = 1 AND VC < 64 THEN SA2 = 1 ELSE SA2 = 0

1250 IF SJ4 = 0 AND VC < 64 AND 64 <= K - I * 128 AND K - I * 128 <= 127 THEN RA4 = RA4 + 1 ELSE
RA4 = 0
1260 IF 1 <= RA4 AND RA4 <= 2 THEN DA4 = 1 ELSE DA4 = 0
1270 IF 1 <= RA4 AND RA4 <= 10 THEN SA4 = 1 ELSE SA4 = 0



1280 S1 = SJ1 - DA3: S2 = SJ2 - DA4: S3 = SJ3 - DA1: S4 = SJ4 - DA2  'MAIN SWITCH COMMAND
1290 A = SA4 * 2 ^ 7 + SA3 * 2 ^ 6 + SA2 * 2 ^ 5 + SA1 * 2 ^ 4 + S4 * 2 ^ 3 + S3 * 2 ^ 2 + S2 * 2 ^ 1 + S1 * 2
^ 0
1300 ' PRINT #1, I; S1; SA1; S2; SA2; S3; SA3; S4; SA4
1310    IF K = U * 16 THEN
1330    U = U + 1
1340       IF TOTAL < 255.5 THEN
1350          IF TOTAL < 15.5 THEN
1360          PRINT #1, "00"; HEX$(TOTAL)
1370          ELSE
```

```
1380          PRINT #1, "0"; HEX$(TOTAL)
1390          END IF
1400        ELSE
1410        PRINT #1, HEX$(TOTAL)
1420        END IF
1430      TOTAL = 0
1440      PRINT #1, ":"; HEX$(K / (U - 1));
1450        IF K < 16 THEN
1460        PRINT #1, "000";
1470        ELSE
1480          IF K < 256 THEN
1490          PRINT #1, "00";
1500          ELSE
1510            IF K < 4096 THEN
1520            PRINT #1, "0";
1530            END IF
1540          END IF
1550        END IF
1560      PRINT #1, HEX$(K); "00";
1570      END IF
1580 TOTAL = TOTAL + A
1590      IF A < 15.5 THEN
1600      PRINT #1, "0"; HEX$(A);
1610      ELSE
1620      PRINT #1, HEX$(A);
1630      END IF
1640    NEXT K
1650    NEXT I
1660      IF TOTAL < 256 THEN
1670      PRINT #1, "0"; HEX$(TOTAL);
1680      ELSE
1690      PRINT #1, HEX$(TOTAL);
1700      END IF
1710 CLOSE
1720 END
```

Chapter 8. A New Diode Clamping Multilevel Inverter

Abstract: This Chapter proposes a new diode clamping multilevel inverter, which rids of the series association of the clamping diodes in the conventional multilevel inverter. Operation fundamentals as well as the snubbing methods for the new inverter are discussed. Experimental results from a 3kW half bridge prototype are also presented.

8.1. Series Association of Diodes in the Conventional Inverter

In a conventional diode clamping multilevel inverter [35][36], voltage rating of each clamping diode is dependent on its position in the inverter. For each leg, one can find two diodes each sees reverse voltage stress of:

$$V_{diode} = \frac{M-1-k}{M-1} V_{dc} \tag{8.1}$$

where M is the number of inverter levels, k goes from 1 to M-2, V_{dc} is the DC link voltage.

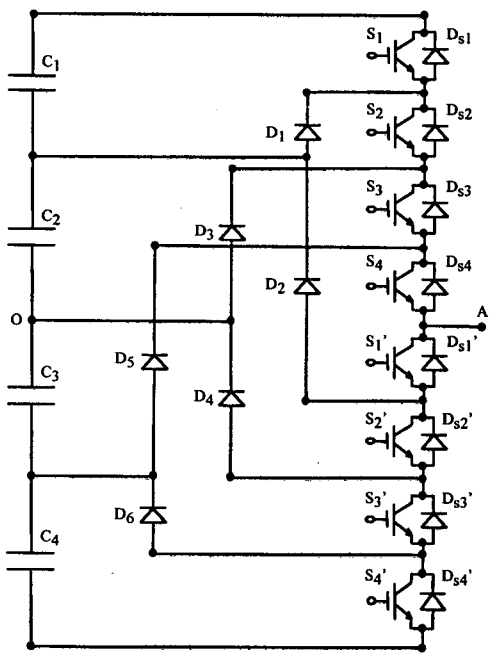


Fig. 8.1. Conventional diode clamping five level inverter leg, where clamping diode has to block high voltage.

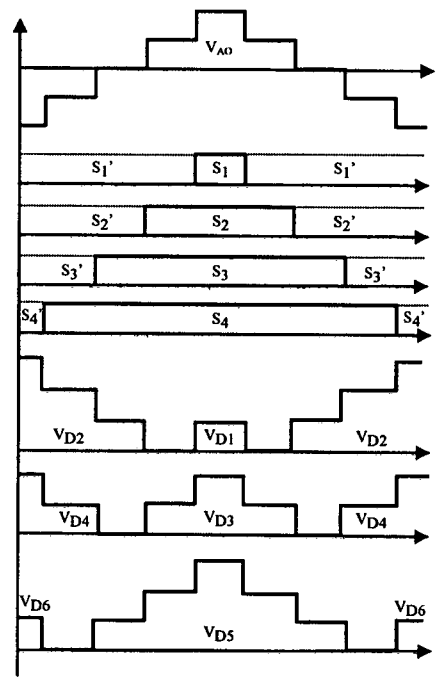


Fig. 8.2. Clamping diode voltage stress in association with the switching state in the conventional inverter.

For a five level case, as shown in Fig. 8.1, D_1 and D_6 see $V_{dc}/4$, D_3 and D_4 see $2V_{dc}/4$, D_2 and D_5 see $3V_{dc}/4$, whereas each main device see only $V_{dc}/4$. Fig. 8.2 shows how the blocking voltage is related to the switching state.

While in a practical situation the main device voltage rating is always fully utilized, it is hence difficult to have fast turn-off diode in the market with multiple voltage rating and yet comparable performance. In high voltage P-N junction designing, larger breakdown voltage is always accompanied by higher on-state loss and longer turn-off transience.

The common solution to this problem is to put appropriate number of diodes in series. The five level case is shown in Fig. 8.3. Diodes in series, though less problematic than GTOs in series, is by no means an optimal solution. Unequal static or dynamic voltage sharing can happen, due to the diversity of switching characteristics and stray parameters of the diodes in series. Measures to prevent the potential over-voltage problem by providing large snubber capacitor and high power resistor network lead to an expensive and voluminous system.

8.2. Operation of the New Inverter

A new diode clamping multilevel inverter has been proposed. For the five level case, as shown in Fig. 8.4, a total of 8 switches and 12 diodes are used, the same amount as that in the conventional inverter. The pyramid structure is extensible to infinite number of levels unless otherwise practically limited.

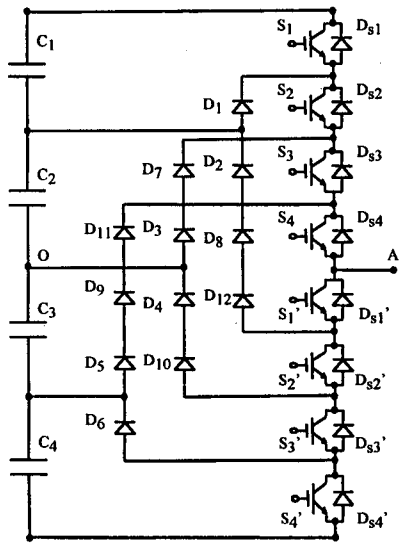


Fig. 8.3. Conventional diode clamping multilevel inverter with diodes in series.

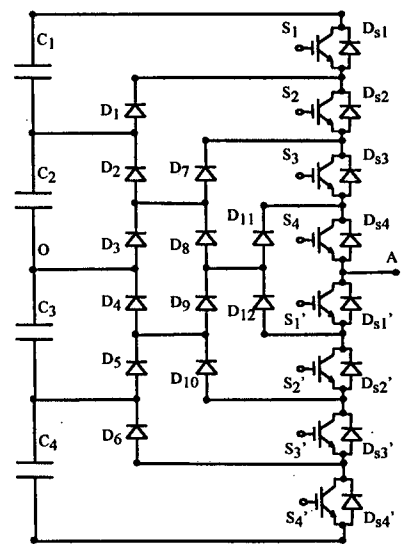


Fig. 8.4. Proposed new diode clamping multilevel inverter.

8.2.1. Switching Cells of the New Inverter

The new inverter can be decomposed into two-level switching cells which constitute its basic operation units. For the five level leg, one can define (5-1) switching cells as shown in Fig. 8.5 (a), (b), (c) and (d). In cell (a), the leg output moves from $V_{dc}/2$ to $V_{dc}/4$ or the reverse. In the same sense, the output moves from $V_{dc}/4$ to 0 or the reverse in cell (b), from 0 to $-V_{dc}/2$ or the reverse in cell (c), and from $-V_{dc}/2$ to $-V_{dc}/4$ or the reverse in cell (d).

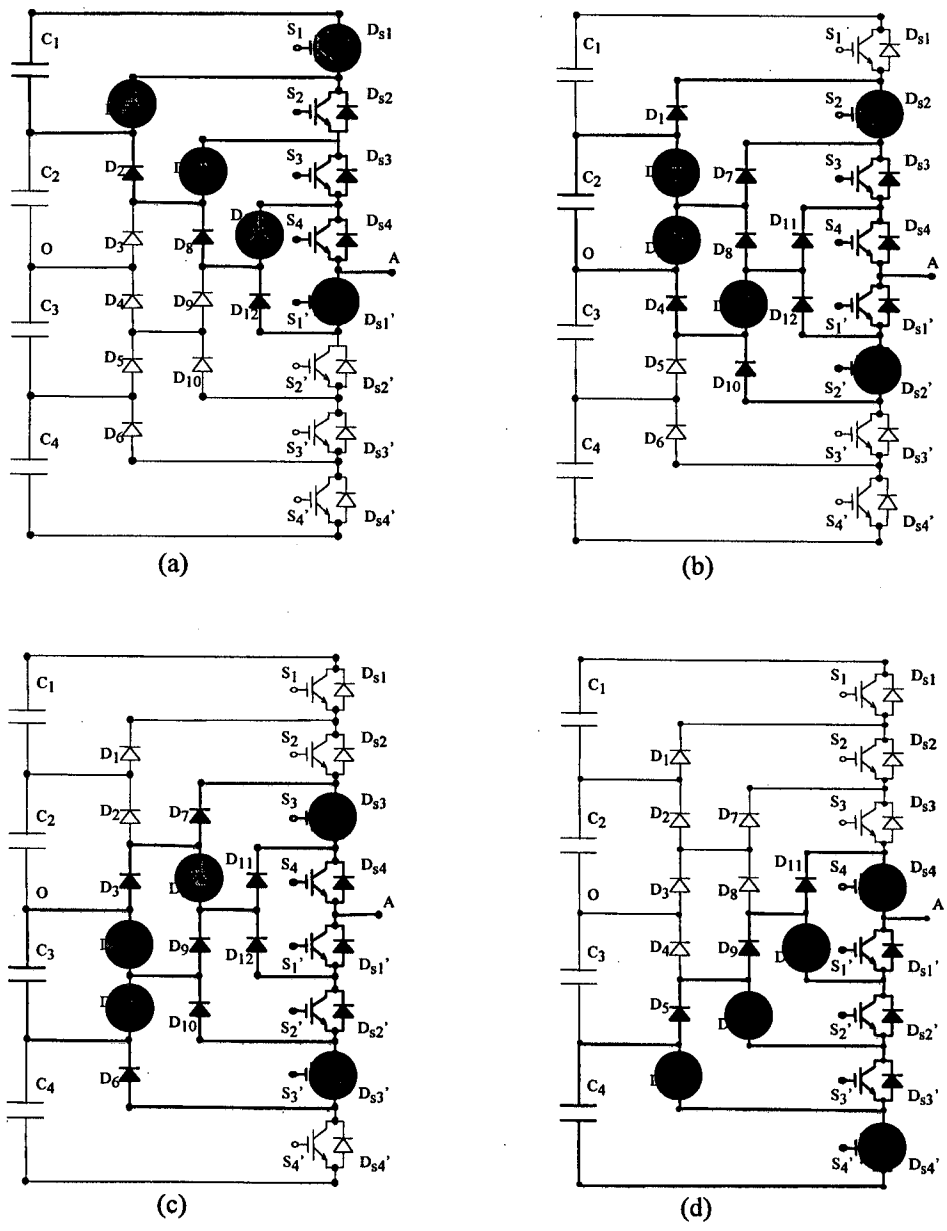
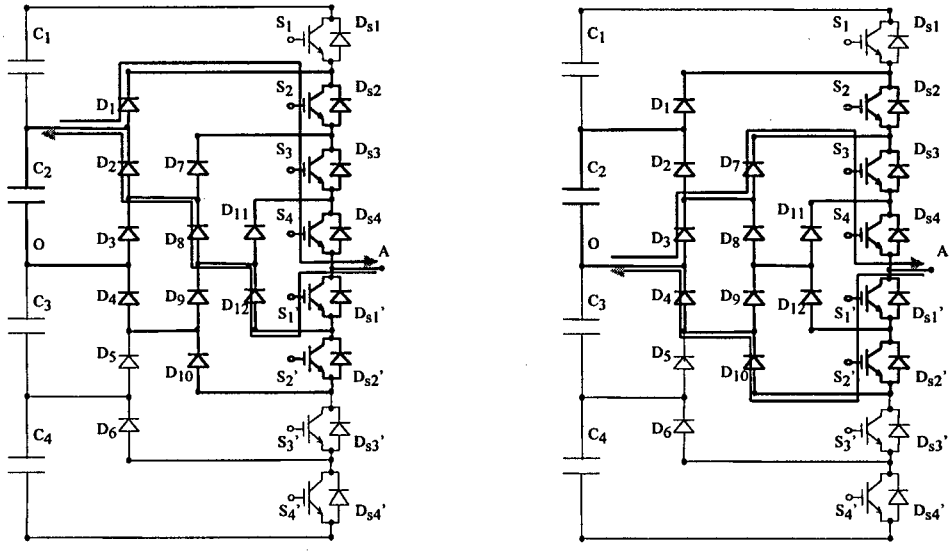


Fig. 8.5. The four switching cells of the new diode clamping multilevel inverter.

To further illustrate how each switching cell works as a two level inverter, the forward and freewheeling paths for the up/down arms of cell(b) are shown in Fig. 8.6(a) and (b). Current paths for the other cells can be analogously found.



(a) forward/freewheeling paths for the up arm (b) forward/freewheeling paths for the down arm

Fig. 8.6. Forward and freewheeling paths for cell (b).

The above decomposition presumes that the output dv/dt is constrained to a single device dv/dt, which has been regarded as one of the most notable attribute of the multilevel inverter over the plain series of devices. To work within this constraint, each switching action must only involve one switching cell. Simultaneous switching of more than one switching cell runs no difference with direct series association and is forbidden in operation.

8.2.2. Switching State of the Diode Network

Take cell (a) for example. In this cell, S_2, S_3 and S_4 are always ON, while S_1 and S_1' work alternatively connecting the output to $V_{dc}/2$ or $V_{dc}/4$ respectively. The remaining switches of the leg, S_2', S_3' and S_4' are always OFF. Thus D_2, D_8 and D_{12} must be in clamping state and each blocks zero voltage ideally. Moreover, D_1, D_7 and D_{11} each must always follows the state of S_1', as shown in Fig. 8.5(a).

In the same sense, for cell (b), D_3 and D_9 follow the state of S_2' while D_2 follows the state of S_2, as shown in Fig. 8.5(b); for cell (c), D_5 follows the state of S_3', D_4 and D_8 follow

the state of S_3, as shown in Fig. 8.5(c); and in cell (d), D_6, D_{10} and D_{12} follow the state of S_4, as shown in Fig. 8.5(d). The switching state of the diode network can thus be summarized in Table 8.1, which is further graphically shown in Fig. 8.7.

Table 8.1. Switching State of the Diode Network verses the switch state

1: Device blocks zero voltage

0: Device blocks $V_{dc}/4$ voltage

Switch state / Diode state / Output level	S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'
		D_1, D_7, D_{11}	D_2	D_3, D_9	D_4, D_8	D_5	D_6, D_{10}, D_{12}	
$V_{dc}/2$	1	0	1	0	1	0	1	0
$V_{dc}/4$	0	1	1	0	1	0	1	0
0	0	1	0	1	1	0	1	0
$-V_{dc}/4$	0	1	0	1	0	1	1	0
$-V_{dc}/2$	0	1	0	1	0	1	0	1

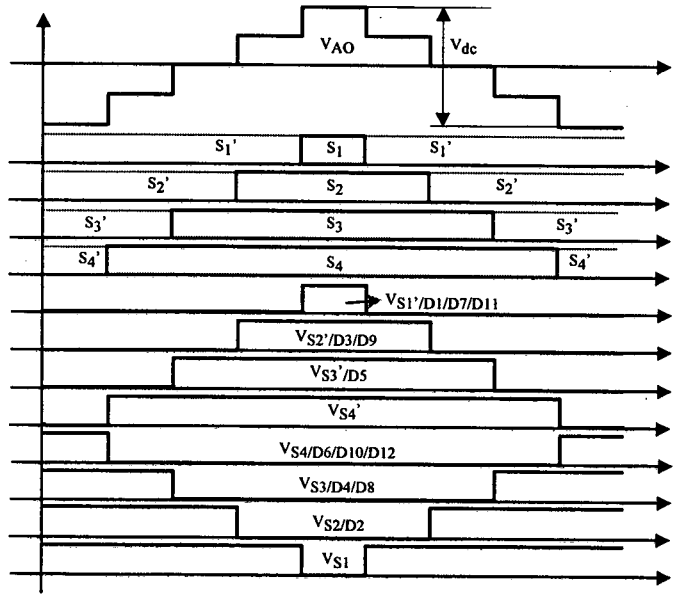


Fig. 8.7. Illustration of the switching state in the new diode clamping multilevel inverter in relation to the output voltage level.

8.2.3. Switch and Diode Clamping Mechanism

Refer back to Fig. 8.5 (a). Obviously, S_1 is directly clamped by D_1 after it's turn-off, while S_1' in series with D_2, D_8 and D_{12} is clamped by D_{s1}, D_{s2}, D_{s3} and D_{s4} after its turn-off. Further, D_{11} in series with D_2 and D_8 is clamped by D_{s1}, D_{s2} and D_{s3}; D_7 in series with D_2 is clamped by D_{s1} and D_{s2}, while D_1 is directly clamped by D_{s1}.

Suppose that when S_2', S_3' and S_4' are all OFF, and each of them blocks $V_{dc}/4$ voltage, D_2, D_8, D_{12} each will then block zero voltage. Then, S_1 and S_1', D_1, D_7, D_{11} are all clamped to $V_{dc}/4$. Among which S_1, D_1 are directly clamped while S_1', D_7, D_{11} are indirectly clamped.

Similar mechanism can be witnessed with cell (b), where S_2', D_3, D_9 as well as S_2, D_2 are all clamped. Among which D_2, D_3 are directly clamped while S_2', D_9, S_2 are indirectly clamped. In cell (c), S_3', D_5 and S_3, D_8, D_4 are all clamped. Among which D_4, D_5 are directly clamped while S_3', S_3, D_8 are indirectly clamped. In cell (d), S_4' and S_4, D_6, D_{10}, D_{12} are all clamped. Among which S_4', D_6 are directly clamped while S_4, D_{10}, D_{12} are indirectly clamped.

As a result, for the proposed new inverter, not only the switches are clamped, so are the clamping diodes. Among them, the 8 lateral components (S_1, S_4', D_1, D_2, D_3, D_4, D_5, and D_6) are directly clamped, the remaining devices, however, are all indirectly clamped.

8.2.4. Over-Voltage from Indirect Clamping

Considering the commutation process from S_1', D_{12}, D_8, D_2 to D_{s4}, D_{s3}, D_{s2}, D_{s1} in cell (a). After the turn-off of S_1', the demagnetization of the parasitic inductance L_S in the clamping path causes over-charging of S_1' (stray capacitance) and discharging of S2', S3' and S4' (stray capacitances), as shown in Fig. 8.8. Such over-charging and discharging will be maintained because the discharging/charging paths are blocked by D_2, D_8 and D_{12}. Consequently, S_1' blocks higher than $V_{dc}/4$ while S2', S3', S4' together block less than $3V_{dc}/4$ and D_2, D_8, D_{12} together sees the voltage difference between V_{s1}, and $V_{dc}/4$. In the meanwhile, D_{11} sees $V_{dc}/4$ plus V_{D2} plus V_{D8}, D_7 sees $V_{dc}/4$ plus V_{D2}, while D_1 sees $V_{dc}/4$.

The indirect clamping and the subsequent over-voltage problem holds also for S_2' and S_2, S_3' and S_3, and S_4 together with their relevant diodes in cell(b), cell(c) and cell(d).

Due to the fact that the stray capacitance of the neighboring outer switch experiences once more discharging, the neighboring outer device (switch and its relevant diodes) always blocks less voltage while the inner device always blocks more voltage. The innermost device, of course, is always exposed to the highest voltage stress.

Over-voltage problem arising from the indirect clamping exists with any diode clamping multilevel inverter. Measures such as refined construction and appropriate snubbing are believed to be helpful in mitigating this problem. Moreover, it can be eliminated if the clamping paths are made bi-directional by anti-paralleling to each clamping diode a small-rating switch.

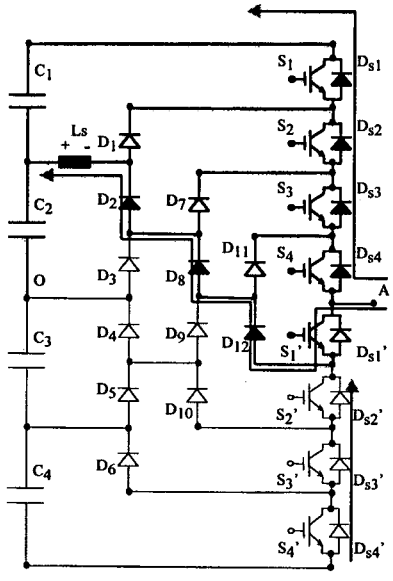


Fig. 8.8. Illustration of the over-voltage across S_1', D_7 and D_{11} due to demagnetization of L_s.

8.3. Snubbing/Soft Switching of the New Inverter

The true attractiveness of the multilevel inverter consists in the expanded capacity of an installation where GTOs are most likely the choice as the switching element. Hence snubber designing plays a role. However, snubbing techniques for the diode clamping multilevel inverter (M>3) have not been covered until the most recent in the literature, probably due to the underlying difficulty in arranging efficient turn-on snubbers for the inner switching cells with bi-directional busses. Non-polarized turn-on snubbers are especially inefficient.

When GTOs are not the choice of device, the clamping scheme shown in Fig. 8.9 and the snubbing scheme shown in Fig. 8.10 shall apply. In Fig. 8.10, instead of linear reactors limiting di/dt over the full load range, saturable reactors are used which go out of saturation at the right moment to limit the diode reverse recovery overshoot.

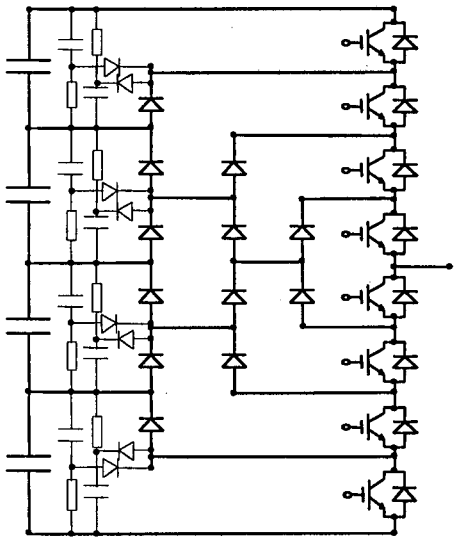


Fig. 8.9. Clamping scheme for the new diode clamping multilevel inverter, extensible to any level.

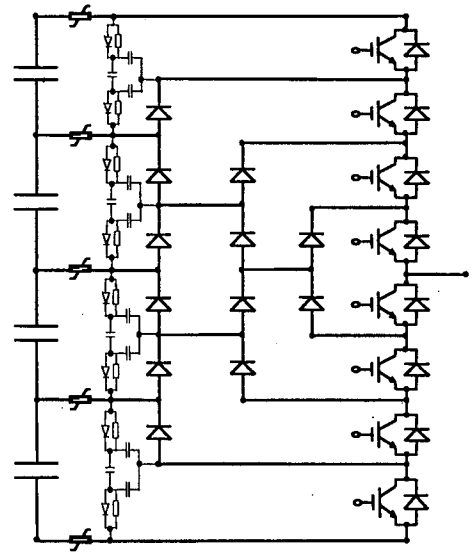


Fig. 8.10. Snubbing scheme for the new diode clamping multilevel inverter, extensible to any level .

In addition, both True-PWM-Pole and ARCPI soft switching methods are applicable to this new inverter, as shown in Fig. 8.11 and Fig. 8.12. In comparison with the arrangements shown in Fig. 7.7 and Fig. 7.8, the auxiliary branches are installed based on each individual switching cell.

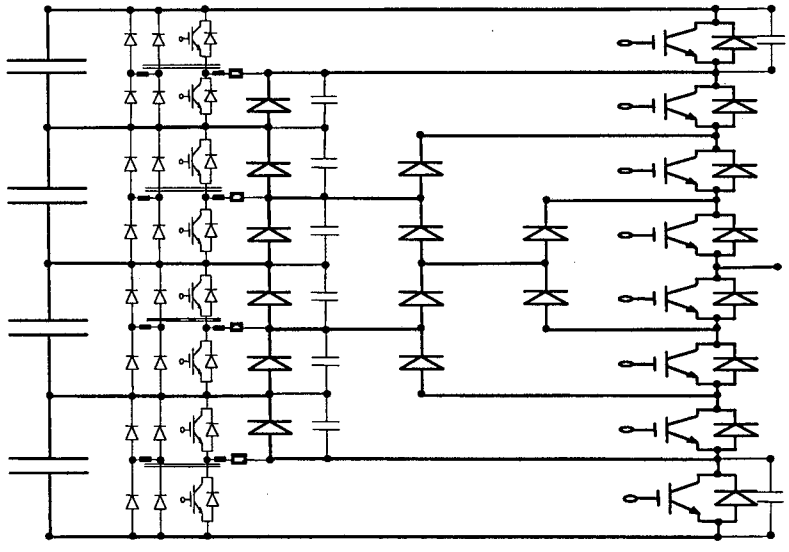


Fig. 8.11. True-PWM-Pole five level diode clamping multilevel inverter. Auxiliary branch is arranged for each switching cell. Main circuitry ZVS switching, auxiliary circuitry ZCS switching.

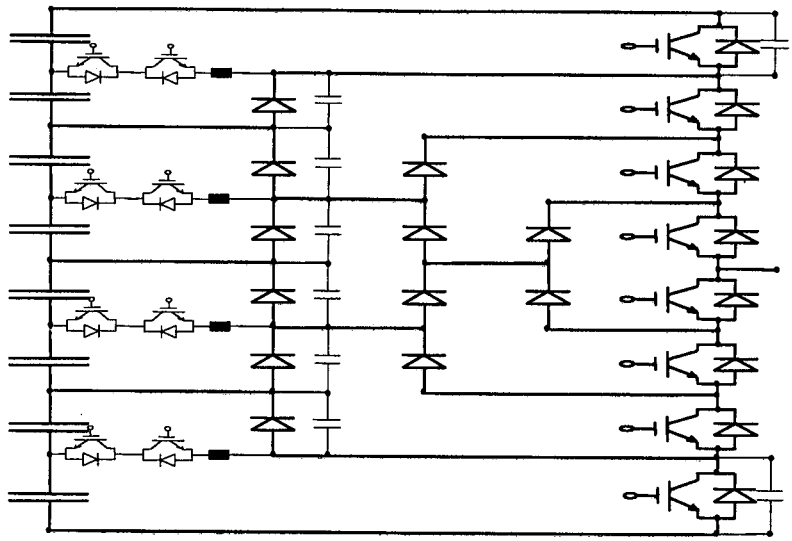


Fig. 8.12. ARCPI five level diode clamping multilevel inverter. Auxiliary branch is arranged for each switching cell. Main circuitry ZVS switching, auxiliary circuitry ZCS switching.

8.4. Experimentation

A scaled half bridge prototype has been built for verification of the new inverter. Four 120V DC power sources each in series with a 10mH inductor establish the four separate DC supplies for the DC link. A 8mH inductor in series with a 12Ω resistor are connected at the output, as shown in Fig. 8.13. Fundamental frequency modulation scheme eliminating the 5th and the 7th harmonic is implemented. The BASIC program for generating the gating signals in EPROM 27256 is listed in Appendix 8.1. Experimental results are shown in Fig. 8.14.

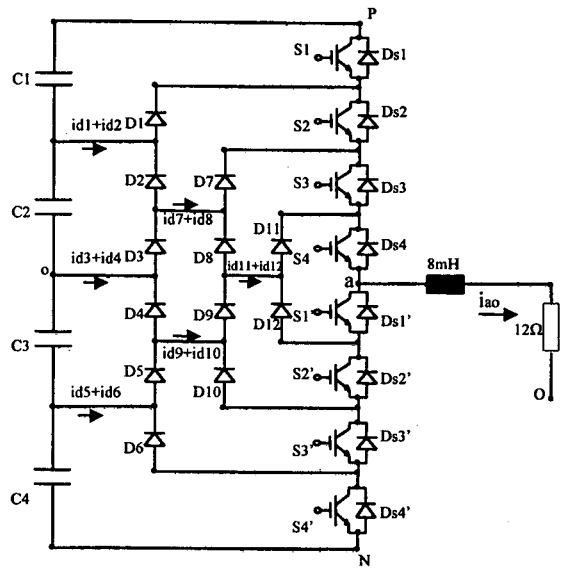
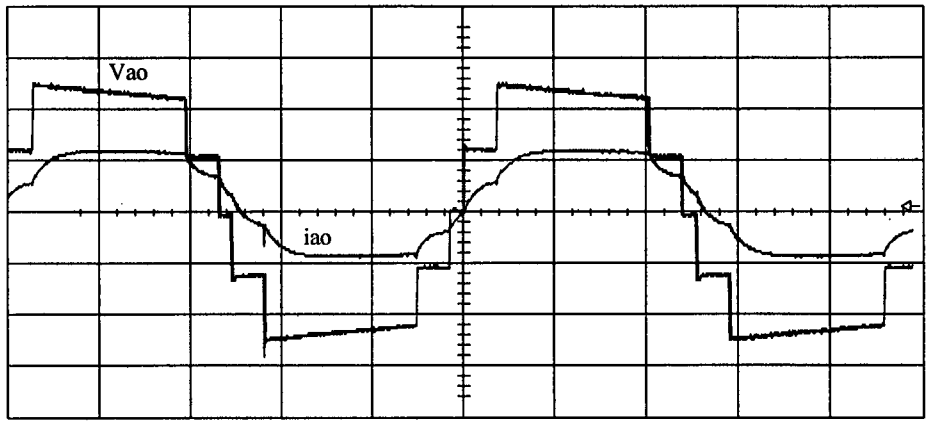
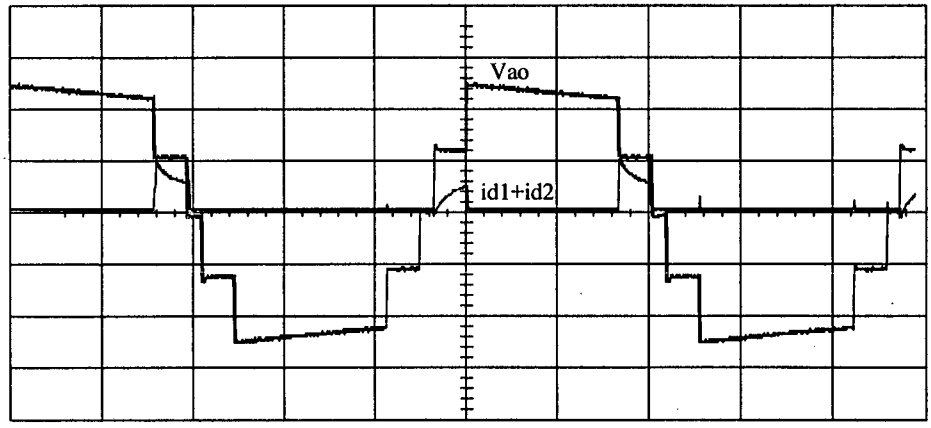


Fig. 8.13. Experimental set-up of the proposed diode clamping inverter.
C1=C2=C3=C4=3300uF, D1-D12: HFA30TA60C, S1-S4': SKM50GB123D.



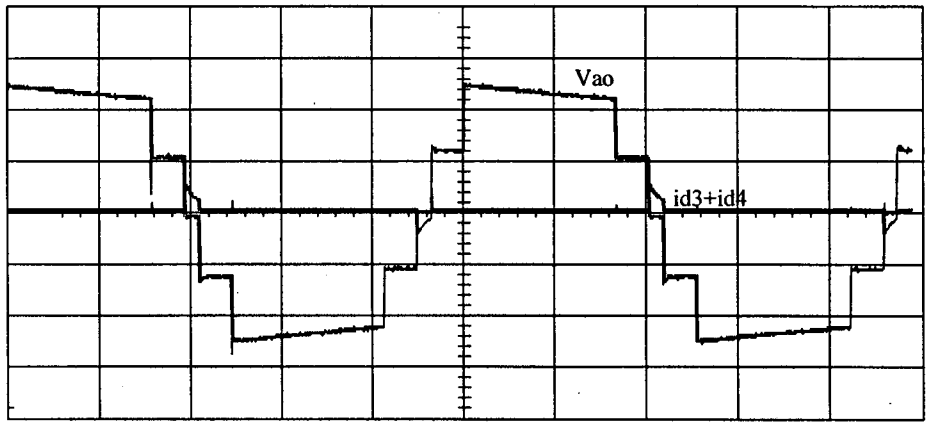
100V/Div; 20A/Div; 4mS/Div

Fig. 8.14(a). Output voltage and load current waveforms.



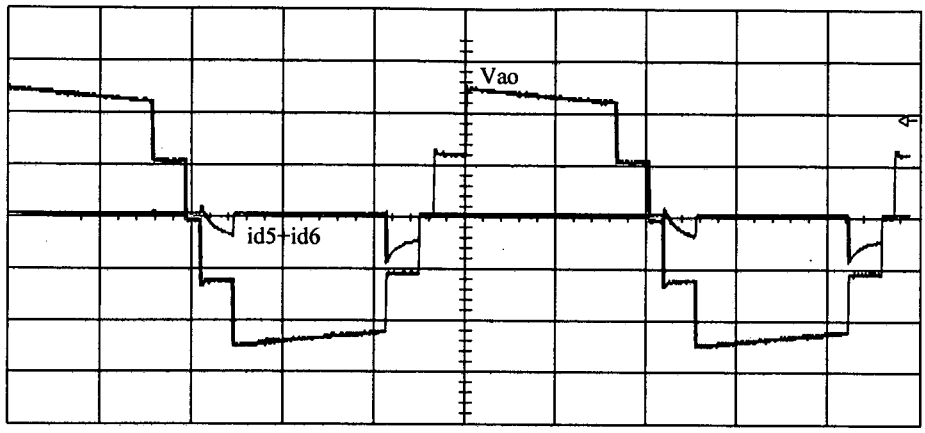
100V/Div; 20A/Div; 4mS/Div

Fig. 8.14(b). Sum of D1 and D2 currents in relation to the output voltage.



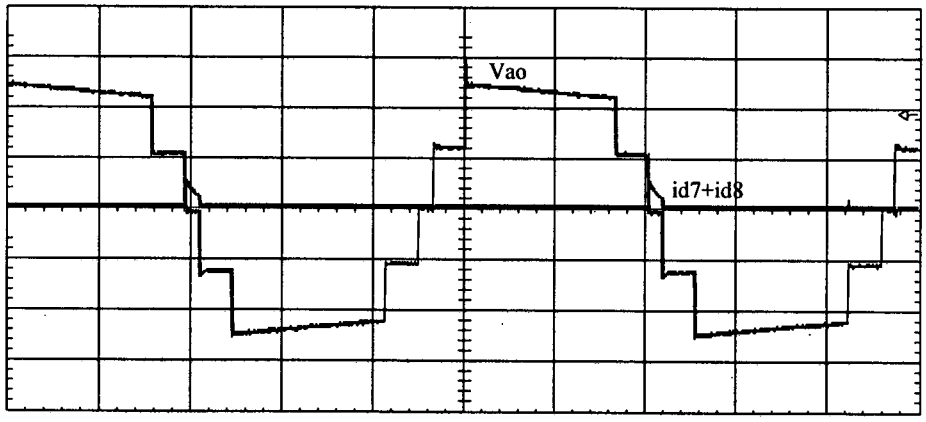
100V/Div; 20A/Div; 4mS/Div

Fig. 8.14(c). Sum of D3 and D4 currents in relation to the output voltage.



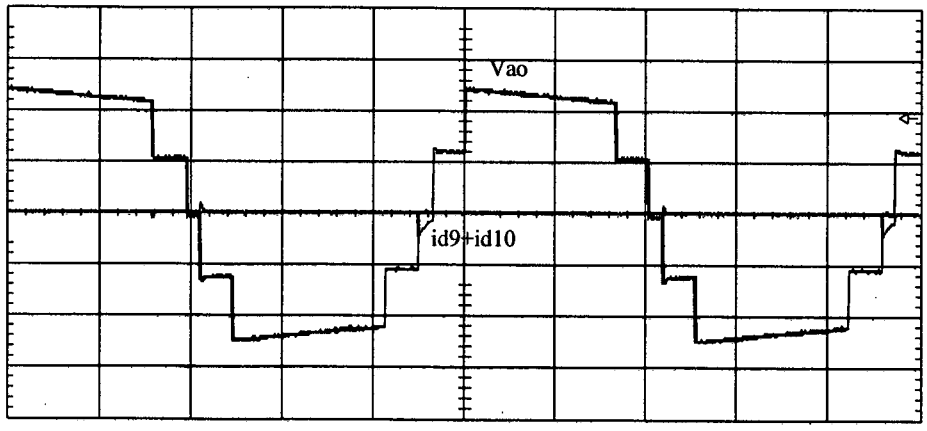
100V/Div; 20A/Div; 4mS/Div

Fig. 8.14(d). Sum of D5 and D6 currents in relation to the output voltage.



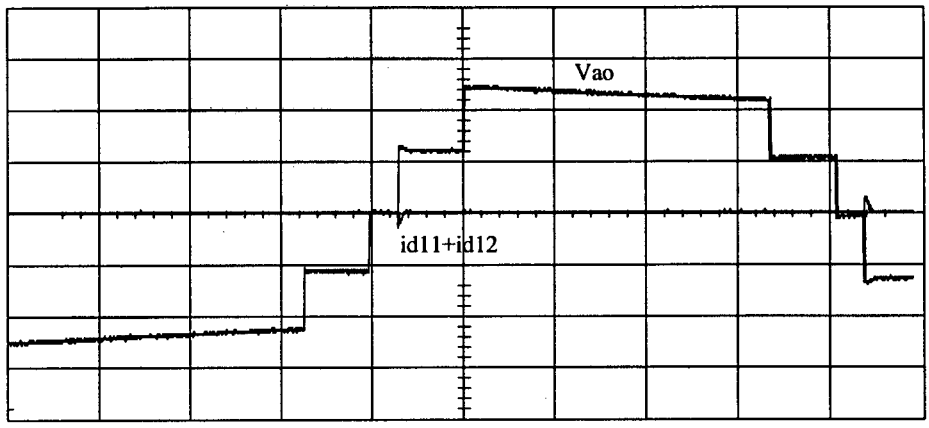
100V/Div; 20A/Div; 4mS/Div

Fig. 8.14(e). Sum of D7 and D8 currents in relation to the output voltage.



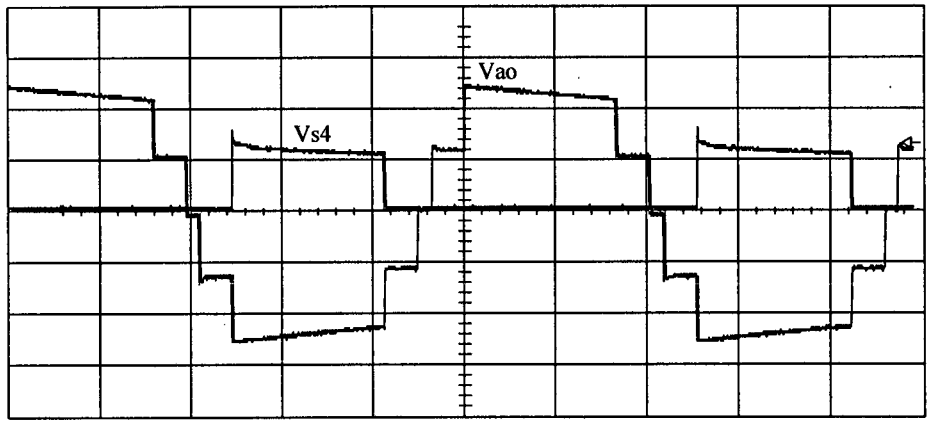
100V/Div; 20A/Div; 4mS/Div

Fig. 8.14(f). Sum of D9 and D10 currents in relation to the output voltage.



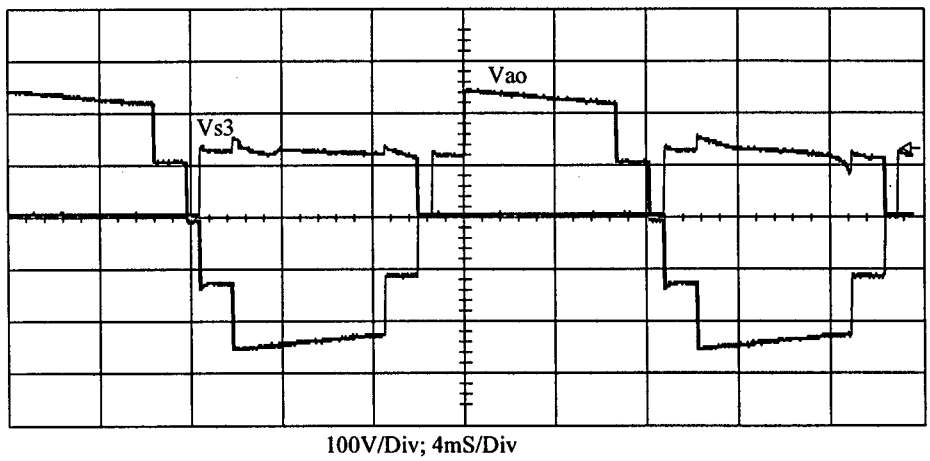
100V/Div; 10A/Div; 4mS/Div

Fig. 8.14(g). Sum of D11 and D12 currents in relation to the output voltage.



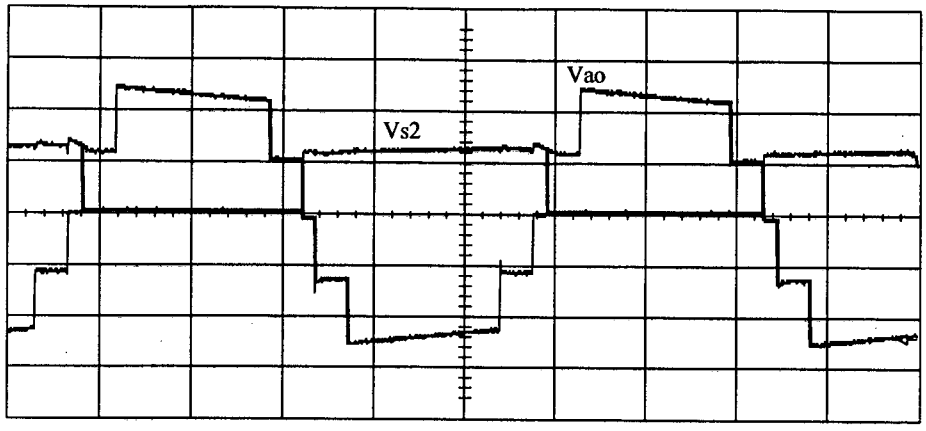
100V/Div; 4mS/Div

Fig. 8.14(h). S4 blocking voltage in relation to the output voltage.



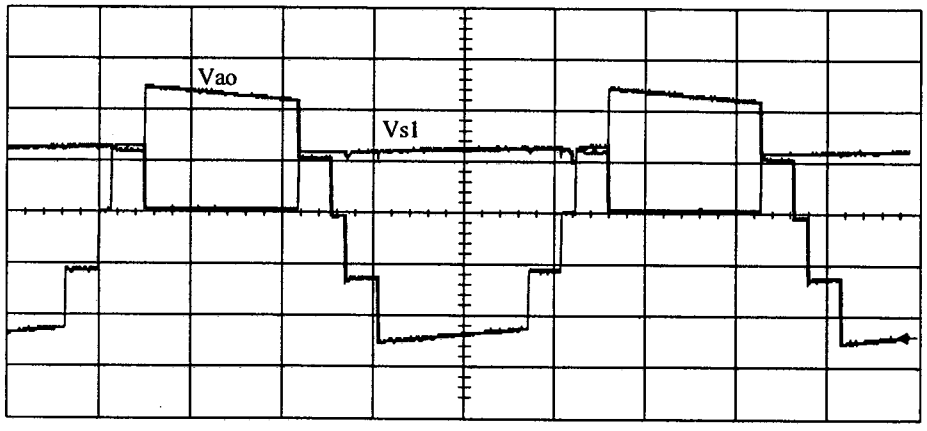
100V/Div; 4mS/Div

Fig. 8.14(i). S3 blocking voltage in relation to the output voltage.



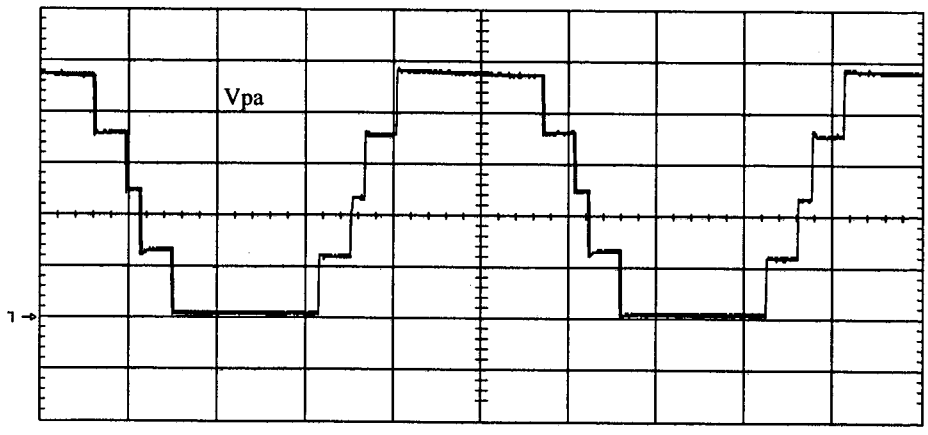
100V/Div; 4mS/Div

Fig. 8.14(j). S2 blocking voltage in relation to the output voltage.



100V/Div; 4mS/Div

Fig. 8.14(k). S1 blocking voltage in relation to the output voltage.



100V/Div; 4mS/Div

Fig. 8.14(l). Up-arm (S1+S2+S3+S4) blocking voltage.

8.5. Conclusions

- Due to the multiple blocking voltages, series associations of clamping diodes are needed in the conventional diode clamping multilevel inverter, which results in static and dynamic voltage sharing problem among the diodes in series. Large RC network dealing with this problem leading to voluminous and expensive system.
- The proposed new diode clamping multilevel inverter is structured with built-in clamping for all the clamping diodes in the clamping network. Thus all components in the new circuit are clamped. The problem of series association of clamping diodes with the conventional diode clamping multilevel inverter structure is solved.
- Over-voltage across the inner devices as a result of indirect clamping is inherent with both the conventional inverter and the new inverter. Current loop inductances play the key role in exciting the problem. Reasonable efforts in layout designing, device selecting (low internal inductance) as well as snubber positioning are helpful in mitigating the problem.

Appendix 8.1. BASIC program for generating the gating signals in EPROM 27256M

```
1120 U = 1  'DATA OUTPUT LINES COUNTER
1130 OPEN "A:MULTD.DAT" FOR OUTPUT AS #1
1140 PRINT #1, ":10";  'FIRST DATA OUTPUT LINE FORMAT
1150 PRINT #1, "000000";  'FIRST DATA OUTPUT LINE FORMAT
1160 FOR K = 0 TO 16383
1170 IF K <= 5498 OR K >= 10883 AND K <= 16383 THEN S11 = 1 ELSE S11 = 0
1180 IF K >= 5500 AND K <= 10881 THEN S1 = 1 ELSE S1 = 0
1190 IF K <= 4340 OR K >= 12041 AND K <= 16383 THEN S22 = 1 ELSE S22 = 0
1200 IF K >= 4342 AND K <= 12039 THEN S2 = 1 ELSE S2 = 0
1210 IF K <= 3847 OR K >= 12534 AND K <= 16383 THEN S33 = 1 ELSE S33 = 0
1220 IF K >= 3849 AND K <= 12532 THEN S3 = 1 ELSE S3 = 0
1230 IF K <= 2689 OR K >= 13692 AND K <= 16384 THEN S44 = 1 ELSE S44 = 0
1240 IF K >= 2691 AND K <= 13690 THEN S4 = 1 ELSE S4 = 0
1250 A = S22 * 2 ^ 7 + S11 * 2 ^ 6 + S4 * 2 ^ 5 + S3 * 2 ^ 4 + S44 * 2 ^ 3 + S33 * 2 ^ 2 + S2 * 2 ^ 1 + S1 * 2 ^
0
'  PRINT #1, S1; S11; S2; S22; S3; S33; S4; S44; K;
1260    IF K = U * 16 THEN
1270    U = U + 1
1280      IF TOTAL < 255.5 THEN
1290        IF TOTAL < 15.5 THEN
1300        PRINT #1, "00"; HEX$(TOTAL)
1320        ELSE
1330        PRINT #1, "0"; HEX$(TOTAL)
1350        END IF
1360      ELSE
1370      PRINT #1, HEX$(TOTAL)
1390      END IF
1400    TOTAL = 0
1420    PRINT #1, ":"; HEX$(K / (U - 1));
1430      IF K < 16 THEN
1440      PRINT #1, "000";
1450      ELSE
1460        IF K < 256 THEN
1470        PRINT #1, "00";
1480        ELSE
1490          IF K < 4096 THEN
1500          PRINT #1, "0";
1510          END IF
1520        END IF
1530      END IF
1540    PRINT #1, HEX$(K); "00";
1550    END IF
1560 TOTAL = TOTAL + A
1570    IF A < 15.5 THEN
1580    PRINT #1, "0"; HEX$(A);
1590    ELSE
1600    PRINT #1, HEX$(A);
1610    END IF
1620  NEXT K
1630    IF TOTAL < 256 THEN
1640    PRINT #1, "0"; HEX$(TOTAL);
1650    ELSE
1660    PRINT #1, HEX$(TOTAL);
1670    END IF
1680 CLOSE
1690 END
```

Chapter 9. General Conclusions

This thesis is dedicated to the soft switching techniques of the multilevel inverters. Included are also the background treatments as regards the main circuits.

Chapter 1 of this thesis deals with the fundamentals of the multilevel inverters. The existing approaches for implementing high voltage high power inverters utilizing device association or cell association are inspected first. While series association of devices offers advantage in terms of redundancy, the output waveform and dv/dt are not favored from the multiple devices. Converter association, on the other hand, necessitates insulation either on the AC side or the DC side which means additional magnetics. The multilevel inverters evolved from cell association, however, generate multi-step outputs without heavy magnetics.

The diode clamping multilevel inverter suffers from indirect clamping, potential drift, clamping diodes series and snubbing problems etc. Except for the Neutral-Point-Clamped (NPC) inverter which is free from the last three problems, practical application can hardly be realized before relevant solutions are verified. Theoretically, the inverter is relieved from the potential drift problem when pure reactive power is transferred.

The capacitor clamping inverter is exempt from the above problems. However other shortcomings arise such as the parasitic inductances resulted from the clamping capacitors, as well as the heat capacity required for these capacitors. It seems more applicable than the diode clamping inverter in the high level case especially when active power transfer is involved.

This chapter also reviews the snubber schemes reported for the NPC inverter. Before which snubbers for two-level inverter are compared. The use of dissipative snubber leads to such objectionable problems as snubber loss, voltage/current spikes, series reactor loss as well as the adverse effects from the snubbing diodes. These problems become more pronounced for multilevel inverters. For regenerative snubber, even though the snubber loss is recovered, the expected increase in operating frequency is limited by the complexity of the recovery circuitry, while the other problems remain.

Chapter 2 assesses the reported two-level inverter soft switching techniques and proposes the transformer connection True-PWM-Pole circuit. While the Actively-Clamped Resonant-DC-Link-Inverter (ACRLI) is not regarded suitable for power level beyond 300kW because of the cost, size and cooling issues of the resonant inductor, the Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI) suffers from the measuring and controlling difficulties to

guarantee the zero voltage switching especially when the DC center tap potential drift is taken into account.

The transformer connection True-PWM-Pole circuit guarantees zero voltage switching of the main device without any of the problems associated with the conventional snubber and without any additional measuring or controlling. In the meanwhile, zero current switching of the auxiliary device is simultaneously attained without the affliction of voltage spike due to the bridge configuration, which is a significant advantage over the regenerative snubber where baby snubber is always required for the recovery chopper in hard switching. Depending on the designing, the auxiliary device can be rated at about 1/4 of the main device. The duty cycle loss due to the resonance transition is comparable to that of the conventional snubbed inverter.

The transformer connection True-PWM-Pole circuit is verified by a 5kW prototype.

Besides transformer connection, auto-transformer connection and capacitor connection True-PWM-Poles are also discussed. Even though the auxiliary device current stress is further halved, the freewheeling current flow during the non-commutation interval evolved from the magnetizing current renders the normal auto-transformer connection hardly applicable before practical measures are found.

The freewheeling current problem is solved in the modified auto-transformer connection family, which is verified by a 5kW prototype. A simple snubbing is needed for the series diode to suppress the voltage spike. The variations of this family allow for further reduction in the auto-transformer voltage/current rating or the resonant inductor current rating, which are also tested in the laboratory.

The capacitor connection circuit, on the other hand, eliminates the magnetics at the price of the fairly augmented resonant circuit stress.

In ***Chapter 3***, the clamping voltage stability in the three level capacitor clamping inverter is explored. Under sub-harmonic modulation, the clamping voltage is stable as far as the inverter load is not pure-reactive, due to the inherent feedback mechanism. The clamping voltage response exhibits typical one-order system characteristics. The time constant of which is dependent on the load properties, modulation index, clamping capacitance etc.

When asymmetries are taken into account, typically gating and switching mismatches, the clamping voltage is balanced at a new operation point other than the nominal value, as a result of the joint effects of the self balancing ability and the asymmetry. In addition, dead

time is not expected to cause any clamping voltage drift, because of its symmetrical influence to the two switching cells during the local switching cycle.

With sub-harmonic modulation, active control over the clamping voltage where necessary can be realized by vertically shifting one of the triangle carriers according to the deviation direction and the load current direction. Clamping voltage is adjusted on the switching cycle basis.

The self-balancing ability is proved in a half-bridge three level prototype system.

Chapter 4 introduces a True-PWM-Pole three level capacitor clamping inverter. By installing the transformer connection True-PWM-Pole to each of the two switching cells, zero voltage switching for all the main devices and zero current switching for all the auxiliary devices are secured, with the same performance as that in the two level inverter.

In particular, the proposed True-PWM-Pole arrangement for the outer switching cell further guarantees the stiffness of the clamping voltage due to the damped second order charging/discharging paths established by the auxiliary circuitry. Most positively, the normal auto-transformer connection True-PWM-Pole is now applicable to the outer switching cell because the freewheeling current path in this case is blocked by the clamping capacitor.

The transformer connection True-PWM-Pole technique along with the Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI) both are extensible to the capacitor clamping multilevel inverter (M>3). Two general zero voltage switching topologies for the capacitor clamping multilevel inverter (M>3) are obtained.

In ***Chapter 5***, the 3kW experimental set-up for the half bridge three level capacitor clamping inverter is described in details. The prototype employs four SEMIKRON IGBT modules each rated at 1200V/50A driven by four single intelligent drivers (SKHI10) for the two main modules and two double intelligent drivers (SKHI23) for the two auxiliary modules. Between the driver and device, a zero voltage detecting circuit is inserted. Gating signals are generated in EPROM 27256M, and time durations including the auxiliary gating signal width and the main gating signal width are set as discussed in Chapter 2.

The proposed circuit and the analyses are well verified through the experimental results from this prototype.

Chapter 6 is concerned with the neutral potential stability in the NPC inverter. Under sub-harmonic modulation, the neutral potential is stable as far as the inverter load is not pure-reactive, due to the inherent feedback mechanism. The neutral potential response exhibits

typical one-order system characteristics. The time constant of which is dependent on the load properties, modulation index, DC link capacitances etc.

When asymmetries are taken into account, typically gating and switching mismatches, the neutral potential is balanced at a new operation point other than zero, dependent on the joint effects of the self balancing ability and the asymmetry. Similarly, the dead time is not expected to cause any neutral potential drift because of its symmetrical influence to the two switching cells during the fundamental cycle.

When Space-Vector-Modulation (SVM) is used, the need for appropriate distribution of the redundant states of the small vector arises, active control over the neutral potential becomes indispensable. On the other hand, with sub-harmonic modulation, active control when needed can be effected by vertically shifting the modulating reference according to the deviation direction and the operation mode (rectifying or inverting).

Self-balancing under ideal and non-ideal conditions are verified by PSPICE simulations.

Chapter 7 proposes a True-PWM-Pole three level NPC inverter. By installing the transformer connection True-PWM-Pole to each of the two switching cells, zero voltage switching for all the main devices and zero current switching for all the auxiliary devices are secured, with the same performance as that in the two level inverter.

The transformer connection True-PWM-Pole technique along with the Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI) both are extensible to the diode clamping multilevel inverter (M>3). The auxiliary circuitry can be configured on the per-cell or per-leg basis. The per-leg structure needs only one resonant inductor and one auxiliary transformer, while in the per-cell case, each cell needs an inductor and a transformer. However, the per-leg structure suffers from the indirect clamping problem also in the auxiliary circuitry, and moreover, resonant current flowing involves multiple devices in the path.

Such extension leads to four general zero voltage switching topologies for the diode clamping multilevel inverter.

Finally, in ***Chapter 8***, a new diode clamping multilevel inverter is proposed, which solves the problem of series association of diodes in the conventional diode clamping inverter. However, the other aspects of operation remain the same as the conventional one.

In summary, the following conclusions are drawn from this thesis:

- Multilevel inverters enable high voltage operation and multi-step output without requiring any magnetics insulation.
- The clamping voltage in the capacitor clamping inverter and the neutral potential in diode clamping inverter are both self-balancing under sub-harmonic modulation so long as the load is not pure reactive.
- The use of snubber leads to the reduction of the switching stress but not necessarily any significant increase in the switching frequency.
- Transformer connection True-PWM-Pole technique offers an alternative of the ARCPI and enables high frequency high power operation.
- Transformer connection True-PWM-Pole technique is extensible to multilevel inverters with the same performance as in the two level case, which facilitates high voltage and high power conversion at high frequency and high efficiency.
- The new diode clamping multilevel inverter works free of the series association of clamping diodes and is hence more applicable in practice.

To the best of the belief of this thesis, the soft switched multilevel inverter is the legitimate contender against the well-entrenched hard switched or snubbed counterpart especially for high performance applications, even though they face greater obstacles than at the two-level low power levels.

Looking ahead, several subjects deserve further specific investigations:

- Identification of potential problems, comparison of its variations, optimization of designing and evaluation of performance of the modified auto-transformer connection True-PWM-Pole family under practical circumstances.
- Possible clamping voltage drift of the capacitor clamping inverter and neutral potential drift of the diode clamping inverter under load unbalance or load transience conditions.
- Solutions to the problems of the diode clamping multilevel inverter (M>3), including indirect clamping, potential drift and turn-on snubbing etc.
- Comparison of the diode clamping inverter, the capacitor clamping inverter and the H-bridge cascade inverter for different applications.

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