Power Loss Investigation in HVDC for Cascaded H-Bridge Multilevel Inverters (CHB-MLI)

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Abstract- **In the last decade, the use of voltage-source multilevel inverters in industrial and utility power applications has been increased significantly mainly due to the many advantages of multilevel inverters, compared to conventional two level inverters. These advantages include: 1) higher output voltage at low switching frequency, 2) low voltage stress (dv/dt) , 3) lower total harmonic distortion (THD), 4) less electro-magnetic interference (EMI), 5) smaller output filter, and 6) higher fundamental output. However, the computation of multilevel inverter power losses is much more complicated compared to conventional two level inverters. This paper presents a detailed investigation of CHB-MLI losses for HVDC. Different levels, and IGBT switching devices have been considered in the study. The inverter has been controlled using selective harmonic elimination in which the switching angles were determined using the Genetic Algorithm (GA). MATLAB-SIMULINK is used for the modelling and simulation. This investigation should result in a deeper knowledge and understanding of the performance of CHB-MLI using different IGBT switching devices.**

Index Terms—**Cascaded H-Bridge Multilevel Inverter (CHB-MLI), Conduction Losses, Switching Losses, Selective Harmonic Elimination (SHE).**

I. INTRODUCTION

Recently, and due to their many technical advantages, multilevel inverters are very widely applied in different power applications from low power to high power and high voltage applications. Main attractions of multilevel inverters compared to conventional two level inverters are producing lower harmonic component at low switching frequency, less losses, lower blocking voltage of switching devices and low electromagnetic interference (EMI) [1]. Practically, there are basically three main topologies of multilevel voltage-source inverters which are well-established in industry. These topologies are: 1) Cascaded H-Bridge multilevel inverter (CHB-MLI), 2) Diode-Clamped multilevel inverter (DC-MLI), and 3) Flying Capacitor multilevel inverter (FC-MLI). The CHB-MLI is preferred for high voltage and high power applications. This is because the CHB-MLI requires the least number of devices among the three basic topologies. In addition, it has a reliable modular structure in which it can be designed and operated at high number of levels with less complexity compared to the DC-MLI and FC-MLI.

It is very important to precisely evaluate the losses in multilevel inverters as the power loss is considered a very important measure value for both cost and system efficiency evaluation. Actually, compared to conventional two level inverters, loss evaluation in multilevel inverter is not an easy task. This is because the current in each device differs within the inverter. In loss evaluation for multilevel inverters, many factors should be considered such as: level of voltage, load, switching devices used and control technique employed.

For a specific voltage and power level, either low number of cascaded H-bridge with high blocking voltage switching devices or a high number of cascaded H-bridge with lower blocking voltage devices can be implemented. The aim of this paper is to investigate the operating of CHB-MLI for a specific voltage and power output using different rating switching devices. The inverter loss is the key parameters in this investigation. In the analysis, all the switching devices are mathematically modelled based on their manufacturer datasheet. Selective harmonic elimination has been applied to control the inverter. In order to solve for the switching angles in SHE problem, genetic algorithm (GA) was applied. At the end of this paper, key findings of this investigation have been summarized.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER (CHB-MLI)

The Cascaded H-Bridge Multilevel Inverters (CHB-MLI) is a basic topology of multilevel inverters in which a series connection of H-bridge inverters is applied. Each bridge has its separate dc source (SDCS). Each bride unit is capable of generating three different voltage levels which then synthesized by the sum of the generated voltage of each cell to obtain the staircase output waveform. The output generated voltage of each single phase H-bridge can be $+V_{dc}$, 0 or $-V_{dc}$. This can be achieved by applying proper switching functions to control the four switches S_1, S_2, S_3 and S_4 of the H-bridge. The CHB-MLI topology has the lowest number of devices when compared to Diode-Clamped (DC-MLI) and Flying Capacitor (FC-MLI). In practice, the separate dc sources (SDCS) are obtained by the use of batteries, fuel cells or PV solar panels [1].

For industrial medium voltage- high power applications, Diode-Clamped (DC-MLI) and Flying Capacitor (FC-MLI) are widely applied when just low number of levels (typically three) is required. On the other hand, Cascaded H-Bridge inverters (CHB-MLI) are most suitable for high voltage-high power, HVDC utility applications. Mainly because of its modular structure that can be extended for high number of
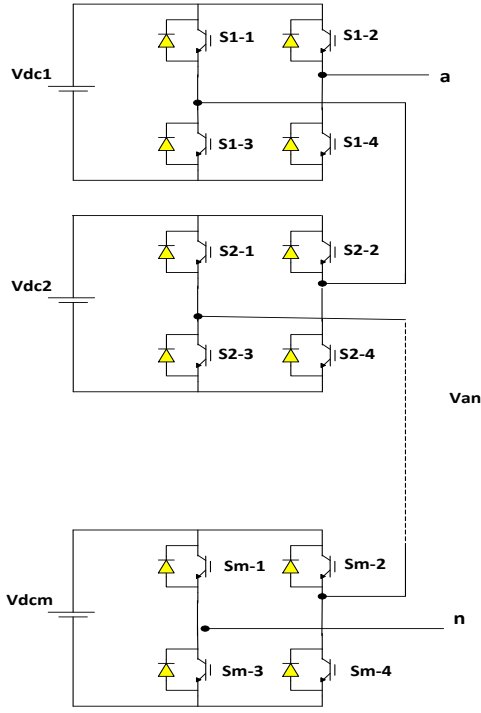
Figure 1. Single-phase m-level cascaded h-bridge inverter circuit layout.

levels with no much complexity. Furthermore, by applying CHB-MLI, higher power and voltage capability can be achieved with lowest number of required devices compared to DC-MLI and FC-MLI. [2-3]

In this paper, CHB-MLI has been considered for high voltage and high power application. Different levels are considered. Figure (1) shows a m-level CHB-MLI circuit layout. The number of levels is equal to $m = 2 \times S + 1$, where m, is number of output levels, S , is the number of cascaded H-bridges.

III. INVERTER CONTROL

For multilevel inverters, there are various control techniques which can be applied to control the output voltage waveform. These control techniques are classified mainly based on the switching frequency f_s into low or high switching techniques Main low frequency technique are Space Vector Control (SVC) and Selective Harmonic Elimination (SHE). At low frequency control, the active power switch is commutated only one or two times within one cycle. On the other hand,   various sinusoidal pulse width modulations (SPWM) are used for high switching techniques in which the power switch is switched many times within a cycle [1].

In this paper, Selective Harmonic Elimination (SHE) was considered to control the inverter. SHE is a low frequency control method, hence result in low switching losses and less EMI because of low switching [4]. Furthermore, it can eliminate the dominant low order harmonic and hence minimize the size of the required filter at the inverter output. This technique is widely applied for HVDC applications.

In SHE, the switching angles are pre-defined to form the desired multilevel fundamental voltage and eliminating the predominant low order harmonics. As a result of this, the total harmonic distortion (THD) is reduced at the inverter output. This is considered open loop control technique as the switching angles pre-calculated off-line.

Figure (2) shows the stepped-voltage waveform for n-level CHB-MLI. It is clear that, there are (n-1) switching angles which can be pre-calculated in this case.
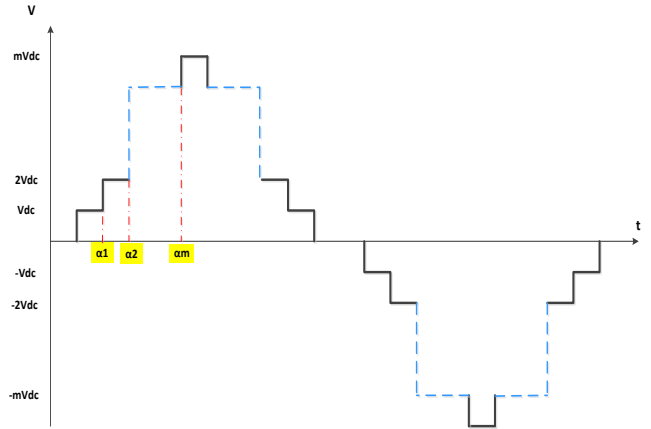

Figure 2. Output stepped-voltage waveform for n-level inverter.

By applying Fourier's expansion, the output voltage stepped wave form can be expressed in sum of sine and cosine periodic signals and a constant. The signal composes of odd and even harmonics. Because of the quarter symmetry of the waveform, the even harmonics and the dc constant are cancelled. Therefore, only odd harmonics are considered. Assuming the three phase system is balanced, all triplen harmonics are zero. Thus, the output voltage waveform can be written as:

$$v_{an}(wt) = \sum_{k=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{k\pi} [cos(k \propto_1) + cos(k \propto_2) \dots + cos(k \propto_s)] \, sin(kwt) \quad (1)$$

Where (S) is the number of H-bride cells of the inverter.

It is clear from Figure (2) that all switching angles are less than 90°, and are all in ascending order. In 7-level CHB-MLI case,

$$\theta_1 < \theta_2 < \cdots \cdots < \theta_S < 90° \qquad (2)$$

And it is possible to eliminate the (S-1) harmonic by solving the following system of non-linear equations where (*mi*) is the modulation index.

$$cos(\theta_1) + cos(\theta_2) + \cdots \cdots + cos(\theta_S) = S \times M_i \qquad (3)$$

$$cos(5\theta_1) + cos(5\theta_2) + \cdots \cdots + cos(5\theta_S) = 0 \qquad (4)$$

$$cos(7\theta_1) + cos(7\theta_2) + \cdots \cdots + cos(7\theta_S) = 0 \qquad (5)$$

$$\vdots \qquad \vdots \qquad \vdots$$
$$\vdots \qquad \vdots \qquad \vdots$$

This system of equations is a highly non-linear. It is also called transcendental equations or SHE equations. The number of equations is equal to (S), where (S) is the number of H-bride cells of the inverter. In order, solve such system, different techniques can be applied. In literatures, iterative and Evolutionary Algorithms are the most commonly used. The Newton-Raphson (NR), as an iterative technique, has been applied extensively for this problem. The main disadvantage is that when the inverter level gets higher, it is getting more difficult to converge into a solution. Furthermore, iterative techniques do need good initial guessed values of the switching angles to help the algorithm to find a solution. However, Evolutionary Algorithms are very powerful and can solve the problem using intelligent approach. The main concept is to transform the problem of SHE into an optimization problem, in which the set of transcendental equations will be the constraints for the optimization. In this research, the problem of SHE for different levels CHB-MLI is solved using genetic algorithm (GA) as it shows better results compared to Newton Raphson (NR) and Particle Swarm Optimization (PSO) [3]. In the next section, a detailed explanation of applying GA for solving SHE is presented.

IV.   GENETIC ALGORITHM (GA) FOR SHE

Genetic Algorithm (GA) is a heuristic global evolutionary optimization algorithm based on mechanics of natural selection and genetics. Compared to other optimization techniques, the main difference is that GA search by population rather than individual points. GA is widely applied for solving both constrained and unconstrained optimization problems. Genetic Algorithm is a simple and easy to implement, hence, it can be easily applied to solve for the switching angles in the problem of selective harmonic elimination [5]. The main process of any Genetic Algorithm optimization consists of five steps which are: 1) Initialization of the population, 2) Evaluation of fitness function, 3) Selection, 4) Apply genetic operators, and 5) Stopping Criterion. Figure (4) demonstrates a general flow chart for genetic algorithm.

STEP_1: *Initialization*

In this step, the algorithm is initialized. All the parameters of the optimization problem are coded. The coding can be in a binary or floating-point string. Based on the coded parameters, a set of solutions is randomly.

STEP_2: *Evaluation of Fitness Function*

To test the goodness of a generated solution in Step_1, a fitness function is to be used as a measure tool. In this analysis, an objective function was defined as a fitness value (FV). Defining the fitness function is a crucial step and should be done very carefully as it has a great effect on the quality of the optimized solution. The objective function should satisfy the fundamental voltage required and eliminate the possible low order harmonics and minimize the THD of the output waveform as well. [3]

$$Obj_F = |V_1 - SM_i|^4 + |V_5|^2 + |V_7|^2 + \cdots + |V_z|^2 + THD \qquad (6)$$

Where V_1, V_5 and V_7 , are the amplitudes of fundamental, 5th and 7th harmonics respectively. V_z , is the most odd harmonic that can be eliminated. S, is the number of cascaded H-bridges.

STEP_3: *Selection*

At selection stage, parents are chosen based on selection rules to produce offspring chromosomes. The selected parents are the main contributors to form the next generation. In this the fittest individual are likely to survive and the less fit are eliminated.

STEP_4: *Crossover and mutation*

In crossover a number of bits are swapped between parents. Here, some genes are exchanged to form a new improved combination. Another very important operator to be applied is called Mutation, in which the genes are alerted.

STEP_5: *Stopping Criterion*

This is very important, it tells the algorithm when to stop and terminate. Therefore, it decides the optimum solution as an output.
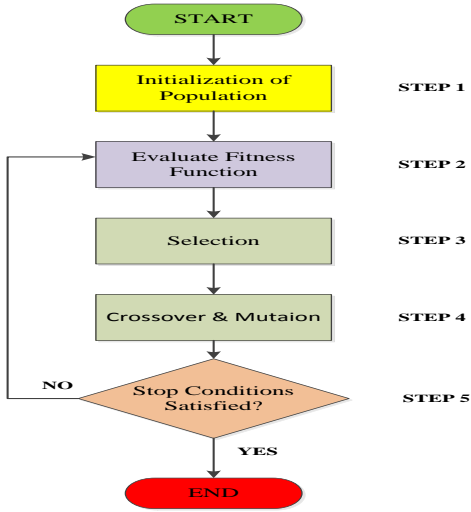
Figure 3. General GA algorithm flowchart. [3]

V. POWER LOSS EVALUATION METHODOLOGY

In the operation of any power electronics devices, there are basically four types of power loss. These are: 1) Conduction losses, 2) Switching losses, 3) OFF-state losses, and 4) Gate losses. In practice, the Off-state and Gate losses are very small and negligible. Only conduction and switching losses have been considered in this investigation. Power loss evaluation in multilevel inverters is a complicated task and requires more critical analysis compared to conventional two level inverters. This is because of the fact that in multilevel inverters, the current in different in each semiconductor device. Hence, each switch has its own loss behavior. The current differ in the switches as a result of having different on-state ratio of each switch for one leg during one period of output phase voltage. In addition to that, at high number of levels, the switching frequency of each switch will not be identical for all switches which add more complexity to power loss calculations. This paper investigates the power loss problem in multilevel inverter. A simplified model is proposed for calculating the conduction and switching losses of CHB-MLI precisely. The proposed model uses the method applied in [2] which based on online calculations. The model is based on on-line calculation in which MATLAB-SIMULINK software has been used for the modelling.

A. Conduction Losses

In a semiconductor device, the device conduction loss is the power loss which occurs while the power device is on the on-state and conducting current. This can be computed by multiplying the on-state saturation voltage by on-state current as follows [6].
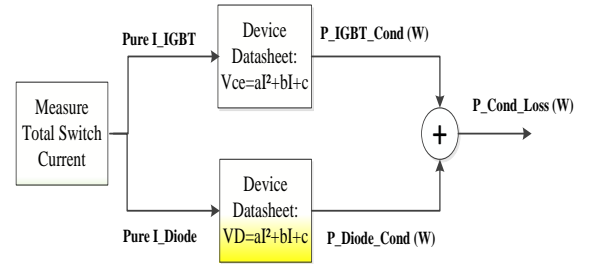
$$p_{Conduction} = |i_c| \cdot v_{on} \qquad (1)$$

Figure 4. Conduction losses calculation block. [2]

In this paper, the on-state voltage is represented by a polynomial equation in terms of the on-state current. Using curve fitting, this equation is obtained based on the actual curves in the device datasheet. Each power device will have two polynomial equations, one for the power switch and one for the anti-parallel diode as shown in figure (4).

B. Switching Losses

The power dissipated during the turn-on and the turn-off switching of the semiconductor device can be defined as the device switching loss. There are the turn-on loss (Eon) and the turn-off loss (Eoff) for a power switch. However, for the anti-parallel diode, the turn-off (Erec) loss is considered only as the turn-on loss is very small and usually neglected. [4]

In order to calculate the switching losses, energy factor curve (K) is obtained by dividing the switching energy by switching current as per the device datasheet. After that, curve fitting tool is used to approximate the energy factor curves by a polynomial equation. Then, to compute the switching losses, first, multiply the energy factor curve equation by the switching current. This gives the energy loss which is then multiplied by the switching frequency to obtain the switching power loss. A normalization factor is added in case of the blocking voltage is different. [2] [4]. The block diagram for switching losses calculation is shown in figure (5). The complete block for the applied modelling of losses calculation in CHB-MLI is presented in Figure (6).
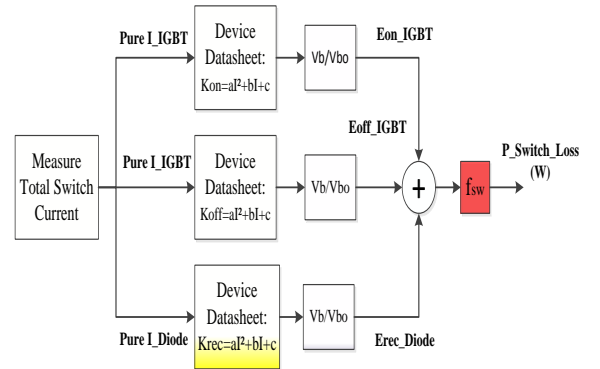

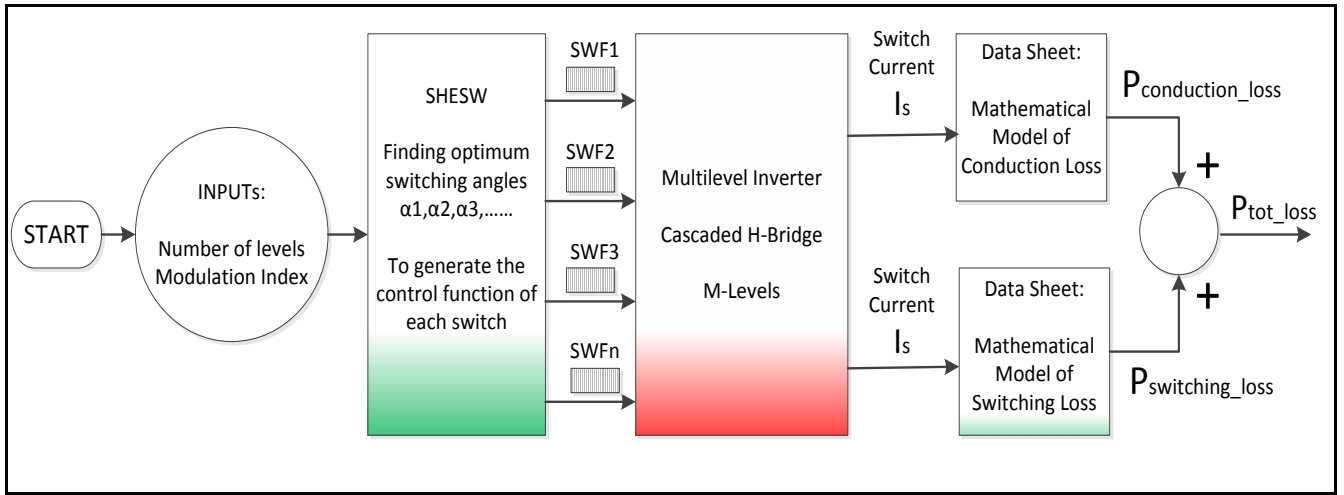Figure 5. Switching losses calculation block. [2]

Figure 6. Basic flow model of applied methodology for losses calculation in CHB-MLI. [2]

VI. SIMULATION RESULTS

This section presents the simulation results carried out in this research. First, a brief explanation of the simulated system and devices is demonstrated. Then, SHE elimination using GA is shown. Finally, the loss investigation results are discussed.

A. Simulation Parameters.

In this analysis the line to line voltage required at the output of the inverter is $V_{L-L} = 11\ kV$, modulation index is $Mi = 0.9$, and the load is $R = 50\ \Omega$, $L = 20\ mH$. The switching devices are of IGBT types which are already available in the market. The devices blocking voltages considered in the anlysis (1.7 kV, 2.5kV, 3.3kV, 4.5 kV and 6.5 kV). The data sheets are given in [8-12].

B. Switching Angles using GA

Based on the considered IGBTs, it is required to investigate multilevel inverters at the following number of levels: 7, 9, 13, 15 and 21 , in order to satisfy the required output voltage. The GA has been implemented to solve the problem of SHE for 7, 9, 13, 15 and 21 levels inverters at 0.9 modulation index. The switching angles obtained are summarized in Table (1).

TABLE 1. GA Solution for Selective Harmonic Elimination (SHE).

Switching Angles	Inverter Number of Levels				
	7	*9*	*13*	*15*	*21*
Θ1	5.4°	5.38°	3.04°	2.41°	2.46°
Θ2	16°	12.83°	8.65°	7.05°	5.61°
Θ3	35°	25.61°	13.35°	12.20°	15.07°
Θ4	-----	40.39°	23.09°	19.08°	28.76°
Θ5	-----	-----	28.88°	23.20°	33.98°
Θ6	-----	-----	42.06°	33.06°	38.85°
Θ7	-----	-----	-----	43.43°	43.83°
Θ8	-----	-----	-----	-----	48.76°
Θ9	-----	-----	-----	-----	70.59°
Θ10	-----	-----	-----	-----	81.99°

C. Inverter Losses

The inverter conduction loss and switching loss have been calculated for different number of levels and using different IGBTs as a power switching devices. Figures (6) (7) and (8) shows the conduction, switching and total loss respectively.

The simulation results show that the inverter conduction loss is directly proportional to the inverter number of levels. As the number of inverter level increases, the conduction loss also increases. On the other, hand the switching loss decreases as the inverter number of levels increases.
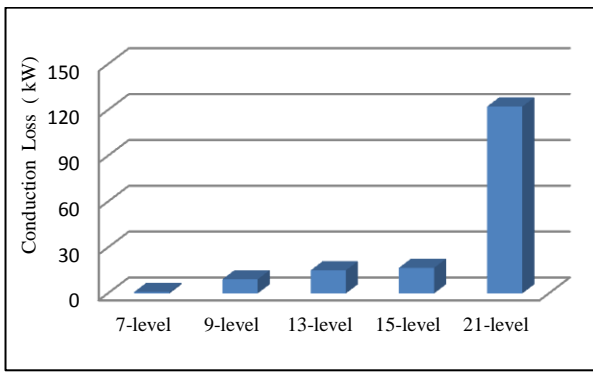
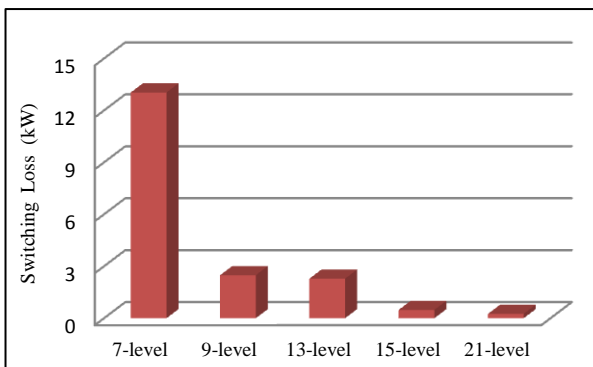Figure 6. Inverter conduction losses at different levels.

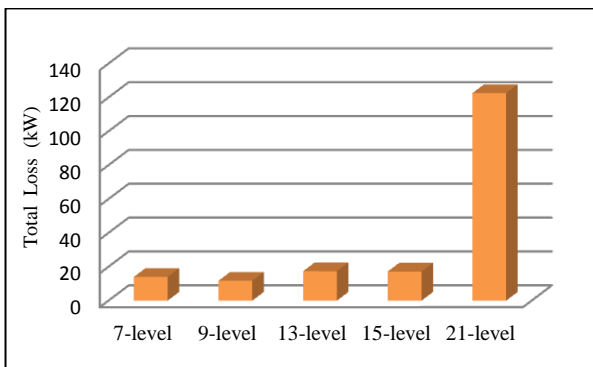Figure 7. Inverter switching losses at different levels.

Figure 8. Inverter total losses at different levels.

From other point of view, the voltage total harmonic distortion (THD) at the inverter output also is related to the applied number of levels. It is a well known fact is that one advantage of multilevel inverters compared to conventional two level inverters is the reduction in THD obtained at the inverter output. In this investigation, the THD has been studied at different levels and the results show that as the number of levels increase, there will be a decrease in the THD. Table (2) compares the THD at different levels.

TABLE 2. THD at different inverter levels

Inverter Number of Levels	%THD
7 – level	5.2
9 – level	3.8
13 – level	2.09
15 – level	1.9
21– level	1.61

It clear from the table that at 21-level, the THD is small and this help in minimizing the size required output filter. Further investigation of inverter loss has been conducted by changing the load level. In this analysis the losses has been calculated at 100% , 70% and 50% of load. As an example of obtained results and study of load changing on the losses, 13-level inverter is considered here below in figure (9).
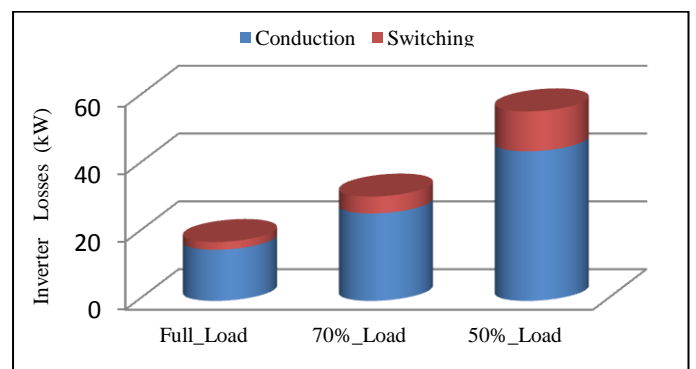

Figure 9. 13-level inverter losses at different load levels.

VII.   CONCLUSION

Losses evaluation of multilevel inverters has been investigated in this paper. Throughout the analysis CHB-MLI topology is chosen as it is more suitable for high power and high voltage applications. The inverter conduction and switching losses was calculated using online precise model based on actual currents and actual curves as per the devices datasheet. Different IGBTs devices included in the analysis. The inverter was controlled using selective harmonic elimination. Genetic algorithm (GA) has been implemented successfully to solve for the switching angles. In the simulation results, it has been found that the conduction loss increases as the inverter levels increase.   However, the switching loss decreases as the number of inverter level increase. The total losses found to be increasing as the many levels is used. But the THD declined significantly when operating at high number of levels.

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