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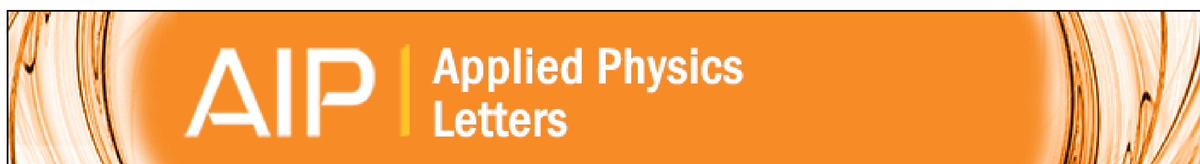

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Memristive operation mode of a site-controlled quantum dot floating gate transistor

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We have realized a floating gate transistor based on a GaAs/AlGaAs heterostructure with site-controlled InAs quantum dots. By short-circuiting the source contact with the lateral gates and performing closed voltage sweep cycles, we observe a memristive operation mode with pinched hysteresis loops and two clearly distinguishable conductive states. The conductance depends on the quantum dot charge which can be altered in a controllable manner by the voltage value and time interval spent in the charging region. The quantum dot memristor has the potential to realize artificial synapses in a state-of-the-art opto-electronic semiconductor platform by charge localization and Coulomb coupling. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4921061]

In 1971, Chua postulated the existence of a fourth fundamental circuit element beside the capacitor, inductor, and resistor.[1,2] This circuit element, now known as memristor, combines the functionality of a switchable resistor (transistor) with memory. Since the pioneering work by Strukov *et al.* in 2008,[3] which described resistance switching in thin TiO_2 layers with oxygen deficient with a memristive model, memristive switching has been identified in various material systems including oxide films,[4–6] silver compounds,[7,8] spin memristive systems,[9] and floating-gate transistors.[10,11] Memristors are characterized by a pinched hysteresis loop with a state and time dependent resistance or conductance which depends on the previous charge flow through the device.[1–3] This state-dependent conductance enables memristors to emulate artificially the functionality of synapses,[12,13] the connections between neurons in neural networks. The strength of these connections can be tuned dynamically depending on the time difference of pre- and post-synaptic pulses,[14,15] a crucial scheme for learning in neural networks.[16,17] Artificial synapses are key building blocks in brain-inspired, non-von Neumann architectures with a parallel computing scheme which can for instance be used to implement multiobject detection and classification.[18]

Here, we demonstrate a memristive operation mode of a quantum dot (QD) floating gate transistor by short-circuiting the source contact of the quantum wire (QW) and lateral gates. The memristive operation mode appears due to the Coulomb interaction of QD localized charges with the nearby QW, which leads in one sweep direction of the voltage to a smaller and in the other sweep direction to a larger conductance. We also examined the amount of QD-localized charges which can be controlled via the charging voltage or the time interval spent in the charging region. The memristive operation mode is observed up to temperatures of 165 K. The application of rectangular voltage pulses to the source and drain contacts of the device allows to tune the conductance in dependence on the time difference of the pulses. This mimics the increase (potentiation) and decrease (depression) of synaptic strength between two neurons by changing the relative timing of pre- and post-synaptic pulses.

Fig. 1(a) depicts an electron microscope image of the studied device. A GaAs/AlGaAs heterostructure was grown by molecular beam epitaxy, forming a two-dimensional electron gas (2DEG) 90 nm below the surface. Precise positioning of the InAs QDs was realized by a growth step with InAs after defining a regular pattern of 50 nm deep nanoholes. The whole structure was covered with a GaAs layer. Lateral gates

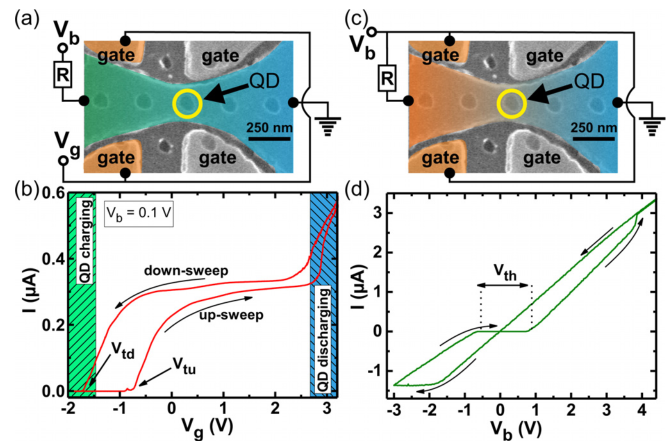

FIG. 1. (a) Electron microscope image of the device and circuit diagram for the floating gate operation mode. The dark contrasts indicate the positions of the QDs and the etched trenches which electrically isolate the quantum wire from the lateral gates. The lateral gates and the QW are connected to the gate voltage V_g and the bias voltage V_b, respectively. A yellow circle highlights the QD in the center of the QW. (b) I-V_g-characteristic in the floating gate operation mode. The arrows indicate the sweep cycle directions as well as the corresponding threshold voltages V_{td} and V_{tu}. (c) Circuit diagram to realize the memristive operation mode. The bias voltage V_b is applied simultaneously to the top contact of the QW and the lateral gates. An additional resistance with 1 MΩ is used in series to the QW. (d) I-V_b-characteristic in the memristive operation mode. A pinched hysteresis loop with a width V_{th} of the low conductive state is observed.

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and a quantum wire structure were realized by electron beam lithography and dry chemical etching. The dark contrast in the electron microscope image indicates the positions of the QDs and the etched trenches to electrically isolate the gates from the QW. A more detailed description of the growth and positioning techniques is given in Refs. 19 and 20.

The device can be operated in two operation modes: the floating gate mode and the memristive mode. Fig. 1(a) displays the circuit diagram in the floating gate operation mode. For this purpose, a constant bias voltage V_b was applied to the left contact of the QW (source) while a gate voltage V_g was applied to the lateral gates. The right contact of the QW (drain) is used as common ground. The current I was determined as voltage drop across a resistor with 10 kΩ in series to the QW. If not stated differently, the measurements were conducted at 4.2 K in the dark. Fig. 1(b) shows the I-V_g characteristic of the device in floating gate operation mode. The gate voltage was swept with a rate of $\Delta V_g/\Delta t = 0.2$ V/s from -2.0 to 4.0 V (up-sweep direction) and back (down-sweep direction), and the bias voltage was set constantly to $V_b = 0.1$ V. The arrows indicate the gate voltage sweep cycle directions and the corresponding threshold voltages V_{tu} and V_{td} for the up- and down-sweep direction, respectively. For small gate voltages, the QW is depleted and the QD becomes charged.[20,21] After exceeding V_{tu}, the current increases monotonically. V_{tu} depends on the number of QD localized charges and the capacitive couplings between the gate, the QD, and the QW.[22,23] The QD becomes discharged for large gate voltages, leading to an enhanced current and a smaller threshold voltage during the down-sweep direction. The approximate gate voltage ranges for charging and discharging the QD are indicated by the shaded regions in Fig. 1(b).

In the memristive operation mode, the bias voltage was applied simultaneously to the source contact of the QW and the lateral gates (see Fig. 1(c)). An additional resistance with 1 MΩ is connected in series to the channel. The I-V_b characteristic in the memristive operation mode is depicted in Fig. 1(d). The voltage was swept between 4.6 V and the minimum value $V_{bm} = -3.0$ V. A pinched hysteresis loop, the finger print of memristors,[1,2] is observed. The differential conductance around zero bias voltage is 0.7 μS for the down- and almost zero for the up-sweep direction. Charging of the QD occurs for $V_b < -1.9$ V (almost zero differential conductance) which corresponds to the charging region in the floating gate operation mode. The Coulomb interaction of QD localized charges with the QW results in the low conductive state with almost zero conductance. The current increase at 3.8 V is attributed to a discharging of the QD. We observe that the voltage ranges for charging and discharging differ from sample to sample because of varying geometries and quantum dot positions leading to small deviations in the current-voltage characteristic and pinched hysteresis loop.

Fig. 2(a) shows current-voltage-characteristics conducted in the memristive operation mode for different V_{bm}. No pinched hysteresis loop is observed above -1.8 V. For smaller V_{bm} (-2.2 and -3.2 V), two distinguishable conductive states (low and high) around zero bias are clearly evident. The widths of the low conductive states are 0.1 and 1.7 V. They can be related to the voltage V_{tu} of the current-onset in the floating gate operation mode with $V_{th} \approx 2V_{tu}$.

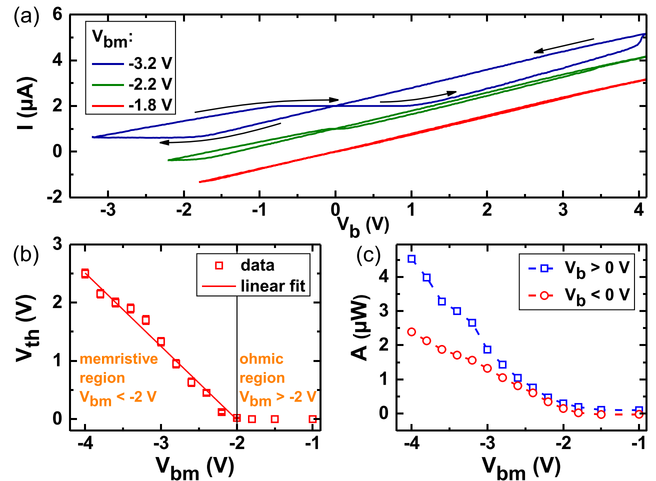

FIG. 2. (a) I-V_b-characteristic of the memristive operation mode for three different minimum bias voltages $V_{bm} = -1.8$, -2.2, and -3.2 V. The pinched hysteresis loop is observed only when the QD is charged and discharged during the sweep cycle. No hysteresis is observed for $V_{bm} = -1.8$ V. For clarity, the curves are offset by 1 μA. (b) Width V_{th} versus V_{bm}. For $V_{bm} < -2.0$ V, the width increases almost linearly. Above $V_{bm} > -2$ V, the number of localized charges remains constant during the sweep cycle. (c) Area A enclosed by the hysteresis loop versus V_{bm}. The area is displayed for positive and negative bias voltages. A increases linearly below but is almost zero above -2.0 V.

Fig. 2(b) shows the plateau width versus V_{bm}. It remains zero above (ohmic response) and increases almost linearly below -2.0 V (memristive response). We attribute this linear shift to the threshold voltage shift $\Delta V_{tu} = \Delta nq/C_{eff}$ of a floating gate transistor in close vicinity to a QD.[22] Here, Δn is the shift of the number of localized charges, q is the elementary charge, and C_{eff} accounts for the effective capacitive coupling between the QD, the 2DEG, and the gate. In the memristive operation mode, charging of the QD occurs for $V_b < -1.9$ V and thus Δn is determined by $\Delta n = (-1.9\,\text{V} - V_{bm})/\Delta V$ with ΔV being the voltage difference to charge the QD with one additional electron. Δn is only defined for $V_{bm} \leq 1.9$ V. For larger V_{bm}, the QD is not charged and we observe linear current-voltage-characteristics (ohmic response). Since $V_{th} \approx 2V_{tu}$, the width of the low conductive state is

$$V_{th} \approx \frac{2q}{\Delta V\, C_{eff}}(-1.9\,V - V_{bm}). \tag{1}$$

The data in Fig. 2(b) were fitted according to Eq. (1) with a shift of $\Delta V \times C_{eff} \approx 0.28 \times 10^{-18}$ C. The memristive operation mode can also be analyzed by means of the area A, which is enclosed by the pinched hysteresis loop. Fig. 2(c) shows A for positive and negative bias voltages versus V_{bm}. Similar to the plateau width, A is almost zero above but increases linearly below -2.0 V. Both V_{th} and A depend on the shape of the pinched hysteresis loop, which correlates to the constitutive relation of the memristor (ideal memristor: $f(\varphi,q) = 0$ with flux φ).[24] Hence, different realizations of memristors result in different shapes and the area is a characteristic parameter of the memristive operation mode.

In Fig. 3(a), current-voltage-characteristics of the memristive operation mode are plotted for different temperatures $T = 4.2$, 145, and 240 K. The bias voltage was swept from -3.5 V to 4.0 V and back. Well defined pinched hysteresis

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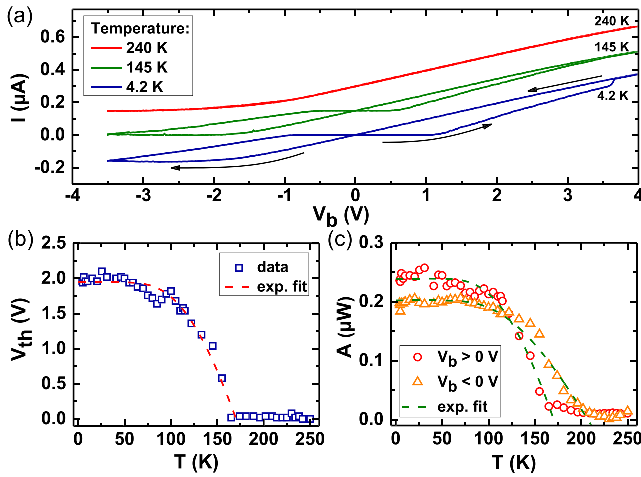

FIG. 3. (a) Current-voltage characteristics of the memristive switching mode for temperatures of 4.2, 145, and 240 K. The pinched hysteresis loop is profound for 4.2 and 145 K, with its two clearly distinguishable conductive states around zero bias. No pinched hysteresis loop is observed for T = 240 K. The curves are offset by 0.15 μA. (b) Plateau width of the low conductive state versus temperature. The maximum operating temperature is found to be 165 K, as obtained from the exponential fit function after Eq. (4). No low conductive state is observed for higher temperatures. (c) Area of the hysteresis for positive and negative voltages versus temperature. The exponential fit functions are based on Eq. (4).

loops are observed for the temperatures ranging between 4.2 and 145 K. For 240 K, the currents during the up- and down-sweep directions cannot be distinguished, thus $A = 0$. The width of the low conductive state around zero bias as well as the area of the hysteresis loop versus the temperature are shown in Figs. 3(b) and 3(c), respectively. V_{th} and A remain almost constant below, but are lowered for temperatures above 50 K. The reductions of V_{th} and A are associated with thermally activated discharging processes of the QD.[21,25] The number of localized charges n on the QD is given by the rate equation[26]

$$\frac{dn}{dt} = \Gamma_{cha} - n\,\Gamma_{dis}. \tag{2}$$

Γ_{cha} and Γ_{dis} are the rates of thermally assisted charging and discharging processes, respectively. These rates can be examined using an Arrhenius type escape rate[27]

$$\Gamma = \Gamma_0 \exp\left[-\frac{E_\alpha}{kT}\right]. \tag{3}$$

Here, E_α are activation energies with $\alpha = \mathrm{cha}$, dis for the charging and discharging processes, respectively, and k is the Boltzmann constant. From the steady state solution ($dn/dt = 0$), we obtain V_{th}, which is directly proportional to the number n of charges on the QD, as

$$V_{th}(T) = V_0 \exp\left[-\frac{E_{cha} - E_{dis}}{kT}\right] + V_{th}(T = 0\,\mathrm{K}). \tag{4}$$

The data in Fig. 3(b) have been fitted according to Eq. (4). The fitting parameters are $V_0 = -47.1$ V, $V_{th}(T = 0\,\mathrm{K}) = 1.9$ V, and $\Delta E = E_{cha} - E_{dis} = 46.8$ meV. ΔE represents the energetic distance between the electrochemical potentials of the 2DEG with activation energy E_{cha} and the QD with activation energy E_{dis}. The areas of the pinched hysteresis loops in Fig. 3(c) are also fitted according to Eq. (4). The parameters are $A_0 = -5.78\,\mu$W, $A_{th}(T = 0\,\mathrm{K}) = 0.24\,\mu$W and $A_0 = -2.78\,\mu$W, $A_{th}(T = 0\,\mathrm{K}) = 0.20\,\mu$W for $V_b > 0$ V and $V_b < 0$ V, respectively. The difference of the activation energies was kept constant with $\Delta E = 46.8$ meV. For positive voltages, the area vanishes for a temperature of 170 K, whereas it is still present for temperatures up to 210 K for negative voltages. The low temperature current-voltage characteristic and pinched hysteresis loop of the device is independent and insensitive to temperature cycles.

We also analyzed the conductance change in the memristive operation mode when applying rectangular voltage pulses as shown in Fig. 4(a). These pulses mimic the input from a pre- and a post-synaptic neuron. The post-synaptic pulses with amplitude V_{po} were applied to the QW and the pre-synaptic pulses with amplitude V_{pr} to the QW and the gates (see Fig. 4(b)). The pulses had a width of 10 ms and the time difference Δt was varied. After each pulse, the conductance G was determined with a read-out pulse (dashed line). Fig. 4(c) depicts the voltage difference of the pulses. Discharging of the QD can occur during the red highlighted voltage range when the difference of both pulses exceeds the threshold voltage for discharging. The conductance versus the pulse number for amplitudes $V_{pr} = 3.8$ and $V_{po} = -0.8$ V

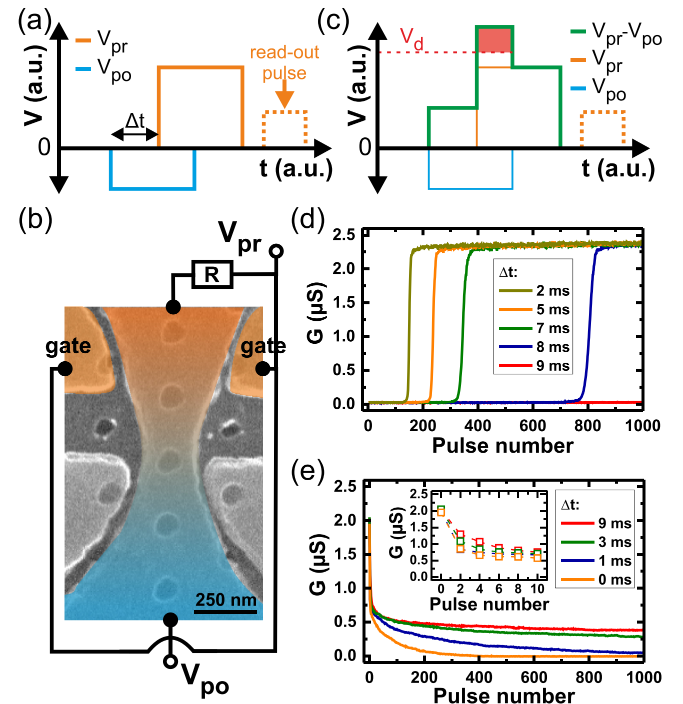

FIG. 4. (a) Time trace of the pre- and post-synaptic voltage pulses which are applied to the source and the drain side, respectively. A read-out pulse with amplitude 1.2 V follows the pulses to determine G. (b) Circuit diagram when applying pre- and post-synaptic pulses to the two terminals of the memristor. (c) Difference of the post- and pre-synaptic pulses shown in (a) versus time. During the red shaded time interval, the voltage difference exceeds the threshold voltage for discharging V_d. (d) Conductance G versus pulse number. The pulses shown in (a) are applied to the memristor and the conductance can be potentiated. Depending on Δt, the potentiation occurs after different pulse numbers. (e) G versus pulse number for a depression of the conductance. For smaller Δt, less pulses are needed to decrease G to zero. The inset shows the conductance after the first pulses in more detail.

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is presented in Fig. 4(d). Initially, the QD was charged and the conductance was almost zero. G remains unaltered when applying 1000 pulses with a time difference of 9 ms. Lowering Δt to 8 ms results in an increase after 780 pulses and the conductance saturates at 2.4 μS. This saturation is attributed to a completely discharged QD. Less pulses are needed to discharge the QD when the time difference is reduced. The amplitudes -2.4 V and 0.8 V of the pre- and post-synaptic pulses, respectively, are used to decrease the conductance of an initially charged QD. The data are shown in Fig. 4(e). For different Δt, the conductance is reduced by a large amount with only a few pulses. For smaller Δt, the change of G is larger (see inset of Fig. 4(e)). The decreasing conductance is attributed to a charging of the QD with electrons, which can be controlled with the time difference between the pre- and post-synaptic pulses.

In summary, we have presented a quantum dot floating gate transistor featuring a memristive operation mode. Sweeping closed voltage cycles allows to charge and discharge QDs in close vicinity of a 2DEG, resulting in a pinched hysteresis loop with two clearly distinguishable conductive states around zero bias. The memristive operation mode is observed up to temperatures of 165 K. The conductance of the device can be controlled by the charging voltage or the time difference between rectangular voltage pulses applied directly to the source and drain contact. The presented QD floating gate transistor with its memristive operation mode may be considered to realize artificial synapses in future non-von Neumann computer architectures.

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