Low-Power In-Circuit Testing of a LNA

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Abstract — A new technique is proposed to tackle in-circuit testing of embedded RF blocks. It relies on observing the cross-correlation between its output voltage and power supply current, using a translinear cross-correlator circuit. Although a structural test is performed, simulation results show that fault detection criteria can be established based on acceptable deviations of performance characterization parameters. The case of a Low Noise Amplifier is presented.

Index Terms — RF, testability and test techniques, low noise amplifier.

I. Introduction

New design for testability (DfT) techniques and test methods are required to cope with the difficulties of testing deeply embedded radio frequency (RF) blocks, in order to allow for a faster yet economical testing [1]. In fact, the majority of analogue and RF circuitry in today's high volume applications resides in system on chip (SoC) and system in package (SiP) designs which require new test equipment paradigms to break the traditional barriers between digital, analogue, RF, and mixed-signal.

While significant effort has been put on improving technological processes in order to obtain ever performing and miniaturized products, test methodologies are essentially still based on conventional approaches, which include the measurement of different quantities [2]. Although the performance of automatic test equipment (ATE) has increased, and allow faster test operations, accessing difficulties and ATE high cost may impair the reduced profit margins dictated by market pressures.

The RF blocks of most wireless systems (e.g., GSM, DCS 1800, and DECT) have a high degree of commonality, even though there may be many variations in practice. The block diagram of a typical wireless transceiver is shown in Fig.1. The basic function of the transmitter is to modulate the base-band information onto a high frequency carrier signal that can be radiated by the antenna. The output of the modulator is referred as the intermediate frequency (IF) signal, ranging usually between 10MHz and 100MHz. The IF signal is then shifted up in frequency, or up-converted, to the desired RF transmit frequency using a mixer. The mixer operates by producing the sum or difference of the IF signal frequency and of the frequency of a separate local oscillator (LO). The power amplifier (PA) increases the output power of the transmitter.

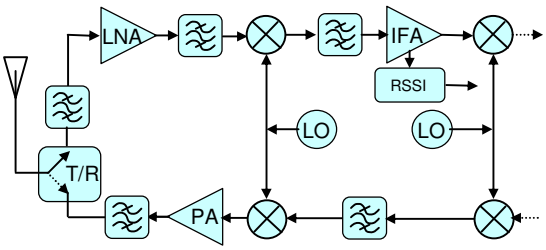

Fig. 1 – Block diagram of a basic heterodyne transceiver.

The receiver recovers the transmitted base-band data by essentially reversing the functions of the transmitter components. The low-noise amplifier (LNA) amplifies the eventually very weak received signal, while minimizing the added noise power. As the LNA is the first stage in the receiving path, its noise is critical for the whole receiver's noise figure and sensitivity. For large signal levels the LNA should not introduce significant distortion to avoid interference. It is therefore a very critical block in radio receiver systems.

The LNA output signal is down-converted to a lower IF signal by a mixer. The LO frequency is then set close to that of the RF carrier input, to enable limiting the mixer output to relatively low frequencies (in most cases less than 100MHz). A high gain IF amplifier raises the power level of the signal so that the base-band information can be recovered more easily in the demodulator. This is known as a heterodyne type receiver, because it uses frequency conversion of the relatively high RF carrier frequency to a lower IF frequency before final demodulation. In more recent architectures modulation and demodulation tend to be carried-out in the digital domain.

Two main approaches have been followed in the development of RF in-circuit testing techniques:

- to test each block individually
- to treat the entire RF front-end as a single block seen from the base-band input and output elements, after connecting the PA output onto the LNA input to create a loop-back signal path

In the first case test methodologies are developed focusing on each single block. As an example, the switch matrix presented in [3] allows defining different configurations to test the down-mixer, the demodulator, the modulator, and the up-mixer. Specific signal processing schemes are required to capture and extract information from the high-frequency, modulated signals observable at each block output, such as presented in [4]. The BiST technique proposed in [5] to measure impedance, gain and noise figure require the inclusion of 3 switches, one extra amplifier and two peak-detectors, but allows using a DC meter to perform the measurements.

In the second approach one avoids to interfere in the high-frequency signal paths. In [6, 7] the characterization of the RF front-end transfer function is carried-out after the analysis of spectral and time signatures captured in the base-band receiver interface. A stimulus composed by an optimized sequence of voltage levels is used in [6], while in [7] an Orthogonal Frequency Division Multiplexing (OFDM) stimulus comprising different frequencies is employed. The comparison between test response signatures and the respective golden ones allows also obtaining information about some characterization parameters. In [8] the inclusion of multiplexers in the antenna interface node allows injecting a stimulus directly into the receiver input to test this block separately, or to test the entire transceiver in a loop-back configuration.

In summary, the techniques in the first group allow diagnosing which block in a RF front-end is defective, and to propagate test signals without being affected by the other blocks inserted in the signal path, but imply a higher overhead in test circuitry. On the other hand, the ones in the second group minimize the circuitry overhead but don't allow identifying which block(s) are behaving incorrectly. The loop-back approach allows re-using transceiver's functional blocks for in-circuit testing operations. However, some architectures and secondary effects, such as an increase in power consumption, may impair the use of loop-back techniques [9]. On the other hand, as the signal path is longer, and involves different modulation and demodulation operations, fault coverage may be impaired.

Two aspects are important in the development of in-circuit RF testing schemes – low power consumption and re-use of existing blocks in order to minimize area overhead and performance degradation.

The work presented here addresses the in-circuit structural testing of the LNA, relying on the observation of the cross-correlation between the output voltage and the power supply current ($v \otimes i$). To perform this operation a current correlator cell is used which requires low power consumption and low implementation area, allowing thus for a low impact on power consumption and area overhead. The impact on performance degradation can also be minimized taking into consideration the correlator's input impedance connected to the LNA output node at the design stage. A simple sinusoidal stimulus is used which can be obtained from the output of the up-converter, provided an extra switch is used to connect it to the LNA input (Fig.2). This allows avoiding both the power consumption and the eventual non-linearity introduced by the PA.

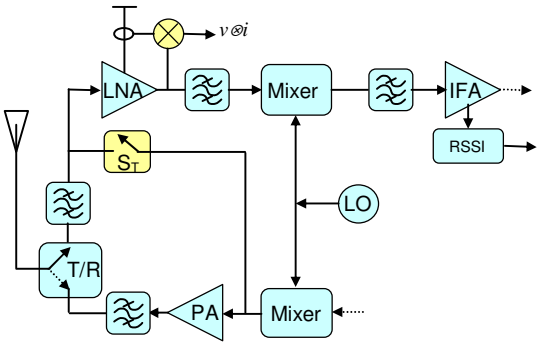

Fig. 2 – Block diagram of transceiver including test features.

Next section describes the cross-correlator circuit being proposed to obtain the $v \otimes i$ signature in-circuit. Section III presents simulation results which confirm the validity of this testing scheme. Conclusions are highlighted in section IV.

II. CROSS-CORRELATOR CIRCUIT

The cross-correlation between a circuit's dynamic output signal (in this case a voltage one, v) and the respective power supply current (i_{DD}), was proposed in [10] as a means to assure an effective structural test of analogue and mixed-signal circuits. In fact, as it is shown by (1), where a faulty signal is modelled as resulting from the good one added with a deviation, $x^F = x^G + \partial x$,

$$\Re v^F i_{DD}^F(\tau) = \tag{1}$$

$$= \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} (v^G(t) + \partial v\ (t))(i_{DD}^G(t+\tau) + \partial i_{DD}(t+\tau))dt =$$

$$= \Re v^G i_{DD}^G(\tau) + \Re v^G \partial i_{DD}(\tau) + \Re \partial v\ i_{DD}^G(\tau) + \Re \partial v\ \partial i_{DD}(\tau)$$

the deviations of either or both v and i_{DD} due to defective behaviours (δv and δi_{DD}), are compressed after cross-correlation into a single $v \otimes i$ signature. That is, $\Re v i_{DD}$ provides a signature that reveals a different degree of similarity between the two signals, which after being compared with the golden signature allows detecting the presence of faults that affect only one or both of v or i_{DD}. Furthermore, observing the dynamic signals allows detecting faults not observable with the static ones, namely I_{DDQ}, which do not translate completely the circuit's dynamic behaviour.

Different circuits exist to implement the cross-correlation function. However, most of these are complex to be used

within a RF transceiver for testing purposes. Using only the cross-correlation for the zero delay value, a simpler circuit can be used. A shorter signature may reduce fault coverage, particularly in the cases where deviations are small, but as it will be shown, it still guarantees a high detectability.

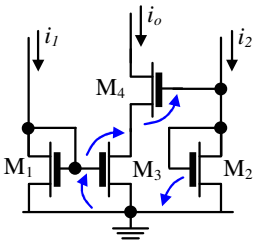

Fig. 3 – Current correlator cell.

Fig. 3 shows the current correlator cell [11] being used here, whose transistors are assumed to operate in the subthreshold region, i.e.,

$$i_{DS} = I_S \frac{W}{L} e^{K v_G} (e^{-v_S} - e^{-v_D}) \quad (2)$$

where I_S is the transistor's specific current, v_G, v_S, and v_D are respectively the transistor's gate, source, and drain voltages, K≈0.7 is the back-gate coefficient, and the voltages are given in units of the thermal voltage ($U_T = kT/q \approx 26$ mV at 300ºK).

It can be shown by developing the sum of voltages in the translinear loop shown in Fig. 2 ($-v_{GS1} + v_{GD3} - -v_{GS4} + v_{GS2} = 0$), and assuming that all transistors except M3 are saturated, the output current becomes

$$i_O = \frac{i_1 i_2 r_{31} r_{42}}{i_1 r_{31} + i_2 r_{42}} \quad (3)$$

where $r_{31,42}$ are the transistors dimensions ratios, respectively, $\frac{W_3/L_3}{W_1/L_1}$, $\frac{W_4/L_4}{W_2/L_2}$. Equation (3) shows that i_O computes a self-normalized correlation of currents i_1 and i_2, which is symmetric in the two input currents. If the transistors operate in strong inversion the output current function is more complicated and is asymmetric. However, for the purpose envisaged here both modes can be used, as long as a signature reporting the behaviour of the two input signals is desired.

III. Simulation Results

This current correlator was then used to obtain a signature of the cross-correlation between output voltage and power supply current of a MOS LNA. One of the correlator's input currents is generated after the LNA's output voltage v, the other is obtained from the power supply current sensor i_{DD}, and i_O is converted into an integrated output voltage ($v_{v\otimes i}$), that is

$$v_{v\otimes i} = \frac{vg \times i_{DD} h}{vg + i_{DD} h} r_o \quad (4)$$

where g is the transconductance gain defined by i_1, r_{31} and v, h is the current gain defined by i_2, r_{42} and i_{DD}, and r_o is the correlator's output transresistance. The current sensor transfer gain, the v capacitor and coupling transistor, the transistors' ratios $r_{31,42}$ and correlator's output RC load determine g, h, and r_o gains.

Fig. 4 illustrates the LNA which was used to obtain preliminary simulation results. It is a MOS cascode LNA with inductive source degeneration [12] with a RLC load tuned at 315MHz.

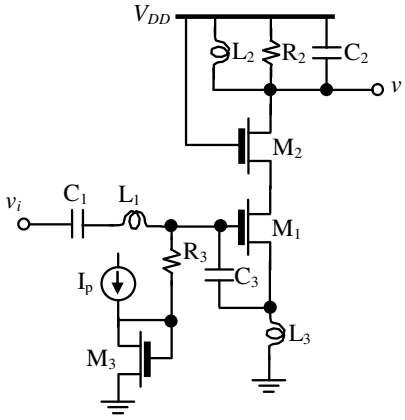

Fig. 4 – MOS LNA used in the simulations.

Its nominal characteristics are: input reflection coefficient S_{11}=-11.6 dB, power gain S_{21}=12.3dB, input 1dB compression point P_{i1dB}=-3.94 dBm, third-order interception point IP_3=1.95 dBm, and noise figure NF=1.25 dB10.

Faults were simulated to evaluate the correlator's detectability. These include catastrophic (shorts and opens) and parametric deviations (doubling and halving in passive components values and transistors' width) – a total of 15 catastrophic and 22 parametric faults.

For each fault the values of S_{11}, S_{21}, and P_{i1dB} functional parameters were also measured to evaluate whether the circuit should be considered faulty or not based on the evaluation of these functional parameters, and not on a simple arbitrary percentage deviation of the correlator's output voltage. Monte Carlo simulations for technology's process deviations of the full circuit, i.e., including also the correlator, were also carried-out to consider these variations in tolerance bands.

The graph shown in Fig. 5 illustrates the values obtained observing correlator's output voltage $v_{v\otimes i}$ for each simulated fault. The first 15 values correspond to

catastrophic faults, and the following ones to parametric faults. The dashed line at 1.59V corresponds to the nominal voltage observed within the non-faulty circuit. The far-end values above this line (3 V) are due to a significant decrease in power supply current, and those below to an increase.

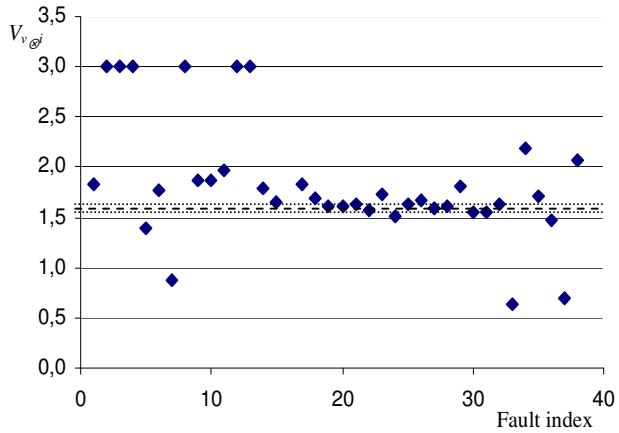

Fig. 5 – Correlator's output voltages per fault.

One can see here the advantage of observing the cross-correlation signal. In the case of, namely, fault no. 36 (due to a 50% reduction of M_3 width), the power supply current is doubled, but the output voltage only shows a 20% increase in amplitude – the worst corresponding functional parameter variation is a 27% reduction of P_{i1dB} to -5.2 dBm. On the other hand, in the case of fault no. 5 (L_2 short-circuited) there is no change in I_{DDQ}, but i_{DD} peak to peak amplitude is multiplied by ~7.

Evaluating the values of the functional parameters for the parametric faults, one can conclude that:

-fault no. 21, the doubling of R_2 (what would correspond to a decrease of the inductor's quality factor) does not affect S_{11}, S_{21}, and P_{i1dB} parameters

-fault no. 18, the doubling of L_2, only leads to a 3.7% reduction of S_{21}

-the detectability of the other faults depends on the limits adopted for the tolerance band

Concerning the definition of these limits if one can tolerate:

- a reduction of S_{21} to 11.5 dB
- values of S_{11} in the interval $-12.05 \leq S_{11} \leq -9.22$
- variations of P_{i1dB} in the interval $-4.12 \leq P_{i1dB} \leq -3.73$

the limits for the admissible correlator's output voltages are $1.57 \leq v_{v_{\otimes}i} \leq 1.62$ V (doted lines in Fig. 5). Considering then these limits all but 7 faults are detected. These 7 non detected faults correspond to doubling and halving L_2, R_2, C_2, and W_{M2}, and doubling of C_1. Fig. 6 illustrates the evolution of the S_{21} parameter in golden (plain line) and in the L_2 doubled cases (dashed line), and Fig. 7 shows P_{i1dB} when L_2 is halved. In both cases it can be seen that the parameters' variations due to the faults are small.

The correlator's output being a DC voltage allows a low frequency analogue bus to be used to observe this signal, making then it easy to include this testing scheme in the global testing strategy of a large chip using simple test equipment.

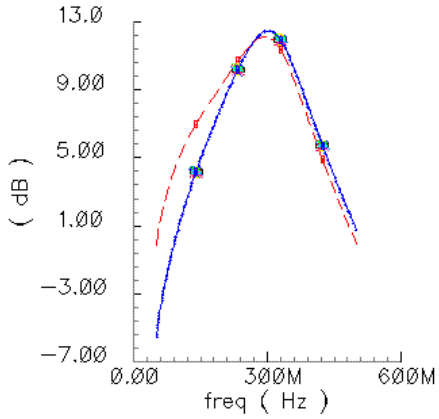

Fig. 6 – S_{21} for golden (plain) and 2xL_2 (dashed) cases.

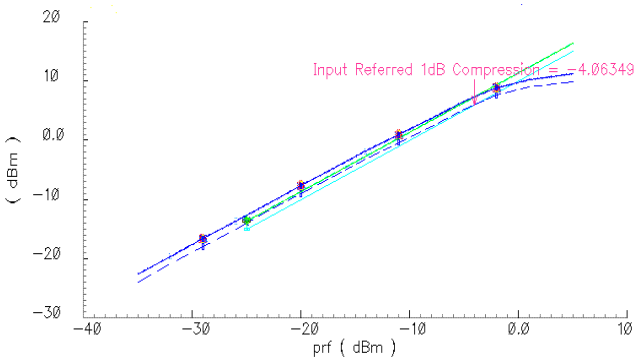

Fig. 7 – P_{i1dB} for golden (plain) and L_2/2 (dashed) cases.

As the transistors in the correlator are operating in the subthreshold mode, their power consumption is small. In fact, the correlator's power consumption is about 5µW. This does not impair that it is maintained permanently connected even in the normal operating mode, avoiding thus the inclusion of an extra switch. Its input impedance is determined by a coupling capacitor which can be included in the total load capacitance of the LNA. Otherwise the presence of the correlator has no influence on the LNA's performance behaviour.

IV. Conclusions

A method is presented for in-circuit structural testing the LNA of a RF front-end receiver. It consists on using a simple current correlator to obtain a signature of the cross-correlation between output voltage and power supply current. Results of detection of catastrophic and parametric faults are presented which confirm its effectiveness. This

circuit operates in the subthreshold mode and, besides assuring a simple detection scheme, requires low power consumption and implementation area. This study shall be extended to include a larger number of faults and the consideration of a larger set of functional parameters, namely noise figure and third order intermodulation point, to establish fault detection limits.

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