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STUDY AND IMPLEMENTATION OF A PVT INSENSITIVE CMOS OSCILLATOR

PEDRO VAZ COKE
DISSERTAÇÃO DE MESTRADO APRESENTADA
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Study and Implementation of a PVT Insensitive CMOS Oscillator

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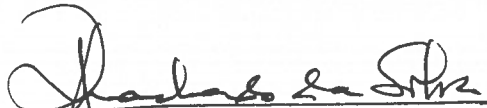
Supervisor: Miguel de Pina (SiliconGate Lda.)

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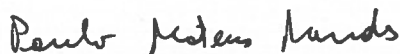
A Dissertação intitulada

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Abstract

Today virtually every consumer electronics device contains one or more integrated circuits (ICs) that require clock signal generation. This signal must present a certain level of frequency stability even in non-nominal conditions. Ideally, the clock generator block should exhibit a reasonably low frequency deviation when subject to process, voltage, and temperature (PVT) variations, such as changes in temperature caused by device heating, low power supply ripple rejection ratio (PSRR), or process parameter fluctuations during the fabrication process.

Typically, clock references are based on crystal oscillators which rely on piezoelectric materials to generate precise frequencies. However, with ever decreasing semiconductor process nodes and a growing trend in system integration, the use of external components like crystal references increases size and cost.

The use of simple oscillator topologies so that they can be fully integrated on-chip is possible, but does not provide any compensation in regards to PVT changes. As such, to realize a more reliable oscillator, a compensation scheme must be integrated so that the oscillation frequency can be stabilized.

The main objective of this work is the CMOS circuit implementation of a PVT insensitive oscillator suitable for full on-chip integration. A study on the key design considerations for realization of PVT insensitive oscillators is also presented. The covered topics include an overview on the performance of several oscillator topologies implemented in different process nodes, as well as an analysis of selected compensation circuits.

An alternative methodology for the tuning of the compensation circuits is proposed, comprising an automatic optimization algorithm. A novel process compensation circuit is also presented, focusing on the concept of orthogonal PVT compensation.

Finally, a complete implementation of a fully integrated PVT compensated oscillator in a deep-submicron process node is presented. It uses a novel open-loop temperature and process compensation circuit and comprises a current starved ring oscillator, as well as an on-chip voltage reference.

Resumo

Hoje em dia a grande maioria dos dispositivos electrónicos contêm um ou mais circuitos integrados que necessitam de geração de sinais de relógio. Este sinal de relógio deve apresentar um certo nível de estabilidade em frequência, mesmo em condições não típicas. Idealmente, o bloco gerador de relógio deverá manter um baixo desvio de frequência quando sujeito a variações de processo, tensão e temperatura (PTT), causadas por aquecimento devido ao calor gerado pelo circuito, baixo rácio de rejeição da tensão de alimentação, ou flutuações no processo de fabrico.

Tipicamente, as referências de relógio usam osciladores de cristal que fazem uso de materiais piezoeléctricos para gerar frequências precisas. No entanto, com a miniaturização do processo de fabrico de semicondutores e a tendência para a integração de sistemas, o uso de componentes externos como referências de cristal aumenta o tamanho e custo de fabrico.

O uso de topologias de oscilador simples de maneira a que estas sejam implementadas em circuitos integrados é possível, mas não permite qualquer tipo de compensação em variações de PTT. Como tal, para realizar um oscilador mais robusto, é necessária a integração de um esquema de compensação de maneira a que a frequência de oscilação possa ser estabilizada.

O objectivo do presente trabalho é a implementação de um oscilador insensível a variações PTT que seja passível de ser projectado em circuitos integrados. É também apresentado um estudo sobre os pontos chave de projecto deste tipo de osciladores. Os tópicos abordados incluem uma visão geral da performance de várias topologias de osciladores implementados em vários nós de processo, assim como uma análise de circuitos de compensação.

Uma metodologia alternativa para ajuste de circuitos de compensação é proposta, com base num algoritmo de optimização. Mais ainda, é apresentado um novo circuito para compensação de variações de processo, com foco no conceito de compensação PTT ortogonal.

Por último, é também apresentada a implementação completa de um oscilador compensado em PTT totalmente integrado num nó de processo sub-micrométrico. Este faz uso de um novo circuito de compensação em processo e temperatura e é formado por um oscilador em anel alimentado em corrente, assim como uma referência de tensão integrada.

Acknowledgments

"It's a machine"

Miguel de Pina

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List of Abbreviations

ADC Analog-to-Digtal Converter

CP Charge Pump

CTAT Complementary To Absolute Temperature

DAC Digtal-to-Analog Converter

EDA Electronic Design Automation

FLL Frequency-Locked Loop

IC Integrated Circuit

LCO LC Oscillator

LPF Low-Pass Filter

NVM Non-Volatile Memory

PDK Process Design Kit

PLL Phase-Locked Loop

PSRR Power Supply Ripple Rejection Ratio

PTAT Proportional To Absolute Temperature

PVT Process, Voltage, and Temperature

RO Ring Oscillator

SAR Successive Approximation Register

TC Temperature Coefficient

TPC Temperature and Process Compensation

VCO Voltage Controlled Oscillator

Chapter 1

Introduction

Variations in process, voltage, and temperature (PVT) have a pronounced effect in the operation of CMOS integrated circuits (ICs). These changes affect numerous MOS device parameters, but the effect is most visible when considering the I-V characteristic of the transistors. To better understand this effect, let us look at the transconductance equation of a typical NMOS transistor:

$$g_m = \mu_n C_{OX} \frac{W}{L} (v_{GS} - V_T) \tag{1.1}$$

This equation shows that for a certain transistor size ratio and gate voltage, the transconductance is defined by the threshold voltage V_T, the carrier mobility μ_n, and the oxide layer capacitance C_{OX}. These paremeters are affected by process and temperature deviations.

If a constant voltage cannot be assured as a bias reference, also v_{GS} and other voltage bias nodes will suffer fluctuations and affect the behaviour of the transistor. To eliminate the dependence on stable external voltages, a regulated on-chip power supply is needed so that variations in the IC supply will not affect transistor biasing.

1.1   Temperature effects

The effect of temperature variations on threshold voltage and carrier mobility causes both to decrease as temperature increases. This can be better expressed as [1]

$$\begin{aligned} V_T(T) &= V_T(T_0) - \alpha_{V_T} \Delta T \\ \mu_n(T) &= \mu_n(T_0) \left(\frac{T}{T_0} \right)^{-\alpha_\mu} \end{aligned} \tag{1.2}$$

where ΔT is the deviation from the reference temperature T_0, α_{V_T} is in the range of 0.5–4 mV/K, and α_μ is in the range of 1.5–2 [2]. With increasing temperature, carrier mobility is reduced due to lattice scattering, while the value of the threshold voltage also decreases [3]. This negative temperature coefficient (TC) of the threshold voltage and carrier mobility have opposite effects in transistor transconductance. The result is that the overall dependency on these effects can have a

1

non-monotonic relation with temperature [4]. In certain conditions, the output may be the same for some different temperatures. This relation has been exploited to realize temperature-stable circuits such as voltage references [5].

1.2   Process variations

The IC fabrication process also leads to variations that have a strong impact in circuit behaviour. Differences in doping levels alter carrier mobility and changes in gate dielectric thickness affect threshold voltages and oxide layer capacitance. Moreover, as semiconductor fabrication technology advances into deep-submicron CMOS process nodes, the magnitude of variability increases. At smaller scales, single dopant atoms and small fluctuations in local oxide thickness can have significant effects in device performance [6]. In fact, the intra-die threshold voltage variability increases in an almost inversely proportional manner, relative to process node size, as shown in table 1.1 [7].

Table 1.1: Intra-die variability of threshold voltage in CMOS technology nodes [7].

Process node	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm
σ_{V_T}/V_T	4.7%	5.8%	8.2%	9.3%	10.7%	16%

1.2.1   Statistical models

Modelling of these variations so that they can be taken into account during the design process relies on electronic design automation (EDA) software, and can cover inter-die or intra-die variations. The case of inter-die variation modeling estimates that all devices in the IC die will suffer the same fluctuations. For this scenario there exist two types of simulation models: statistical analysis models for Monte Carlo simulations and absolute corners. The statistical analysis models contain typical distribution functions for process parameters, provided by the foundry. These models allow running large amounts of single simulations where these parameters are selected at random from the distribution functions. They are particularly useful for fabrication yield estimation in large production circuits. A typical target in IC design is to achieve 3-sigma yields, where the device passes specifications in 99.7% of the Monte Carlo simulations (a 6-sigma target may be used for high-yield designs).

The absolute corner process models are simpler to use in terms of computation time and simulation setup, and approach the issue of process variability modeling from a worst case perspective. They are derived from the distribution functions used in the previously mentioned statistical models, where the corners (maximum and minimum) for each process parameter are taken from a 3 or 6-sigma variation. As such, a circuit design which is within specification in all process corners, could be estimated to produce > 99% yield. Typically corners are provided for MOS devices, as well as passive and other types of active devices such as diodes and bipolar transistors. For MOS devices, the model includes corners for fast and slow cases of NMOS and PMOS variations,

resulting in four corners: fastN-fastP (FF), fastN-slowP (FS), slowN-fastP (SF) and slowN-slowP (SS). The slow process corners are a consequence of reduced carrier mobility and thicker gate dielectric, which lowers the oxide layer capacitance and increases the threshold voltage, with the fast corner experiencing opposite effects. These variations result in a lower (higher for the fast corner) drain current for the same bias voltage, hence the "slow" and "fast" nomenclature. For the rest of the device types there typically exist minimum and maximum corners to model the worst case variations.

For intra-die variation modeling, random variation are taken from a set of process parameter distribution functions, for each device in the design. For this reason, they are also known as mismatch models. Such models become more useful for large IC designs, where the assumption that all devices will suffer the same process variations is no longer reasonable, due to the large die area. For small designs, however, the use of yield targets with mismatch models may lead to unreasonable overdesign. Moreover, for some circuits, critical constructs where matching is important may be easily identified, and taken into account during layout design such that the effect of device mismatch is minimized. Examples of such cases are MOS current mirrors, resistor pairs or capacitor arrays, where layout techniques such as interdigitation and common centroid can greatly increase matching and reduce the effect of intra-die process variations. In sum, although mismatch models are needed for large area or high-yield designs, for small designs where good layout techniques for device matching are employed, their use might be unnecessary or even detrimental to the design process.

1.3   Design for variability

In deep-submicron nodes, variability not only increases in magnitude, as mentioned earlier, but is also highly process-dependent. This further increases the need for foundry process variation models to validate IC designs. It also increases the complexity of designing and realizing PVT-insensitive circuits, which falls in the scope of this work.
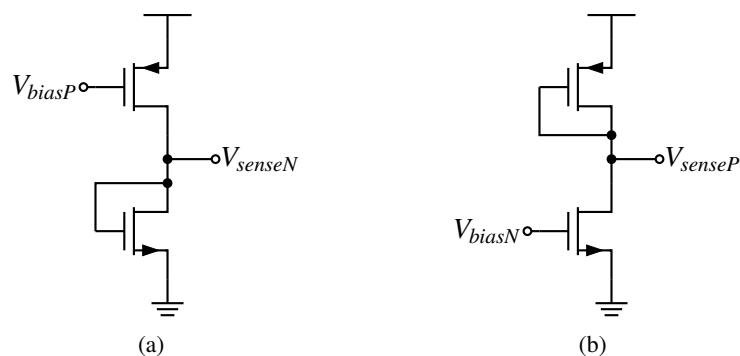
Figure 1.1: Circuit for process sensing in (a) NMOS and (b) PMOS versions.

As a basic example of process variability, let us consider a classic example of a threshold voltage sensor used for process compensation [8]. The circuit is shown in Fig. 1.1, in both PMOS and

NMOS versions. It comprises a diode connected MOS device, which acts as the process sensor, and a complementary transistor acting as a current source, with a fixed bias voltage applied at the gate. The output voltage is at the drain of the process sensor device, and varies according to process deviations. To illustrate the sensitivity to device sizing and process corner interaction between devices, the circuit was implemented in a 90 nm process and simulated for different process sensor gate lengths, while the current source MOS device was kept at constant size.
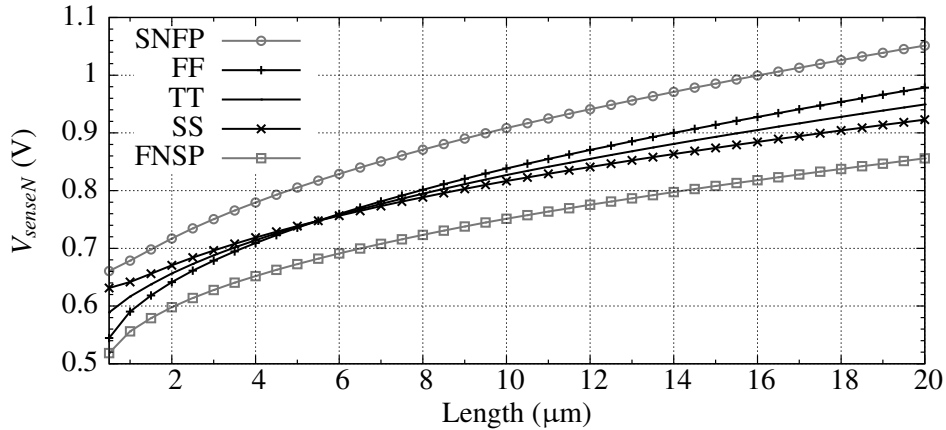
(a)
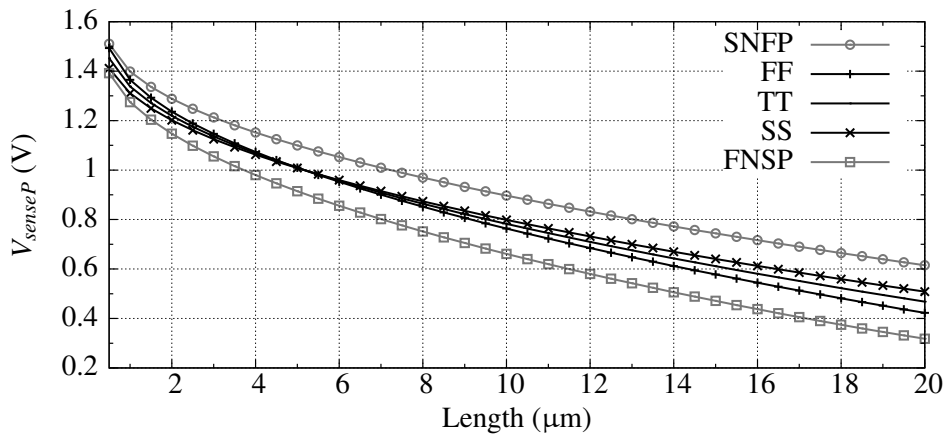
(b)

Figure 1.2: Output of the (a) NMOS and (b) PMOS process sensor over sensor transistor length and process corners.

The simulation results are shown in Fig. 1.2. The net result from process variations is the circuit becoming more sensitive to mismatched PMOS and NMOS process variations (FS and SF corners). Also note that depending on the process sensor size, the FF and SS corners change order. Not shown is the variation in the TC, which changes from negative to positive as the NMOS process sensor length increases, while the PMOS version exhibits the opposite behaviour.

The purpose of this example is to show how device sizing and interaction in a circuit may result in unexpected behaviour over process and temperature variations. As circuit complexity increases,

it can become difficult to predict the result over corners. The use of analytical expressions for such a task is non-trivial due to the complexity of the process parameters that must be taken into account, and falls outside the scope of this work.

1.4   Problem statement

Today virtually every consumer device contains one or more ICs comprising some type of circuitry that requires a clock signal. As such, clock generation is a required component on almost any electronic system.

For many electronic circuits, the clock signal must also present a certain level of stability even in non-nominal conditions. Ideally, the clock generator block should exhibit a reasonably low frequency deviation when subject to PVT variations. Changes in temperature and voltage occur over time, and can be caused by internal factors such as heat generated by the device or low power supply ripple rejection ratio (PSRR), or external such to environmental changes or electrical noise. In contrast, changes in process are by nature static and permanent for each device, as they occur due to parameter deviations during the fabrication process.

Typically, clock references are based on crystal oscillators. They rely on piezoelectric materials to generate precise frequencies, and provide good stability over temperature. However, with ever decreasing semiconductor process nodes and a growing trend in system integration, the use of external components like crystal references increases size and cost.

The use of simple oscillator topologies, so that they can be fully integrated on-chip, is possible, but does not provide any compensation in regards to PVT changes. As such, to realize a more reliable oscillator, a compensation scheme must be integrated so that the oscillation frequency can be stabilized.

1.5   Proposed approach

This works aims to cover the key design considerations for the realization of PVT insensitive oscillators, as well as to propose new methodologies and circuit implementations. Due to the unpredictable nature of process variations, analytical analysis is of limited use, and instead a practical approach is taken. The focus is on providing straightforward design flows and simple circuit realization methodologies through the use of orthogonal compensation mechanisms for process, voltage, and temperature variations.

In regards to the use of EDA software, the *Cadence Virtuoso* design suite was used for circuit schematic capture, *Synopsys HSPICE* and *WaveView* for circuit simulation and results visualization, and *Mathworks MATLAB* for additional numeric processing of results and implementation of optimization algorithms.

1.6   Document structure

The document structure consists of a literature review, and analysis on the performance of oscillators, analysis of compensation circuits, description of the proposed implementation and finally conclusions and future work.

In chapter 2, a brief review of the existing literature on PVT insensitive oscillators is presented, providing an overview of the state of the art.

Chapter 3 covers a selected set of oscillator topologies to provide a brief circuit study and general comparison on key performance metrics.

On chapter 4, the focus shifts to compensation circuits, where new approaches to design flow are proposed and tested.

The implementation of this new compensation circuit is described in chapter 5, and the obtained results are presented.

Lastly, chapter 6 provides the insights and conclusions that arise from the development of this work, as well as stating future work on the topic.

Chapter 2

Literature Review

In this chapter a brief review of current literature on design techniques for PVT insensitive oscillators is presented. Most PVT insensitive oscillator designs are comprised of two main blocks, an oscillator block and a compensation circuit. The oscillator is responsible for synthesizing the output signal, however it is sensitive to PVT variations and must be able to be tuned in order to compensate for frequency deviations. As such, this block is usually a voltage controlled oscillator (VCO), and in most systems it is based on a ring oscillator (RO) architecture, since it is relatively simple to realize without large area and power requirements. However, implementations using other oscillator topologies, such as LC or relaxation, also exist.

The compensation block must sense in some way any deviations from the nominal frequency, and tune the VCO in order to correct them. In sections 2.1 and 2.2 the two most relevant compensation methods are described, analog open-loop and closed loop. The former relies on an analog compensation block that corrects for temperature and process variations. This process is essentially a form of pre-distortion. Whereas in an ideal circuit the VCO voltage would be kept to generate a constant frequency, analog open-loop compensation generates a process and temperature dependent control voltage that opposes the VCO variation. This control voltage is specific to the VCO used, and must also be tuned for the PVT behaviour of the process node used in the design.

Conversely, closed-loop compensation schemes employ a more generic approach, which can be applied to any generic VCO block. The control voltage correction is performed by sensing the output frequency, comparing it with a reference, and minimizing the error. This compensation block can be implemented in different ways, from a full analog comparator-based scheme, to a digital successive approximation register (SAR)-based approach.

The last section covers other selected PVT compensation techniques, which are included to provide a complete overview of the state of the art.

Throughout the analysis of relevant literature, it is evident that the challenge in designing PVT insensitive oscillators lies mostly in process and temperature compensation. The realization of PVT insensitive voltage references is a well-understood topic and many works in this area exist, e.g. bandgap references [9, 10], used in some of the compensation methods found in literature.

2.1   Analog open-loop compensation
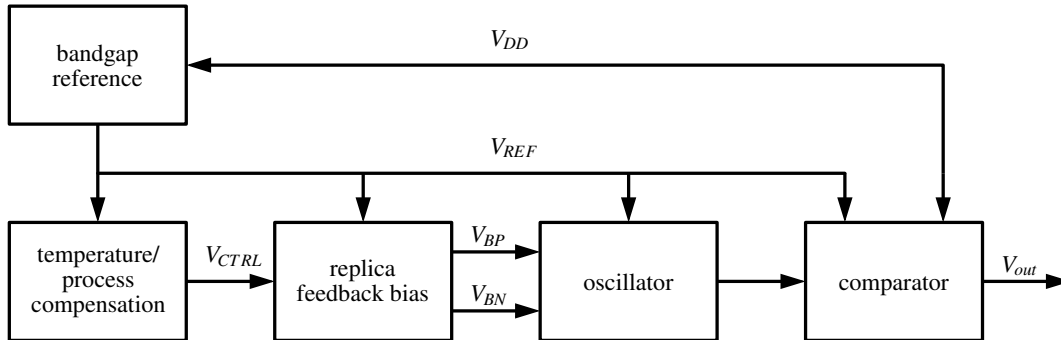
Figure 2.1: Block diagram of typical open-loop compensation topology.

Design of PVT insensitive oscillators employing analog open-loop compensation methods rely on process and temperature-sensitive bias circuits to control the oscillator frequency. These compensation schemes follow a similar topology as shown in Fig. 2.1, which comprises the following blocks:

- Bandgap reference which provides a reference voltage V_{REF}, independent of temperature, process, and supply variations. This is used as a supply voltage for all the circuits up until, and including, the oscillator block, to reduce system variations due to voltage sensitivity.

- A temperature and process compensation (TPC) circuit that senses changes in these quantities and generates a proportional output voltage V_{CTRL}, similar to pre-distortion methods. This voltage is used to control the oscillator and thus the TPC block is ultimately responsible for making the system insensitive to temperature and process variations.

- The replica biasing circuit generates the oscillator bias voltages V_{BN} and V_{BP} from V_{CTRL}. This block uses self-biasing techniques to generate stable voltages.

- The oscillator block synthesizes the reference frequency, which will depend on the bias voltage applied by the replica feedback circuit. A buffer is used at the block output to saturate the signal to V_{REF}. In relevant literature a RO is commonly used.

- A comparator is used to buffer the output signal and saturate it to V_{DD}.

Due to the open-loop nature of the system, the TPC should be tuned so that the control voltage closely matches the oscillator deviations due to process and temperature changes. Assuming we define a reasonable working temperature and voltage range, there should exist a bias voltage that keeps the oscillator at the target nominal frequency across the PVT corners. Once the variation of this optimal bias voltage across the desired corners is obtained, the TPC circuit should be tuned to match it. Depending on the TPC block design, several circuit parameters may be used for tuning the control voltage. These tuning points result in varying degrees of freedom when adjusting the

temperature and process slopes to achieve ideal compensation throughout all corners. This tuning procedure is done via circuit simulation, using process variation corner models.

(a)

(b)
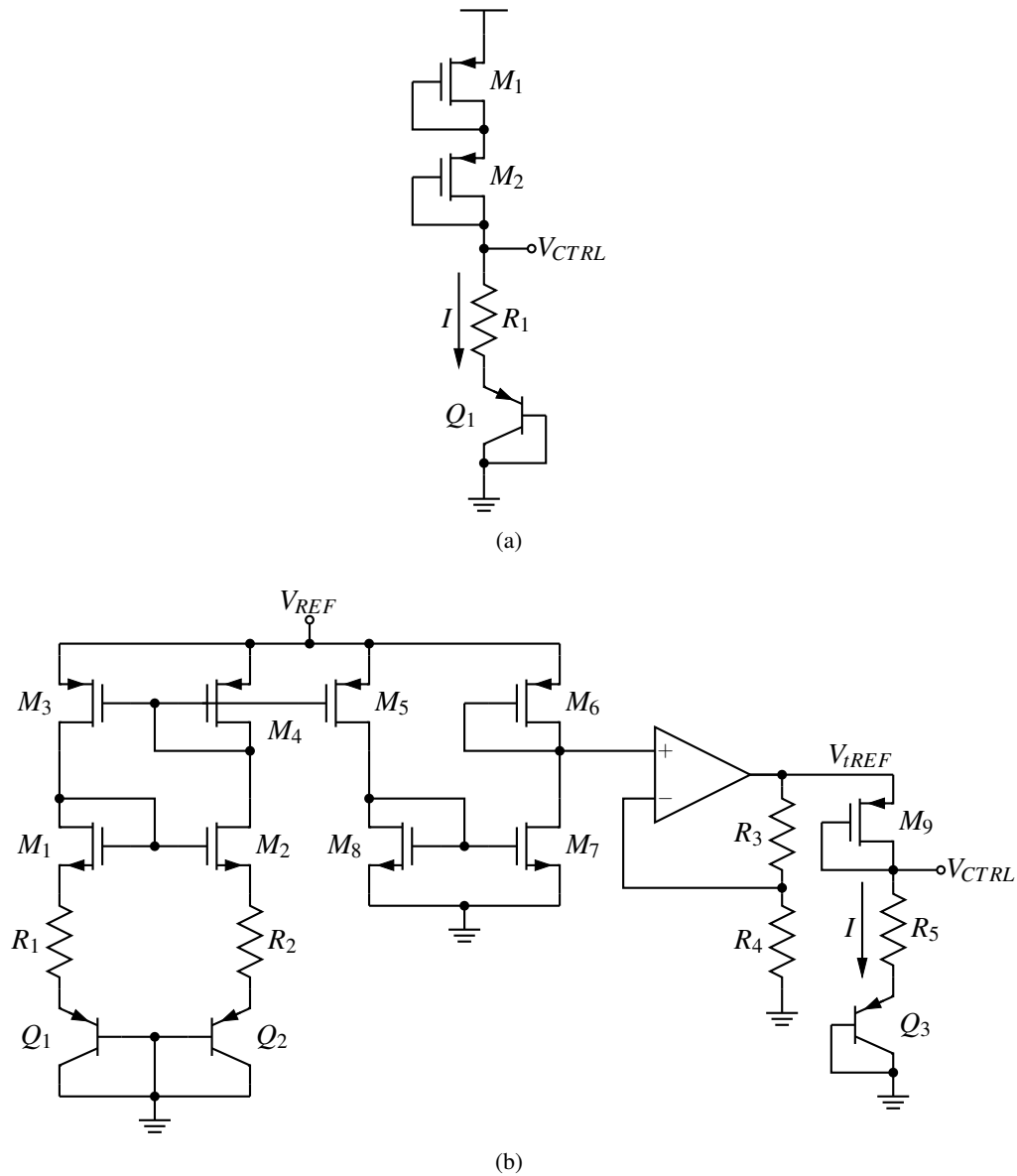
Figure 2.2: Circuits for TPC proposed by (a) Shyu *et al.* [8] and (b) Sundaresan *et al.* [11].

The TPC circuits typically comprise two sections, where different elements are responsible for sensing temperature and process variations. One of the first such circuits is proposed in [8] and is shown in Fig. 2.2(a). The diode-connected MOS transistor M_2 is used as a threshold voltage V_T sensitive element. Temperature sensing is done via the v_{EB} of the diode-connected PNP transistor Q_1 that exhibits a negative temperature coefficient. The resistor R_1 and Q_1 can be seen as a

temperature-dependent current source, and the output voltage V_{CTRL} is given by

$$V_{CTRL} = V_{DD} - 2|V_T| - \sqrt{\frac{I}{K(W/L)_2}} \tag{2.1}$$

This compensation circuit is used in [8] with RO-based VCO and implemented in a 0.6 μm process, achieving a 680 kHz output frequency with 4.7% measured accuracy.

The circuit in Fig. 2.2(b), proposed by Sundaresan *et al.*, uses a similar V_t sensor, relying on a more robust reference current source. This first stage generates a process-dependent buffered signal V_{tREF}, which is also temperature independent, limited by the matching of the resistors. The second stage, closely resembles the previous TPC circuit, and as such senses both temperature and process changes. Similarly to (2.1), the output V_{CTRL} is given by [11]

$$V_{CTRL} = V_{tREF} - |V_{T9}| - \sqrt{\frac{I}{K(W/L)_9}} \tag{2.2}$$

It depends on both the process-dependent voltage V_{tREF}, but also on the threshold voltage of M_9. This is done since the size of M_9, along with the value of R_5, can used as an additional degree of freedom for tuning the process and temperature slopes of the TPC circuit.

An enhanced version of this circuit is also proposed by Sundaresan *et al.*, which includes additional elements to provide more tuning points. This version is implemented in [11] in a 0.25 μm process, and is able to achieve 1.29% and 0.84% measured process and temperature variations, respectively, with a 7 MHz nominal output frequency.

Other works opt to reduce the overall complexity of the TPC circuit, using a bandgap voltage reference as a proportional to absolute temperature (PTAT) current source [12]. In [13], a leakage current sensor [14] is used as a process sensor, but on the other hand, a 2-bit DAC is required to generate the control voltage.
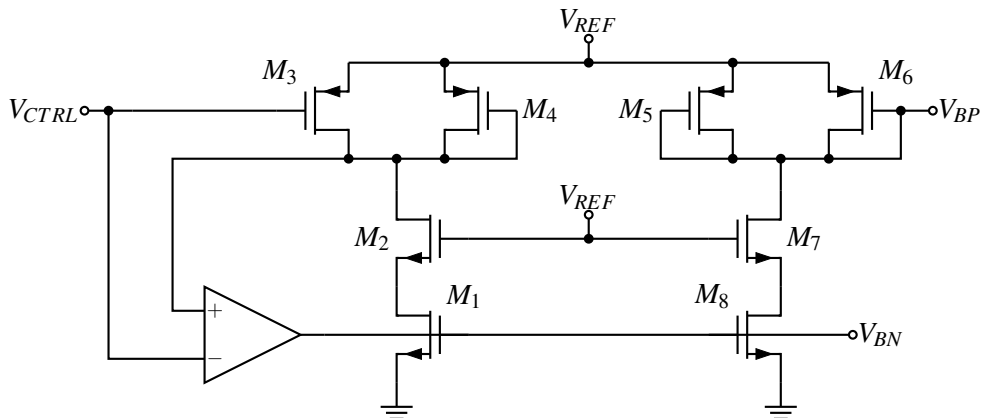
Figure 2.3: Replica biasing circuit proposed in [15].

The control voltage generated by the TPC block is fed to a replica biasing circuit [15] that drives the RO, as shown in Fig. 2.3. The bias generator produces the bias voltage V_{BN} from V_{CTRL},

using a half-buffer replica. An additional half-buffer replica is used to generate V_{BP}, which tracks V_{CTRL}, but is isolated to prevent potential capacitive coupling.

The premise of this method is that the control voltages generated by the TPC block will compensate the oscillator deviations due to process and temperature variations. One must ensure the TPC block is accurately tuned, since any error directly compromises the frequency accuracy of the system across PVT corners. Due to the fact that the control voltage must be tuned to match the oscillator behaviour, the design and implementation of this topology must target a specific oscillator type and fabrication process. This compromises the portability of this compensation method, since changes in the oscillator or migration to a different process will require re-tuning the TPC block, which in the worst case can imply a re-design effort. Moreover, since it is infeasible to measure the oscillator block behaviour from fabricated CMOS samples due to cost and time restrictions, one must typically rely on simulation results to tune the TPC circuit. As such, one must ensure that the foundry-provided process design kit (PDK) contains device models that allow process corner and statistical analysis with acceptable accuracy.

Table 2.1: Comparison of analog open-loop implementations.

Ref	Process	Frequency	Area	Power (mW)	Accuracy (%)
[8]	$0.6\,\mu m$	$680\,kHz$	$0.075\,mm^2$	0.4	4.7
[11]	$0.25\,\mu m$	$7\,MHz$	$1.6\,mm^2$	1.5	2.64
[12]	$0.18\,\mu m$	$150\,MHz$	Simulation	0.537	2.29
[13]	$0.18\,\mu m$	$2\,MHz$	$0.045\,\mu m^2$	0.048	2.81
[16]	$0.18\,\mu m$	$20\,MHz$	N/A	N/A	2.98

This open-loop topology has been used to realize oscillators in the range of $640\,kHz$ to $150\,MHz$ [8, 11–13, 16], with a frequency sensitivity that is typically around 3%. A brief comparison of relevant works in literature is shown in table 2.1.

2.2 Closed-loop approach

Closed-loop topologies aim to minimize the error between the output clock and a stable, on-chip reference, through a feedback loop. In this approach, the compensation blocks in the feedback path are designed to be insensitive to PVT variations in order to reliably measure and minimize the error of the blocks that are not.

Unlike open-loop methods where the control voltage is generated to compensate a well-known oscillator behaviour over process and temperature corners, in closed-loop methods the compensation circuit senses the output frequency and acts on the VCO accordingly in order to correct for deviations.

2.2.1 Comparator loop

Comparator-based loops have a similar working principle as typical phase-locked loop (PLL) architectures (Fig. 2.4), where the phase-frequency detector is replaced by a frequency sensor that

outputs a DC signal which is compared to a stable voltage reference.

The frequency sensor in Fig. 2.5 uses a capacitance to integrate a reference current, which is then discharged to a second capacitor to obtain a DC voltage V_{FS} proportional to the oscillator frequency. In order to minimize the switching frequency, a timing block uses the output clock signal to generate the (4 times slower) control signals that drive the frequency sensor switches.
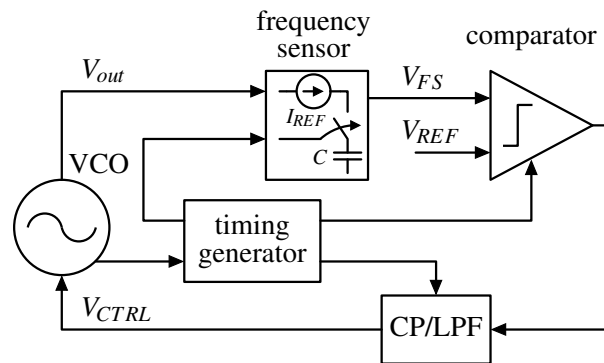
Figure 2.4: System diagram of the comparator-based compensation loop.

The output of the frequency sensor V_{FS} is then compared to a reference voltage in order to determine if the oscillator is operating at the desired frequency. The voltage V_{FS} is fed into a pair of comparators that decide if it is above or below a reference V_{REF}, which defines the nominal oscillator frequency. The comparator can be realized with simple differential amplifier, with emphasis on reducing its offset voltage.

A charge pump (CP) and low-pass filter (LPF), controlled by the comparator outputs adjusts the oscillator control voltage to eventually compensate for process and temperature variations. When V_{FS} approaches V_{REF}, the comparator falls into the transition region. As such, the charge pump "up" and "down" currents, I_{UP} and I_{DN}, should match also when the comparator output is at $V_{DD}/2$.
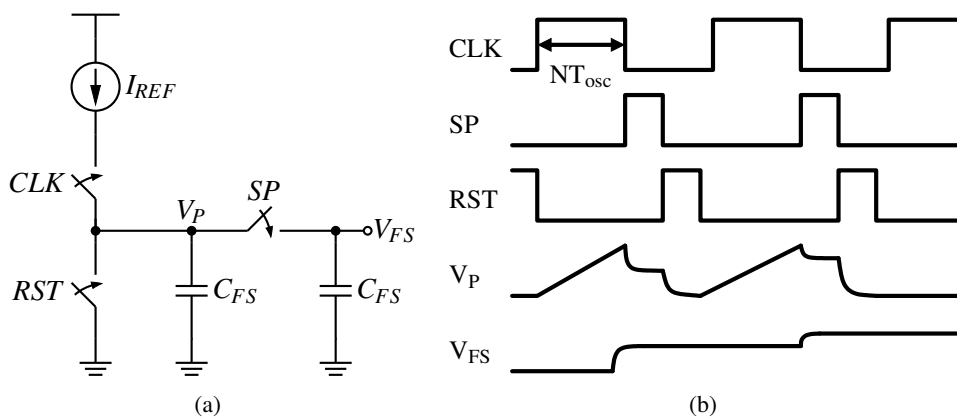
Figure 2.5: (a) Frequency sensor as proposed in [17], and (b) control signals.

The relative frequency accuracy of the compensation loop is defined by [17]

$$
\left(\frac{\sigma_f}{f_{osc}^0} \right)^2 = \left(\frac{\sigma_T}{T_{osc}^0} \right)^2
$$

$$
\approx \left(\frac{\sigma_I}{I_{REF}^0} \right)^2 + \left(\frac{\sigma_C}{C_{FS}^0} \right)^2 + \frac{\sigma_{REF}^2 + \sigma_{CP,off}^2 + \frac{\sigma_{UP-DN}^2}{A_{CP}^2 G_{CP}^2}}{(V_{REF}^0)^2}
\tag{2.3}
$$

The accuracy of the oscillator is mainly dependent on a stable current reference I_{REF}, deviations in the C_{FS} capacitor, and comparator offset, which comprise the main challenges when realizing this type of topology. The current sink I_{UP} and I_{DN} should match as closely as possible, and a current reference with good absolute accuracy is needed for I_{REF}. Furthermore, large capacitors can be used to minimize deviations, as well as choosing a high V_{REF} value to reduce the effects of mismatches in the comparator and charge pump.
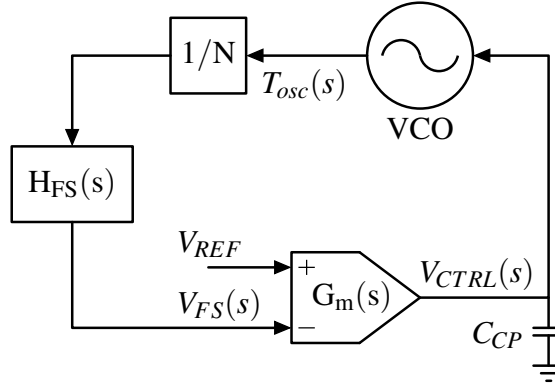
Figure 2.6: Linear continuous-time model of the comparator-based compensation loop.

The comparator-based compensation loop behaviour experiences two dynamic regimes. If the operating frequency is far from the reference value, the loop exhibits bang-bang dynamics due to the binary output of the comparator. As the frequency approaches the reference value, the relative error is small enough that the comparator operates in its linear region, such that a linear model can be applied. The linear continuous-time model is depicted in Fig. 2.6, and its closed-loop transfer function is given by [17]

$$
T_{osc}(s) = \frac{V_{REF} C_{FS}}{N I_{REF}} \frac{1 + \frac{s}{p_{FS}}}{1 + \frac{s}{K_{Pout}} \left(1 + \frac{s}{p_{CP}} \right) \left(1 + \frac{s}{p_{FS}} \right)}
\tag{2.4}
$$

Due to the third-order nature of the loop, care should be taken regarding the loop gain K. If too small ($\ll 0.2$), the convergence time increases considerably and if too large ($\gg 5$), it can become unstable.

This topology has been explored in [18], and realized in [17] in a 90 nm CMOS process with an oscillating frequency of 2.1 GHz and a frequency accuracy of 4.6%.

2.2.2 Switched capacitor loop
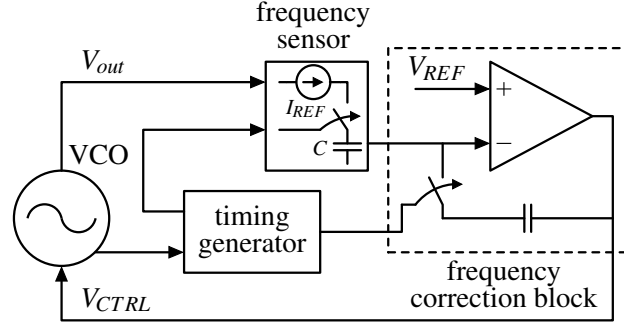
Figure 2.7: System diagram of the capacitor-based compensation loop proposed.

Expanding on the previous architecture, Zhang *et al.* propose a similar concept, using switched capacitors [17], depicted in Fig. 2.7. This topology aims to address a potential shortcoming of the previous comparator-based architecture that arises from the third-order behaviour of the loop and its potential for instability. The system is otherwise identical to the comparator-based loop, except for the frequency correction block.

The frequency correction block (Fig. 2.8) is based on a discrete time, switched capacitor integrator, consisting of a current source I_{REF}, capacitors C_1 and C_2, a high-gain operational amplifier, transmission gate switches, and external signals V_{REF} and RST.

The external RST signal is asserted at the beginning of operation to initialize the timing signal generator and establish a DC operating point for the output of the amplifier. Once the signal is de-asserted, the VCO oscillates with its free running frequency. The VCO output is divided and shaped into a 50% duty cycle square wave from which the timing generator produces the signals φ_{AB}, φ_A, φ_B and φ_C. The operation of the frequency correction block is divided into three phases: initialization phase, comparison phase, and correction phase.

During the initialization phase, φ_{AB} and φ_A are asserted and the capacitor C_1 is charged to V_{REF}. This state is used to set the initial condition on C_1 so that a comparison can be made between V_{REF} and frequency-proportional voltage. On the comparison phase, φ_{AB} and φ_B are asserted and one plate of the capacitor C_1 is charged by I_{REF} for a period of NT_{osc}. This phase establishes a charge difference at C_1 that is proportional to the difference between the reference frequency and the actual VCO oscillation frequency. The φ_{AB} signal is then de-asserted, leaving C_1 floating and holding its charge. At the correction phase, φ_C is asserted and the charge from C_1 is transferred to C_2 by the operational amplifier.

The relative frequency accuracy of the compensation loop can be approximated to [17]

$$\left(\frac{\sigma_f}{f_{osc}^0}\right)^2 = \left(\frac{\sigma_T}{T_{osc}^0}\right)^2$$
$$\approx \frac{\sigma_I^2 + \frac{C_1^2}{A^2 K_{VCO}'^2}\left(\frac{\sigma_{K'}^2}{K_{VCO}'} + \frac{\sigma_C}{C_1^0}\right)}{(I_{REF}^0)^2} + \left(\frac{\sigma_C}{C_1^0}\right)^2 + \frac{\sigma_V^2 + \sigma_{off}^2}{(V_{REF}^0)^2} \qquad (2.5)$$
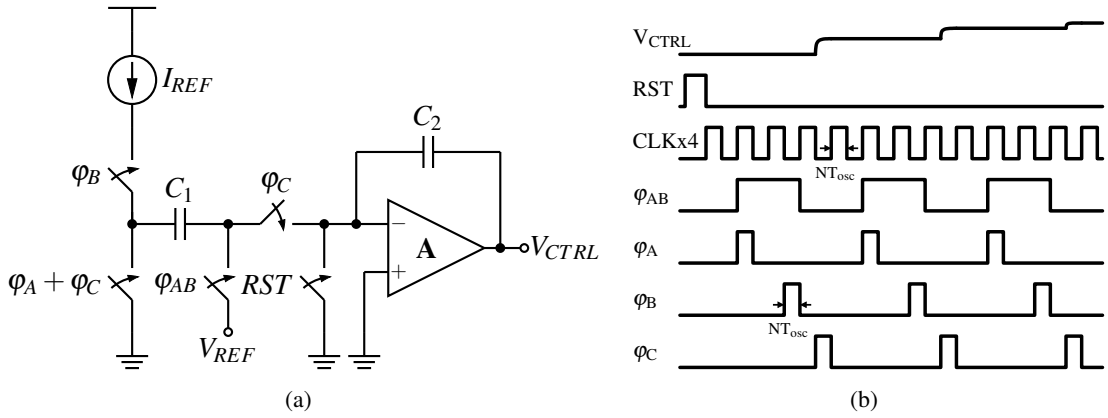
Figure 2.8: (a) Switched capacitor implementation of the frequency correction block and (b) control signals.

from which we observe that accuracy depends mostly on V_{REF}, I_{REF} and capacitor deviations, as with the comparator-based loop. The loop dynamics however, are quite different, and the output voltage of the operation amplifier after n cycles, can be expressed as [17]

$$
\begin{aligned}
V_{CTRL}(n+1) = & V_{CTRL}(n)\frac{C_2(A+1)}{C_1+C_2(A+1)} + V_{offset}\frac{AC_1}{C_1+C_2(A+1)} \\
& + \frac{A(I_{REF}NT_{osc}(n)-V_{REF}C_1)}{C_1+C_2(A+1)}
\end{aligned}
\tag{2.6}
$$

The compensation loop is stable and will converge even with a finite gain, due to a first-order negative feedback exhibited by the third term, regardless of the starting condition. The static offset can cause some ripple on V_{CTRL}, which can be minimized by increasing the ratio of C_1 to C_2 and ensuring the input transistors of the amplifier are large and well matched. Care should also be taken when choosing the size of C_2. A too large value will make the voltage increment on V_{CTRL} smaller, increasing compensation time. If the value is too small, V_{CTRL} becomes less precise, leading to undershoots or overshoots.

This design is implemented in [17] using a 90 nm CMOS process with an oscillating frequency of 2.9 GHz and a frequency accuracy of 6.2%.

2.2.3 SAR loop

This topology aims to increase efficiency, compared to the previous closed-loop approaches, by employing digital blocks to control the VCO [19, 20].

The output of the comparator, the error between the reference and the current frequency, is fed into a SAR, as shown in Fig. 2.9. In this configuration, the comparator effectively operates as a 1-bit analog-to-digtal converter (ADC). The SAR stores these values to increment or decrement a digital code that will approximate the correct control voltage of the VCO. This digital code is
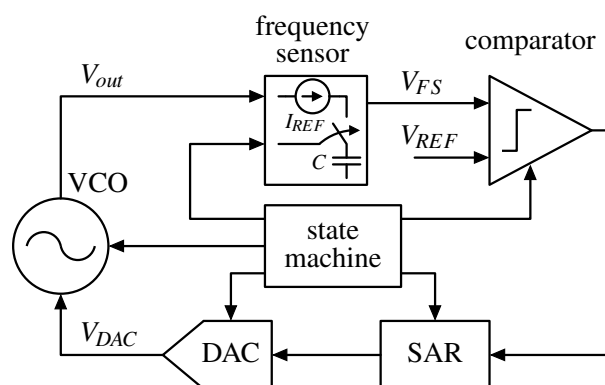
Figure 2.9: System diagram of the SAR compensation loop.

converted to analog through a digtal-to-analog converter (DAC), which feeds back into the VCO to correct for frequency deviations.

The accuracy of the system is limited by the finite resolution of the comparator and number of bits available at the SAR and DAC, the variation of I_{REF}, and the capacitor in the frequency sensor block. Let the worst-case comparator resolution be V_{RSN} and the LSB voltage of the DAC be V_{LSB}, the frequency accuracy will be [20]

$$max\left\{\frac{V_{RSN}}{V_{REF}}, V_{LSB}K'_{VCO}\right\} + \sigma_I + \sigma_C \tag{2.7}$$

where V_{RSN}/V_{REF} is the result of the finite comparator resolution and V_{LSB}/K'_{VCO} is the result of finite bit resolution.

Due to the increase in the complexity of the digital control signals which comes with the inclusion of a DAC and SAR, the system requires a more advanced control block. A state machine, which runs on a derived clock from the VCO output, is used to control the timing of system events. At initialization the state machine is in a sleep/reset state, moving onto auto zero and conversion, when a request is initiated, and then iterating between update, sample, and compare modes until the final approximation is completed. As output frequency can vary during the control process, provisions are made for synchronization using hand-shake signals at crucial stages, such as update, sample and comparison, for robustness.

The state machine also performs clock gating to different blocks to save power. This is one of the main advantages of this topology. Since the compensation routine can be run periodically (depending on how quickly voltage and temperature conditions are expected to change), unneeded blocks can be disabled when idle and the VCO control voltage latched. This is further demonstrated with the realization of this system on a 65 nm process with an operating frequency of 0.8–2 GHz and power consumption between 46 µW and 226 µW [20], achieving a 2.1% frequency accuracy.
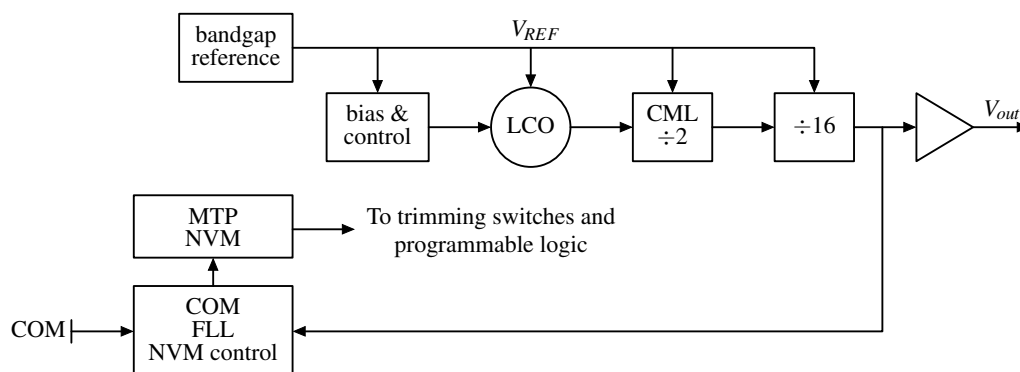
Figure 2.10: System diagram of the FLL compensation loop.

2.2.4 Frequency-locked loop

In [21], a LC oscillator (LCO) is compensated for PVT variations, making use of an external reference at post-fabrication to increase accuracy – Fig. 2.10. Tolerance to voltage variations is ensured by employing a bandgap as a voltage supply. This is similar to previous designs, and this supply is used for all blocks except the output buffer, which should saturate the signal to V_{DD}.

To compensate over temperature changes, a PTAT circuit is used to adjust a series of variable capacitors and digitally controlled bias levels. This is similar to the process used in open-loop topologies.

However, to compensate for process variation, a closed-loop system is used. It requires an initial post-fabrication calibration where an in-chip frequency-locked loop (FLL) adjusts the LCO frequency to that of an external precision reference. This trimming procedure is done via a digitally controlled capacitor array. Once the FLL converges, the trimming values are stored in a non-volatile memory (NVM). As such, this procedure needs to be executed only once.

The realized circuit in [21] is able to achieve 152 ppm (0.0152%) frequency accuracy. This result comes close to that of typical quartz oscillators (±50 ppm), and is already sufficient to satisfy the requirements of high-speed protocols such as HS-USB, S-ATA, or Gigabit Ethernet. However, this comes at the cost of a potentially expensive post-fabrication calibration step, and a high power consumption of 59.4 mW.

Table 2.2: Comparison of closed-loop implementations.

Ref	Process	Loop type	Frequency	Area	Power (mW)	Accuracy (%)
[20]	65 nm	SAR	0.8–2 GHz	0.06 mm^2	0.046	2.1
[21]	0.25 µm	FLL	25 MHz	N/A	59.4	0.0152
[22]	90 nm	Comparator	2.1 GHz	0.096 mm^2	1.95	4.6
[22]	90 nm	Switched capacitor	2.9 GHz	0.084 mm^2	3.3	6.2

The analysed closed-loop implementations and relevant figures of merit are shown in table 2.2. Compared to open-loop topologies, they are able to achieve higher frequencies, while maintain-

ing comparable area and power consumption, although most of the works are realized in smaller processes.

2.3   Other techniques

2.3.1   Structural approaches
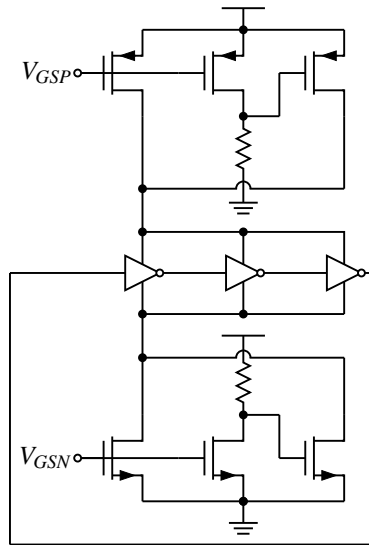
Figure 2.11: Schematic of the addition-based RO.

In [22, 23], a different approach is taken. Instead of more complex compensation systems, an effort is made to modify the basic RO design in order to make it more tolerant to process variations. The focus is specifically on the current starved RO, which relies on symmetric current sources for biasing.

The proposed modified RO uses instead an addition-based current source [24, 25], which exhibits a low sensitivity to process changes – Fig. 2.12. The current source has an output current I, that is the sum of the currents I_1 and I_2, flowing through the transistors M_1 and M_2, respectively. The transistor M_3 will mirror M_1, and the resistance R ensures that the gate voltage of M_2 changes proportionally to the current I_1. As process deviations affect the threshold voltage of transistors M_1 and M_3, the drain voltages and I_1 will also change, in an inversely proportional manner. In other words, when I_1 increases due to process variations, the gate voltage of M_2, and thus I_2, will decrease in a proportional manner. Therefore, the underlying principle of the addition-based current source, is that although I_1 and I_2 may vary due to process variations, they are self-compensating and their sum I, will exhibit a much lower variation.

The addition-based current source was used in a common current starved RO, realized in a 90nm process [22], resulting in a 5.8% frequency accuracy. When compared to the common RO using typical current sources, there is a 65.1% decrease in process variation, while increasing the power consumption by only $33\,\mu W$ and the area by $3\,\mu m^2$.
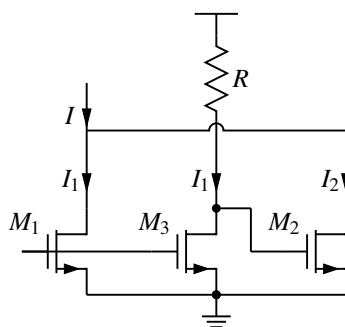
Figure 2.12: Schematic of the addition-based current-source.

2.3.2   Reference modeling

Some of the previous compensation techniques are limited by factors such as the reliance on specific properties of a process or the inability to scale down some of the analog constructs like bandgap references. In an attempt to overcome these limitations, an all-digital oscillator is proposed in [26, 27]. The compensation method uses a model that maps the delay ratio between two cells to the delay of an inverter, across several PVT corners. The digital mapper, however, requires a set of coefficients that must be obtained by chip testing procedures, thus involving a post-fabrication step.

Since this topology relies almost entirely on digital gates, the design is highly portable and occupies a small area (0.04mm^2), while achieving 2.3% frequency accuracy [27].

2.4   Overview

From the relevant compensation methods covered in this chapter, open-loop topologies generally achieve better frequency accuracy. Most published works are realized in larger process nodes, and target lower output frequencies.

On the other hand, closed-loop implementations are able to attain higher frequencies, and generally do not require such extensive tuning during implementation as analog open-loop systems.

The trade off between a fully autonomous system and precision also becomes quite visible, with some implementations achieving high accuracy with the use of external calibration procedures. However, this can be a costly and time-consuming step in the IC manufacturing process.

In sum, we conclude that state of the art implementations are able to cover a reasonable range of demands, from high-frequency/low accuracy to low-frequency/high precision, or low-power/low-area realizations. The relevant figures of merit of the examined works are summarized in table 2.3.

Table 2.3: Comparison of PVT compensated oscillators.

Ref	Process	PVT compensation	Frequency	Area	Power (mW)	Accuracy (%)
[8]	0.6 μm	Open loop	680 kHz	0.075 mm^2	0.4	4.7
[11]	0.25 μm	Open loop	7 MHz	1.6 mm^2	1.5	2.64
[12]	0.18 μm	Open loop	150 MHz	Simulation	0.537	2.29
[13]	0.18 μm	Open loop	2 MHz	0.045 μm^2	0.048	2.81
[16]	0.18 μm	Open loop	20 MHz	N/A	N/A	2.98
[17]	90 nm	Comparator loop	2.1 GHz	0.096 mm^2	1.95	4.6
[17]	90 nm	Switched-cap. loop	2.9 GHz	0.084 mm^2	3.3	6.2
[20]	65 nm	SAR loop	0.8–2 GHz	0.06 mm^2	0.046	2.1
[21]	0.25 μm	FLL	25 MHz	N/A	59.4	0.0152
[22]	90 nm	None	1.8 GHz	0.013 mm^2	0.087	5.8
[27]	90 nm	Reference modeling	5 MHz	0.004 mm^2	0.65	2.3

Chapter 3

Analysis on Oscillator Performance

This chapter presents a brief analysis of selected oscillator topologies. The purpose is to provide a general performance overview of oscillator architectures most suited for PVT compensation.

The selection criteria weighed not only on the suitability for integration with compensation circuits, but as well on portability between processes, area, and power consumption. Most systems shown in the previous chapter rely on differential delay cell or current starved ROs. Additionally, the high-performance VCO and relaxation oscillator were also selected for analysis.

Each topology was implemented in six different CMOS processes from two foundries, hereafter referred as foundry A and B, ranging from 110 nm to 28 nm. This allows an general assessment on portability of each oscillator architecture, as well as providing a sense of typical behaviour changes when moving to smaller nodes. When possible, each implementation uses thick gate devices with similar sizes, supply voltages (3.3 V for 110 nm to 40 nm and 1.8 V for 28 nm), as well as MOS-based passive devices when available. This is done in order to ease portability, simplify the design flow and avoid excessive process-specific tuning. Therefore, the following is not a comprehensive study on oscillator design and optimization, but rather takes a more practical and straightforward approach to implementation. Such extensive circuit analysis of each specific oscillator topology would fall outside the scope of this work. The next sections present the concepts behind the current starved and differential delay cell ROs, high-performance VCO, and relaxation oscillator, as well as general performance figures.

Each architecture was tuned for 25 MHz oscillation frequency. Additionally, where possible, the implementation was optimized for a balanced performance-power trade off.

3.1   Current starved ring oscillator

The current starved RO is a variation of the classic ring oscillator, where each inverter is current-limited. The circuit for this architecture is shown in Fig. 3.1. The current limiting is implemented through simple PMOS and NMOS current mirrors, realized by the M_3–M_4, M_5–M_6, and M_7–M_8 pairs. A bias voltage V_{CTRL} is applied to the PMOS devices, which will set the I_{bias}
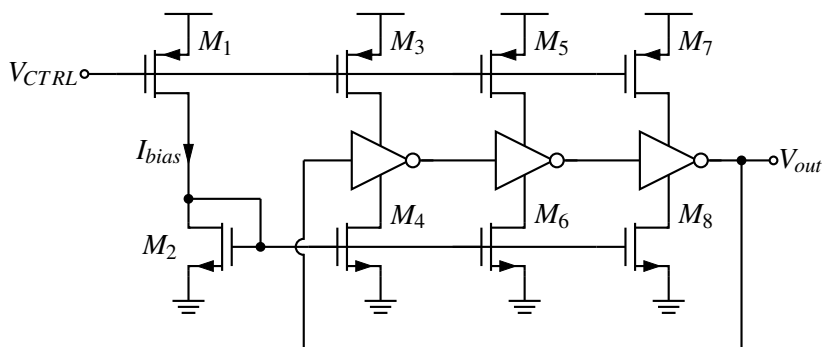
Figure 3.1: Schematic of the current starved RO.

current for each stage, i.e. $I_{bias}(V_{CTRL})$. The NMOS bias voltage is generated by the self-biased M_2 transistor. The oscillation period depends directly on the current, and is given by

$$T_{osc} = \frac{N\,C_{eff}\,V_{DD}}{I_{bias}(V_{CTRL})} \tag{3.1}$$

where N is the number of stages in the chain and C_{eff} is the effective load capacitance of each stage, comprised by the intrinsic capacitances $C_{jd_{P,N}}$, $C_{gd_{P,N}}$, and the input capacitance of the following stage.
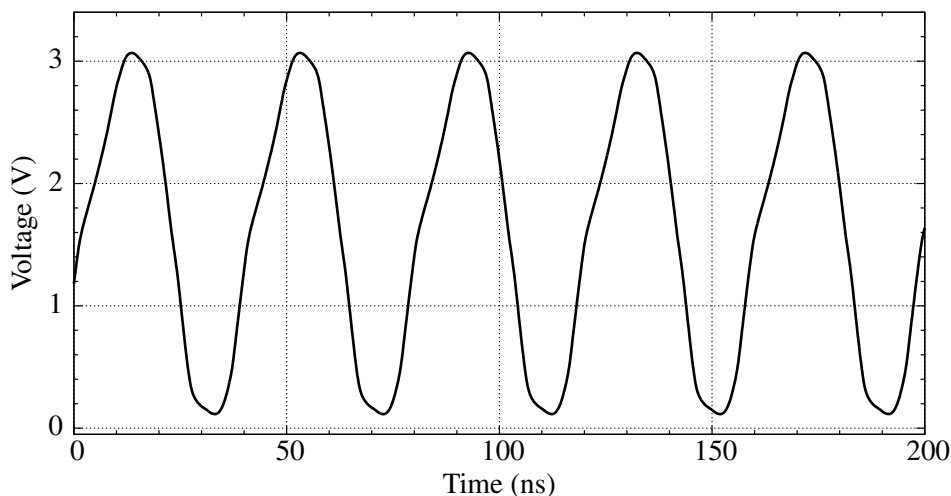
Figure 3.2: Simulation results of the current starved RO output waveform implemented in a 90 nm process, adjusted for 25 MHz.

The simulation results for the output waveform of the 90 nm implementation is shown in Fig. 3.2. An output buffer after the output is required to restore logic levels and ensure 50% duty cycle. The oscillator variation over process and temperature corners is shown in Fig. 3.3. The current starved RO exhibits a negative TC with around 30% worst corner frequency deviation. It should be noted that the process and temperature corner behaviour of the current starved oscillator can vary depending on the operating region, which is determined by the value of V_{CTRL}. Lower

voltages, which increase the oscillating frequency, result in lower TC and less deviation between the FF-SF and SS-FS corners. Increasing V_{CTRL} reduces the TC and leads to a more evenly spaced process corner behaviour.
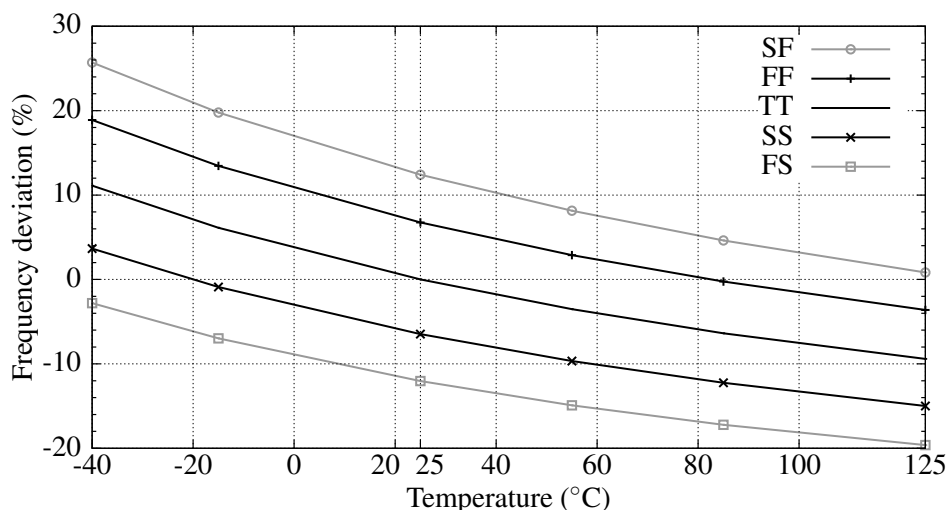
Figure 3.3: Simulation results for frequency deviation of the current starved RO over process (foundry A 90 nm) and temperature corners.

If a certain operating region is desired, the device sizing can be tuned so that the target frequency occurs for a V_{CTRL} voltage that sets the oscillator with that specific process and temperature corner behaviour. However, following this behaviour-driven design flow can result in a nominal V_{CTRL} voltage that is not optimal. The required control voltage may happen to be in the extremes of the oscillator tuning range, where frequency variations with V_{CTRL} are highly non-linear. A related scenario is that the resulting tuning range may end up being much larger than required, resulting in high sensitivity to V_{CTRL} variations, which may increase the compensation circuit design effort.

In order to avoid such issues, the chosen design flow targeted a reasonable tuning range, not higher than required for corner compensation. This results in the nominal control voltage being set roughly in the middle of the tuning range, where frequency variations with V_{CTRL} are linear.

The low component count, and low bias currents required for MHz operation (≈ 2–$4\,\mu A$), are reflected in the reduced power requirements for this topology. In table 3.1, the performance values for the current starved oscillator are shown.

Table 3.1: Performance of the current starved RO for various processes.

Process		Worst case ΔT_{osc} (%)	TC (%/°C)	Power (μW)
A	28 nm	33.86	-0.094	21.5
A	40 nm	38.82	-0.231	59.0
B	40 nm	35.53	-0.135	34.1
A	65 nm	31.20	-0.247	69.5
A	90 nm	25.70	-0.124	29.4
B	110 nm	40.02	-0.219	29.4

3.2   Differential delay cell ring oscillator
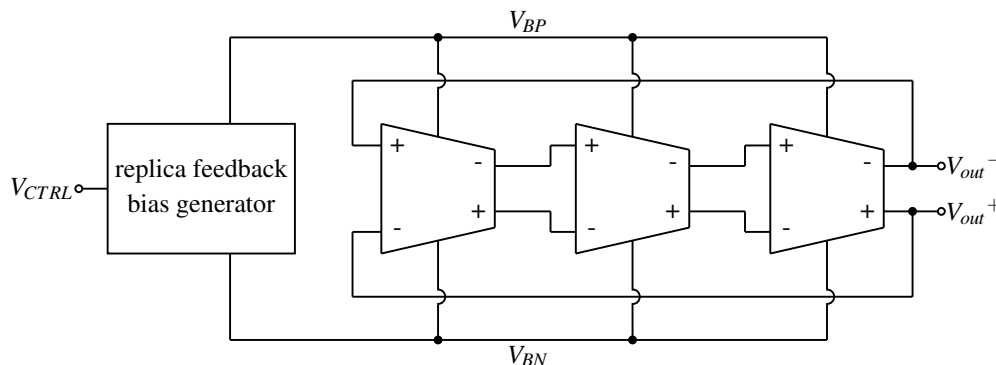
Figure 3.4: Schematic of the differential delay cell RO.

Another ring oscillator configuration uses differential delay stages, as shown in Fig. 3.4. Each delay cell is based on a coupled pair and symmetric load [15]. The delay cell is controlled by the bias voltage V_{BP}, which sets the output voltage swing, and V_{BN}, which controls the bias current I_{bias}, as shown in Fig. 3.5. These voltages are dynamically generated through a replica feedback block [15, 28]. This circuit ensures the bias voltage V_{BP} tracks V_{CTRL}, and also generates V_{BN}. The oscillation period is defined by

$$T_{osc} = \frac{(V_{DD} - V_{CTRL}) \, N \, C_{eff}}{I_{bias}(V_{CTRL})} \tag{3.2}$$

where C_{eff} is the effective load capacitance at the output of each stage, N is the number of delay cells in the chain, and I_{bias} is the delay cell bias current (Fig. 3.5).
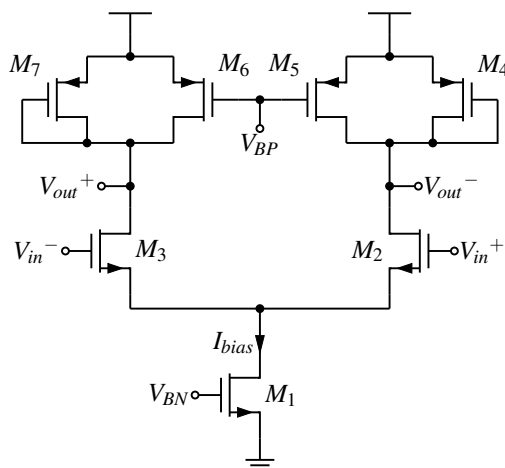
Figure 3.5: Schematic of the differential delay cell.

The replica feedback generator consists of a half-buffer replica (M_1–M_4) and amplifier to generate V_{BN}, and buffer to isolate V_{BP} from V_{CTRL}. This circuit is shown in Fig. 3.6. It should be noted that the operational amplifier used in the replica bias generator was not implemented, and an ideal

block used instead. However, the behaviour of the amplifier should not considerably affect the operating principle of the circuit.
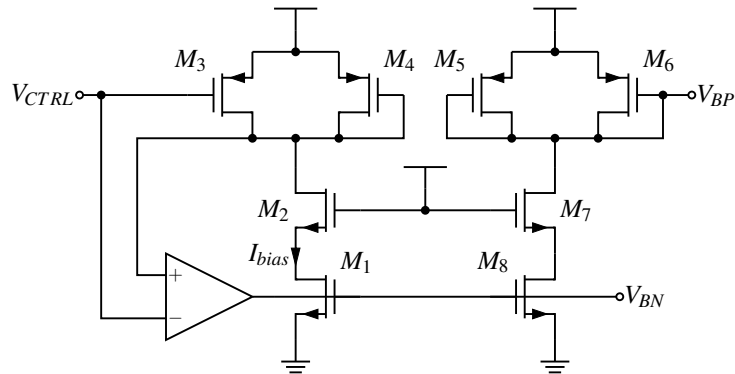
Figure 3.6: Schematic of the replica bias generator.

In Fig. 3.7 the simulation results for a 90 nm process implementation output waveform are shown. The output of the oscillator is not rail-to-rail, since the output swing is defined by V_{CTRL}, and as such it requires an output buffer to restore the voltage to adequate levels.
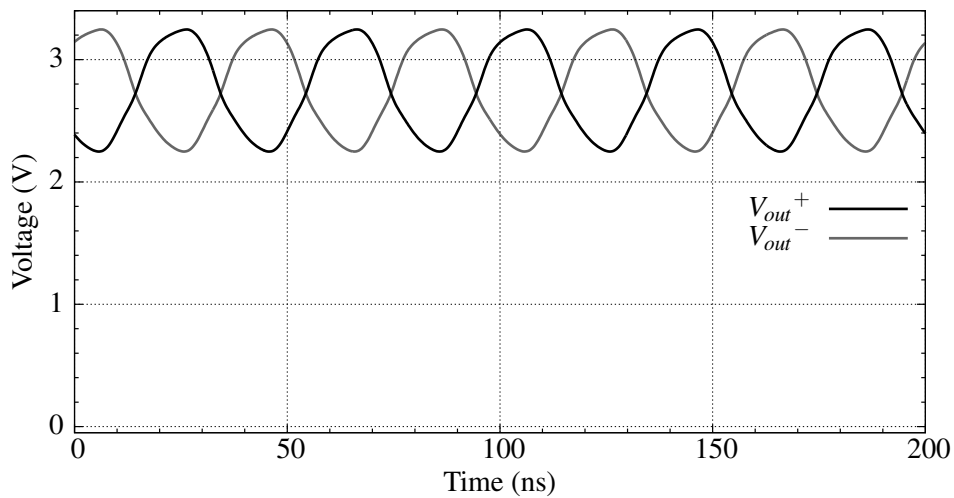
Figure 3.7: Simulation results of the differential delay cell RO output waveform implemented in a 90 nm process, adjusted for 25 MHz.

The behaviour over process and temperature corners is shown in Fig. 3.8, and exhibits a positive TC and increased sensitivity to PMOS corners (small deviation between FF-SF and FS-SS corners). Similarly to the previous topology, process and temperature behaviour can change considerably depending on the operating region, with TC decreasing to negative values for lower control voltages (higher frequencies). The design flow followed a slightly different design approach. Where previously the target was a tuning range adequate for the desired output frequency and required compensation, for this topology the circuit was tuned so that the nominal V_{CTRL} falls in a higher voltage range.

The reason for this design choice was due to power consumption. Higher control voltages increase power requirements considerably, both due to the differential nature of the design, as well as the replica bias generator. In table 3.3, the performance values for the differential delay cell RO are shown.
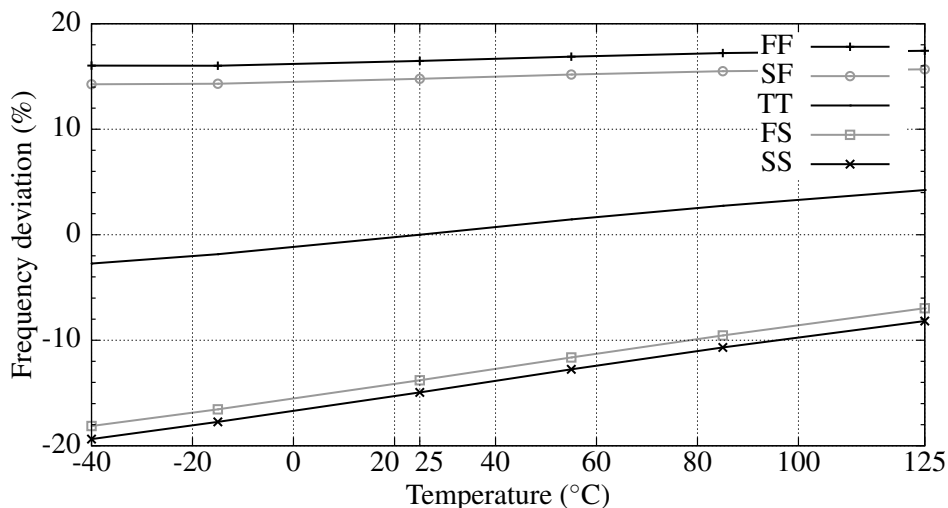
Figure 3.8: Simulation results for frequency deviation of the differential delay cell RO over process (foundry A 90 nm) and temperature corners.

Table 3.2: Performance of the differential delay cell RO for various processes.

Process		Worst case ΔT_{osc} (%)	TC (%/°C)	Power (µW)
A	28 nm	111.3	0.528	23.1
A	40 nm	46.21	0.187	70.4
B	40 nm	-39.69	0.114	92.5
A	65 nm	-46.84	0.175	99.3
A	90 nm	-19.37	0.042	114
B	110 nm	38.01	0.026	92.6

3.3 High-performance VCO

The high-performance VCO is another variation of the ring oscillator topology [29] that introduces two delay cells in the inverter chain, as shown in Fig. 3.9. Each delay cell consists of a PMOS transistor in series with the signal, and a NMOS transistor connected to ground. The control voltages V_{CTRL} and V_{PLAGE} are used to adjust the delay. Due to the PMOS in series, this delay cell has a greater influence on the falling edge, with the rising edge remaining mostly unchanged. To maximize the influence of the delay cell, the inverter that follows must have a low commutation point. This is realized by doubling the width of the inverter NMOS transistor. Moreover, as high V_{CTRL} voltages increase the delay, the falling transition may be slow enough that the following inverter will operate in linear mode most of the time. This severely increases power consumption,
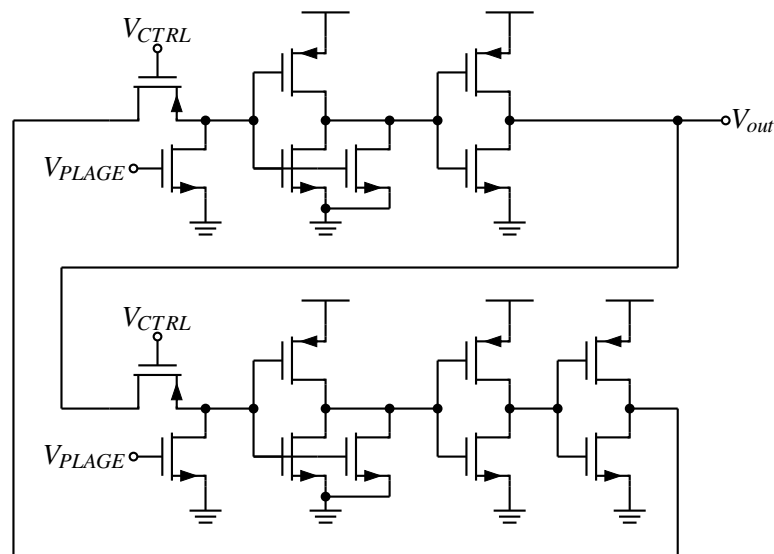
Figure 3.9: Schematic of the high-performance VCO.

and further reinforces the need for a low commutation point inverter. In order to introduce delay on both rising and falling edges, cells are positioned after an odd and even number of inverters. Since these delay cells introduce a much greater delay than the otherwise fast inverters, the output signal has fast transitions and is near rail-to-rail, as seen on Fig. 3.10.
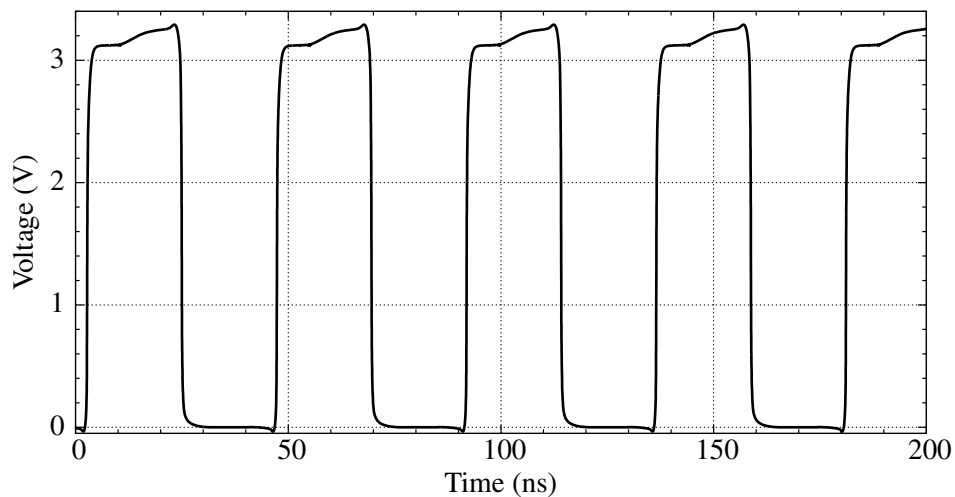
Figure 3.10: Simulation results of the high-performance VCO output waveform implemented in a 90 nm process, adjusted for 25 MHz.

The design flow for this topology assumes a fixed V_{PLAGE} voltage, thus using V_{CTRL} as the frequency tuning voltage. Similarly to the current starved oscillator, the design flow aimed for a balanced frequency tuning range with a nominal V_{CTRL} falling in the linear control region.

However, unlike previous designs, process and temperature behaviour do not show such a strong dependence on control voltage. This is due to the fact that V_{CTRL} (and V_{PLAGE}) only sets the

operation of the delay cell, which is part of a chain that is otherwise not subject to external control. Nonetheless, process-specific restrictions and behaviours can lead to design tuning resulting in exceptional variation over corners. This was the case for the 28 nm node implementation, where restrictions on transistor length resulted in high inverter oscillating frequency and required a non-optimal design tuning to achieve a 25 MHz nominal frequency.

Table 3.3 shows the worst case corner variation, TC, and power consumption from the simulation results in the processes where the oscillator was implemented.
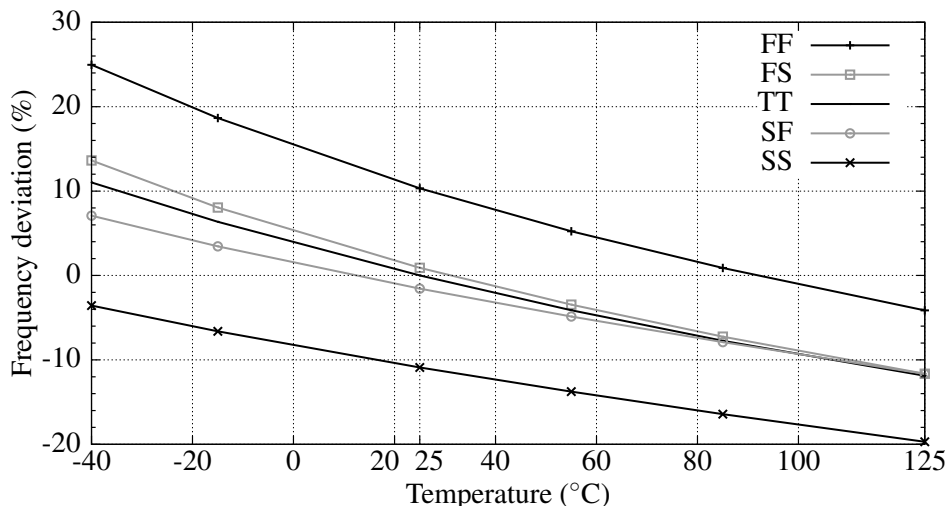
Figure 3.11: Simulation results for frequency deviation of the high-performance VCO over process (foundry A 90 nm) and temperature corners.

Table 3.3: Performance of the high-performance VCO for various processes.

Process		Worst case ΔT_{osc} (%)	TC (%/°C)	Power (µW)
A	28 nm	121.8	0.635	67
A	40 nm	32.92	-0.204	145
B	40 nm	34.00	-0.232	70
A	65 nm	35.77	-0.263	152
A	90 nm	24.96	-0.139	58
B	110 nm	53.37	-0.212	55

3.4   Relaxation oscillator

The relaxation oscillator is based on the repetitive charge of a capacitor, and then discharging it once it reaches a certain threshold level. It comprises a timing circuit, comparator block, and SR latch, as shown in Fig. 3.12. The timing circuit charges a capacitor with a constant current I_{REF}, which can be adjusted with V_{CTRL}. The current I_{REF} will charge one of the capacitors, e.g. C_1, resulting a linearly increasing voltage V_{ramp1} at its positive terminal. This voltage feeds into the comparator, which will trigger when it reaches the threshold voltage V_{REF}. The comparator output
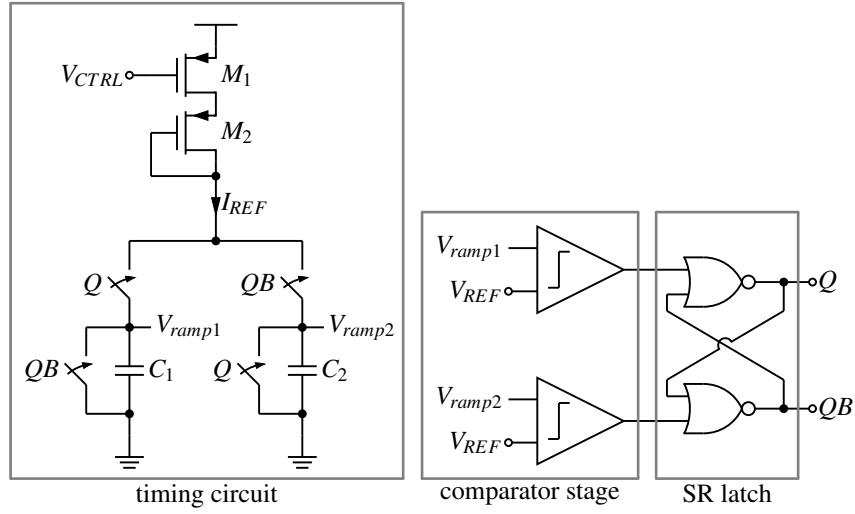
Figure 3.12: Schematic of the relaxation oscillator.

will reset the SR latch, setting voltage QB to high and Q to low. This changes the switching configuration to discharge C_1, and charge C_2 with I_{REF}. The same sequence happens for C_2, and then the cycle repeats.

This generates a constant frequency at the SR latch output that, in an ideal system, depends only on the time the capacitor takes to reach V_{REF}. Taking into account the delay D_{tot} introduced by the comparator and latch, the oscillation period is given by

$$T_{osc} = 2\frac{C\,V_{REF}}{I_{REF}} + 2D_{tot} \tag{3.3}$$

Whereas the delay of a typical SR latch is negligible at oscillation frequencies in the *MHz* range, the comparator can introduce a bigger effect. The delay introduced by the comparator itself is not an issue, as the oscillator can be tuned to the desired nominal frequency. However, the higher the delay, the higher the oscillation frequency will depend on the stability of the comparator over the PVT corners.

The comparator design was based on [30] and is comprised of two stages. In the first stage V_{REF} sets a bias current in M_4 that is mirrored to M_3 and M_1 via M_2. The drain node of $M3$ (V_{fast}) is the output of the first stage. On the second stage, transistors M_5–M_8 are a replica of the output stage (M_9–M_{12}). The purpose of this replica is to bias the output stage such that the decision threshold is set at V_{REF}.

The comparator exhibits a static power consumption that is highly dependent on the threshold voltage V_{REF}. This voltage sets the bias current in M_2 and M_4, as well as on the output stage replica realized by M_5–M_8.

The power consumption of the oscillator blocks also has a dependency on V_{REF}. In fact, lower voltages allow the use of a lower charging current I_{REF} or smaller capacitors to save area, while keeping the same frequency. However, at low values of V_{REF}, the fall time of the comparator after the capacitors are discharged becomes slower than the oscillation period, at which point the
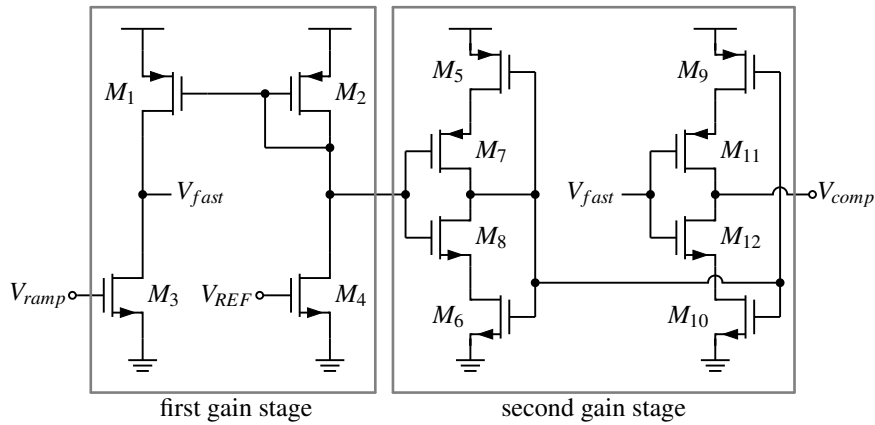
Figure 3.13: Schematic of the two-stage comparator.

oscillator stops. This is due to the bias current mirrored to M_3 being too small when V_{ramp} is low, such that V_{fast} rises too slowly.

In order to improve the comparator fall time, the comparator was modified and a reset circuit was implemented. This circuit sets V_{fast} to the supply voltage, and the comparator output ground, effectively bringing the comparator to a known state. It is comprised by simple logic (NOT and AND gates) and two transmission gates, as shown in Fig. 3.14. The switches are triggered when V_{ramp} is low (after capacitor discharge) and V_{comp} is high. Note that the NOT gate connecting to V_{ramp} should have a low commutation point, around V_{REF}. This is needed since the "high" condition of V_{comp} is close to the value of V_{REF}, and typically below half the supply voltage.

In Fig. 3.15 the comparator behaviour is shown with and without the reset circuit, with a voltage V_{REF} of 0.7 V and a supply voltage of 3.3 V. The result is a greatly reduced fall time, which allows the use of lower V_{REF} voltages in the oscillator. This yields a considerable decrease in the power consumption of the comparator by a factor of approximately 2–3, depending on the process.

The capacitors were implemented using the gate capacitance of an array of square PMOS
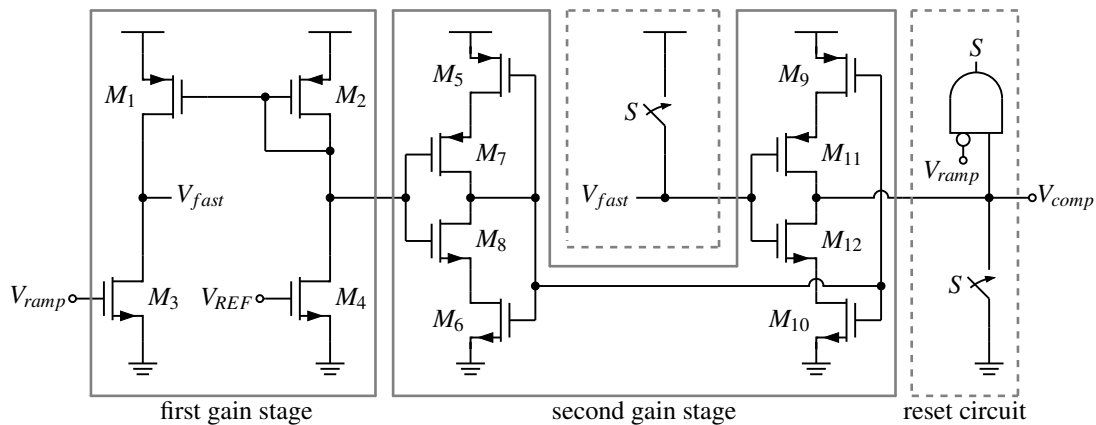
Figure 3.14: Schematic of the modified two-stage comparator for low V_{REF} operation.
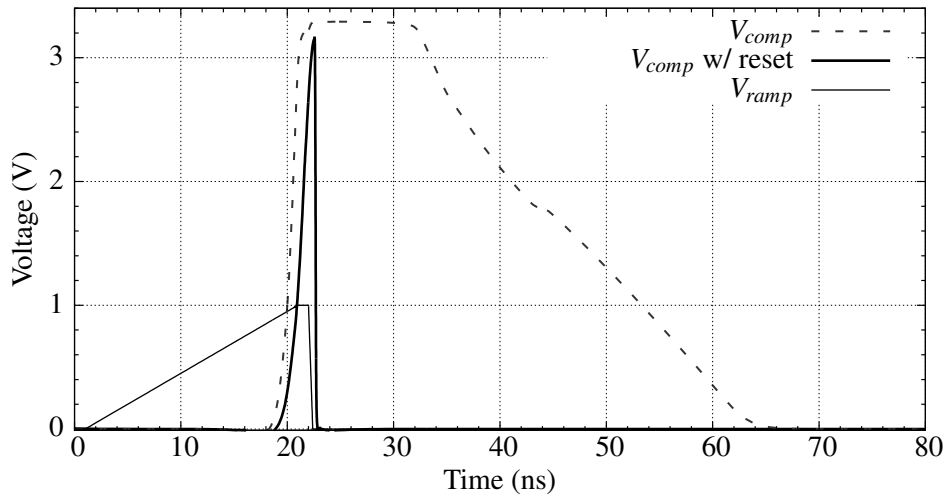
Figure 3.15: Comparator output behaviour at low V_{REF} operation (0.7 V) with and without the added reset circuit.

transistors (gate as negative terminal, source and drain shorted as positive terminal). A basic current source (M_1 and M_2) is used to provide I_{REF} from the control voltage V_{CTRL}. Taking (3.3) and assuming V_{REF} and V_{CTRL} are stable voltage sources, the frequency deviation depends on the comparator delay and capacitor variations, as well as variations in M_1 and M_2 which will affect I_{REF}.

The impact of the comparator and capacitors can be somewhat minimized, since they exhibit opposite behaviour in process and temperature corners. Furthermore, the amount of variation over these corners also changes with the value of V_{REF}. Thus, V_{REF} can be tuned so that the corner behaviour of the comparator and capacitors cancel each other. This allows for a degree of freedom when optimizing for PVT insensitivity, potentially at the cost of higher power consumption.

The oscillator output at 25 MHz is shown in Fig. 3.16. The use of an SR latch results in a square output and the symmetrical nature of the system ensures the duty cycle is close to 50%.

The implementation of the relaxation oscillator follows a relatively simple design flow. The voltage V_{REF} is fixed at a low value to reduce power consumption, and the current source and capacitor values are then tuned so that an adequate tuning range is achieved.

The performance values for the oscillator are shown in table 3.4. Despite the efforts to minimize power requirements, the relaxation oscillator falls short of other designs in this metric. This is mainly due to the high static power consumption of the comparator.
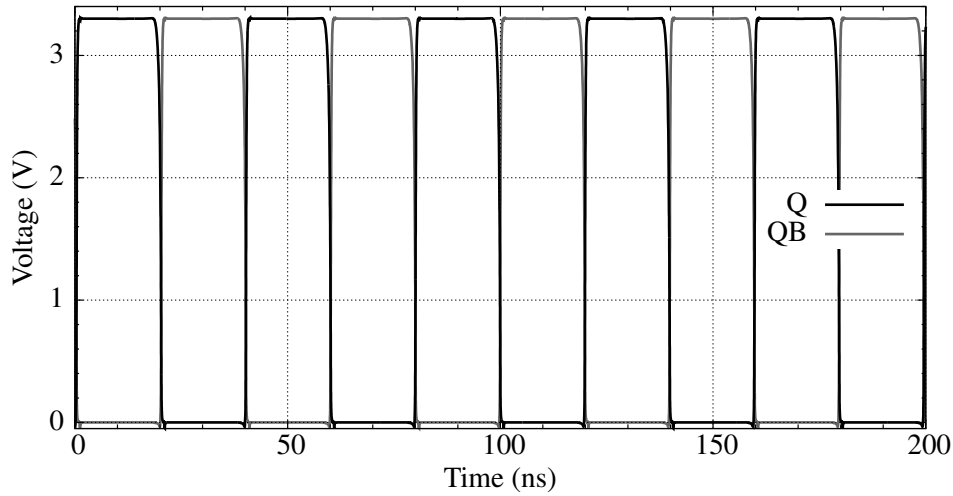
Figure 3.16: Simulation results of the relaxation oscillator output waveform implemented in a 90 nm process, adjusted for 25 MHz.
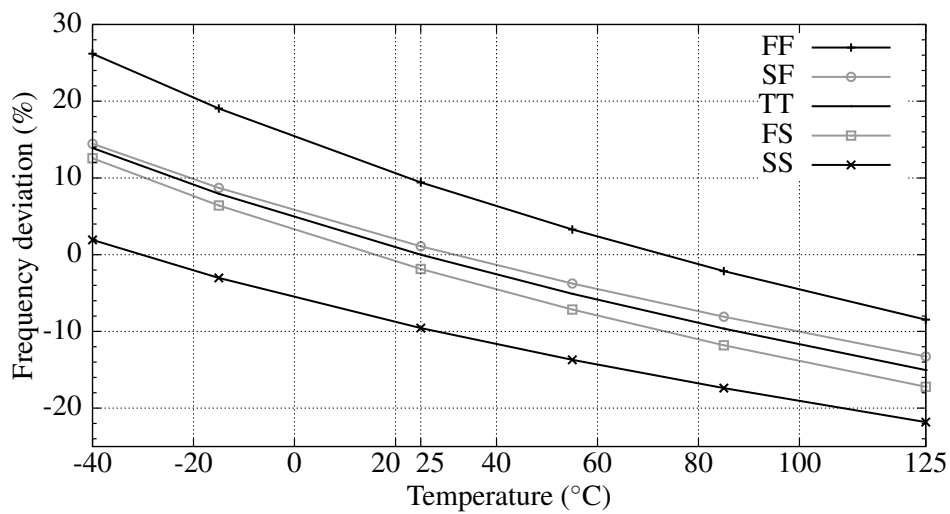
Figure 3.17: Simulation results for frequency deviation of the relaxation oscillator over process (foundry A 90 nm) and temperature corners.

Table 3.4: Performance of the relaxation oscillator for various processes.

Process		Worst case ΔT_{osc} (%)	TC (%/°C)	Power (µW)
A	28 nm	42.44	-0.201	45
A	40 nm	35.31	-0.207	264
B	40 nm	38.16	-0.279	228
A	65 nm	40.59	-0.289	295
A	90 nm	26.19	-0.175	196
B	110 nm	53.57	-0.248	309

3.5   Results overview

To provide a better perspective of how each oscillator performs in comparison, a selection of key metrics was used. These not only aim to characterize the oscillator performance, but also its suitability for integration in a PVT insensitive system.

Since the target of the oscillator block is to fit in a compensation system, the frequency stability over process and temperature corners is an important factor. The compensation system aims to provide an acceptable degree of stability regardless of the variation of the oscillator. However, if the variation is low, the effort on the compensation block also decreases, which maximizes the effectiveness of the system. The linearity of the frequency variation over corners and V_{CTRL} is important as well. The complexity of the compensation system increases considerably if it must compensate in a non-linear manner over process and temperature corners. This is specially important in open-loop systems, where the compensation block must realize a function that pre-distorts the control voltage in order to cancel variations.

The frequency variation over process corners is considerably different for each architecture. The current starved RO shows an evenly spaced change in frequency from one corner to the other. However, it experiences a greater deviation for the skewed corners (SF and FS), than for SS and FF corners. Other architectures show different behaviours, with some corners introducing very little variation. The differential delay cell RO exhibits small variations between the slow and fast NMOS corners – FF-SF and SS-FS. This reveals a strong dependency on the PMOS behaviour. The relaxation oscillator and high-performance VCO show similar behaviours, where the frequency deviation is maximum in the SS and FF corners, but considerably lower for the FS and SF corners. This points to a situation where opposite variations in the PMOS and NMOS transistors cancel out.

Nonetheless, for some topologies, the behaviour over process and temperature can change depending on the operating range of the control voltage. This change in behaviour is process-specific, and is a consequence of the interaction of different PVT reactions by each circuit construct in the system, as first noted in chapter 1.

Regarding power consumption, the ring oscillator based designs require the least power, with the current starved oscillator showing the lowest power usage. The differential delay cell RO is based on a similar principle, but the use of a more complex bias generator, differential output and symmetric loads, result in higher power consumption. In the high-performance VCO, the use of a higher number of stages, free-running inverters, slow fall times due to the PMOS delay cell, result in a high dynamic power consumption. The relaxation oscillator shows the highest power consumption, due to the high static power requirement of the comparators.

It should be noted that although there are visible trends in the figures of merit for each oscillator, they are still highly process dependent and exceptional behaviours can be observed in certain process nodes.

Moreover, there is room for further optimization for each architecture and process node. Detailed analysis of PMOS and NMOS dependence for each oscillator could lead to a more optimal

tuning of the circuit, resulting in more linear behaviour over process corners. The same methodology could also be applied to temperature variations. Such an analysis could be also performed for each oscillator block, to better understand if certain adjustments lead to the cancellation of variation between blocks. An example of this is given for the relaxation oscillator in section 3.4, where the comparator and PMOS capacitor exhibit opposite variations with process and temperature corners.

Chapter 4

Compensation Circuits

This chapter presents an analysis on selected compensation circuits and their performance when paired with an oscillator. As described in chapter 2, the most common PVT compensation circuits can be categorized as open or closed-loop architectures.

A closed-loop architecture takes a straightforward approach to PVT compensation, where the system is aware of variations and acts accordingly. The output signal feeds back to a compensation block that senses the frequency deviation and corrects the oscillator control voltage, eventually converging to a stable reference value. However, one of the challenges of closed-loop compensation architectures is the realization of the sensing block that translates the output frequency into a more easily comparable quantity, such as voltage. Typical frequency-to-voltage sensors rely on current integration into a capacitor during the pulse width of the oscillator output. As such, to ensure that the frequency sensor remains accurate, both the capacitance and current must be accurate and stable. In other words, the design of a reliable frequency-to-voltage sensor requires the use of a PVT insensitive current reference as well as a stable capacitance, of which neither is trivial to implement. Moreover, the feedback loop of such topologies can add a considerable circuit and power overhead, as well as stability issues.

This section focuses on open-loop topologies, which require less additional blocks to perform PVT compensation. However, they are not without design challenges. The effort shifts from realizing a PVT insensitive frequency sensing circuit, to a PVT sensitive control block that generates the required voltage to keep the oscillation frequency constant. This control block is effectively performing a pre-distortion of the control signal across PVT variations, opposing the frequency deviation. As such, the circuit needs to be tuned for the specific frequency variation of the oscillator. This tuning process can require considerable effort in order to match the compensation block to the oscillator, specially if the tuning points are not orthogonal. Thus, a robust design flow and implementation of orthogonal process, voltage and temperature compensation, are key factors in streamlining the realization of PVT insensitive oscillators based on open-loop topologies.

In this chapter two different circuits are studied, named conventional and quasi-orthogonal. The conventional circuit is based on previous work by Sundaresan *et al.*, for which a new tuning methodology is presented. The quasi-orthogonal circuit is a new contribution introduced in this

work, focusing on independent temperature and process compensation.

Since open-loop topologies are tuned to a particular oscillator, two architectures were chosen from chapter 3 to integrate with the compensation circuit. The most fitting designs are the current starved RO and the differential delay cell RO, which exhibit the lowest process variation and power requirements from all tested oscillators.

An assumption is made that compensation of supply variations is done by the use of a voltage reference, and thus it is not covered in this chapter. Nonetheless, the compensation circuits and oscillators used in this analysis are implemented in a 90 nm process from foundry A, using a 2.2 V supply voltage to account for the drop introduced by a typical voltage reference.
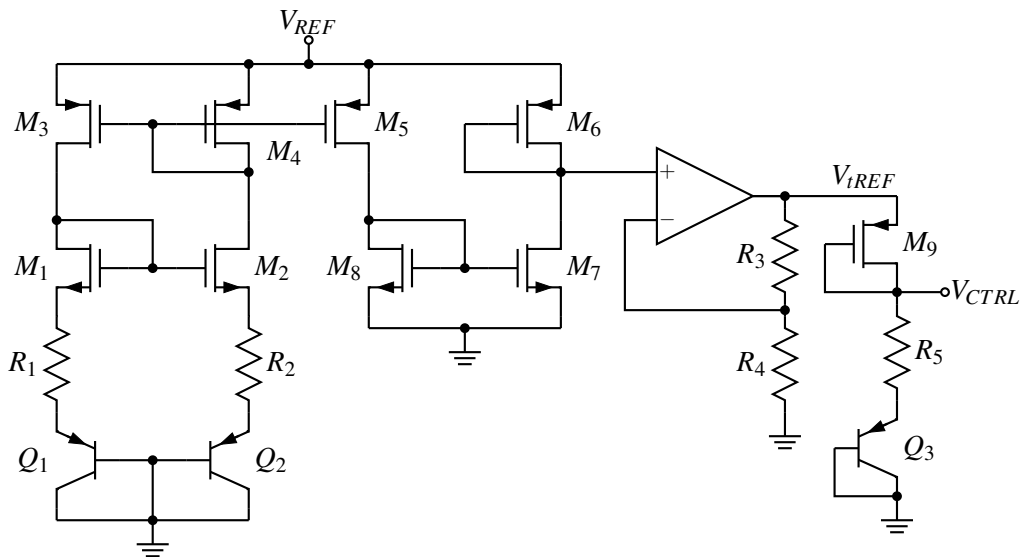
4.1 Conventional compensation

Figure 4.1: Schematic of the conventional compensation circuit.

The conventional TPC circuit shown in Fig. 4.1 is based on the work by Sundaresan *et al.* [11]. It comprises a current source, process sensor, followed by a gain stage that feeds into a thermal compensation circuit. The current source is tuned to provide a temperature-insensitive current that is mirrored to bias the process sensor M_6. The transistor M_6 output is boosted by an amplifier to V_{tREF} with the gain of the feedback loop formed by R_3 and R_4. This process-dependent voltage is applied to a temperature compensation circuit, with a TC that can be adjusted by R_5 and M_9. However, tuning of the variation across process corners is also required so that the control voltage V_{CTRL} fits the required curves in order to compensate the oscillator. Moreover, the transistor M_9 also has influence on corner behaviour, and adjusting it for temperature slope matching can compromise optimal corner behaviour. The available tuning points of the circuit are in fact, not orthogonal, and the tuning process becomes an iterative process. This type of circuit is used in [11, 12, 16] to achieve generally good results ($\approx$ 2–4%), but lacks in providing a robust design flow in order to adjust the compensation circuit to the oscillator. Moreover, the implementations

in [11, 12, 16] do not account for the skewed process corners (FS and SF) during tuning, and are realized in $\geq 180\,\text{nm}$ process nodes, which are considered legacy by current standards and benefit from lower process variability [7].

In order to optimize this tuning process, a straightforward design flow and tuning algorithm was developed. This flow starts with a non-optimal initial solution as a starting point, and then focuses on two different tuning sections of the circuit, which are adjusted in sequence, iteratively, through an automatic process. The optimization algorithm relies on the assumption that although the tuning points are not orthogonal, they exert greater influence in some parameters than in others. In the conventional TPC circuit, the major tuning points are the size of the process sensor M_6, the V_{tREF} gain defined by R_3 and R_4, size of the transistor M_9, and resistor R_5. The process sensor size and V_{tREF} gain have a greater effect in the behaviour over process corners, where the size of M_9 and R_5 mostly influence the TC.

The first step consists in adjusting R_1 and R_2 in order to achieve a temperature independent current on M_5. This ensures that the biasing current of M_6 is temperature insensitive, minimizing the effect of the current source in the tuning process. The second step consists in finding an initial solution by a coarse tuning of the circuit through manual adjustment. With this initial solution, the tuning algorithm takes over and iteratively adjusts the circuit.
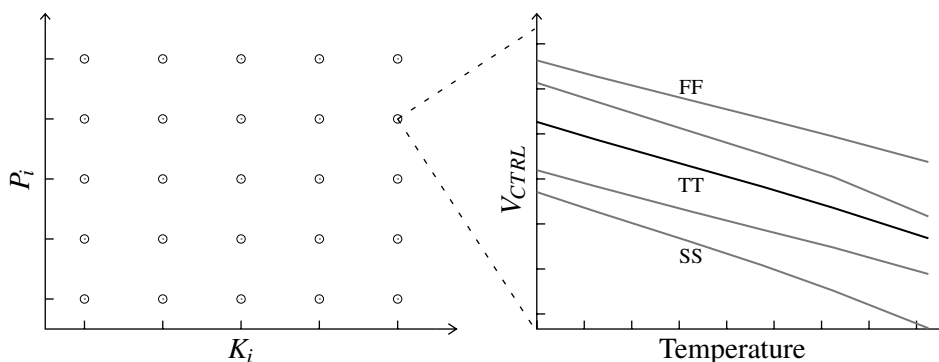

Figure 4.2: Representation of the bi-dimensional algorithm sweep space. The voltage V_{CTRL} over temperature, for each process corner, is determined for each value of (K_i, P_i).

The optimization algorithm works by performing parametric simulations on two variables (K_i, P_i) at a time. These variable pairs are the V_{tREF} gain and M_6 size – K_1 and P_1 – and R_5 and M_5 size – K_2 and P_2 – which have a greater influence on the circuit behaviour across process and temperature variations, respectively. In every parametric iteration the variable pair (K_i, P_i) is swept in a fixed range, and for each value of (K_i, P_i) in this bi-dimensional space, the V_{CTRL} voltage curves across temperature and process corners are obtained through circuit simulations. The results of these simulations, represented in Fig. 4.2, are then numerically processed. Each set of V_{CTRL} curves is compared to the curves required to optimally compensate the oscillator, and the mean squared error across the temperature range, for each process corner, is calculated. The maximum of the mean squared error over the process corners is stored.
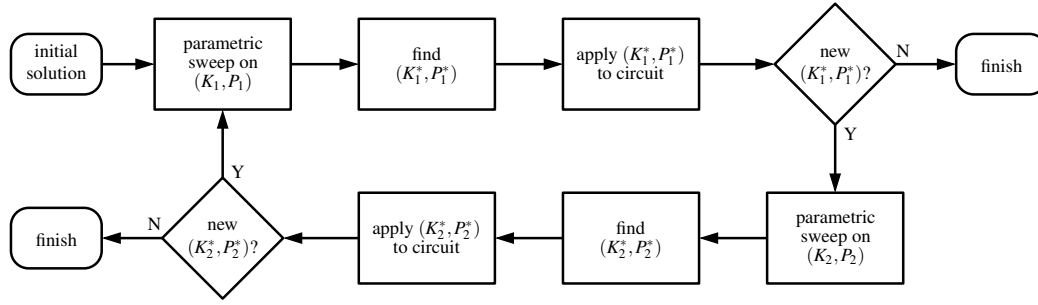
Figure 4.3: Optimization algorithm flow chart.

The result of each parametric iteration is a matrix containing, for every value of (K_i, P_i), the maximum of the mean squared error over temperature for any given corner. From this matrix the algorithm finds the minimum value, (K_i^*, P_i^*), for which the circuit best fits the optimal compensation curves across both process and temperature. Those values are then applied to the circuit, the algorithm re-iterates the parametric simulations for the second parameter pair, and repeats the process until there is no further change in the optimal values (K_1^*, P_1^*) and (K_2^*, P_2^*). A flow chart of the optimization algorithm is shown in Fig. 4.3.

The algorithm is implemented using shell scripts that execute the control flow. They are responsible for applying the tuning values to the circuit netlist, running the simulations, extracting results and triggering the numeric processing, and verifying if the stop condition is reached. The simulations are performed using the *Synopsys HSPICE* engine, and processing of the results is done with the *Mathworks MATLAB* numerical computing environment.

Using the developed design flow and optimization algorithm, the conventional compensation circuit was applied to the current starved and differential delay cell RO architectures. The performance results for the oscillators with and without conventional compensation are shown in table 4.1. The simulations results for the conventional circuit include not only the MOS device corners, but also resistor and bipolar device variations. Parameter deviations in these devices can have a strong influence in the compensation effectiveness, as shown by the curve spreading in Fig. 4.4. A better fitting is obtained for the differential delay cell RO, which results in a 4.95% variation over corners, compared to 11.69% for the current starved architecture. The power overhead of the compensation circuit is around $\approx 50\,\mu\text{W}$, which is non-negligible and in the case of the current starved RO, the compensation circuit draws over 3 times the power of the oscillator itself.

One of the drawbacks of the proposed algorithm is that it has some dependence on the ini-

Table 4.1: Performance of the current starved and differential delay cell ROs with and without conventional compensation.

Oscillator	Compensation	Worst case ΔT_{osc} (%)	TC (%/°C)	Power (μW)
Current starved	None	22.59	-0.097	16
	Conventional	11.68	0.020	71
Differential delay cell	None	18.12	-0.025	105
	Conventional	4.95	-0.008	159

tial solution since it does not cover every single possible combination of (K_1, K_2, P_1, P_2) – a four dimensional sweep – and as such it can converge to a local minimum. Nonetheless, even by testing every combination of all four variables, there is no guarantee that the error could be further minimized. The tuning points are non-orthogonal and thus solutions that reduce the error below a certain point may not exist at all, with the solution space being further restrained due to practical limitations in parameter values (voltage, resistance and transistor size). Moreover, the bipolar devices and resistor variations are not taken into account by the optimization algorithm due to computation time limitations, and would increase the final fitting error.
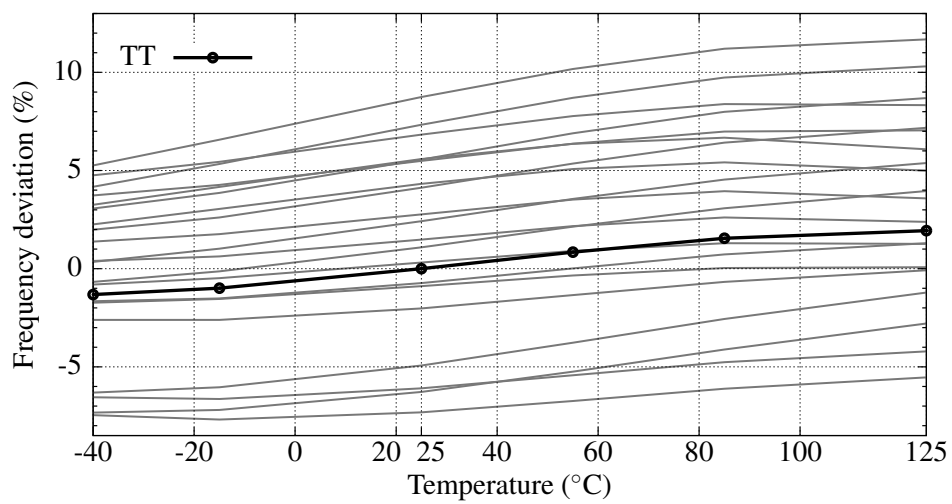
(a)
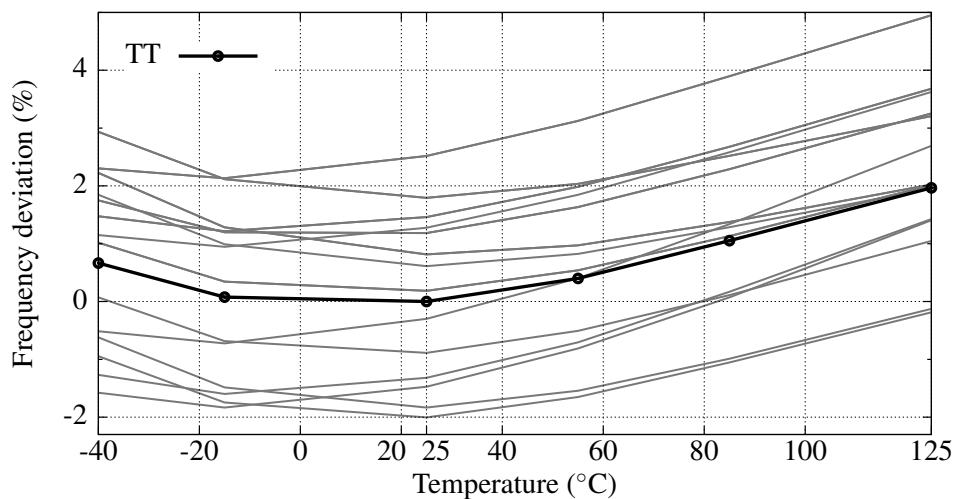
(b)

Figure 4.4: Simulation results of the (a) current starved and (b) differential delay cell ROs compensated by the conventional circuit across MOS, resistor and bipolar process corners.

4.2   Quasi-orthogonal compensation

The quasi-orthogonal compensation circuit is a new contribution, motivated by the problem of non-orthogonal temperature and process sensing. In most open-loop TPC circuits, the process sensing is performed as a first stage, as is the case with the conventional circuit studied in section 4.1. In order for such a circuit to work effectively, the next stages for temperature compensation must be process insensitive, to avoid compromising the process sensing output. This poses the challenge of realizing a temperature sensor that is able to combine the output of the process sensor without changing the behaviour over process corners, i.e. in an orthogonal manner.

One solution is to generate a temperature dependent signal as the first stage, and use a second stage to combine it with a process sensor. In fact, the generation of such a signal, can be realized with a CMOS current reference, which exhibits a PTAT behaviour [31]. The effort now shifts to realizing a process sensor whose output does not have a strong influence on the input TC.
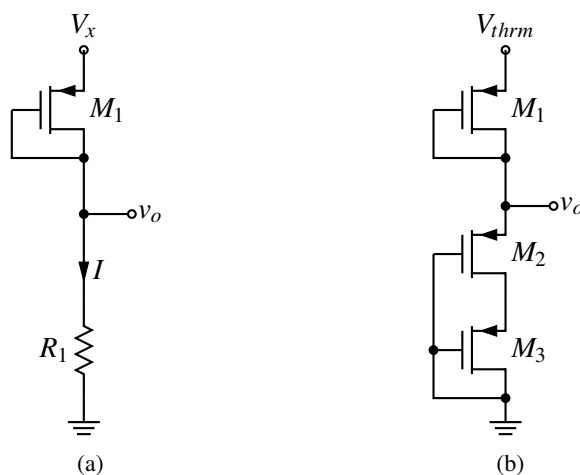
Figure 4.5: Schematic of an (a) ideal v_t sensor, and (b) the proposed quasi-orthogonal compensation circuit.

Let us consider the ideal v_t sensor circuit in Fig. 4.5(a), the output voltage v_o is given by

$$
\begin{aligned}
v_o &= V_x - v_{SG} \\
&= R_1 K (v_{SG} - |V_T|)^2
\end{aligned}
\tag{4.1}
$$

and if we solve for v_{SG}

$$
v_{SG} = |V_T| + \sqrt{\frac{v_o}{R_1 K}}
\tag{4.2}
$$

for $R_1 \gg 1/K$, (4.2) becomes

$$
v_{SG} \cong |V_T|
\tag{4.3}
$$

and thus the output voltage v_o is now

$$v_o \cong V_x - |V_T| \qquad (4.4)$$

Thus, the circuit in Fig. 4.5(a) effectively imposes a voltage drop on the input V_x equal to the threshold voltage V_T of the transistor, for large values of R_1. However, values of R_1 that make the above approximation true, are around $\approx 20\,\text{M}\Omega$. This becomes impractical to realize as an on-chip device due to the large area requirements.

In circuit Fig. 4.5(b), two PMOS transistors M_2 and M_3 are added instead of the resistor R_1, to form the quasi-orthogonal compensation circuit. The transistor M_2 has a small W/L and operates in the linear region, acting as a large resistance. To ensure M_2 stays in the linear region M_3 is added. This increases the drain voltage of M_2, and minimizes the influence over process corners. This circuit effectively subtracts the process dependent threshold voltage from the input. Moreover, it exhibits a constant process and temperature behaviour independently of the input voltage, as long as it is high enough that M_3 does not enter weak inversion mode ($V_{thrm} \gtrsim 3|V_T|$). Although it does not provide adjustable thermal compensation – as the TC of the circuit is quasi-constant over process and input voltage variations – it realizes an extremely flexible process sensor, that can be easily integrated in a compensation system. To form a complete TPC circuit, the quasi-orthogonal compensation must be used with a process-independent temperature sensor, thus creating a fully orthogonal compensation scheme.

To test the performance of the circuit it was coupled with an ideal temperature dependent supply as input, and an ideal amplifier with fractional gain to attenuate the output voltage to the required levels for oscillator compensation. Since the behaviour of the quasi-orthogonal circuit is near-constant across input and temperature variations, tuning of the circuit becomes a straightforward approach. The tuning points become the voltage and TC of the input, and the output gain. The performance figures for the current starved and differential delay cell ROs with quasi-orthogonal compensation are shown in table 4.2. Since the circuit is only comprised of PMOS devices, it is only subject to variations over MOS corners, shown in Fig. 4.6. The current starved RO is compensated within 6% of the nominal frequency, whereas the differential delay cell achieves a worst case deviation of 9.18%. One drawback of the circuit is the fixed behaviour over process corners, namely the distance of the FF and SS corners from the typical case, which in the tested oscillators limits the optimal V_{CTRL} curve fitting. This could potentially be mitigated by increasing the corner distance through the use of a positive output gain, followed by a negative offset to keep

Table 4.2: Performance of the current starved and differential delay cell ROs with and without quasi-orthogonal compensation.

Oscillator	Compensation	Worst case ΔT_{osc} (%)	TC (%/°C)	Power (μW)
Current starved	None	22.59	-0.097	16
	Quasi-orthogonal	-5.91	-0.001	16
Differential delay cell	None	18.12	-0.025	105
	Quasi-orthogonal	9.18	-0.0009	105

the nominal voltage at the required levels. Nonetheless, this compensation scheme adds a minimal circuit overhead and negligible power draw, typically below 1 µW.
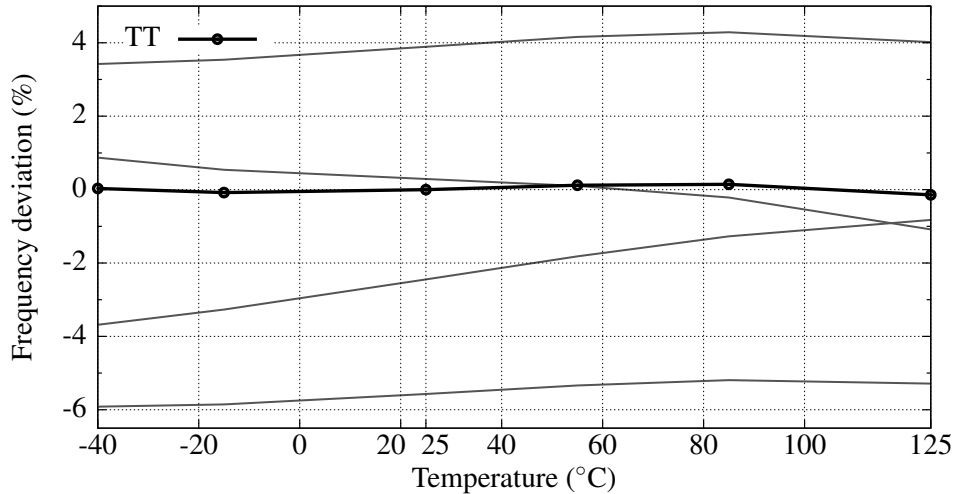
(a)
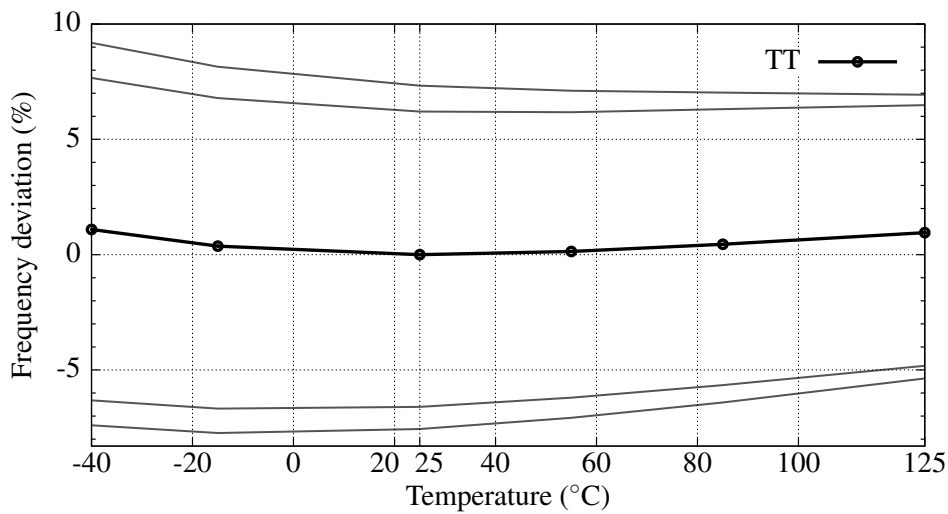
(b)

Figure 4.6: Simulation results of the (a) current starved and (b) differential delay cell ROs compensated by the quasi-orthogonal circuit across MOS process corners.

4.3 Results overview

In this chapter two approaches to practical open-loop compensation design were presented. For the conventional circuit, which provides a series of non-orthogonal adjustment points, a tuning algorithm was proposed to automate the optimization process.

Conversely, in section 4.2 a new orthogonal-by-design compensation circuit is presented, suitable for use as part of a TPC system where process, voltage, and temperature compensation is performed in an independent manner.

Both compensation circuits are able to improve PVT variations in the current starved and differential delay cell ROs. The conventional compensation circuit shows better fitting for the differential delay cell RO, while the quasi-orthogonal scheme yields better improvement in the current starved RO. However, the latter can be further optimized for other types of oscillators by applying separate offset and gain adjustments, thus allowing control over the distance between corners, as mentioned in the previous chapter.
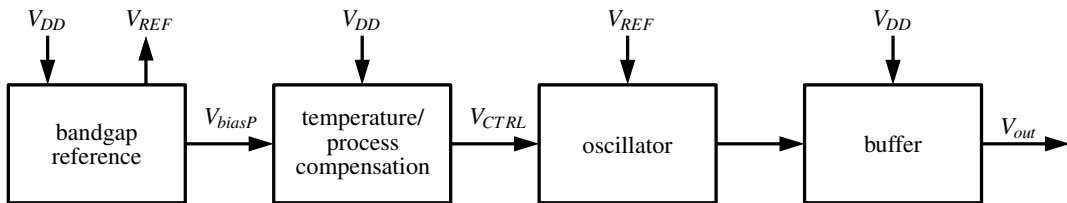
Chapter 5

Implementation

Figure 5.1: Block diagram of the implemented PVT insensitive oscillator.

This chapter presents the complete PVT insensitive oscillator implementation, taking from the blocks covered in the previous chapters. The system comprises a bandgap voltage reference, a temperature and process compensation circuit that generates the control voltage V_{CTRL}, the oscillator block, and an output buffer to drive the output frequency at the external supply levels.

The circuits were implemented in a 90 nm CMOS process from foundry A and simulated over MOS, resistor and bipolar corners to asses the worst case variation.

5.1   Bandgap voltage reference

To reduce the sensitivity of the circuit to fluctuations in the external supply voltage V_{DD}, a bandgap voltage reference is used [31], shown in Fig. 5.2. It exploits the opposing variations of a PTAT current generated from the difference in current densities of two p-n junctions and the complementary to absolute temperature (CTAT) voltage across these junctions. The temperature effects cancel on the first order, thus creating a stable voltage limited by the resistor matching.

The bandgap reference output is then buffered so that V_{REF} can be used as a PVT insensitive supply voltage for the oscillator block. Moreover, the PMOS bias voltage V_{biasP} is also used for biasing the TPC block. The amplifier used for output buffering comprises a differential pair gain stage with NMOS inputs, and a second gain stage to decrease output impedance, shown in Fig. 5.3. The amplifier used in bandgap reference to bias M_1 and M_2 is realized using only the differential pair gain stage also shown in Fig. 5.3.
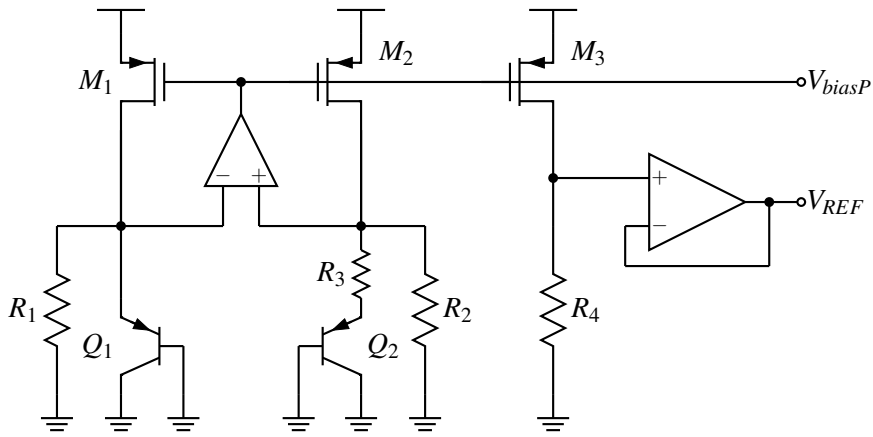
Figure 5.2: Schematic of the bandgap voltage reference.

The oscillator topologies covered in chapter 3, when implemented with thick gate transistors, require a supply voltage of at least $\approx 2.2\,\mathrm{V}$ to operate properly. Taking into account the voltage drop in the bandgap reference ($\approx |V_T|$), as well as a reasonable margin to account for external variations ($\approx 400\,\mathrm{mV}$), the system is tuned for a nominal external supply voltage of 2.9 V. In fact, the realized bandgap voltage reference keeps V_{REF} at 2.2 V for an external supply range of 2.5–3.3 V, across MOS, resistor, and bipolar process corners, as shown in Fig. 5.4.
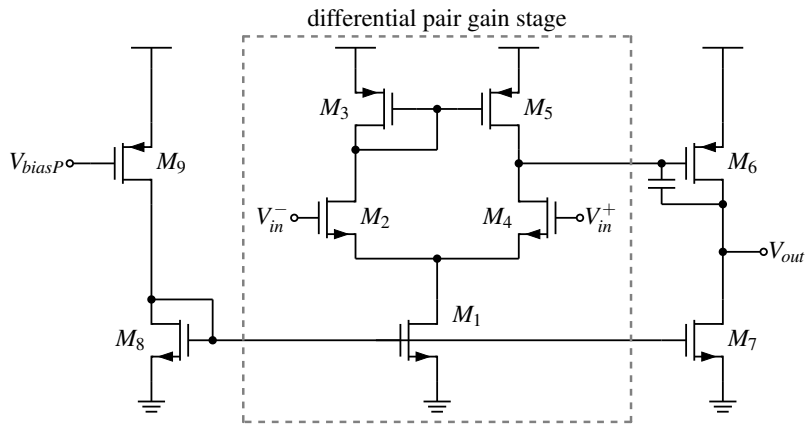

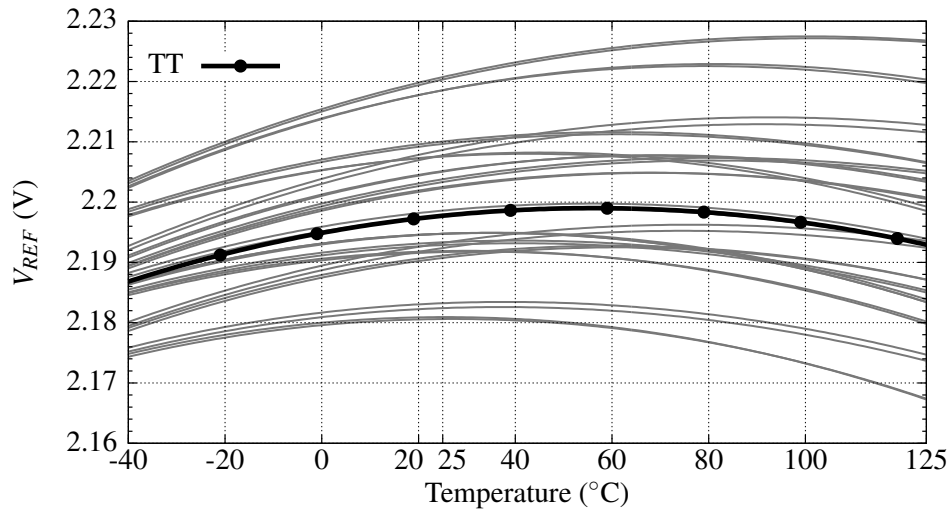Figure 5.3: Schematic of the operational amplifier.

Figure 5.4: Simulation results of the bandgap output voltage V_{REF} across supply and MOS, resistor and bipolar process corners.

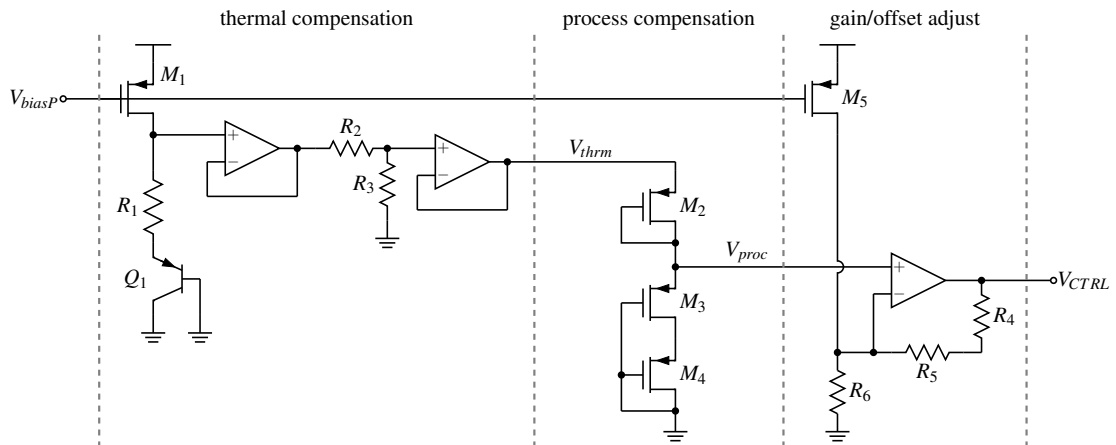## 5.2 Temperature and process compensation

Figure 5.5: Schematic of TPC circuit.

The temperature and process compensation circuit is based on thermal compensation stage, followed by a process sensor, and a final gain adjustment to set the nominal voltage to the required levels. In the first stage, a CTAT voltage is generated through current biasing of Q_1, with the output level defined by R_1. This voltage was set at 1.6 V to ensure correct operation of the following stage. This voltage is buffered to generate the V_{thrm} voltage that feeds into the next stage. The feedback resistors R_2 and R_3 can be used to attenuate the temperature dependent voltage, changing the TC as required. The process sensor stage uses the quasi-orthogonal compensation circuit introduced in chapter 4 , which imposes a voltage drop on V_{thrm} that is equal to the threshold voltage V_T. In the last stage, an amplifier isolates the process compensation stage output, and a feedback loop allows gain and offset adjustment to the required nominal level of V_{CTRL}.

To tune the TPC block for 25 MHz, a straightforward approach is taken, since the tuning points are nearly orthogonal. The value of R_1 and the amplifier gain in the thermal compensation stage are used to set the TC and nominal level of V_{thrm}, and the offset and gain of the output stage are tuned to the required V_{CTRL} levels.

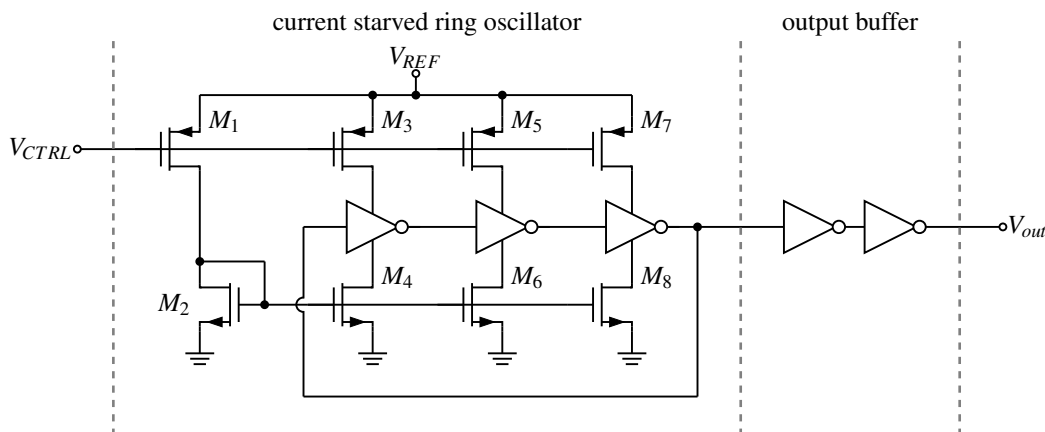## 5.3   Oscillator and output stage

Figure 5.6: Schematic of oscillator block and output buffer circuits.

The oscillator stage comprises a current starved ring oscillator controlled by the V_{CTRL} voltage generated in the TPC block. At the oscillator output a pair of inverters isolates the output signal and restores the voltage to V_{DD} levels.

5.4   Results

The final implementation of the circuit was simulated across MOS, resistor and bipolar process corners as well as temperature variations. Over a range of -40–125°C and across corner variations, the worst case frequency deviation is 5.5%, with an average power draw of 164 μW, for a nominal frequency of 24.8 MHz. The behaviour over temperature across is shown in Fig. 5.7 and the simulated output waveform in Fig. 5.8.

In table 5.1, a brief comparison with other PVT insensitive oscillators using open-loop compensation techniques is presented. When compared to other similar works, the proposed implementation targets a smaller process node, where greater process variability is expected, and realizes a fully self-sufficient system, including on-ship voltage supply. Furthermore, it achieves the lowest power consumption when compared with other works implementing on-chip supplies. It should also be noted that the experimental measurements are a more realistic metric of the typical process variation, where as a worst case corner measurement is a inherently pessimistic figure of merit.
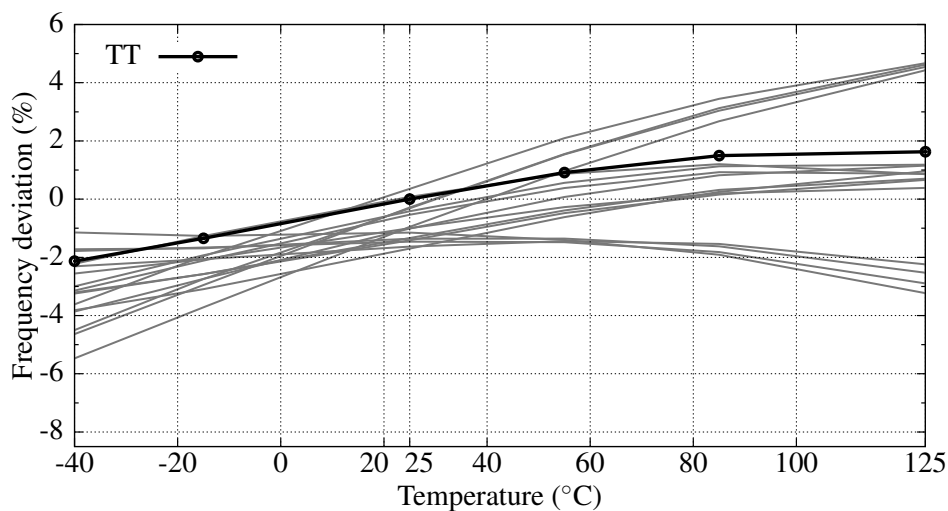
Figure 5.7: Simulation results of the compensated oscillator across MOS, resistor and bipolar process corners.
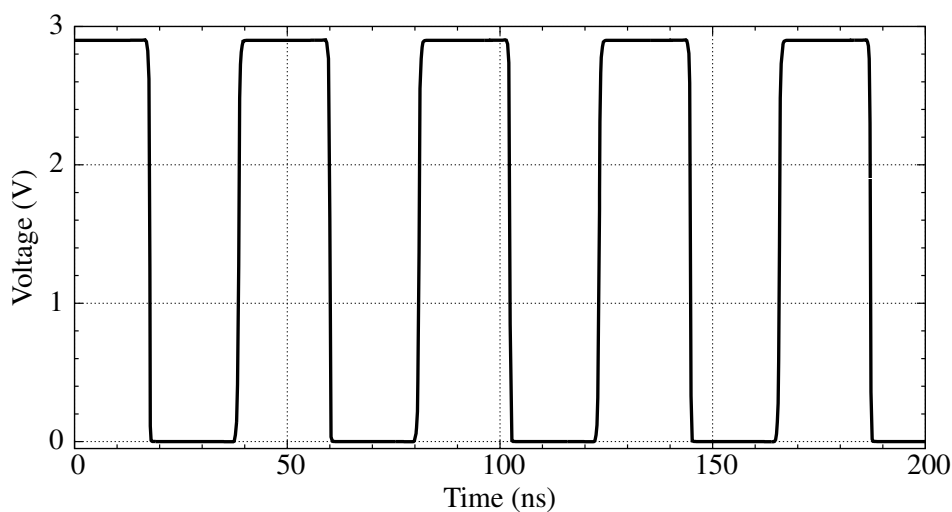
Figure 5.8: Simulation results of output waveform of the compensated oscillator.

Table 5.1: Comparison of open-loop PVT compensated oscillators.

Ref	Process	Frequency	Power	V_{DD} (V)	On-chip regulation	Accuracy (%)	Measurement
This work	90 nm	23.6 MHz	129 μW	2.5	Y	8.05	Worst case
[8]	0.6 μm	680 kHz	400 μW	4	N	4.7	Experimental
[11]	0.25 μm	7 MHz	1.5 mW	2.5	Y	2.64	Experimental
[12]	0.18 μm	150 MHz	537 μW	1.8	N	2.29	Worst case
[13]	0.18 μm	2 MHz	48 μW	1.8	Y	2.81	Experimental
[16]	0.18 μm	20 MHz	N/A	N/A	Y	2.98	Experimental

Chapter 6

Conclusions and Future Work

The design of a PVT insensitive oscillator, specially using open-loop compensation methods, requires the understanding of each block in the system and how it behaves over process and temperature corners. This becomes the key factor in the compensation scheme, as the compensation of the blocks requires the realization of a magnitude that opposes the circuit variation over PVT variations. Moreover, a further step is to tune each block not only for the conventional power-performance-area trade off, but also from a design for variability perspective. In other words, each design should be tuned as to lower the compensation effort.

In sum, this work provides a study on the key design considerations for the realization of PVT insensitive oscillators, and presents the following contributions:

- A study on the performance of oscillator topologies across process and temperature corners is presented. It comprises four oscillator architectures suitable for use with PVT compensation circuits, and includes circuit implementations in six process nodes from two foundries, ranging from 28 nm to 110 nm.

- Study of the TPC circuit proposed by Sundaresan *et al.* [11] and proposal of a new design flow, comprising an algorithm for automated circuit tuning and optimization. This proposed methodology is able to optimize the TPC circuit for different types of oscillators.

- A novel quasi-orthogonal process compensation circuit is proposed, based on the concept of systems comprising fully independent compensation for process, voltage, and temperature variations.

- Implementation of a fully integrated PVT compensated oscillator using a novel open-loop TPC circuit in a deep-submicron process node.

6.1 Future work

The next step in the realization process of the oscillator system would be the complete layout design in the proposed process node. This would allow the extraction of the parasitic devices to perform a post-layout simulation, thus validating the feasibility of the circuit for fabrication.

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With regards to the analysis of the oscillator blocks, a more comprehensive study on the behaviour of each oscillator topology could be performed, as was briefly stated in section 3.5. This could provide a better insight on how to tune each specific oscillator architecture from a design for variability perspective.

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